MASW-008206-000DIE

GaAs WLAN Dual SPDT Switch
2.4 - 5.8 GHz

Rev. V2

Features

- 802.11a & b/g, UNII, and Hiperlan Applications
- Optimized for 2.4 - 5.8 GHz WLAN
- Low Insertion Loss:
- 0.85 dB @ 2.4 GHz
- 1.1 dB @ 5.8 GHz
- High Isolation: 28 dB Typical
- Low Harmonics: <-63 dBc @ 20 dBm
- RoHS* Compliant

Description

M/A-COM's MASW-008206-000DIE is a WLAN GaAs PHEMT MMIC Dual SPDT switch. One SPDT (RF2) is optimized for 2.4 GHz WLAN and the other (RF5) is optimized for 5.8 GHz WLAN applications. Typical applications are for 802.11a and 802.11b/g PC card and access point applications.

The MASW-008206-000DIE delivers high isolation, low insertion loss, and high linearity up to 5.8 GHz. The MASW-008206-000DIE is fabricated using a 0.5 micron gate length GaAs pHEMT process. The process features full passivation for performance and reliability.

Ordering Information [1]

Part Number	Package
MASW-008206-000DIE	Separated Die on Grip Ring

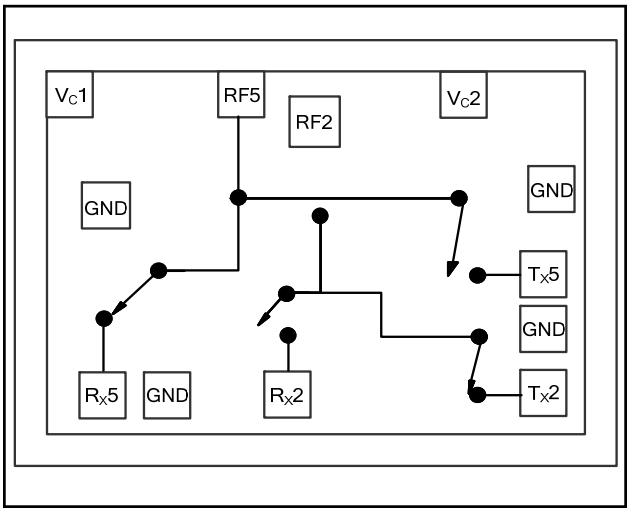
1. Die quantity varies.

Absolute Maximum Ratings [2,3]

Parameter	Absolute Maximum
Input Power @ 3 V Control	+32 dBm
Input Power @ 5 V Control	+33 dBm
Operating Voltage	+8 volts
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

2. Exceeding any one or combination of these limits may cause permanent damage to this device.
3. M/A-COM does not recommend sustained operation near these survivability limits.

Die Bond Pad Layout



Die Bond Pad Configuration

Pad No.	Name	Description
1	V_C1	Voltage Control 1
2	GND	Ground
3	R_X5	5 GHz R_X Port
4	GND	Ground
5	R_X2	2.4 GHz R_X Port
6	T_X2	2.4 GHz T_X Port
7	GND	Ground
8	T_X5	5 GHz T_X Port
9	GND	Ground
10	V_C2	Voltage Control 2
11	RF2	2.4 GHz Antenna Port
12	RF5	5 GHz Antenna Port

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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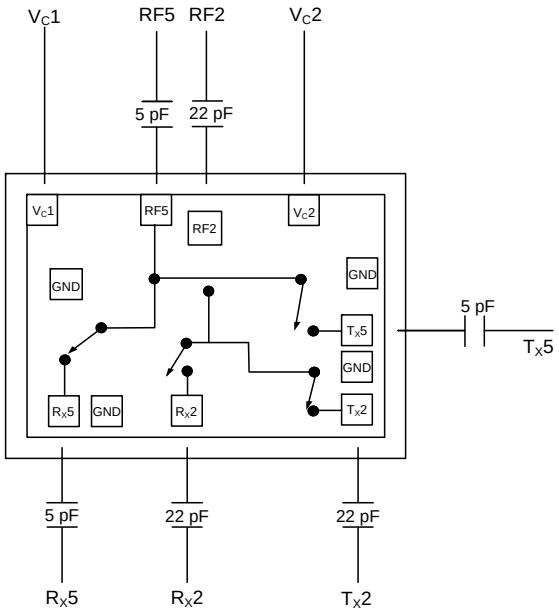
Electrical Specifications[4,5]: T_A = 25°C, Z_0 = 50 Ω, V_C = 0V / 3V, P_{IN} = 0 dBm

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	RF2 to Tx2/R_X2, 2.4 GHz RF5 to Tx5/Rx5, 5.0 GHz	dB dB	— —	0.85 1.1	1.0 1.2
Isolation	RF2 to Tx2/R_X2, 2.4 GHz RF5 to Tx5/Rx5, 5.0 GHz	dB dB	25.5 21.0	30.0 25.0	— —
Return Loss	DC - 6.0 GHz	dB	—	15	—
IP3	RF2 to Tx2/Rx2, 2.4 GHz, 20dBm Total Power, 1MHz Spacing RF5 to Tx5/Rx5, 4.9 GHz, 20dBm Total Power, 1MHz Spacing	dBm dBm	— —	54 55	— —
Input P1dB	RF2 to Tx2, 2.4-2.5 GHz RF5 to Tx5, 4.9-5.9 GHz	dBm dBm	— —	28 28	— —
Harmonics	RF2 to Tx2, 2.4-2.5 GHz, 20 dBc RF5 to Tx5, 4.9-5.9 GHz, 20 dBc	dBc dBc	— —	-63 -67	— —
Control Current	$\|V_C\|$ = 3 V	µA	—	<1	10.0
T_{RISE} / T_{FALL}	10% - 90% RF, 90% - 10% RF	nS	—	22	—
T_{ON} / T_{OFF}	50% Control - 90% RF, 50% Control - 10% RF	nS	—	30	—

4. External blocking capacitors on all RF ports.
5. Electrical min/max are guaranteed in die form only.

Application Schematic



RF2 to T_X2 and RF2 to R_X2 paths are optimized for 2.4 -2.5 GHz WLAN applications.

RF5 to T_X5 and RF5 to R_X5 paths are optimized for 4.8 - 6.0 GHz WLAN applications.

Truth Table [6,7,8]

Control V_C1	Control V_C2	RF2 - T_X2 RF5 - R_X5	RF2 - R_X2 RF5 - T_X5
1	0	On	Off
0	1	Off	On

6. For positive voltage control, external DC blocking capacitors are required on all RF ports.
7. Differential voltage, V (state 1) - V (state 0), must be +2.7 V minimum and must not exceed +5 V.
8. 0 = 0 ± 0.3 V, 1 = +2.7 V to +5 V.

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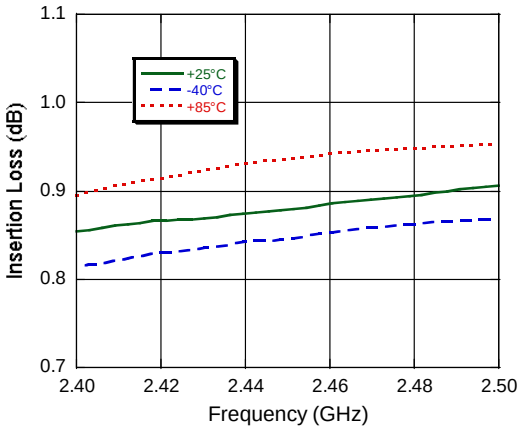
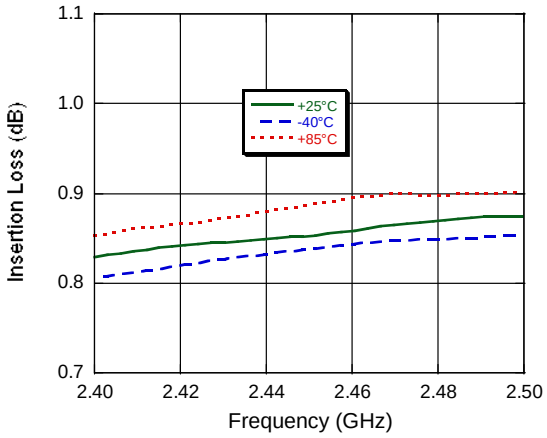
Typical Performance Curves: 2.4-2.5 GHz (plots = chip on board assembly)

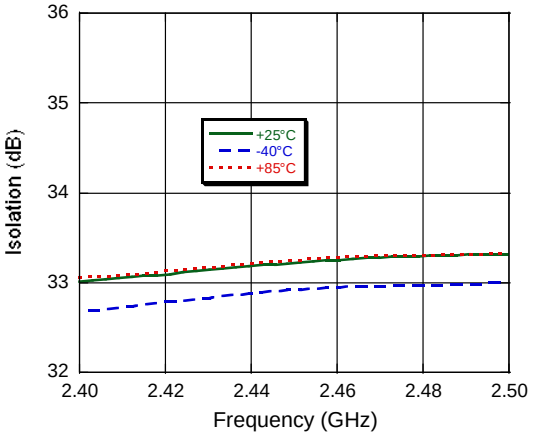
T_X Insertion Loss



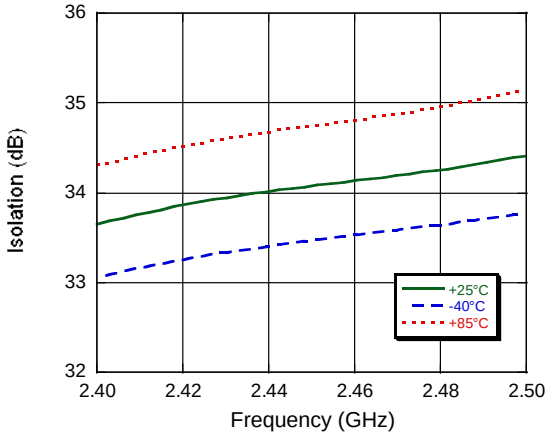
R_X Insertion Loss



T_X Isolation

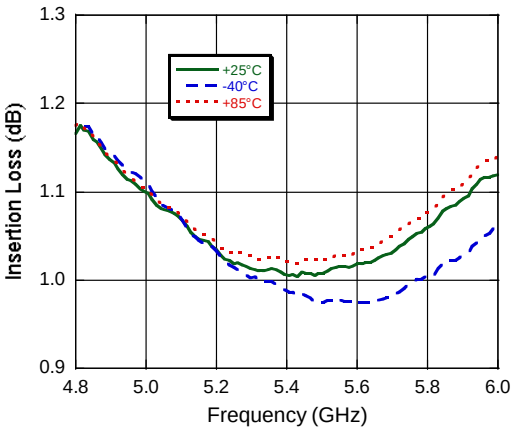


R_X Isolation

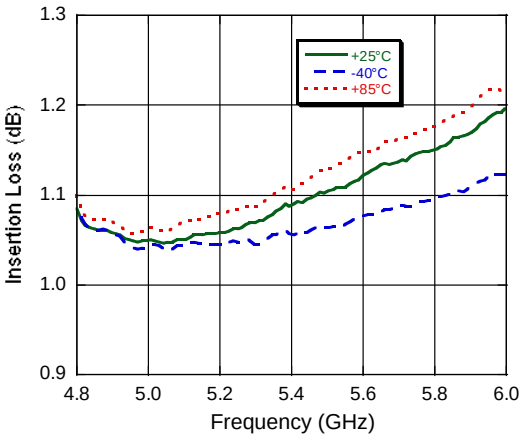


Typical Performance Curves: 4.8-6.0 GHz (plots = chip on board assembly)

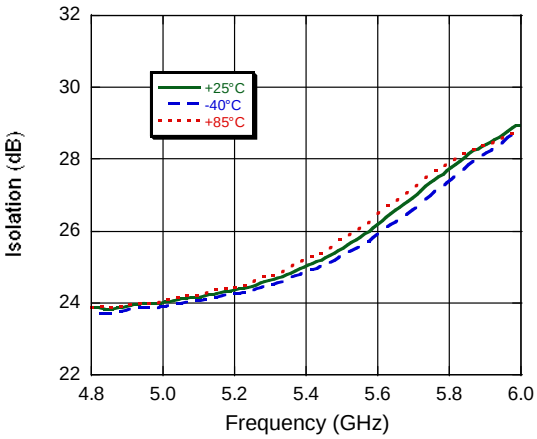
T_X Insertion Loss



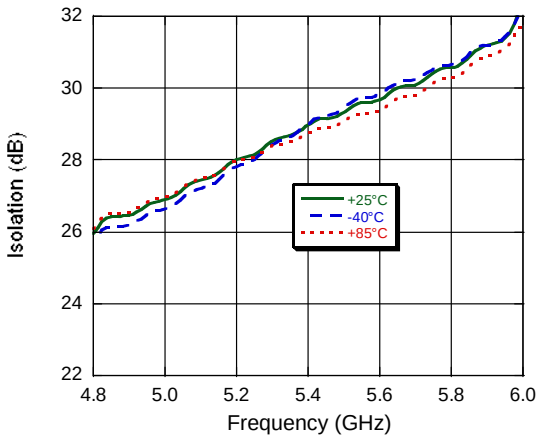
R_X Insertion Loss



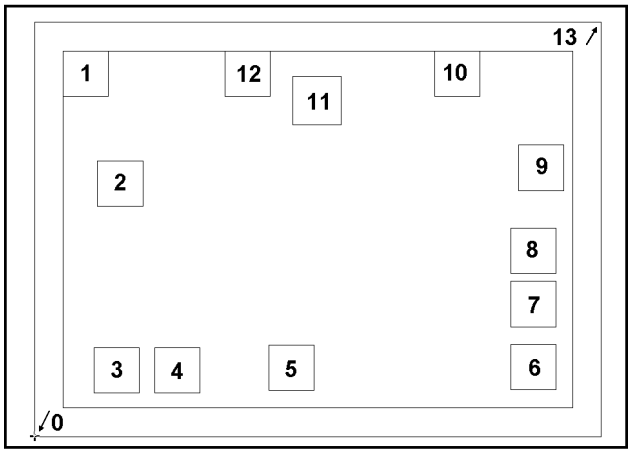
T_X Isolation



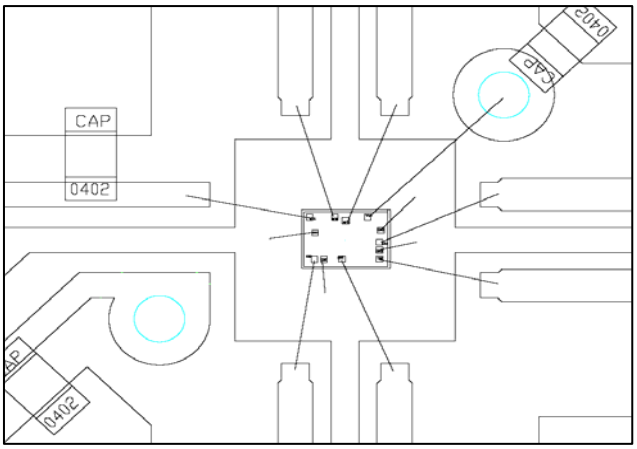
R_X Isolation



Outline Drawing



Chip mounted to PWB for testing purposes



Pad Configuration [8]

Die Size: 890 x 650 µm (nominal)

Pad No.	X (µm) nominal	Y (µm) nominal	Pad Size (µm)
0	0	0	Lower left edge of die
1	80.5	569.5	71 x 71
2	134.5	397	71 x 71
3	129	104	71 x 71
4	224	104	71 x 71
5	403.75	108	71 x 71
6	783.5	109	71 x 71
7	783.5	208	71 x 71
8	783.5	292	71 x 71
9	795.25	421.75	71 x 71
10	664	569.5	71 x 71
11	443	527	76 x 76
12	334.75	569.5	71 x 71
13	890	650	Upper right edge of die

8. All X,Y dimensions are at bond pad center.

Qualification

Qualified to M/A-COM specification REL-201, Process Flow –2.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling MASW-008206-000DIE, which are Class Zero (100 V) devices.

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