

PSRAM

4-Mbit (512K x 8)

Pseudo Static RAM

Features

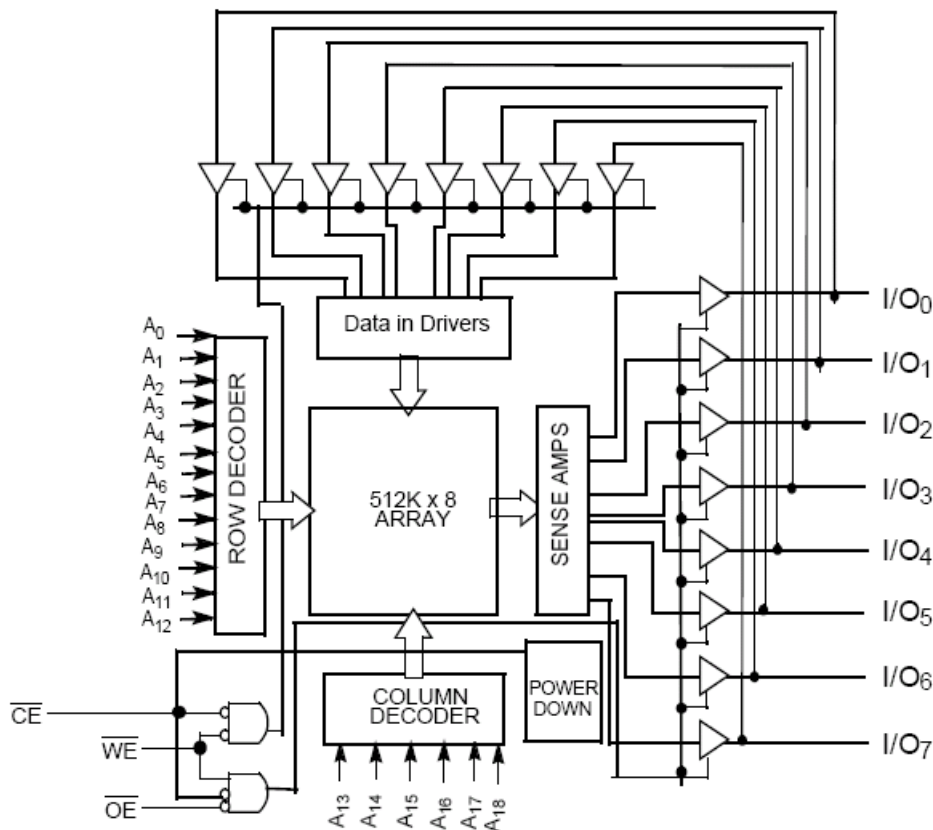
- Advanced low power architecture
- High speed: 55 ns, 60 ns and 70 ns
- Wide voltage range: 2.7V to 3.6V
- Typical active current: 1mA @ f = 1 MHz
- Low standby power
- Automatic power-down when deselected

Functional Description

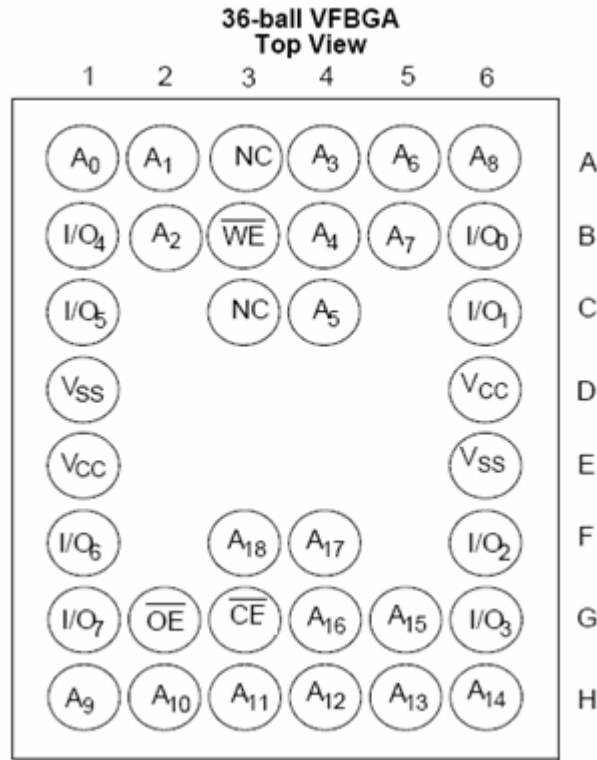
The M24L48512SA is a high-performance CMOS pseudo static RAM (PSRAM) organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}) and active LOW Output Enable (\overline{OE}). This device has an automatic power-down feature that reduces power

consumption dramatically when deselected. Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₈). Reading from the device is accomplished by asserting the Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) inputs LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during write operation (\overline{CE} LOW and \overline{WE} LOW). See the Truth Table for a complete description of read and write modes.

Logic Block Diagram



Pin Configuration[2]



Product Portfolio

| Product | V _{CC} Range(V) | | | Speed (ns) | Power Dissipation | | | | | |
|-------------|--------------------------|------|----------------------|---------------|---------------------------------|------|---------|------|--------------------------------|------|
| | | | | | Operating, I _{CC} (mA) | | | | Standby, I _{SB2} (μA) | |
| | f = 1 MHz | | f = f _{MAX} | | | | | | | |
| | Min. | Typ. | Max. | | Typ.[3] | Max. | Typ.[3] | Max. | Typ.[3] | Max. |
| M24L48512SA | 2.7 | 3.0 | 3.6 | 55 | 1 | 5 | 14 | 22 | 17 | 40 |
| | | | | 60 | | | | | | |
| | | | | 70 | | | 8 | 15 | | |

Notes:

2. NC “no connect”—not connected internally to the die.

3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)} and T_A = 25°C.

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature-65°C to +150°C
 Ambient Temperature with Power Applied-55°C to +125°C
 Supply Voltage to Ground Potential-0.4V to 4.6V
 DC Voltage Applied to Outputs in High-Z State[4, 5, 6]-0.4V to 3.7V
 DC Input Voltage[4, 5, 6]-0.4V to 3.7V
 Output Current into Outputs (LOW)20 mA
 Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current> 200 mA

Operating Range

| Range | Ambient Temperature (T _A) | V _{CC} |
|------------|---------------------------------------|-----------------|
| Extended | -25°C to +85°C | 2.7V to 3.6V |
| Industrial | -40°C to +85°C | 2.7V to 3.6V |

Electrical Characteristics (Over the Operating Range)

| Parameter | Description | Test Conditions | -55, 60, 70 | | | Unit |
|------------------|---|--|---|---|--|------|
| | | | Min. | Typ.[3] | Max. | |
| V _{CC} | Supply Voltage | | 2.7 | 3.0 | 3.6 | V |
| V _{OH} | Output HIGH Voltage | I _{OH} = -0.1 mA | V _{CC} - 0.4 | | | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 0.1 mA | | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 0.8 * V _{CC} | | V _{CC} + 0.4 | V |
| V _{IL} | Input LOW Voltage | | -0.4 | | 0.4 | V |
| I _{IX} | Input Leakage Current | GND ≤ V _{IN} ≤ V _{CC} | -1 | | +1 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled | -1 | | +1 | μA |
| I _{CC} | V _{CC} Operating Supply Current | f = f _{MAX} = 1/t _{RC} f = 1 MHz | V _{CC} = 3.6V, I _{OUT} = 0 mA, CMOS level | 14 for 55ns speed 14 for 60 ns speed 8 for 70 ns speed 1 for all speed | 22 for 55 ns speed 22 for 60 ns speed 15 for 70 ns speed 5 for all speeds | mA |
| I _{SB1} | Automatic \overline{CE} Power-down Current —CMOS Inputs | $\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V, f = f _{MAX} (Address and Data Only), f = 0, V _{CC} = 3.6V | | 150 | 250 | μA |
| I _{SB2} | Automatic \overline{CE} Power-down Current —CMOS Inputs | $\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 3.6V | | 17 | 40 | μA |

Capacitance[7]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|--|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz | 8 | pF |
| C _{OUT} | Output Capacitance | V _{CC} = V _{CC(typ)} | 8 | pF |

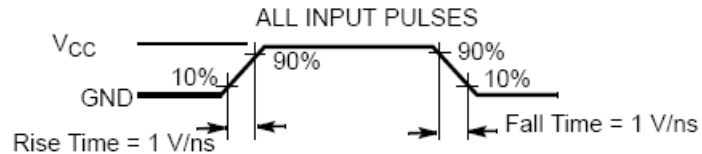
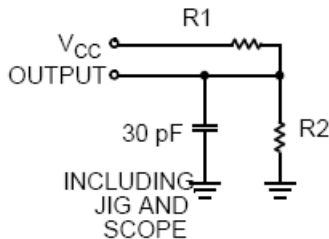
Notes:

4. V_{IH(MAX)} = V_{CC} + 0.5V for pulse durations less than 20 ns.
5. V_{IL(MIN)} = -0.5V for pulse durations less than 20 ns.
6. Overshoot and undershoot specifications are characterized and are not 100% tested.
7. Tested initially and after design or process changes that may affect these parameters.

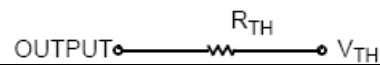
Thermal Resistance[7]

| Parameter | Description | Test Conditions | VFBGA | Unit |
|---------------|--|--|-------|----------------------|
| θ_{JA} | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 55 | $^{\circ}\text{C/W}$ |
| θ_{JC} | Thermal Resistance (Junction to Case) | | 17 | $^{\circ}\text{C/W}$ |

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT



| Parameters | 3.0V V _{CC} | Unit |
|-----------------|----------------------|----------|
| R1 | 22000 | Ω |
| R2 | 22000 | Ω |
| R _{TH} | 11000 | Ω |
| V _{TH} | 1.50 | V |

Switching Characteristics (Over the Operating Range)[8]

| Parameter | Description | -55 | | -60 | | -70 | | Unit |
|---------------------------------|--|--------------------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | |
| t _{RC} | Read Cycle Time | 55 ^[12] | | 60 | | 70 | | ns |
| t _{AA} | Address to Data Valid | | 55 | | 60 | | 70 | ns |
| t _{OHA} | Data Hold from Address Change | 5 | | 8 | | 10 | | ns |
| t _{ACE} | $\overline{\text{CE}}$ LOW | | 55 | | 60 | | 70 | ns |
| t _{DOE} | $\overline{\text{OE}}$ LOW to Data Valid | | 25 | | 25 | | 35 | ns |
| t _{LZOE} | $\overline{\text{OE}}$ LOW to Low Z[9, 10] | 5 | | 5 | | 5 | | ns |
| t _{HZOE} | $\overline{\text{OE}}$ HIGH to High Z[9, 10] | | 25 | | 25 | | 25 | ns |
| t _{LZCE} | $\overline{\text{CE}}$ LOW | 2 | | 2 | | 5 | | ns |
| t _{HZCE} | $\overline{\text{CE}}$ HIGH | | 25 | | 25 | | 25 | ns |
| t _{SK} ^[12] | Address Skew | | 0 | | 0 | | 10 | ns |
| Write Cycle[11] | | | | | | | | |
| t _{WC} | Write Cycle Time | 55 | | 60 | | 70 | | ns |
| t _{SCE} | $\overline{\text{CE}}$ LOW | 45 | | 45 | | 60 | | ns |
| t _{AW} | Address Set-up to Write End | 45 | | 45 | | 55 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | ns |

Notes:

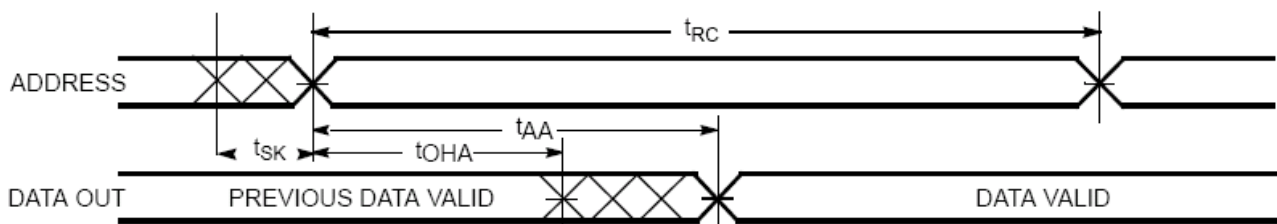
- Test conditions assume signal transition time of 1 V/ns or higher, timing reference levels of $V_{CC(\text{typ})}/2$, input pulse levels of 0V to $V_{CC(\text{typ})}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
- High-Z and Low-Z parameters are characterized and are not 100% tested.
- The internal write time of the memory is defined by the overlap of $\overline{\text{WE}}$, $\overline{\text{CE}} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.
- To achieve 55-ns performance, the read access should be $\overline{\text{CE}}$ controlled. In this case t_{ACE} is the critical parameter and t_{SK} is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

Switching Characteristics (Over the Operating Range)[8] (continued)

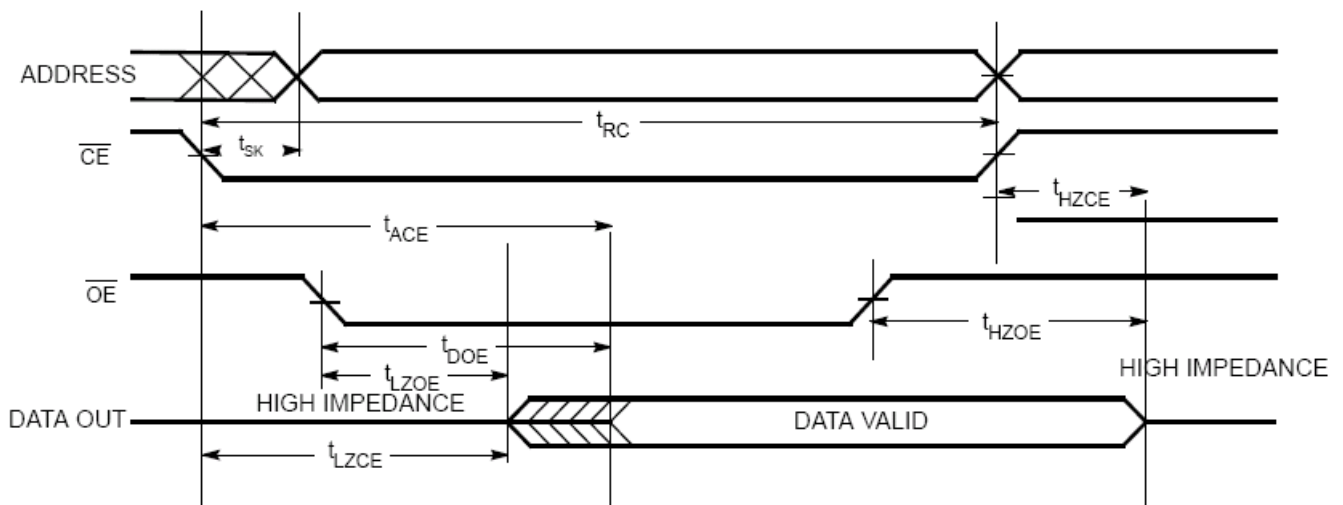
| Parameter | Description | -55 | | -60 | | -70 | | Unit |
|------------|--------------------------------------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{SA} | Address Set-up to Write Start | 0 | | 0 | | 0 | | ns |
| t_{PWE} | \overline{WE} Pulse Width | 40 | | 40 | | 45 | | ns |
| t_{SD} | Data Set-up to Write End | 25 | | 25 | | 25 | | ns |
| t_{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t_{HZWE} | \overline{WE} LOW to High Z[9, 10] | | 25 | | 25 | | 25 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z[9, 10] | 5 | | 5 | | 5 | | ns |

Switching Waveforms

Read Cycle 1 (Address Transition Controlled) [12, 13, 14]



Read Cycle 2 (\overline{OE} Controlled) [12, 14]



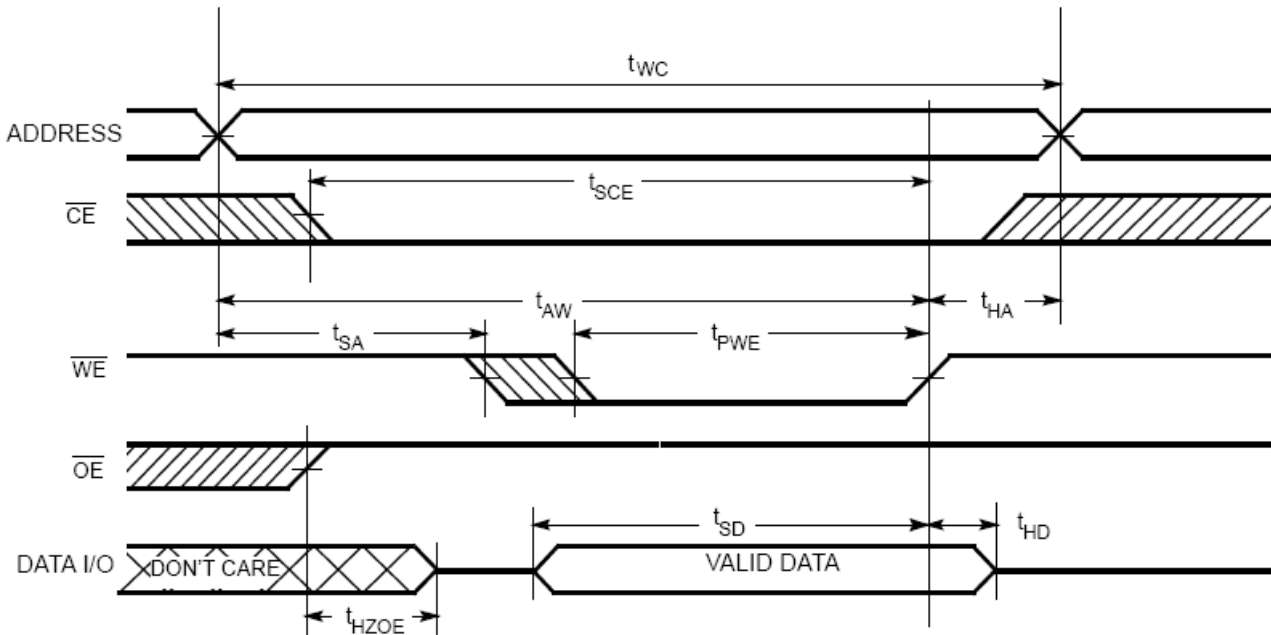
Notes:

13. Device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} .

14. \overline{WE} is HIGH for Read Cycle.

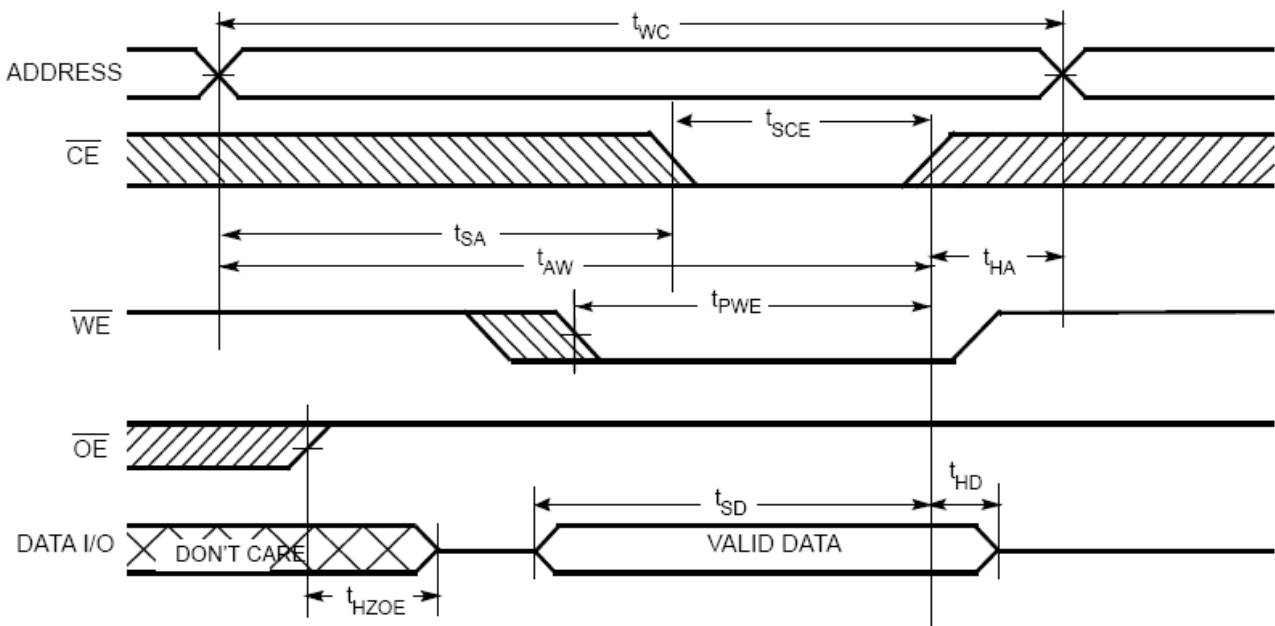
Switching Waveforms (continued)

Write Cycle No. 1 (WE Controlled) [10, 11, 15, 16, 17]



Switching Waveforms (continued)

Write Cycle 2 (CE Controlled) [10, 11, 15, 16, 17]



Notes:

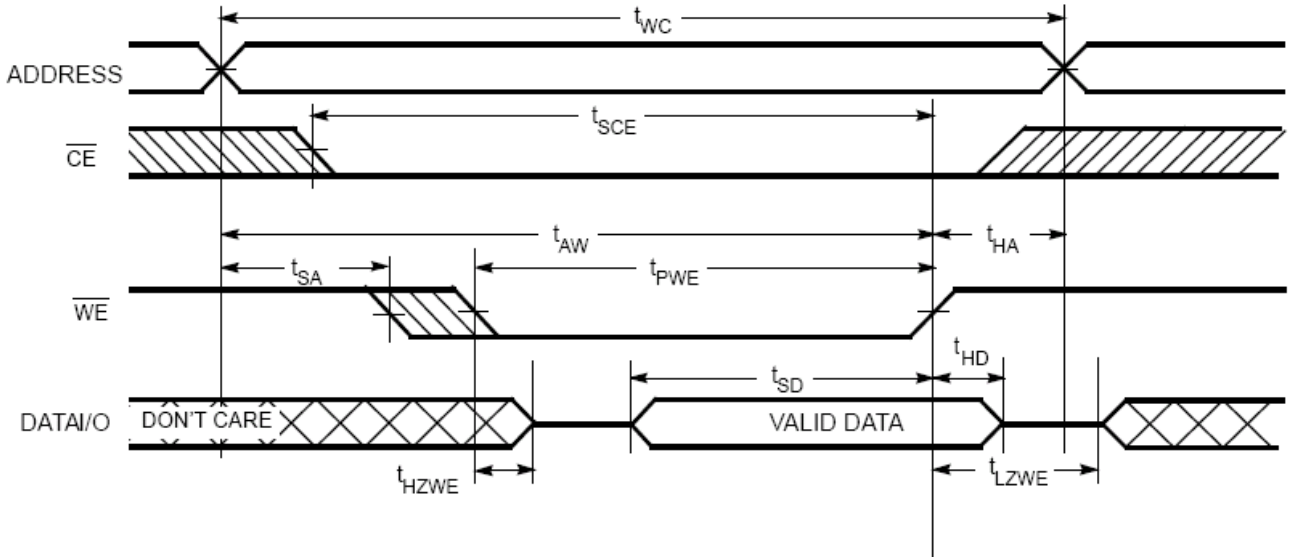
15. Data I/O is high impedance if $\overline{OE} \geq V_{IH}$.

16. If Chip Enable goes INACTIVE simultaneously with $\overline{WE} = \text{HIGH}$, the output remains in a high-impedance state.

17. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

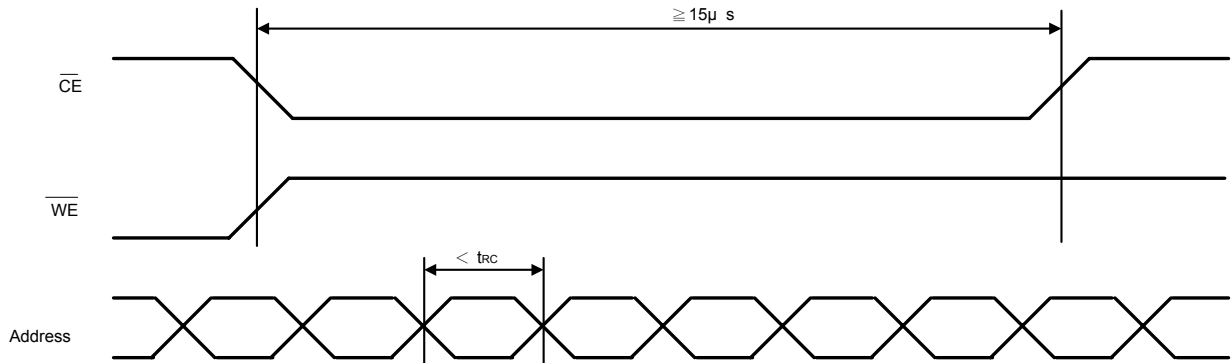
Write Cycle 3 (\overline{WE} Controlled, \overline{OE} LOW)[16, 17]



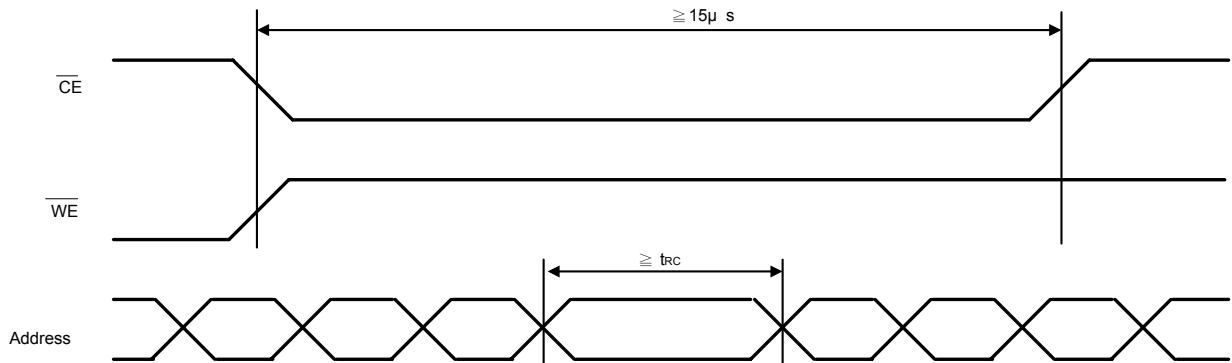
Avoid Timing

ESMT Pseudo SRAM has a timing which is not supported at read operation, If your system has multiple invalid address signal shorter than t_{RC} during over $15\mu s$ at read operation shown as in Abnormal Timing, it requires a normal read timing at least during $15\mu s$ shown as in Avoidable timing 1 or toggle \overline{CE} to high ($\geq t_{RC}$) one time at least shown as in Avoidable Timing 2.

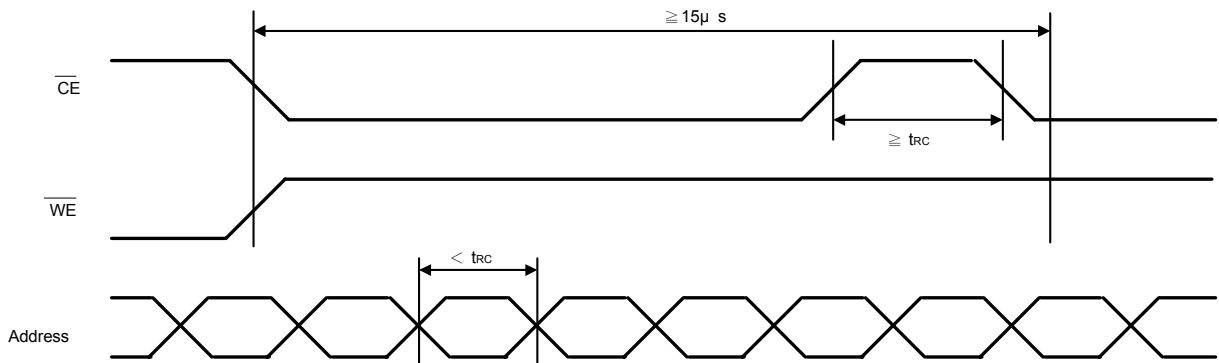
Abnormal Timing



Avoidable Timing 1



Avoidable Timing 2



Truth Table[18]

| \overline{CE} | \overline{OE} | \overline{WE} | I/O ₀ -I/O ₇ | Mode | Power |
|-----------------|-----------------|-----------------|------------------------------------|----------------------------|----------------------------|
| H | X | X | High Z | Power-down | Standby (I _{SB}) |
| X | X | X | High Z | Power-down | Standby (I _{SB}) |
| L | L | H | Data Out | Read | Active (I _{CC}) |
| L | X | L | Data in | Write | Active (I _{CC}) |
| L | H | H | High Z | Selected, Outputs Disabled | Active (I _{CC}) |

Ordering Information

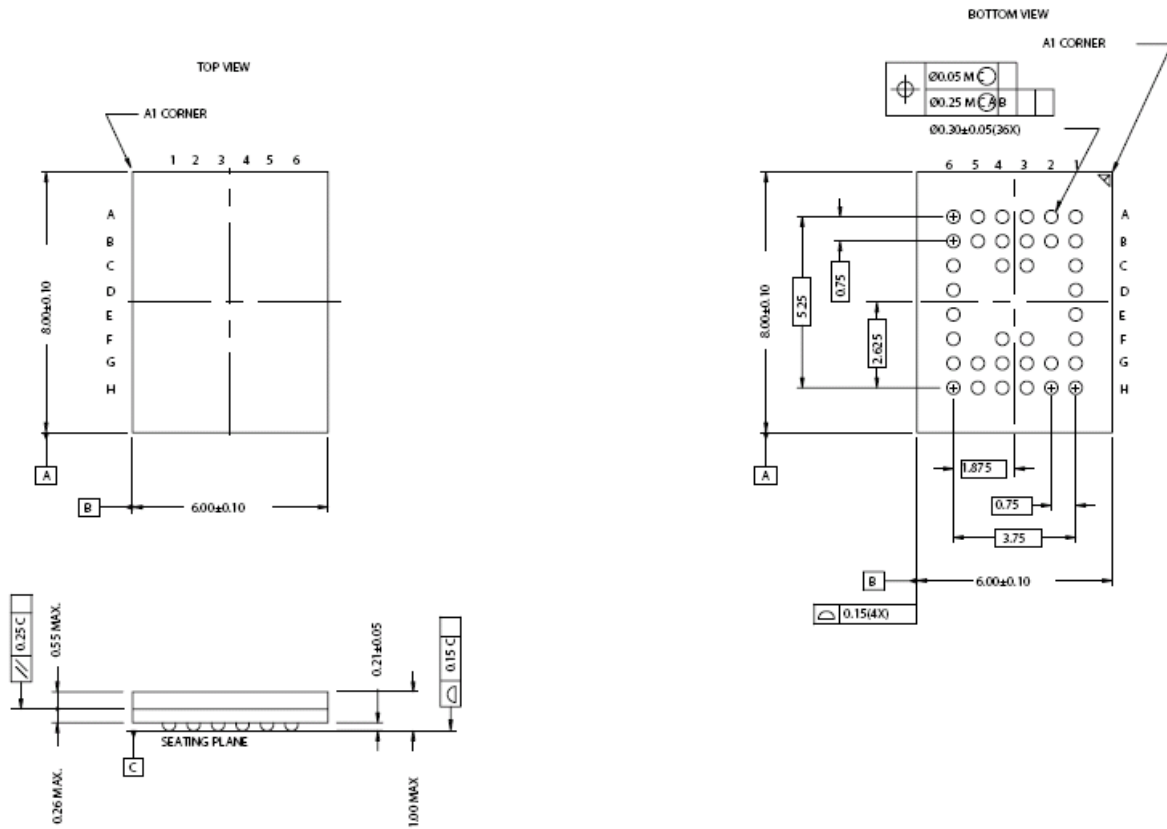
| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|--------------------|--|-----------------|
| 55 | M24L48512SA-55BEG | 36-Lead VFBGA (6 x 8 x 1 mm) (pb-free) | Extended |
| 60 | M24L48512SA -60BEG | 36-Lead VFBGA (6 x 8 x 1 mm) (pb-free) | Extended |
| 70 | M24L48512SA -70BEG | 36-Lead VFBGA (6 x 8 x 1 mm) (pb-free) | Extended |
| 55 | M24L48512SA-55BIG | 36-Lead VFBGA (6 x 8 x 1 mm) (pb-free) | Industrial |
| 60 | M24L48512SA-60BIG | 36-Lead VFBGA (6 x 8 x 1 mm) (pb-free) | Industrial |
| 70 | M24L48512SA-70BIG | 36-Lead VFBGA (6 x 8 x 1 mm) (pb-free) | Industrial |

Note:

18.H = Logic HIGH, L = Logic LOW, X = Don't Care.

Package Diagram

36-Lead VFBGA (6 x 8 x 1 mm)



Revision History

| Revision | Date | Description |
|-----------------|-------------|--|
| 1.0 | 2007.07.19 | Original |
| 1.1 | 2008.07.04 | 1. Move Revision History to the last 2. Modify voltage range 2.7V~3.3V to 2.7V~3.6V 3. Add Industrial grade 4. Add Avoid timing |

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