FX-400

Low Jitter Frequency Translator
Previous Part Number FX-424

Description

The FX-400 is a precision quartz-based frequency translator used to translate an input frequency such as 8 kHz, 1.544 MHz, 2.048 MHz, 19.44 MHz etc. to any specific frequency from 1.544 MHz to 1.0 GHz. The FX-400 can perform either up or down frequency conversion. The FX-400's superior jitter performance is achieved through the use of a precision VCXO or VCSO. With the use of an external multiplexer, up to 4 different input clocks can be translated to a common output frequency.

Features

- Quartz-based PLL for Ultra-Low Jitter
- Frequency Translation up to 1 GHz
- Accepts up to 4 ext.-muxed clock inputs
- LVCMOS / LVDS / LVPECL Inputs compatible
- Differential LVPECL /LVDS or LVCMOS Output
- Lock Detect / Loss of Signal Alarms
- Output Disable
- 20.3 x 13.7 x 5.1 mm SMT package
- RoHS/Lead Free Compliant

Applications

- Wireless Infrastructure
- 10 Gigabit FC
- 10GbE LAN / WAN
- OADM and IP Routers
- Test Equipment
- Military Communications

Block Diagram

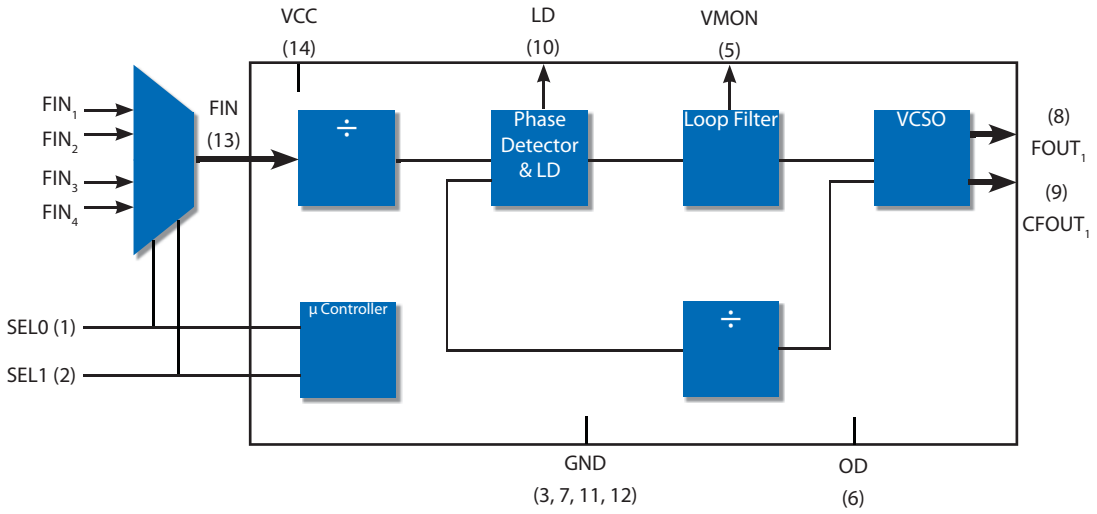

Figure 1. Functional block diagram

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Rev: 01Apr2009

Performance Specifications

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Frequency [1, 2, 3]					
Input Frequency	F_{IN}	0.008		800	MHz
Capture Range	APR	±40			ppm
Output Frequency	F_{OUT}	1.544		1000	MHz
Supply					
Voltage [2, 3]	V_{CC}	3.13	3.3	3.46	V
Current (No Load)[3]	I_{CC}		60	100	mA
Input Signal [2, 3]					
LVCMOS	F_{IN}		CMOS		
LVDS	F_{IN}		LVDS		
LVPECL	F_{IN}		LVPECL		
LVCMOS Output (Option A) [2, 3]			LVCMOS		
Differential Output (Options C and D) [2, 3, 4, 5]					
Mid Level - LVPECL		V_{CC}-1.4	V_{CC}-1.25	V_{CC}-1.0	V
Swing - LVPECL		450	600	950	mV p-p
Mid Level - LVDS		V_{CC}-2.4	V_{CC}-2.3	V_{CC}-2.5	V
Swing - LVDS		250	410	450	mV p-p
Rise Time	t_R		0.5		ns
Fall Time	t_F		0.5		ns
Symmetry	SYM	45	50	55	%
SSB Phase Noise, Fout = 155.52/622.08 [5, 6]					
10Hz Offset	Φ_n		-64/-27		dBc/Hz
100Hz Offset	Φ_n		-95/-55		dBc/Hz
1kHz Offset	Φ_n		-123/-123		dBc/Hz
10kHz Offset	Φ_n		-143/-110		dBc/Hz
100kHz Offfset	Φ_n		-146/-130		dBc/Hz
1 MHz Offset	Φ_n		-146/-146		dBc/Hz
10 MHz Offset	Φ_n		-146/-146		dBc/Hz
Jitter Generation [5, 6]					
155.52 MHz (12kHz - 20MHz BW)	Φ_J		0.30		ps RMS
622.08 MHz (12kHz - 20 MHz BW)	Φ_J		0.12		ps RMS
Operating Temperature (Options T of E) [1, 3]	T_{OP}		0 to 70 or -40 to 85		°C

1. *See Standard Frequencies and Ordering Information.*
2. *Parameters are tested with production test circuit below (Fig 2).*
3. *Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.*
4. *Measured from 20% to 80% of a full output swing (Fig 3).*
5. *Not tested in production, guaranteed by design, verified at qualification.*
6. *The FX-400 phase noise and jitter performance can be optimized for specific applications. Please consult with Vectron's Application Engineers for more information.*

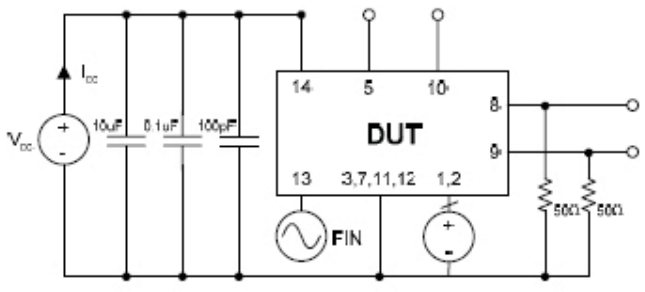


Figure 2. Test Circuit

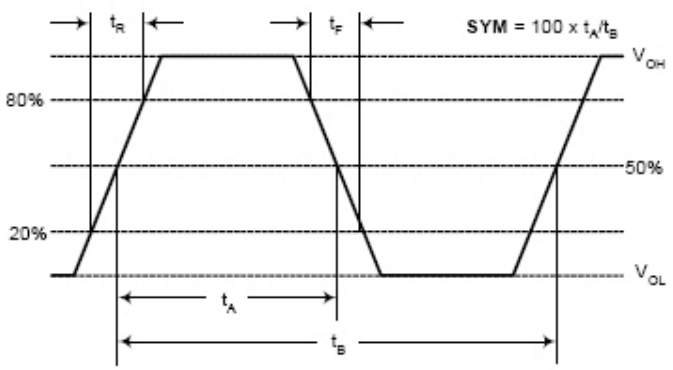


Figure 3. LVPECL Waveform

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	6	V
Storage Temperature	T_{STR}	-55 to 125	ºC
Soldering Temp/TIme	T_{LS}	260/40	ºC/sec

Reliability

The FX-400 is capable of meeting the following qualification tests

Table 3. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Handling Precautions

Although ESD protection circuitrry has been designed into the the FX-400, proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance=1.5Kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes

Table 4. Predicted ESD Ratings

Model	Minimum	Conditions
Human Body Model	500 V	MIL-STD 883, Method 3015
Charged Device Model	500 V	JEDEC, JESD22-C101

Reflow Profile

Table 5. Reflow Profile (IPC/JEDEC J-STD-020C)		
Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 ºC/sec Max
Time Above 217 ºC	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 ºC	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 ºC/sec Max

The FX-400 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-400 should not be subjected to a wash process that will immerse it in solvents. NO CLEAN is the recommended procedure. The FX-400 has been designed for pick and place reflow soldering. The FX-400 may be reflowed once and should not be reflowed in the inverted position.

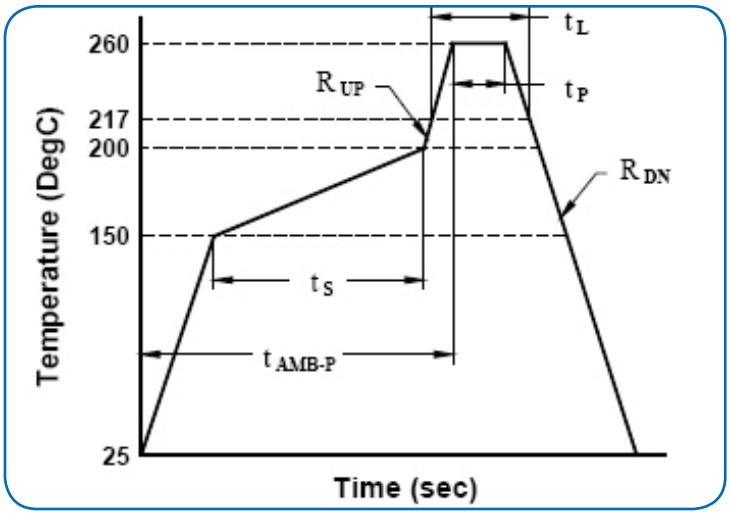


Figure 4. Suggested IR Profile

Tape and Reel

Table 6. Tape and Reel Information												
Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
44	20.2	1.5	4	20	330	1.5	13	20.2	100	44.4	50.4	200

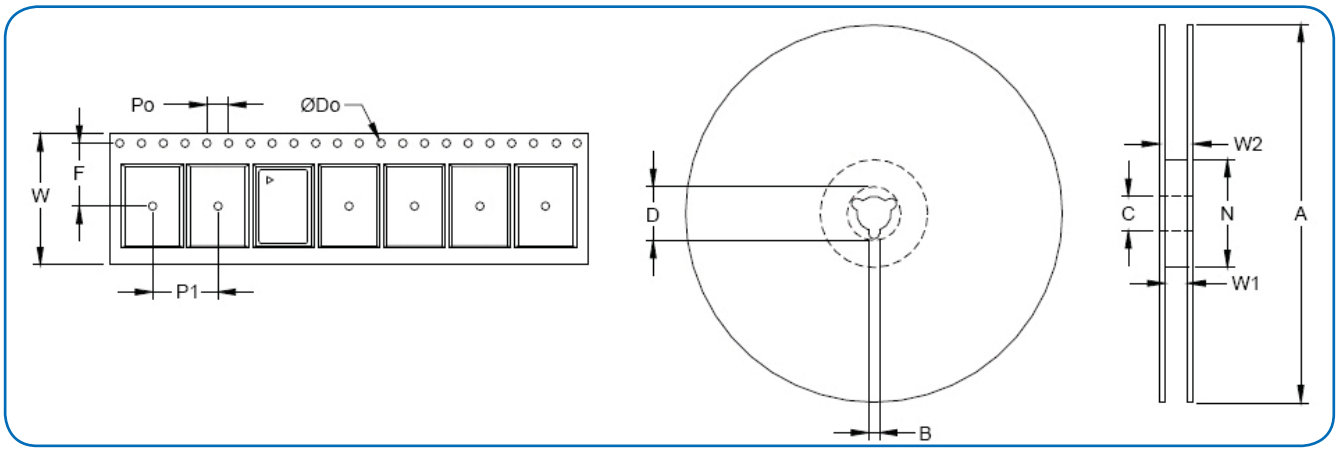


Figure 5. Tape and Reel

Pin Configuration

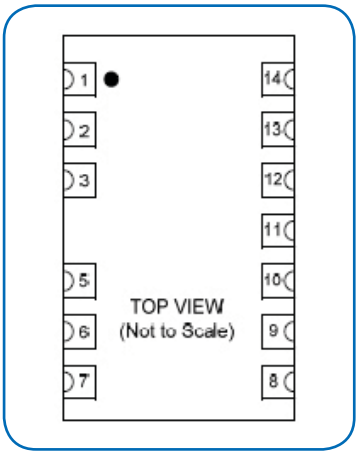


Figure 6. Pin Configuration

Table 7. Pin Functions

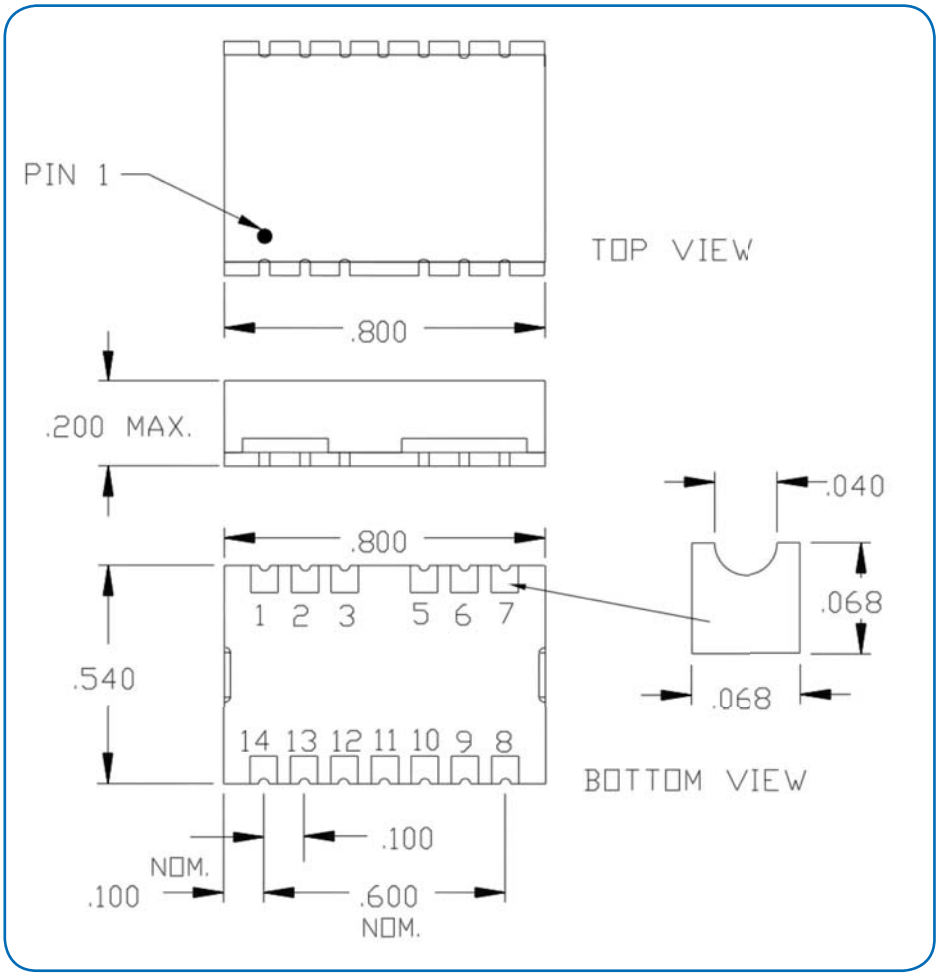
Pin #	Symbol	I/O	Level	Function
1	SEL0	I	LVCMOS	Frequency Select * (See Table 8)
2	SEL1	I	LVCMOS	Frequency Select * (See Table 8)
3	GND	GND	Supply	Case and Electrical Ground
4				Not present
5	VMON	O		VCXO Control Voltage Monitor Under locked conditions VMON should be > 0.3V and <3.0V. The input frequency may be out of range if the voltage exceeds these levels
6	OD	I	LVCMOS	Output Disable Disabled = Logic "1" Enabled = Logic "0" or no connect
7	GND	GND	Supply	Case and Electrical Ground
8	FOUT	O	LCPECL. LVDS or LVCMOS	Frequency Output
9	CFOUT	O	LVPECL, LVDS or LVCMOS	Complementary Frequency Output – Note for LVCMOS option this pad will be tied to GND.
10	LD	O	LVCMOS	Lock Detect Locked = Logic "1" Loss of Signal = Logic "0"
11	GND	GND	Supply	Case and Electrical Ground
12	GND	GND	Supply	Case and Electrical Ground
13	FIN	I	LVCMOS or LVPECL	Input Frequency – AC Coupled
14	VCC	VCC	Supply	Power Supply Voltage (3.3 V ±5%)

*For applications requiring two to four input frequencies, Vectron will assign a unique part number and the Input Frequency versus SEL[1:0] settings will be provided in a Specification Control Drawing. For single input configurations it is recommended that SEL0 and SEL1 are tied to ground.

Table 8. Control Logic (LVCMOS)

SEL0	SEL1	Reference Clock Input
0	0	F_1
0	1	F_2
1	0	F_3
1	1	F_4

FX-400 Outline Diagram and Pad Layout



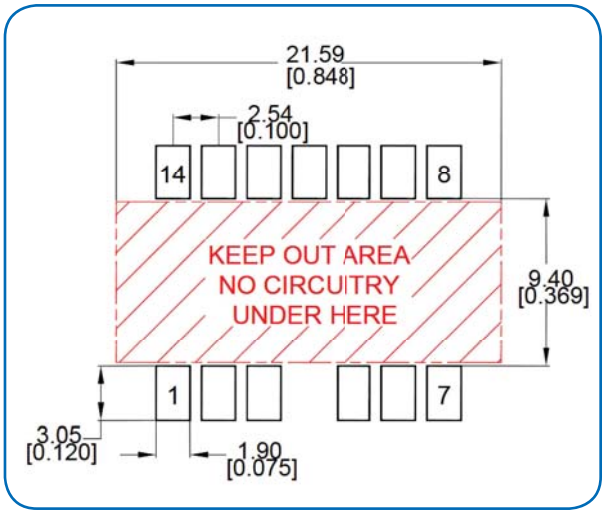


Figure 7. Outline and Pad Layout

Suggested Output Load Configurations

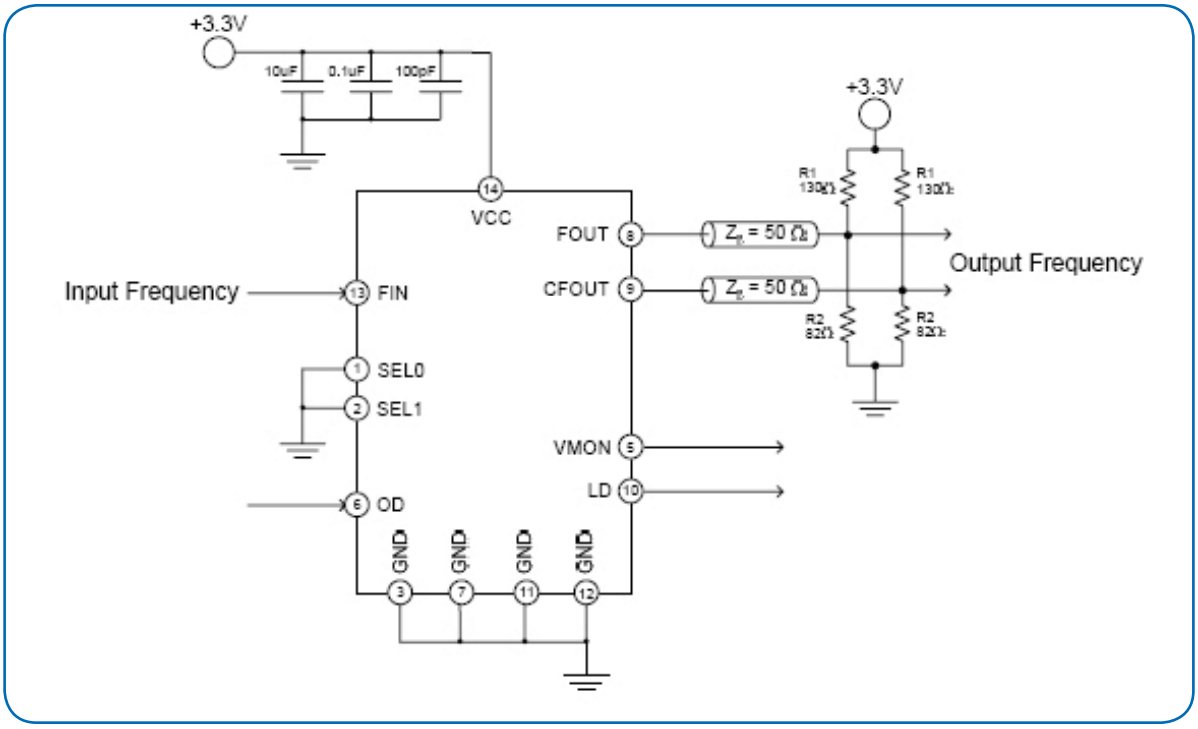


Figure 8. Single Input Frequency Translation - LVPECL Termination

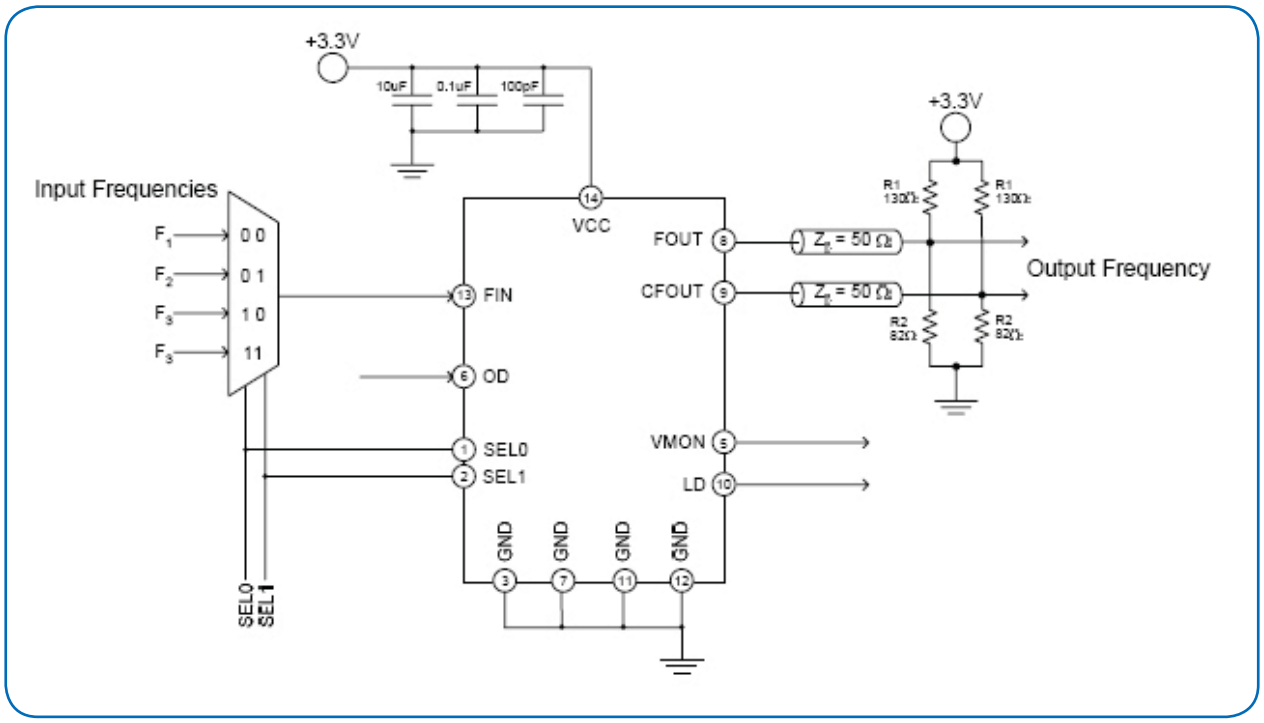


Figure 9. Four Input Frequencies Translated to Common Output Frequency – LVPECL Termination

Table 8. Standard Frequencies (MHz)

0.08000000	A9	6.29145600	CF	19.7190000	DH	38.8800000	H5	63.3600000	JJ	130.000000	LD	318.750000	PV	669.642900	R1
0.10000000	AH	6.31200000	C7	19.9218750	ED	39.0625000	HH	63.8976000	JN	139.264000	L5	320.000000	PP	670.838600	R7
0.12800000	AX	6.48000000	C2	20.0000000	E2	39.3216000	HD	64.0000000	JT	150.000000	M8	322.265650	PW	672.000000	RT
0.24300000	A8	6.75000000	CB	20.1416000	E3	39.8437500	HJ	64.1520000	JH	150.144000	M6	328.710950	PX	672.156250	TX
0.25600000	AM	7.68000000	C9	20.4800000	E4	40.0000000	JF	65.5360000	J6	153.600000	MA	333.257150	PY	672.162712	R5
0.32000000	AW	7.77600000	C5	20.5444340	EF	40.2830630	KK	66.0000000	JA	155.520000	M2	334.663300	RB	673.456600	RA
0.38400000	AY	8.19200000	C3	20.7135000	E1	40.9600000	J1	70.0000000	KB	156.250000	M3	336.081350	RC	684.255400	R9
0.40000000	AF	9.21600000	CH	20.8285720	EG	41.0888870	KM	70.6560000	KC	159.375000	M7	353.676350	RD	687.700000	TV
0.48000000	AK	9.72000000	C8	20.8286000	EB	41.6571440	KP	71.6100000	KF	160.000000	M1	368.640000	RY	690.569196	R4
0.50000000	BP	9.75000000	CE	20.9165460	EH	41.6600000	LM	73.7280000	K8	161.132813	M4	375.000000	RF	693.468750	RV
0.51200000	AJ	9.83040000	C1	21.0050840	EJ	41.8329130	KT	74.1250000	K1	164.355475	M9	382.800000	RU	693.482991	R6
0.65545000	AE	10.0000000	C4	22.0000000	E9	42.0000000	JB	74.1758000	KA	166.628572	M5	400.000000	RR	693.750000	R8
0.77200000	AT	10.2300000	DP	22.1047720	EK	42.0101690	KV	74.2500000	K7	167.331646	N2	409.600000	RE	696.390625	RW
0.96000000	A7	10.2400000	DM	22.2171000	E5	42.5000000	JC	75.0000000	KH	168.040678	N3	491.520000	PM	696.421478	V1
1.00000000	BB	10.4142850	DV	22.5792000	E8	42.6600000	JZ	76.8000000	K4	170.000000	N4	500.000000	RK	696.421875	TY
1.02400000	B2	10.4582260	DU	24.0000000	EC	44.2095440	KX	77.7600000	K2	172.500000	NU	505.000000	V3	704.380600	TG
1.21500000	BU	10.4872000	DN	24.5760000	E6	44.4343000	LF	78.0000000	LH	173.370748	ND	531.000000	PH	707.352700	TC
1.22880000	BK	10.9490000	DG	24.7040000	E7	44.6218000	JW	78.1250000	K3	173.437500	NP	531.250000	P8	707.500000	V2
1.25000000	BG	10.9500000	DJ	25.0000000	F7	44.7360000	J3	78.6432000	K5	176.838175	NA	568.928600	PJ	710.948600	T2
1.33330000	BF	11.1840000	DF	25.1658000	F8	44.9280000	JE	79.6875000	KG	182.016000	N8	569.196400	P9	712.520000	TW
1.50000000	BE	12.2880000	D8	25.6000000	F6	45.1584000	JG	80.0000000	K9	182.857142	NM	588.000000	RH	716.573200	T1
1.53600000	BV	12.3076860	DY	25.9200000	F2	45.8240000	JM	80.5664130	KJ	184.000000	NG	595.056000	PL	718.750000	T5
1.54400000	B3	12.3520000	D1	26.0000000	F3	46.0379460	LG	82.1777380	KL	184.320000	NH	600.000000	PR	719.734400	T3
1.92000000	B1	12.8000000	D2	27.0000000	F4	46.7200000	JK	82.9440000	K6	187.500000	N5	614.400000	RG	737.280000	TL
2.00000000	B8	13.0000000	D3	27.6480000	FB	46.8750000	JY	83.3142880	KN	195.000000	N7	622.080000	P2	739.200000	TT
2.04800000	B4	13.5000000	DT	28.7040000	F1	48.0000000	JV	83.6658250	KR	200.000000	NE	624.693800	PD	742.500000	V4
2.30400000	BD	14.8351600	DL	29.4912000	F5	49.1520000	J7	84.0203380	KU	200.192000	N6	624.704800	P6	748.070900	T6
2.45760000	BJ	15.0000000	D4	29.5000000	F9	49.4080000	J2	86.6853740	LJ	201.416020	N1	625.000000	P3	750.000000	T7
2.50000000	BM	15.0336000	DR	30.0000000	HE	50.0000000	JD	88.4190880	KW	212.500000	NF	627.329600	P7	768.000000	TN
2.55750000	B9	15.3600000	DW	30.7200000	H1	50.0480000	KD	95.7000000	LK	219.429571	NL	629.987800	PA	777.600000	T4
3.08800000	B6	16.0000000	D9	30.8800000	HF	51.2000000	LL	97.5000000	KE	240.000000	NR	637.500000	PG	779.568600	T8
3.24000000	BL	16.3840000	D5	31.2500000	H8	51.8400000	J4	100.000000	L8	243.000000	NC	640.000000	PN	780.881000	TD
3.25000000	BC	17.1840000	DE	32.0000000	H2	52.0000000	JP	105.000000	L6	245.760000	N9	644.531250	P4	781.250000	T9
3.37500000	BH	18.4320000	D7	32.7680000	H3	53.3300000	JU	106.250000	L9	250.000000	NT	645.120000	RJ	796.875000	TB
3.84000000	B7	18.5280000	DC	33.0000000	H7	54.7460000	JL	108.000000	LA	252.571428	NJ	647.239400	PE	800.000000	TK
4.00000000	BN	18.7500000	EE	33.3330000	HC	55.0000000	JX	110.000000	L1	256.000000	NK	647.250800	PK	805.664100	TA
4.09600000	B5	19.2000000	DD	34.3680000	H6	60.0000000	JR	112.000000	L2	262.144000	NB	649.970300	PF	809.063500	TE
4.19430400	CJ	19.3926580	DX	34.5600000	HB	61.3800000	KY	114.000000	L3	292.571429	NN	657.421875	PB	819.200000	TH
5.00000000	C6	19.4400000	D6	36.8640000	HG	61.4400000	J5	120.000000	LC	300.000000	PT	665.625600	PC	821.777300	TF
5.12000000	CD	19.5312500	DZ	37.0560000	H4	62.2080000	J8	122.880000	LB	307.200000	RX	666.514286	P5	850.000000	TJ
6.14400000	CG	19.6608000	DB	37.1250000	H9	62.5000000	J9	124.416000	L7	311.040000	P1	669.128100	R2	983.400000	TU
6.29140000	CC	19.6989680	DK	37.5000000	HK	62.9145000	LE	125.000000	L4	312.500000	PU	669.326582	R3	1,000.0000	TM

Ordering Information

F X - 4 0 0 - E A E - K N N N - XX - XX

Product Family
FX: Frequency Translator

Package
400: 20.3 13.0 5.1mm

Input
E: 3.3 Vdc ±10%

Output
A: LVCMOS
C: LVPECL
D: LVDS

Operating Temperature
E: -40 to 85 °C
T: 0 to 70 °C

Absolute Pull Range
K: ± 50 ppm
S: ± 100 ppm

Factory Use

Factory Use

Factory Use

Factory Use

Input Frequency (See Above)

Output Frequency (See Above)

1. For non-listed frequencies and/or multiple input frequencies a unique part number will be assigned with the following format FX-400-XXX-SNNNN. "SNNNN" is the SCD number.

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