

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 175 \text{ mA}$  at 10 ns
- Low CMOS standby power
  - $I_{SB2} = 25 \text{ mA}$
- Operating voltages of  $3.3 \pm 0.3\text{V}$
- 2.0V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free 54-Pin TSOP II package

## Functional Description

The CY7C10612DV33 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

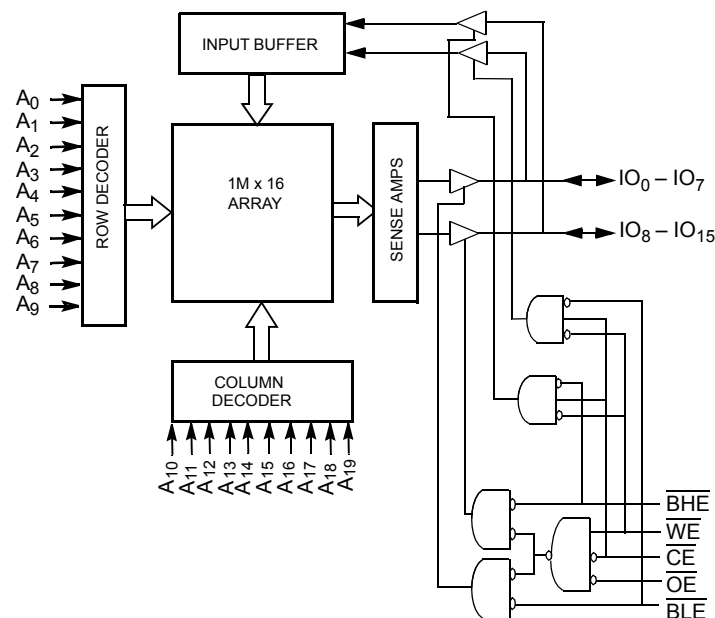
To write to the device, take Chip Enables ( $\overline{CE}$ ) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from IO pins (IO<sub>0</sub> through IO<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>). If Byte High Enable (BHE) is LOW, then data from IO pins (IO<sub>8</sub> through IO<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>).

To read from the device, take Chip Enables ( $\overline{CE}$ ) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on IO<sub>0</sub> to IO<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on IO<sub>8</sub> to IO<sub>15</sub>. See the [Truth Table](#) on page 9 for a complete description of Read and Write modes.

The input or output pins (IO<sub>0</sub> through IO<sub>15</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW and WE LOW).

The CY7C10612DV33 is available in a 54-Pin TSOP II package with center power and ground (revolutionary) pinout.

## Logic Block Diagram

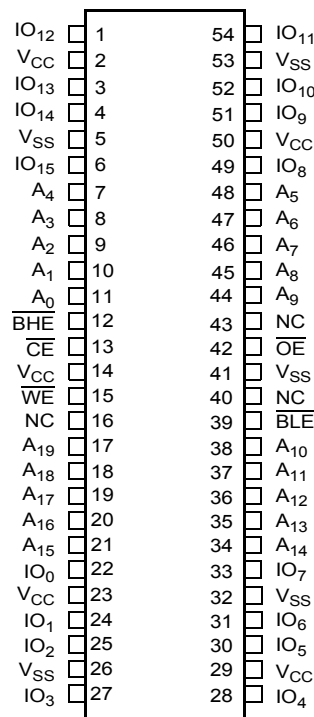


### Selection Guide

Description	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	175	mA
Maximum CMOS Standby Current	25	mA

### Pin Configuration

Figure 1. 54-Pin TSOP II (Top View) [1]



**Note**

1. NC pins are not connected on the die.

**Maximum Ratings**

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied ..... -55°C to +125°C
- Supply Voltage on V<sub>CC</sub> Relative to GND <sup>[2]</sup> ..... -0.5V to +4.6V
- DC Voltage Applied to Outputs in High Z State <sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

- DC Input Voltage <sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V
- Current into Outputs (LOW) ..... 20 mA
- Static Discharge Voltage..... >2001V (MIL-STD-883, Method 3015)
- Latch Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	3.3V ± 0.3V

**DC Electrical Characteristics**

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit
			Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , I <sub>OUT</sub> = 0 mA CMOS levels		175	mA
I <sub>SB1</sub>	Automatic CE Power Down Current — TTL Inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		30	mA
I <sub>SB2</sub>	Automatic CE Power Down Current — CMOS Inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		25	mA

**Note**

2. V<sub>IL</sub> (min) = -2.0V and V<sub>IH</sub> (max) = V<sub>CC</sub> + 2V for pulse durations of less than 20 ns.

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	6	pF
C <sub>OUT</sub>	IO Capacitance		8	pF

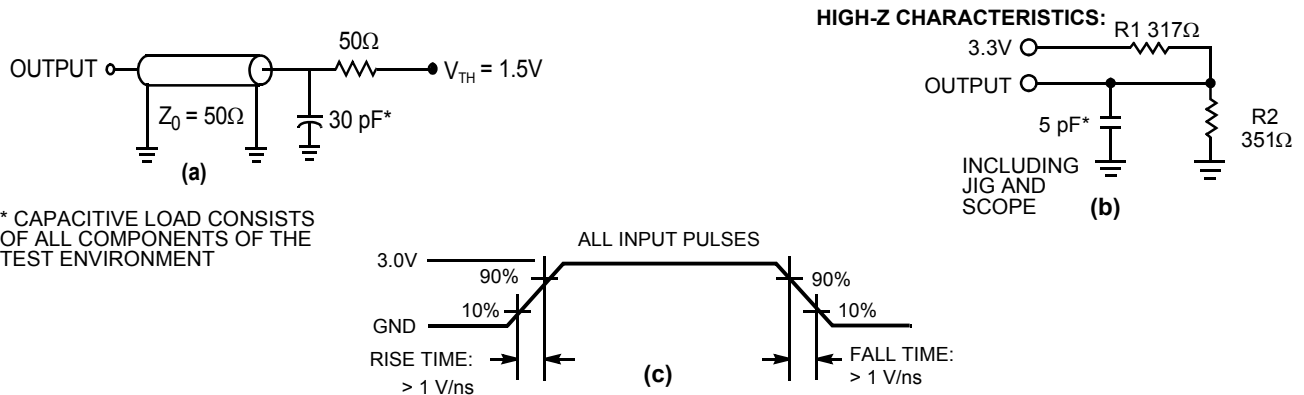
## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	24.18	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		5.40	°C/W

The AC Test Loads and Waveforms diagram follows. [3]

Figure 2. AC Test Loads and Waveforms



### Note

- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V<sub>DD</sub> (3.0V). 100 μs (t<sub>power</sub>) after reaching the minimum operating V<sub>DD</sub>, normal SRAM operation begins including reduction in V<sub>DD</sub> to the data retention (V<sub>CCDR</sub>, 2.0V) voltage.

## AC Switching Characteristics

 Over the Operating Range <sup>[4]</sup>

Parameter	Description	-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{\text{power}}$	$V_{\text{CC}}$ (Typical) to the First Access <sup>[5]</sup>	100		$\mu\text{s}$
$t_{\text{RC}}$	Read Cycle Time	10		ns
$t_{\text{AA}}$	Address to Data Valid		10	ns
$t_{\text{OHA}}$	Data Hold from Address Change	3		ns
$t_{\text{ACE}}$	$\overline{\text{CE}}$ LOW to Data Valid		10	ns
$t_{\text{DOE}}$	$\overline{\text{OE}}$ LOW to Data Valid		5	ns
$t_{\text{LZOE}}$	$\overline{\text{OE}}$ LOW to Low Z	1		ns
$t_{\text{HZOE}}$	$\overline{\text{OE}}$ HIGH to High Z <sup>[6]</sup>		5	ns
$t_{\text{LZCE}}$	$\overline{\text{CE}}$ LOW to Low Z <sup>[6]</sup>	3		ns
$t_{\text{HZCE}}$	$\overline{\text{CE}}$ HIGH to High Z <sup>[6]</sup>		5	ns
$t_{\text{PU}}$	$\overline{\text{CE}}$ LOW to Power Up <sup>[7]</sup>	0		ns
$t_{\text{PD}}$	$\overline{\text{CE}}$ HIGH to Power Down <sup>[7]</sup>		10	ns
$t_{\text{DBE}}$	Byte Enable to Data Valid		5	ns
$t_{\text{LZBE}}$	Byte Enable to Low Z	1		ns
$t_{\text{HZBE}}$	Byte Disable to High Z		5	ns
<b>Write Cycle <sup>[8, 9]</sup></b>				
$t_{\text{WC}}$	Write Cycle Time	10		ns
$t_{\text{SCE}}$	$\overline{\text{CE}}$ LOW to Write End	7		ns
$t_{\text{AW}}$	Address Setup to Write End	7		ns
$t_{\text{HA}}$	Address Hold from Write End	0		ns
$t_{\text{SA}}$	Address Setup to Write Start	0		ns
$t_{\text{PWE}}$	$\overline{\text{WE}}$ Pulse Width	7		ns
$t_{\text{SD}}$	Data Setup to Write End	5.5		ns
$t_{\text{HD}}$	Data Hold from Write End	0		ns
$t_{\text{LZWE}}$	$\overline{\text{WE}}$ HIGH to Low Z <sup>[6]</sup>	3		ns
$t_{\text{HZWE}}$	$\overline{\text{WE}}$ LOW to High Z <sup>[6]</sup>		5	ns
$t_{\text{BW}}$	Byte Enable to End of Write	7		ns

### Notes

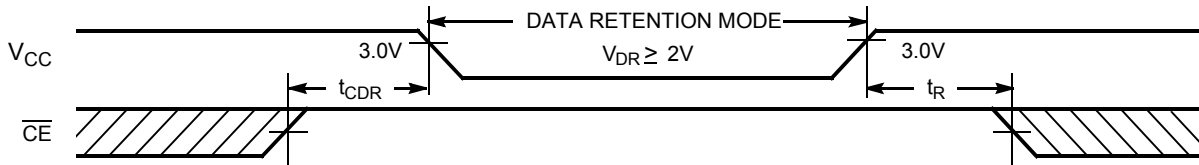
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and input pulse levels of 0 to 3.0V. Test conditions for the read cycle use output loading shown in part a) of [AC Test Loads and Waveforms](#), unless specified otherwise.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply is at typical  $V_{\text{CC}}$  values until the first memory access is performed.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZWE}}$ ,  $t_{\text{HZBE}}$ ,  $t_{\text{LZOE}}$ ,  $t_{\text{LZCE}}$ ,  $t_{\text{LZWE}}$ , and  $t_{\text{LZBE}}$  are specified with a load capacitance of 5 pF as in (b) of [AC Test Loads and Waveforms](#). Transition is measured  $\pm 200$  mV from steady state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ . Chip enable must be active and  $\overline{\text{WE}}$  and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 2 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

### Data Retention Characteristics

Over the Operating Range

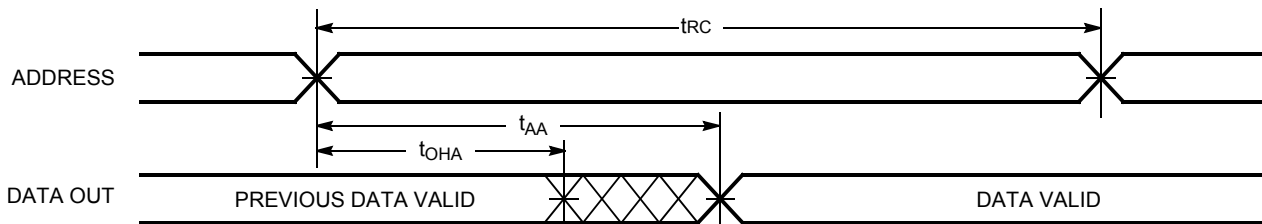
Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 2V, \overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			25	mA
$t_{CDR}^{[10]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[11]}$	Operation Recovery Time		$t_{RC}$			ns

### Data Retention Waveform



### Switching Waveforms

Figure 3. Read Cycle No. 1 [12, 13]



**Notes**

- 10. Tested initially and after any design or process changes that may affect these parameters.
- 11. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50 \mu s$  or stable at  $V_{CC(min.)} \geq 50 \mu s$ .
- 12. The device is continuously selected. OE, CE =  $V_{IL}$ , BHE, BLE or both =  $V_{IL}$ .
- 13. WE is HIGH for read cycle.

Switching Waveforms (continued)

Figure 4. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [13, 14]

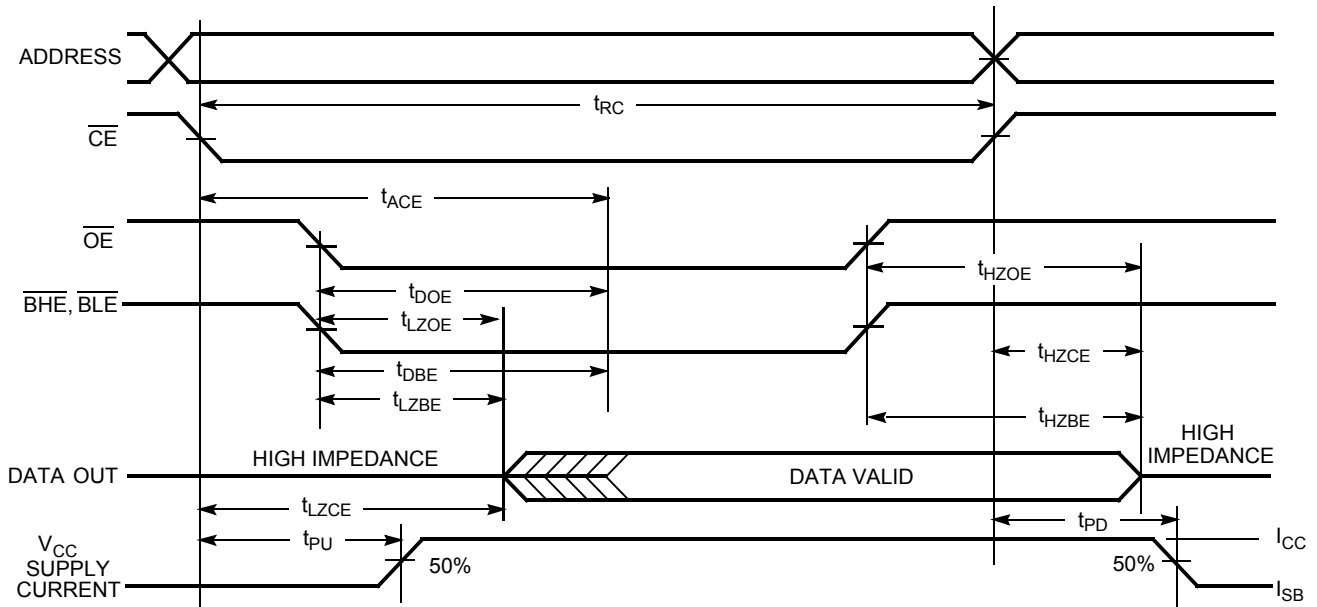
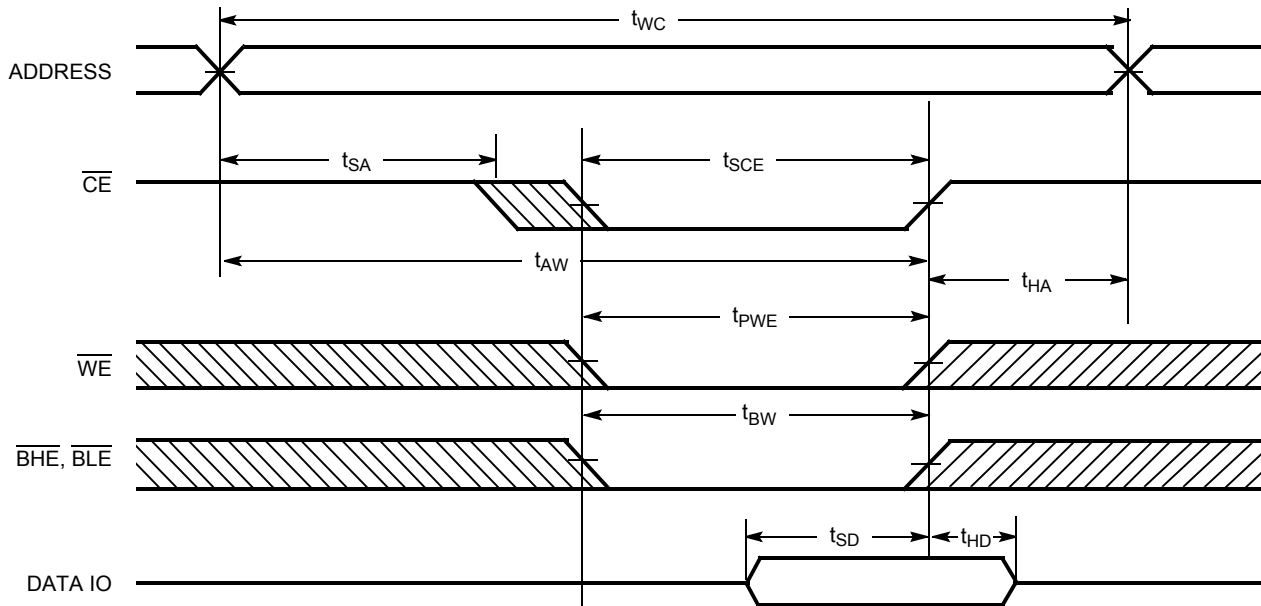


Figure 5. Write Cycle No. 1 ( $\overline{CE}$  Controlled) [15, 16]



Notes

- 14. Address valid before or similar to  $\overline{CE}$  transition LOW.
- 15. Data IO is high impedance if  $\overline{OE}$ ,  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .
- 16. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [15, 16]

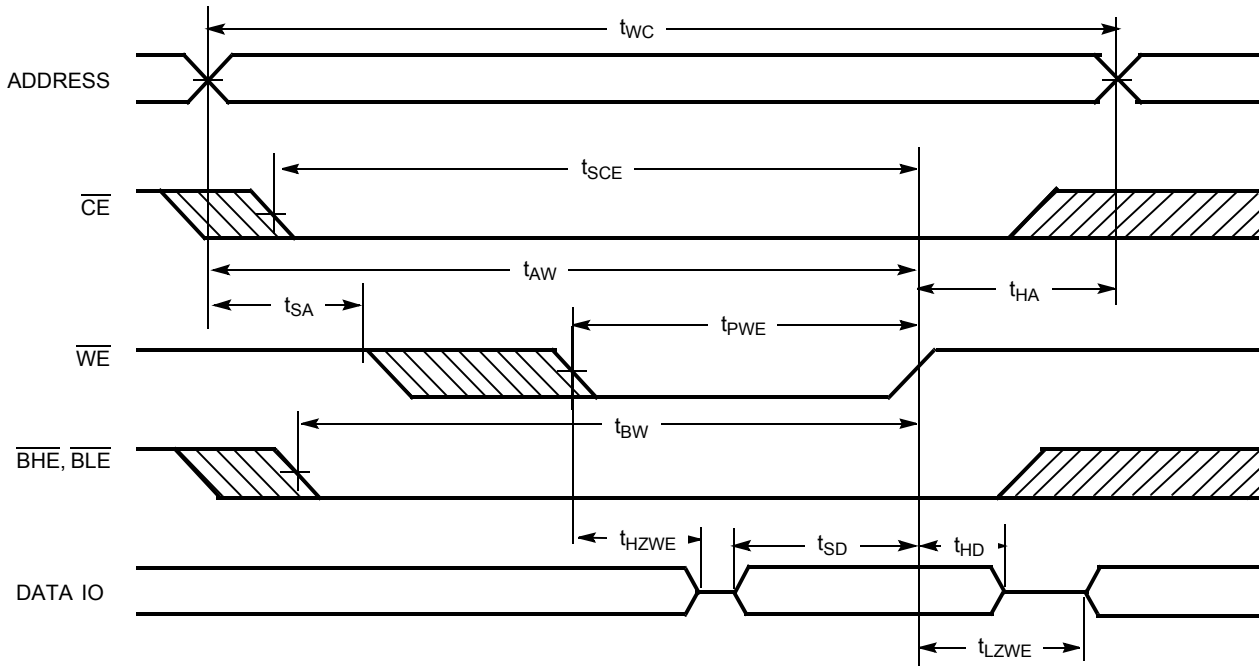
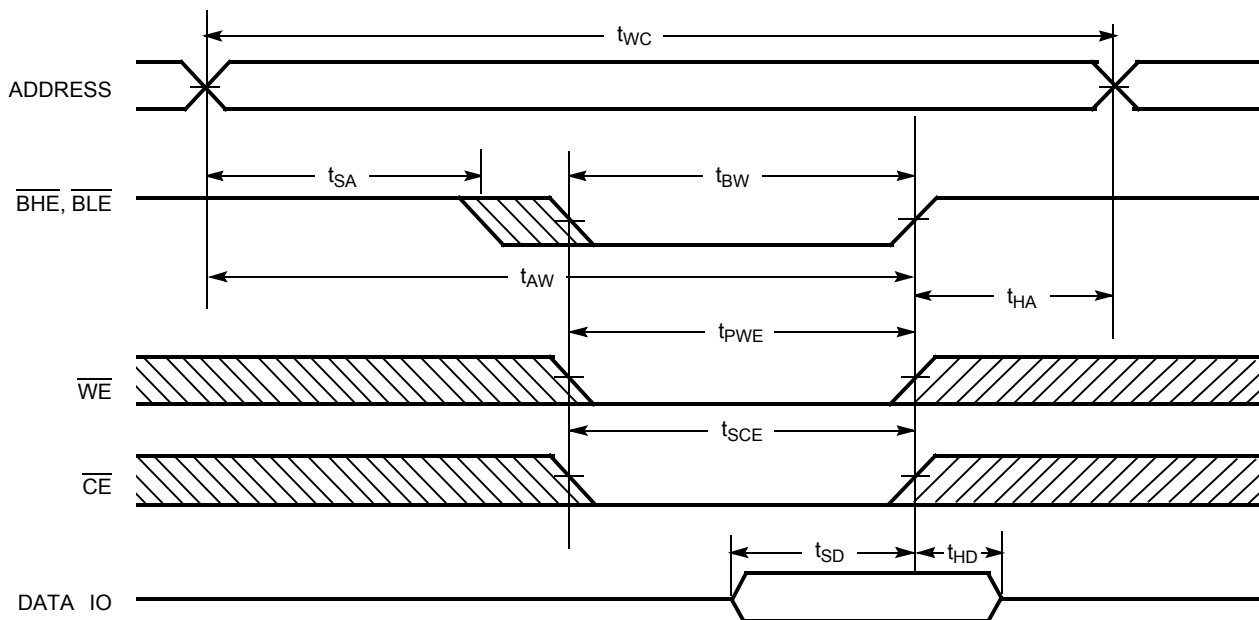


Figure 7. Write Cycle No. 3 ( $\overline{BLE}$  or  $\overline{BHE}$  Controlled) [15]







## Document History Page

Document Title: CY7C10612DV33, 16-Mbit (1M x 16) Static RAM				
Document Number: 001-49315				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2589743	VKN/PYRS	10/15/08	New datasheet
*A	2718906	VKN	06/15/2009	Post to external web

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives, and distributors. To find the office closest to you, visit us at [cypress.com/sales](http://cypress.com/sales).

#### Products

PSoC	<a href="http://psoc.cypress.com">psoc.cypress.com</a>
Clocks & Buffers	<a href="http://clocks.cypress.com">clocks.cypress.com</a>
Wireless	<a href="http://wireless.cypress.com">wireless.cypress.com</a>
Memories	<a href="http://memory.cypress.com">memory.cypress.com</a>
Image Sensors	<a href="http://image.cypress.com">image.cypress.com</a>

#### PSoC Solutions

General	<a href="http://psoc.cypress.com/solutions">psoc.cypress.com/solutions</a>
Low Power/Low Voltage	<a href="http://psoc.cypress.com/low-power">psoc.cypress.com/low-power</a>
Precision Analog	<a href="http://psoc.cypress.com/precision-analog">psoc.cypress.com/precision-analog</a>
LCD Drive	<a href="http://psoc.cypress.com/lcd-drive">psoc.cypress.com/lcd-drive</a>
CAN 2.0b	<a href="http://psoc.cypress.com/can">psoc.cypress.com/can</a>
USB	<a href="http://psoc.cypress.com/usb">psoc.cypress.com/usb</a>

© Cypress Semiconductor Corporation, 2008-2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress’ product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.