TERIDIAN SEMICONDUCTOR CORP.

73S8009C Versatile Power Management and Smart Card Interface IC

Simplifying System Integration™

DATA SHEET

DS_8009C_025 **January 2010**

ISO/IEC 7816-3

EMVCo

DESCRIPTION

The Teridian 73S8009C is a versatile power management and single smart card interface circuit that is ideally suited for smart card reader products that are battery and/or USB bus-powered. In addition to its EMV 4.1 and ISO-7816-3 compliant smart card-to-host interface circuitry; it provides control, conversion, and regulation of power for a companion host processor circuit and power for the smart card. The 73S8009C can operate from a single 2.7 V to 6.5 V source supply, or a combination of battery power (4.0 V to 6.5 V) and USB power (4.4 V to 5.5 V).

The 73S8009C supports 5 V, 3 V, and 1.8 V smart cards. The smart card signals for RST, CLK, IO, and auxiliary signals AUX1 and AUX2 are level-shifted to the selected V_{CC} value. Although the host controller is required to handle the detailed signal timing for activation and de-activation under normal conditions, the 73S8009C blocks any spurious signals on CLK, RST and IO during power-up (as V_{CC} rises) and power-down. The 73S8009C contains two handshaking signals for the controller: $\overline{\text{OFF}}$ indicates that a card is present, and RDY indicates that V_{CC} is at an acceptable value. The 73S8009C will perform emergency deactivation upon card removal, voltage faults, or over-current events

The power management circuitry of the 73S8009C allows operation from a wide range of voltages from multiple sources. V_{PC} is converted by using an inductive, step-up power converter to the intermediate voltage, V_P. V_P is used by linear voltage regulators and switches to create the voltages V_{DD} and as required, V_{CC}. V_{DD} is used by the 73S8009C and is also made available for the companion controller circuit or other external circuits. The two pins, V_{BAT} and V_{BUS} provide inputs from alternate power sources as required. An internal switch in the 73S8009C acts as a single-pole, double-throw switch that selects either V_{BAT} or V_{BUS} to be connected to V_{PC}. When the voltage on V_{BUS} is zero, V_{BAT} is connected to V_{PC}. When voltage is applied to V_{BUS}, the switch will select V_{BUS} as the source for power.

When power is supplied by V_{PC} or V_{BAT}, the 73S8009C is controlled by the ON_OFF pin in the manner of a "push-on/push-off" button action. The signals OFF_REQ and OFF_ACK provide handshaking and control of the power "off" function by the controller. A SPST momentary switch to ground connected to ON_OFF is all that is required for power control. Alternatively, the "off" state can be initiated from the host controller through OFF_ACK. When the 73S8009C is "off," the current is less than 1 µA.

When power is supplied via the V_{BUS} pin, the 73S8009C is unconditionally in the "power-on" state regardless of the action of the ON/OFF switch or OFF_ACK signal. Power supply current operating from the V_{BUS} power when V_{CC} is off is less than 500 µA to conform to USB "SUSPEND" requirements.

APPLICATIONS

- Handheld PINpad smart card readers for e-commerce, secure login, e-health, Gov't ID and loyalty
- Point of Sales & Transaction Terminals
- General Purpose Smart Card Readers

ADVANTAGES

- Ideally suited to USB bus-powered applications
  - → Ideal for combo bus-powered and/or self-powered systems
  - → Automatic battery switchover in bus powered systems
- Very low-power mode (sub-µA) with push-button ON/OFF switch input with de-bounce
- Provides 3.3 V / 40 mA power to external circuitry (host processor or peripheral circuits)
- The inductor-based DC-DC converter provides higher current and efficiency than usual charge-pump capacitor-based converters:
  - → Ideal for battery-powered applications

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FEATURES

- Smart card Interface:
  - Complies with ISO-7816-3 and EMV 4.1 and derivative standards
  - A DC-DC Converter provides 1.8 V/3 V/5 V to the card from a wide range of external power supply inputs
  - Provides up to 65 mA to the card
  - ISO-7816-3 Card emergency deactivation sequencer
  - 2 voltage supervisors detect voltage drops on the V_{CC} (card) and V_{DD} (digital) power supplies
  - Card over-current detection 150 mA max.
  - 2 card detection inputs, 1 for either user polarity
  - Auxiliary I/O lines for synchronous and ISO-7816-12 USB card support
  - Card CLK clock frequency up to 20 MHz
  - 6 kV ESD and short circuit protection on the card interface
- System Controller Interface:
  - 5 Signal images of the card signals (RSTIN, CLKIN, I/OUC, AUX1UC and AUX2UC)
  - 2 Inputs activate and select the card voltage ($\overline{\text{CMDVCC5}}$ and $\overline{\text{CMDVCC3}}$)
  - 2 Outputs, interrupt to the system controller ($\overline{\text{OFF}}$ and RDY), to inform the system controller of the card presence / faults and status of the interface
  - 1 Chip Select input (CS - QFN32 only)
  - 2 Handshaking signals for proper shutdown sequencing of all output supply voltages (OFF_REQ, OFF_ACK)
- ON/OFF Main System Switch:
  - Input for an SPST momentary switch to ground
- DC-DC Converter:
  - Step-up converter
  - Generates an intermediary voltage V_P
  - Requires a single 10 μH Inductor
- System Power Supply requirements:
  - When using VBUS: Standard USB +5 input (range +4.4 V to 5.5 V)
  - When using V_{BAT}: 4.0 V to 6.5 V
  - When using V_{PC}: 2.7 V to 6.5 V
  - Automated detection of voltage presence - Priority on VBUS over VBAT
- Power Supply Output:
  - V_{DD} supply output available to power up external circuitry: 3.3 V $\pm$0.3 V, 40 mA
- Industrial temperature range
- Small format QFN20 and QFN packages
- RoHS compliant (6/6) lead-free package

FUNCTIONAL DIAGRAM

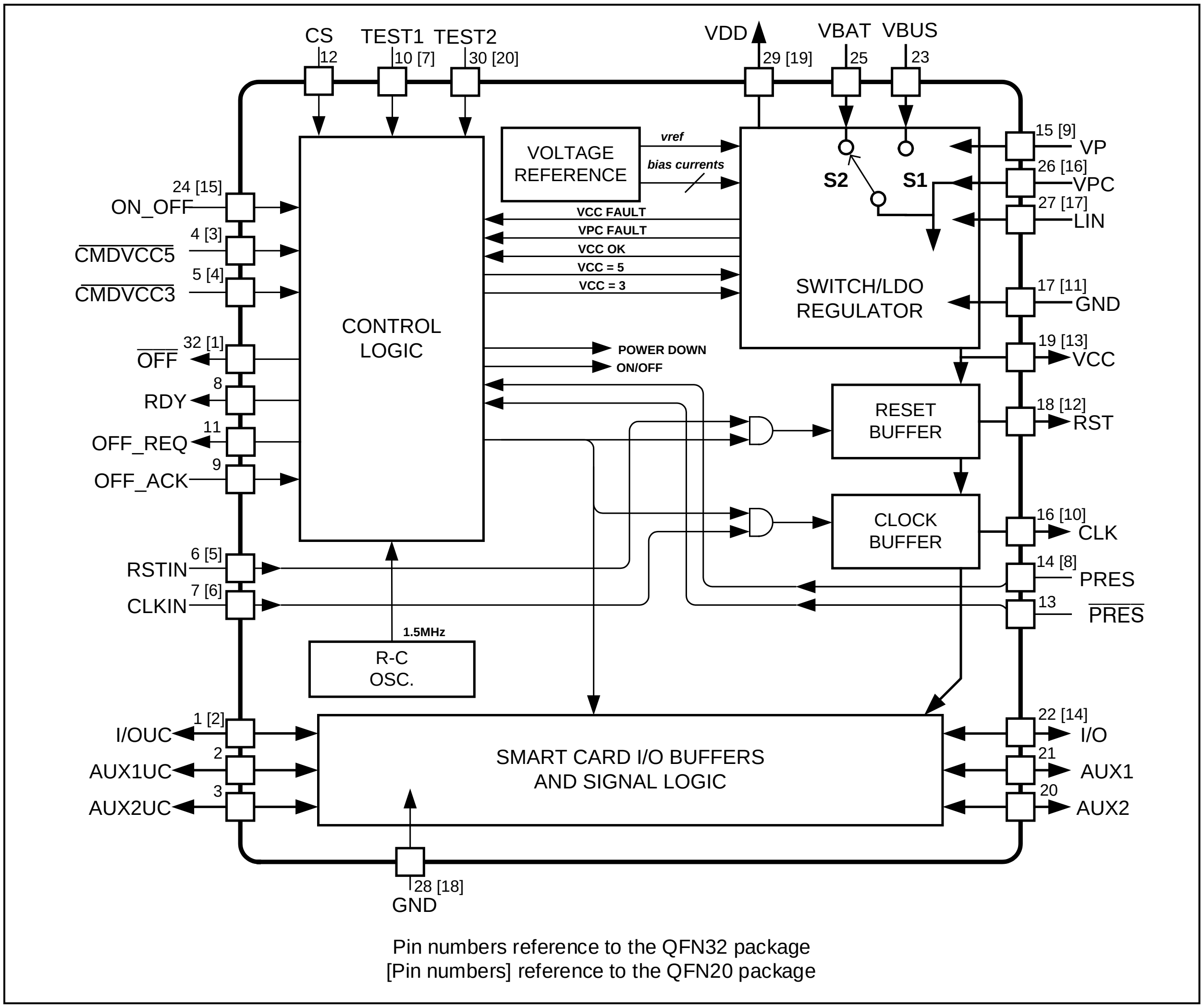

Figure 1: 73S8009C Block Diagram

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1 Pinout

The 73S8009C is supplied as a 32-pin QFN package and as a 20-pin QFN package.

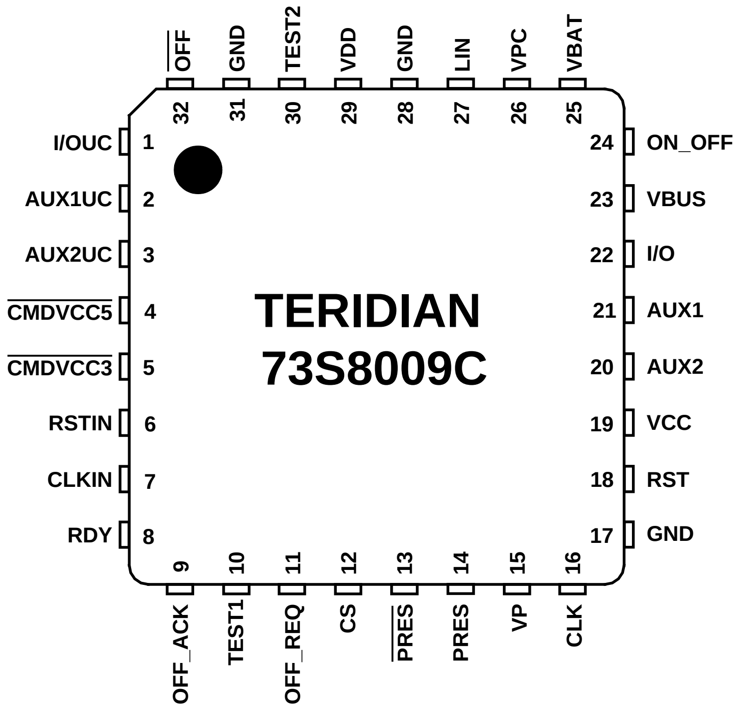


Figure 2: 73S8009C 32-Pin QFN Pinout

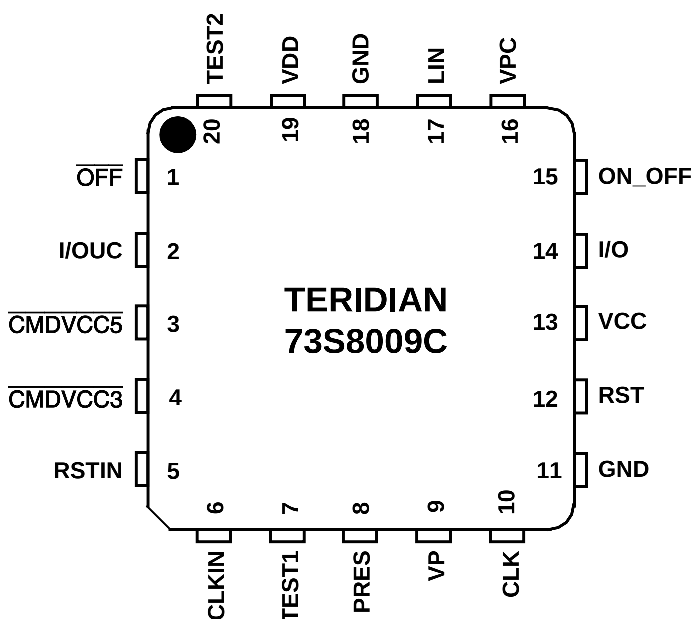


Figure 3: 73S8009C 20-Pin QFN Pinout

Table 1 describes the pin functions for the device.

Table 1: 73S8009C Pin Definitions

Pin Name	Pin (QFN32)	Pin (QFN20)	Type	Equivalent Circuit	Description
Card Interface					
I/O	22	14	IO	Figure 17	Card I/O: Data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
AUX1	21	N/A	IO	Figure 17	AUX1: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
AUX2	20	N/A	IO	Figure 17	AUX2: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
RST	18	12	O	Figure 16	Card reset: provides reset (RST) signal to card. RST is the pass through signal on RSTIN. Internal control logic will hold RST low when card is not activated or VCC is too low.
CLK	16	10	O	Figure 15	Card clock: provides clock signal (CLK) to card. CLK is the pass through of the signal on pin CLKIN. Internal control logic will hold CLK low when card is not activated or VCC is too low.
PRES	14	8	I	Figure 19	Card Presence switch: active high indicates card is present. Should be tied to GND when not used, but it Includes a high-impedance pull-down current source.
$\overline{\text{PRES}}$	13	N/A	I	Figure 19	Card Presence switch: active low indicates card is present. Should be tied to V_{DD} when not used, but it Includes a high-impedance pull-up current source.
VCC	19	13	PSO	Figure 14	Card power supply – logically controlled by sequencer, output of LDO regulator. Requires an external 0.47 µF low ESR filter capacitor to GND.
GND	17	11	GND	–	Card ground.
Miscellaneous Inputs and Outputs					
CLKIN	7	6	I	Figure 19	Clock signal source for the card clock.
TEST1	10	7	–	–	Factory test pin. This pin must be tied to GND in typical applications
TEST2	30	20	–	–	Factory test pin. This pin must be tied to GND in typical applications
Power Supply and Ground					
VDD	29	19	PSO	Figure 14	System interface supply voltage and supply voltage for companion controller circuitry. Requires a minimum of two 0.1 µF capacitors to ground for proper decoupling.

Pin Name	Pin (QFN32)	Pin (QFN20)	Type	Equivalent Circuit	Description
VPC	26	16	PSI	Figure 14	Power supply source for main voltage converter circuit. A 10 µF and a 0.1 µF ceramic capacitor must be connected to this pin.
VBAT	25	N/A			Alternate power source input, typically from two series cells, V > 4 V.
VBUS	23	N/A			Alternate power source input from USB connector or hub.
LIN	27	17	PSI	Figure 14	Connection to 10 µH inductor for internal step up converter. Note: inductor must be rated for 400 mA maximum peak current.
VP	15	9	PSO	Figure 14	Intermediate output of main converter circuit. Requires an external 4.7 µF low ESR filter capacitor to GND
GND	28,31	18		–	Ground.
Microcontroller Interface					
CS	12	N/A	I	Figure 19	When CS = 1, the control and signal pins are configured normally. When CS is set low, $\overline{\text{CMDVCC5}}$, RSTIN, and $\overline{\text{CMDVCC3}}$. are latched. I/OUC, AUX1UC, and AUX2UC are set to high-impedance pull-up mode and do not pass data to or from the smart card. Signals RDY and OFF are disabled to prevent a low output and the internal pull-up resistors are disconnected.
$\overline{\text{OFF}}$	32	1	O	Figure 13	Interrupt signal to the processor. Active Low - Multi-function indicating fault conditions and card presence. Open drain output configuration – It includes an internal 20 kΩ pull-up to $V_{DD.}$ Pull-up is disabled in Power down state and CS = 0 modes.
I/OUC	1	2	IO	Figure 18	System controller data I/O to/from the card. Includes a pull-up resistor to $V_{DD.}$
AUX1UC	2	N/A	IO	Figure 18	System controller auxiliary data I/O to/from the card. Includes a pull-up resistor to $V_{DD.}$
AUX2UC	3	N/A	IO	Figure 18	System controller auxiliary data I/O to/from the card. Includes a pull-up resistor to $V_{DD.}$

Pin Name	Pin (QFN32)	Pin (QFN20)	Type	Equivalent Circuit	Description
$\overline{\text{CMDVCC5}}$ $\overline{\text{CMDVCC3}}$	4 5	3 4	I I	Figure 19	Logic low on one or both of these pins will cause the LDO to ramp the Vcc supply to the smart card and smart card interface to the value described in the following table. $\overline{\text{CMDVCC5}}$ $\overline{\text{CMDVCC3}}$ Vcc Output Voltage 0 0 1.8 V 0 1 5.0 V 1 0 3.0 V 1 1 LDO Off Note: See the description of the Card Power Supply for more detail on the operation of $\overline{\text{CMDVCC5}}$ and $\overline{\text{CMDVCC3}}$.
RSTIN	6	5	I	Figure 19	Reset Input: This signal is the reset command to the card.
RDY	8	N/A		Figure 13	Signal to controller indicating the 73S8009C is ready because V_{CC} is above the required value after $\overline{\text{CMDVCC5}}$ and/or $\overline{\text{CMDVCC3}}$ is asserted low. A 20 kΩ pull-up resistor to V_{DD} is provided internally. Pull-up is disabled in Power down state and CS=0 modes.
ON_OFF	24	15	I	Figure 12	Power control pin. Connected to normally open SPST switch to ground. Closing switch for duration greater than de-bounce period will turn 73S8009C circuit “on.” If 73S8009C is “on,” closing switch will turn 73S8009C to “off” state after the de-bounce period and OFF_REQ/OFF_ACK handshake.
OFF_REQ	11	N/A	O	Figure 20	Digital output. Request to the host system controller to turn the 73S8009C off. If ON_OFF switch is closed (to ground) for de-bounce duration and circuit is “on,” OFF_REQ will go high (Request to turn OFF). Connected to OFF_ACK via 100 kΩ internal resistor.
OFF_ACK	9	N/A	I	Figure 19	Setting OFF_ACK high will power “off” all analog functions and disconnect the 73S8009C from V_{BAT} or V_{PC}. The pin has an internal 100 kΩ resistor connection to OFF_REQ so that when not connected or no host interaction is required, the Acknowledge will be true and the circuit will turn “off” immediately with OFF_REQ.

2 Electrical Specifications

This section provides the following:

- Absolute maximum ratings
- Recommended operating conditions
- Smart card interface requirements
- Digital signals characteristics
- Voltage / temperature fault detection circuits
- Thermal characteristics

2.1 Absolute Maximum Ratings

Table 2 lists the maximum operating conditions for the 73S8009C. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to the extremes of the absolute maximum rating for extended periods may affect device reliability. The smart card interface pins are protected against short circuits to V_{CC}, ground, and each other.

Table 2: Absolute Maximum Device Ratings

Parameter	Rating
Supply Voltage V_{BUS}	-0.5 to 6.6 VDC
Supply Voltage V_{BAT}	-0.5 to 6.6 VDC
Supply Voltage V_{PC}	-0.5 to 6.6 VDC
V_{DD}	-0.5 to 4.0 VDC
Input Voltage for Digital Inputs	-0.3 to (V_{DD} +0.5) VDC
Storage Temperature	-60 to 150°C
Pin Voltage (except card interface)	-0.3 to (V_{DD} + 0.5) VDC
Pin Voltage (card interface)	-0.3 to (V_{CC} + 0.3) VDC
Pin Voltage, LIN pin	0.3 to 6.5 VDC
ESD Tolerance – Card interface pins	+/- 6 kV
ESD Tolerance – Other pins	+/- 2 kV
Pin Current, except LIN	± 200 mA
Pin Current, LIN	+ 500 mA in, -200 mA out

Note: ESD testing on smart card pins is HBM condition, 3 pulses, each polarity referenced to ground.
Note: Smart Card pins are protected against shorts between any combinations of Smart Card pins.

2.2 Recommended Operating Conditions

Function operation should be restricted to the recommended operating conditions specified in Table 3.

Table 3: Recommended Operating Conditions

Parameter	Rating
Supply voltage V_{PC}	2.7 to 6.5 VDC
Supply Voltage V_{BUS}	4.4 to 5.5 VDC
Supply Voltage V_{BAT}	4.0 to 6.5 VDC
Ambient operating temperature	-40 °C to +85 °C

2.3 Smart Card Interface Requirements

Table 4 lists the 73S8009C Smart Card interface requirements.

Table 4: DC Smart Card Interface Requirements

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Card Power Supply (V_{CC}) Regulator General Conditions: -40C < 85C, 2.7 V < V_{PC} < 6.6 V						
V_{CC}	Card supply voltage including ripple and noise	Inactive mode	-0.1	–	0.1	V
		Inactive mode I_{CC} = 1 mA	-0.1	–	0.4	V
		Active mode; I_{CC} <65 mA; 5 V	4.65	–	5.25	V
		Active mode; I_{CC} < 65 mA; 3 V	2.85	–	3.15	V
		Active mode; I_{CC} < 40 mA; 1.8 V	1.68	–	1.92	V
		Active mode; single pulse of 100 mA for 2 μs; 5 V, fixed load = 25 mA	4.6	–	5.25	V
		Active mode; single pulse of 100 mA for 2 μs; 3 V, fixed load = 25 mA	2.76	–	3.15	V
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200 mA, t <400 ns; 5 V	4.6	–	5.25	V
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200 mA, t <400 ns; 3 V	2.7	–	3.15	V
		Active mode; current pulses of 20nAs with peak $\|I_{CC}\|$ <100 mA, t <400 ns; 1.8 V	1.62	–	1.92	V
V_{CCrip}	V_{CC} ripple	f_{RIPPLE} = 20 kHz – 200 MHz		–	350	mV
I_{CCmax}	Card supply output current	Static load current, V_{CC}>1.65		–	40	mA
		Static load current, V_{CC}>4.6 or 2.7 volts as selected		–	65	mA
I_{CCF}	I_{CC} fault current	Class A, B (5 V and 3 V)	75	–	150	mA
		Class C (1.8 V)	55	–	130	mA
I_{SC}	Maximum current prior to shut-down	Load current limit prior to Vcc shut-down	80	–	150	mA.
		Load current limit prior to Vcc shut-down for Vcc=1.8 V	60	–	130	mA

V_S	Vcc slew rate, rise and fall	C = 0.5 μF	0.10	0.30	0.70	V/μs
V_{rdy}	Vcc ready voltage (RDY = 1)	5 V operation, Vcc rising	4.6	–	–	V
		3 V operation, Vcc rising	2.75	–	–	V
		1.8 V operation, Vcc rising	1.65	–	–	V
V_{CCF}	RDY = 0 (V_{CC} voltage supervisor threshold)	V_{CC} = 5 V	–	–	4.6	V
C_{VPC}	External filter cap for V_{PC}		8.0	10.0	12.0	μF
Cvp	External filter cap for VP		2.0	4.7	6.8	μF
C_F	External filter capacitor (V_{CC} to GND)	C_F should be ceramic with low ESR (<100mΩ).	0.2	0.47	1.0	μF
C_{VDD}	VDD filter capacitor		0.2	–	1.0	μF
Ivpcoff	VPC supply current for Vcc=0	Vpc=5 V, Vcc=0 V (off)			400	μA

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Interface Requirements – Data Signals: I/O, AUX1, AUX2, and host interfaces: I/OUC, AUX1UC, AUX2UC, DP, DM. I_{SHORTL}, I_{SHORTH}, and V_{INACT} requirements do not pertain to I/OUC, AUX1UC, AUX2UC						
V_{OH}	Output level, high (I/O, AUX1, AUX2)	I_{OH} =0	0.9 * V_{CC}	–	V_{CC}+0.1	V
V_{OH}	Output level, high (I/OUC, AUX1UC, AUX2UC)	I_{OH} = -40 µA	0.75 V_{CC}	–	V_{CC}+0.1	V
		I_{OH} =0	0.9 V_{DD}	–	V_{DD}+0.1	V
V_{OL}	Output level, low (I/O, AUX1, AUX2)	I_{OH} = -40 µA	0.75 V_{DD}	–	V_{DD}+0.1	V
		I_{OL}=1 mA	–	–	0.15 *V_{CC}	V
V_{OL}	Output level, low (I/OUC, AUX1UC, AUX2UC)	I_{OL}=1 mA	–	–	0.3	V
V_{IH}	Input level, high (I/O, AUX1, AUX2)		0.6 * V_{CC}	–	V_{CC}+0.30	V
V_{IH}	Input level, high (I/OUC, AUX1UC, AUX2UC)		0.6 * V_{DD}	–	V_{DD}+0.30	V
V_{IL}	Input level, low (I/O, AUX1, AUX2)		-0.15	–	0.2 * V_{CC}	V
V_{IL}	Input level, low (I/OUC, AUX1UC, AUX2UC)		-0.15	–	0.2 * V_{DD}	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0	–	–	0.1	V
		I_{OL} = 1 mA	–	–	0.3	V
I_{LEAK}	Input leakage	V_{IH} = V_{CC}	–	–	10	µA
I_{IL}	Input current, low (I/O, AUX1, AUX2)	V_{IL} = 0	–	–	0.65	mA
I_{IL}	Input current, low (I/OUC, AUX1UC, AUX2UC)	V_{IL} = 0	–	–	0.7	mA
I_{SHORTL}	Short circuit output current	For output low, shorted to V_{CC} through 33 Ω	–	–	15	mA
I_{SHORTH}	Short circuit output current	For output high, shorted to ground through 33 Ω	–	–	15	mA
t_R, t_F	Output rise time, fall times	For I/O, AUX1, AUX2, C_L = 80pF, 10% to 90%. For I/OUC, AUX1UC, AUX2UC, CL=50Pf, 10% to 90%.	–	–	100	ns
t_{IR}, t_{IF}	Input rise, fall times		–	–	1	µs
R_{PU}	Internal pull-up resistor	Output stable for >200ns	8	11	14	kΩ
FD_{MAX}	Maximum data rate		–	–	1	MHz
T_{FDIO}	Delay, I/O to I/OUC, AUX1 to AUX1UC, AUX2 to AUX2UC,I/OUC to I/O, AUX1UC to AUX1, AUX2UC to AUX2 (respectively falling edge to falling edge and rising edge to rising edge)	Edge from master to slave, measured at 50%	60	100	200	ns
T_{RDIO}			–	15	–	ns
C_{IN}	Input capacitance		–	–	10	pF

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Reset and Clock for card interface, RST, CLK						
V_{OH}	Output level, high	I_{OH} =-200 µA	0.9 * V_{CC}	–	V_{CC}	V
V_{OL}	Output level, low	I_{OL}=200 µA	0	–	0.15 *V_{CC}	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0	–	–	0.1	V
I_{RST_LIM}	Output current limit, RST		–	–	30	mA
I_{CLK_LIM}	Output current limit, CLK		–	–	70	mA
t_R, t_F	Output rise time, fall time	C_L = 35pF for CLK, 10% to 90%	–	–	12	ns
		C_L = 200pF for RST, 10% to 90%	–	–	100	ns
δ	Duty cycle for CLK	C_L =35pF, F_{CLK} ≤ 20 MHz, CLKIN duty cycle is 48% to 52%.	45	–	55	%

2.4 Digital Signals Characteristics

Table 5 lists the 73S8009C digital signals characteristics.

Table 5: Digital Signals Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
Digital I/O (except for I/OUC, AUX1UC, AUX2UC; see Smart Card Interface Requirements for those specifications)						
V_{IL}	Input Low Voltage		-0.3	–	0.8	V
VIL_{OFFACK}	Input low voltage for OFF_ACK pin	OFF_REQ pin = VDD	-0.3	–	0.7	V
V_{IH}	Input High Voltage		1.8	–	V_{DD} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		–	0.45	V
V_{OH}	Output High Voltage	I_{OH} = -1 mA	V_{DD} - 0.45	–		V
R_{OUT}	Pull-up resistor; $\overline{OFF}$, RDY		14	20	26	kΩ
R_{ACK}	Resistor between OFF_REQ and 0FF_ACK		70	100	130	kΩ
$\vert I_{IL1}\vert$	Input Leakage Current	GND < V_{IN} < V_{DD}	–	–	5	µA
t_{SL}	Time from CS goes high to interface active		50	–	–	ns
t_{DZ}	Time from CS goes low to interface inactive, Hi-Z		50	–	–	ns
t_{IS}	Set-up time, control signals to CS rising edge		50	–	–	ns
t_{SI}	Hold time, control signals from CS rising edge		–	–	50	ns
t_{ID}	Set-up time, control signals to CS fall		50	–	–	ns
t_{DI}	Hold time, control signals from CS fall		–	–	50	ns

2.5 DC Characteristics

Table 6 lists the DC characteristics.

Table 6: DC Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	V_{DD} Supply Voltage	2.7v < VPC < 6.5v, I_{VDDEXT} < 40 mA.	3.0	3.3	3.6	V
I_{DDEXT}	V_{DD} Current to External Load		–	–	40	mA
I_{VPC}	Supply Current	Vpc = 2.7V, V_{CC} off, I_{DD} = 0	–	1.7	–	mA
		Vpc = 3.3V, V_{CC} off, I_{DD} = 0	–	1.1	–	mA
		Vpc = 5.0V, V_{CC} off, I_{DD} = 0	–	0.7	–	mA
		OFF mode	–	0.01	1	µA
$VBUS_{ON}$	VBUS detection threshold	V_{DD} =3.3 V	3.5	3.9	4.3	V
$VBUS_{IDIS}$	VBUS discharge current		0.5	1.0	3	mA
$VBUS_{STBY}$	VBUS standby current			370	500	µA

2.6 Voltage / Temperature Fault Detection Circuits

Table 7 lists the voltage / temperature fault detection circuits.

Table 7: Voltage / Temperature Fault Detection Circuits

Symbol	Parameter	Condition	Min	Nom	Max	Unit
IV_{Pmax}	V_P over-current fault		–	–	150	mA
I_{CCF}	Card overcurrent fault		80	–	150	mA
I_{CCF1P8}	Card overcurrent fault	V_{CC} = 1.8 V	60	–	130	mA

2.7 Thermal Characteristics

Table 8 lists the thermal characteristics.

Table 8: Thermal Characteristics

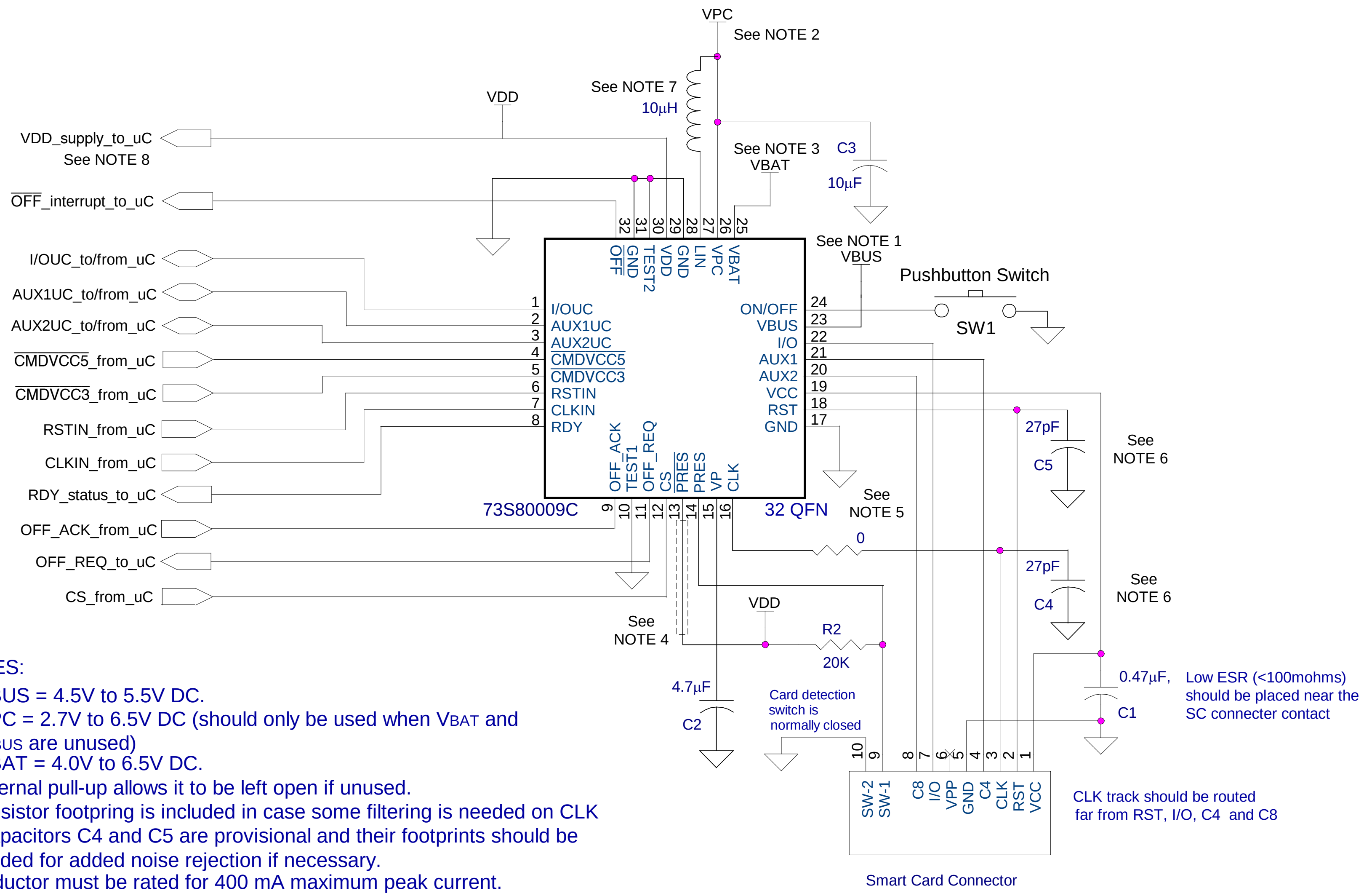
Symbol	Parameter	Condition	Min	Nom	Max	Unit
Tj	Junction temperature		–	–	125	°C
θ ja	Thermal Resistance, Junction-to-Ambient		–	70	–	°C/W
θ jc	Thermal Resistance, Junction-to-case		–	6	–	°C/W

3 Applications Information

This section provides general usage information for the design and implementation of the 73S8009C. The documents listed in Related Documentation provide more detailed information.

3.1 Example 73S8009C Schematics

Figure 4 shows a typical application schematic for the implementation of the 73S8009C with a main system switch. Note that minor changes may occur to the reference material from time to time and the reader is encouraged to contact Teridian for the latest information.



NOTES:

1) VBUS = 4.5V to 5.5V DC.
2) VPC = 2.7V to 6.5V DC (should only be used when VBAT and VBUS are unused)
3) VBAT = 4.0V to 6.5V DC.
4) Internal pull-up allows it to be left open if unused.
5) Resistor footpring is included in case some filtering is needed on CLK
6) Capacitors C4 and C5 are provisional and their footprints should be added for added noise rejection if necessary.
7) Inductor must be rated for 400 mA maximum peak current.
8) VDD - 3.3V, +/- 0.3V, 40mA max. Requires min two 0.1µF caps to gnd)

Figure 4: Typical 73S8009C Application Schematic

3.2 Power Supply and Converter

The power supply and converter circuit takes power from any one of three sources; V_{PC}, V_{BUS}, and V_{BAT}. V_{PC} is specified to range from 2.7 to 6.5 volts and would typically be supplied by a single cell battery with a voltage range of 2.7 to approximately 3.1 volts. V_{PC} is also appropriate for system supplies of 3.3 or 5 volts. V_{BUS} is typically supplied by a connected USB cable and ranges in value from 4.5 to 5.5 volts (6.5 V maximum). V_{BAT} is expected to be supplied from a battery of two series connected cells with a voltage value of 4.0 to 6.5 volts. V_{BAT} and V_{BUS} are connected to V_{PC} by two FET switches configured as a SPDT switch (break-before-make). They will not be enabled at the same time. V_{BUS} is automatically selected in lieu of V_{BAT} when V_{BUS} is present. If V_{PC} is provided and V_{BAT} or V_{BUS} are also used, the source of V_{PC} must be diode isolated from the V_{PC} pin to prevent current flow from V_{BAT} or V_{BUS} into the V_{PC} source.

The power supplied to the V_{PC} pin is up-converted to the voltage V_P utilizing an inductive, step-up converter. A series power inductor (nominal value = 10 μH) is connected from V_{PC} to LIN, and a 10 μF filter capacitor must be connected to V_{PC}. V_P requires a 4.7 μF filter capacitor and will have a nominal value of 5.5 volts during normal operation. V_P is used by the smartcard interface circuits (CLK, RST, IO, AUX1, and AUX2) and is the source of the regulated smart card supply V_{CC}. V_{CC} can be programmed for values of 5 V, 3 V, and 1.8 V. V_{DD} is also produced from V_P. V_{DD} is used by the 73S8009C circuit for logic, input/output buffering, and analog functions as well as being capable of supplying up to 40 mA of current to external devices. Figure 2 shows the block diagram of the 73S8009C.

3.3 Power ON/OFF

When no power is applied to the V_{BUS} pin, a power ON/OFF function is provided such that the circuit will be inoperative during the “OFF” state, consuming minimum current from V_{PC} and V_{BAT}. If V_{BUS} power is supplied, the functions of the ON/OFF switch and circuitry are overridden and the 73S8009C is in the “ON” state with V_P and V_{DD} available. Without V_{BUS} applied, and in the OFF state, the circuit responds only to the ON_OFF pin. The ON_OFF pin shall be connected to a SPST switch to ground. If the circuit is OFF and the switch is closed for a de-bounce period of 50-100ms, the circuit shall go into the “ON” state wherein all functions are operating in normal fashion. If the circuit is in the “ON” state and the ON_OFF pin is connected to ground for a period greater than the de-bounce period, OFF_REQ will be asserted high and held. Typically, the OFF_REQ signal is presented to a host controller that will assert OFF_ACK high when it has completed all shutdown activities. When OFF_ACK is set high, the circuit will de-activate the smart card interface if required and turn off all analog functions and the V_{DD} supply for the logic and companion circuits. The OFF_ACK pin is connected internally to OFF_REQ with a resistor such that if OFF_ACK is unconnected, the action of OFF_REQ will assert OFF_ACK high. In this configuration, the circuit shall go into the “OFF” state immediately upon OFF_REQ = 1. The default state upon application of power is the “OFF” state unless power is supplied to the V_{BUS} supply. Note that at any time, the controller may assert OFF_ACK and the 73S8009C will go into the “OFF” state (when V_{BUS} is not present.)

If power is applied to both V_{BAT} and V_{BUS}, the circuit will automatically consume power from only the V_{BUS} source. The circuit will be unconditionally “ON” when V_{BUS} is applied. If the V_{BUS} source is removed, the circuit will switchover to the VBAT input supply and remain in the “ON” state. The controller circuit firmware is required to assert OFF_ACK based on no activity or V_{BUS} removal to reduce battery power consumption. When operating from V_{BUS}, and not calling for V_{CC}, the step-up converter becomes a simple switch connecting V_{BUS} to V_P in order to save power. This condition is appropriate for the USB “SUSPEND” state. The USB “SUSPEND” state requires the power supply current to be less than 500uA. In order to obtain and meet this low current limitation, the companion controller must be configured into a power-down condition using less than 20 μA from V_{DD}.

Note: When using the VBUS input as the sole power source for an ‘always on’ configuration (ON_OFF input not used), the OFF_ACK and ON_OFF inputs must be connected to ground.

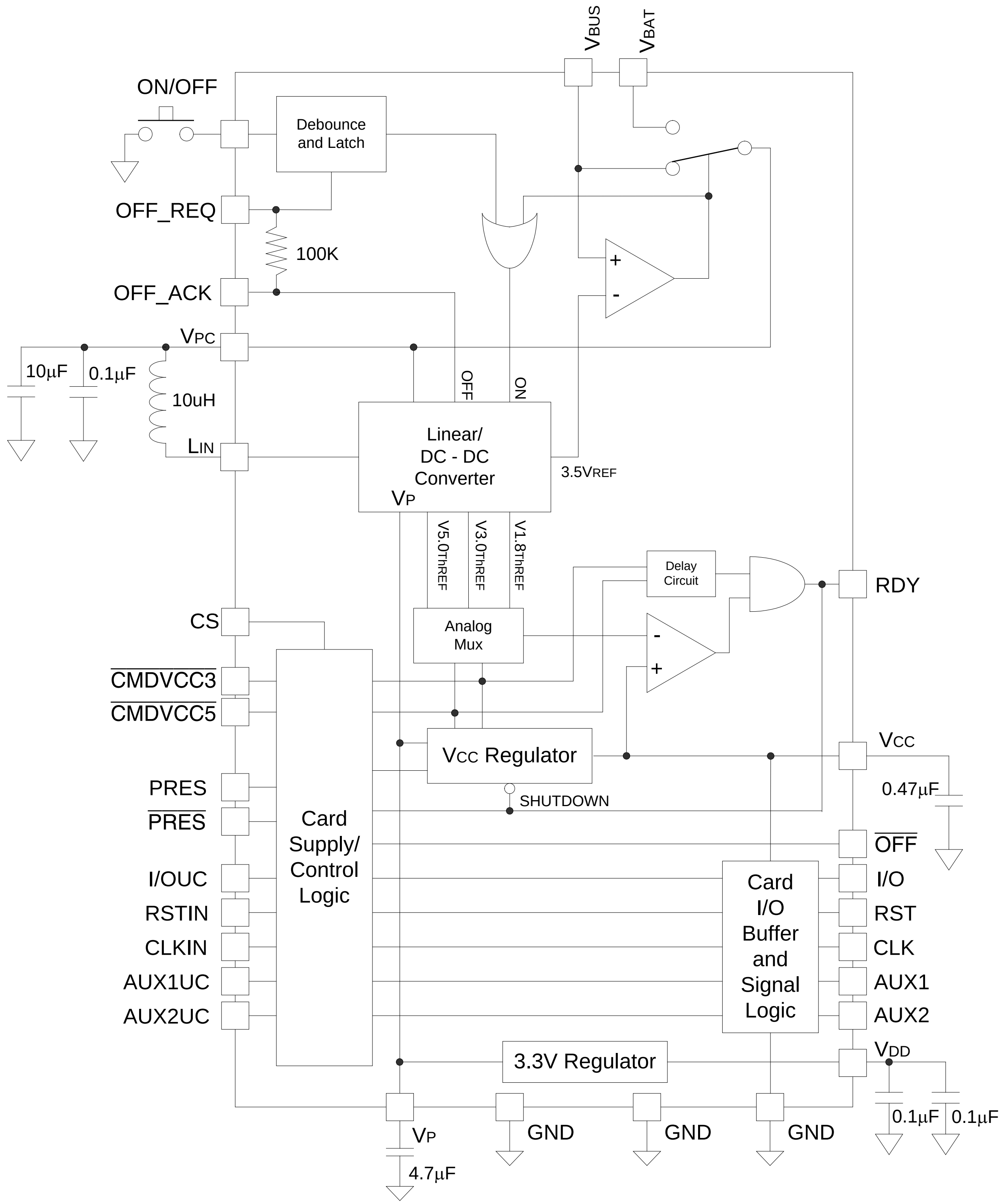


Figure 5: 73S8009C Logical Block Diagram

3.4 System Controller Interface

Four separate digital inputs and two outputs allow direct control of the card interface from the host:

- Pin CS: Chip select control.
- Pin $\overline{\text{CMDVCC3}}$ and/or $\overline{\text{CMDVCC5}}$: When low, starts an activation sequence.
- Pin RSTIN: controls the card RST signal.
- Pin RDY: Indicates when smart card power supply is stable and ready.
- Pin $\overline{\text{OFF}}$: Indicator of card presence and any card fault conditions.

Interrupt output to the host: When the card is not activated, the $\overline{\text{OFF}}$ pin informs the host about the card presence only (Low = No card in the reader, high = card inserted). When $\overline{\text{CMDVCC}}$ ($\overline{3}/\overline{5}$ signals) is/are set low (card activation sequence requested from the host), low level on $\overline{\text{OFF}}$ means a fault has been detected (e.g. card removal during card session, or voltage fault, or thermal / over-current fault) that automatically initiates a deactivation sequence. The smart card pass through signals are enabled when the RDY conditions are met.

3.5 Card Power Supply and Voltage Supervision

The 73S8009C smart card interface IC incorporates an LDO voltage regulator for the card power supply, V_{CC} (V_P to V_{CC} conversion uses an internal LDO). The voltage output is controlled by the digital input sequence of $\overline{\text{CMDVCC3}}$ and $\overline{\text{CMDVCC5}}$. This regulator is able to provide 1.8V, 3V or 5V card voltage sourced from the V_P power supply. Internal digital circuitry is also powered by the V_P power supply (except for the ON/OFF circuitry which is powered from V_{PC}). . A card deactivation sequence is forced upon fault detected by an overcurrent condition or card removal event. The voltage regulator can provide a card current of 65 mA in compliance with EMV 4.1 for 3-V and 5-V cards and 40 mA for 1.8 V cards. The signals $\overline{\text{CMDVCC3}}$ and $\overline{\text{CMDVCC5}}$ control the turn-on, output voltage value, and turn-off of V_{CC}. When either signal is asserted low, V_{CC} will ramp to the selected value or if both signals are asserted low (within 400ns of each other), V_{CC} will ramp to 1.8V. These signals are edge triggered. If $\overline{\text{CMDVCC5}}$ is asserted low (to command V_{CC} to be 5V) and at a much later time (greater than 2 µs, typically), $\overline{\text{CMDVCC3}}$ is asserted low, it will be ignored (and vice versa.)

At the assertion (low) of either or both $\overline{\text{CMDVCC}}$ ($\overline{3}/\overline{5}$ signals), V_{CC} will rise to the requested value. When V_{CC} rises to an acceptable value, and stays above that value for approximately 20 µs, RDY will be set high. Approximately 510 µs after the fall of $\overline{\text{CMDVCC}}$ ($\overline{3}/\overline{5}$), the circuit will check the see if V_{CC} is at or above the required minimum value (indicated by RDY=1) and if not, will begin an emergency deactivation sequence. During the 510 µs time, card removal, or de-assertion of $\overline{\text{CMDVCC}}$ ($\overline{3}/\overline{5}$) shall also initiate an emergency deactivation sequence. The circuit provides over-current protection and limits Icc to 150 mA, maximum for self-protection. When an over-current condition is sensed, the circuit will invoke a de-activation sequence.

3.6 Activation and De-activation Sequence

The host controller is fully responsible for the activation sequencing of the smart card signals CLK, RST, I/O, AUX1 and AUX2. All these signals are held low by the 73S8009C when the card is in the de-activated state. Upon card activation (the fall of $\overline{\text{CMDVCC}}$ ($\overline{3}/\overline{5}$)), all the signals are held low by the 73S8009C until RDY goes high. The host should set the signals RSTIN, I/OUC, CLKIN, AUX1UC and AUX2UC low prior to activating the card and allow RDY to go high before transitioning any of these signals. In order to initiate activation, the card must be present and $\overline{\text{OFF}}$ must be high.

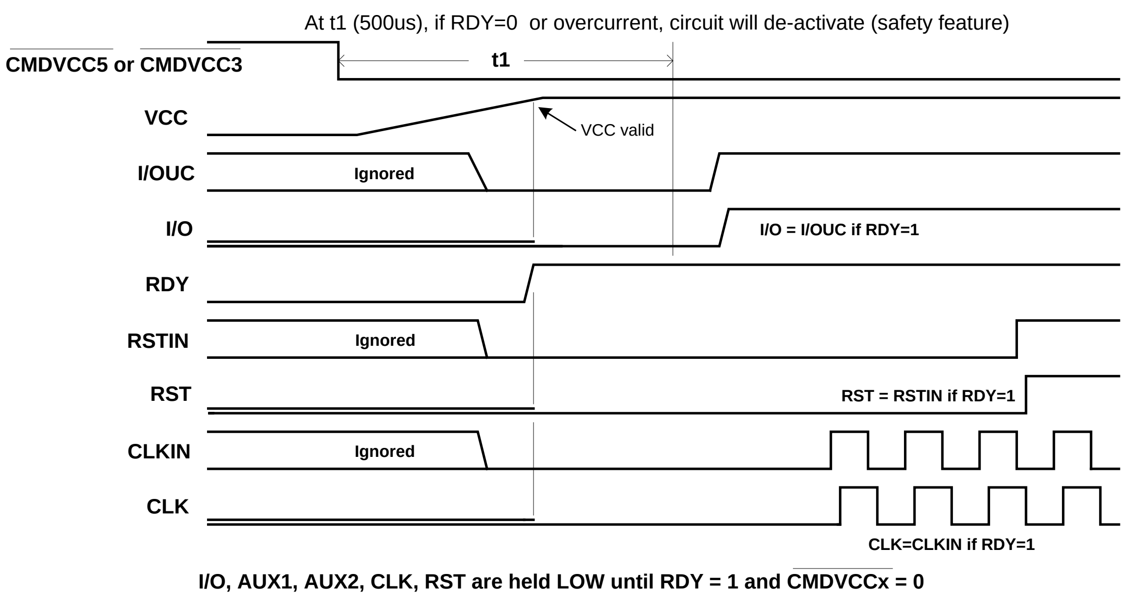


Figure 6: Activation Sequence

Deactivation is initiated either by the system controller by setting both $\overline{\text{CMDVCC}}$ ($\overline{3}/\overline{5}$) high, or automatically in the event of hardware faults or assertion of the OFF_ACK signal. Hardware faults are over-current, under-voltage, and card extraction during the session. The host can manage the I/O signals, CLKIN, RSTIN, and $\overline{\text{CMDVCC}}$ ($\overline{3}/\overline{5}$) to create other de-activation sequences for non-emergency situations.

The following steps show the deactivation sequence and the timing of the card control signals when the system controller sets the CMDVCC(x)B high:

1. RST goes low at the end of time t1.
2. De-assert CLK at the end of time t2.
3. I/O goes low at the end of time t3. Exit reception mode.
4. De-assert internal VCC_ON at the end of time t4. After a delay, VCC is de-asserted.

Note: Since the 73S8009C does not control the waveshape of CLK (it is determined by the input form the host CLKIN), there is no guarantee that the duty cycle of the last CLK high pulse will conform to duty cycle requirements during an emergency deactivation.

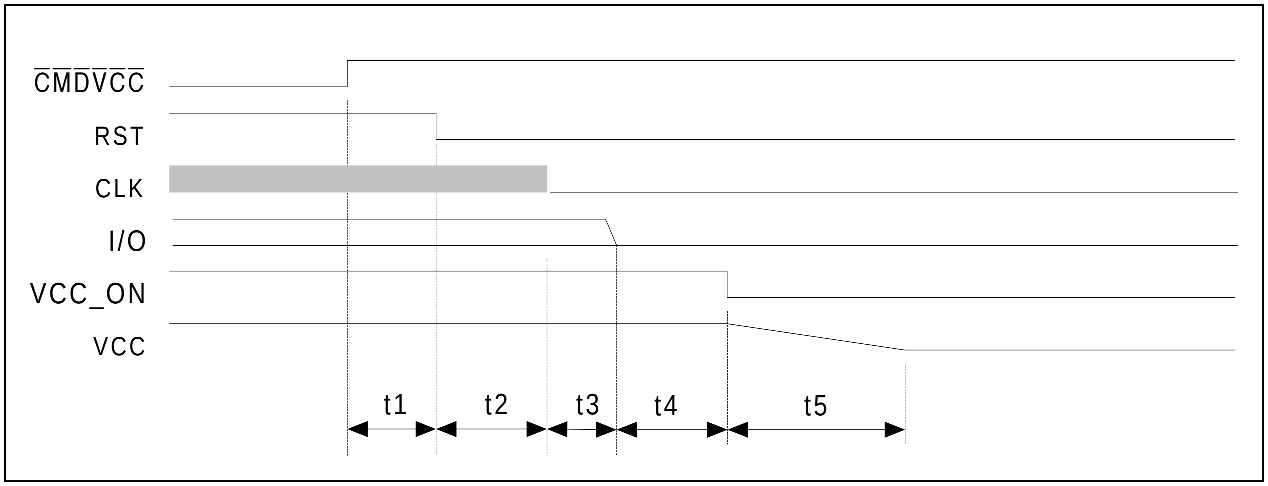


Figure 7: Deactivation Sequence

3.7 OFF and Fault Detection

There are two different cases that the system controller can monitor the OFF signal: to query regarding the card presence outside card sessions, or for fault detection during card sessions.

Outside a card session: In this condition, CMDVCC (3/5) are always high, OFF is low if the card is not present, and high if the card is present. Because it is outside a card session, no fault detection can occur and it will not act upon the OFF signal. No deactivation is required during this time.

During a card session: CMDVCC3 and/or CMDVCC5 is always low, and OFF falls low if the card is extracted or if any fault detection is detected. At the same time that OFF is set low, the sequencer starts the deactivation process and the host should stop all transitions on the signal lines.

Figure 8 shows the timing diagram for the signals CMDVCC (3/5), PRES, and OFF during a card session and outside the card session.

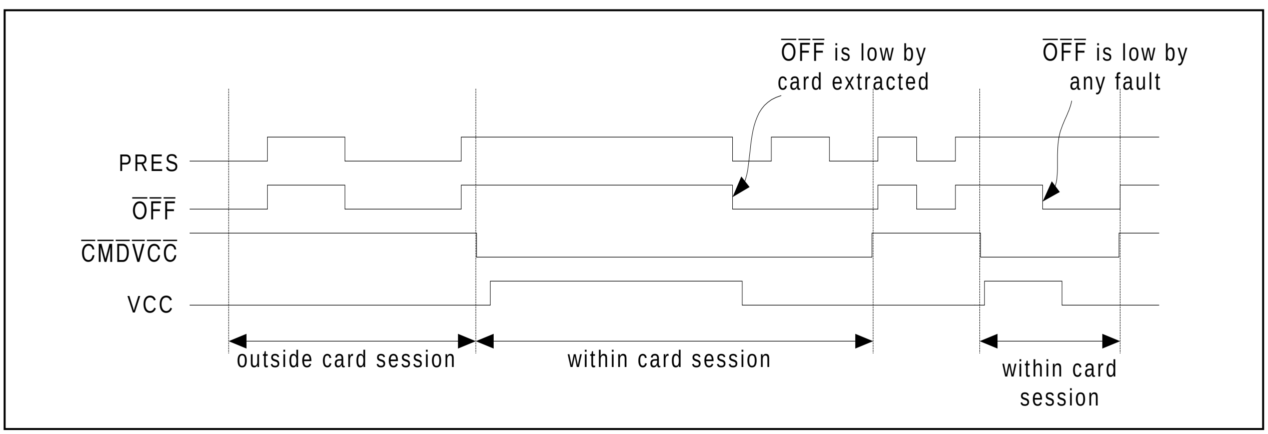


Figure 8: OFF Activity

3.8 Chip Selection

The CS pin allows multiple circuits to operate in parallel, driven from the same host control bus. When CS is high, the pins RSTIN, $\overline{\text{CMDVCC5}}$, $\overline{\text{CMDVCC3}}$ and CLKIN control the chip as described. The pins I/OUC, AUX1UC, and AUX2UC have 11 kΩ pull-up resistors and operate to transfer data to the smart card via I/O, AUX1, and AUX2 when the smart card is activated. The signals $\overline{\text{OFF}}$ and RDY have 20 kΩ pull-up resistors.

When CS goes low, the states of the pins RSTIN, $\overline{\text{CMDVCC5}}$, $\overline{\text{CMDVCC}}$, and CLKIN are latched and held internally. The pull-up for pins I/OUC, AUX1UC, and AUX2UC become a very weak pull-up of approximately 3 microamperes. No transfer of data is possible between I/OUC, AUX1UC, AUX2UC and the smart-card signals I/O, AUX1, and AUX2. The signals $\overline{\text{OFF}}$ and RDY are set to high impedance and the internal pull-up resistors of 20 kΩ are disconnected. With regard to de-activation, CS does not affect the operation of the fault sensing circuits and card sense input.

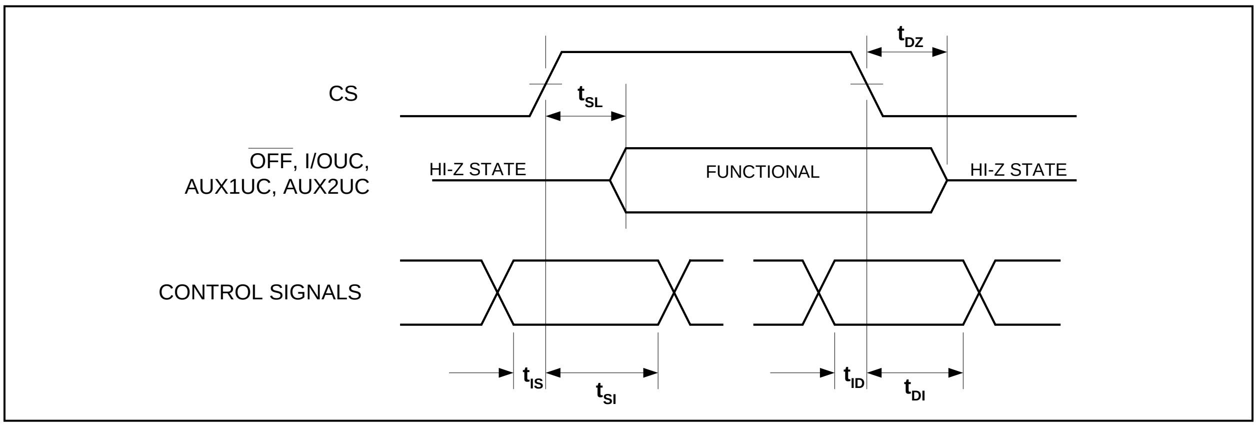


Figure 9: CS Timing Definitions

3.9 I/O Circuitry and Timing

The states of the I/O, AUX1, and AUX2 pins are low after power on reset and they are in high when the activation sequencer turns on the I/O reception state. See the Activation and De-activation Sequence section for more details on when the I/O reception is enabled. The states of I/OUC, AUX1UC, and AUX2UC are high after power on reset.

Within a card session and when the I/O reception state is turned on, the first I/O line on which a falling edge is detected becomes the input I/O line and the other becomes the output I/O line. When the input I/O line rising edge is detected, then both I/O lines return to their neutral state. Figure 10 shows the state diagram of how the I/O and I/OUC lines are managed to become input or output.

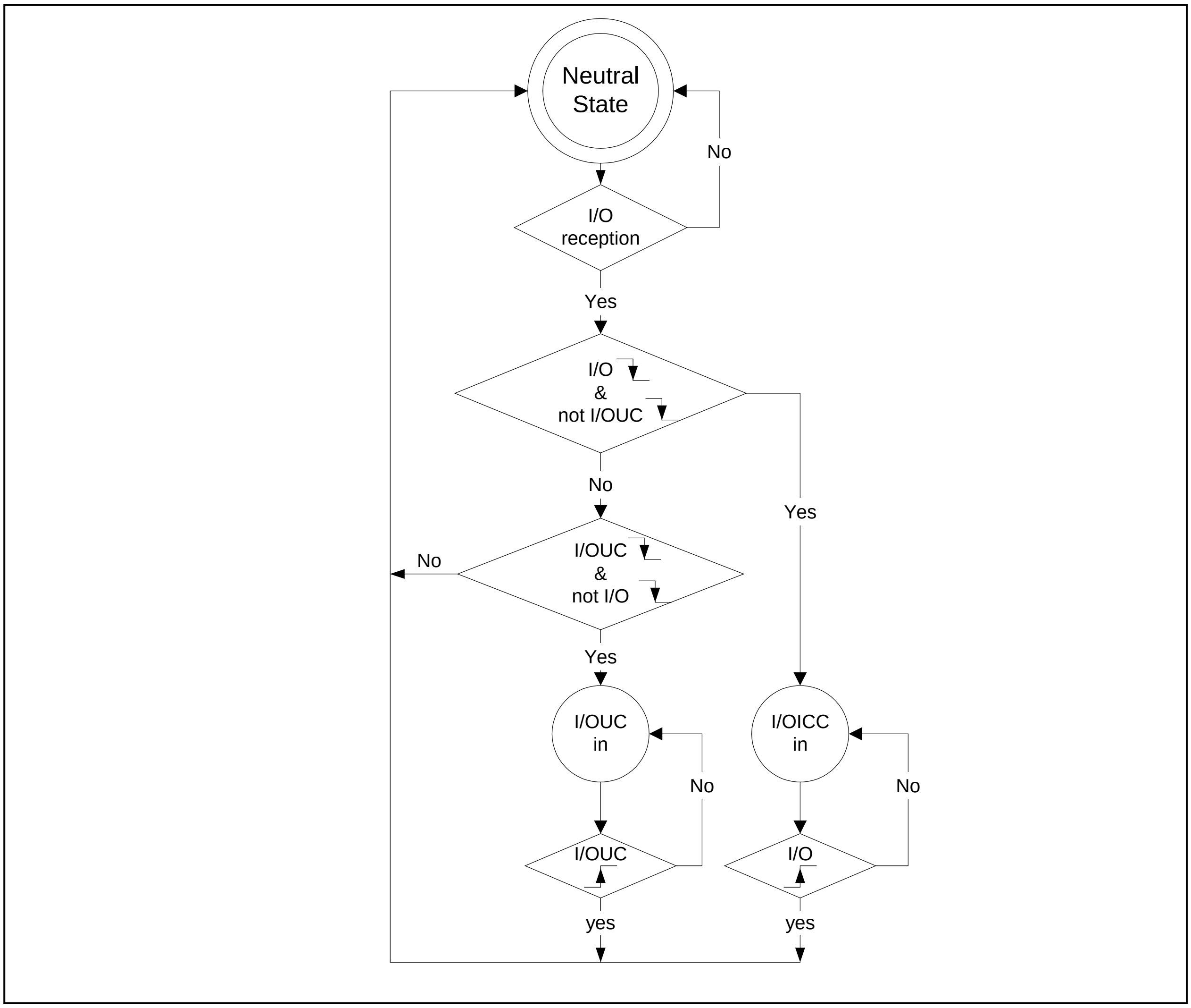
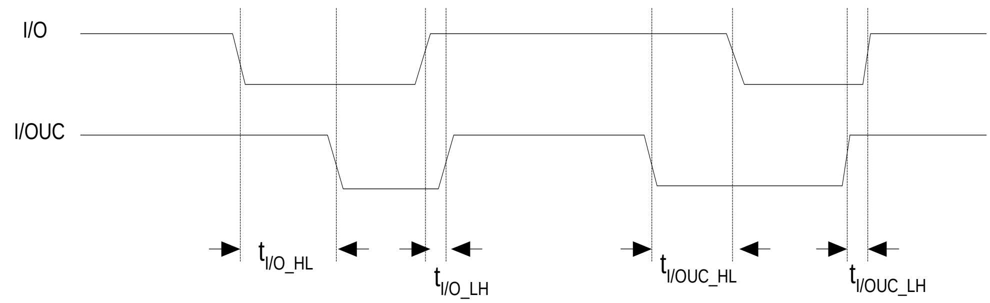


Figure 10: I/O and I/OUC State Diagram

The delay between the I/O signals is shown in Figure 11.



Delay from I/O to I/OUC:	t_{I/O_HL} = 100ns	t_{I/O_LH} = 15ns
Delay from I/OUC to I/O:	t_{I/OUC_HL} = 100ns	t_{I/OUC_LH} = 15ns

Figure 11: I/O – I/OUC Delays - Timing Diagram

4 Equivalent Circuits

This section provides illustrations of circuits equivalent to those described in the Pinout section.

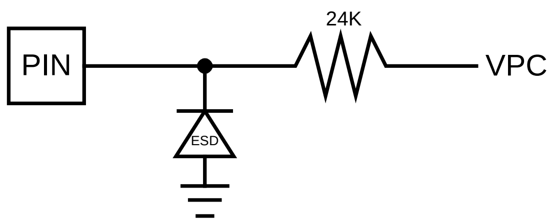


Figure 12: On_Off Pin

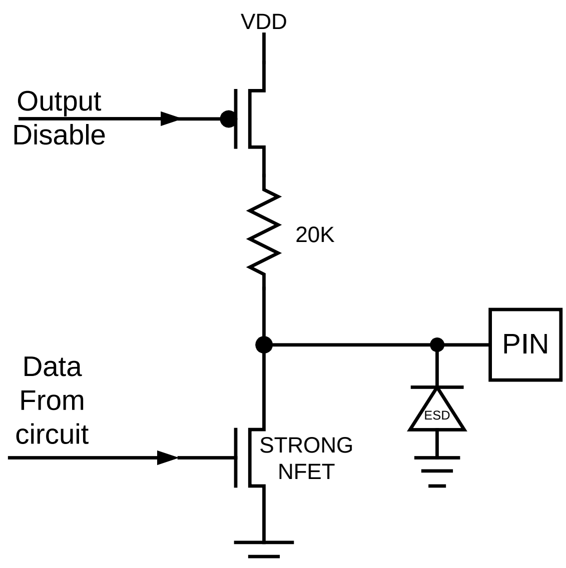


Figure 13: Open Drain type – $\overline{\text{OFF}}$ and RDY

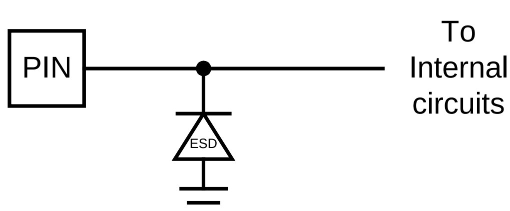


Figure 14: Power Input/Output Circuit, VDD, LIN, VPC, VCC, VP

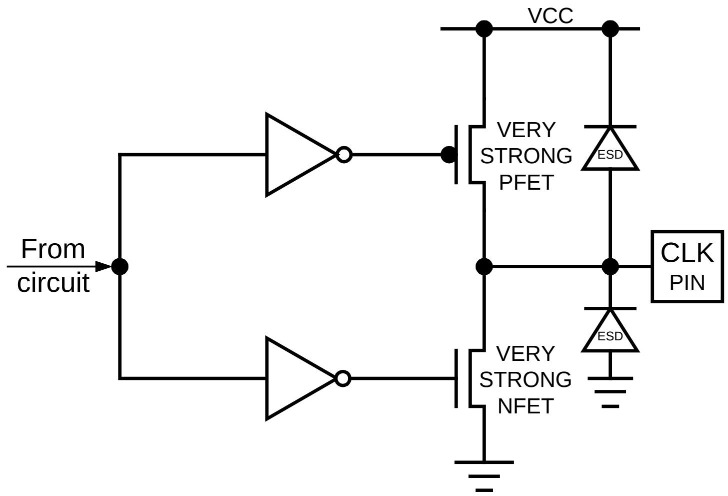


Figure 15: Smart Card CLK Driver Circuit

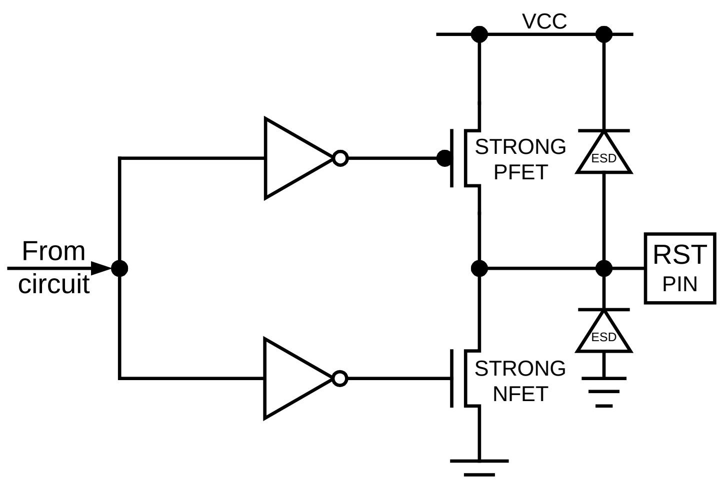


Figure 16: Smart Card RST Driver Circuit

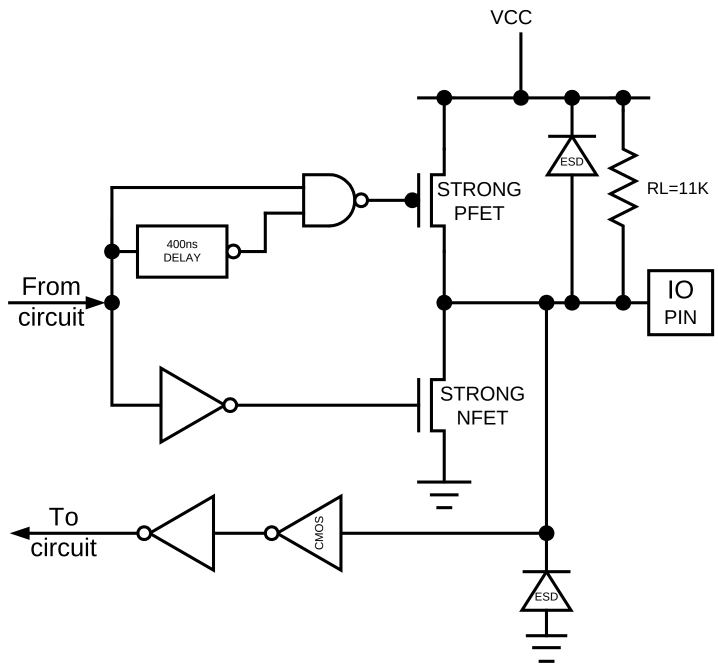


Figure 17: Smart Card IO, AUX1, and AUX2 Interface Circuit

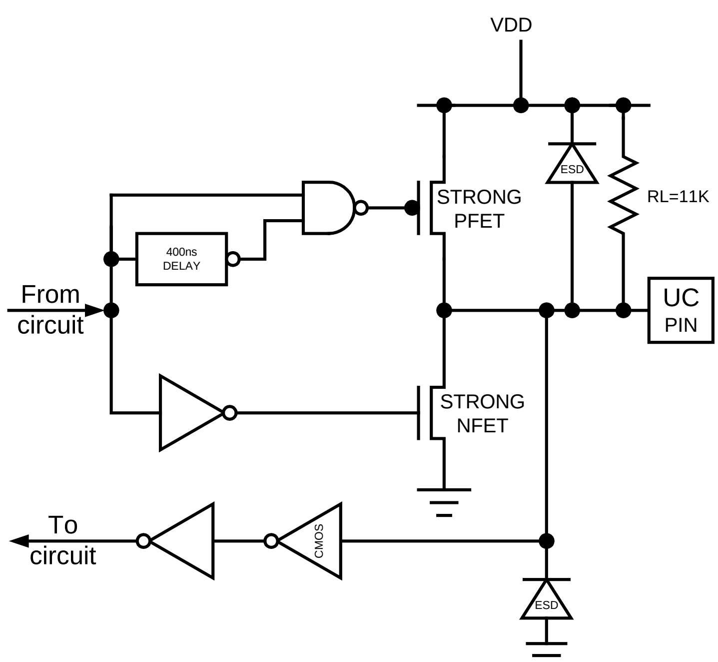
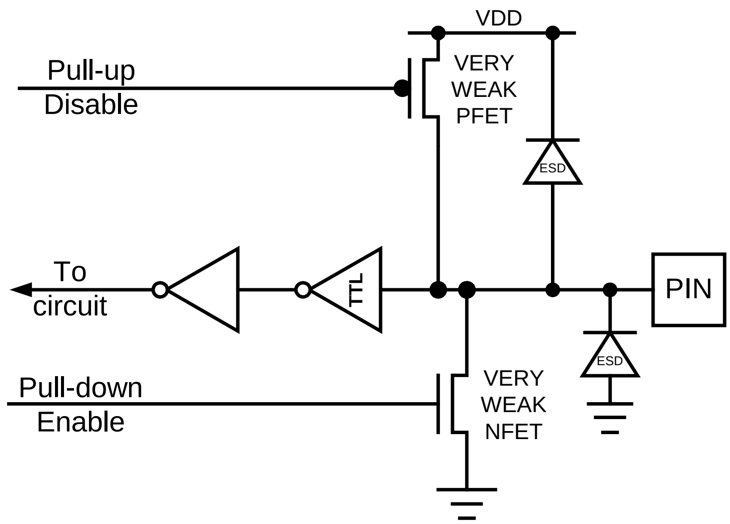
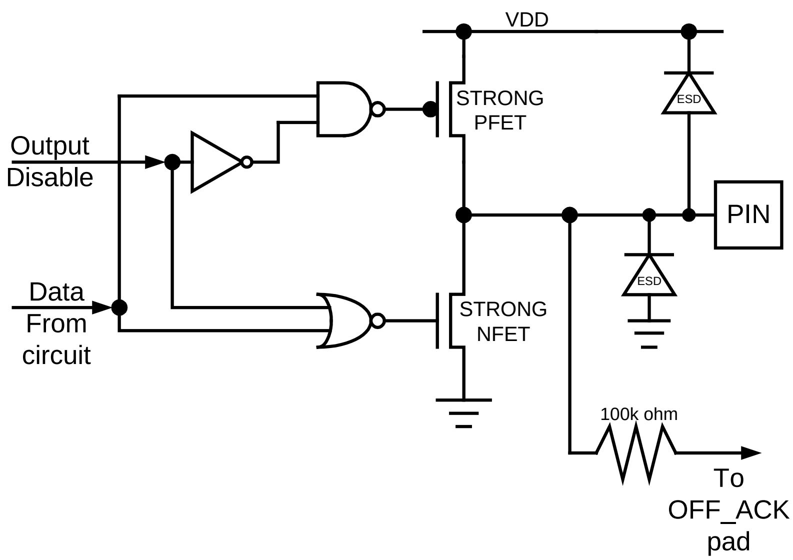


Figure 18: Smart Card I/OUC, AUX1UC and AUX2UC Interface Circuit



Note: Pins $\overline{\text{CMDVCC5}}$, $\overline{\text{CMDVCC3}}$, CS have the pull-up enabled.
Pins RSTIN, CLKIN, PRES, EXT_RST have the pull-down enabled.
Pin OFF_ACK has a 100 kΩ resistor connected to pin OFF_REQ internally.

Figure 19: General Input Circuit



Notes: Strong PFET or NFET is approximately 100 Ω
Very strong PFET or NFET is approximately 50 Ω
Medium strength PFET is approximately 1 kΩ
Very weak PFET or NFET is approximately 1 MΩ
The diodes represent ESD protection devices that will conduct current if forward biased.

Figure 20: OFF_REQ Interface Circuit

5 Mechanical Drawings

5.1 20-Pin QFN Mechanical Drawing

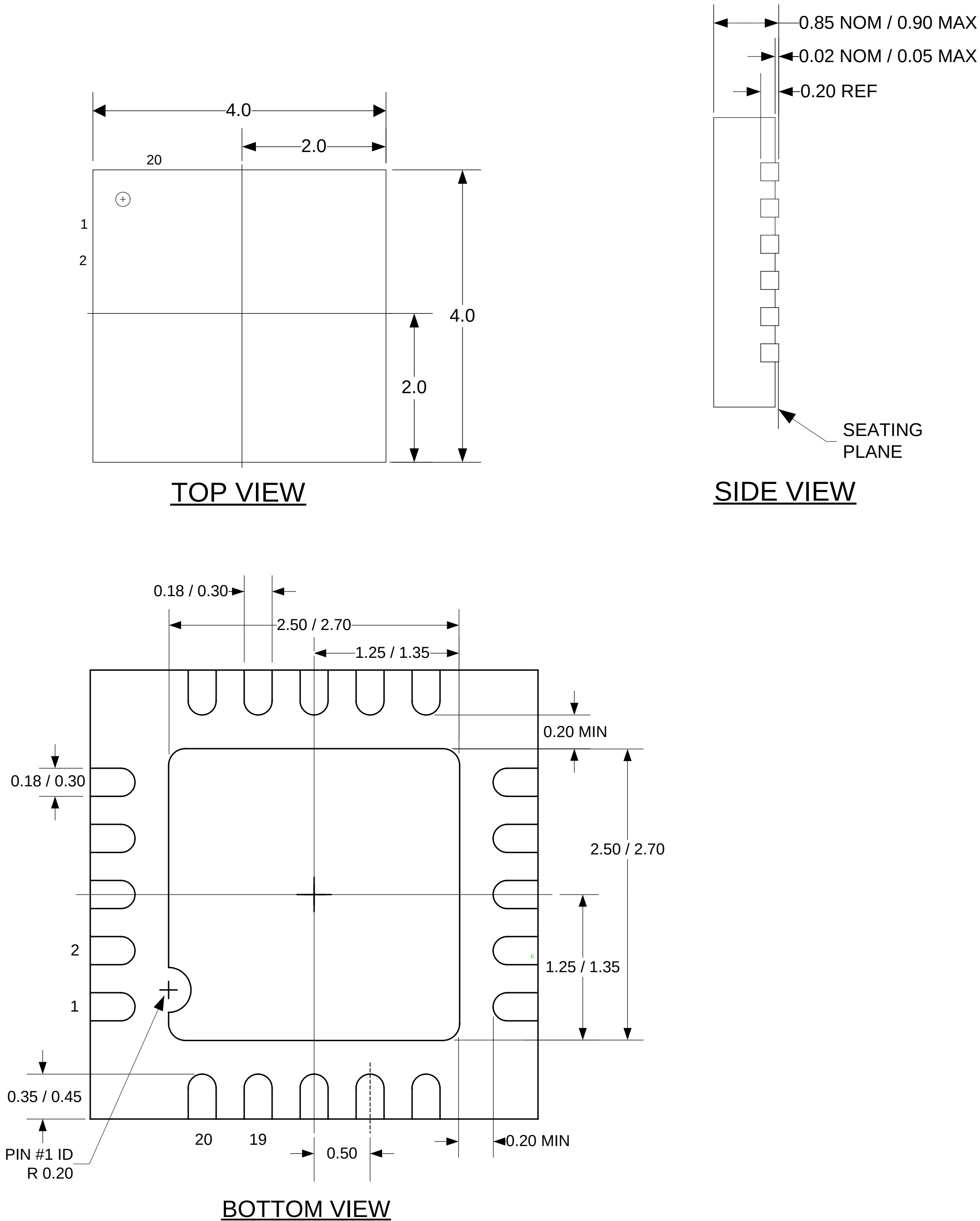


Figure 21: 20-Pin QFN Package Dimensions

5.2 32-Pin QFN Mechanical Drawing

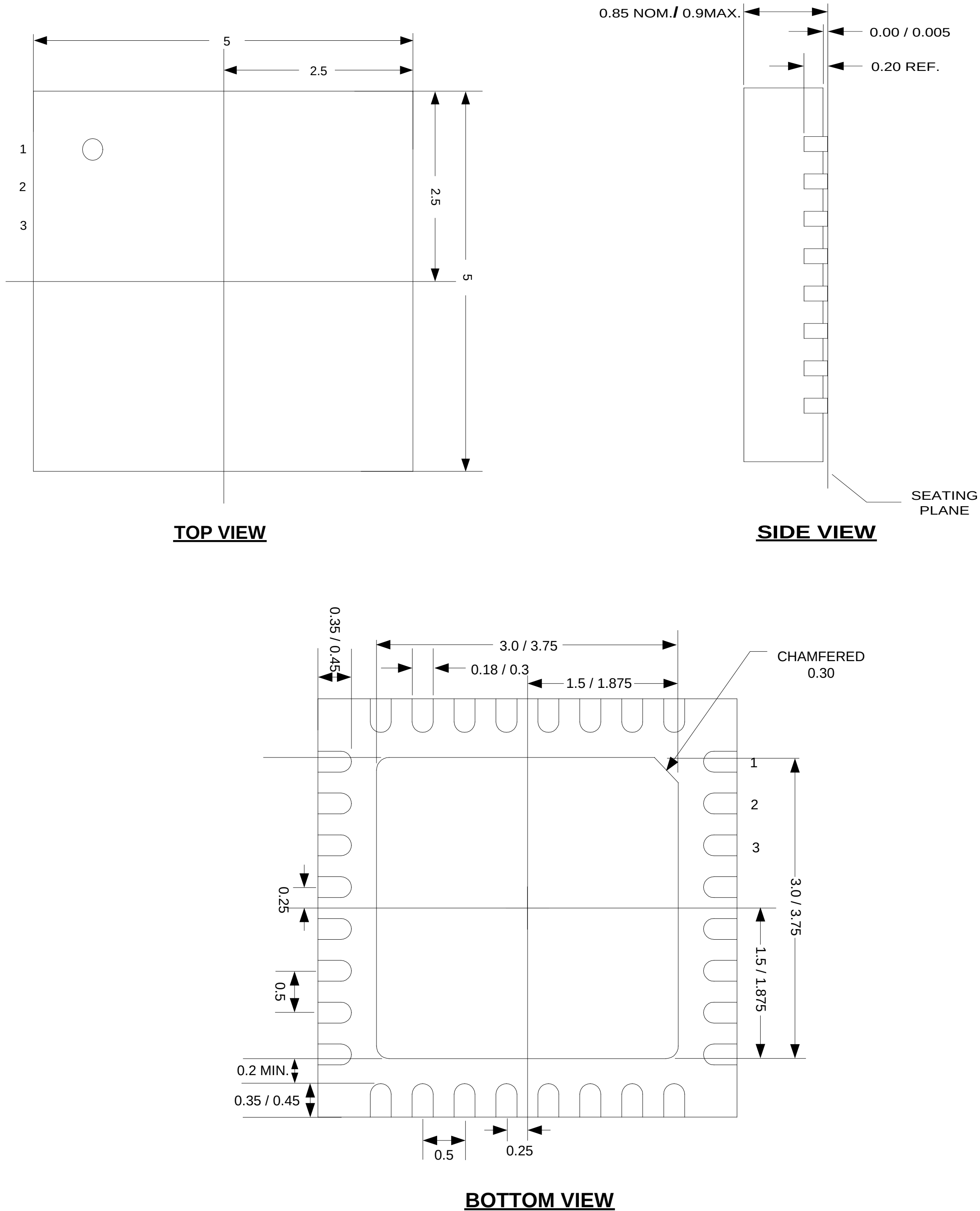


Figure 22: 32-Pin QFN Package Dimensions

6 Ordering Information

Table 9 lists the order numbers and packaging marks used to identify 73S8009C products.

Table 9: Order Numbers and Packaging Marks

Part Description	Order Number	Packaging Mark
73S8009C-20QFN 20-pin Lead-Free QFN	73S8009C-20IM/F	S8009C
73S8009C-20QFN 20-pin Lead-Free QFN Tape / Reel	73S8009C-20IMR/F	S8009C
73S8009C-32QFN 32-pin Lead-Free QFN	73S8009C-32IM/F	73S8009C
73S8009C-32QFN 32-pin Lead-Free QFN Tape / Reel	73S8009C-32IMR/F	73S8009C

7 Related Documentation

The following 73S8009C document is available from Teridian Semiconductor Corporation:

73S8009C Demo Board User's Guide

8 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S8009C, contact us at:

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For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	2/15/2007	First publication.
1.1	12/5/2007	Replaced 32 QFN punched with SAWN. Updated 32QFN package mark.
1.2	1/21/2008	Changed the dimension of the bottom view 32-pin QFN package.
1.3	8/28/2009	Added Pin Current, LIN to Table 2. Added Section 2.7, Thermal Characteristics. Added a note to the end of Section 3.6. Added Section 4, Equivalent Circuits. Added Section 7 Related Documentation and Section 8 Contact Information section. Formatted to new documentation style. Miscellaneous editorial changes.
1.4	1/5/2010	Changed the name of the "ON/OFF" pin to "ON_OFF" throughout the document. In Figure 1, corrected the name of the "IOUC" pin to "I/OUC". In Table 1, corrected the OFF_ACK name, pin number and type information. In Table 7, changed "I_{DDmax}" to "I_{VPmax}". At the end of Section 3.3, added a note about using VBUS input. In Section 3.5, deleted "A voltage supervisor checks the value of the voltage V_{CC}" and added "and 40 mA for 1.8 V cards".

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