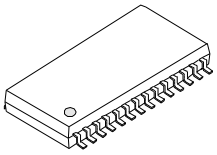
VFD CONTROLLER/DRIVER

DESCRIPTION

SC16315S is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/4 to 1/8 duty factor. It has eight segment output lines, 4 grid output lines, 4 segment/grid output drive lines, one display memory, control circuit, key scan circuit, those above are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to SC16315S via a three-line serial interface. It is housed in a 28-pin, SOP Package.



SOP-28-375-1.27

FEATURES

* CMOS Technology
* Low Power Consumption
* Key Scanning (8 x 2 matrix)
* Multiple Display Modes: (8 Segments, 8 Digits to 12 Segments, 4 Digits)
* 8-Step Dimming Circuitry
* Serial Interface for Clock, Data Input, Data Output, Strobe Pins
* No External Resistors Needed for Driver Outputs
* Available in 28-pin, SOP Package

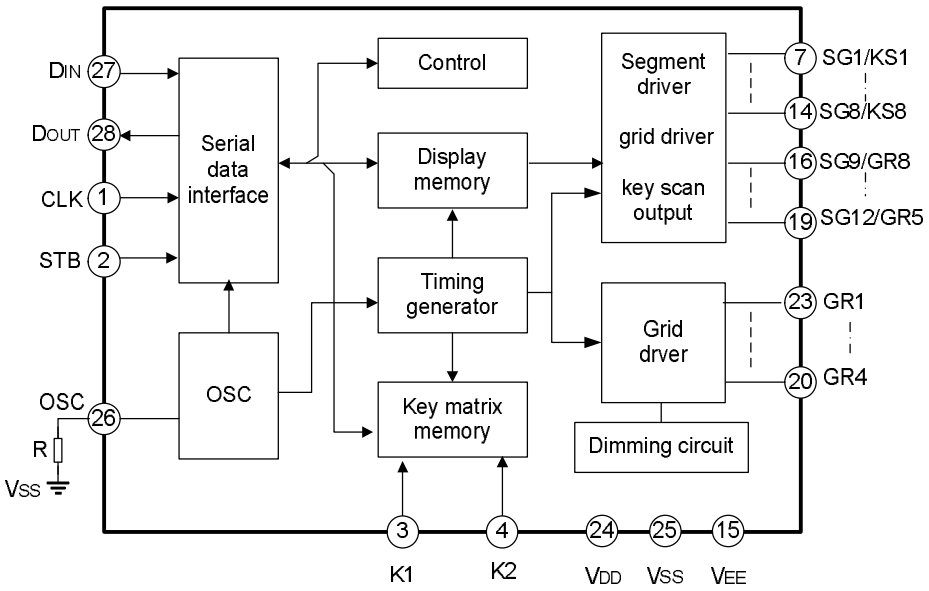
ORDERING INFORMATIONS

Device	Package
SC16315S	SOP-28-375-1.27

APPLICATIONS

* Microcomputer peripheral device

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (unless otherwise stated, T_{amb}=25°C, GND=0V)

Characteristic	Symbol	Value	Unit
Logic Supply Voltage	V_{DD}	-0.5 ~ +7	V
Driver Supply Voltage	V_{EE}	V_{DD} + 0.5 ~ V_{DD} - 40	V
Logic Input Voltage	V_I	-0.5 ~ V_{DD} + 0.5	V
VFD Driver Output Voltage	V_O	V_{EE} - 0.5 ~ V_{DD} + 0.5	V
VFD Driver Output Current	I_{OVFD}	-40(Grid) -15(Segment)	mA

RECOMMENDED OPERATING RANGE (Unless otherwise stated, T_{amb}=-20 ~ 70 °C, GND=0V)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V_{DD}	4.5	5	5.5	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD}	--	V_{DD}	V
Low-Level Input Voltage	V_{IL}	0	--	0.3V_{DD}	V
Driver Supply Voltage	V_{EE}	V_{DD}-35	--	0	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, Tamb=25 °C, V_{DD} =5V, GND=0V, V_{EE}=V_{DD}-35V)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Low -Level Output Voltage	V_{OLDOUT}	DOUT, I_{OLDOUT} =4mA	--	--	0.4	V
High-Level Output Current	I_{OHGR}	V_O=V_{DD}-2V, GR1 to GR4, SG9/GR8 to SG12/GR5	-15	--	--	mA
High-Level Output Current	I_{OHSG}	VO=V_{DD}-2V, SG1/KS1 to SG8/KS8	-3	--	--	mA
High-Level Input Voltage	V_{IH}	--	0.7V_{DD}	--	--	V
Low-Level Input Voltage	V_{IL}	--	--	--	0.3V_{DD}	V
Oscillation Frequency	f_{osc}	R=100KΩ	350	500	650	kHz
Input Current	I_I	VI=V_{DD} or V_{SS}	--	--	±1	μA
Dynamic Current Consumption	I_{DDdyn}	Under no load, display off	--	--	5	mA

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, Tamb=25 °C, V_{DD} =3.3V, GND=0V, V_{EE}=V_{DD}-35V)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Low -Level Output Voltage	V_{OLDOUT}	DOUT, I_{OLDOUT} =4mA	--	--	0.4	V
High-Level Output Current	I_{OHGR}	V_O=V_{DD}-2V, GR1 to GR4, SG9/GR8 to SG12/GR5	-6	--	--	mA
High-Level Output Current	I_{OHSG}	VO=V_{DD}-2V, SG1/KS1 to SG8/KS8	-1.5	--	--	mA

(To be continued)

(Continued)

Characteristic	Symbol	Test conditions	Min.	Typ.	Max.	Unit
High-Level Input Voltage	V_{IH}	--	0.7 V_{DD}	--	V_{DD}	V
Low-Level Input Voltage	V_{IL}	--	V_{SS}	--	0.3V_{DD}	V
Oscillation Frequency	f_{osc}	R=100KΩ	350	500	650	kHz
Input Current	I_I	VI=V_{DD} or V_{SS}	--	--	±1	μA
Dynamic Current Consumption	I_{DDdyn}	Under no load, display off	--	--	3	mA

PIN DESCRIPTION

Pin No.	Pin Name	Description
1	CLK	Clock input pin. This pin reads serial data at the rising edge and outputs data at the falling edge.
2	STB	Serial interface strobe pin. The data input after the STB has fallen is processed as a command. When this pin is"HIGH", CLK is ignored.
3, 4	K1 to K2	Key data input pins. At the end of the display cycle, the data sent to these pins are latched.
5, 25	V_{SS}	Logic ground pin
6, 24	V_{DD}	Logic power supply
7~14	SG1/KS1 to SG8/KS8	High voltage segment output pins also acts as the key source.
15	V_{EE}	Pull down level.
16~19	SG9/GR8 to SG12/GR5	High voltage segment/Grid output pins.
20~23	GR4 to GR1	High voltage Gird output pins
26	OSC	Oscillator input pin. Determining the oscillation frequency by a resistor which is connected to this pin and GND (VSS).
27	DOUT	Data output pin (N-channel, open drain) this pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).
28	DIN	Data input pin. This pin inputs serial data at the rising edge of the shift clock (starting from the lower bits).

FUNCTIONAL DESCRIPTION

Commands

Commands determine the display mode and status of SC16315S. A command is the first byte (b0 to b7) inputted to SC16315S via the DIN Pin after STB Pin has changed from "HIGH" to "LOW" State. For some reason, if STB Pin is set to "HIGH" while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

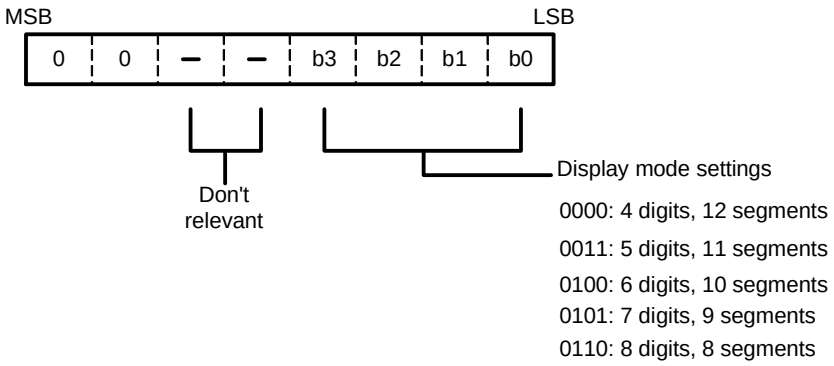
COMMAND1: Display mode setting commands

SC16315S provides 4 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to SC16315S via the DIN Pin when STB is "LOW". However, for these commands, the bits 5 to 6 (b4 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of "0".

The Display Mode Setting Commands determine the number of segments and grids to be used (1/4 to 1/8 duty, 12 to 8 segments). The display will be forcibly turned off and the key scanning will stop when these commands are executed. In order to resume display, a display command "ON" must be executed. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned "ON", the 8-digit, 8-segment mode is selected.

Figure 3: display mode settings

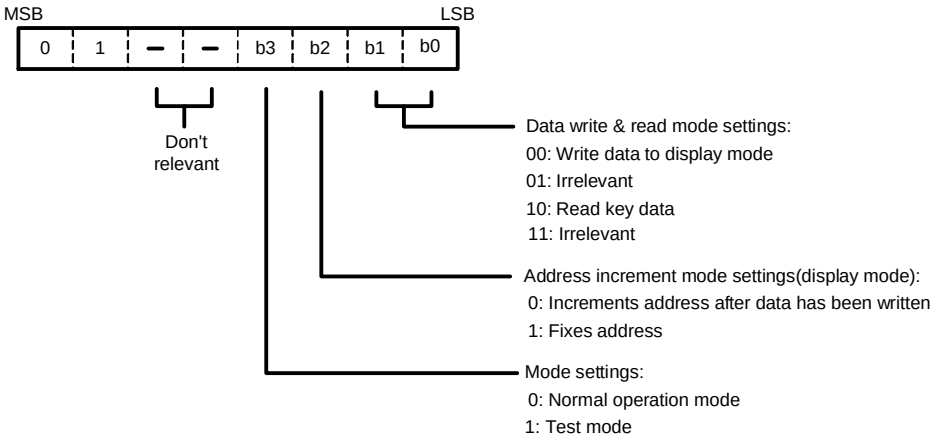


COMMAND 2: Data setting commands

The Data Setting Commands executes the Data Write or Data Read Modes for SC16315S. The Data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of "1" while bit 8 (b7) is given the value of "0". Please refer to the diagram below.

When power is turned ON, the bit 4 to bit 1 (b3 to b0) are given the value of "0".

Figure 4: data settings

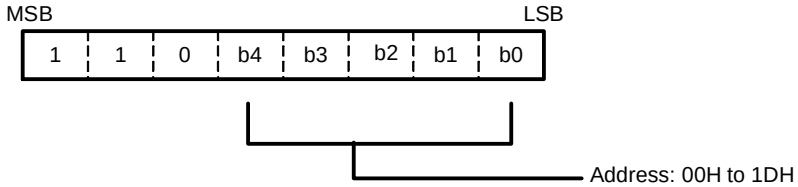


COMMAND 3: Address setting commands

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of "00H" to "1DH". The data is ignored until a valid address is set if the address is set to 1EH or higher. When power is turned ON, the address is set at "00H".

Please refer to the diagram below.

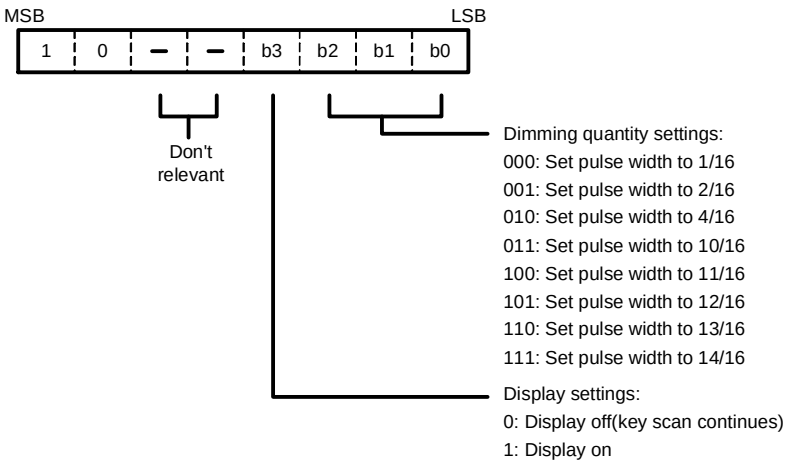
Figure 5: address settings



COMMAND 4: Display control commands

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is stopped).

Figure 6: display control settings



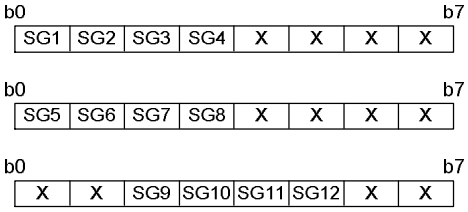
Display mode and RAM address

Data transmitted from an external device to SC16315S via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of SC16315S are given below in 8 bits unit.

Figure 7:SC16315S RAM address

SG1	SG4 SG5	SG8 SG9	SG12	
00H	01H	02H		DGT1
03H	04H	05H		DGT2
06H	07H	08H		DGT3
09H	0AH	0BH		DGT4
12H	13H	14H		DGT5
15H	16H	17H		DGT6
18H	19H	1AH		DGT7
1BH	1CH	1DH		DGT8

Figure 8: SC16315S written RAM data bytes

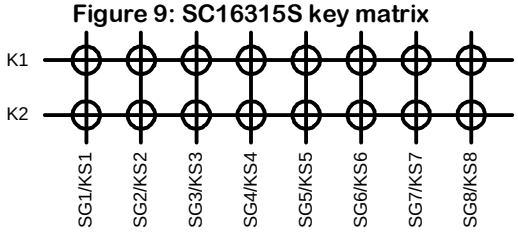


Note: X=don't care

Key matrix & Key-input data storage ram

The key matrix is made up of 8x 2 arrays as shown below:

Figure 9: SC16315S key matrix



Each data entered by each key is stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG1, b0) has been read, the least significant bit of the next data (SG8, b7) is read.

Figure 10: SC16315S key input data storage

K1…… K2	K1…… K2	K1……..K2	K1……..K2	
SG1/KS1	SG2/KS2	SG3/KS3	SG4/KS4	
*	*	*	*	
SG5/KS5	SG6/KS6	SG7/KS7	SG8/KS8	Reading sequence

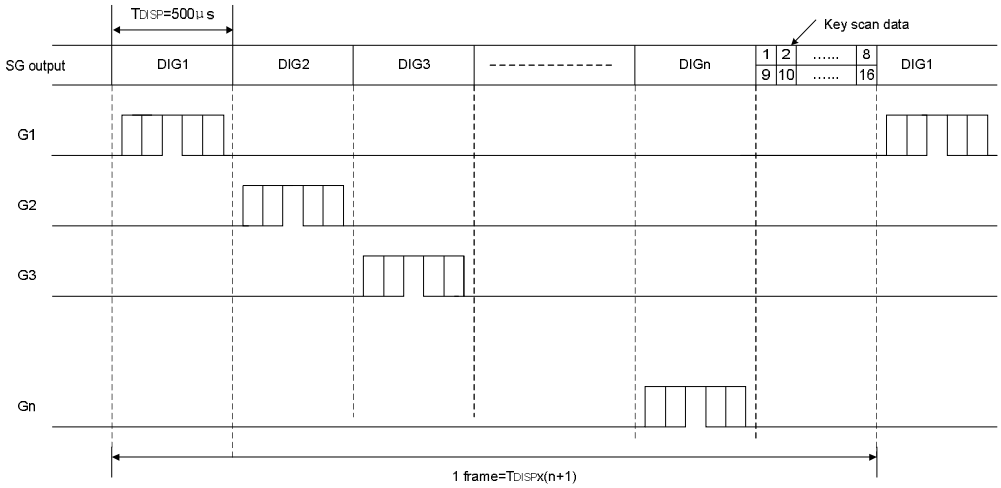
b0 ------- b1 b2 ------- b3 b4-------- b5 b6 -------- b7

Note: *=These sections are not relevant but are needed to read the transmission clock.

KEY SCANNING AND DISPLAY TIMING

The Key Scanning and display timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the 8 x 2 matrix is stored in the RAM.

Figure 11: SC16315S scanning & display timing diagram

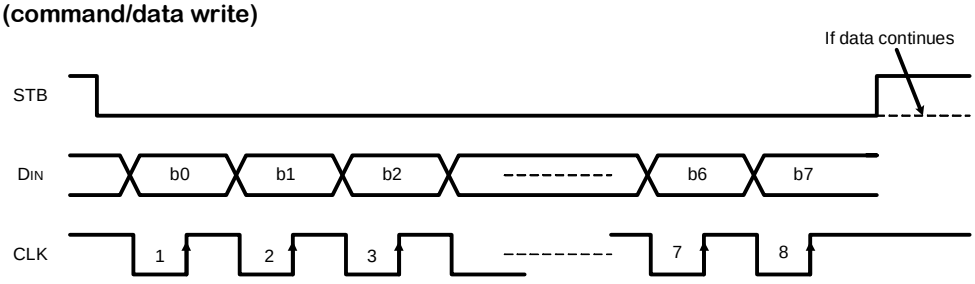


SERIAL COMMUNICATION FORMAT

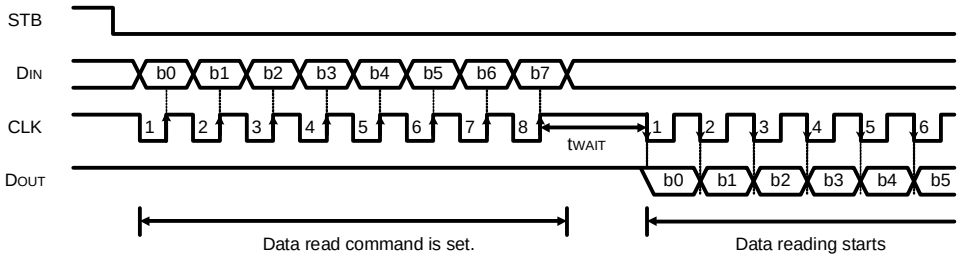
The following diagram shows the SC16315S serial communication format. The DOUT Pin is an N- channel, open-drain output pin; therefore, it is highly recommended that an external pull-up resistor (1 KΩ to 10 KΩ) must be connected to DOUT.

Figure 12: SC16315S serial communication format

Reception (command/data write)



Transmission (data read)



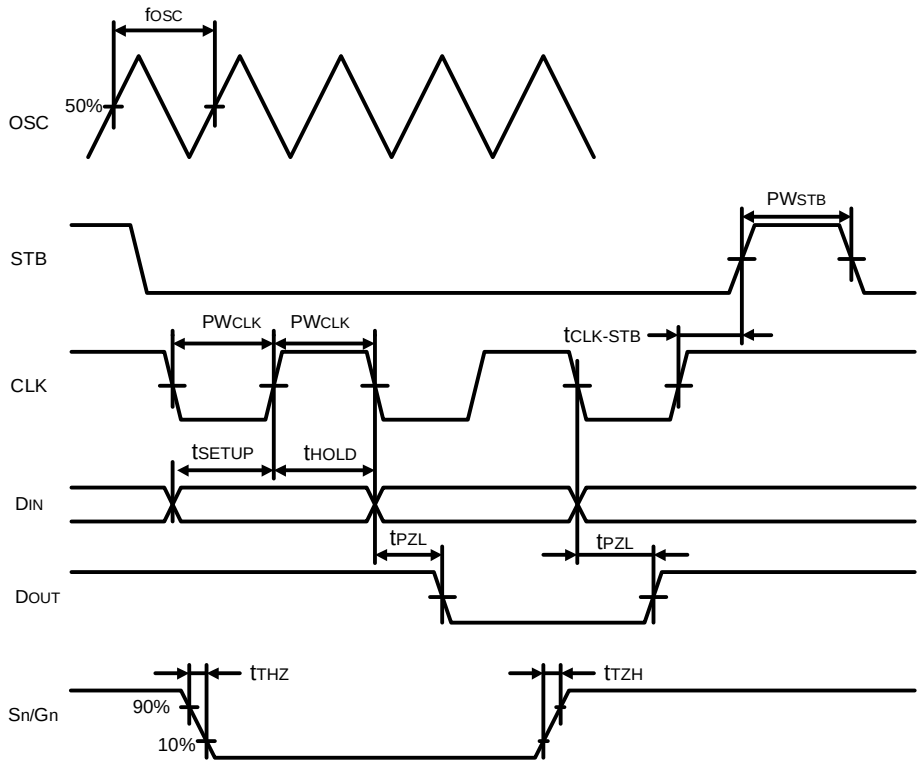
Where: twait (waiting time) ≥ 1μs.

It must be noted that when the data is read, the waiting time (t_{wait}) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μs.

SWITCHING CHARACTERISTIC WAVEFORM

SC16315S switching characteristics waveform is given below.

Figure 13: SC16315S switching characteristic waveform

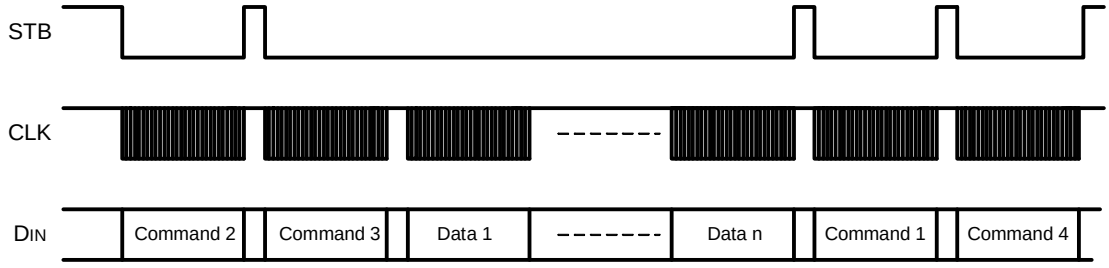


Where: PW CLK(clock pulse width)≥400ns
PW STB(strobe pulse width) ≥1μs
t_{setup}(data setup time) ≥100ns
t_{hold} (data hold time) ≥100ns
$t_{CLK-STB}$ (clock-strobe time) ≥1μs
t_{THZ} (fall time)≤150μs
t_{TZH2} (grid rise time) ≤0.5μs(at V_{DD}=5V)
t_{PZL} (propagation delay time)≤100ns
t_{TZH2} (grid rise time) ≤1.0μs(at V_{DD}=3.3V)
t_{PLZ} (propagation delay time) ≤400ns
t_{TZH1} (segment rise time) ≤2.0μs(at V_{DD}=5V)
f_{osc}=oscillation frequency
t_{TZH1} (segment rise time) ≤3.0μs(at V_{DD}=3.3V)

APPLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.

Figure 14: display memory updated by address increments



where : Command1: display mode setting command

Command2: data setting command

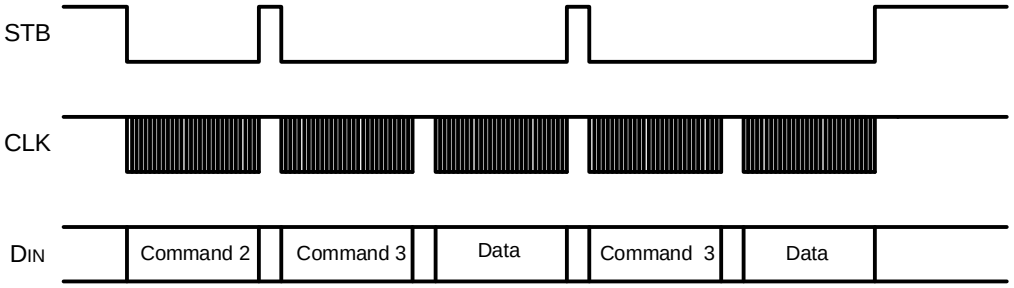
Command3: address setting command

Data 1 to n: transfers display data (24 bytes max.)

Command4: display control command

The following diagram shows the waveforms when updating specific addresses.

Figure 15: address update.



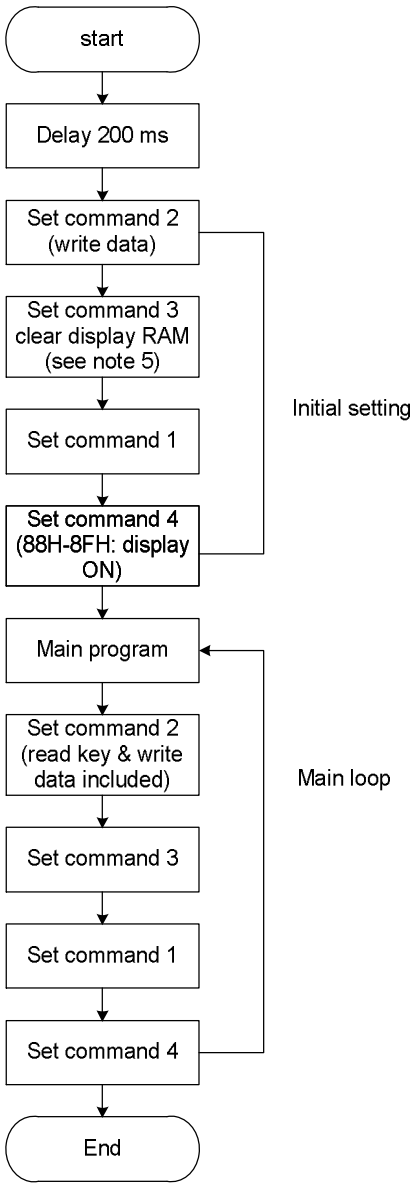
Where: Command 2— data setting command

Command 3— address setting command

Data— display data

RECOMMENDED SOFTWARE FLOWCHART

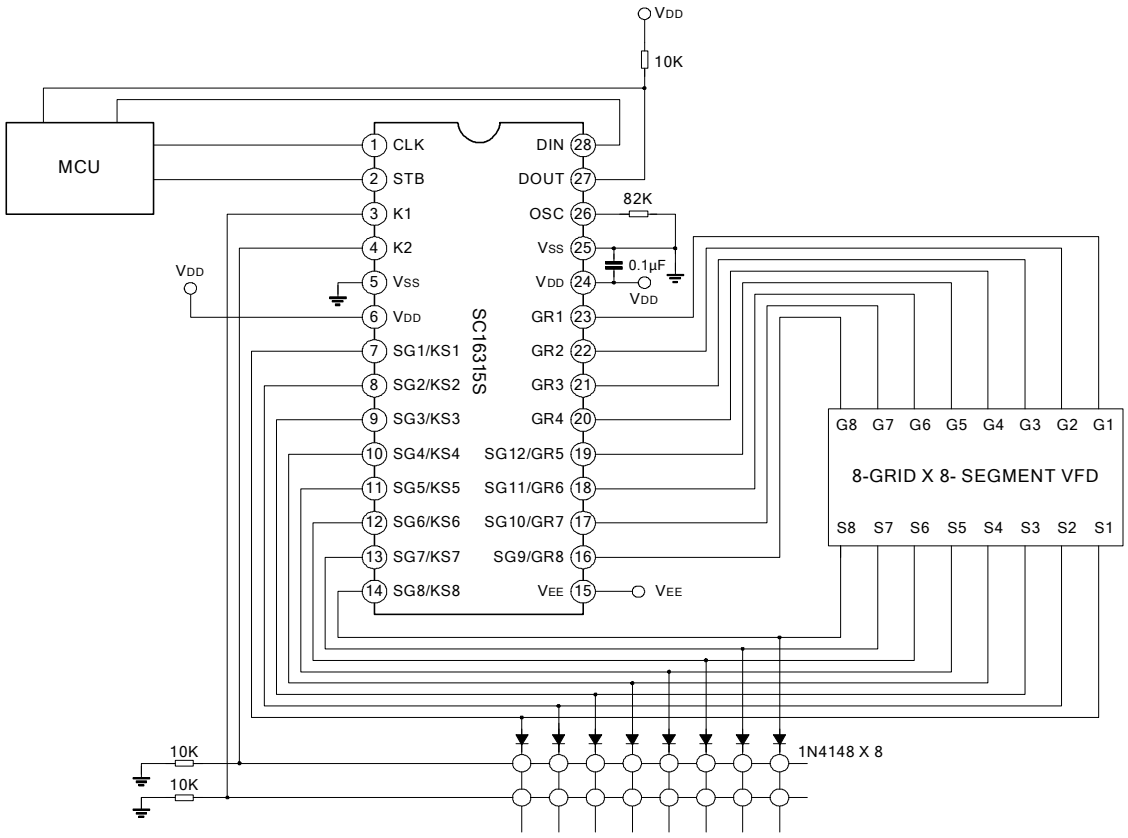
Figure 17: recommended software flowchart



Note: 1. Command 1: Display Mode Commands

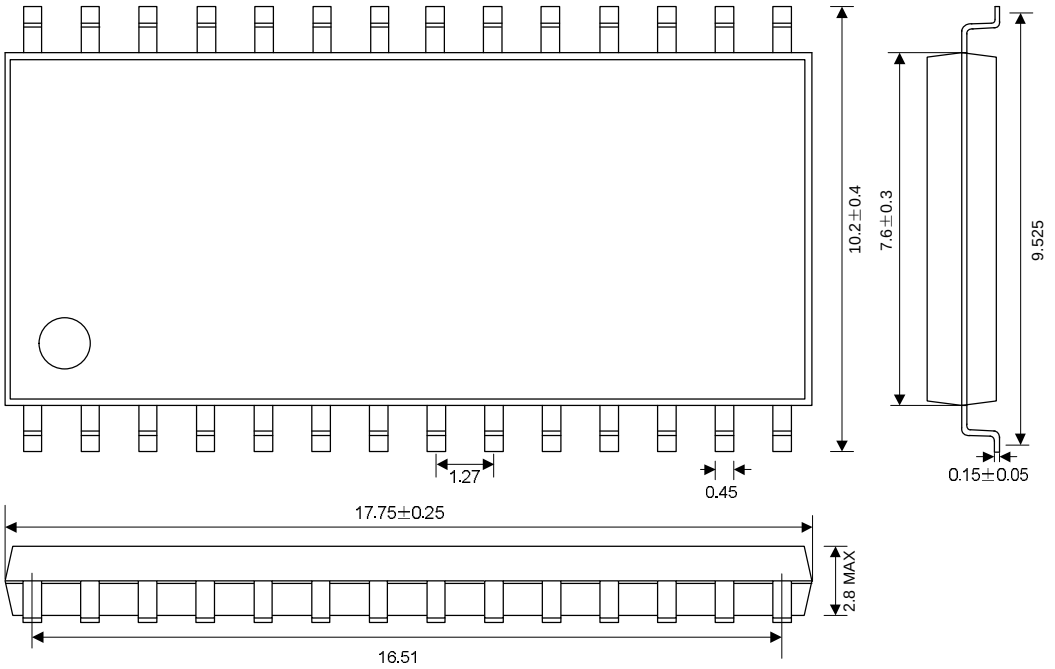
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

TYPICAL APPLICATION CIRCUIT



PACKAGE OUTLINE

SOP-28-375-1.27 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.