Low Voltage Synchronous Boost Converter

Features

- Input voltage — 0.7V to 3.8V
- Minimum start-up voltage — 0.85V
- Output voltage — fixed at 3.3V; adjustable from 1.8V to 4.0V
- Peak input current limit — 1.2A typically
- Output current at 3.3 V_{OUT} — 100mA with V_{IN} = 1.0V, 150mA with V_{IN} = 1.5V
- Efficiency up to 94%
- Internal synchronous rectifier
- Switching frequency — 1.2MHz
- Automatic power save
- Anti-ringing circuit
- Operating supply current (measured at OUT) — 50µA
- Shutdown current — 0.1µA (typ)
- No forward conduction path during shutdown
- Available in ultra-thin 1.5 x 2.0 x 0.6 (mm) MLPD-6 package
- Fully WEEE and RoHS compliant

Applications

- MP3 players
- Smart Phones and cellular phones
- Palmtop computers and handheld Instruments
- PCMCIA cards
- Memory cards
- Digital cordless phones
- Personal medical products
- Wireless VoIP phones
- Small motors

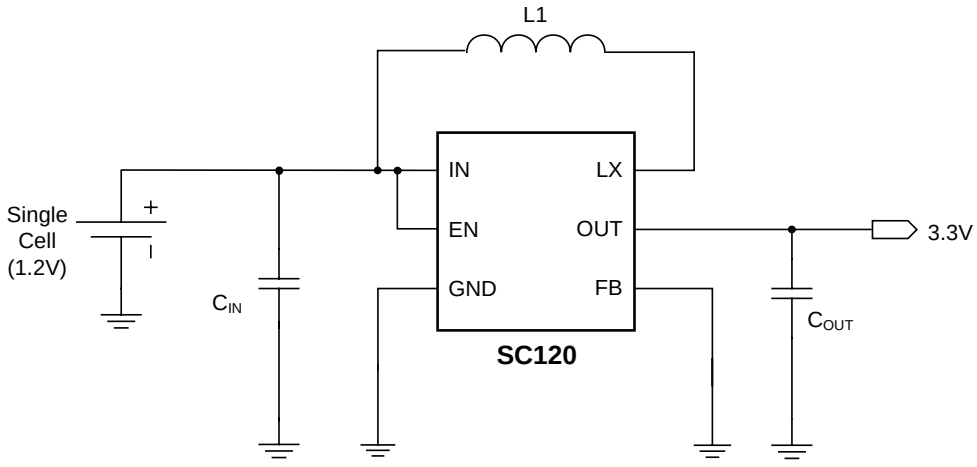
Description

The SC120 is a high efficiency, low noise, synchronous step-up DC-DC converter that provides boosted voltage levels in low-voltage handheld applications. The wide input voltage range allows use in systems with single NiMH or alkaline battery cells as well as in systems with higher voltage battery supplies. It features an internal 1.2A switch and synchronous rectifier to achieve up to 94% efficiency and to eliminate the need for an external Schottky diode. The output voltage can be set to 3.3V with internal feedback, or to any voltage within the specified range using a standard resistor divider.

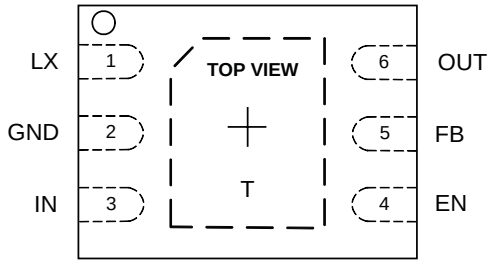
The SC120 operates in Pulse Width Modulation (PWM) mode for moderate to high loads and Power Save Mode (PSAVE) for improved efficiency under light load conditions. It features anti-ringing circuitry for reduced EMI in noise sensitive applications. Output disconnect capability is included to reduce leakage current, improve efficiency, and eliminate external components sometimes needed to disconnect the load from the supply during shutdown.

Low quiescent current is maintained with a high 1.2MHz operating frequency. Small external components and the space saving MLPD-6, 1.5x2.0x0.6mm package make this device an excellent choice for small handheld applications that require the longest possible battery life.

Typical Application Circuit



Pin Configuration



MLPD-UT; 1.5x2, 6 LEAD

θ_{JA} = 84°C/W

Ordering Information

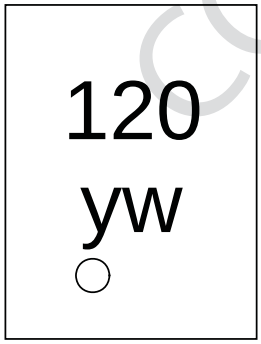
Device	Package
SC120ULTRT[1][2]	MLPD-UT-6 1.5×2
SC120EVB	Evaluation Board

Notes:

(1) Available in tape and reel only. A reel contains 3,000 devices.

(2) Lead-free package only. Device is WEEE and RoHS compliant.

Marking Information



y = year of manufacture

w = week of manufacture

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Absolute Maximum Ratings

IN, OUT, LX, FB (V) ..... -0.3 to +6.0
EN (V) ..... -0.3 to (V_{IN} + 0.3)
ESD Protection Level[1] (kV) 3

Recommended Operating Conditions

Ambient Temperature Range (°C)..... -40 to +85
V_{IN} (V) ..... 0.7 to 3.8
V_{OUT} (V)..... 1.8 to 4.0

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) 84
Maximum Junction Temperature (°C)..... 150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted V_{IN} = 2.5V, C_{IN} = C_{OUT} = 22µF, L_1 = 4.7µH, T_A = -40 to +85°C. Typical values are at T_A = 25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		0.7		3.8	V
Minimum Startup Voltage	V_{IN-SU}	I_{OUT} < 1mA, T_A = 0°C to 85°C			0.85	V
Shutdown Current	I_{SHDN}	T_A = 25°C, V_{EN} = 0V		0.1	1	µA
Operating Supply Current[1]	I_Q	In PSAVE mode, non-switching, measured at OUT		50		µA
Internal Oscillator Frequency	f_{OSC}			1.2		MHz
Maximum Duty Cycle	DC_{MAX}			90		%
Minimum Duty Cycle	DC_{MIN}				15	%
Output Voltage	V_{OUT}	V_{FB} = 0V		3.3		V
Adjustable Output Voltage Range	V_{OUT_RNG}	$V_{OUT} \geq V_{IN}$ + 0.3V	1.8		4.0	V
Internal Feedback Reference Accuracy	V_{INT_FB}	V_{FB} = 0V, (V_{OUT} set to 3.3V)	-3		3	%
FB Pin Regulation Voltage	V_{FB}		1.182	1.200	1.218	V
FB Pin Input Current	I_{FB}	V_{FB} = 1.2V			0.1	µA
Startup Time	t_{SU}			1		ms
P-Channel ON Resistance	R_{DSP}	V_{OUT} = 3.3V		0.6		Ω

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Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
N-Channel ON Resistance	R_{DSN}	V_{OUT} = 3.3V		0.5		Ω
N-Channel Current Limit	$I_{LIM(N)}$	V_{IN} = 3.0V	0.9	1.2		A
P-Channel Startup Current Limit	$I_{LIM(P)-SU}$	$V_{IN} > V_{OUT}$, $V_{EN} > V_{IH}$		150		mA
LX Leakage Current PMOS	I_{LXP}	T_A = 25°C, V_{LX} = 0V			1	µA
LX Leakage Current NMOS	I_{LXN}	T_A = 25°C, V_{LX} = 3.3V			1	µA
Logic Input High	V_{IH}	V_{IN} = 3.0V	0.85			V
Logic Input Low	V_{IL}	V_{IN} = 3.0V			0.2	V
Logic Input Current High	I_{IH}	$V_{EN} = V_{IN}$ = 3.0V			1	µA
Logic Input Current Low	I_{IL}	V_{EN} = 0V	-0.2			µA

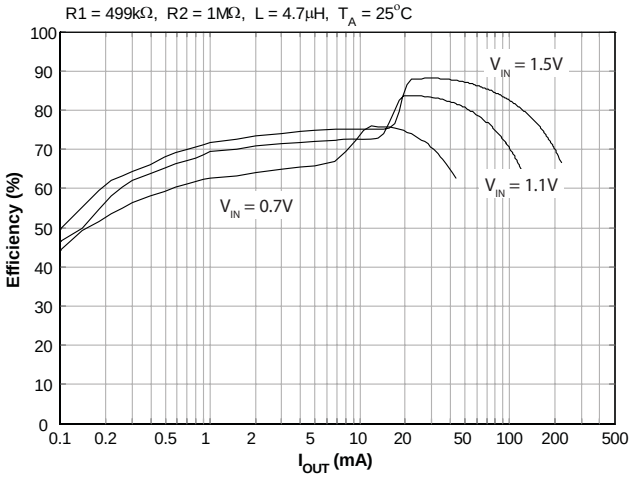
NOTES:

(1) Quiescent operating current is drawn from OUT while in regulation. The quiescent operating current projected to IN is approximately $I_Q \times (V_{OUT}/V_{IN})$.

Typical Characteristics

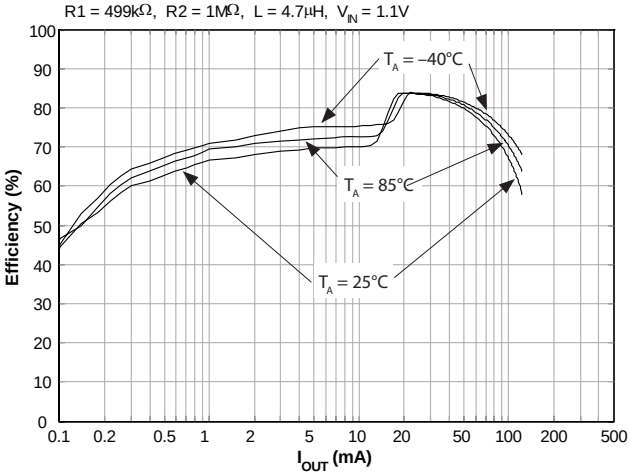
Efficiency vs. I_{OUT} (V_{OUT} = 1.8V)

R1 = 499kΩ, R2 = 1MΩ, L = 4.7µH, T_A = 25°C



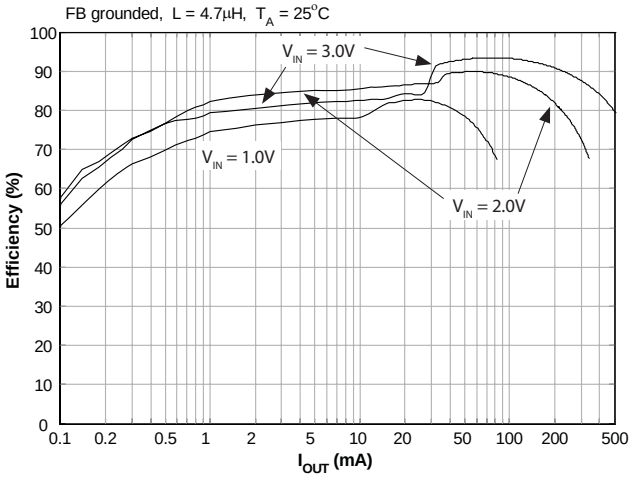
Efficiency vs. I_{OUT} (V_{OUT} = 1.8V)

R1 = 499kΩ, R2 = 1MΩ, L = 4.7µH, V_{IN} = 1.1V



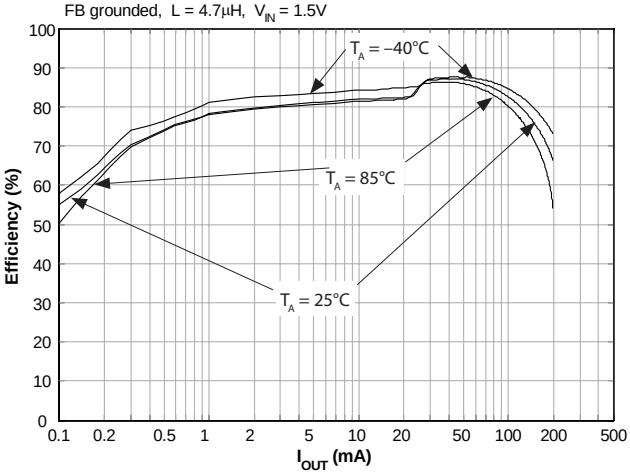
Efficiency vs. I_{OUT} (V_{OUT} = 3.3V)

FB grounded, L = 4.7µH, T_A = 25°C



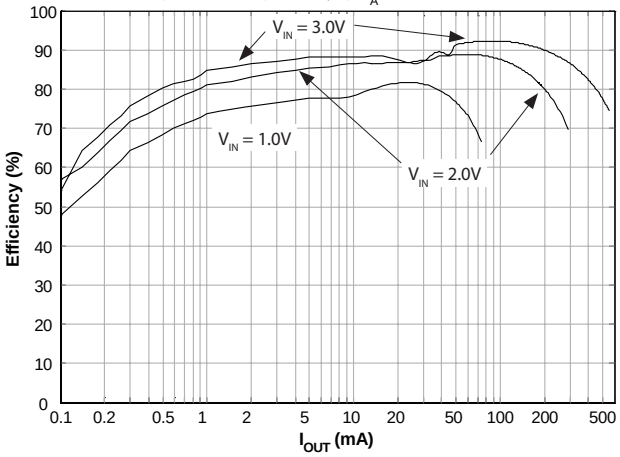
Efficiency vs. I_{OUT} (V_{OUT} = 3.3V)

FB grounded, L = 4.7µH, V_{IN} = 1.5V



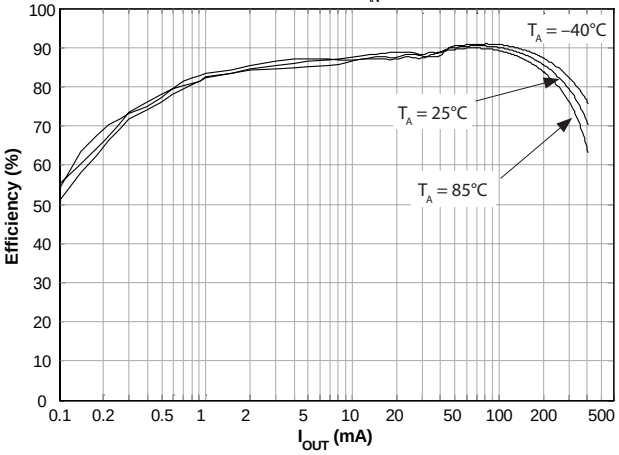
Efficiency vs. I_{OUT} (V_{OUT} = 4.0V)

R1 = 1.37MΩ, R2 = 590kΩ, L = 4.7µH, T_A = 25°C



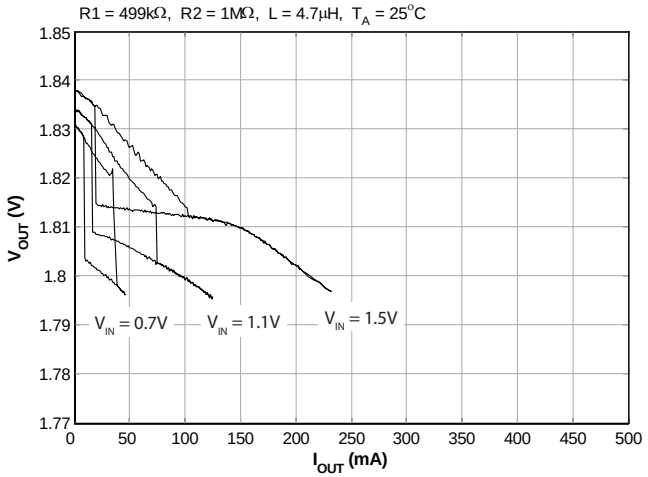
Efficiency vs. I_{OUT} (V_{OUT} = 4.0V)

R1 = 1.37MΩ, R2 = 590kΩ, L = 4.7µH, V_{IN} = 2.4V

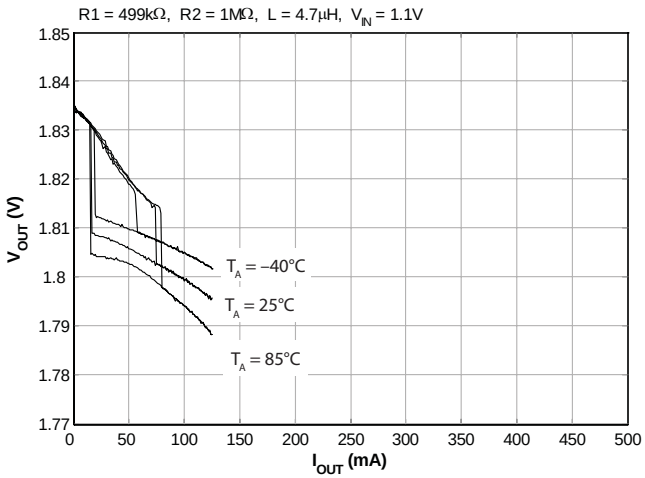


Typical Characteristics (continued)

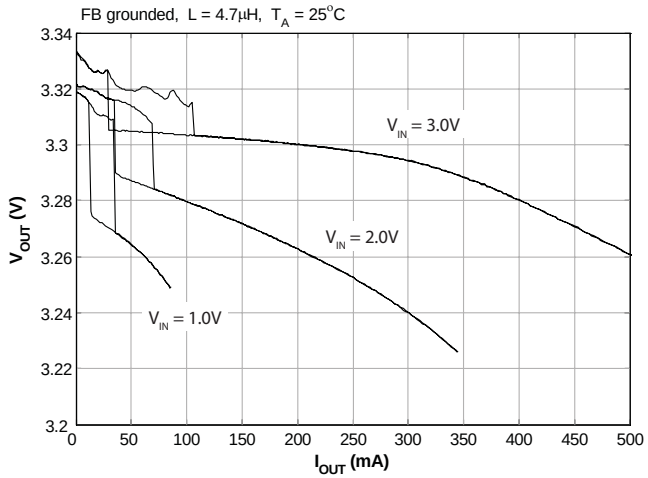
Load Regulation (V_{OUT} = 1.8V)



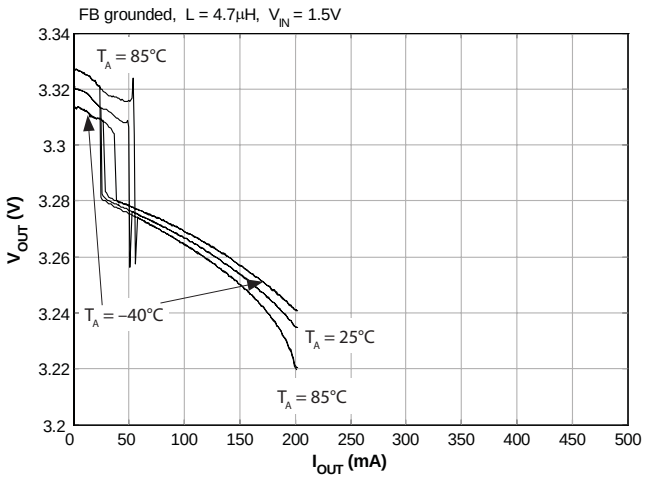
Load Regulation (V_{OUT} = 1.8V)



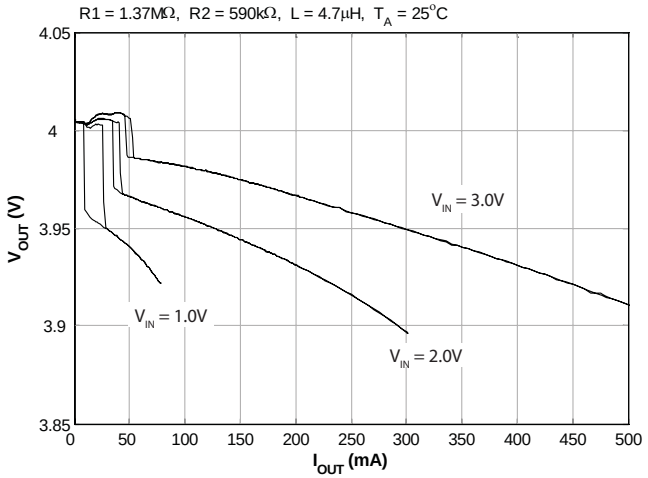
Load Regulation (V_{OUT} = 3.3V)



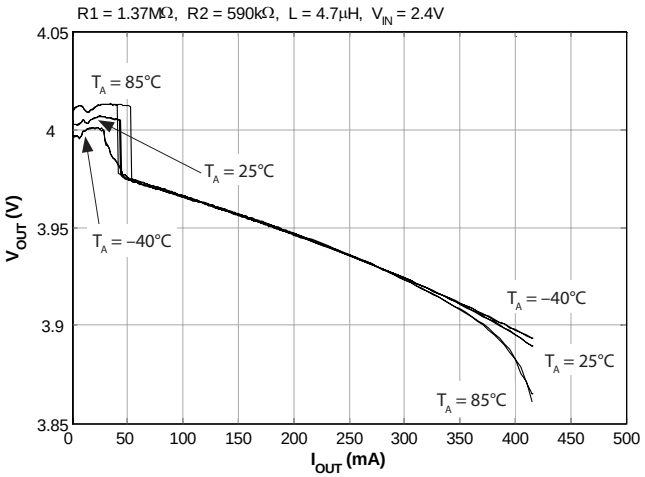
Load Regulation (V_{OUT} = 3.3V)



Load Regulation vs. (V_{OUT} = 4.0V)



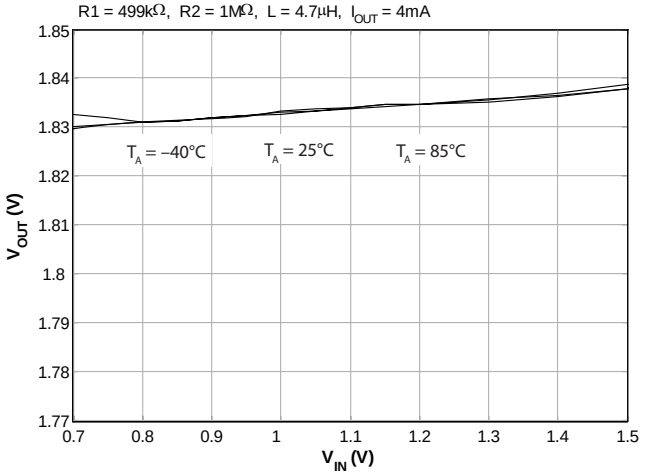
Load Regulation (V_{OUT} = 4.0V)



Typical Characteristics (continued)

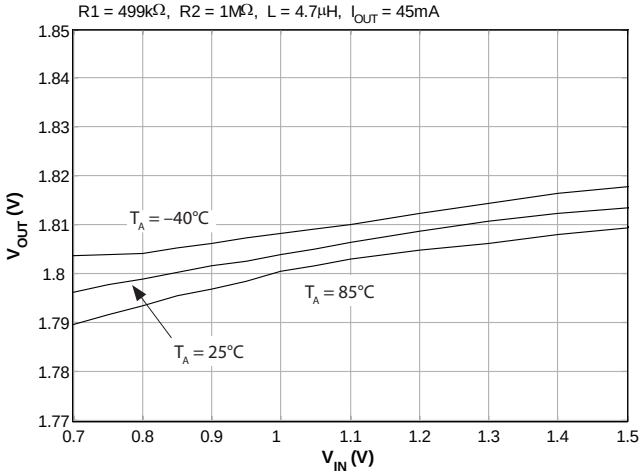
Line Regulation — PSAVE Mode (V_{OUT} = 1.8V)

R1 = 499kΩ, R2 = 1MΩ, L = 4.7µH, I_{OUT} = 4mA



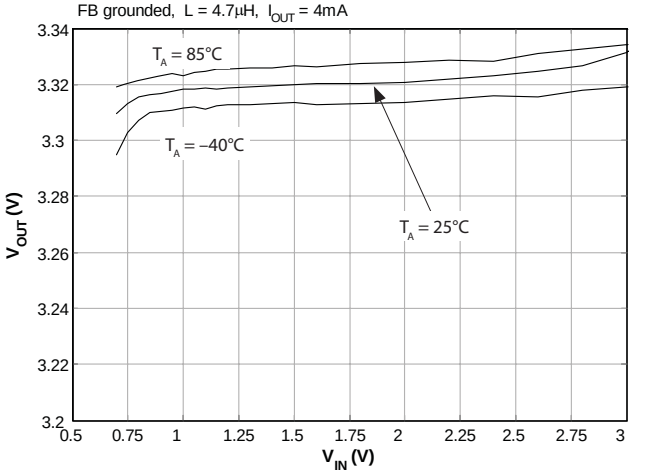
Line Regulation — PWM Mode (V_{OUT} = 1.8V)

R1 = 499kΩ, R2 = 1MΩ, L = 4.7µH, I_{OUT} = 45mA



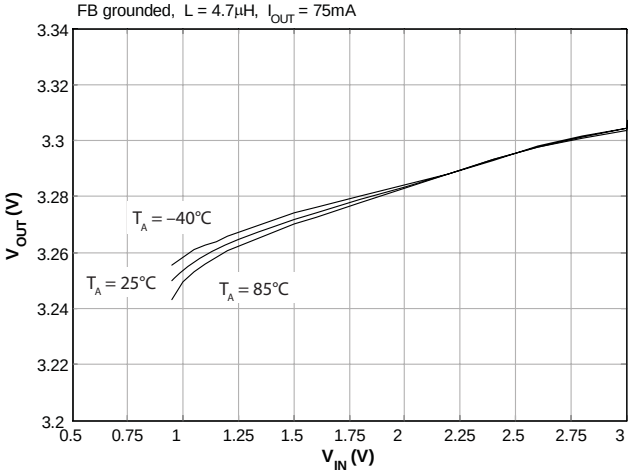
Line Regulation — PSAVE Mode (V_{OUT} = 3.3V)

FB grounded, L = 4.7µH, I_{OUT} = 4mA



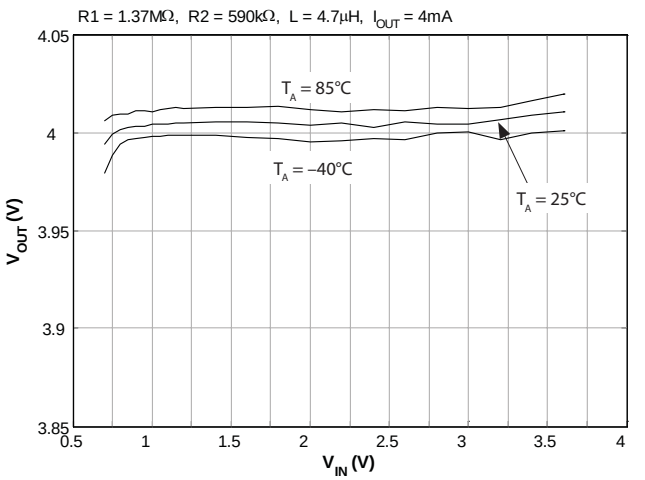
Line Regulation — PWM Mode (V_{OUT} = 3.3V)

FB grounded, L = 4.7µH, I_{OUT} = 75mA



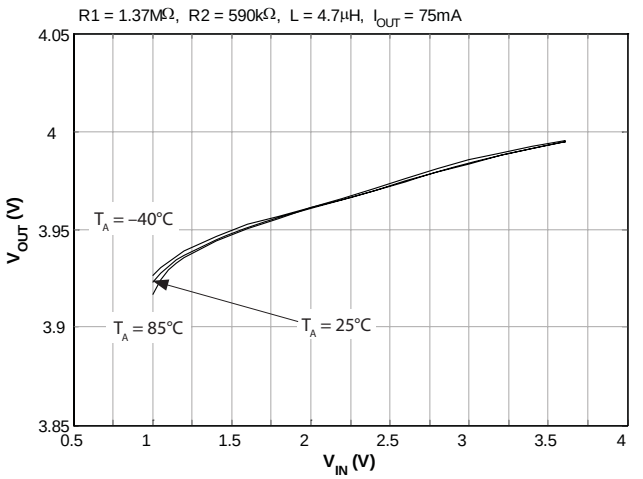
Line Regulation — PSAVE Mode (V_{OUT} = 4.0V)

R1 = 1.37MΩ, R2 = 590kΩ, L = 4.7µH, I_{OUT} = 4mA



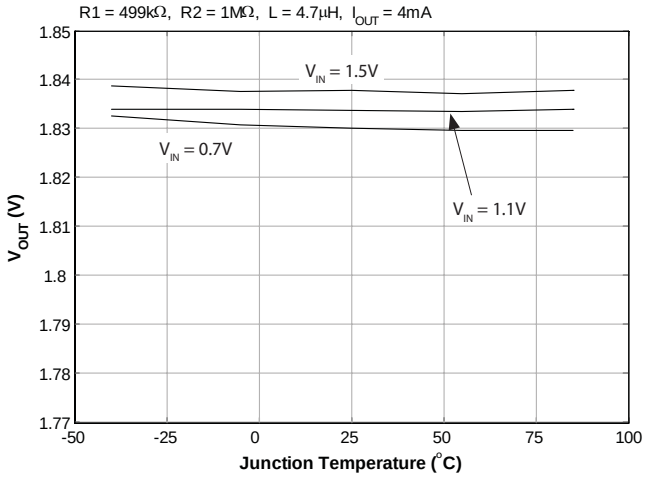
Line Regulation — PWM Mode (V_{OUT} = 4.0V)

R1 = 1.37MΩ, R2 = 590kΩ, L = 4.7µH, I_{OUT} = 75mA

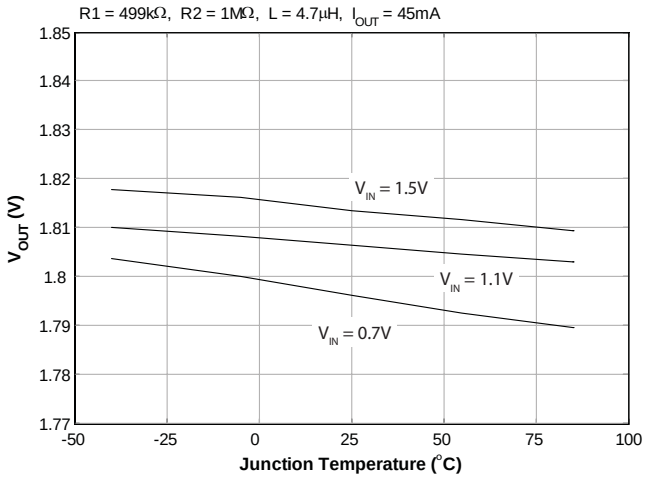


Typical Characteristics (continued)

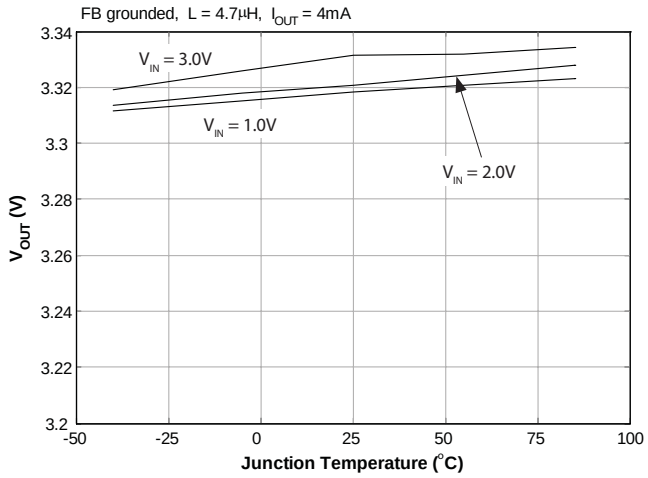
Temperature Reg. — PSAVE Mode (V_{OUT} = 1.8V)



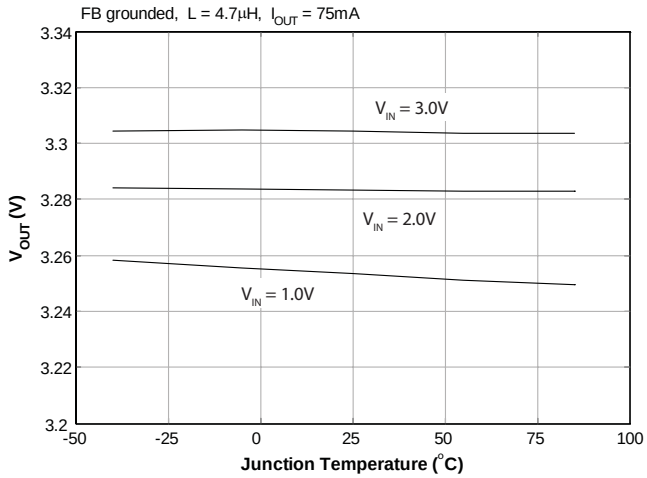
Temperature Reg. — PWM Mode (V_{OUT} = 1.8V)



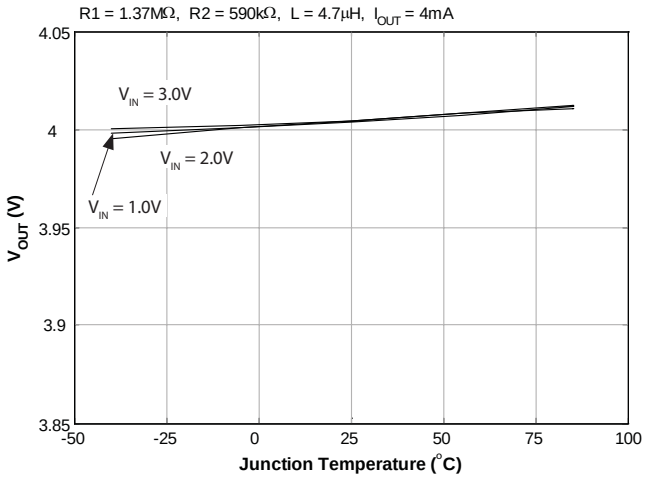
Temperature Reg. — PSAVE Mode (V_{OUT} = 3.3V)



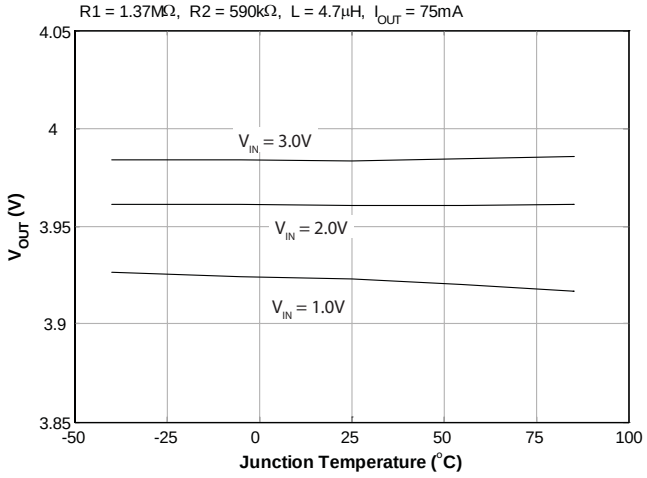
Temperature Reg. — PWM Mode (V_{OUT} = 3.3V)



Temperature Reg. — PSAVE Mode (V_{OUT} = 4.0V)

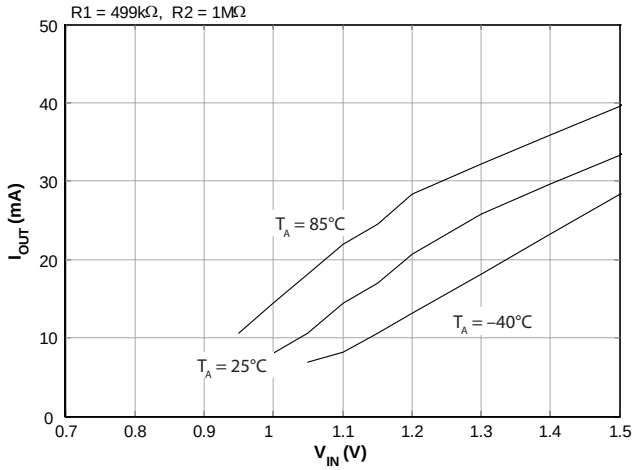


Temperature Reg. — PWM Mode (V_{OUT} = 4.0V)

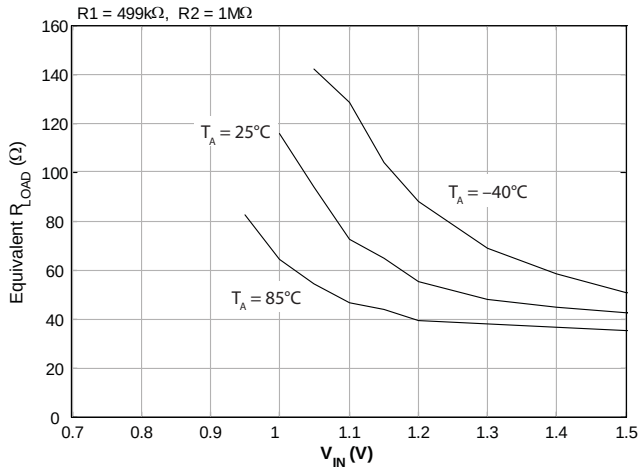


Typical Characteristics (continued)

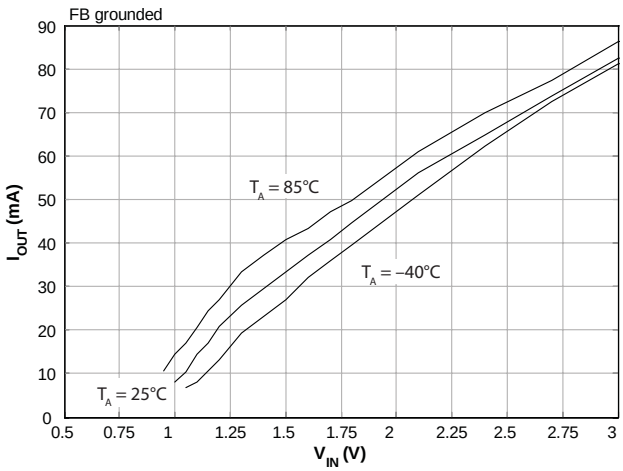
Startup Max. Load Current vs. V_{IN} (V_{OUT} = 1.8V)



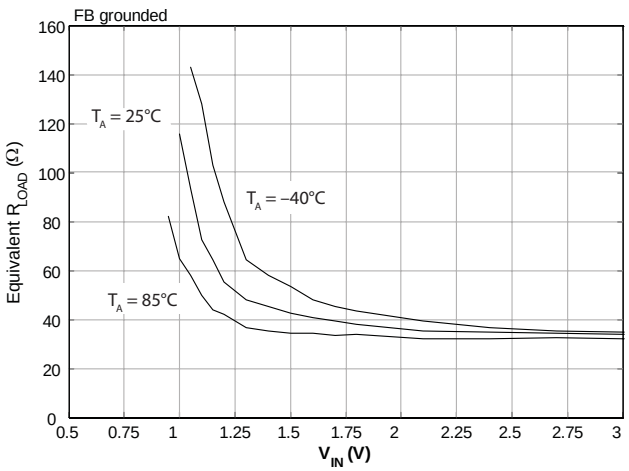
Startup Min. Load Resistance vs. V_{IN} (V_{OUT} = 1.8V)



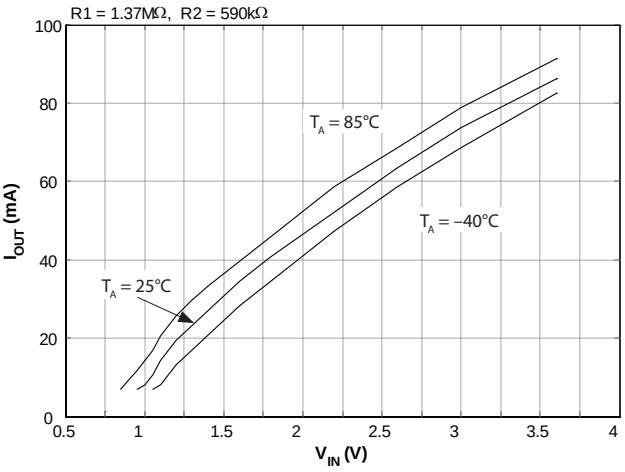
Startup Max. Load Current vs. V_{IN} (V_{OUT} = 3.3V)



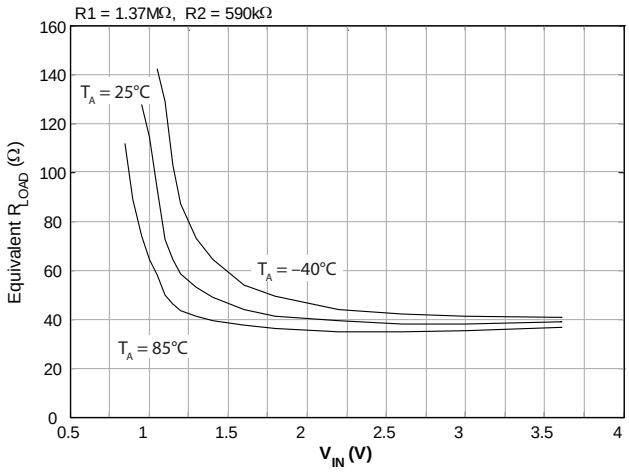
Startup Min. Load Resistance vs. V_{IN} (V_{OUT} = 3.3V)



Startup Max. Load Current vs. V_{IN} (V_{OUT} = 4.0V)



Startup Min. Load Resistance vs. V_{IN} (V_{OUT} = 4.0V)



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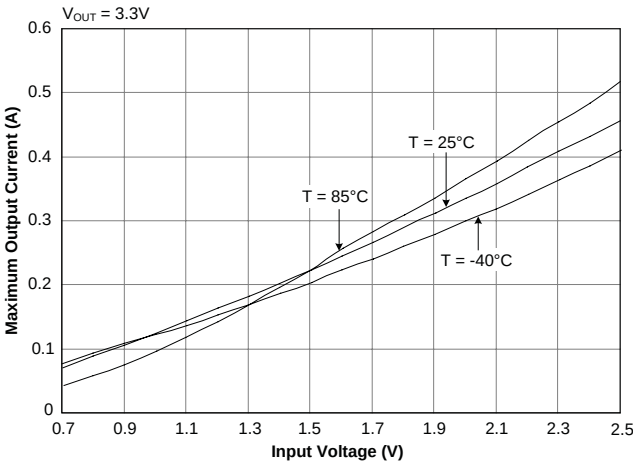
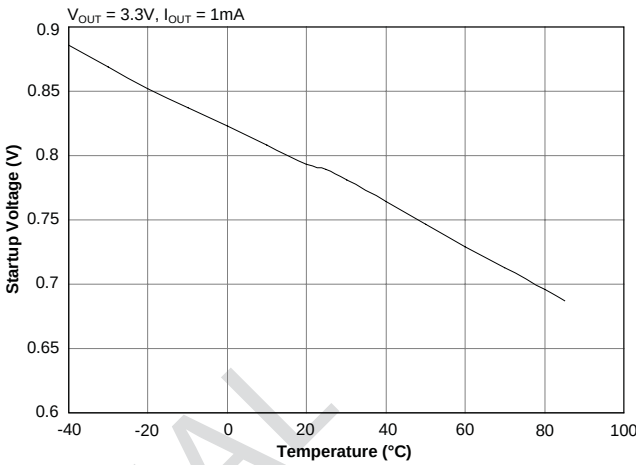
Typical Characteristics (continued)

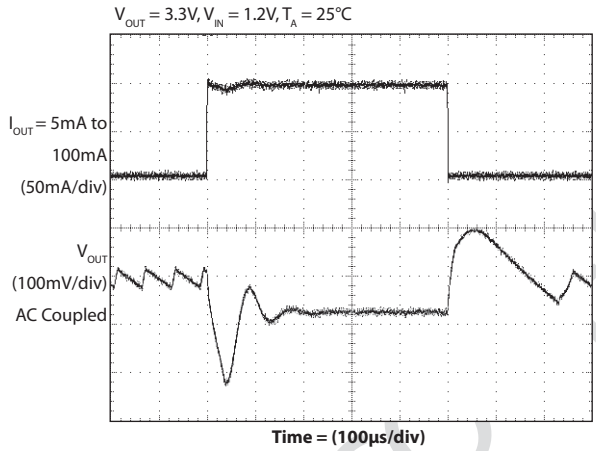
I_{OUT} (max) vs. V_{IN}



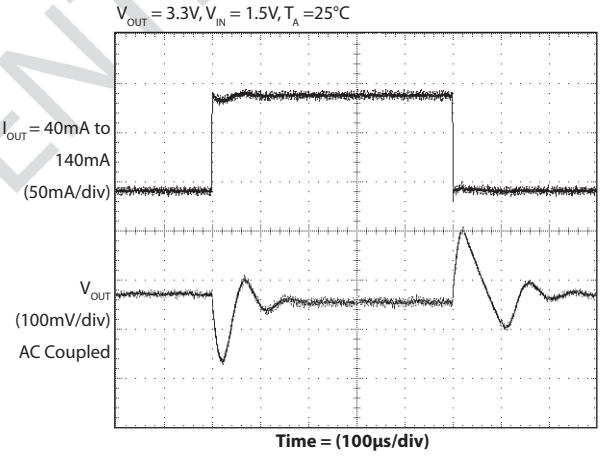
Minimum Start-up Voltage vs. Temperature



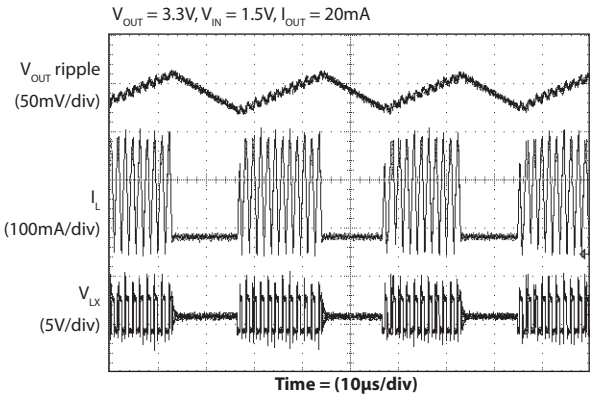
Load Transient (PSAVE to PWM)



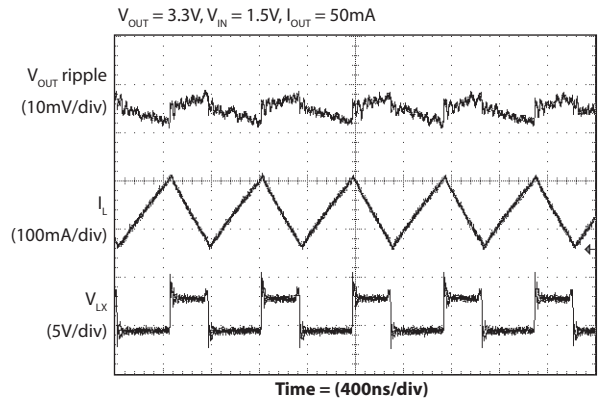
Load Transient (PWM to PWM)



PSAVE Operation



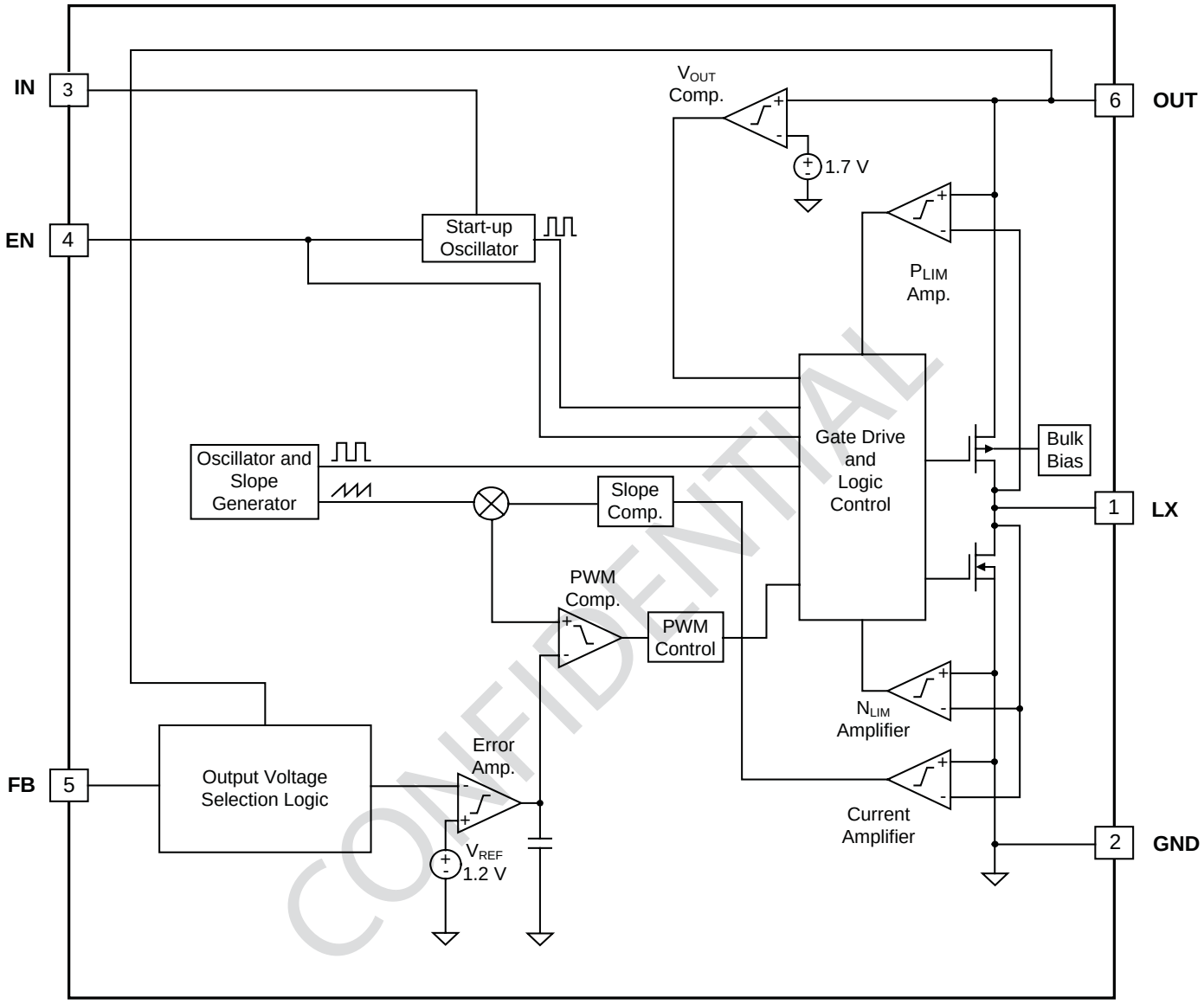
PWM Operation



Pin Descriptions

Pin #	Pin Name	Pin Function
1	LX	Switching node — connect an inductor from the input supply to this pin.
2	GND	Signal and power ground.
3	IN	Battery input and damping switch connection.
4	EN	Enable digital control input — active high.
5	FB	Feedback input — connect to GND for preset 3.3V output. A voltage divider is connected from OUT to GND to adjust output from 1.8V to 4.0V.
6	OUT	Output voltage supply pin — requires an external 10µF bypass capacitor (while under V_{OUT} bias) for normal operation.
T	Thermal Pad	Thermal Pad is for heat sinking purposes — connect to ground using multiple vias — not connected internally.

Block Diagram



SEMTECH

Applications Information

Detailed Description

The SC120 is a synchronous step-up Pulse Width Modulated (PWM) DC-DC converter utilizing a 1.2MHz fixed frequency current mode architecture. It is designed to provide output voltages in the range 1.8V to 4.0V from an input voltage as low as 0.7V, with a (output unloaded) start up input voltage of 0.85V.

The device operates in two modes: PWM and automatic PSAVE mode. In PWM operation, the devices uses pulse width modulation control to regulate the output under moderate to heavy load conditions. It switches to PSAVE mode when lightly loaded. Quiescent current consumption is as little as 50µA, into the OUT pin, when in PSAVE mode.

The regulator control circuitry is shown in the Block Diagram. It is comprised of a programmable feedback controller, an internal 1.2MHz oscillator, an n-channel Field Effect Transistor (FET) between the LX and GND pins, and a p-channel FET between the LX and OUT pins. The current flowing through both FETs is monitored and limited as required for startup, PWM operation, and PSAVE operation. An external inductor must be connected between the IN pin and the LX pin. When the n-channel FET is turned on, the LX pin is internally grounded, connecting the inductor between IN and GND. This is called the on-state. During the on-state, inductor current flows to ground and is increasing. When the n-channel FET is turned off and the p-channel FET is turned on (known as the off-state), the inductor is then connected between IN and OUT. The (now decreasing) inductor current flows from the input to the output, boosting the output voltage above the input voltage.

Output Voltage Selection

The SC120 output voltage can be programmed to an internally preset value or it can be programmed with external resistors. The output is internally programmed to 3.3V when the FB pin is connected to GND. Any output voltage in the range 1.8V to 4.0V can be programmed with a resistor voltage divider between OUT and the FB pin as shown in Figure 1.

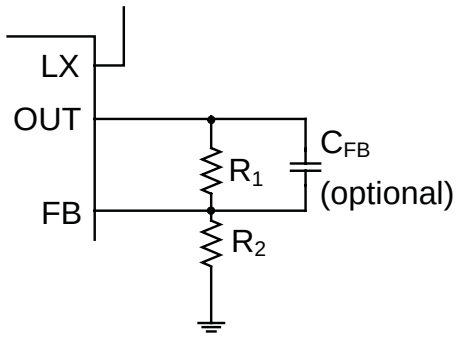


Figure 1 — Output Voltage Feedback Circuit

The values of the resistors in the voltage divider network are chosen to satisfy the equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right)$$

The value of R_2 should be 590kΩ or larger for stability. Otherwise, the values of R_1 and R_2 can be as large as desired to achieve low quiescent current.

PWM Operation

The PWM cycle runs at a fixed frequency (f_{osc} = 1.2MHz), with a variable duty cycle (D). PWM operation continually draws current from the input supply (except for discontinuous mode, described below). During the on-state, of the PWM cycle, the n-channel FET is turned on, grounding the inductor at the LX pin. This causes the current flowing from the input supply through the inductor to ground to ramp up. During the off-state, the n-channel FET is turned off and the p-channel FET (synchronous rectifier) is turned on. This causes the inductor current to flow from the input supply through the inductor into the output capacitor and load, boosting the output voltage above the input voltage. The cycle then repeats to re-energize the inductor.

Ideally, the steady state (constant load) duty cycle is determined by $D = 1 - (V_{IN}/V_{OUT})$, but must be greater in practice to overcome dissipative losses. The SC120 PWM controller constrains the value of D such that $0.15 < D < 0.9$, (approximately).

The average inductor current during the off-state multiplied by (1-D) is equal to the average load current. The inductor current is alternately ramping up (on-state) and down (off-state) at a rate and amplitude determined by

Applications Information (continued)

the inductance value, the input voltage, and the on-time (D×T). Therefore, the instantaneous inductor current will be alternately larger and smaller than the average. If the average output current is sufficiently small, the minimum inductor current can reach zero during the off-state. If the energy stored in the inductor is depleted (if the inductor current decreases to zero) during the off-state, both FETs turn off for the remainder of the off-state. If this discontinuous mode (DM) operation persists, the SC120 transitions to PSAVE operation.

PSAVE Operation

At light loads, the SC120 will operate in PSAVE mode. PSAVE mode ensures proper regulation when V_{IN} is too close to V_{OUT} while the output load is too small to keep the duty cycle above its minimum value. At very low output load, PSAVE mode will operate more efficiently than PWM mode. PSAVE operation is triggered by 256 consecutive cycles of DM operation in PWM mode, when the output of the P_{LIM} amplifier falls to 0V during the off-state due to low load current.

PSAVE mode requires fewer circuit resources than PWM mode. All unused circuitry is disabled to reduce quiescent power dissipation. In PSAVE mode, the OUT pin voltage monitoring circuit remains active and the output voltage error amplifier operates as a comparator. PSAVE regulation is shown in Figure 2. When $V_{OUT} < 1.008xV_{REG}$, where V_{REG} is the programmed output voltage, a burst of fixed-period switching occurs to boost the output voltage. The n-channel FET turns on (on-state) until the inductor current rises to approximately 240mA. Then the n-channel FET turns off and the p-channel FET turns on to transfer the inductor energy to the output capacitor and load for the duration of the off-state. This cycle repeats until $V_{OUT} > 1.018×V_{REG}$, at which point bot FETs are turned off. The output capacitor then discharges into the load until $V_{OUT} < 1.008×V_{REG}$, and the burst cycle repeats.

When the output current increases above a predetermined level, either of two PSAVE exit conditions will force the resumption of PWM operation. The first PSAVE exit criterion is shown in Figure 2. If the PSAVE burst cycle cannot provide sufficient current to the output, the output voltage will decrease during the burst. If

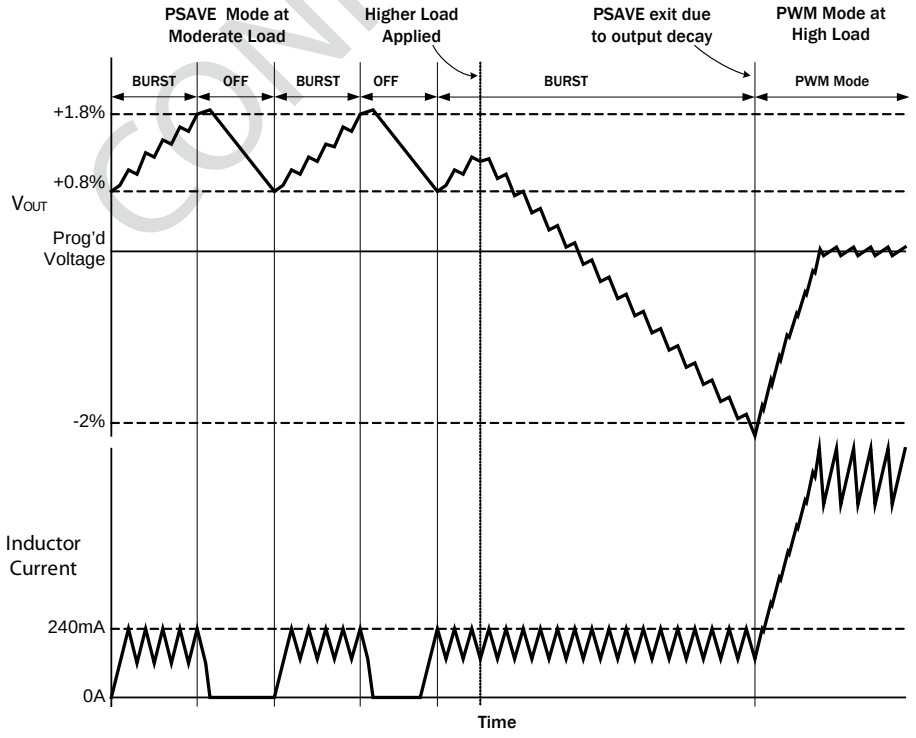


Figure 2 — PSAVE Operation With Exit to PWM Due To Output Voltage Decay

Applications Information (continued)

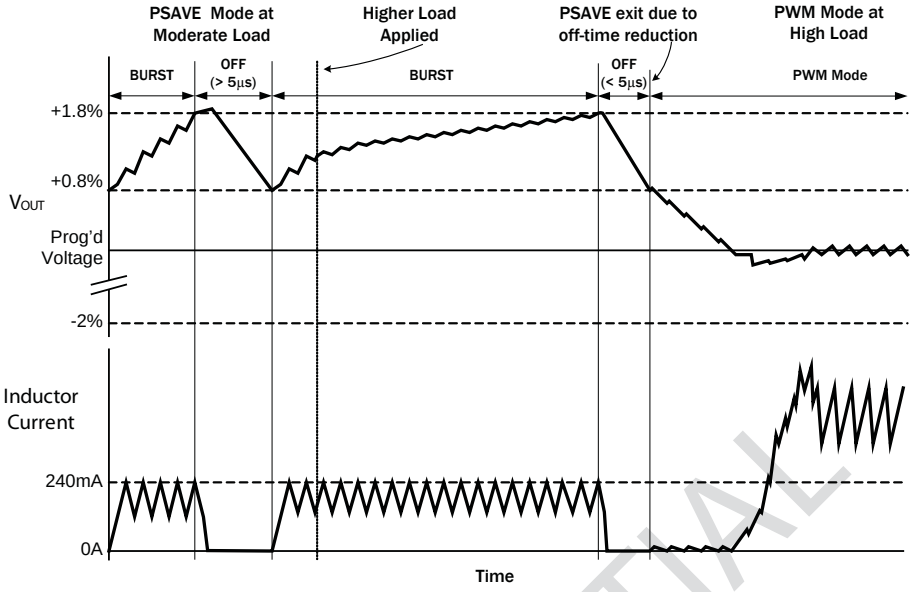


Figure 3 — PSAVE Operation With Exit to PWM Due To Off-time < 5µs

$V_{OUT} < 0.98 \times V_{REG}$, PWM operation will resume. The second PSAVE exit criterion, illustrated in Figure 3, depends on the rate of discharge of the output capacitor between PSAVE bursts. If the time between bursts is less than 5µs, then PWM operation resumes. The output capacitance value will affect the second criterion, but not the first. Reducing the output capacitor will reduce the output load at which PSAVE mode exits to PWM mode.

Within each on/off cycle of a PSAVE burst, the rate of decrease of the inductor current during the off-state is proportional to $(V_{OUT} - V_{IN})$. If V_{IN} is sufficiently close to V_{OUT}, the decrease in current during the off-state may not overcome the increase in current during the minimum on-time of the on-state, approximately 100ns. This can result in the peak inductor current rising above the PSAVE mode n-channel FET current limit. (Normally, when the n-channel FET current limit is reached, the on-state ends immediately and the off-state begins. This sets the duty cycle on a cycle-by-cycle basis.) This inductor current rise accumulates with each successive cycle in the burst. The result is that the output load current that can be supported in PSAVE under this high V_{IN} condition will be greater than occurs if the 240mA current limit can be enforced. Therefore the PSAVE exit load due to the first exit criterion (Figure 2) can increase significantly. This phenomenon is advantageous. Reverting to PWM operation with high V_{IN} can result in V_{OUT} rising above V_{REG}, due to the PWM minimum duty cycle. PSAVE operation avoids this voltage rise because of its voltage-threshold on/off control. If the load remains low enough to remain in PSAVE, V_{IN} can approach and even slightly exceed V_{OUT}. To initally enter PSAVE mode, the initial startup load must be small enough to cause discontinuous mode PWM operation. This PSAVE mode startup load upper limit can be increased if needed by reducing the inductance (refer to the section Inductor Selection). Sufficiently large output capacitance will prevent PSAVE exit due to the second exit criterion (Figure 3).

PSAVE V_{OUT} ripple may increase due to parasitic capacitance on the external FB pin network. If using external feedback programming, it is prudent to add a small capacitor between OUT and FB to the circuit board layout. When operating the SC120 in the final configuration in PSAVE, observe the amplitude of PSAVE ripple. If the ripple exceeds 50mV for the expected range of input voltage, a small-value capacitor should be tried. Capacitance on the order of a few picofarads is often sufficient to bring the ripple amplitude to approximately 50mV.

Applications Information (continued)

The Enable Pin

The EN pin is a high impedance logical input that can be used to enable or disable the SC120 under processor control. V_{EN} < 0.2V will disable regulation, set the LX pin in a high-impedance state (turn off both FET switches), and turn on an active discharge device to discharge the output capacitor via the OUT pin. V_{EN} > 0.85V will enable the output. The startup sequence from the EN pin is identical to the startup sequence from the application of input power.

Regulator Startup, Short Circuit Protection, and Current Limits

The SC120 permits power up at input voltages from 0.85V to 3.8V. Startup current limiting of the internal switching n-channel and p-channel FET power devices protects them from damage in the event of a short between OUT and GND. As the output voltage rises, progressively less-restrictive current limits are applied. This protection unavoidably prevents startup into an excessive load.

To begin, the p-channel FET between the LX and OUT pins turns on with its current limited to approximately 150mA, the short-circuit output current. When V_{OUT} approaches V_{IN} (but is still below 1.7V), the n-channel current limit is set to 350mA (the p-channel limit is disabled), the internal oscillator turns on (approximately 200kHz), and a fixed 75% duty cycle PWM operation begins. (See the section PWM Operation.) When the output voltage exceeds 1.7V, normal fixed frequency variable duty cycle PWM operation begins, with the n-channel FET's current limited to 350mA to prevent excessive output voltage overshoot. If the n-channel FET current limit is exceeded, the on-state ends immediately and the off-state begins, overriding the output voltage regulation controller. This reduces the duty cycle on a cycle-by-cycle basis. When V_{OUT} is within 2% of the programmed regulation voltage, the n-channel FET current limit is raised to 1.2A.

Once variable duty cycle PWM operation is initiated, the output becomes independent of V_{IN} and output regulation can be maintained for V_{IN} as low as 0.7V, subject to the maximum duty cycle and peak current limits. The duty cycle must remain between 15% and 90% for the device to operate within specification.

Note that startup with a regulated active load is not the same as startup with a resistive load. The resistive load output current increases proportionately as the output voltage rises until it reaches programmed V_{OUT}/R_{LOAD}, while a regulated active load presents a constant load as the output voltage rises from 0V to programmed V_{OUT}. Note also that if the load applied to the output exceeds an applicable V_{OUT}–dependent startup current limit or duty cycle limit, the criterion to advance to the next startup stage may not be achieved. In this situation startup may pause at a reduced output voltage until the load is reduced further.

Output Overload and Recovery

When in PSAVE operation, an increasing load will eventually satisfy one of the PSAVE exit criteria and regulation will revert to PWM operation. As previously noted, the PWM steady state duty cycle is determined by $D = 1 - (V_{IN}/V_{OUT})$, but must be somewhat greater in practice to overcome dissipative losses. As the output load increases, the dissipative losses also increase. The PWM controller must increase the duty cycle to compensate. Eventually, one of two overload conditions will occur, determined by V_{IN}, V_{OUT}, and the overall dissipative losses due to the output load current. Either the maximum duty cycle of 90% will be reached or the n-channel FET 1.2A (nominal) peak current limit will be reached, which effectively limits the duty cycle to a lower value. Above that load, the output voltage will decrease rapidly and in reverse order the startup current limits will be invoked as the output voltage falls through its various voltage thresholds. How far the output voltage drops depends on the load V-I characteristics.

A reduction in input voltage, such as due to a discharging battery, will lower the load current at which overload occurs. Lower input voltage increases the duty cycle required to produce a given output voltage. And lower input voltage also increases the input current to maintain the input power, which increases dissipative losses and further increases the required duty cycle. Therefore an increase in load current or a decrease in input voltage can result in output overload.

Once an overload has occurred, the load must be decreased to permit recovery. The conditions required for

Applications Information (continued)

overload recovery are identical to those required for successful initial startup.

Anti-ringing Circuitry

In PWM operation, the n-channel and p-channel FETs are simultaneously turned off when the inductor current reaches zero. They remain off for the zero-inductor-current portion of the off-state. Note that discontinuous mode is a marginal-load condition, which if persistent will trigger a transition to PSAVE operation.

When both FET switches are simultaneously turned off, an internal switch between the IN and LX pins is closed, providing a moderate resistance path across the inductor to dampen the oscillations at the LX pin. This effectively reduces EMI that can develop from the resonant circuit formed by the inductor and the drain capacitance at LX.

The anti-ringing circuitry is disabled between PSAVE bursts.

Component Selection

The SC120 provides optimum performance when a 4.7µH inductor is used with a 10µF output capacitor. Different component values can be used to modify PSAVE exit or entry loads, modify output voltage ripple in PWM mode, improve transient response, or to reduce component size or cost.

Inductor Selection

The inductance value primarily affects the amplitude of inductor current ripple (ΔI_L). Reducing inductance increases ΔI_L. This raises the inductor peak current, $I_{L\text{-}max} = I_{L\text{-}avg} + \Delta I_L/2$, where $I_{L\text{-}avg}$ is the inductor current averaged over a full on/off cycle. $I_{L\text{-}max}$ is subject to the n-channel FET current limit $I_{LIM(N)}$, therefore reducing the inductance may lower the output overload current threshold. Increasing ΔI_L also lowers the inductor minimum current, $I_{L\text{-}min} = I_{L\text{-}avg} - \Delta I_L/2$, thus raising the PSAVE entry load current threshold. This is the output load below which $I_{L\text{-}min} = 0$, the boundary between continuous mode and discontinuous mode PWM regulation, which signals the SC120 controller to switch to PSAVE operation. In the extreme case of V_{IN} approaching V_{OUT}, smaller inductance can also *reduce* the PSAVE inductor burst-envelope current ripple and voltage ripple.

The governing equations for inductor selection are the following. Equating input power to output power, noting that input current equals inductor current, and averaging over a full PWM switching cycle,

$$I_{L-avg} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}}$$

where η is efficiency.

ΔI_L is the inductor (and thus the input) peak-to-peak current. Neglecting the n-channel FET $R_{DS\text{-}ON}$ and the inductor DCR, for duty cycle D, and with $T = 1/f_{osc}$,

$$\Delta I_{L-on} = \frac{1}{L}\int_0^{DT} V_{IN}\, dt = \frac{V_{IN} \times D \times T}{L}$$

This is the change in I_L during the on-state. During the off-state, again neglecting the p-channel FET $R_{DS\text{-}ON}$ and the inductor DCR,

$$\Delta I_{L-off} = \frac{1}{L}\int_{DT}^{T} (V_{IN} - V_{OUT})\, dt = \frac{(V_{IN} - V_{OUT}) \times T}{L}(1-D)$$

Note that this is a negative quantity, since $V_{OUT} > V_{IN}$ and $0 < D < 1$. For a constant load in steady-state, the inductor current must satisfy $\Delta I_{L\text{-}on} + \Delta I_{L\text{-}off} = 0$. Substituting the two expressions and solving for D, obtain $D = 1 - V_{IN}/V_{OUT}$. Using this expression, and the positive valued expression $\Delta I_L = \Delta I_{L\text{-}on}$ for current ripple amplitude, obtain expanded expression for $I_{L\text{-}max}$ and $I_{L\text{-}min}$.

$$I_{L-max,min} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \pm \frac{T}{2 \times L} \times \frac{V_{IN}}{V_{OUT}} \times (V_{OUT} - V_{IN})$$

If the value of I_{OUT} decreases until $I_{L\text{-}min} = 0$, which is the boundary of continuous and discontinuous PWM operation, the SC120 will transition from PWM operation to PSAVE operation. Define this value of I_{OUT} as $I_{PSAVE\text{-}entry}$. Setting the expression for $I_{L\text{-}min}$ to 0 and solving,

$$I_{PSAVE-entry} = \frac{\eta \times T}{2 \times L}\left(\frac{V_{IN}}{V_{OUT}}\right)^2 (V_{OUT} - V_{IN})$$

Applications Information (continued)

The programmed value of V_{OUT} is constant. $I_{PSAVE\text{-}entry}$ is a polynomial function of V_{IN}. Equating $dI_{PSAVE\text{-}entry}/dV_{IN} = 0$ and solving for V_{IN} reveals that there is one non-zero extremum of this function, a maximum, at $V_{IN} = {}^{2}/_{3}\, V_{OUT}$. Applying this value of V_{IN},

$$I_{PSAVE-entry-max} = \frac{\eta \times T}{L} \times \frac{2}{27} \times V_{OUT}$$

The value of the inductor determines the PSAVE entry output load current. Evaluate $I_{PSAVE\text{-}entry}$ at the smallest and largest expected values of V_{IN}. If the input range includes $V_{IN} = {}^{2}/_{3}\, V_{OUT}$, also determine $I_{PSAVE\text{-}entry\text{-}max}$. If the largest V_{IN} exceeds approximately 90% of V_{OUT}, then instead evaluate PSAVE entry at $V_{IN} = 0.9V_{OUT}$. Since PSAVE exit will require an unusually high output load current at high V_{IN}. This was explained in a previous section, therefore PSAVE entry under this condition may not be relevant.

The inductor selection should also consider the n-channel FET current limit for the expected range of input voltage and output load current. The largest $I_{L\text{-}avg}$ will occur at the expected smallest V_{IN} and largest I_{OUT}. Determine the largest allowable ΔI_L, based on the largest expected $I_{L\text{-}avg}$, the minimum n-channel FET current limit, and the inductor tolerance. Ensure that in the worst case, $I_{L\text{-}avg} + \Delta I_L/2 < I_{LIM(N)}$.

These calculations include the parameter η, efficiency. Efficiency varies with V_{IN}, I_{OUT}, and temperature. Estimate η using the plots provided in this datasheet, or from experimental data, at the operating condition of interest when computing the effect of a new inductor value on PSAVE entry and I-limit margin.

Any chosen inductor should have low DCR, compared to the $R_{DS\text{-}ON}$ of the FET switches, to maintain efficiency, though for DCR << $R_{DS\text{-}ON}$, further reduction in DCR will provide diminishing benefit. The inductor I_{SAT} value should exceed the expected $I_{L\text{-}max}$. The inductor self-resonant frequency should exceed $5 \times f_{osc}$. Any inductor with these properties should provide satisfactory performance.

Table 1 lists the manufacturers of recommended inductor options.

Table 1 — Recommended Inductors

Manufacturer/ Part #	Value (µH)	DCR (Ω)	Rated Current (mA)	Tolerance (%)	Dimensions LxWxH (mm)
Murata LQH43MN4R7K03L	4.7	0.4	500	10	4.5 x 3.2 x 2.6

Capacitor Selection

Input and output capacitors must be chosen carefully to ensure that they are of the correct value and rating. The output capacitor requires a minimum capacitance value of 10µF at the programmed output voltage to ensure stability over the full operating range. This must be considered when choosing small package size capacitors as the DC bias must be included in their derating to ensure this required value. For example, a 10µF 0805 capacitor may provide sufficient capacitance at low output voltages but may be too low at higher output voltages. Therefore, a higher capacitance value may be required to provide the minimum of 10µF at these higher output voltages. Additional output capacitance may be required for V_{IN} close to V_{OUT} to reduce ripple in PSAVE mode and to ensure stability in PWM mode, especially at higher output load currents.

Low ESR capacitors such as X5R or X7R type ceramic capacitors are recommended for input bypassing and output filtering. Low-ESR tantalum capacitors are not recommended due to possible reduction in capacitance seen at the switching frequency of the SC120. Ceramic capacitors of type Y5V are not recommended as their temperature coefficients make them unsuitable for this application. Table 2 lists the manufacturer of the recommended capacitor.

Table 2 — Recommended Capacitor

Manufacturer/ Part Number	Value (µF)	Rated Voltage (VDC)	Type	Case Size
Murata GRM21BR60J226ME39B	22	6.3	X5R	0805

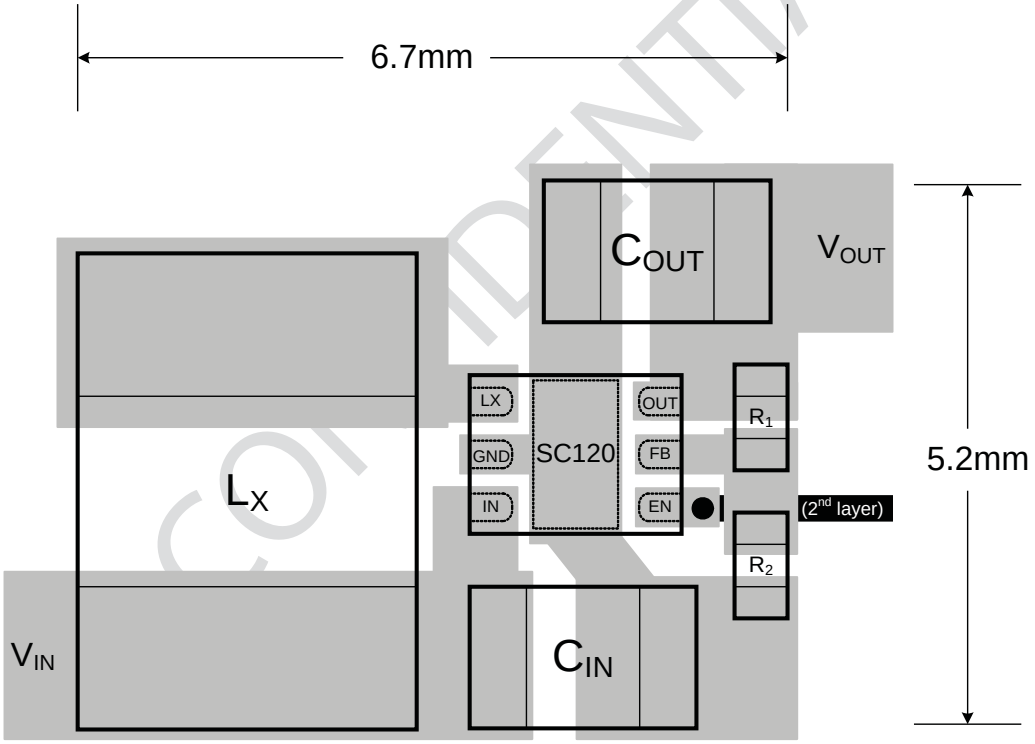
Applications Information (continued)

PCB Layout Considerations

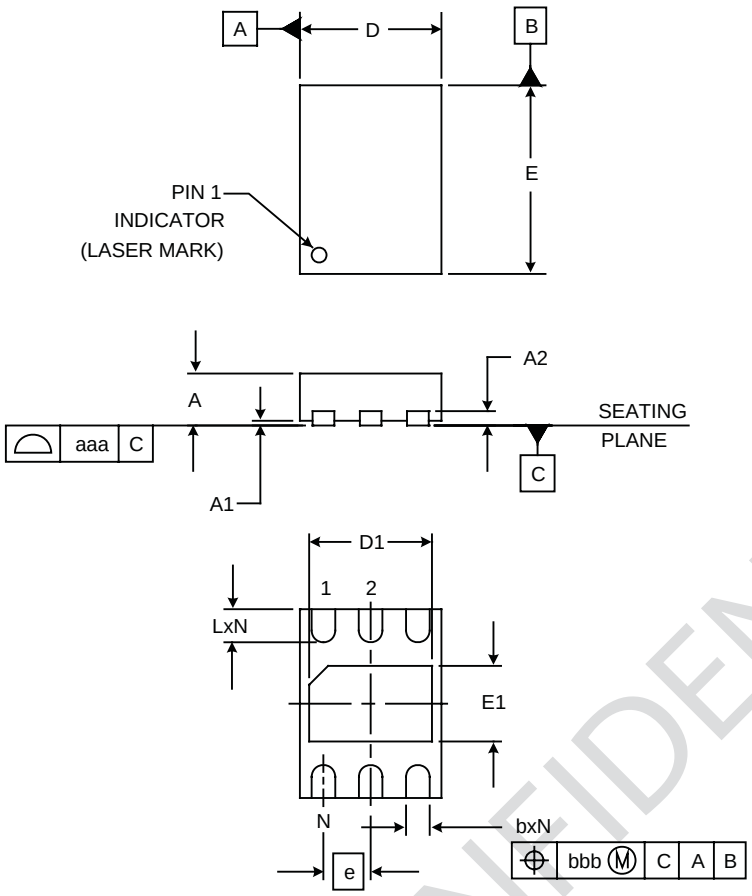
Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

A few simple design rules can be implemented to ensure good layout:

- Place the inductor and filter capacitors as close to the device as possible and use short wide traces between the power components.
- Route the output voltage feedback path away from the inductor and LX node to minimize noise and magnetic interference.
- Maximize ground metal on the component side to improve the return connection and thermal dissipation. Separation between the LX node and GND should be maintained to avoid coupling capacitance between the LX node and the ground plane.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.



Outline Drawing — MLPD-UT-6 1.5x2

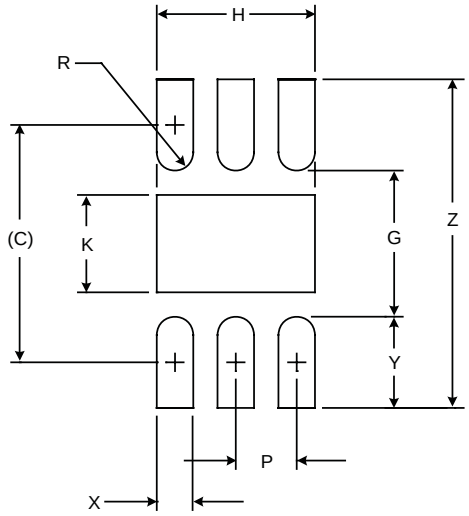


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(.152)	
b	.007	.010	.012	0.18	0.25	0.30
D	.055	.059	.063	1.40	1.50	1.60
D1	.035	-	.055	0.90	-	1.40
E	.075	.079	.083	1.90	2.00	2.10
E1	.026	.031	.035	0.65	0.80	0.90
e		.020 BSC			0.50 BSC	
L	.012	.014	.016	0.30	0.35	0.40
N		6			6	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Land Pattern — MLPD-UT-6 1.5x2



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.077)	(1.95)
G	.047	1.20
H	.051	1.30
K	.031	0.80
P	.020	0.50
R	.006	0.15
X	.012	0.30
Y	.030	0.75
Z	.106	2.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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