

**AOT5N60**  
**600V, 5A N-Channel MOSFET**
*formerly engineering part number AOT9604*

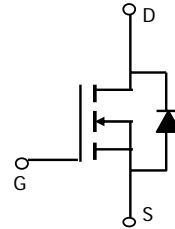
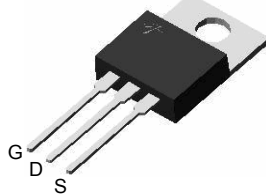
**General Description**

The AOT5N60 has been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low  $R_{DS(on)}$ ,  $C_{iss}$  and  $C_{rss}$  along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

**Features**

$V_{DS}$  (V) = 700V @ 150°C  
 $I_D$  = 5A  
 $R_{DS(on)} < 1.8 \Omega$  ( $V_{GS} = 10V$ )  
**100% UIS Tested!**  
**100%  $R_g$  Tested!**  
 **$C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$  Tested!**

Top View TO-220


**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Continuous Drain Current <sup>B</sup>	$I_D$	$T_C=25^\circ\text{C}$	5
		$T_C=100^\circ\text{C}$	3.2
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	16	A
Avalanche Current <sup>C</sup>	$I_{AR}$	2.6	A
Repetitive avalanche energy <sup>C</sup>	$E_{AR}$	100	mJ
Single pulsed avalanche energy <sup>G</sup>	$E_{AS}$	200	mJ
Peak diode recovery dv/dt	dV/dt	5	V/ns
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	132
		Derate above 25°C	1.05
Junction and Storage Temperature Range	$T_J, T_{STG}$	-50 to 150	°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	$T_L$	300	°C

**Thermal Characteristics**

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	54	65	°C/W
Maximum Case-to-Sink <sup>A</sup>	$R_{\theta CS}$	-	0.5	°C/W
Maximum Junction-to-Case <sup>D,F</sup>	$R_{\theta JC}$	0.76	0.95	°C/W

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}, T_J=25^\circ\text{C}$	600			V
		$I_D=250\mu\text{A}, V_{GS}=0\text{V}, T_J=150^\circ\text{C}$		700		V
$BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$		0.65		$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=600\text{V}, V_{GS}=0\text{V}$			1	$\mu\text{A}$
		$V_{DS}=480\text{V}, T_J=125^\circ\text{C}$			10	
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	3	3.9	5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=2.5\text{A}$		1.44	1.8	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=40\text{V}, I_D=2.5\text{A}$		7.7		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.76	1	V
$I_S$	Maximum Body-Diode Continuous Current				5	A
$I_{SM}$	Maximum Body-Diode Pulsed Current				16	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=25\text{V}, f=1\text{MHz}$	466	583	700	pF
$C_{oss}$	Output Capacitance		46	58.4	70	pF
$C_{riss}$	Reverse Transfer Capacitance		4.2	5.3	6.5	pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	2.9	3.7	5.6	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=480\text{V}, I_D=5\text{A}$		16.8	20	nC
$Q_{gs}$	Gate Source Charge		3.1	4	nC	
$Q_{gd}$	Gate Drain Charge		8.5	11	nC	
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=300\text{V}, I_D=5\text{A}, R_G=25\Omega$		21	25	ns
$t_r$	Turn-On Rise Time		44	55	ns	
$t_{D(off)}$	Turn-Off Delay Time		35	45	ns	
$t_f$	Turn-Off Fall Time		37	45	ns	
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=5\text{A}, di/dt=100\text{A}/\mu\text{s}, V_{DS}=100\text{V}$		208	250	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=5\text{A}, di/dt=100\text{A}/\mu\text{s}, V_{DS}=100\text{V}$		2	2.4	$\mu\text{C}$

A: The value of  $R_{\theta JA}$  is measured with the device in a still air environment with  $T_A=25^\circ\text{C}$ .

B: The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ .

D: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=150^\circ\text{C}$ .

G:  $L=60\text{mH}, I_{AS}=2.6\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$

Rev 0. July 2008

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

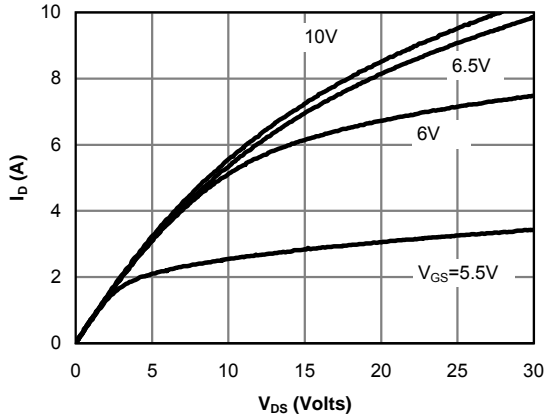


Fig 1: On-Region Characteristics

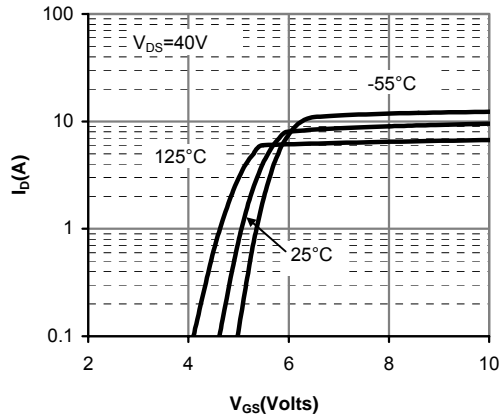


Figure 2: Transfer Characteristics

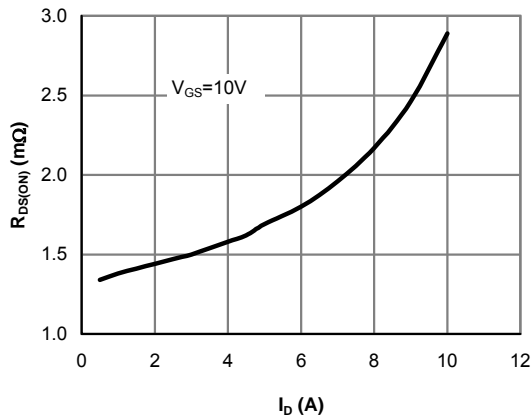


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

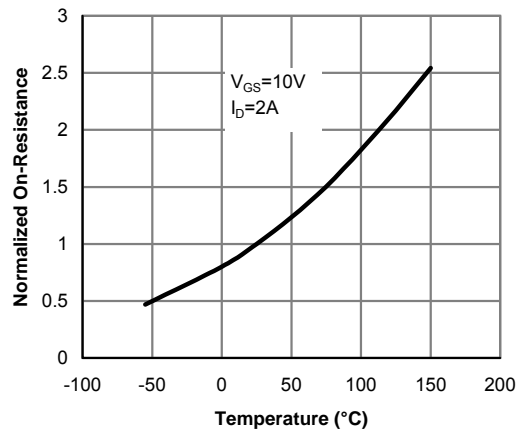


Figure 4: On-Resistance vs. Junction Temperature

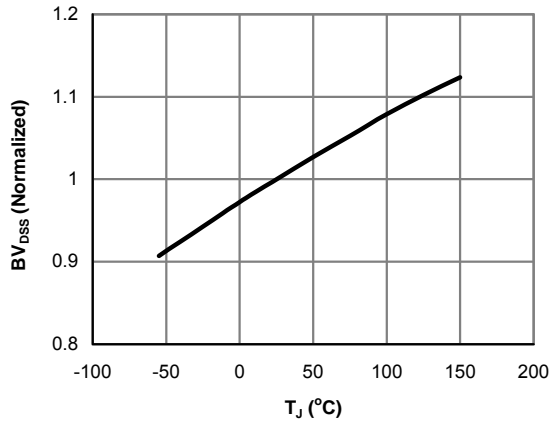


Figure 5: Break Down vs. Junction Temperature

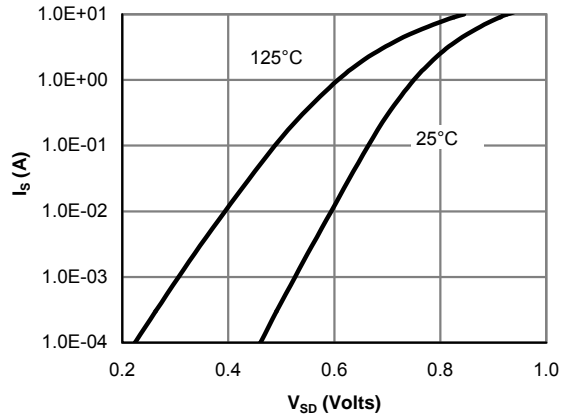


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

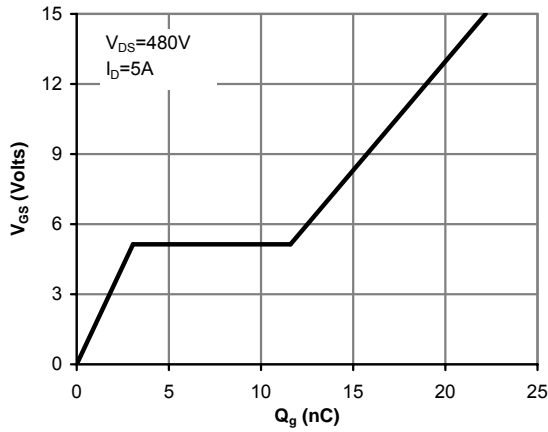


Figure 7: Gate-Charge Characteristics

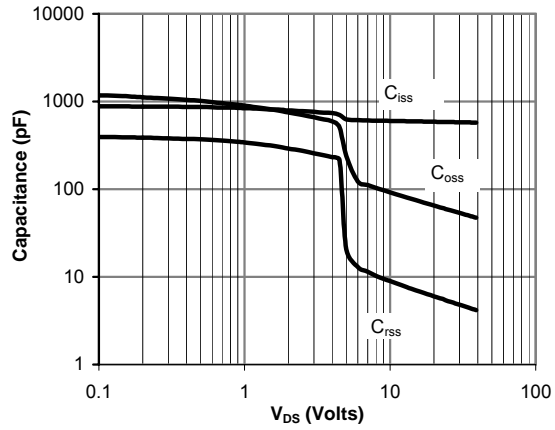


Figure 8: Capacitance Characteristics

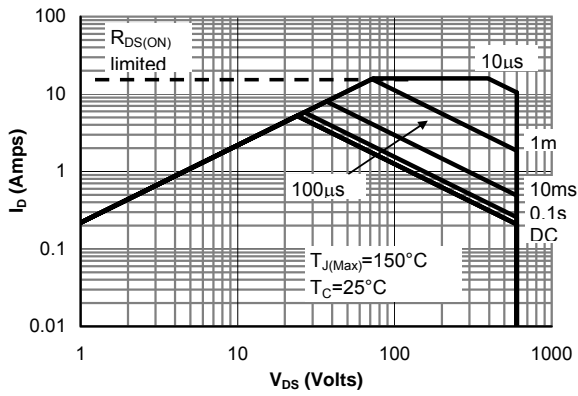


Figure 9: Maximum Forward Biased Safe Operating Area for AOT5N60 (Note F)

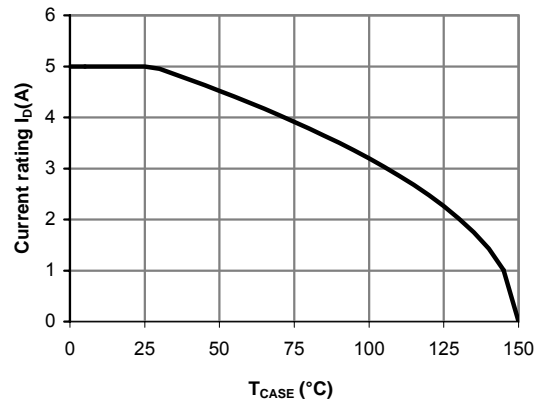


Figure 10: Current De-rating (Note B)

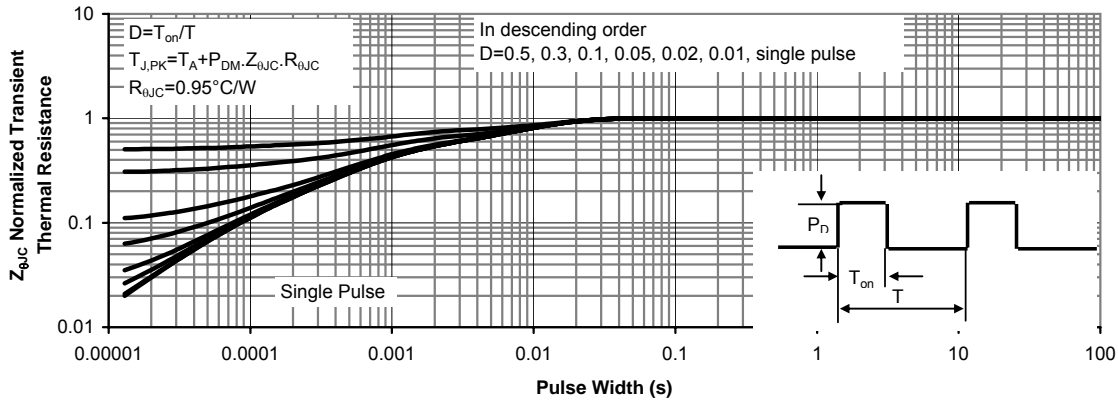
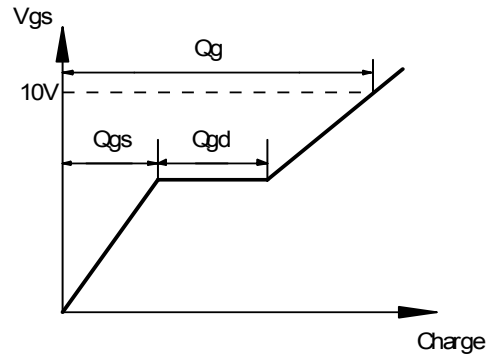
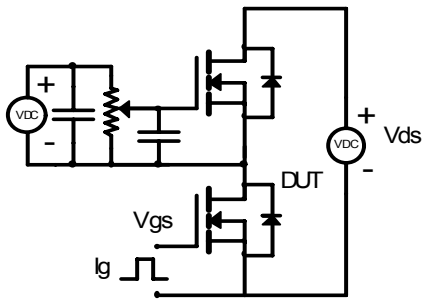
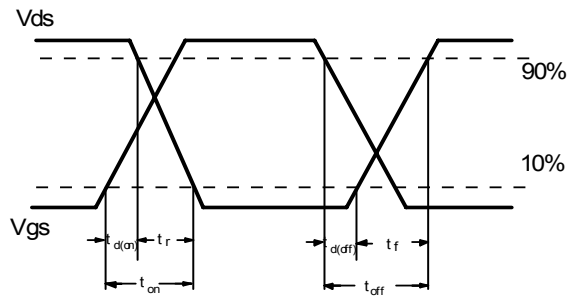
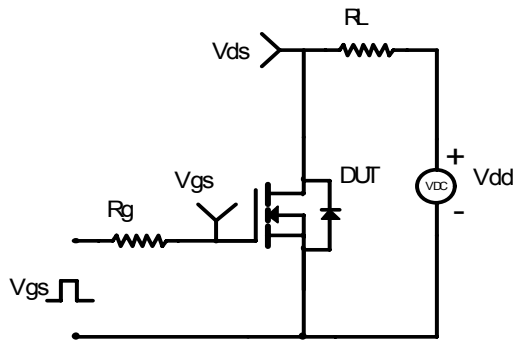


Figure 11: Normalized Maximum Transient Thermal Impedance for AOT5N60 (Note F)

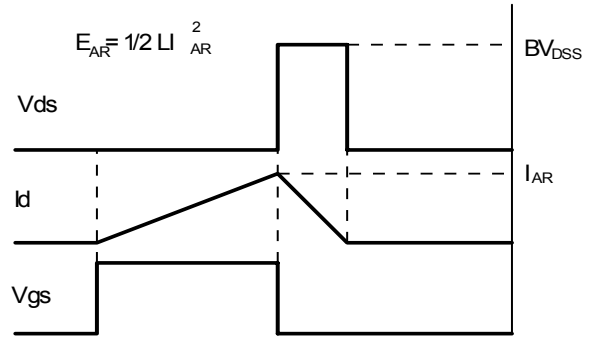
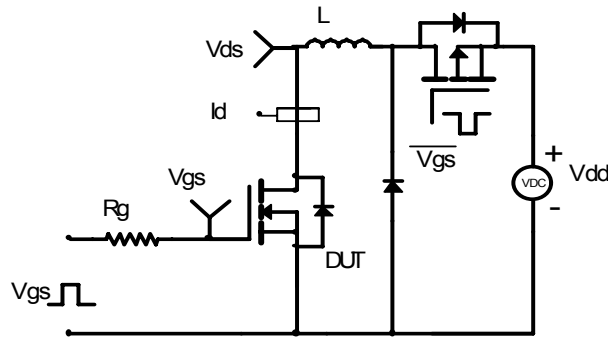
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

