TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6LD4

Gate Driver for TFT LCD Panels

Unit : mm

T6LD4	User Pitch Area	
	IN	OUT

For the latest TCP / COF specifications and product line-up, contact Toshiba or your local sales office.

COF (Chip On Film)

The T6LD4 is a 350 / 342-channel output gate driver for TFT LCD panels.

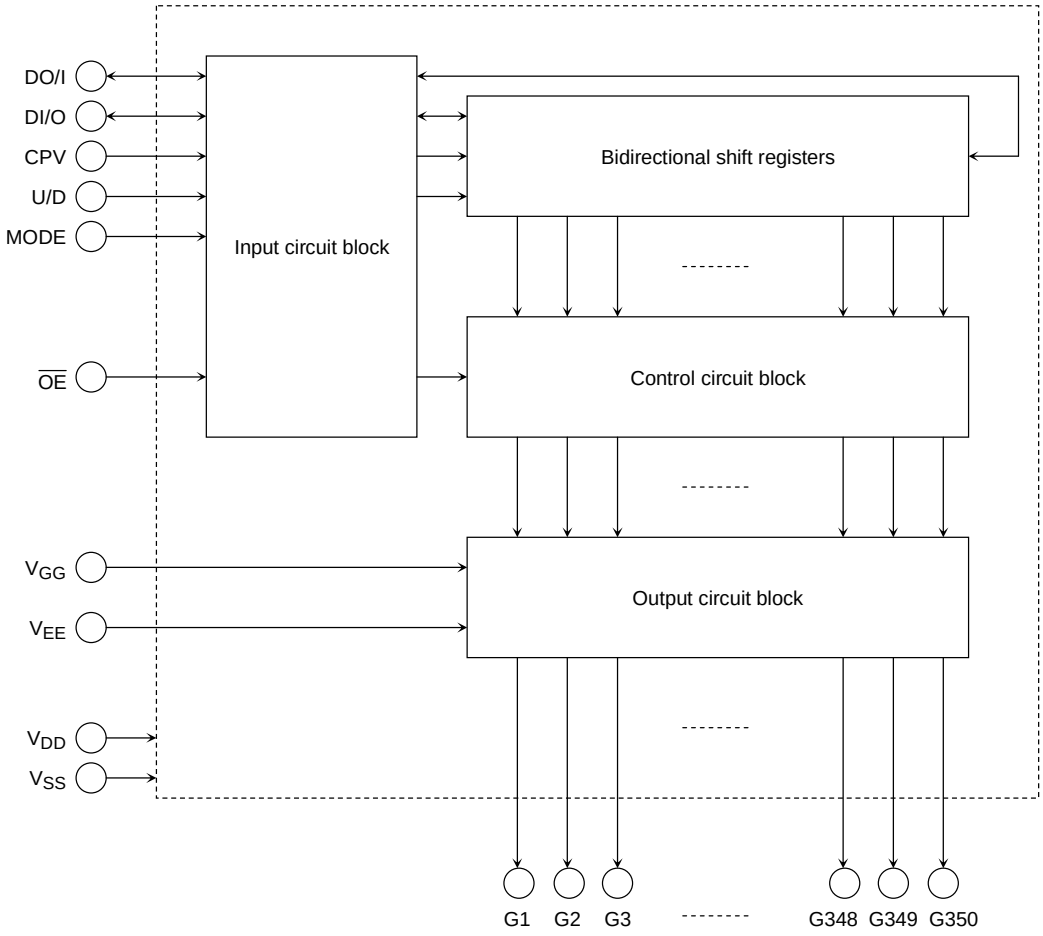
Features

- LCD drive output pins : Switchable 350 / 342 pins
- Logic power supply voltage : 2.3 to 3.6V
- LCD drive voltage : max 43.5V
- Data transfer method : Bidirectional shift register
- Operating temperature : −20 to 75°C
- Package : COF
- Built-in power on reset circuit

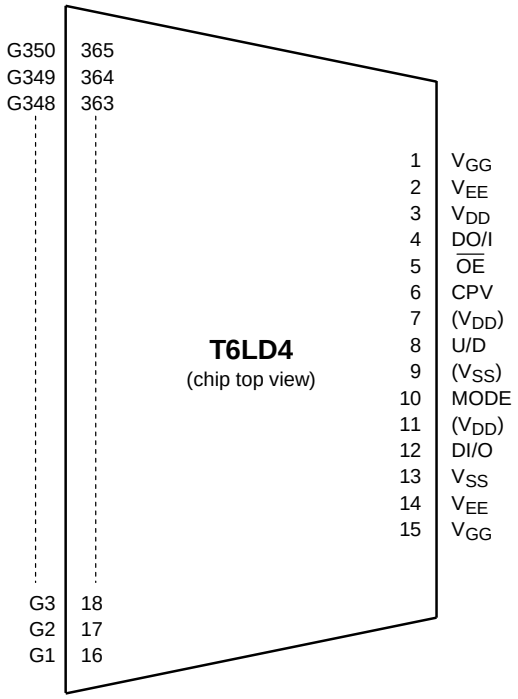
Application

Modules for PC monitor and Note PC

Block Diagram



Pin Assignment



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest COF specification.

Pin Description

<table>
<tr><th>Signal Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Vertical shift data input/output pins
These pins are used to input and output shift data. The function of these pins is switched for input or output by U/D as shown below:
<table>
<tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
When set for input
The data is latched into the internal shift registers synchronously with the rising edge of CPV.
When set for output
When two or more T6LD4s are cascaded, this pin outputs the data to be fed into the next stage. This data changes state synchronously with the falling edge of CPV.</td></tr>
<tr><td>U/D</td><td>I</td><td>Transfer direction select pin
This pin specifies the direction in which data is transferred through the shift registers.
The shift register data is shifted synchronously with each rising edge of CPV as follows:
When U/D is high, data is shifted in the direction
U/D = “H”: G1 → G2 → G3 → G4 → ··· → G350
When U / D is low, the direction is reversed to give
U/D = “L”: G350 → G349 → G348 → G347 → ··· → G1
The voltage applied to this pin must be a DC-level voltage that is either high (V_{DD}) or low (V_{SS}).
Apply the same DC-level voltage to these pins.</td></tr>
<tr><td>CPV</td><td>I</td><td>Vertical shift clock pin
This is the shift clock for the shift registers. Data is shifted through the shift registers synchronously with the rising edge of CPV.</td></tr>
<tr><td>$\overline{OE}$</td><td>I</td><td>Output enable pin
This signal controls the data appearing at the TFT -LCD panel drive pins (G1 to G350).
This pin operates asynchronously with CPV.
$\overline{OE}$ = high level : controls the LCD panel drive output to V_{EE}
$\overline{OE}$ = low level : outputs shift data and data contents.</td></tr>
<tr><td>MODE</td><td>I</td><td>Output select pin
This signal selects 350 / 342-pin mode for the LCD panel driver.
<table>
<tr><th>MODE</th><th>Output mode</th><th>The unapplied LCD panel drive pins</th></tr>
<tr><td>H</td><td>350-out</td><td>—</td></tr>
<tr><td>L</td><td>342-out</td><td>G171 to G178 (V_{EE} level)</td></tr>
</table>
The voltage applied to this pin must be a DC -level voltage that is either high (V_{DD}) or low (V_{SS}).</td></tr>
<tr><td>G1 to G350</td><td>O</td><td>TFT-LCD panel driver pins
These pins output the shift register data or the voltage of V_{GG} or V_{EE} depending on the control $\overline{OE}$ signal.</td></tr>
<tr><td>V_{GG}</td><td></td><td>Power supply for TFT-LCD drive pin</td></tr>
<tr><td>V_{EE}</td><td></td><td>Power supply for TFT-LCD drive pin</td></tr>
<tr><td>V_{DD}</td><td></td><td>Power supply for the internal logic pin
These signals arranged right and left is connected on the film.
Apply the same voltage to these pins. The (V_{DD}) is the pin for connection.</td></tr>
<tr><td>V_{SS}</td><td></td><td>Power supply for the internal logic pin
These signals arranged right and left is connected on the film.
Apply the same voltage to these pins. The (V_{SS}) is the pin for connection.</td></tr>
</table>

Device Operation

● Shift data transfer method

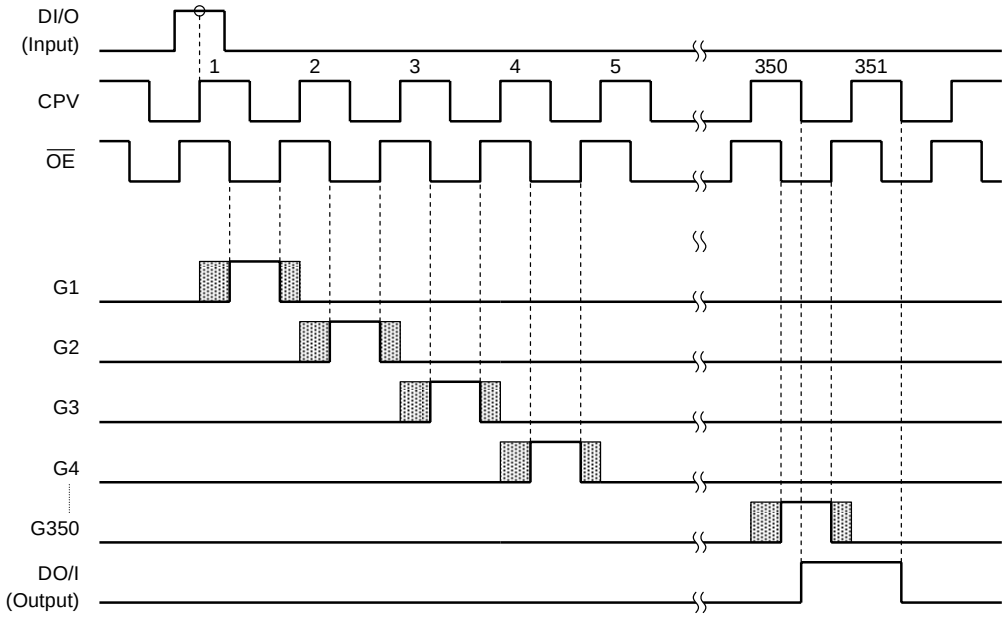
MODE	Output Mode	U/DPin	Shift data		Data Transfer Method
			Input	Output	
H	350-out	H	DI/O	DO/I	G1 → G2 → G3 → G4 → ··· → G350
		L	DO/I	DI/O	G350 → G349 → G348 → ··· → G1
L	342-out	H	DI/O	DO/I	G1 → G2 → G3 → G4 → ··· → G170→ G179 → ··· → G350
		L	DO/I	DI/O	G350 → G349 → G348 → ···→ G179 → G170 → ··· → G1

The input data (DI/O or DO/I) is latched into the internal register synchronously with the rising edge of the shift clock CPV. At the same time that the data is shifted to the next register at the next rise of CPV, new vertical shift data is latched into.

In the output operation, the data in the last shift register (G350 or G1) is output synchronously with the falling edge of CPV. (The output high voltage is the V_{DD} level; the output low voltage is the V_{SS} level.)

Timing Chart 1

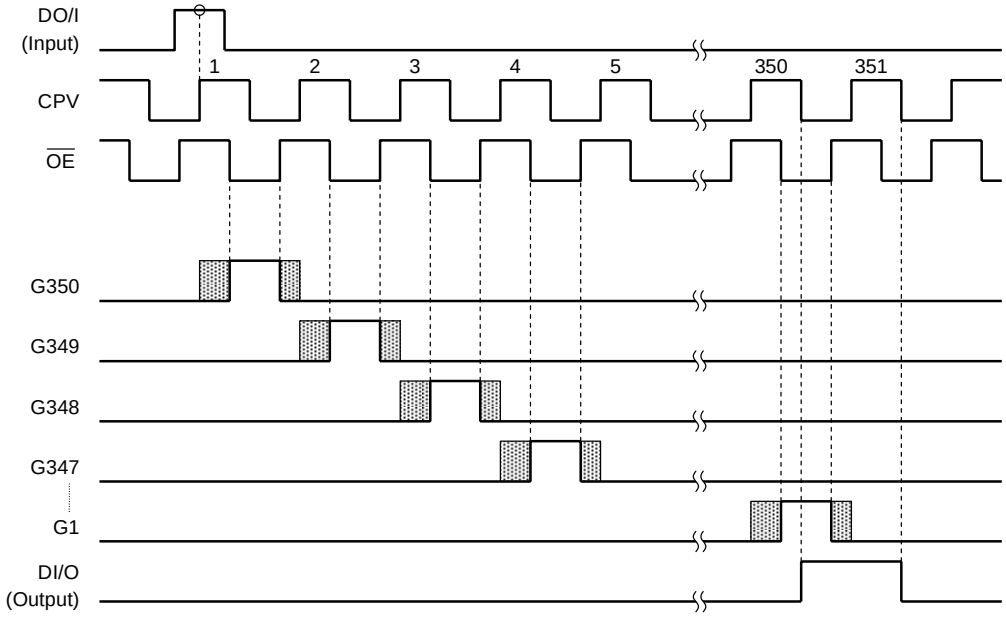
(350-out mode, U/D = high level, MODE = high level)



: This part is output which is controlled (fixed to V_{EE}) by $\overline{OE}$ pin

Timing Chart 2

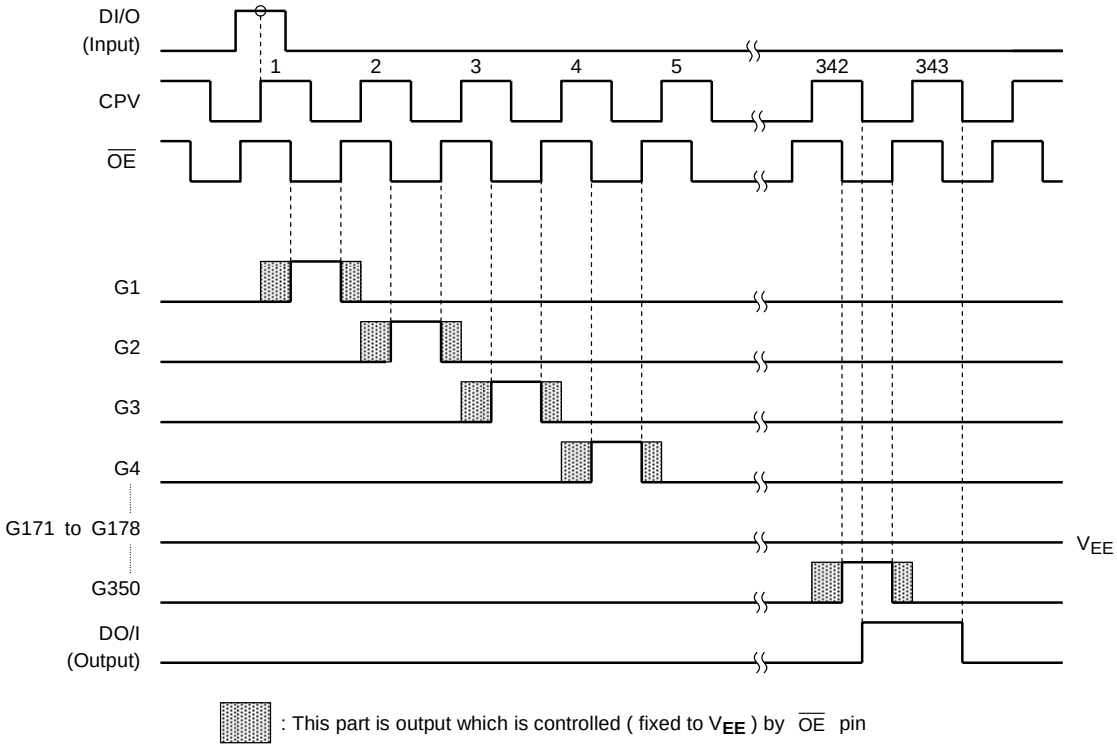
(350-out mode, U/D = low level, MODE = high level)



: This part is output which is controlled (fixed to V_{EE}) by $\overline{OE}$ pin

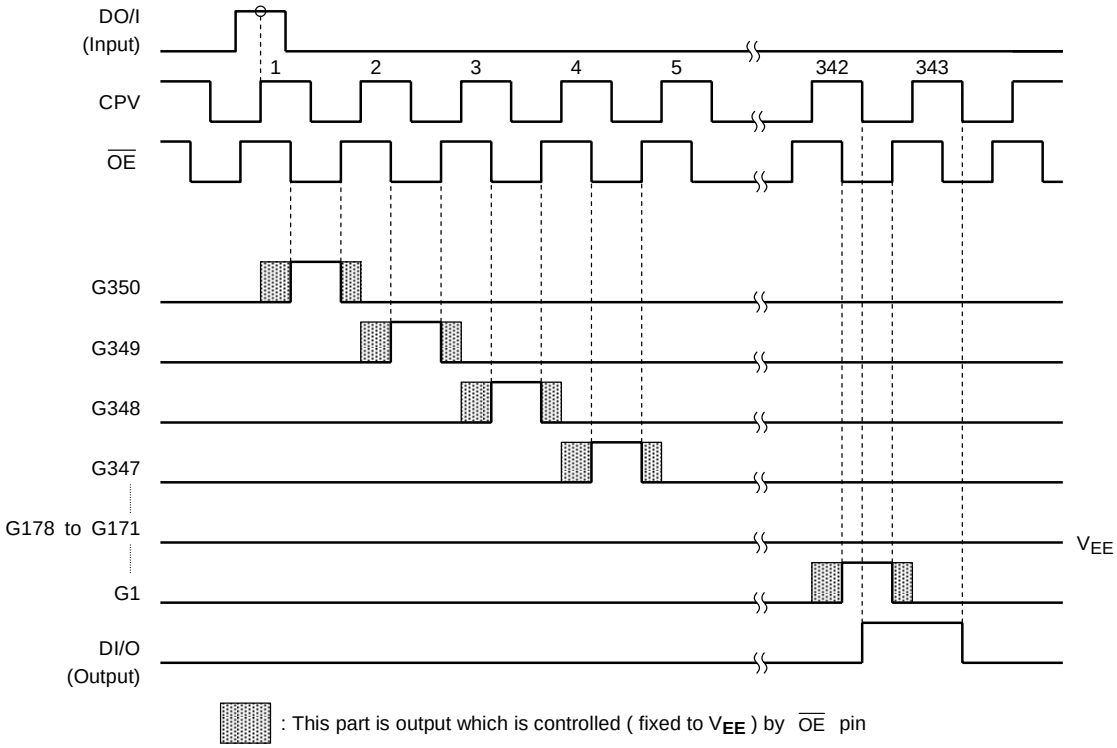
Timing Chart 3

(342-out mode, U/D = high level, MODE = low level)



Timing Chart 4

(342-out mode, U/D = low level, MODE = low level)



Maximum Ratings (V_{SS} = 0 V)

Characteristics	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	−0.3 to 4.0	V
Supply voltage (2)	V_{GG}	−0.3 to 45.0	
Supply voltage (3)	V_{EE}	−20.0 to 0.3	
Supply voltage (1)	$V_{GG} - V_{EE}$	−0.3 to 45.0	
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Storage temperature	T_{stg}	−55 to 125	°C

Operating Range (V_{SS} = 0 V)

Characteristics	Symbol	Rating	Unit
Supply voltage (3)	V_{DD}	2.3 to 3.6	V
Supply voltage (2)	V_{GG}	10 to 35	
Supply voltage (4)	V_{EE}	−15 to −5	
Supply voltage (1)	$V_{GG} - V_{EE}$	15.0 to 43.5	
Operating temperature	T_{opr}	−20 to 75	°C
Operating frequency	f_{CPV}	100 (max)	kHz
Output load capacitance	C_L	600 (max)	pF/PIN

Electrical Characteristics

DC Characteristics (unless otherwise specified, $V_{GG} - V_{EE}$ = 30.0 to 43.5 V, V_{DD} = 2.3 to 3.6 V, V_{SS} = 0 V, Ta = −20 to 75°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Max	Unit	Relevant Pin
Input voltage	Low level	V_{IL}	—	—	V_{SS}	0.3 × V_{DD}	V	(Note 1)
	High level	V_{IH}	—		0.7 × V_{DD}	V_{DD}		
Output voltage	Low level	V_{OL}	—	I_{OL} = 40 μA	V_{SS}	V_{SS} + 0.4	V	DI/O, DO/I
	High level	V_{OH}	—	I_{OH} = −40 μA	V_{DD} − 0.4	V_{DD}		
Output resistance	Low level	R_{OL}	—	V_{OUT} = V_{EE} + 0.5 V	—	1000	Ω	G1 to G350
	High level	R_{OH}		V_{OUT} = V_{GG} − 0.5 V				
Input current		I_{IN}	—	—	−1	1	μA	(Note 1)
Current dissipation		I_{GG}	—	no load (Note 2)	—	200	μA	V_{GG}
		I_{DD}	—		—	50		V_{DD}
		I_{EE}	—		—	200		V_{EE}

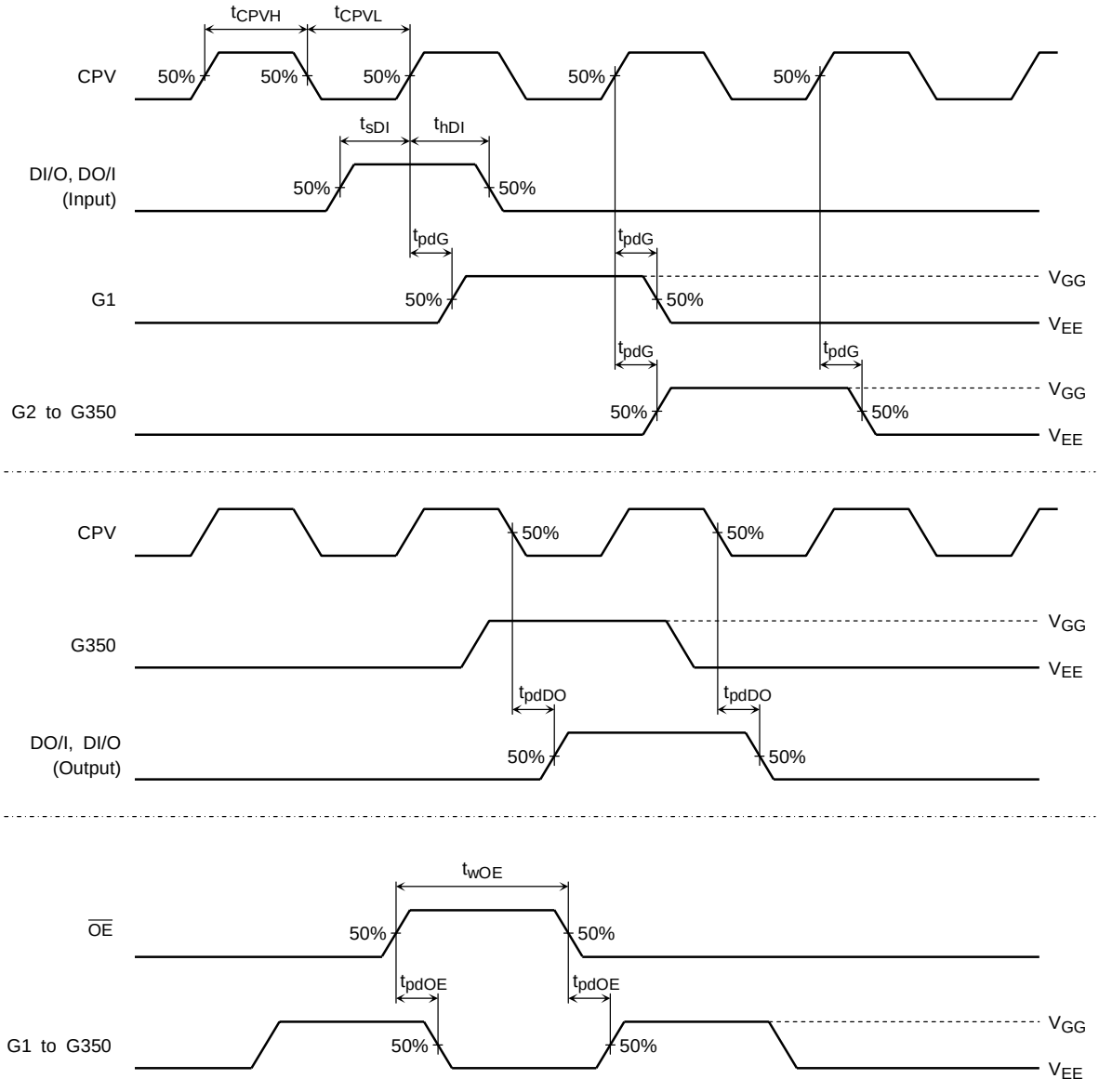
Note1: DI/O , DO/I , CPV, $\overline{OE}$

Note2: f_{CPV} = 50 kHz, Shift data input : 60Hz 1pulse, $\overline{OE}$ = low level, MODE = high level

AC Characteristics

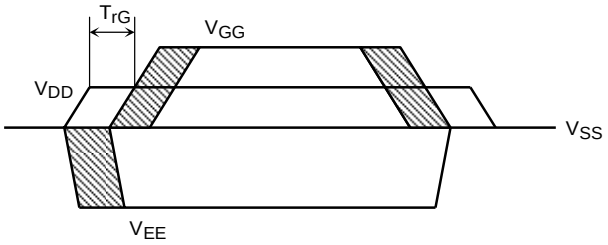
(unless otherwise specified, $V_{GG} - V_{EE}$ = 30.0 to 43.5 V, V_{DD} = 2.3 to 3.6 V, V_{SS} = 0 V, Ta = −20 to 75°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Max	Unit
Clock pulse frequency	t_{CPV}	—	—	—	100	kHz
Clock pulse width (H)	t_{CPVH}	—	—	500	—	ns
Clock pulse width (L)	t_{CPVL}	—	—	500	—	
Data setup time	t_{sDI}	—	—	200	—	ns
Data hold time	t_{hDI}	—	—	200	—	
OE pulse width	t_{wOE}	—	—	1	—	μs
Output delay time (1)	t_{pdDO}	—	C_L = 50 pF	—	200	ns
Output delay time (2)	t_{pdG}	—	C_L = 600 pF	—	1000	
Output delay time (3)	t_{pdOE}	—	C_L = 600 pF	—	1000	



Power Supply Sequence

Turn power on in the order $V_{DD} \rightarrow V_{EE} \rightarrow$ Input signal $\rightarrow V_{GG}$. Turn power off in th reverse order.
It may input V_{EE}, input signal and V_{GG} simultaneously.
T6LD4 have the Power On Reset function. ($T_{rG} \geq 10\mu s$)



Instruction for operating circumstances

- Light striking a semiconductor device can generate electromotive force due to photoelectric effects. In some cases this may cause the device to malfunction.
  This is more likely to be affected for the devices in which the surface (back), or side of the chip is exposed. At the design phase, please make sure that devices are protected against incident light from external sources. Please take into account of incident light from external sources during actual operation and during inspection.

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