To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

RENESAS
Renesas Technology Corp.

DESCRIPTION

The 38C3 group is the 8-bit microcomputer based on the 740 family core technology.

The 38C3 group has a LCD drive control circuit, a 10-channel A-D converter, and a Serial I/O as additional functions.

The various microcomputers in the 38C3 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 38C3 group, refer to the section on group expansion.

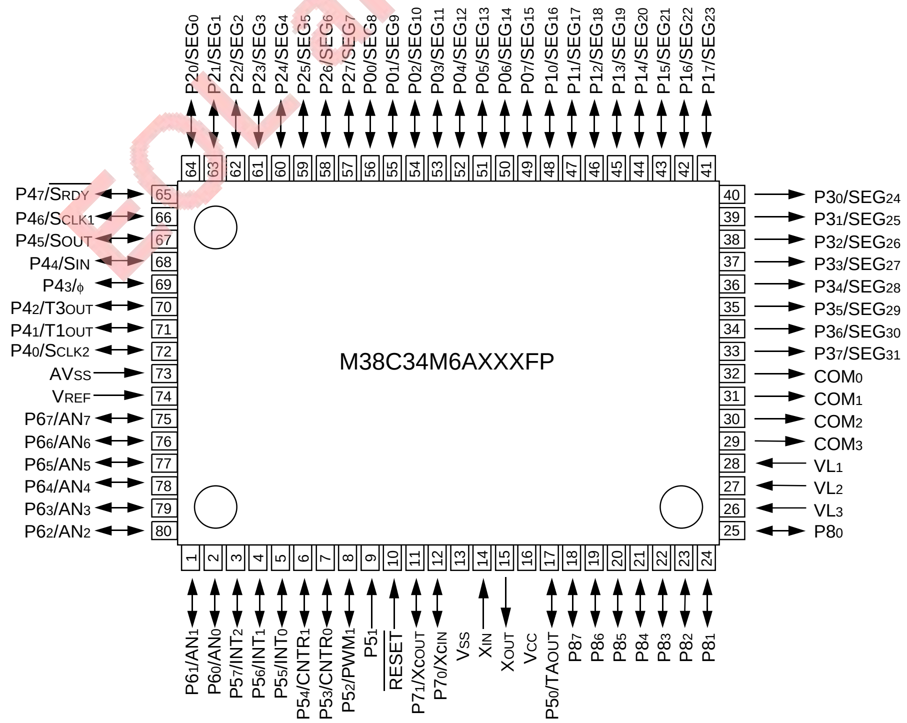
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time .... 0.5 µs
  (at 8MHz oscillation frequency)
- Memory size
  ROM .... 4 K to 48 K bytes
  RAM .... 192 to 1024 bytes
- Programmable input/output ports 57
- Software pull-up/pull-down resistors
  .... (Ports P0–P8 except Port $P5_1$)
- Interrupts .... 16 sources, 16 vectors
  (includes key input interrupt)
- Timers .... 8-bit × 6, 16-bit × 1
- A-D converter .... 10-bit × 8 channels
- Serial I/O .... 8-bit × 1 (Clock-synchronized)
- LCD drive control circuit
  Bias 1/1, 1/2, 1/3
  Duty 1/1, 1/2, 1/3, 1/4
  Common output 4
  Segment output 32
- 2 Clock generating circuit
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  In high-speed mode .... 4.0 to 5.5 V
  In middle-speed mode .... 2.5 to 5.5 V
  In low-speed mode .... 2.5 to 5.5 V
- Power dissipation
  In high-speed mode .... 32 mW
  (at 8 MHz oscillation frequency)
  In low-speed mode .... 45 µW
  (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range .... – 20 to 85°C

APPLICATIONS

Camera, household appliances, consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : 80P6N-A
80-pin plastic-molded QFP

Fig. 1 M38C34M6AXXXFP pin configuration

FUNCTIONAL BLOCK DIAGRAM

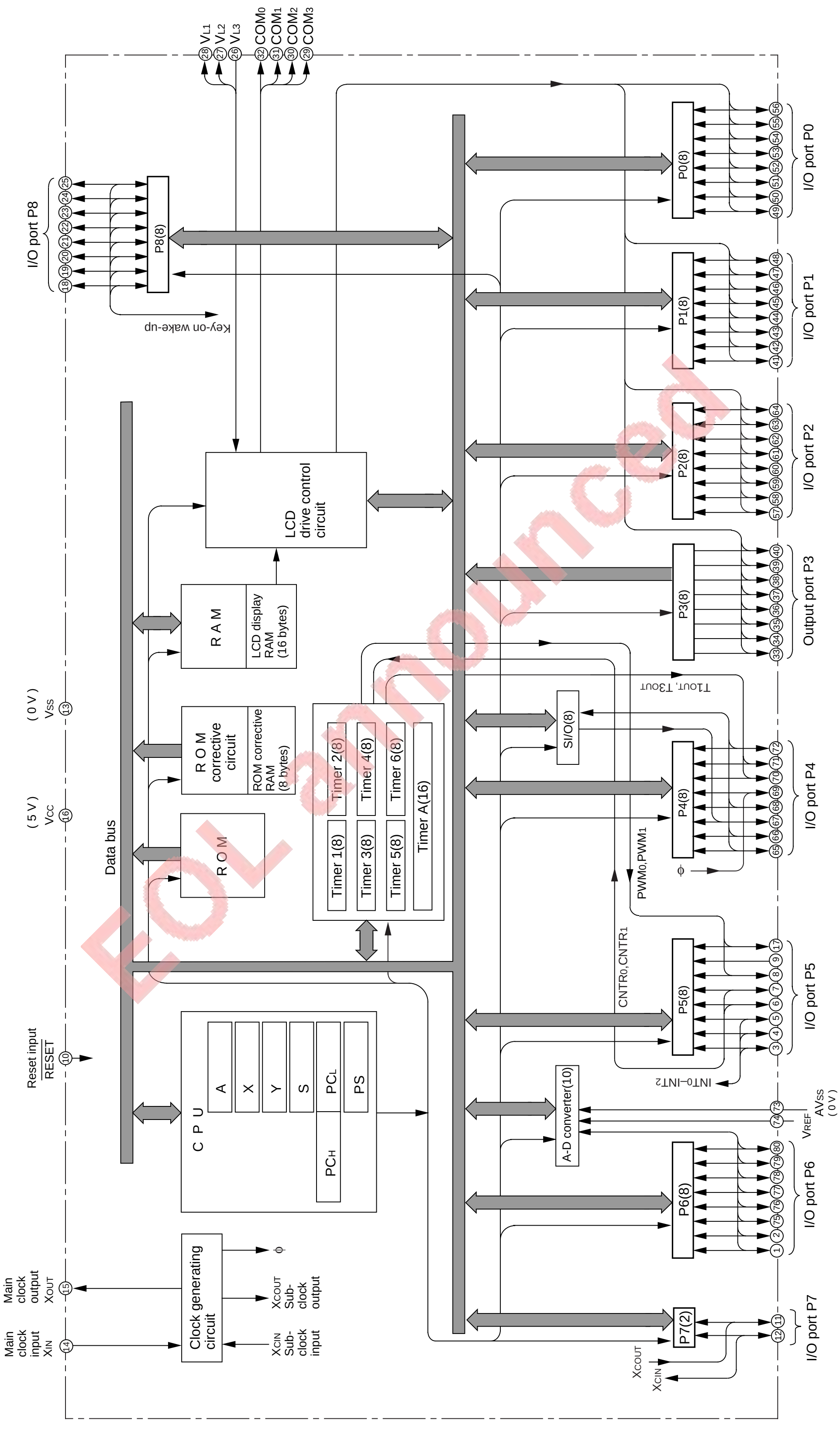


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	• Apply voltage of 2.5 V to 5.5 V to V_{CC}, and 0 V to V_{SS}.	
V_{REF}	Analog reference voltage	• Reference voltage input pin for A-D converter.	
AV_{SS}	Analog power source	• GND input pin for A-D converter. • Connect to V_{SS}.	
$\overline{RESET}$	Reset input	• Reset input pin for active “L.”	
X_{IN}	Clock input	• Input and output pins for the main clock generating circuit. • Feedback resistor is built in between X_{IN} pin and X_{OUT} pin. • Connect a ceramic resonator or a quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. • If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
V_{L1} – V_{L3}	LCD power source	• Input $0 \leq V_{L1} \leq V_{L2} \leq V_{L3} \leq V_{CC}$ voltage. • Input 0 – V_{L3} voltage to LCD.	
COM_0 – COM_3	Common output	• LCD common output pins. • COM_1, COM_2, and COM_3 are not used at 1/1 duty ratio. • COM_2 and COM_3 are not used at 1/2 duty ratio. • COM_3 is not used at 1/3 duty ratio.	
$P0_0/SEG_9$ – $P0_7/SEG_{15}$	I/O port P0	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each port to be individually programmed as either input or output. • Pull-down control is enabled.	• LCD segment pins
$P1_0/SEG_{16}$ – $P1_7/SEG_{23}$	I/O port P1		
$P2_0/SEG_0$ – $P2_7/SEG_7$	I/O port P2		
$P3_0/SEG_{24}$ – $P3_7/SEG_{31}$	Output port P3	• 8-bit output port. • CMOS state output. • Pull-down control is enabled.	
$P4_0/S_{CLK2}$	I/O port P4	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Serial I/O function pin
$P4_1/T_{1OUT}$			• Timer output pin
$P4_2/T_{3OUT}$			• Timer output pin
$P4_3/\phi$			• ϕ output pin
$P4_4/S_{IN}$, $P4_5/S_{OUT}$, $P4_6/\overline{S_{CLK1}}$, $P4_7/\overline{S_{RDY}}$			• Serial I/O function pins

Table 2 Pin description (2)

Pin	Name	Function	Function except a port function
$P5_1$	Input port P5	• 1-bit input pin. • CMOS compatible input level.	
$P5_0/TA_{OUT}$	I/O port P5	• 7-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Timer A output pin
$P5_2/PWM_1$			• PWM_1 output (timer output) pin
$P5_3/CNTR_0$, $P5_4/CNTR_1$			• External count I/O pins
$P5_5/INT_0$, $P5_6/INT_1$, $P5_7/INT_2$			• External interrupt input pins
$P6_0/AN_0$ – $P6_7/AN_7$	I/O port P6	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• A-D conversion input pins
$P7_0/X_{COUT}$, $P7_1/X_{CIN}$	I/O port P7	• 2-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Sub-clock generating circuit I/O pins
$P8_0$ – $P8_7$	I/O port P8	• 8-bit I/O port. • TTL input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Key input (Key-on wake-up) interrupt input pins

PART NUMBERING

Product M38C3 4 M 6 A XXX FP

- FP — Package type
  - FP : 80P6N-A package
  - FS : 80D0 package
- XXX — ROM number
  - Omitted in some types.
- A
  - A : Standard**(Note)**
  - M : M version
- 6 — ROM/PROM size
  - 1 : 4096 bytes
  - 2 : 8192 bytes
  - 3 : 12288 bytes
  - 4 : 16384 bytes
  - 5 : 20480 bytes
  - 6 : 24576 bytes
  - 7 : 28672 bytes
  - 8 : 32768 bytes
  - 9 : 36864 bytes
  - A : 40960 bytes
  - B : 45056 bytes
  - C : 49152 bytes

  The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used.
- M — Memory type
  - M : Mask ROM version
  - E : EPROM or One Time PROM version
- 4 — RAM size
  - 0 : 192 bytes
  - 1 : 256 bytes
  - 2 : 384 bytes
  - 3 : 512 bytes
  - 4 : 640 bytes
  - 5 : 768 bytes
  - 6 : 896 bytes
  - 7 : 1024 bytes

Note : Difference between standard and M version

- Standard : Port P5$_0$/TA$_{OUT}$ pin remains set to the input mode until the direction register is set to the output mode during reset and after reset.
- M version : Port P5$_0$/TA$_{OUT}$ pin remains set to the output mode (“L” output) until the direction register is set to the input mode during reset and after reset.

Fig. 3 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 38C3 group as follows.

Memory Type

Support for mask ROM, One Time PROM, and EPROM versions

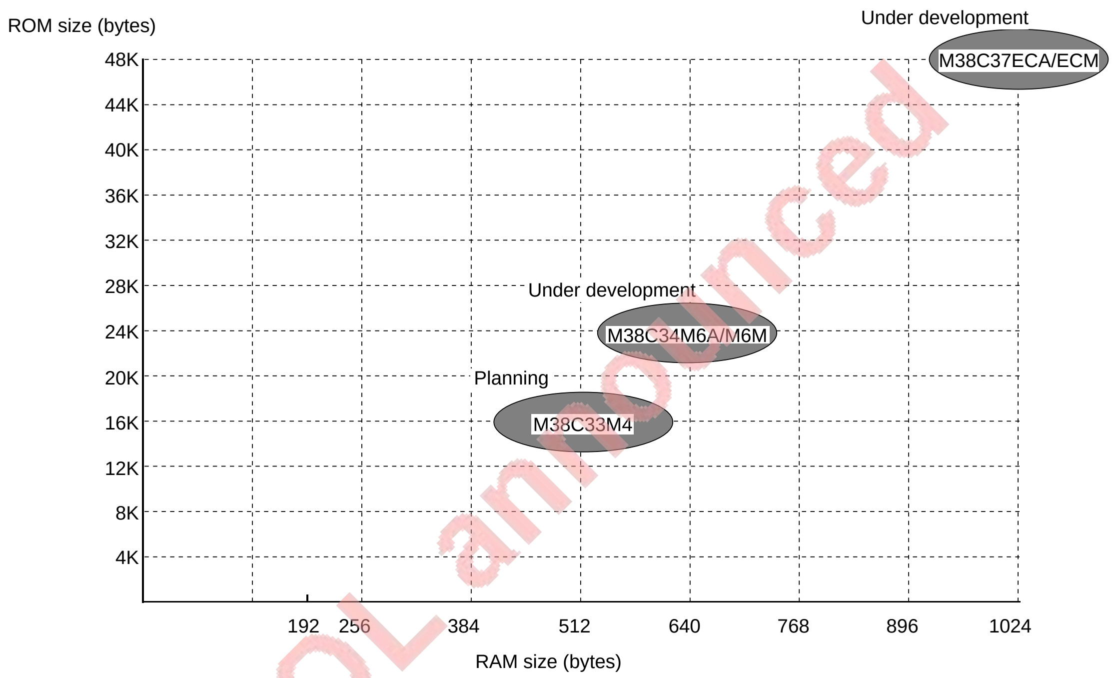
Memory Size

ROM/PROM size .... 16 K to 48 K bytes
RAM size .... 512 to 1024 bytes

Packages

80P6N-A .... 0.8 mm-pitch plastic molded QFP
80D0 .... 0.8 mm-pitch ceramic LCC (EPROM version)

Memory Expansion Plan



Products under development or planning : the development schedule and specification may be revised without notice.
Planning products may be stopped the development.

Fig. 4 Memory expansion plan

Currently planning products are listed below.

Table 3 Support products As of April 1998

Product name	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38C34M6AXXXFP	24576 (24446)	640	80P6N-A	Mask ROM version
M38C37ECAXXXFP	49152 (49022)	1024	80P6N-A	One Time PROM version
M38C37ECAFP	49152 (49022)	1024	80P6N-A	One Time PROM version (blank)
M38C37ECAFS	49152 (49022)	1024	80D0	EPROM version
M38C34M6MXXXFP	24576 (24446)	640	80P6N-A	Mask ROM version
M38C37ECMXXXFP	49152 (49022)	1024	80P6N-A	One Time PROM version
M38C37ECMFP	49152 (49022)	1024	80P6N-A	One Time PROM version (blank)
M38C37ECMFS	49152 (49022)	1024	80D0	EPROM version

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 38C3 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

[CPU Mode Register (CPUM)] $003B_{16}$

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

The CPU mode register is allocated at address $003B_{16}$.

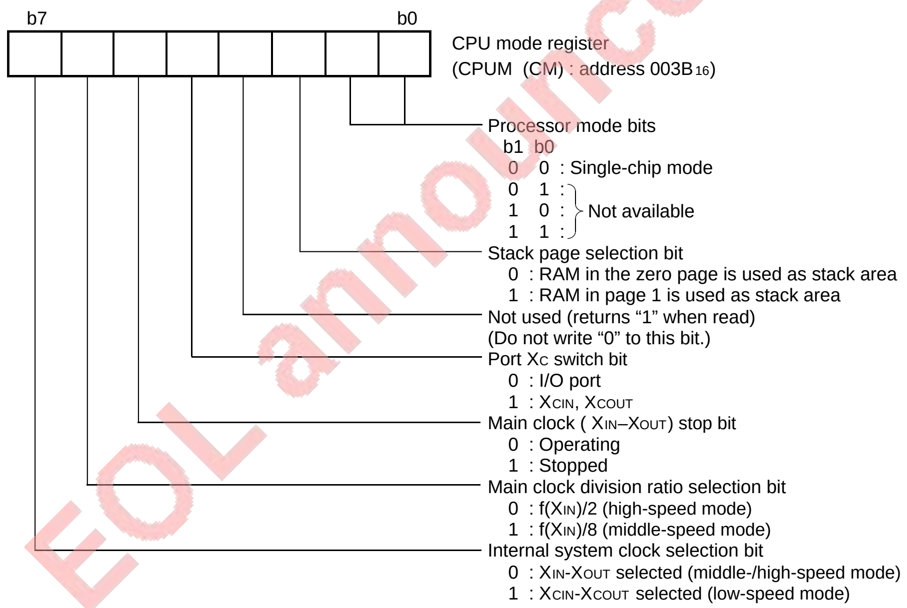


Fig. 5 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

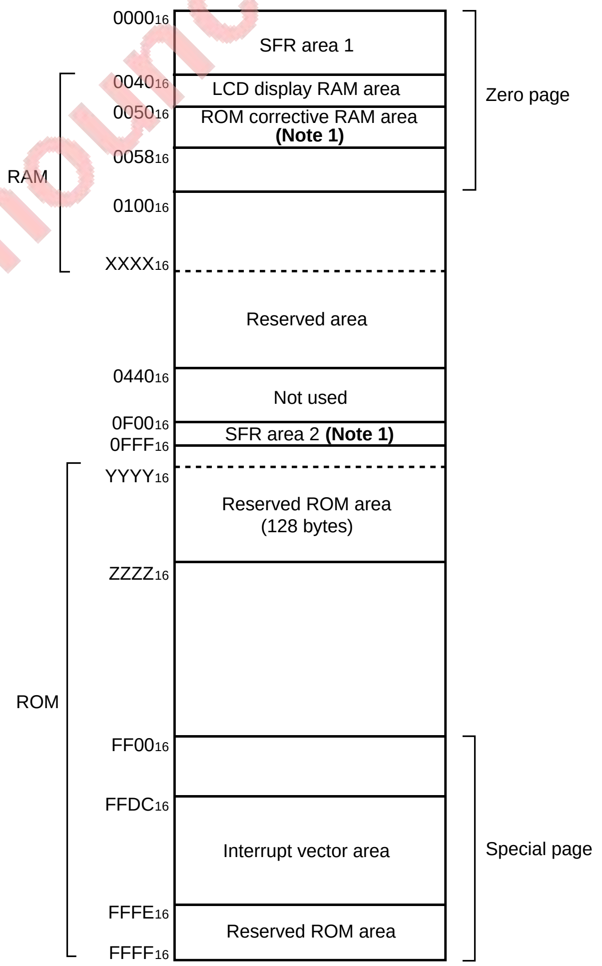
Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM size (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}
45056	5000_{16}	5080_{16}
49152	4000_{16}	4080_{16}



Note 1 : This is valid only in mask ROM version.

Fig. 6 Memory map diagram

Address	Register
0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	
0008_{16}	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)
$000A_{16}$	Port P5 (P5)
$000B_{16}$	Port P5 direction register (P5D)
$000C_{16}$	Port P6 (P6)
$000D_{16}$	Port P6 direction register (P6D)
$000E_{16}$	Port P7 (P7)
$000F_{16}$	Port P7 direction register (P7D)
0010_{16}	Port P8 (P8)
0011_{16}	Port P8 direction register (P8D)
0012_{16}	
0013_{16}	
0014_{16}	
0015_{16}	
0016_{16}	PULL register A (PULLA)
0017_{16}	PULL register B (PULLB)
0018_{16}	Port P8 output selection register (P8SEL)
0019_{16}	Serial I/O control register 1 (SIOCON1)
$001A_{16}$	Serial I/O control register 2 (SIOCON2)
$001B_{16}$	Serial I/O register (SIO)
$001C_{16}$	
$001D_{16}$	
$001E_{16}$	
$001F_{16}$	

Address	Register
0020_{16}	Timer 1 (T1)
0021_{16}	Timer 2 (T2)
0022_{16}	Timer 3 (T3)
0023_{16}	Timer 4 (T4)
0024_{16}	Timer 5 (T5)
0025_{16}	Timer 6 (T6)
0026_{16}	
0027_{16}	Timer 6 PWM register (T6PWM)
0028_{16}	Timer 12 mode register (T12M)
0029_{16}	Timer 34 mode register (T34M)
$002A_{16}$	Timer 56 mode register (T56M)
$002B_{16}$	ϕ output control register (CKOUT)
$002C_{16}$	Timer A register (low) (TAL)
$002D_{16}$	Timer A register (high) (TAH)
$002E_{16}$	Compare register (low) (CONAL)
$002F_{16}$	Compare register (high) (CONAH)
0030_{16}	Timer A mode register (TAM)
0031_{16}	Timer A control register (TACON)
0032_{16}	A-D control register (ADCON)
0033_{16}	A-D conversion register (low) (ADL)
0034_{16}	A-D conversion register (high) (ADH)
0035_{16}	
0036_{16}	
0037_{16}	
0038_{16}	Segment output enable register (SEG)
0039_{16}	LCD mode register (LM)
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)

Address	Register
$0F01_{16}$	ROM correct enable register 1 **(Note)**
$0F02_{16}$	ROM correct high-order address register 1 **(Note)**
$0F03_{16}$	ROM correct low-order address register 1 **(Note)**
$0F04_{16}$	ROM correct high-order address register 2 **(Note)**
$0F05_{16}$	ROM correct low-order address register 2 **(Note)**
$0F06_{16}$	ROM correct high-order address register 3 **(Note)**
$0F07_{16}$	ROM correct low-order address register 3 **(Note)**
$0F08_{16}$	ROM correct high-order address register 4 **(Note)**
$0F09_{16}$	ROM correct low-order address register 4 **(Note)**

Address	Register
$0F0A_{16}$	ROM correct high-order address register 5 **(Note)**
$0F0B_{16}$	ROM correct low-order address register 5 **(Note)**
$0F0C_{16}$	ROM correct high-order address register 6 **(Note)**
$0F0D_{16}$	ROM correct low-order address register 6 **(Note)**
$0F0E_{16}$	ROM correct high-order address register 7 **(Note)**
$0F0F_{16}$	ROM correct low-order address register 7 **(Note)**
$0F10_{16}$	ROM correct high-order address register 8 **(Note)**
$0F11_{16}$	ROM correct low-order address register 8 **(Note)**

Note: This register is valid only in mask ROM version.

Fig. 7 Memory map of special function register (SFR)

I/O PORTS
[Direction Registers (ports P2, P4, $P5_0$, $P5_2$–$P5_7$, and P6–P8)]

The I/O ports P2, P4, $P5_0$, $P5_2$–$P5_7$, and P6–P8 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.
When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.
If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

[Direction Registers (ports P0 and P1)]

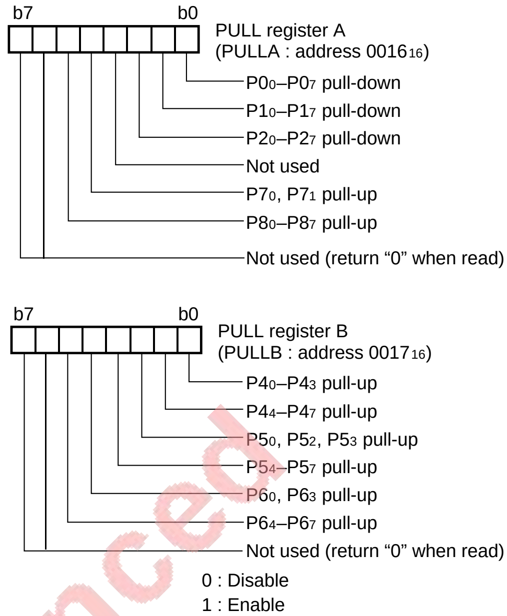
Ports P0 and P1 have direction registers which determine the input/output direction of each individual port.
Each port in a direction register corresponds to one port, each port can be set to be input or output.
When “0” is written to the bit 0 of a direction register, that port becomes an input port. When “1” is written to that port, that port becomes an output port. Bits 1 to 7 of ports P0 and P1 direction registers are not used.

Pull-up/Pull-down Control

By setting the PULL register A (address 0016_{16}) or the PULL register B (address 0017_{16}), ports except for ports P3 and $P5_1$ can control either pull-down or pull-up (pins that are shared with the segment output pins for LCD are pull-down; all other pins are pull-up) with a program.
However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports.

Port P8 Output Selection

Ports $P8_0$ to $P8_7$ can be switched to N-channel open-drain output by setting “1” to the port P8 output selection register.



Note : The contents of PULL register A and PULL register B do not affect ports programmed as the output ports.

Fig. 8 Structure of PULL register A and PULL register B

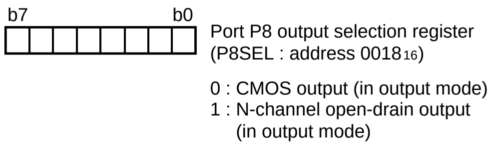


Fig. 9 Structure of port P8 output selection register

Table 4 List of I/O port function (1)

Pin	Name	Input/Output	I/O format	Non-port function	Related SFRs	Ref. No.
$P0_0$/SEG_8 – $P0_7$/SEG_{15}	Port P0	Input/Output, port unit	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1)
$P1_0$/SEG_{16} – $P1_7$/SEG_{23}	Port P1	Input/Output, port unit	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	
$P2_0$/SEG_0 – $P2_7$/SEG_7	Port P2	Input/Output, individual bits	CMOS compatible input CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	
$P3_0$/SEG_{24} – $P3_7$/SEG_{31}	Port P3	Output, individual bits	CMOS 3-state output	LCD segment output	Segment output enable register	(2)

Table 5 List of I/O port function (2)

Pin	Name	Input/Output	I/O format	Non-port function	Related SFRs	Ref. No.
$P4_0/S_{CLK2}$	Port P4	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O function I/O	Serial I/O control registers 1, 2 PULL register B	(3)
$P4_1/T_{1OUT}$				Timer output	Timer 12 mode register PULL register B	(4)
$P4_2/T_{3OUT}$				Timer output	Timer 34 mode register PULL register B	(4)
$P4_3/\phi$				ϕ clock output	ϕ output control register PULL register B	(5)
$P4_4/S_{IN}$ $P4_5/S_{OUT}$ $P4_6/S_{CLK1}$ $P4_7/\overline{S_{RDY}}$				Serial I/O function I/O	Serial I/O control registers 1, 2 PULL register B	(6) (7) (8) (9)
$P5_0/TA_{OUT}$	Port P5	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Timer A output	Timer A mode register Timer A control reigster PULL register B	(10)
$P5_1$		Input	CMOS compatible input level			(11)
$P5_2/PWM_1$		Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	PWM output	Timer 56 mode register PULL register B	(4)
$P5_3/CNTR_0$ $P5_4/CNTR_1$				External count I/O	Interrupt edge selection register PULL register B	(12)
$P5_5/INT_0$ $P5_6/INT_1$ $P5_7/INT_2$				External interrupt input	Interrupt edge selection register PULL register B	(12)
$P6_0/AN_0$ – $P6_7/AN_7$	Port P6	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	A-D converter input	A-D control register PULL register B	(13)
$P7_0/X_{CIN}$	Port P7	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit I/O	CPU mode register PULL register A	(14)
$P7_1/X_{COUT}$						(15)
$P8_0$ – $P8_7$	Port P8	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt input	Interrupt control register 2 PULL register A	(17)
COM_0 – COM_3	Common	Output	LCD common output		LCD mode register	(16)

Notes 1: Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction.
When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.
2: For details of the functions of ports P0 to P3 in modes other than single-chip mode, and how to use double function ports as function I/O ports, refer to the applicable sections.

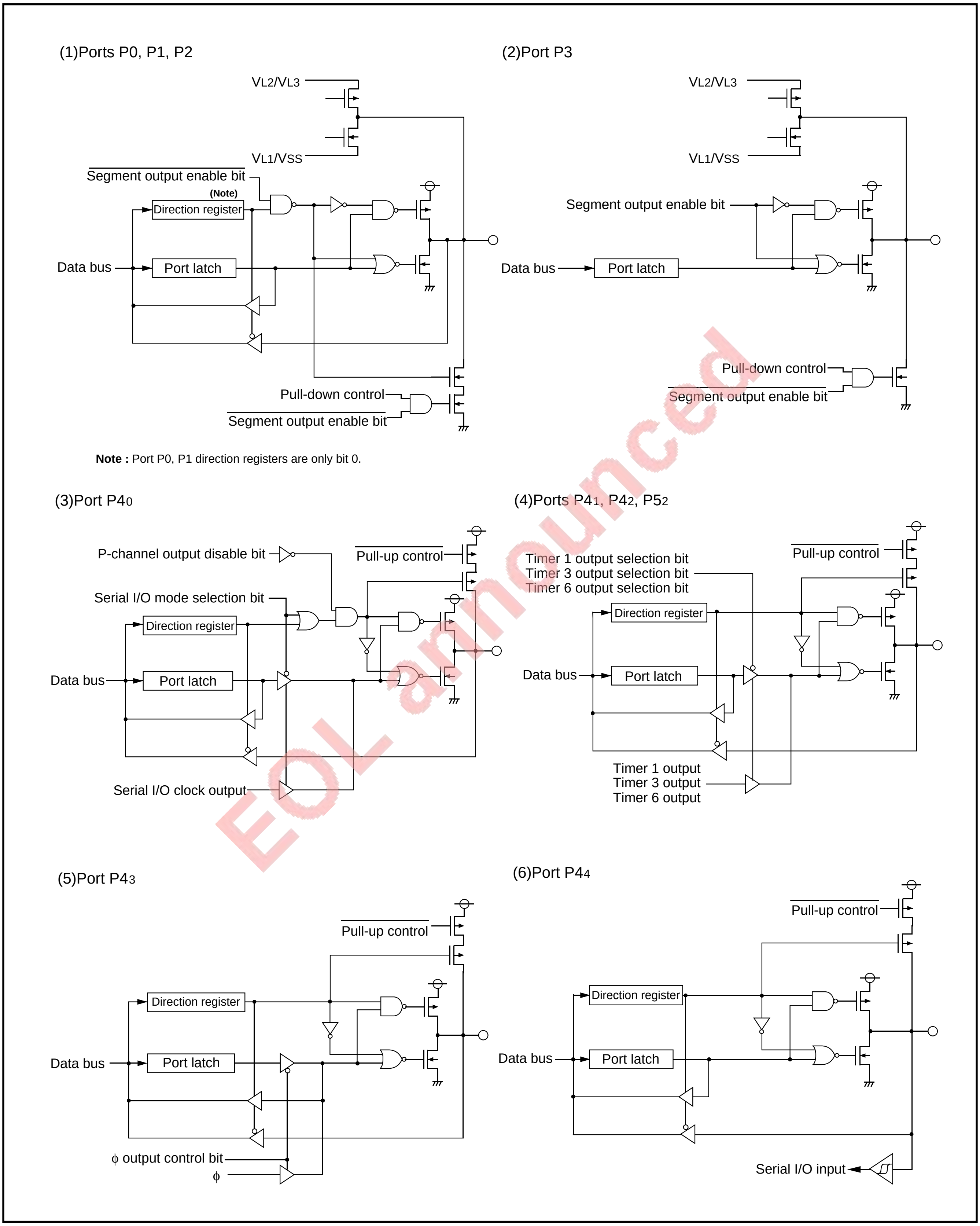


Fig. 10 Port block diagram (1)

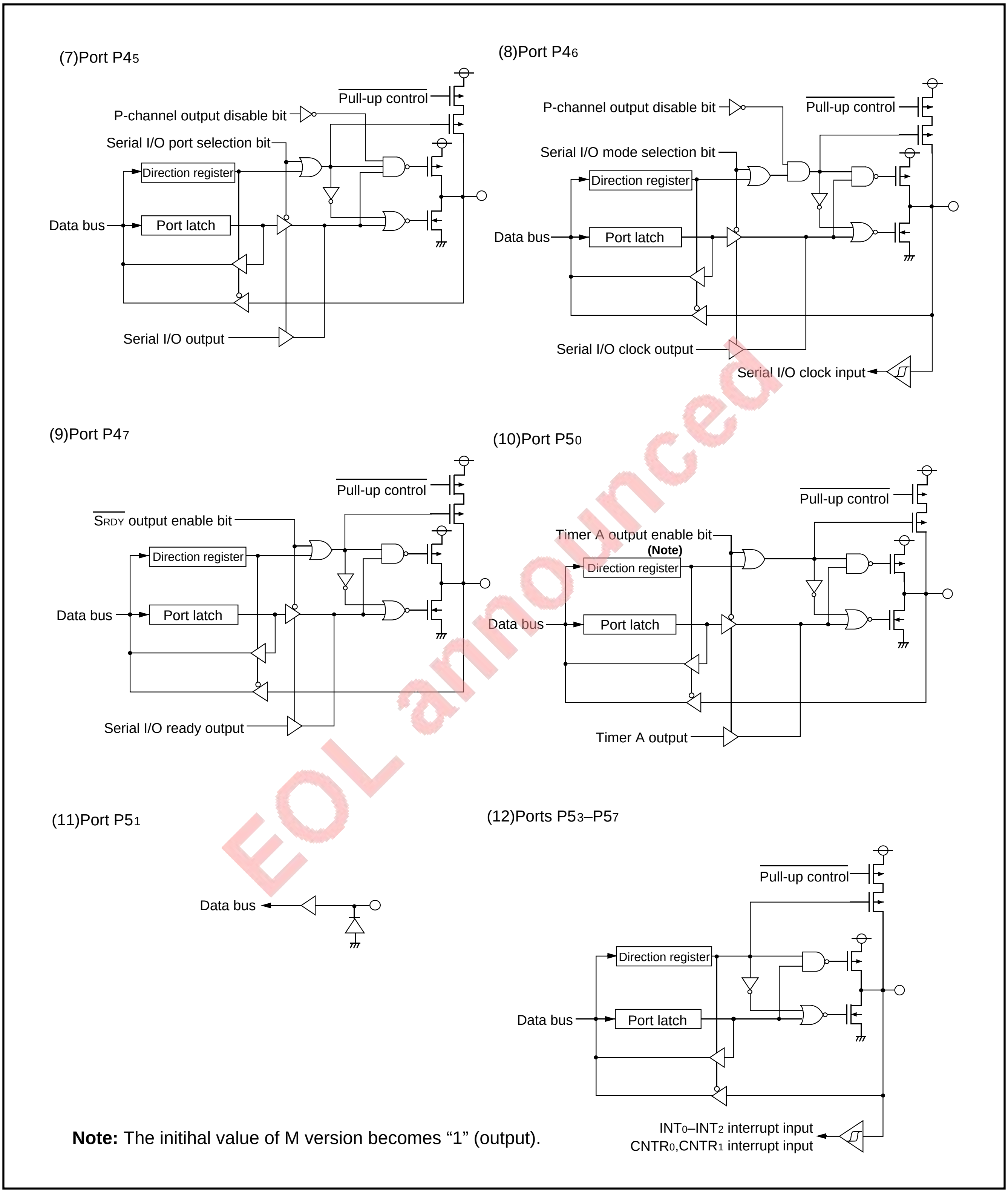


Fig. 11 Port block diagram (2)

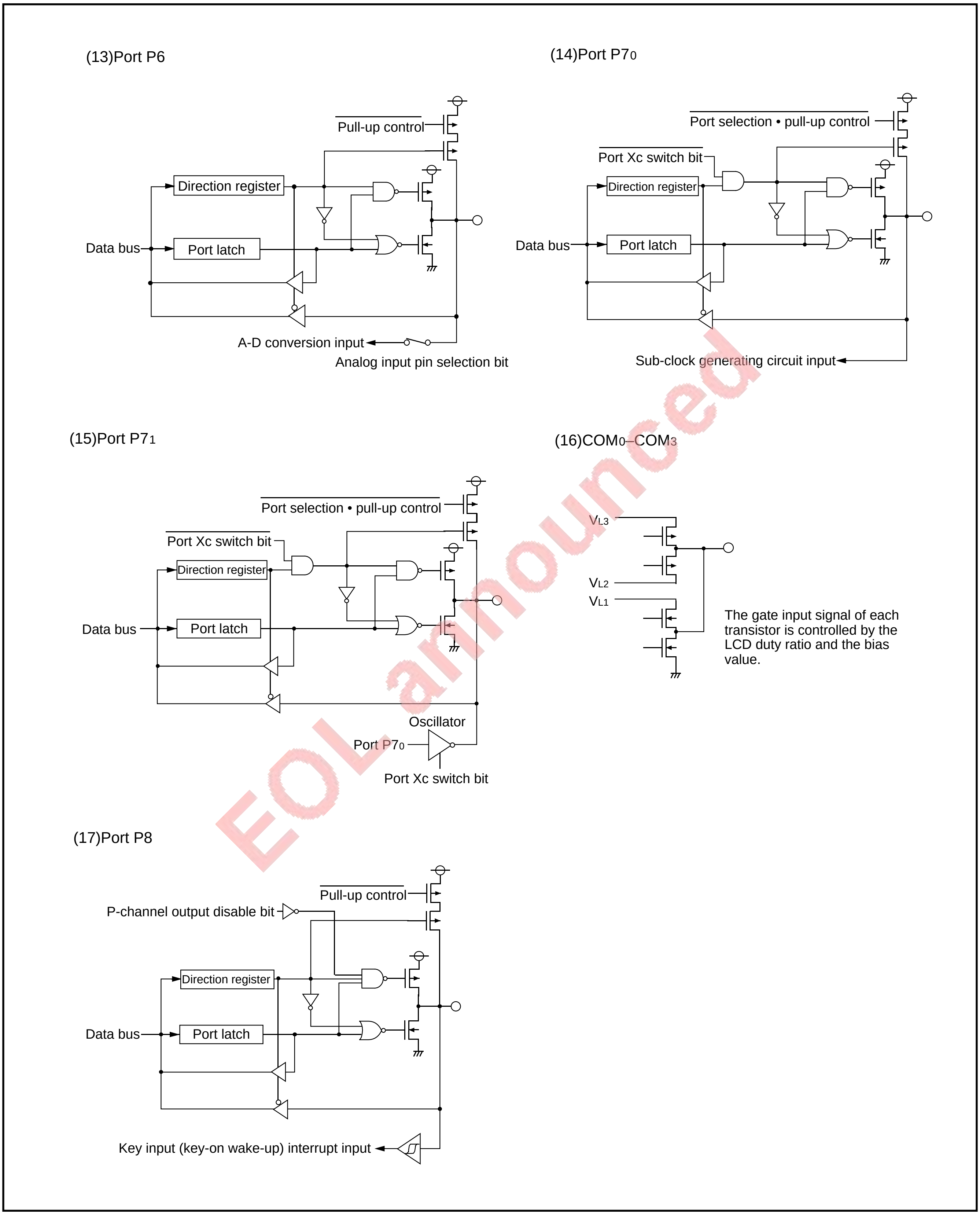


Fig. 12 Port block diagram (3)

INTERRUPTS

Interrupts occur by sixteen sources: six external, nine internal, and one software.

Interrupt Control

Each interrupt except the BRK instruction interrupt have both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.
Interrupt enable bits can be set or cleared by software. Interrupt request bits can be cleared by software, but cannot be set by software. The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupts requests occurs at the same time the interrupt with highest priority is accepted first.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. The interrupt jump destination address is read from the vector table into the program counter.

■Notes on Interrupts

When the active edge of an external interrupt (INT_0 – INT_2, $CNTR_0$ or $CNTR_1$) is set or an vector interrupt source where several interrupt source is assigned to the same vector address is switched, the corresponding interrupt request bit may also be set. Therefore, take following sequence:

(1) Disable the interrupt.
(2) Change the active edge in interrupt edge selection register.
(3) Clear the set interrupt request bit to “0.”
(4) Enable the interrupt.

Table 6 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset **(Note 2)**	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 intput	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
INT_2	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
Serial I/O	5	$FFF5_{16}$	$FFF4_{16}$	At completion of serial I/O data transmit/receive	Valid when serial I/O is selected
Timer A	6	$FFF3_{16}$	$FFF2_{16}$	At timer A underflow	
Timer 1	7	$FFF1_{16}$	$FFF0_{16}$	At timer 1 underflow	
Timer 2	8	$FFEF_{16}$	$FFEE_{16}$	At timer 2 underflow	STP release timer underflow
Timer 3	9	$FFED_{16}$	$FFEC_{16}$	At timer 3 underflow	
Timer 4	10	$FFEB_{16}$	$FFEA_{16}$	At timer 4 underflow	
Timer 5	11	$FFE9_{16}$	$FFE8_{16}$	At timer 5 underflow	
Timer 6	12	$FFE7_{16}$	$FFE6_{16}$	At timer 6 underflow	
$CNTR_0$	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Key input (Key-on wake-up)	15	$FFE1_{16}$	$FFE0_{16}$	At falling of port P8 (at input) input logical level AND	External interrupt (falling valid)
A-D conversion	16	$FFDF_{16}$	$FFDE_{16}$	At completion of A-D conversion	Valid when A-D conversion interrupt is selected
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

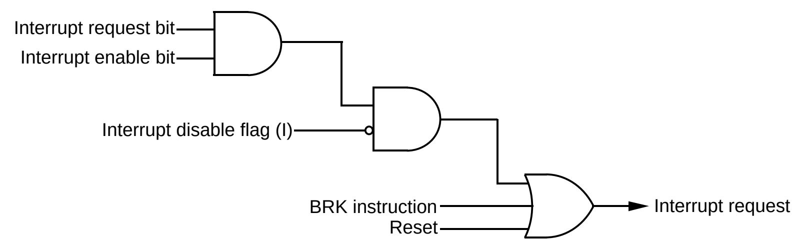


Fig. 13 Interrupt control

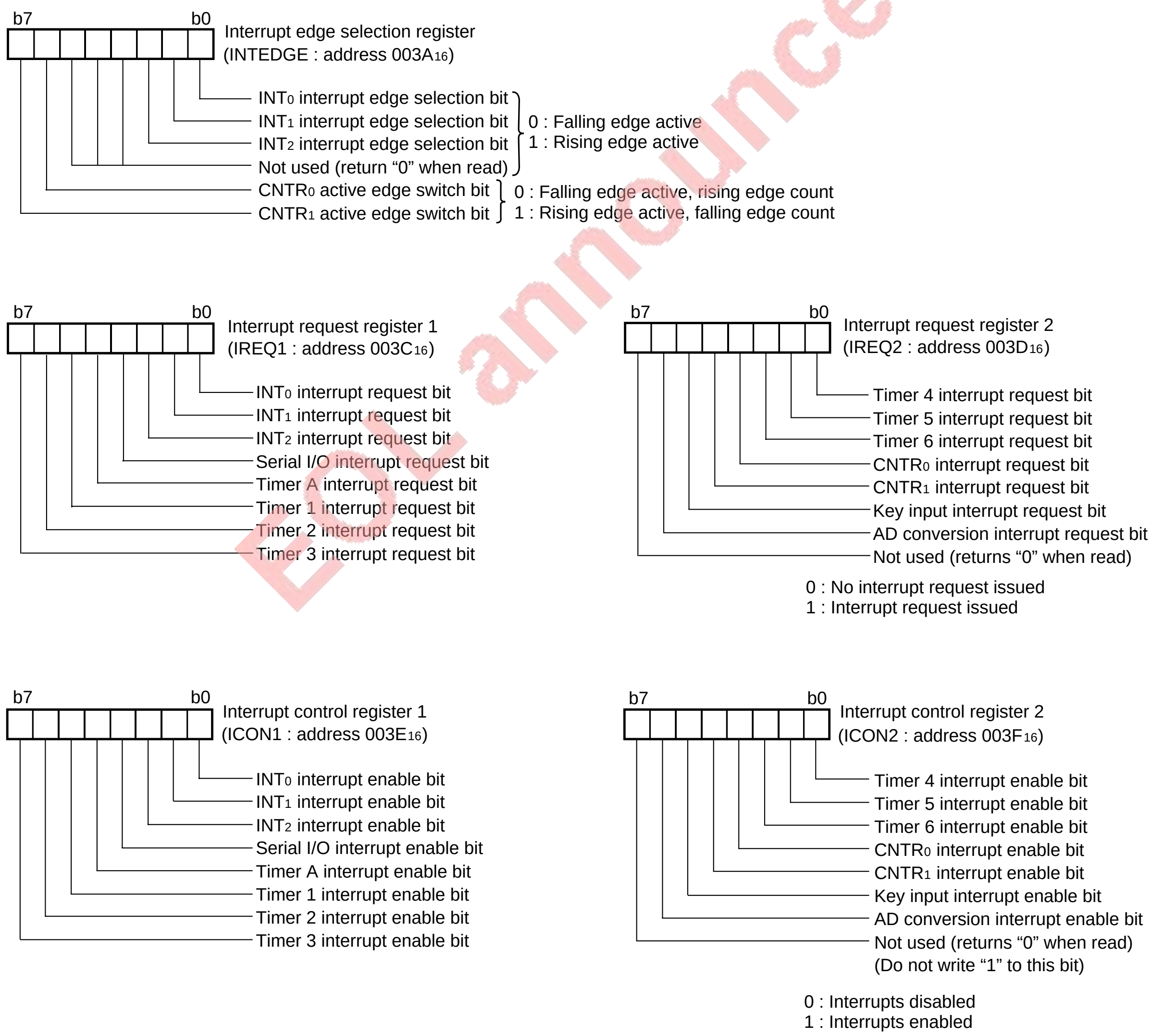


Fig. 14 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake-Up)

A key input interrupt request is generated by applying “L” level to any pin of port P8 that have been set to input mode. In other words, it is generated when AND of input level goes from “1” to “0”. An example of using a key input interrupt is shown in Figure 15, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports $P8_0$–$P8_3$.

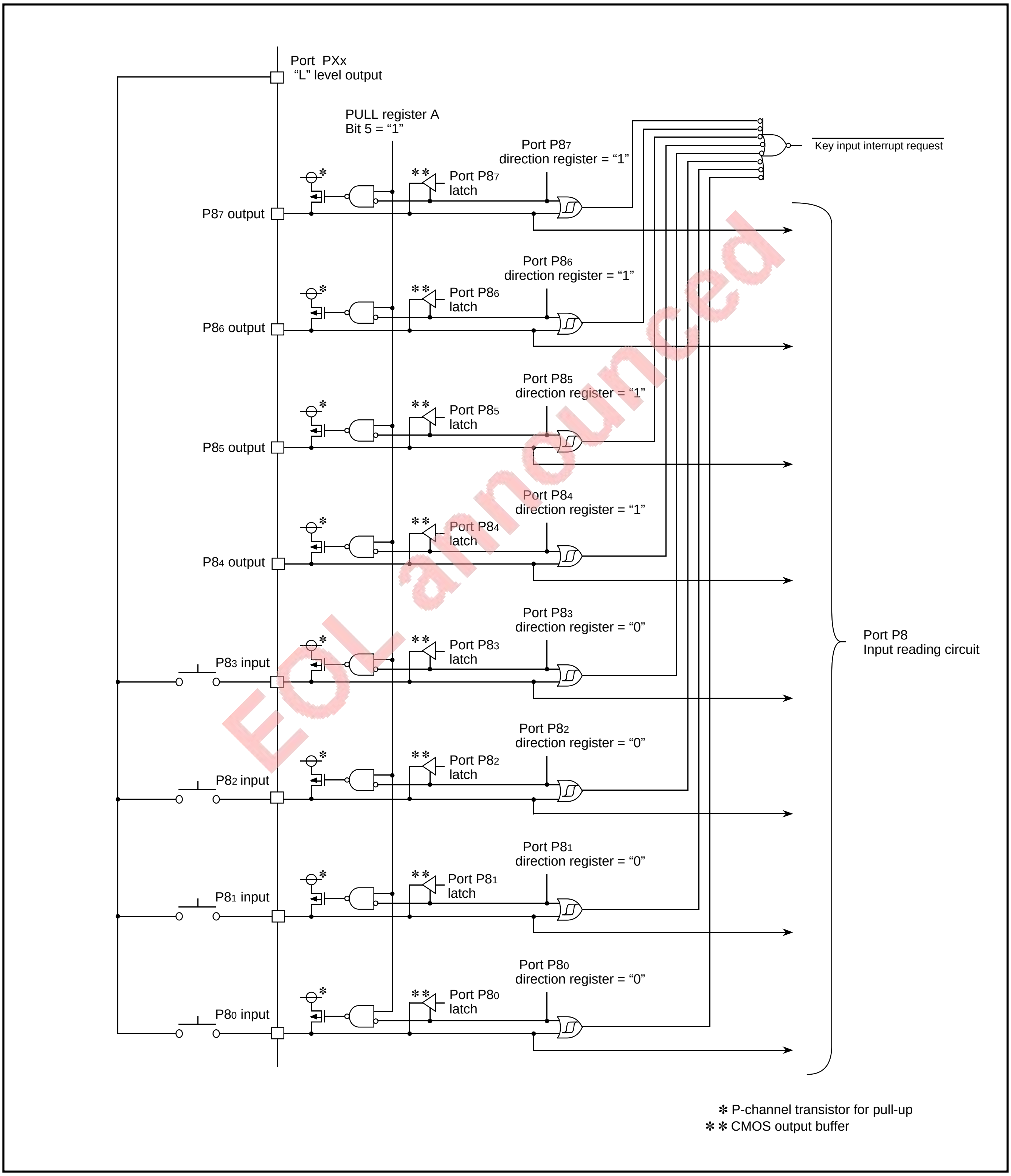


Fig. 15 Connection example when using key input interrupt and port P8 block diagram

TIMERS
8-Bit Timer

The 38C3 group has six built-in timers : Timer 1, Timer 2, Timer 3, Timer 4, Timer 5, and Timer 6.
Each timer has the 8-bit timer latch. All timers are down-counters. When the timer reaches "00_{16}," an underflow occurs with the next count pulse. Then the contents of the timer latch is reloaded into the timer and the timer continues down-counting. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1."
The count can be stopped by setting the stop bit of each timer to "1."
The system clock ϕ can be set to either the high-speed mode or low-speed mode with the CPU mode register. At the same time, timer internal count source is switched to either $f(X_{IN})$ or $f(X_{CIN})$.

●Timer 1, Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register. A rectangular waveform of timer 1 underflow signal divided by 2 is output from the $P4_1/T1_{OUT}$ pin. The waveform polarity changes each time timer 1 overflows. The active edge of the external clock $CNTR_0$ can be switched with the bit 6 of the interrupt edge selection register.
At reset or when executing the STP instruction, all bits of the timer 12 mode register are cleared to "0," timer 1 is set to "FF_{16}," and timer 2 is set to "01_{16}."

●Timer 3, Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. A rectangular waveform of timer 3 underflow signal divided by 2 is output from the $P4_2/T3_{OUT}$ pin. The waveform polarity changes each time timer 3 overflows. The active edge of the external clock $CNTR_1$ can be switched with the bit 7 of the interrupt edge selection register.

●Timer 5, Timer 6

The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register. A rectangular waveform of timer 6 underflow signal divided by 2 can be output from the $P5_2/PWM_1$ pin.

●Timer 6 PWM_1 Mode

Timer 6 can output a rectangular waveform with "H" duty cycle n/(n+m) from the $P5_2/PWM_1$ pin by setting the timer 56 mode register (refer to Figure 17). The n is the value set in timer 6 latch (address 0025_{16}) and m is the value in the timer 6 PWM register (address 0027_{16}). If n is "0," the PWM output is "L," if m is "0," the PWM output is "H" (n = 0 is prior than m = 0). In the PWM mode, interrupts occur at the rising edge of the PWM output.

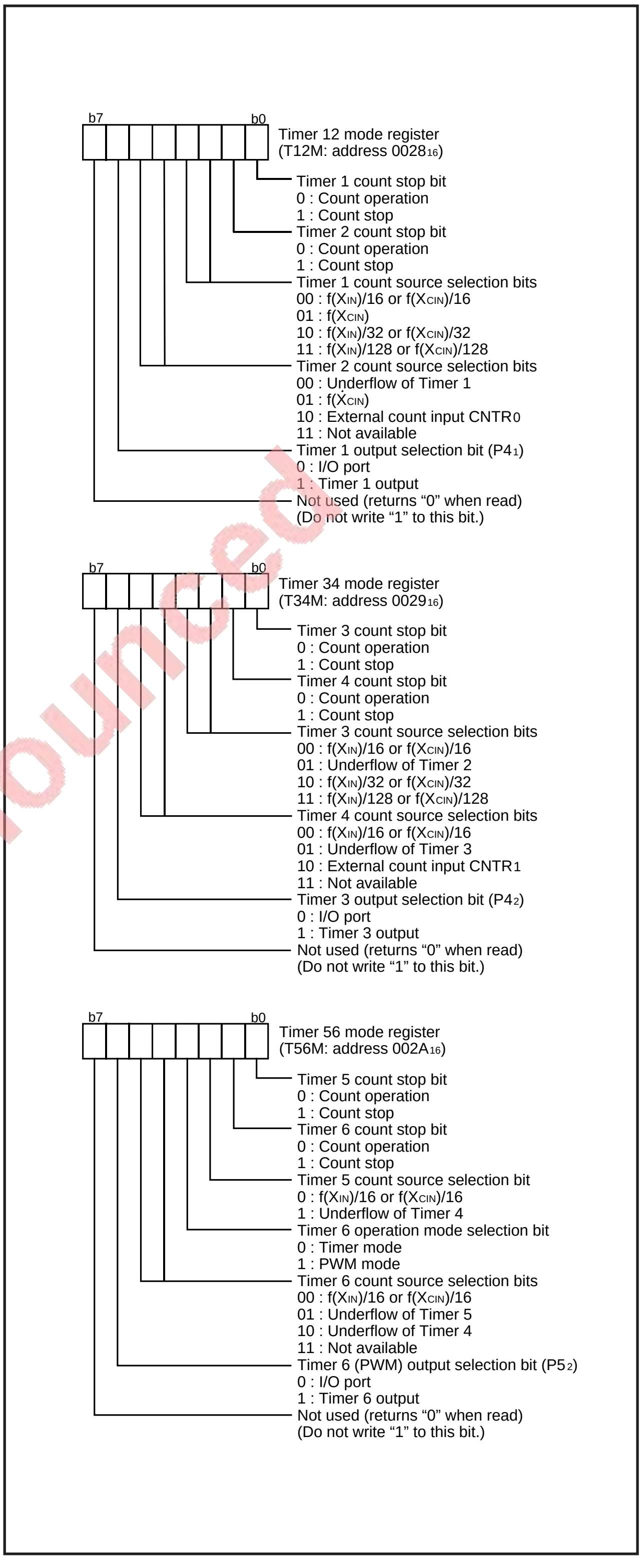


Fig. 16 Structure of Timer Related Register

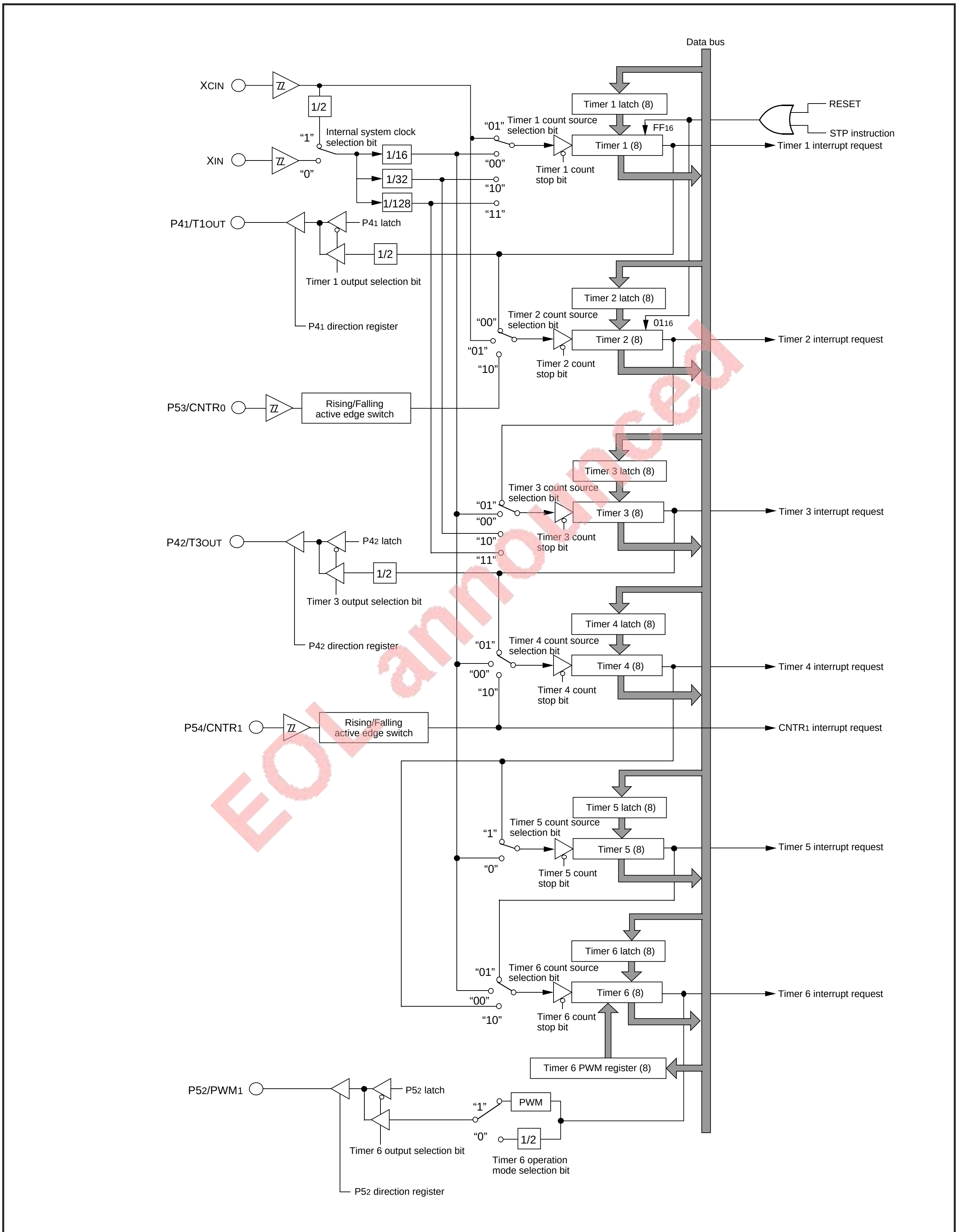


Fig. 17 Block diagram of timer

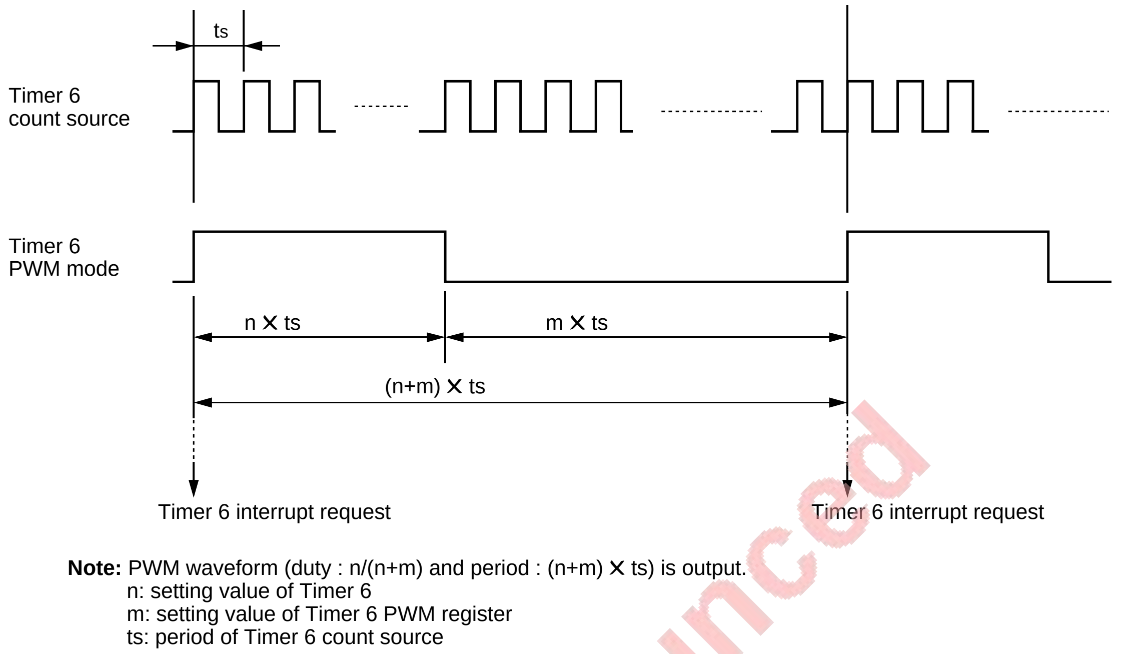


Fig. 18 Timing chart of timer 6 PWM1 mode

16-bit Timer

Timer A is a 16-bit timer that can be selected in one of four modes by the timer A mode register and the timer A control register.

●Timer A

The timer A operates as down-count. When the timer contents reach "0000_{16}", an underflow occurs at the next count pulse and the timer latch contents are reloaded. After that, the timer continues count-down. When the timer underflows, the interrupt request bit corresponding to the timer A is set to "1".

(1) Timer mode

The count source can be selected by setting the timer A mode register.

(2) Pulse output mode

Pulses of which polarity is inverted each time the timer underflows are output from the TA_{OUT} pin. Except for that, this mode operates just as in the timer mode.
When using this mode, set port $P5_0$ sharing the TA_{OUT} pin to output mode.

(3) IGBT output mode

After dummy output from the TA_{OUT} pin, count starts with the INT_0 pin input as a trigger. When the trigger is detected or the timer A underflows, "H" is output from the the TA_{OUT} pin.
When the count value corresponds with the compare register value, the TA_{OUT} output becomes "L". When the INT_0 signal becomes "H", the TA_{OUT} output is forced to become "L".
After noise is cleared by noise filters, judging continuous 4-time same levels with sampling clocks to be signals, the INT_0 signal can use 4 types of delay time by a delay circuit.
When using this mode, set port $P5_5$ sharing the INT_0 pin to input mode and set port $P5_0$ sharing the TA_{OUT} pin to output mode.
It is possible to force the timer A output to be "L" using pins INT_1 and INT_2 by the timer A control register.

(4) PWM mode

IGBT dummy output, an external trigger with the INT_0 pin and output control with pins INT_1 and INT_2 are not used. Except for those, this mode operates just as in the IGBT output mode.
The period of PWM waveform is specified by the timer A set value.
The "H" term is specified by the compare register set value.
When using this mode, set port $P5_0$ sharing the TA_{OUT} pin to output mode.

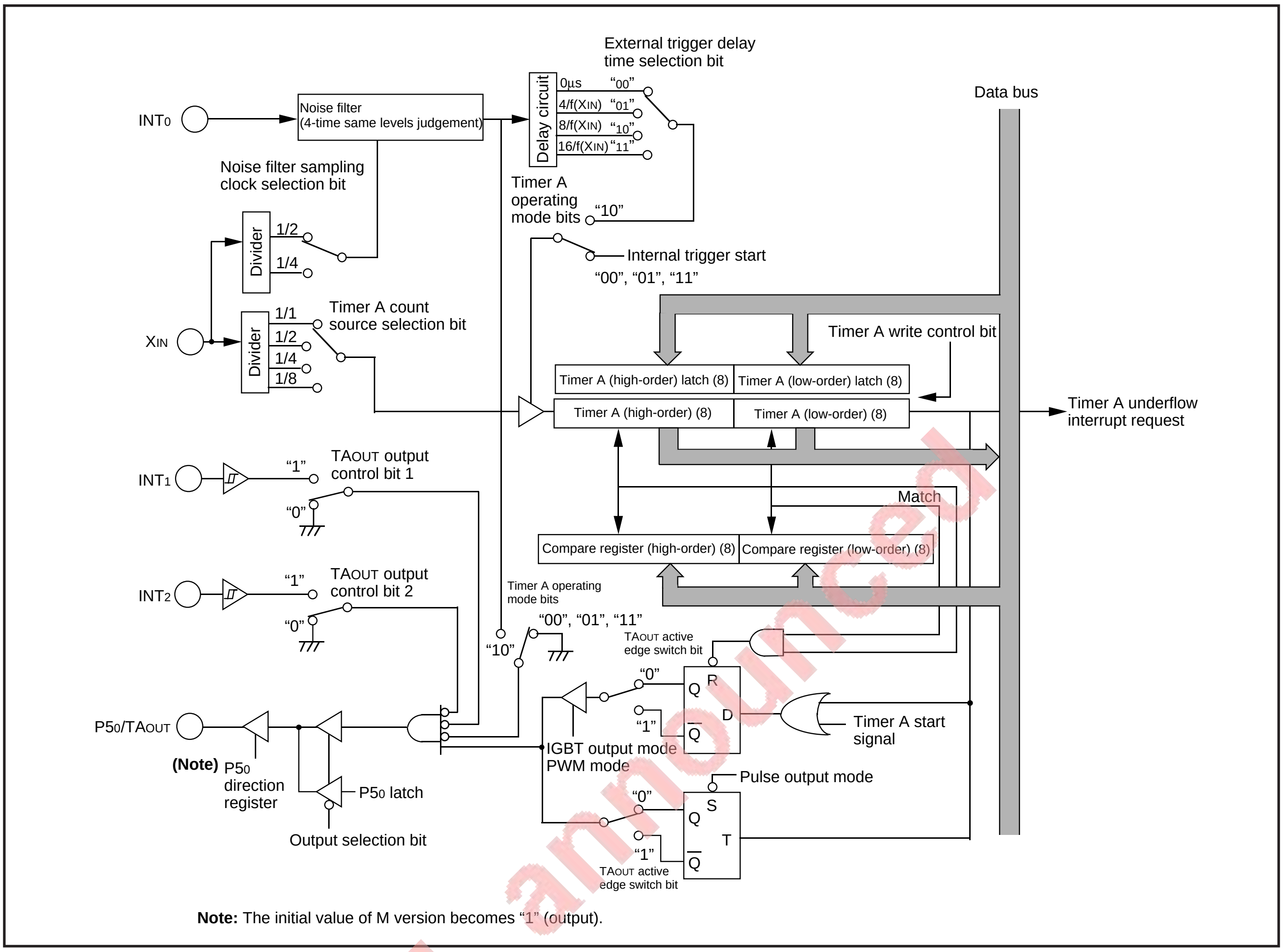


Fig. 19 Block diagram of timer A

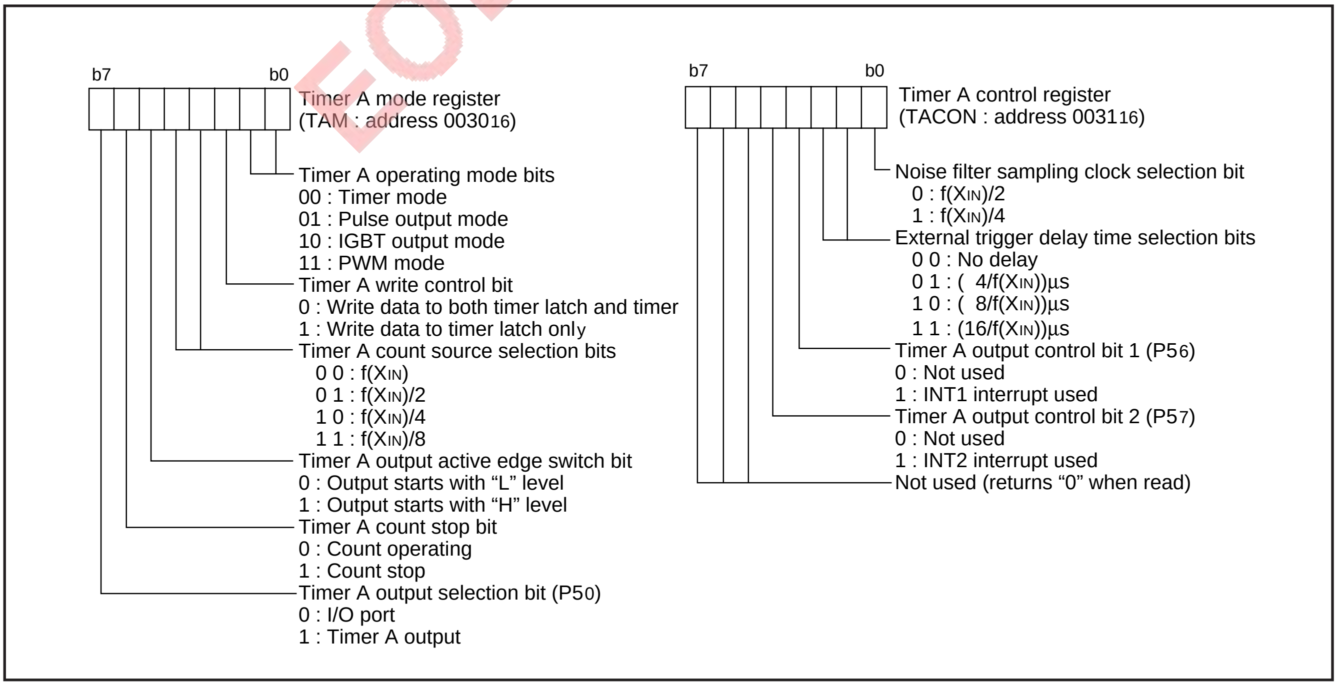


Fig. 20 Structure of timer A related registers

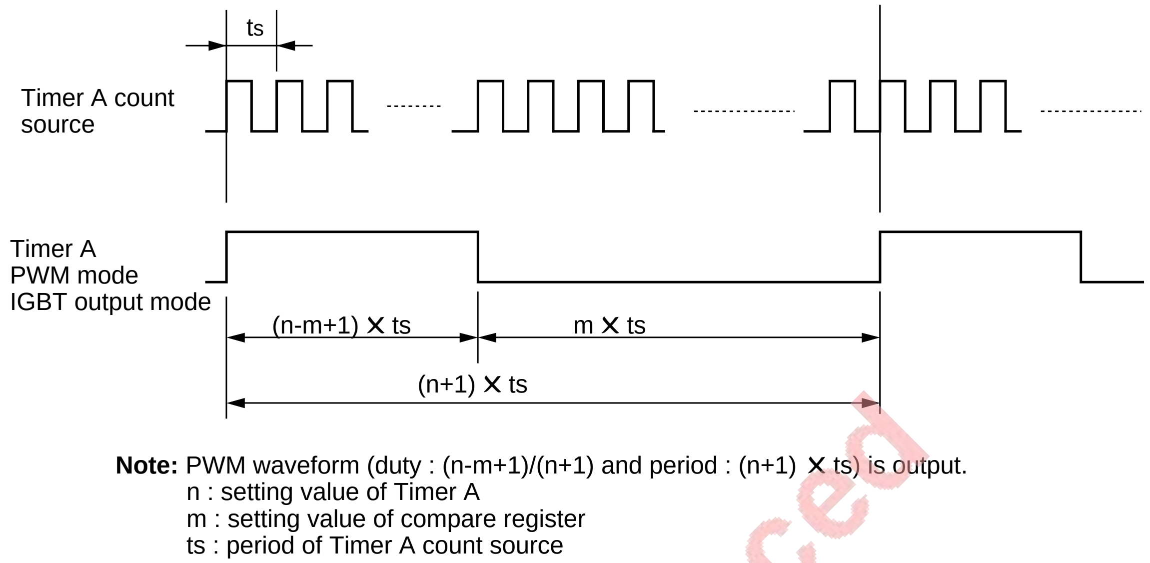


Fig. 21 Timing chart of timer A PWM, IGBT output modes

■Notes on Timer A

(1) Write order to timer A

- In the timer and pulse output modes, write to the timer A register (low-order) first and to the timer A register (high-order) next. Do not write to only one side.
- In the IGBT and PWM modes, write to the registers as follows:
  the compare register (high- and low-order)
  the timer A register (low-order)
  the timer A register (high-order).
  It is possible to use whichever order to write to the compare register (high- and low-order). However, write both the compare register and the timer A register at the same time.

(2) Read order to timer A

- In all modes, read to the timer A register (high-order) first and to the timer A register (low-order) next. Read order to the compare register is not specified.
- If reading to the timer A register during write operation or writing to it during read operation, normal operation will not be performed.

(3) Write to timer A

- When writing a value to the timer A address to write to the latch only, the value is set into the reload latch and the timer is updated at the next underflow. Normally, when writing a value to the timer A address, the value is set into the timer and the timer latch at the same time, because they are written at the same time.
  When writing to the latch only, if the write timing to the high-order reload latch and the underflow timing are almost the same, an expected value may be set in the high-order counter.
- Do not switch the timer count source during timer count operation. Stop the timer count before switching it. Additionally, when performing write to the latch and the timer at the same time, the timer count value may change large.

(4) Set of timer A mode register

Set the write control bit to “1” (write to the latch only) when setting the IGBT and PWM modes.
Output waveform simultaneously reflects the contents of both registers at the next underflow after writing to the timer A register (high-order).

(5) Output control function of timer A

When using the output control function (INT_1 and INT_2) in the IGBT mode, set the levels of INT_1 and INT_2 to “H” in the falling edge active or to “L” in the rising edge active before switching to the IGBT mode.

SERIAL I/O

The 38C3 group has a built-in 8-bit clock synchronous serial I/O. The I/O pins of serial I/O also operate as I/O port P4, and their function is selected by the serial I/O control register 1 (address 0019_{16}).

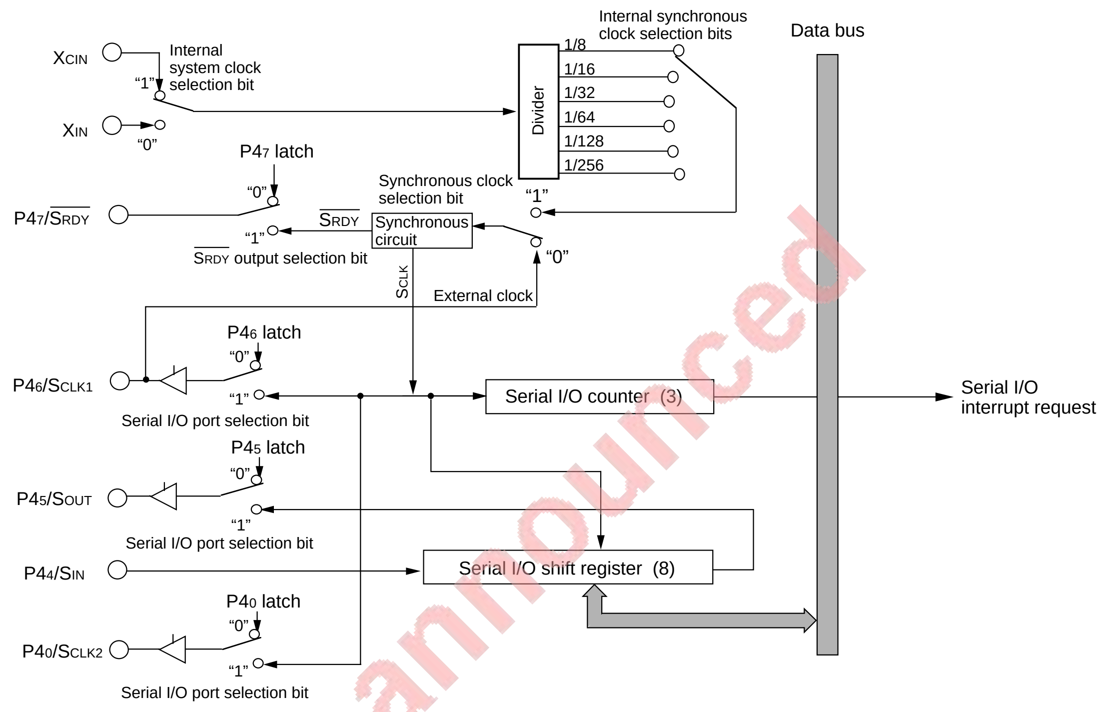


Fig. 22 Block diagram of serial I/O

[Serial I/O Control Registers 1, 2 (SIOCON1, SIOCON2)] 0019_{16}, $001A_{16}$

Each of the serial I/O control registers 1, 2 contains 8 bits that select various control parameters of serial I/O.

●Operation in serial I/O mode

Either an internal clock or an external clock can be selected as the synchronous clock for serial I/O transfer. A dedicated divider is built-in as the internal clock, giving a choice of six clocks.

When internal clock is selected, serial I/O starts to transfer by a write signal to the serial I/O register (address $001B_{16}$). After 8 bits have been transferred, the SOUT pin goes to high impedance.

When external clock is selected, the clock must be controlled externally because the contents of the serial I/O register continue to shift while the transfer clock is input. In this case, the SOUT pin does not go to high impedance at the completion of data transfer.

The interrupt request bit is set at the end of the transfer of 8 bits, regardless of whether the internal or external clock is selected.

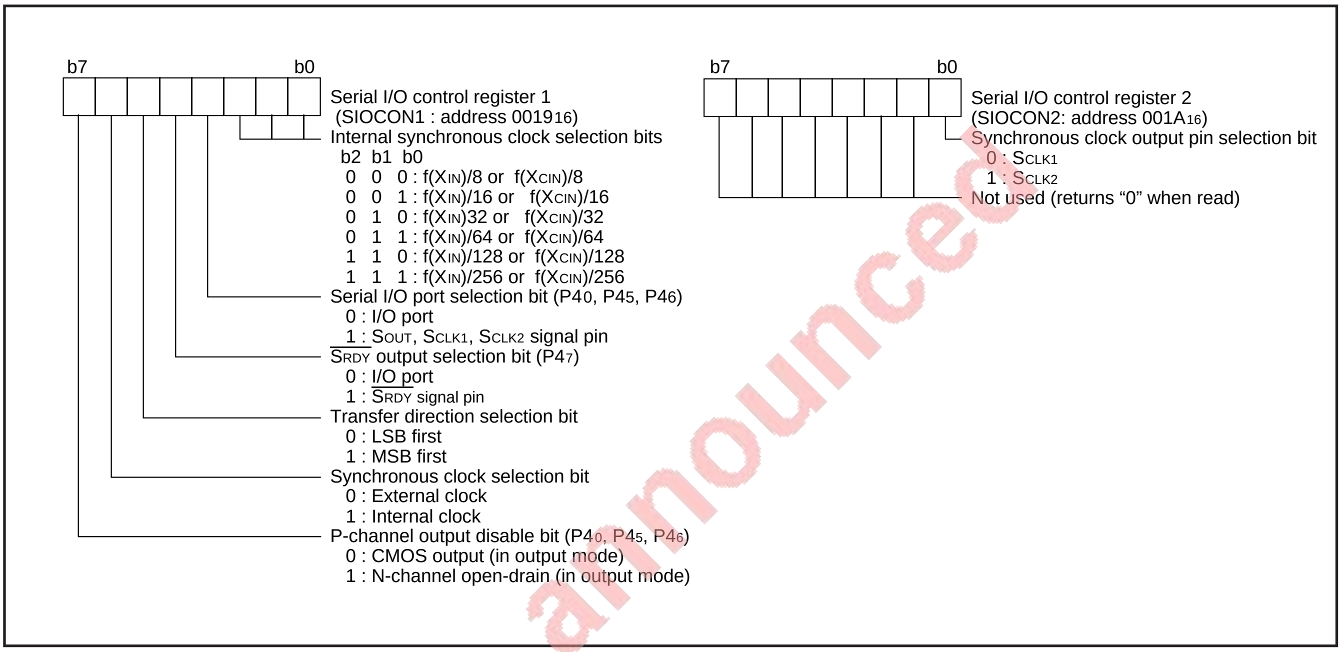


Fig. 23 Structure of serial I/O control register

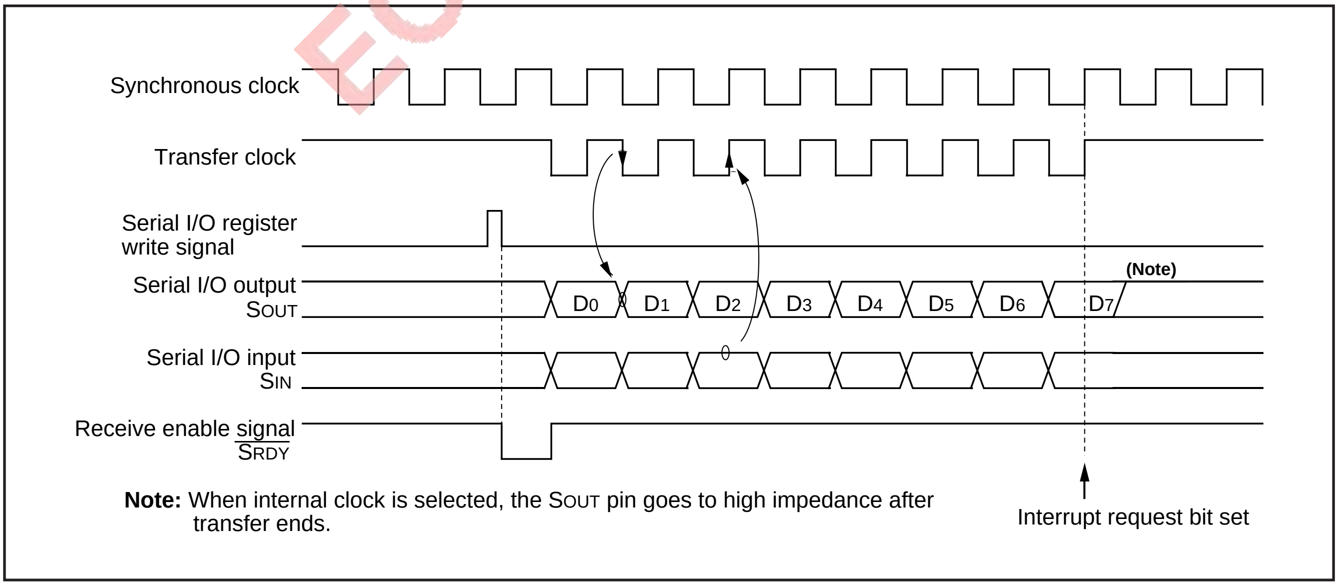


Fig. 24 Serial I/O timing (for LSB first)

A-D CONVERTER

The 38C3 group has a 10-bit A-D converter. The A-D converter performs successive approximation conversion.

[A-D Conversion Register (AD)] 0033_{16}, 0034_{16}

One of these registers is a high-order register, and the other is a low-order register. The high-order 8 bits of a conversion result is stored in the A-D conversion register (high-order) (address 0034_{16}), and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the A-D conversion register (low-order) (address 0033_{16}).
During A-D conversion, do not read these registers.

[A-D Control Register (ADCON)] 0032_{16}

This register controls A-D converter. Bits 2 to 0 are analog input pin selection bits. Bit 4 is an AD conversion completion bit and “0” during A-D conversion. This bit is set to “1” upon completion of A-D conversion.
A-D conversion is started by setting “0” in this bit.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF}, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports $P6_7/AN7$–$P6_0/AN0$ and inputs it to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to “1.”

Note that the comparator is constructed linked to a capacitor, so set $f(X_{IN})$ to at least 500 kHz during A-D conversion. Use a CPU system clock dividing the main clock X_{IN} as the internal system clock.

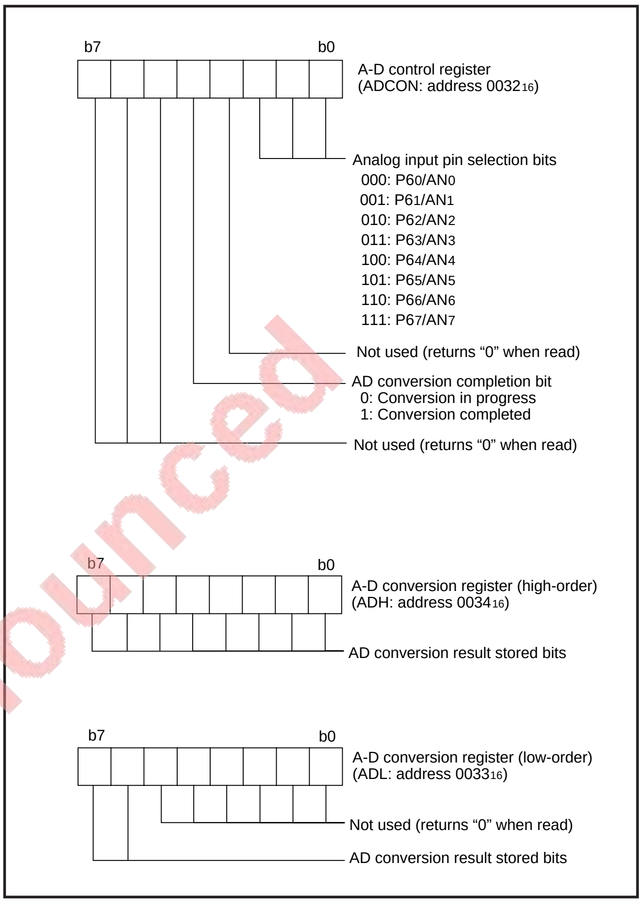


Fig. 25 Structure of A-D control register

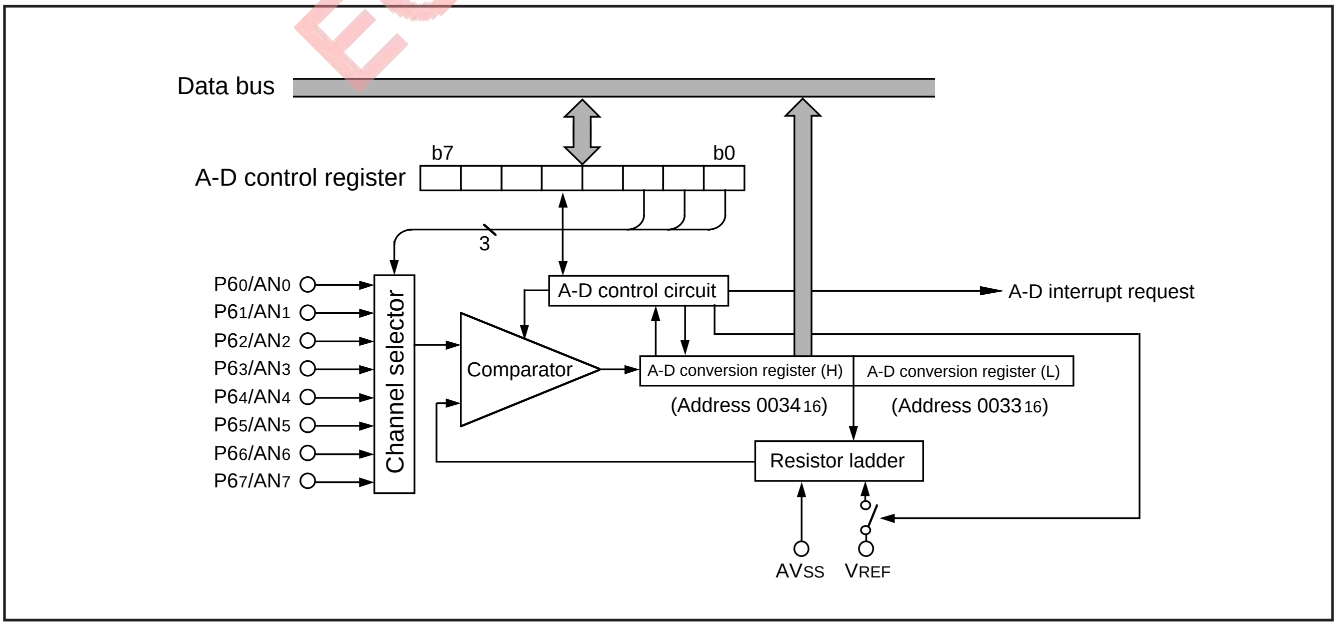


Fig. 26 Block diagram of A-D converter

LCD DRIVE CONTROL CIRCUIT

The 38C3 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

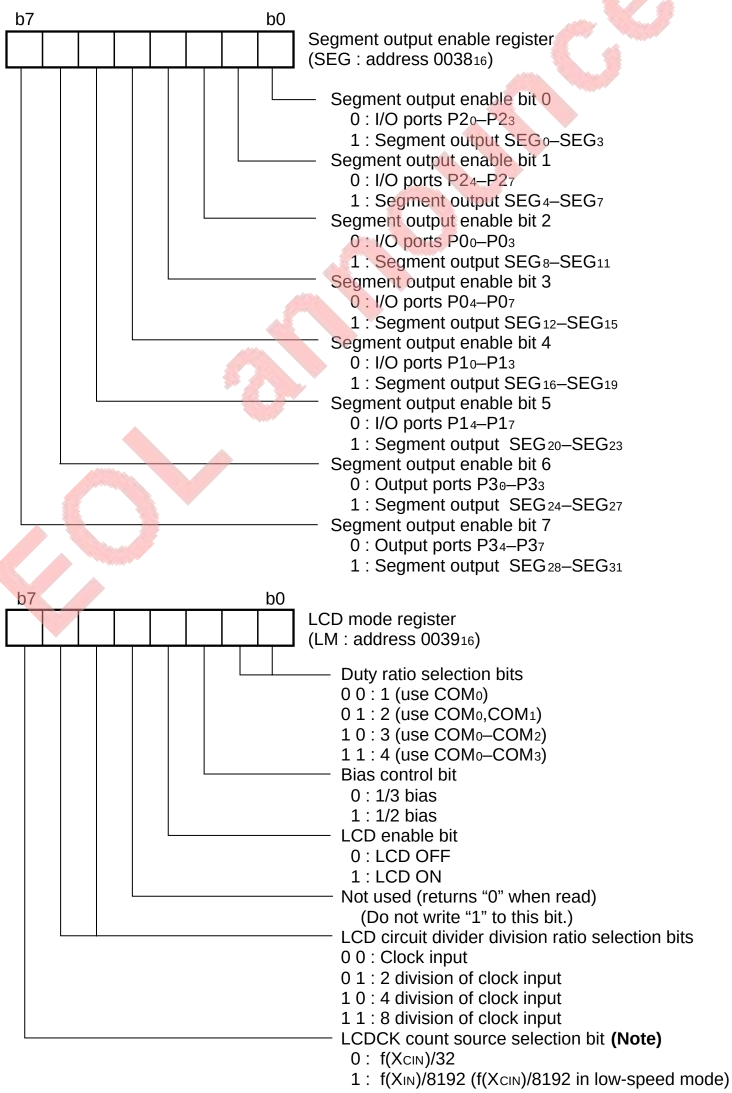
- LCD display RAM
- Segment output enable register
- LCD mode register
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 32 segment output pins and 4 common output pins can be used.

Up to 128 pixels can be controlled for a LCD display. When the LCD enable bit is set to “1” after data is set in the LCD mode register, the segment output enable register, and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 7 Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixels
1	32 dots or 8 segment LCD 4 digits
2	64 dots or 8 segment LCD 8 digits
3	96 dots or 8 segment LCD 12 digits
4	128 dots or 8 segment LCD 16 digits



Note : LCDCK is a clock for a LCD timing controller.

Fig. 27 Structure of LCD related registers

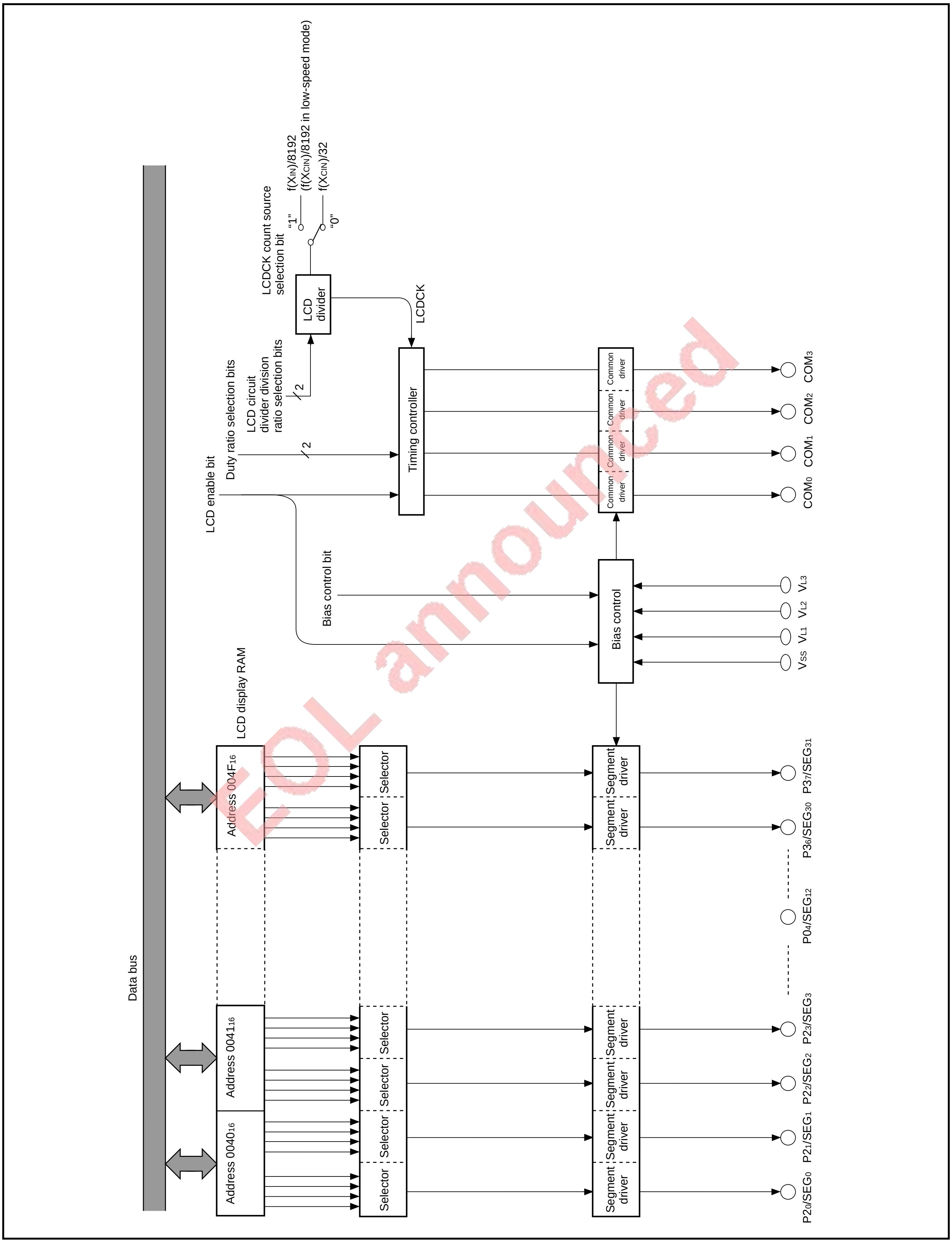


Fig. 28 Block diagram of LCD controller/driver

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (V_{L1}–V_{L3}), apply the voltage value shown in Table 8 according to the bias value.
Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Common Pin and Duty Ratio Control

The common pins (COM_0–COM_3) to be used are determined by duty ratio.
Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).
When selecting 1-duty ratio, 1/1 bias can be used.

Table 8 Bias control and applied voltage to V_{L1}–V_{L3}

Bias value	Voltage value
1/3 bias	$V_{L3}=V_{LCD}$ $V_{L2}=2/3\ V_{LCD}$ $V_{L1}=1/3\ V_{LCD}$
1/2 bias	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=1/2\ V_{LCD}$
1/1 bias (1-duty ratio)	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=V_{SS}$

Note 1: V_{LCD} is the maximum value of supplied voltage for the LCD panel.

Table 9 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bit		Common pins used
	Bit 1	Bit 0	
1	0	0	COM_0 **(Note 1)**
2	0	1	COM_0, COM_1 **(Note 2)**
3	1	0	COM_0–COM_2 **(Note 3)**
4	1	1	COM_0–COM_3

Notes 1: COM_1, COM_2, and COM_3 are open.
2: COM_2 and COM_3 are open.
3: COM_3 is open.

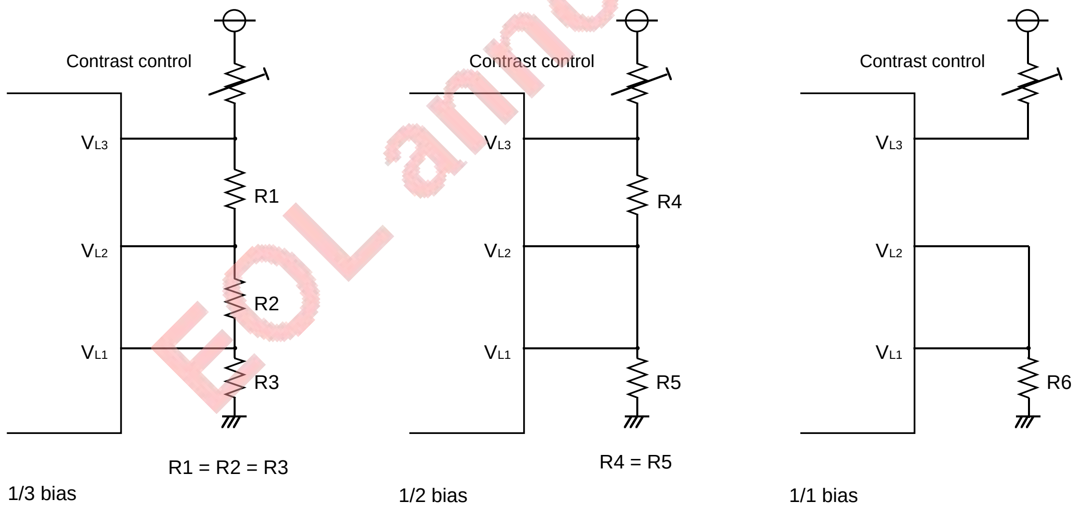


Fig. 29 Example of circuit at each bias

LCD Display RAM

Address 0040_{16} to $004F_{16}$ is the designated RAM for the LCD display. When “1” are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(LCDCK)=\frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency}=\frac{f(LCDCK)}{\text{duty ratio}}$$

Address \ Bit	7	6	5	4	3	2	1	0
0040_{16}	SEG_1				SEG_0			
0041_{16}	SEG_3				SEG_2			
0042_{16}	SEG_5				SEG_4			
0043_{16}	SEG_7				SEG_6			
0044_{16}	SEG_9				SEG_8			
0045_{16}	SEG_{11}				SEG_{10}			
0046_{16}	SEG_{13}				SEG_{12}			
0047_{16}	SEG_{15}				SEG_{14}			
0048_{16}	SEG_{17}				SEG_{16}			
0049_{16}	SEG_{19}				SEG_{18}			
$004A_{16}$	SEG_{21}				SEG_{20}			
$004B_{16}$	SEG_{23}				SEG_{22}			
$004C_{16}$	SEG_{25}				SEG_{24}			
$004D_{16}$	SEG_{27}				SEG_{26}			
$004E_{16}$	SEG_{29}				SEG_{28}			
$004F_{16}$	SEG_{31}				SEG_{30}			
	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0

Fig. 30 LCD display RAM map

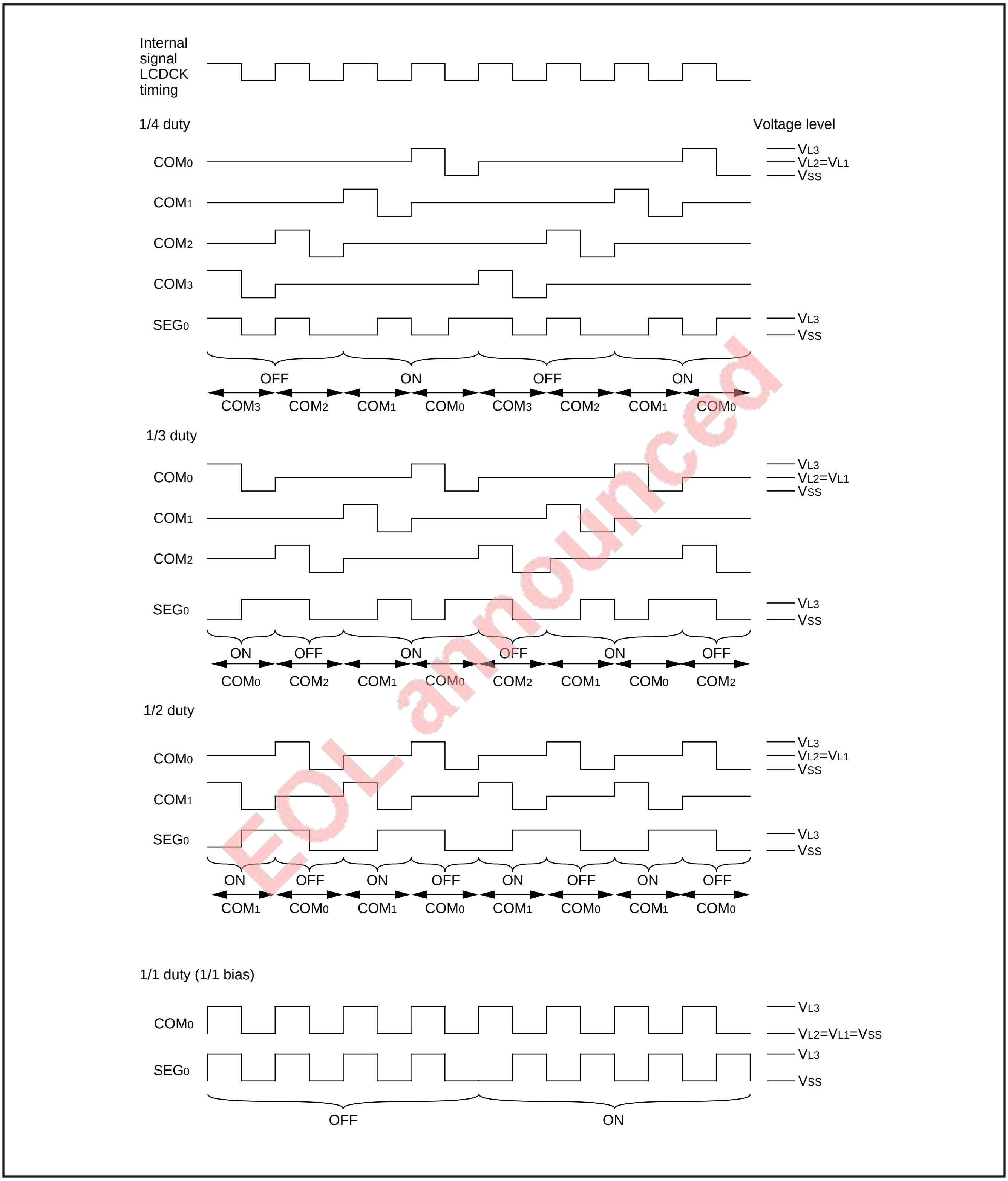


Fig. 31 LCD drive waveform (1/2 bias)

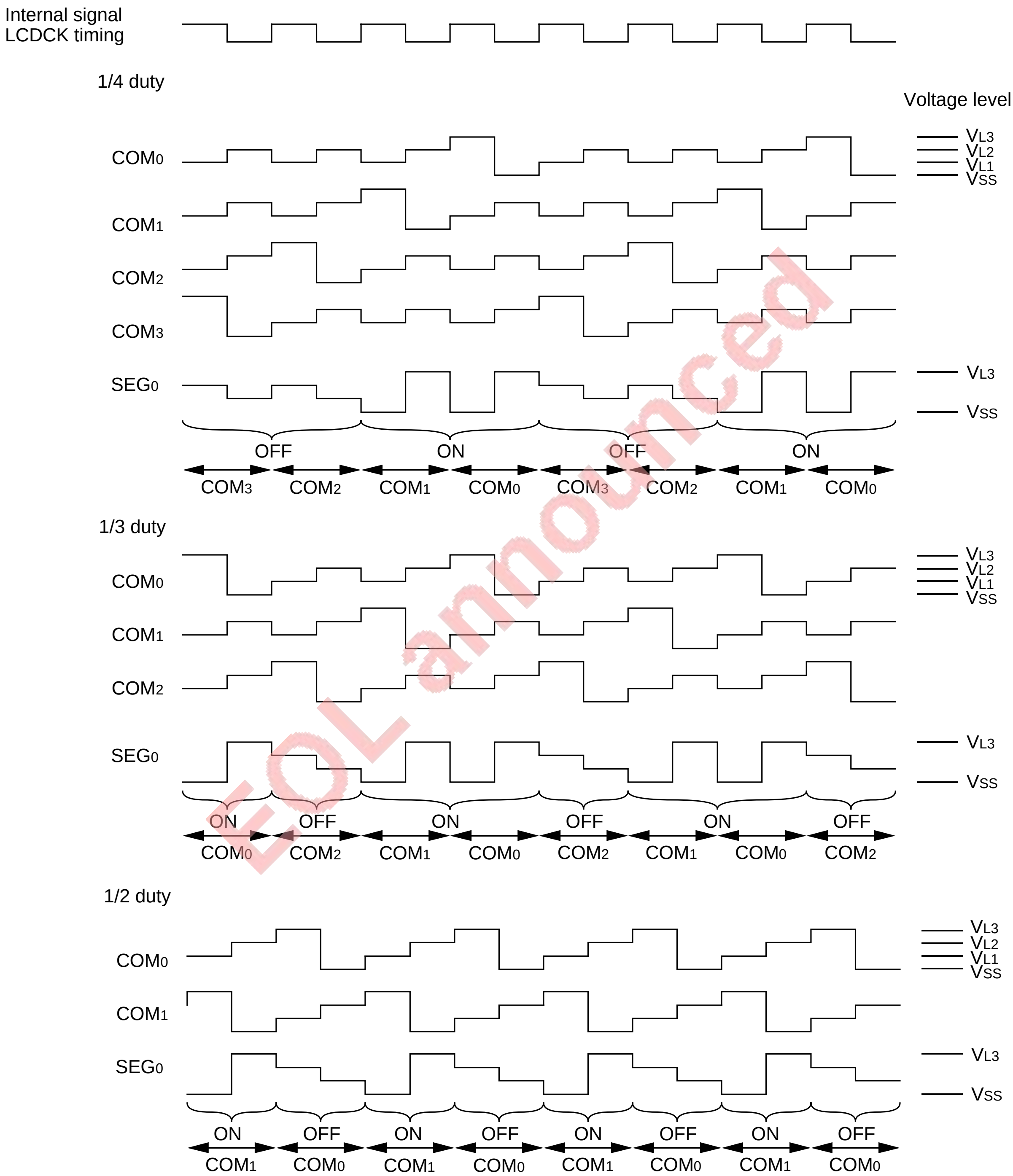


Fig. 32 LCD drive waveform (1/3 bias)

ϕ CLOCK OUTPUT FUNCTION

The internal system clock ϕ can be output from port $P4_3$ by setting the ϕ output control register. Set “1” to bit 3 of the port P4 direction register when outputting ϕ clock.

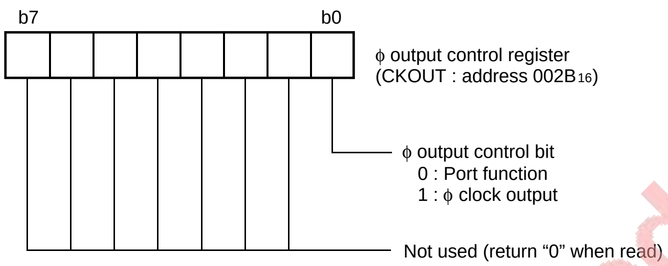


Fig. 33 Structure of ϕ output control register

ROM CORRECTION FUNCTION

The 38C3 group has the ROM correction function correcting data at the arbitrary addresses in the ROM area.

[ROM correct address register] $0F02_{16}$ – $0F11_{16}$

This is the register to store the address performing ROM correction. There are two types of registers to correct up to 8 addresses: one is the register to store the high-order address and the other is to store the low-order address.

[ROM correct enable register (RC1)] $0F01_{16}$

This is the register to enable the ROM correction function. When setting the bit corresponding to the ROM correction address to “1”, the ROM correction function is enabled.
It becomes invalid to the addresses of which corresponding bit is “0”.
All bits are “0” at the initial state.

[ROM correct data]

This is the register to store a correct data for the address specified by the ROM correct address register.

■Notes on ROM correction function

1. To use the ROM correction function, transfer data to each ROM correct data register in the initial setting.
2. Do not specify the same addresses in the ROM correct address register.

$0F02_{16}$	ROM correct high-order address register 1
$0F03_{16}$	ROM correct low-order address register 1
$0F04_{16}$	ROM correct high-order address register 2
$0F05_{16}$	ROM correct low-order address register 2
$0F06_{16}$	ROM correct high-order address register 3
$0F07_{16}$	ROM correct low-order address register 3
$0F08_{16}$	ROM correct high-order address register 4
$0F09_{16}$	ROM correct low-order address register 4
$0F0A_{16}$	ROM correct high-order address register 5
$0F0B_{16}$	ROM correct low-order address register 5
$0F0C_{16}$	ROM correct high-order address register 6
$0F0D_{16}$	ROM correct low-order address register 6
$0F0E_{16}$	ROM correct high-order address register 7
$0F0F_{16}$	ROM correct low-order address register 7
$0F10_{16}$	ROM correct high-order address register 8
$0F11_{16}$	ROM correct low-order address register 8

Fig. 34 Structure of ROM correct address register

0050_{16}	ROM correct data 1
0051_{16}	ROM correct data 2
0052_{16}	ROM correct data 3
0053_{16}	ROM correct data 4
0054_{16}	ROM correct data 5
0055_{16}	ROM correct data 6
0056_{16}	ROM correct data 7
0057_{16}	ROM correct data 8

Fig. 35 Structure of ROM correct data

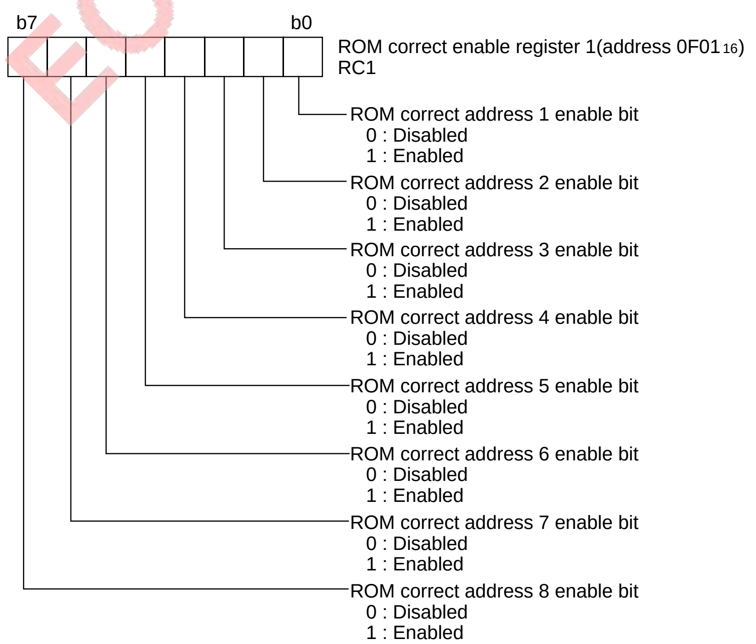


Fig. 36 Structure of ROM correct enable register 1

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage should be between 2.5 V and 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage is less than 0.5 V for V_{CC} of 2.5 V (switching to the high-speed mode, a power source voltage must be between 4.0 V and 5.5 V).

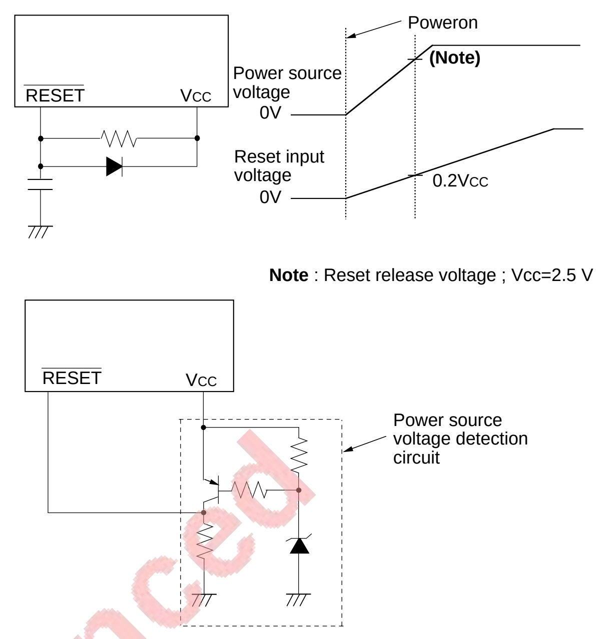
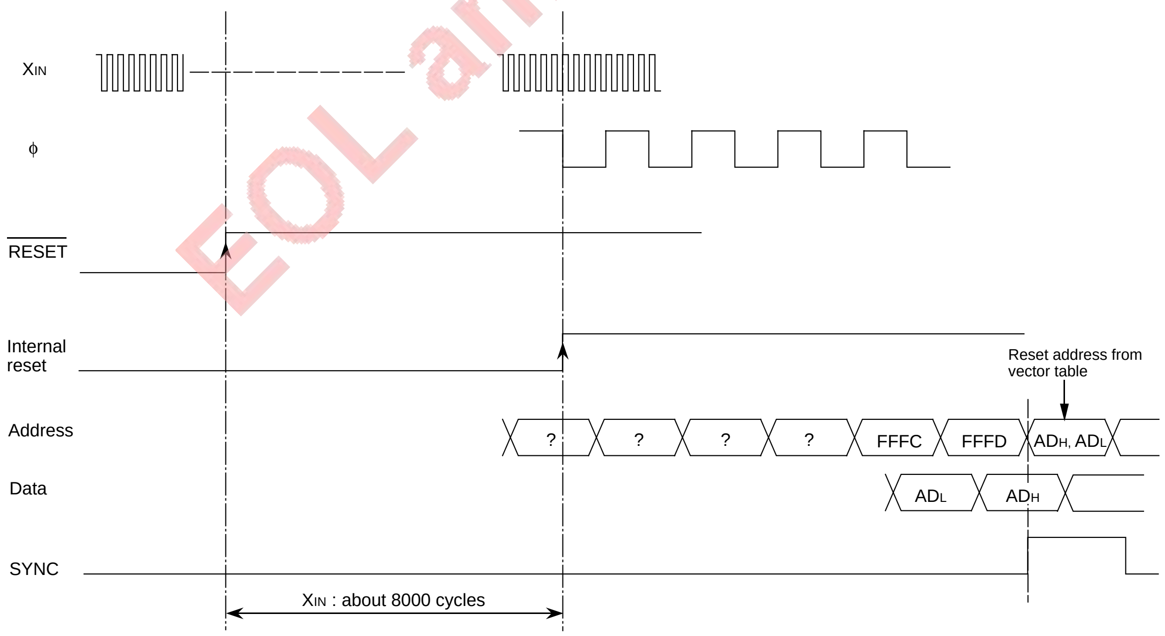


Fig. 37 Reset circuit example



Note 1: The frequency relation of $f(X_{IN})$ and $f(\phi)$ is $f(X_{IN}) = 8 \cdot f(\phi)$.
2: The question marks (?) indicate an undefined state that depends on the previous state.

Fig. 38 Reset sequence

No.	Register	Address	Register contents
(1)	Port P0	0000_{16}	00_{16}
(2)	Port P0 direction register	0001_{16}	00_{16}
(3)	Port P1	0002_{16}	00_{16}
(4)	Port P1 direction register	0003_{16}	00_{16}
(5)	Port P2	0004_{16}	00_{16}
(6)	Port P2 direction register	0005_{16}	00_{16}
(7)	Port P3	0006_{16}	00_{16}
(8)	Port P4	0008_{16}	00_{16}
(9)	Port P4 direction register	0009_{16}	00_{16}
(10)	Port P5	$000A_{16}$	00_{16}
(11)	Port P5 direction register	$000B_{16}$	00_{16}
(12)	Port P6	$000C_{16}$	00_{16}
(13)	Port P6 direction register	$000D_{16}$	00_{16}
(14)	Port P7	$000E_{16}$	00_{16}
(15)	Port P7 direction register	$000F_{16}$	00_{16}
(16)	Port P8	0010_{16}	00_{16}
(17)	Port P8 direction register	0011_{16}	00_{16}
(18)	PULL register A	0016_{16}	$0F_{16}$
(19)	PULL register B	0017_{16}	00_{16}
(20)	Port P8 output selection register	0018_{16}	00_{16}
(21)	Serial I/O control register 1	0019_{16}	00_{16}
(22)	Serial I/O control register 2	$001A_{16}$	00_{16}
(23)	Timer 1	0020_{16}	FF_{16}
(24)	Timer 2	0021_{16}	01_{16}
(25)	Timer 3	0022_{16}	FF_{16}
(26)	Timer 4	0023_{16}	FF_{16}
(27)	Timer 5	0024_{16}	FF_{16}
(28)	Timer 6	0025_{16}	FF_{16}
(29)	Timer 12 mode register	0028_{16}	00_{16}
(30)	Timer 34 mode register	0029_{16}	00_{16}
(31)	Timer 56 mode register	$002A_{16}$	00_{16}
(32)	ϕ output control register	$002B_{16}$	00_{16}
(33)	Timer A (low-order)	$002C_{16}$	FF_{16}
(34)	Timer A (high-order)	$002D_{16}$	FF_{16}
(35)	Compare register (low-order)	$002E_{16}$	00_{16}
(36)	Compare register (high-order)	$002F_{16}$	00_{16}
(37)	Timer A mode register	0030_{16}	00_{16}
(38)	Timer A control register	0031_{16}	00_{16}
(39)	A-D control register	0032_{16}	10_{16}
(40)	Segment output enable register	0038_{16}	00_{16}
(41)	LCD mode register	0039_{16}	00_{16}
(42)	Interrupt edge selection register	$003A_{16}$	00_{16}
(43)	CPU mode register	$003B_{16}$	0 1 0 0 1 0 0 0
(44)	Interrupt request register 1	$003C_{16}$	00_{16}
(45)	Interrupt request register 2	$003D_{16}$	00_{16}
(46)	Interrupt control register 1	$003E_{16}$	00_{16}
(47)	Interrupt control register 2	$003F_{16}$	00_{16}
(48)	ROM correct enable register 1	$0F01_{16}$	00_{16}
(49)	ROM correct high-order address register 1	$0F02_{16}$	FF_{16}
(50)	ROM correct low-order address register 1	$0F03_{16}$	FF_{16}
(51)	ROM correct high-order address register 2	$0F04_{16}$	FF_{16}
(52)	ROM correct low-order address register 2	$0F05_{16}$	FF_{16}
(53)	ROM correct high-order address register 3	$0F06_{16}$	FF_{16}
(54)	ROM correct low-order address register 3	$0F07_{16}$	FF_{16}
(55)	ROM correct high-order address register 4	$0F08_{16}$	FF_{16}
(56)	ROM correct low-order address register 4	$0F09_{16}$	FF_{16}
(57)	ROM correct high-order address register 5	$0F0A_{16}$	FF_{16}
(58)	ROM correct low-order address register 5	$0F0B_{16}$	FF_{16}
(59)	ROM correct high-order address register 6	$0F0C_{16}$	FF_{16}
(60)	ROM correct low-order address register 6	$0F0D_{16}$	FF_{16}
(61)	ROM correct high-order address register 7	$0F0E_{16}$	FF_{16}
(62)	ROM correct low-order address register 7	$0F0F_{16}$	FF_{16}
(63)	ROM correct high-order address register 8	$0F10_{16}$	FF_{16}
(64)	ROM correct low-order address register 8	$0F11_{16}$	FF_{16}
(65)	Processor status register	(PS)	X X X X X 1 X X
(66)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

X: Not fixed
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.
In the M version, bit 0 of the port P5 direction register becomes "1."

Fig. 39 Internal status at reset

CLOCK GENERATING CIRCUIT

The 38C3 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT} (X_{CIN} and X_{COUT}). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between X_{IN} and X_{OUT} since a feedback resistor exists on-chip. However, an external feedback resistor is needed between X_{CIN} and X_{COUT}.
Immediately after power on, only the X_{IN} oscillation circuit starts oscillating, and X_{CIN} and X_{COUT} pins function as I/O ports.

Frequency control
(1) Middle-speed mode

The internal system clock is the frequency of X_{IN} divided by 8. After reset, this mode is selected.

(2) High-speed mode

The internal system clock is the frequency of X_{IN} divided by 2.

(3) Low-speed mode

The internal system clock is the frequency of X_{CIN} divided by 2.

■Notes on clock generating circuit

If you switch the mode between middle/high-speed and low-speed, stabilize both X_{IN} and X_{CIN} oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that $f(X_{IN}) > 3f(X_{CIN})$.

Oscillation control
(1) Stop mode

If the STP instruction is executed, the internal system clock stops at an “H” level, and X_{IN} and X_{CIN} oscillators stop. Timer 1 is set to “FF_{16}” and timer 2 is set to “01_{16}.”
Either X_{IN} divided by 16 or X_{CIN} divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2. The bits of the timer 12 mode register are cleared to “0.” Set the interrupt enable bits of the timer 1 and timer 2 to disabled (“0”) before executing the STP instruction. Oscillator restarts when an external interrupt is received, but the internal system clock is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait mode

If the WIT instruction is executed, the internal system clock stops at an “H” level. The states of X_{IN} and X_{CIN} are the same as the state before executing the WIT instruction. The internal system clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

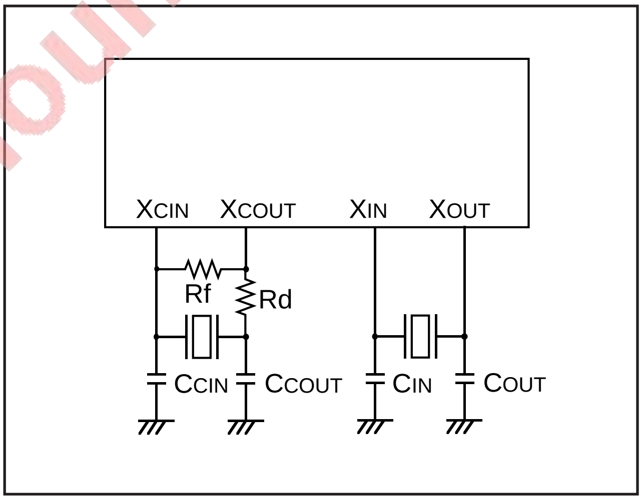


Fig. 40 Ceramic resonator circuit

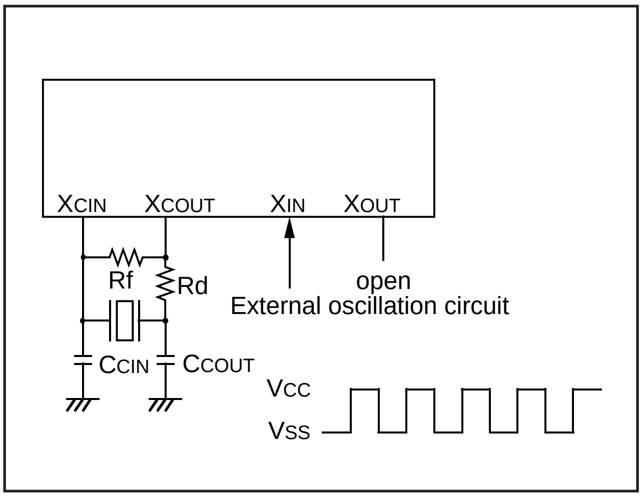
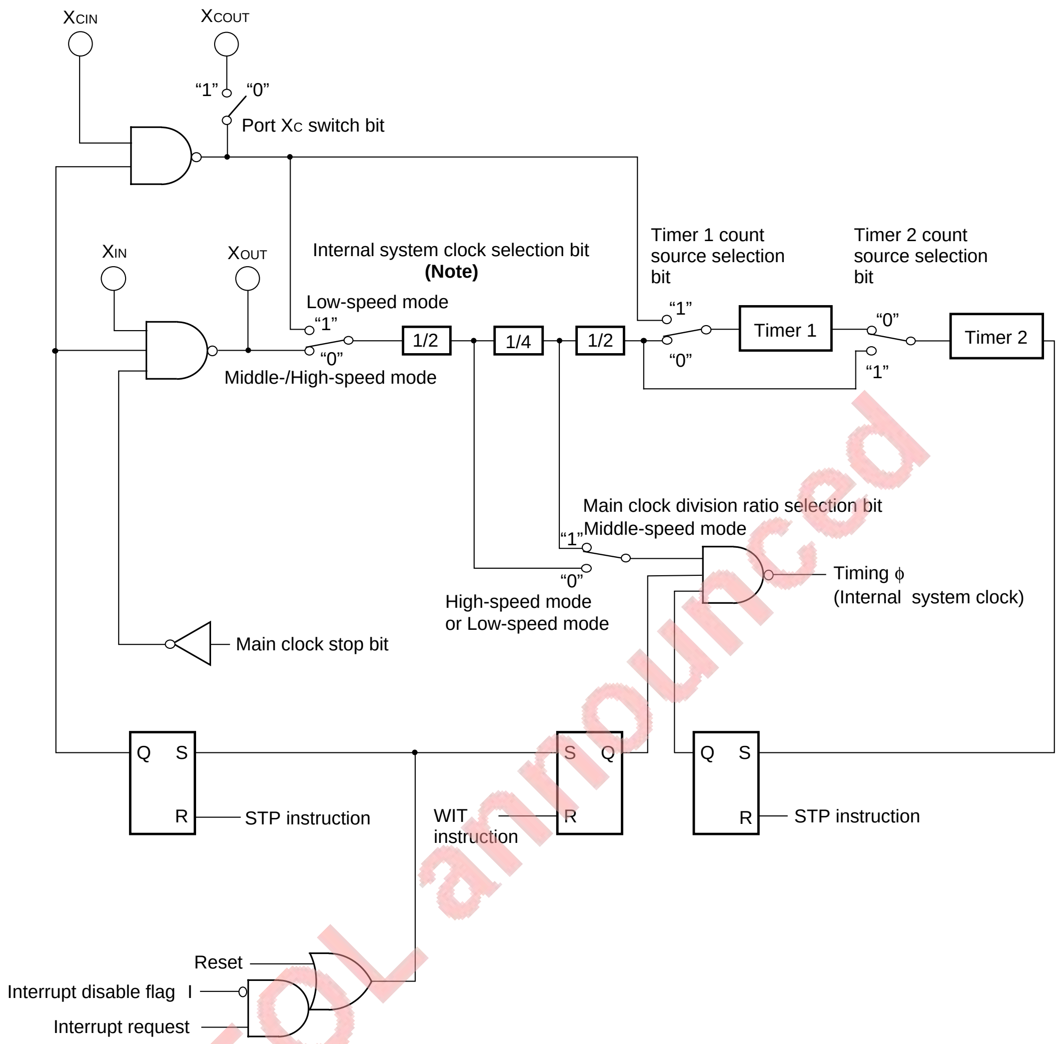
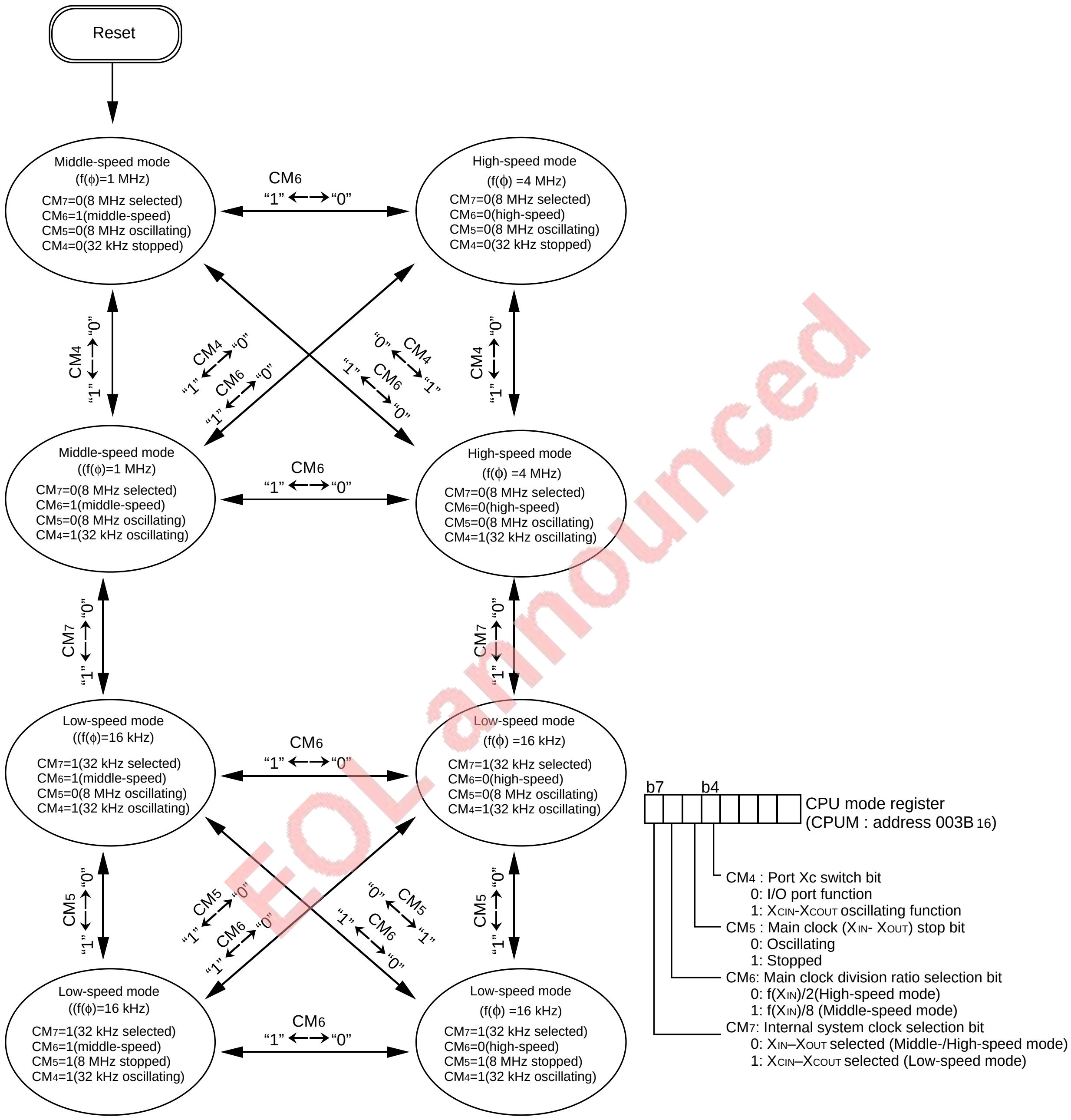


Fig. 41 External clock input circuit



Note : When using the low-speed mode, set the port XC switch bit to "1" .

Fig. 42 Clock generating circuit block diagram



Notes 1: Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
2: The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3: Timer,LCD operate in the wait mode.
4: When the stop mode is ended, a delay of approximately 1 ms occurs by connecting Timer 1 and Timer 2 in middle-/high-speed mode.
5: When the stop mode is ended, a delay of approximately 0.25 s occurs in low-speed mode.
6: Wait until oscillation stabilizes after oscillating the main clock X_{IN} before the switching from the low-speed mode to middle/high-speed mode.
7: The example assumes that 8 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. ϕ indicates the internal system clock.

Fig. 43 State transitions of system clock

NOTES ON PROGRAMMING
Processor Status Register
The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts
The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations
- To calculate in decimal notation, set the decimal mode flag (D) to "1," then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers
If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions
- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports
The contents of the port direction registers cannot be read. The following cannot be used:
- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O
- Using an external clock
  When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing serial I/O transfer and serial I/O automatic transfer.
- Using an internal clock
  When using an internal clock, set the synchronous clock to the internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer and serial I/O automatic transfer.

A-D Converter
The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Therefore, make sure that f(X_{IN}) is at least on 500 kHz during an A-D conversion.
Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time
The instruction execution time is obtained by multiplying the frequency of the internal system clock by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal system clock is the same half of the X_{IN} frequency in high-speed mode.

At STP Instruction Release
At the STP instruction release, all bits of the timer 12 mode register are cleared.

NOTES ON USE
Notes on Built-in EPROM Version
The $P5_1$ pin of the One Time PROM version or the EPROM version functions as the power source input pin of the internal EPROM.
Therefore, this pin is set at low input impedance, thereby being affected easily by noise.
To prevent a malfunction due to noise, insert a resistor (approx. 5 kΩ) in series with the $P5_1$ pin.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

DATA REQUIRED FOR ROM WRITING ORDERS

The following are necessary when ordering a ROM writing:

1. ROM Writing Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

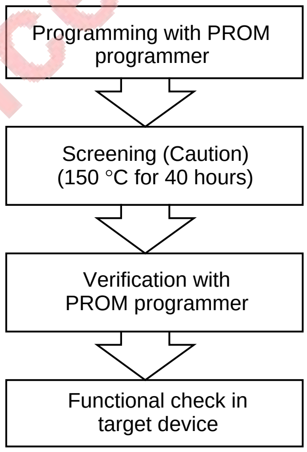
ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Table 10 Programming adapter

Package	Name of Programming Adapter
80P6N-A	PCA4738F-80A
80D0	PCA4738L-80A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 44 is recommended to verify programming.



Caution : The screening temperature is far higher than the storage temperature. Never expose to 150 °C exceeding 100 hours.

Fig. 44 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

Table 11 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on Vss. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$, $P8_0$–$P8_7$		–0.3 to V_{CC}+0.3	V
V_I	Input voltage	V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage	V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage	V_{L3}		V_{L2} to V_{CC}+0.3	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC}+0.3	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	At output port	–0.3 to V_{CC}+0.3	V
			At segment output	–0.3 to V_{L3}+0.3	V
V_O	Output voltage	COM_0–COM_3		–0.3 to V_{L3}+0.3	V
V_O	Output voltage	$P4_0$–$P4_7$, $P5_0$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$, $P8_0$–$P8_7$		–0.3 to V_{CC}+0.3	V
V_O	Output voltage	X_{OUT}		–0.3 to V_{CC}+0.3	V
P_d	Power dissipation		Ta = 25°C	300	mW
T_{opr}	Operating temperature			–20 to 85	°C
T_{stg}	Storage temperature			–40 to 125	°C

Table 12 Recommended operating conditions (Vcc = 2.5 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Power source voltage	High-speed mode f(X_{IN}) = 8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(X_{IN}) = 8 MHz	2.5	5.0	5.5	V
		Low-speed mode	2.5	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	A-D converter reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage	AN_0–AN_7	AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$	0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ (CM4 = 0)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$P8_0$–$P8_7$	0.4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$	0		0.3V_{CC}	V
V_{IL}	"L" input voltage	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ (CM4 = 0)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage	$P8_0$–$P8_7$	0		0.16V_{CC}	V
V_{IL}	"L" input voltage	$\overline{RESET}$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.2V_{CC}	V

Table 13 Recommended operating conditions (Vcc = 2.5 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ $P8_0$–$P8_7$, $P5_0$			–60	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current **(Note 1)** $P4_0$–$P4_7$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$			–30	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** $P8_0$–$P8_7$, $P5_0$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** $P4_0$–$P4_7$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$			40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ $P8_0$–$P8_7$, $P5_0$			–30	mA
$\Sigma I_{OH(avg)}$	"H" total average output current **(Note 1)** $P4_0$–$P4_7$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$			–15	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** $P8_0$–$P8_7$, $P5_0$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** $P4_0$–$P4_7$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$			20	mA
$I_{OH(peak)}$	"H" peak output current **(Note 2)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–2.0	mA
$I_{OH(peak)}$	"H" peak output current **(Note 2)** $P4_0$–$P4_7$, $P5_0$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ $P8_0$–$P8_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			5.0	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** $P4_0$–$P4_7$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$			10	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** $P8_0$–$P8_7$, $P5_0$			30	mA
$I_{OH(avg)}$	"H" average output current **(Note 3)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–2.0	mA
$I_{OH(avg)}$	"H" average output current **(Note 3)** $P4_0$–$P4_7$, $P5_0$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ $P8_0$–$P8_7$			–5.0	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			2.5	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** $P4_0$–$P4_7$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$			5.0	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** $P8_0$–$P8_7$, $P5_0$			15	mA

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current is average value measured over 100 ms.

Table 14 Recommended operating conditions (Vcc = 2.5 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$f(CNTR_0)$ $f(CNTR_1)$	Input frequency (duty cycle 50%)	(4.0 V ≤ V_{CC} ≤ 5.5 V)			4.0	MHz
		(V_{CC} ≤ 4.0 V)			(2×V_{CC})–4	MHz
$f(X_{IN})$	Main clock input oscillation frequency **(Note 4)**	High-speed mode (4.0 V ≤ V_{CC} ≤ 5.5 V)			8.0	MHz
		High-speed mode (V_{CC} ≤ 4.0 V)			(4×V_{CC})–8	MHz
		Middle-speed mode			8.0	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency **(Notes 4, 5)**			32.768	50	kHz

Notes 4: When the oscillation frequency has a duty cycle of 50%.
5: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Table 15 Electrical characteristics (Vcc = 4.0 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	I_{OH} = –2.0 mA	V_{CC}–2.0			V
		I_{OH} = –0.6 mA, V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OH}	"H" output voltage $P4_0$–$P4_7$, $P5_0$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$, $P8_0$–$P8_7$ **(Note)**	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.25 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA, V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	I_{OL} = 2.5 mA			2.0	V
		I_{OL} = 1.25 mA			0.5	V
		I_{OL} = 1.25 mA, V_{CC} = 2.5 V			1.0	V
V_{OL}	"L" output voltage $P4_0$–$P4_7$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OL} = 5.0 mA			2.0	V
		I_{OL} = 2.5 mA			0.5	V
		I_{OL} = 2.5 mA, V_{CC} = 2.5 V			1.0	V
V_{OL}	"L" output voltage $P8_0$–$P8_7$, $P5_0$	I_{OL} = 15 mA			2.0	V
V_{T+}–V_{T-}	Hysteresis INT_0–INT_2, $CNTR_0$, $CNTR_1$, $P8_0$–$P8_7$			0.5		V
V_{T+}–V_{T-}	Hysteresis S_{CLK1}, S_{IN}			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$	$\overline{RESET}$: V_{CC} = 2.5 V – 5.5 V		0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$	V_I = V_{CC}, Pull-down "off"			5.0	µA
		V_{CC} = 5.0 V, V_I = V_{CC}, Pull-down "on"	30	70	140	µA
		V_{CC} = 3.0 V, V_I = V_{CC}, Pull-down "on"	6.0	25	45	µA
I_{IH}	"H" input current $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$, $P8_0$–$P8_7$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P5_1$				–5.0	µA
I_{IL}	"L" input current $P4_0$–$P4_7$, $P5_0$, $P5_2$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$, $P8_0$–$P8_7$	V_I = V_{SS}, Pull-up "off"			–5.0	µA
		V_{CC} = 5.0 V, V_I = V_{SS}, Pull-up "on"	–30	–70	–140	µA
		V_{CC} = 3.0 V, V_I = V_{SS}, Pull-up "on"	–6	–25	–45	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4		µA

Note: When "1" is set to the port X_C switch bit (bit 4 of address $003B_{16}$) of the CPU mode register, the drive ability of Port $P7_0$ is different from the value above mentioned.

Table 16 Electrical characteristics (V_{CC} = 2.5 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{RAM}	RAM hold voltage	When clock is stopped	2.0		5.5	V
I_{CC}	Power source current	High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”, A-D converter in operating		6.4	13	mA
		High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”, A-D converter stopped		1.6	3.2	mA
		Low-speed mode, V_{CC} = 3 V, Ta ≤ 55 °C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”		15	22	µA
		Low-speed mode, V_{CC} = 3 V, Ta = 25 °C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”		4.5	9.0	µA
		All oscillation stopped (in STP state) Output transistors “off” — Ta = 25 °C		0.1	1.0	µA
		All oscillation stopped (in STP state) Output transistors “off” — Ta = 85 °C			10	µA

Table 17 A-D converter characteristics
(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, 4 MHz ≤ f(XIN) ≤ 8 MHz, in middle-speed/high-speed mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 5.12 V		±1	±2.5	LSB
T_{conv}	Conversion time		61		62	tc(φ)
IV_{REF}	Reference input current	V_{REF} = 5 V	50	150	200	μA
I_{IA}	Analog port input current			0.5	5.0	μA
R_{LADDER}	Ladder resistor			35		kΩ

Table 18 Timing requirements 1 (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\overline{RESET})$	Reset input “L” pulse width	2			µs
$t_c(X_{IN})$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH}(X_{IN})$	Main clock input “H” pulse width	45			ns
$t_{wL}(X_{IN})$	Main clock input “L” pulse width	40			ns
$t_c(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	250			ns
$t_{wH}(CNTR)$	$CNTR_0$, $CNTR_1$ input “H” pulse width	105			ns
$t_{wL}(CNTR)$	$CNTR_0$, $CNTR_1$ input “L” pulse width	105			ns
$t_{wH}(INT)$	INT_0–INT_2 input “H” pulse width	80			ns
$t_{wL}(INT)$	INT_0–INT_2 input “L” pulse width	80			ns
$t_c(S_{CLK})$	Serial I/O clock input cycle time	800			ns
$t_{wH}(S_{CLK})$	Serial I/O clock input “H” pulse width	370			ns
$t_{wL}(S_{CLK})$	Serial I/O clock input “L” pulse width	370			ns
$t_{su}(S_{IN}-S_{CLK})$	Serial I/O input setup time	220			ns
$t_h(S_{CLK}-S_{IN})$	Serial I/O input hold time	100			ns

Table 19 Timing requirements 2 (Vcc = 2.5 to 4.0 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\overline{RESET})$	Reset input “L” pulse width	2			µs
$t_c(X_{IN})$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH}(X_{IN})$	Main clock input “H” pulse width	45			ns
$t_{wL}(X_{IN})$	Main clock input “L” pulse width	40			ns
$t_c(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	$500/(V_{CC}–2)$			ns
$t_{wH}(CNTR)$	$CNTR_0$, $CNTR_1$ input “H” pulse width	$250/(V_{CC}–2)–20$			ns
$t_{wL}(CNTR)$	$CNTR_0$, $CNTR_1$ input “L” pulse width	$250/(V_{CC}–2)–20$			ns
$t_{wH}(INT)$	INT_0–INT_2 input “H” pulse width	230			ns
$t_{wL}(INT)$	INT_0–INT_2 input “L” pulse width	230			ns
$t_c(S_{CLK})$	Serial I/O clock input cycle time	2000			ns
$t_{wH}(S_{CLK})$	Serial I/O clock input “H” pulse width	950			ns
$t_{wL}(S_{CLK})$	Serial I/O clock input “L” pulse width	950			ns
$t_{su}(S_{IN}-S_{CLK})$	Serial I/O input setup time	400			ns
$t_h(S_{CLK}-S_{IN})$	Serial I/O input hold time	200			ns

Table 20 Switching characteristics 1 (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

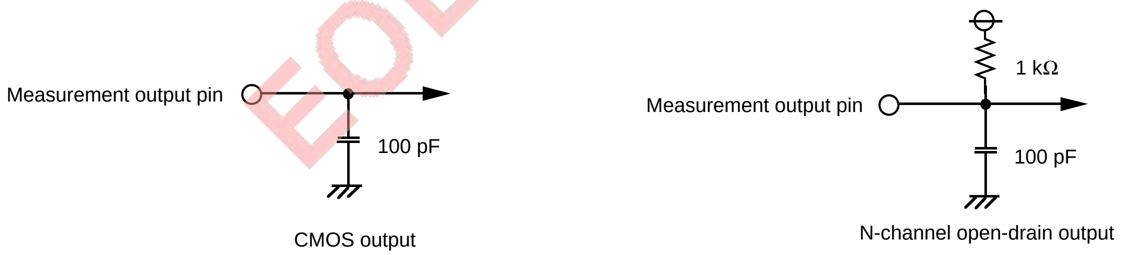
Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{wH}(SCLK)	Serial I/O clock output “H” pulse width	t_c(SCLK)/2–30			ns
t_{wL}(SCLK)	Serial I/O clock output “L” pulse width	t_c(SCLK)/2–30			ns
t_d(SCLK-SOUT)	Serial I/O output delay time **(Note 1)**			140	ns
t_v(SCLK-SOUT)	Serial I/O output valid time **(Note 1)**	–30			ns
t_r(SCLK)	Serial I/O clock output rising time			30	ns
t_f(SCLK)	Serial I/O clock output falling time			30	ns
t_r(CMOS)	CMOS output rising time **(Note 2)**		10	30	ns
t_f(CMOS)	CMOS output falling time **(Note 2)**		10	30	ns

Notes 1: When the P-channel output disable bit (bit 7 of address 0019_{16}) is “0.”
2: The XOUT, XCOUT pins are excluded.

Table 21 Switching characteristics 2 (Vcc = 2.5 to 4.0 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{wH}(SCLK)	Serial I/O clock output “H” pulse width	t_c(SCLK)/2–50			ns
t_{wL}(SCLK)	Serial I/O clock output “L” pulse width	t_c(SCLK)/2–50			ns
t_d(SCLK-SOUT)	Serial I/O output delay time **(Note 1)**			350	ns
t_v(SCLK-SOUT)	Serial I/O output valid time **(Note 1)**	–30			ns
t_r(SCLK)	Serial I/O clock output rising time			50	ns
t_f(SCLK)	Serial I/O clock output falling time			50	ns
t_r(CMOS)	CMOS output rising time **(Note 2)**		20	50	ns
t_f(CMOS)	CMOS output falling time **(Note 2)**		20	50	ns

Notes 1: When the P-channel output disable bit (bit 7 of address 0019_{16}) is “0.”
2: The XOUT, XCOUT pins are excluded.



Note: When bit 7 of the serial I/O control register 1 (address 0019_{16}) is “ 1.”
(N-channel open-drain output mode)

Fig. 45 Circuit for measuring output switching characteristics

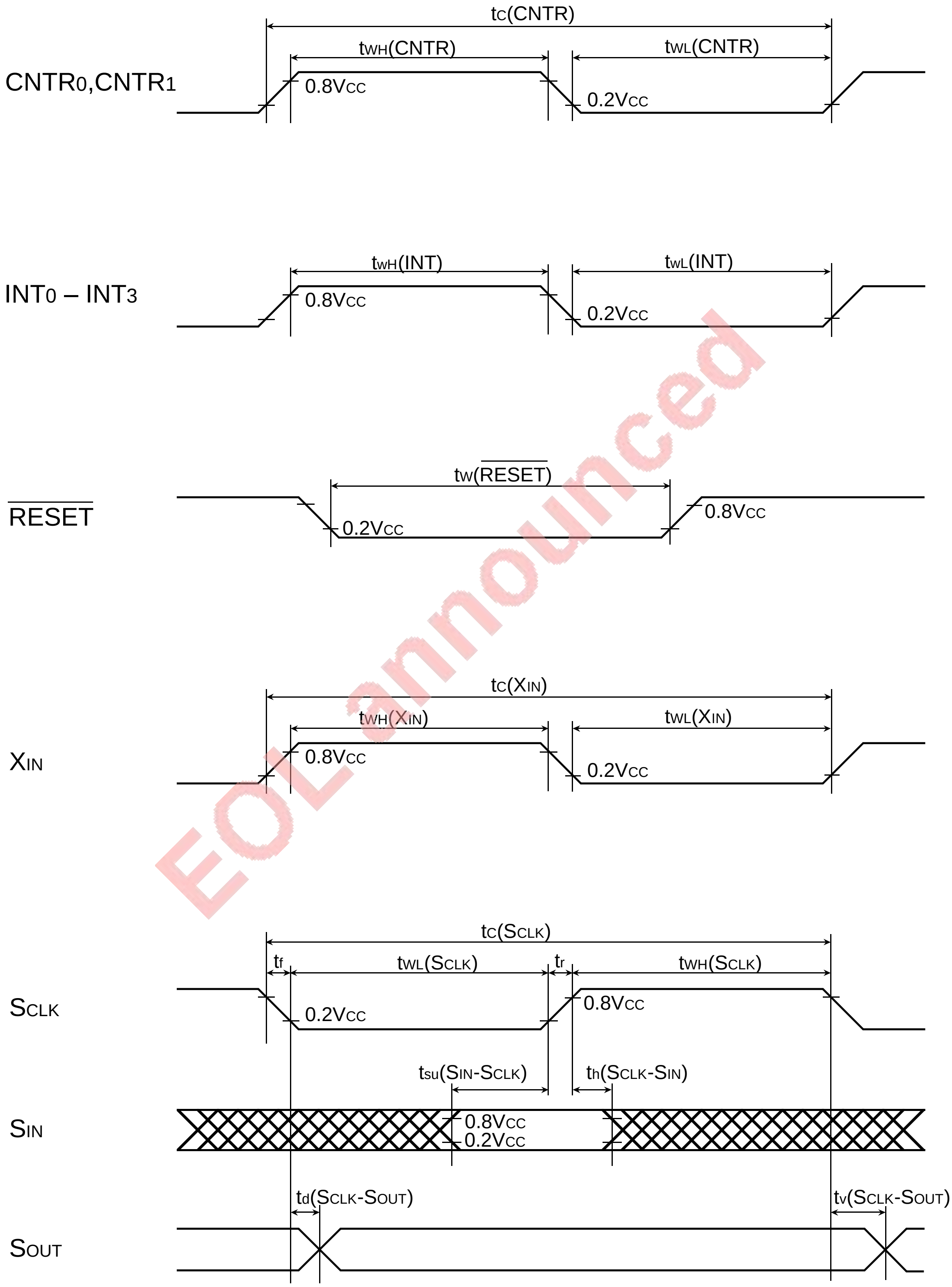


Fig. 46 Timing diagram

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

GZZ-SH52-95B<85A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C34M6AXXXFP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ❋.

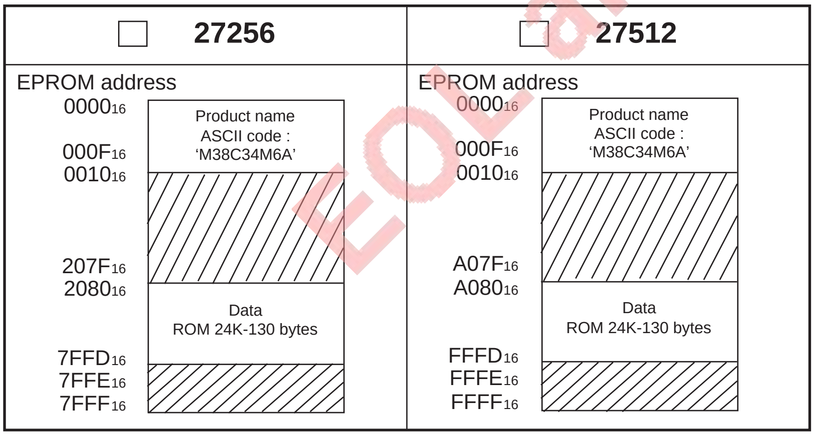
❋					
Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

❋ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address $A080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".
(2) The ASCII codes of the product name "M38C34M6A" must be entered in addresses 0000_{16} to 0008_{16}. And set data "FF_{16}" in addresses 0009_{16} to $000F_{16}$. The ASCII codes and addresses are listed to the right in hesadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'A' = 41_{16}
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'8' = 38_{16}	$000A_{16}$	FF_{16}
0003_{16}	'C' = 43_{16}	$000B_{16}$	FF_{16}
0004_{16}	'3' = 33_{16}	$000C_{16}$	FF_{16}
0005_{16}	'4' = 34_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'6' = 36_{16}	$000F_{16}$	FF_{16}

(1/2)

GZZ-SH52-95B<85A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C34M6AXXXFP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembier source program because ASCII codes of the product name are written to addresses 0000_{16} to 0008_{16} of EPROM.

EPROM type	27256	27512
The pseudo-command	*=Δ$8000 .BYTEΔ'M38C34M6A'	*=Δ$0000 .BYTEΔ'M38C34M6A'

Note : If the name of the product written to the EPROMs does not match the name of the mask ROM confirmation form, the ROM will not be processed.

❋ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N) and attach it to the mask ROM confirmation form.

❋ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other ( )

At what frequency? $f(X_{IN})$ = [ ] MHz

(2) Which function will you use the $P7_0/X_{CIN}$ and $P7_0/X_{COUT}$ pins?

☐ Port $P7_0$ and $P7_1$ function ☐ X_{CIN}-X_{COUT} function (external resonator)

❋ 4. Comments

(2/2)

RENESAS
Renesas Technology Corp.

GZZ-SH52-96B<85A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C34M6MXXXFP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ❋.

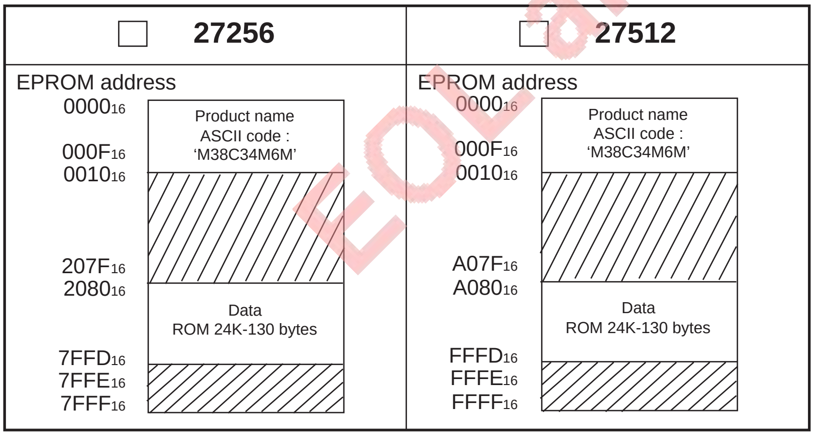
❋ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

❋ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address $A080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".
(2) The ASCII codes of the product name "M38C34M6M" must be entered in addresses 0000_{16} to 0008_{16}. And set data "FF_{16}" in addresses 0009_{16} to $000F_{16}$. The ASCII codes and addresses are listed to the right in hesadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'M' = $4D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'8' = 38_{16}	$000A_{16}$	FF_{16}
0003_{16}	'C' = 43_{16}	$000B_{16}$	FF_{16}
0004_{16}	'3' = 33_{16}	$000C_{16}$	FF_{16}
0005_{16}	'4' = 34_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'6' = 36_{16}	$000F_{16}$	FF_{16}

(1/2)

GZZ-SH52-96B<85A0>

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C34M6MXXXFP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembier source program because ASCII codes of the product name are written to addresses 0000_{16} to 0008_{16} of EPROM.

EPROM type	27256	27512
The pseudo-command	*=Δ$8000 .BYTEΔ'M38C34M6M'	*=Δ$0000 .BYTEΔ'M38C34M6M'

Note : If the name of the product written to the EPROMs does not match the name of the mask ROM confirmation form, the ROM will not be processed.

❋ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N) and attach it to the mask ROM confirmation form.

❋ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other (   )

At what frequency? $f(X_{IN})$ = ☐ MHz

(2) Which function will you use the $P7_0/X_{CIN}$ and $P7_0/X_{COUT}$ pins?

☐ Port $P7_0$ and $P7_1$ function ☐ X_{CIN}-X_{COUT} function (external resonator)

❋ 4. Comments

(2/2)

GZZ-SH52-97B<85A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C37ECAXXXFP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ❋.

❋ Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

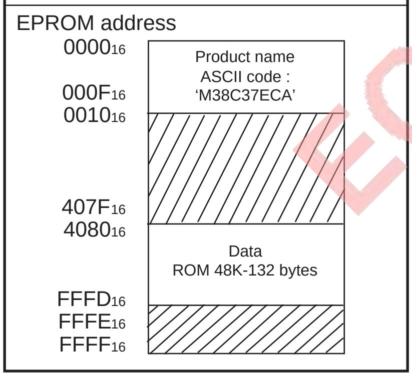
❋ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM programming based on this data. We shall assume the responsibility for errors only if the ROM programming data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)

☐ **27512**



In the address space of the microcomputer, the internal ROM area is from address 4080_{16} to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".
(2) The ASCII codes of the product name "M38C37ECA" must be entered in addresses 0000_{16} to 0008_{16}. And set data "FF_{16}" in addresses 0009_{16} to $000F_{16}$. The ASCII codes and addresses are listed to the right in hesadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'A' = 41_{16}
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'8' = 38_{16}	$000A_{16}$	FF_{16}
0003_{16}	'C' = 43_{16}	$000B_{16}$	FF_{16}
0004_{16}	'3' = 33_{16}	$000C_{16}$	FF_{16}
0005_{16}	'7' = 37_{16}	$000D_{16}$	FF_{16}
0006_{16}	'E' = 45_{16}	$000E_{16}$	FF_{16}
0007_{16}	'C' = 43_{16}	$000F_{16}$	FF_{16}

(1/2)

GZZ-SH52-97B<85A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C37ECAXXXFP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembier source program because ASCII codes of the product name are written to addresses 0000_{16} to 0008_{16} of EPROM.

EPROM type	27512
The pseudo-command	*=Δ$0000 .BYTEΔ‘M38C37ECA’

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM will not be processed.

❋ 2. Mark specification
Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N) and attach it to the ROM programming confirmation form.

❋ 3. Usage conditions
Please answer the following questions about usage for use in our product inspection :
(1) How will you use the X_{IN}-X_{OUT} oscillator?

☐ Ceramic resonator ☐ Quartz crystal
☐ External clock input ☐ Other ( )

At what frequency? $f(X_{IN})$ = ☐ MHz

(2) Which function will you use the $P7_0/X_{CIN}$ and $P7_0/X_{COUT}$ pins?

☐ Port $P7_0$ and $P7_1$ function ☐ X_{CIN}-X_{COUT} function (external resonator)

❋ 4. Comments

(2/2)

RENESAS
Renesas Technology Corp.

GZZ-SH52-98B<85A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C37ECMXXXFP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ❋.

❋ Customer	Company name		TEL ( )	Issuance signature	Submitted by	Supervisor
	Date issued	Date:				

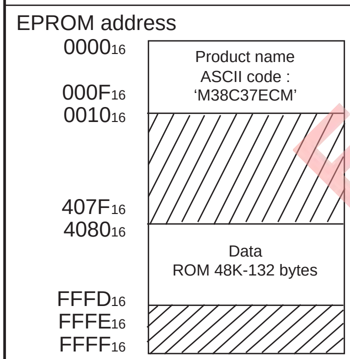
❋ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM programming based on this data. We shall assume the responsibility for errors only if the ROM programming data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)

☐ **27512**



In the address space of the microcomputer, the internal ROM area is from address 4080_{16} to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".
(2) The ASCII codes of the product name "M38C37ECM" must be entered in addresses 0000_{16} to 0008_{16}. And set data "FF_{16}" in addresses 0009_{16} to $000F_{16}$. The ASCII codes and addresses are listed to the right in hesadecimal notation.

Address	
0000_{16}	'M' = $4D_{16}$
0001_{16}	'3' = 33_{16}
0002_{16}	'8' = 38_{16}
0003_{16}	'C' = 43_{16}
0004_{16}	'3' = 33_{16}
0005_{16}	'7' = 37_{16}
0006_{16}	'E' = 45_{16}
0007_{16}	'C' = 43_{16}

Address	
0008_{16}	' M ' =$4D_{16}$
0009_{16}	FF_{16}
$000A_{16}$	FF_{16}
$000B_{16}$	FF_{16}
$000C_{16}$	FF_{16}
$000D_{16}$	FF_{16}
$000E_{16}$	FF_{16}
$000F_{16}$	FF_{16}

(1/2)

GZZ-SH52-98B<85A0>

ROM number	

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38C37ECMXXXFP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembier source program because ASCII codes of the product name are written to addresses 0000_{16} to 0008_{16} of EPROM.

EPROM type	27512
The pseudo-command	*=Δ$0000 .BYTEΔ'M38C37ECM'

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM will not be processed.

❋ 2. Mark specification
Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N) and attach it to the ROM programming confirmation form.

❋ 3. Usage conditions
Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator?

☐ Ceramic resonator ☐ Quartz crystal
☐ External clock input ☐ Other ( )

At what frequency? $f(X_{IN})$ = ☐ MHz

(2) Which function will you use the $P7_0/X_{CIN}$ and $P7_0/X_{COUT}$ pins?

☐ Port $P7_0$ and $P7_1$ function ☐ X_{CIN}-X_{COUT} function (external resonator)

❋ 4. Comments

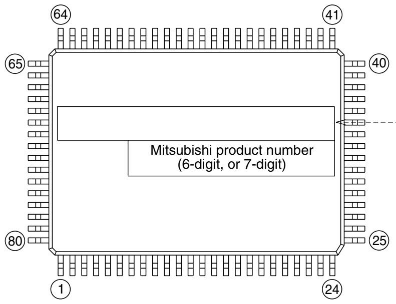
(2/2)

80P6N (80-PIN QFP) MARK SPECIFICATION FORM

Mitsubishi IC catalog name

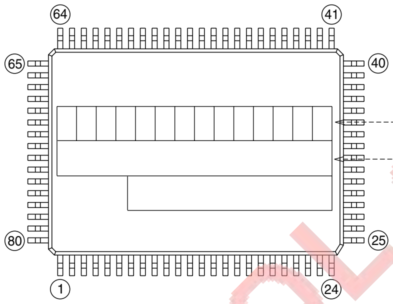
Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



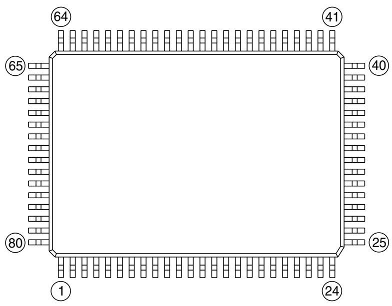
Mitsubishi IC catalog name

B. Customer's Parts Number + Mitsubishi IC Catalog Name



Customer's Parts Number
Note : The fonts and size of characters are standard Mitsubishi type.
Mitsubishi IC catalog name
Notes 1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.

C. Special Mark Required



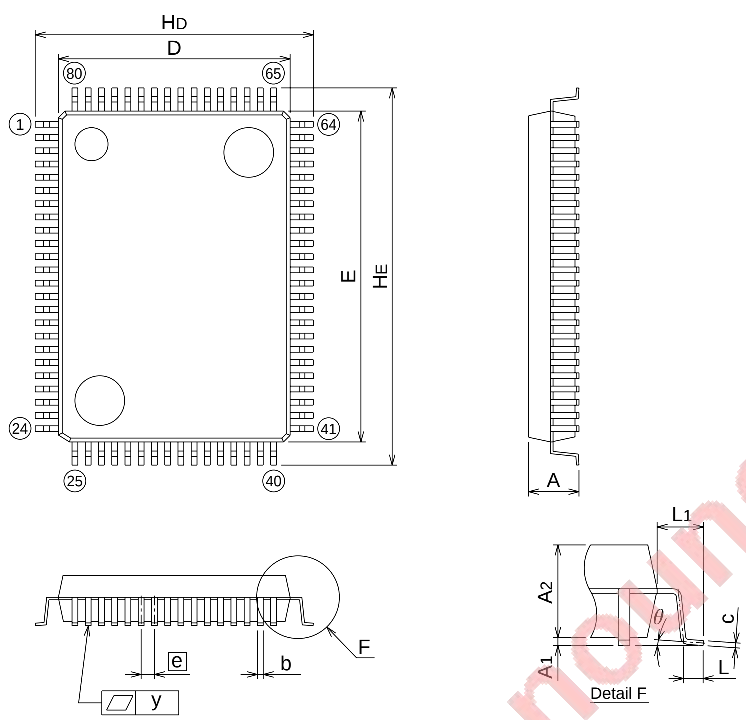
Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible.
Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.
2 : If special character fonts (e,g., customer's trade mark logo) must be used in Special Mark, check the box below.
For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

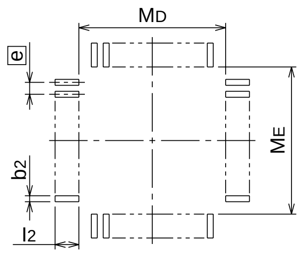
Special character fonts required

80P6N-A

Plastic 80pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1420-0.80	–	1.58	Alloy 42





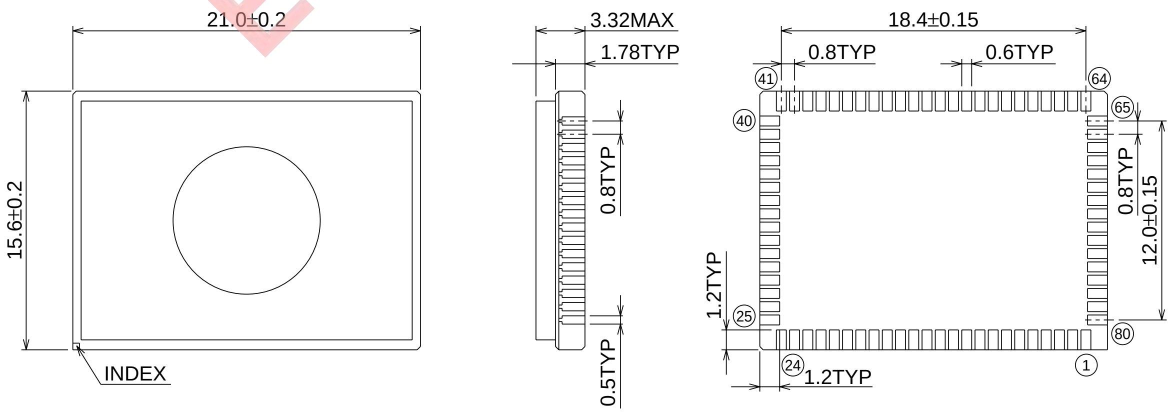
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
$\boxed{e}$	–	0.8	–
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	–	1.4	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.5	–
l_2	1.3	–	–
M_D	–	14.6	–
M_E	–	20.6	–

80D0

Glass seal 80pin QFN

EIAJ Package Code	JEDEC Code	Weight(g)
–	–	



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REVISION DESCRIPTION LIST	38C3 GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	980602