

16/32

M32C/84 Group (M32C/84, M32C/84T) Hardware Manual

RENESAS 16/32-BIT SINGLE-CHIP MICROCOMPUTER
M16C FAMILY / M32C/80 SERIES

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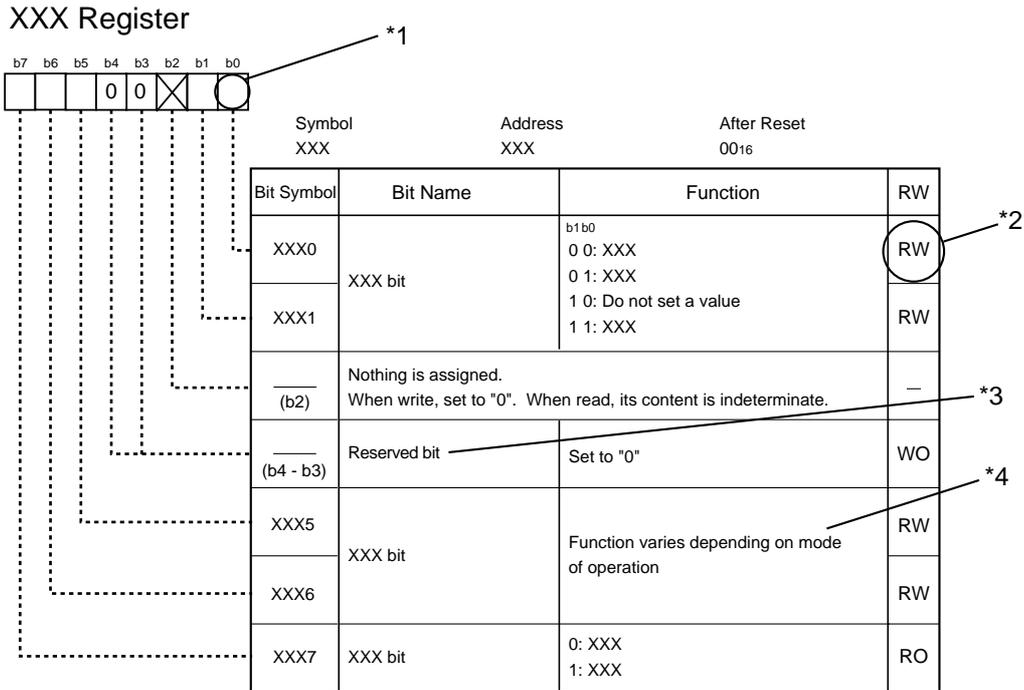
How to Use This Manual

1. Introduction

This hardware manual provides detailed information on the M32C/84 group (M32C/84, M32C/84T) microcomputers. Users are expected to have basic knowledge of electric circuits, logical circuits and microcomputers.

2. Register Diagram

The symbols, and descriptions, used for bit function in each register are shown below.



*1
Blank: Set to "0" or "1" according to the application

- 0: Set to "0"
- 1: Set to "1"
- X: Nothing is assigned

*2
RW: Read and write
RO: Read only
WO: Write only
—: Nothing is assigned

*3
• Reserved bit
Reserved bit. Set to specified value.

*4
• Nothing is assigned
Nothing is assigned to the bit concerned. As the bit may be use for future functions, set to "0" when writing to this bit.
• Do not set a value
The operation is not guaranteed when a value is set.
• Function varies depending on mode of operation
Bit function varies depending on peripheral function mode.
Refer to respective register for each mode.

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032A ₁₆	UART3 Transmit Buffer Register (U3TB)	195	
032B ₁₆			
032C ₁₆	UART3 Transmit/Receive Control Register 0 (U3C0)	197	
032D ₁₆	UART3 Transmit/Receive Control Register 1 (U3C1)	198	
032E ₁₆	UART3 Receive Buffer Register (U3RB)	195	
032F ₁₆			
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 Special Mode Register 4 (U2SMR4)	201	
0335 ₁₆	UART2 Special Mode Register 3 (U2SMR3)	200	
0336 ₁₆	UART2 Special Mode Register 2 (U2SMR2)	199	
0337 ₁₆	UART2 Special Mode Register (U2SMR)	198	
0338 ₁₆	UART2 Transmit/Receive Mode Register (U2MR)	196	
0339 ₁₆	UART2 Bit Rate Register (U2BRG)		
033A ₁₆	UART2 Transmit Buffer Register (U2TB)	195	
033B ₁₆			
033C ₁₆	UART2 Transmit/Receive Control Register 0 (U2C0)	197	
033D ₁₆	UART2 Transmit/Receive Control Register 1 (U2C1)	198	
033E ₁₆	UART2 Receive Buffer Register (U2RB)	195	
033F ₁₆			
0340 ₁₆	Count Start Flag (TABSR)	158	
0341 ₁₆	Clock Prescaler Reset Flag (CPSRF)	87	
0342 ₁₆	One-Shot Start Flag (ONSF)	159	
0343 ₁₆	Trigger Select Register (TRGSR)	160	
0344 ₁₆	Up-Down Flag (UDF)	159	
0345 ₁₆			
0346 ₁₆	Timer A0 Register (TA0)	157	
0347 ₁₆			
0348 ₁₆	Timer A1 Register (TA1)		
0349 ₁₆			
034A ₁₆	Timer A2 Register (TA2)		
034B ₁₆			
034C ₁₆	Timer A3 Register (TA3)		
034D ₁₆			
034E ₁₆	Timer A4 Register (TA4)		
034F ₁₆			

Blank spaces are reserved. No access is allowed.

Quick Reference by Address

Address	Register	Page	Address	Register	Page
0350 ¹⁶ 0351 ¹⁶	Timer B0 Register (TB0)	173	0380 ¹⁶ 0381 ¹⁶	A/D0 Register0 (AD00)	253
0352 ¹⁶ 0353 ¹⁶	Timer B1 Register (TB1)		0382 ¹⁶ 0383 ¹⁶	A/D0 Register1 (AD01)	
0354 ¹⁶ 0355 ¹⁶	Timer B2 Register (TB2)		0384 ¹⁶ 0385 ¹⁶	A/D0 Register2 (AD02)	
0356 ¹⁶	Timer A0 Mode Register (TA0MR)	158	0386 ¹⁶ 0387 ¹⁶	A/D0 Register3 (AD03)	
0357 ¹⁶	Timer A1 Mode Register (TA1MR)		0388 ¹⁶ 0389 ¹⁶	A/D0 Register4 (AD04)	
0358 ¹⁶	Timer A2 Mode Register (TA2MR)		038A ¹⁶ 038B ¹⁶	A/D0 Register5 (AD05)	
0359 ¹⁶	Timer A3 Mode Register (TA3MR)		038C ¹⁶ 038D ¹⁶	A/D0 Register6 (AD06)	
035A ¹⁶	Timer A4 Mode Register (TA4MR)	174	038E ¹⁶ 038F ¹⁶	A/D0 Register7 (AD07)	
035B ¹⁶	Timer B0 Mode Register (TB0MR)		0390 ¹⁶		
035C ¹⁶	Timer B1 Mode Register (TB1MR)		0391 ¹⁶		
035D ¹⁶	Timer B2 Mode Register (TB2MR)	188	0392 ¹⁶	A/D0 Control Register 4 (AD0CON4)	253
035E ¹⁶	Timer B2 Special Mode Register (TB2SC)	87	0393 ¹⁶		
035F ¹⁶	Count Source Prescaler Register (TCSPR)		0394 ¹⁶	A/D0 Control Register 2 (AD0CON2)	251
0360 ¹⁶			0395 ¹⁶	A/D0 Control Register 3 (AD0CON3)	252
0361 ¹⁶			0396 ¹⁶	A/D0 Control Register 0 (AD0CON0)	249
0362 ¹⁶			0397 ¹⁶	A/D0 Control Register 1 (AD0CON1)	250
0363 ¹⁶			0398 ¹⁶	D/A Register 0 (DA0)	267
0364 ¹⁶	UART0 Special Mode Register 4 (U0SMR4)	201	0399 ¹⁶		
0365 ¹⁶	UART0 Special Mode Register 3 (U0SMR3)	200	039A ¹⁶	D/A Register 1 (DA1)	267
0366 ¹⁶	UART0 Special Mode Register 2 (U0SMR2)	199	039B ¹⁶		
0367 ¹⁶	UART0 Special Mode Register (U0SMR)	198	039C ¹⁶	D/A Control Register (DACON)	267
0368 ¹⁶	UART0 Transmit/Receive Mode Register (U0MR)	196	039D ¹⁶		
0369 ¹⁶	UART0 Bit Rate Register (U0BRG)		039E ¹⁶		
036A ¹⁶ 036B ¹⁶	UART0 Transmit Buffer Register (U0TB)	195	039F ¹⁶		
036C ¹⁶	UART0 Transmit/Receive Control Register 0 (U0C0)	197	03A0 ¹⁶	Function Select Register A8 (PS8)	381
036D ¹⁶	UART0 Transmit/Receive Control Register 1 (U0C1)	198	03A1 ¹⁶	Function Select Register A9 (PS9)	382
036E ¹⁶ 036F ¹⁶	UART0 Receive Buffer Register (U0RB)	195	03A2 ¹⁶		
0370 ¹⁶			03A3 ¹⁶		
0371 ¹⁶			03A4 ¹⁶		
0372 ¹⁶			03A5 ¹⁶		
0373 ¹⁶			03A6 ¹⁶		
0374 ¹⁶			03A7 ¹⁶	Function Select Register D1 (PSD1)	382
0375 ¹⁶			03A8 ¹⁶		
0376 ¹⁶			03A9 ¹⁶		
0377 ¹⁶			03AA ¹⁶		
0378 ¹⁶	DMA0 Request Source Select Register (DM0SL)	137	03AB ¹⁶		
0379 ¹⁶	DMA1 Request Source Select Register (DM1SL)		03AC ¹⁶	Function Select Register C2 (PSC2)	385
037A ¹⁶	DMA2 Request Source Select Register (DM2SL)		03AD ¹⁶	Function Select Register C3 (PSC3)	386
037B ¹⁶	DMA3 Request Source Select Register (DM3SL)		03AE ¹⁶		
037C ¹⁶ 037D ¹⁶	CRC Data Register (CRCD)	268	03AF ¹⁶	Function Select Register C (PSC)	385
037E ¹⁶	CRC Input Register (CRCIN)				
037F ¹⁶					

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Quick Reference by Address

Address	Register	Page	Address	Register	Page
03B0 ₁₆	Function Select Register A0 (PS0)	379	03E0 ₁₆	Port P14 Register (P0)	378
03B1 ₁₆	Function Select Register A1 (PS1)		03E1 ₁₆	Port P14 Register (P1)	
03B2 ₁₆	Function Select Register B0 (PSL0)	383	03E2 ₁₆	Port P14 Direction Register (PD0)	377
03B3 ₁₆	Function Select Register B1 (PSL1)		03E3 ₁₆	Port P14 Direction Register (PD1)	
03B4 ₁₆	Function Select Register A2 (PS2)	376	03E4 ₁₆	Port P14 Register (P2)	378
03B5 ₁₆	Function Select Register A3 (PS3)		03E5 ₁₆	Port P14 Register (P3)	
03B6 ₁₆	Function Select Register B2 (PSL2)	384	03E6 ₁₆	Port P14 Direction Register (PD2)	377
03B7 ₁₆	Function Select Register B3 (PSL3)		03E7 ₁₆	Port P14 Direction Register (PD3)	
03B8 ₁₆		381	03E8 ₁₆	Port P14 Register (P4)	378
03B9 ₁₆	Function Select Register A5 (PS5)		03E9 ₁₆	Port P14 Register (P5)	
03BA ₁₆			03EA ₁₆	Port P14 Direction Register (PD4)	377
03BB ₁₆			03EB ₁₆	Port P14 Direction Register (PD5)	
03BC ₁₆			03EC ₁₆		
03BD ₁₆			03ED ₁₆		
03BE ₁₆			03EE ₁₆		
03BF ₁₆			03EF ₁₆		
03C0 ₁₆	Port P6 Register (P6)		378	03F0 ₁₆	Pull-up Control Register 0 (PUR0)
03C1 ₁₆	Port P7 Register (P7)	03F1 ₁₆		Pull-up Control Register 1 (PUR1)	
03C2 ₁₆	Port P6 Direction Register (PD6)	377	03F2 ₁₆		
03C3 ₁₆	Port P7 Direction Register (PD7)		03F3 ₁₆		
03C4 ₁₆	Port P8 Register (P8)	378	03F4 ₁₆		
03C5 ₁₆	Port P9 Register (P9)		03F5 ₁₆		
03C6 ₁₆	Port P8 Direction Register (PD8)	377	03F6 ₁₆		
03C7 ₁₆	Port P9 Direction Register (PD9)		03F7 ₁₆		
03C8 ₁₆	Port P10 Register (P10)	378	03F8 ₁₆		
03C9 ₁₆	Port P11 Register (P11)		03F9 ₁₆		
03CA ₁₆	Port P10 Direction Register (PD10)	377	03FA ₁₆		
03CB ₁₆	Port P11 Direction Register (PD11)		03FB ₁₆		
03CC ₁₆	Port P12 Register (P12)	378	03FC ₁₆		
03CD ₁₆	Port P13 Register (P13)		03FD ₁₆		
03CE ₁₆	Port P12 Direction Register (PD12)	377	03FE ₁₆		
03CF ₁₆	Port P13 Direction Register (PD13)		03FF ₁₆	Port Control Register (PCR)	389
03D0 ₁₆	Port P14 Register (P14)	378			
03D1 ₁₆	Port P15 Register (P15)				
03D2 ₁₆	Port P14 Direction Register (PD14)	377			
03D3 ₁₆	Port P15 Direction Register (PD15)				
03D4 ₁₆					
03D5 ₁₆					
03D6 ₁₆					
03D7 ₁₆					
03D8 ₁₆					
03D9 ₁₆					
03DA ₁₆	Pull-Up Control Register 2 (PUR2)		387		
03DB ₁₆	Pull-Up Control Register 3 (PUR3)	388			
03DC ₁₆	Pull-Up Control Register 4 (PUR4)				
03DD ₁₆					
03DE ₁₆					
03DF ₁₆					

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M32C/84 Group (M32C/84, M32C/84T)

SINGLE-CHIP 16/32-BIT CMOS MICROCOMPUTER

1. Overview

The M32C/84 group (M32C/84, M32C/84T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/84 group (M32C/84, M32C/84T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Performance Overview

Tables 1.1 and 1.2 list performance overview of the M32C/84 group (M32C/84, M32C/84T).

Table 1.1 M32C/84 Group (M32C/84, M32C/84T) Performance (144-Pin Package)

Characteristic		Performance	
		M32C/84	M32C/84T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, Vcc1=4.2 V to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, Vcc1=3.0 V to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, Vcc1=4.2 V to 5.5 V)
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	123 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus ⁽¹⁾ , I ² C bus ⁽²⁾	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 1 circuit, 34 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	38 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Voltage Detection Circuit	Available (optional)	Not available ⁽⁴⁾
Electrical Characteristics	Supply Voltage	Vcc1=4.2 V to 5.5 V, Vcc2=3.0 V to Vcc1 (f(BCLK)=32 MHz) Vcc1=3.0 V to 5.5 V, Vcc2=3.0 V to Vcc1 (f(BCLK)=24 MHz)	Vcc1=Vcc2=4.2 V to 5.5 V, (f(BCLK)=32 MHz) ⁽³⁾
	Power Consumption	28 mA (Vcc1=Vcc2=5 V, f(BCLK)=32 MHz) 22 mA (Vcc1=Vcc2=3.3 V, f(BCLK)=24 MHz) 10µA (Vcc1=Vcc2=5 V, f(BCLK)=32 kHz, in wait mode)	28 mA (Vcc1=Vcc2=5 V, f(BCLK)=32 MHz) 10µA (Vcc1=Vcc2=5 V, f(BCLK)=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V	
	Program and Erase Endurance	100 times (all space)	
Operating Ambient Temperature		-20 to 85°C	-40 to 85°C (T version)
		-40 to 85°C (optional)	
Package	144-pin plastic molded LQFP		

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
 2. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
 3. The supply voltage of M32C/84T (High-reliability version) must be Vcc1=Vcc2.
 4. The cold start-up/warm start-up determine function is available only at the user's option.
- All options are on a request basis.

Table 1.2 M32C/84 Group (M32C/84, M32C/84T) Performance (100-Pin Package)

Characteristic		Performance	
		M32C/84	M32C/84T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V _{CC1} =4.2 V to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, V _{CC1} =3.0 V to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, V _{CC1} =4.2 V to 5.5 V)
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	87 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus ⁽¹⁾ , I ² C bus ⁽²⁾	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	38 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Electrical Characteristics	Supply Voltage	V _{CC1} =4.2 V to 5.5 V, V _{CC2} =3.0 V to V _{CC1} (f(BCLK)=32 MHz) V _{CC1} =3.0 V to 5.5 V, V _{CC2} =3.0 V to V _{CC1} (f(BCLK)=24 MHz)
Power Consumption		28 mA (V _{CC1} =V _{CC2} =5 V, f(BCLK)=32 MHz) 22 mA (V _{CC1} =V _{CC2} =3.3 V, f(BCLK)=24 MHz) 10 μ A (V _{CC1} =V _{CC2} =5 V, f(BCLK)=32 kHz, in wait mode)	28 mA (V _{CC1} =V _{CC2} =5 V, f(BCLK)=32 MHz) 10 μ A (V _{CC1} =V _{CC2} =5 V, f(BCLK)=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V \pm 0.3 V or 5.0 V \pm 0.5 V	
	Program and Erase Endurance	100 times (all space)	
Operating Ambient Temperature		-20 to 85°C	-40 to 85°C (T version)
		-40 to 85°C (optional)	
Package	100-pin plastic molded LQFP/QFP		

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/84T (High-reliability version) must be V_{CC1}=V_{CC2}.
4. The cold start-up/warm start-up determine function is available only at the user's option.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/84 group (M32C/84, M32C/84T) microcomputer.

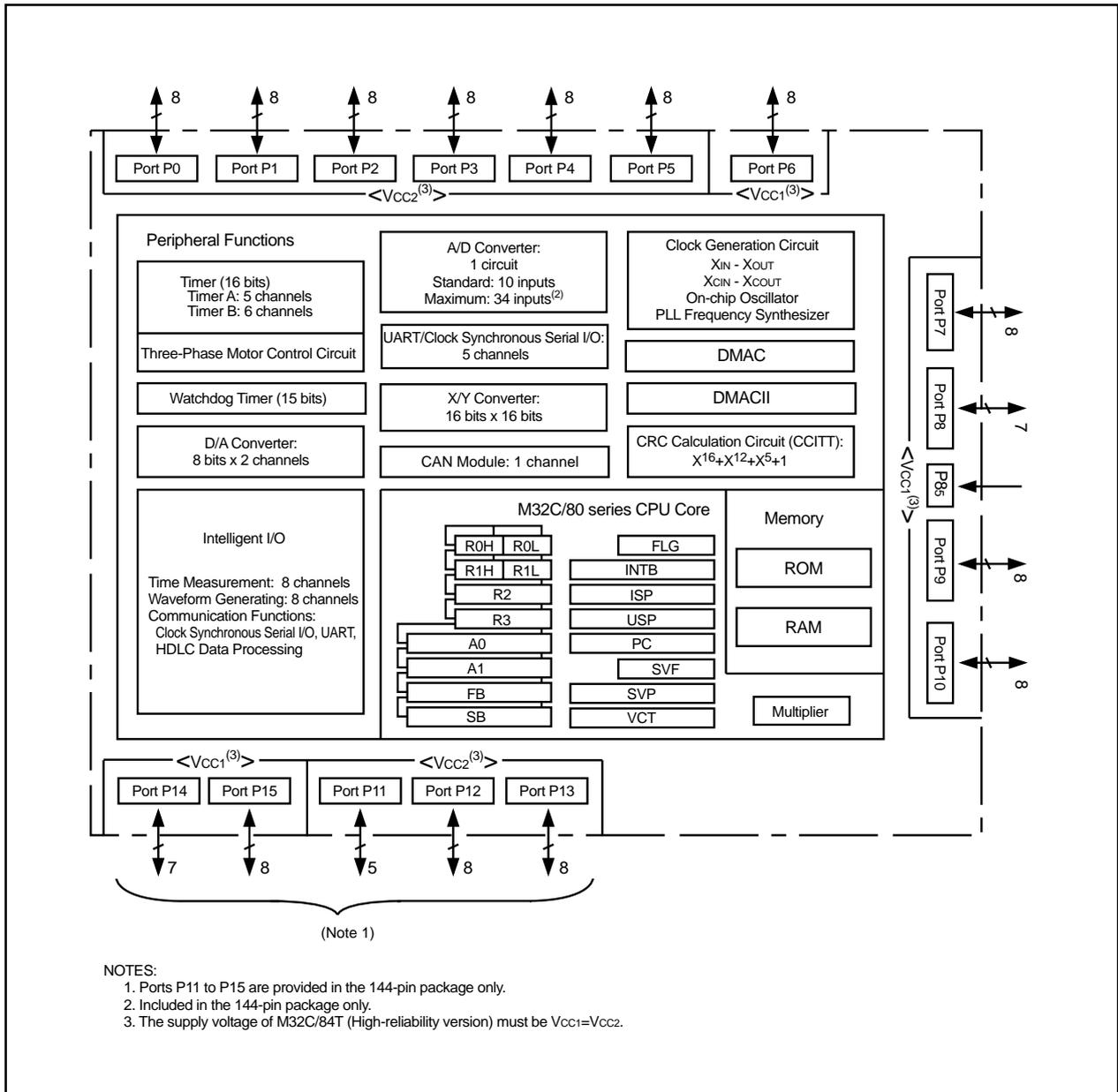


Figure 1.1 M32C/84 Group (M32C/84, M32C/84T) Block Diagram

1.4 Product Information

Table 1.3 lists product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/84 Group (1) (M32C/84)

As of July, 2005

Type Number	Package	ROM Capacity	RAM Capacity	Remarks		
M30845FJGP	PLQP0144KA-A (144P6Q-A)	512K+4K	24K	Flash Memory		
M30843FJGP	PLQP0100KB-A (100P6Q-A)					
M30843FJFP	PRQP0100JB-A (100P6S-A)					
M30845FHGP	PLQP0144KA-A (144P6Q-A)	384K+4K				
M30843FHGP	PLQP0100KB-A (100P6Q-A)					
M30843FHFP	PRQP0100JB-A (100P6S-A)					
M30845FWGP	PLQP0144KA-A (144P6Q-A)	320K+4K				
M30843FWGP	PLQP0100KB-A (100P6Q-A)					
M30845MW-XXXGP	PLQP0144KA-A (144P6Q-A)	320K				
M30843MW-XXXGP	PLQP0100KB-A (100P6Q-A)					
M30843MW-XXXFP	PRQP0100JB-A (100P6S-A)					
M30842ME-XXXGP	PLQP0144KA-A (144P6Q-A)	192K	16K	Mask ROM		
M30840ME-XXXGP	PLQP0100KB-A (100P6Q-A)					
M30840ME-XXXFP	PRQP0100JB-A (100P6S-A)					
M30842MC-XXXGP	PLQP0144KA-A (144P6Q-A)	128K				
M30840MC-XXXGP	PLQP0100KB-A (100P6Q-A)					
M30840MC-XXXFP	PRQP0100JB-A (100P6S-A)					
M30842SGP (D)	PLQP0144KA-A (144P6Q-A)	---			10K	ROMless
M30840SGP (D)	PLQP0100KB-A (100P6Q-A)					
M30840SFP (D)	PRQP0100JB-A (100P6S-A)					

(D): Under Development

Table 1.3 M32C/84 Group (2) (T Version, M32C/84T)

As of July, 2005

Type Number	Package	ROM Capacity	RAM Capacity	Remarks
M30845FJTGP	PLQP0144KA-A (144P6Q-A)	512K+4K	24K	Flash Memory T Version (High-releability 85° C Version)
M30843FJTGP	PLQP0100KB-A (100P6Q-A)			
M30845FHTGP	PLQP0144KA-A (144P6Q-A)	384K+4K		
M30843FHTGP	PLQP0100KB-A (100P6Q-A)			
M30843FWTGP	PLQP0100KB-A (100P6Q-A)	320K+4K		
M30842MCT-XXXGP (D)	PLQP0144KA-A (144P6Q-A)	128K	10K	Mask ROM
M30840MCT-XXXGP (D)	PLQP0100KB-A (100P6Q-A)			

(D): Under Development

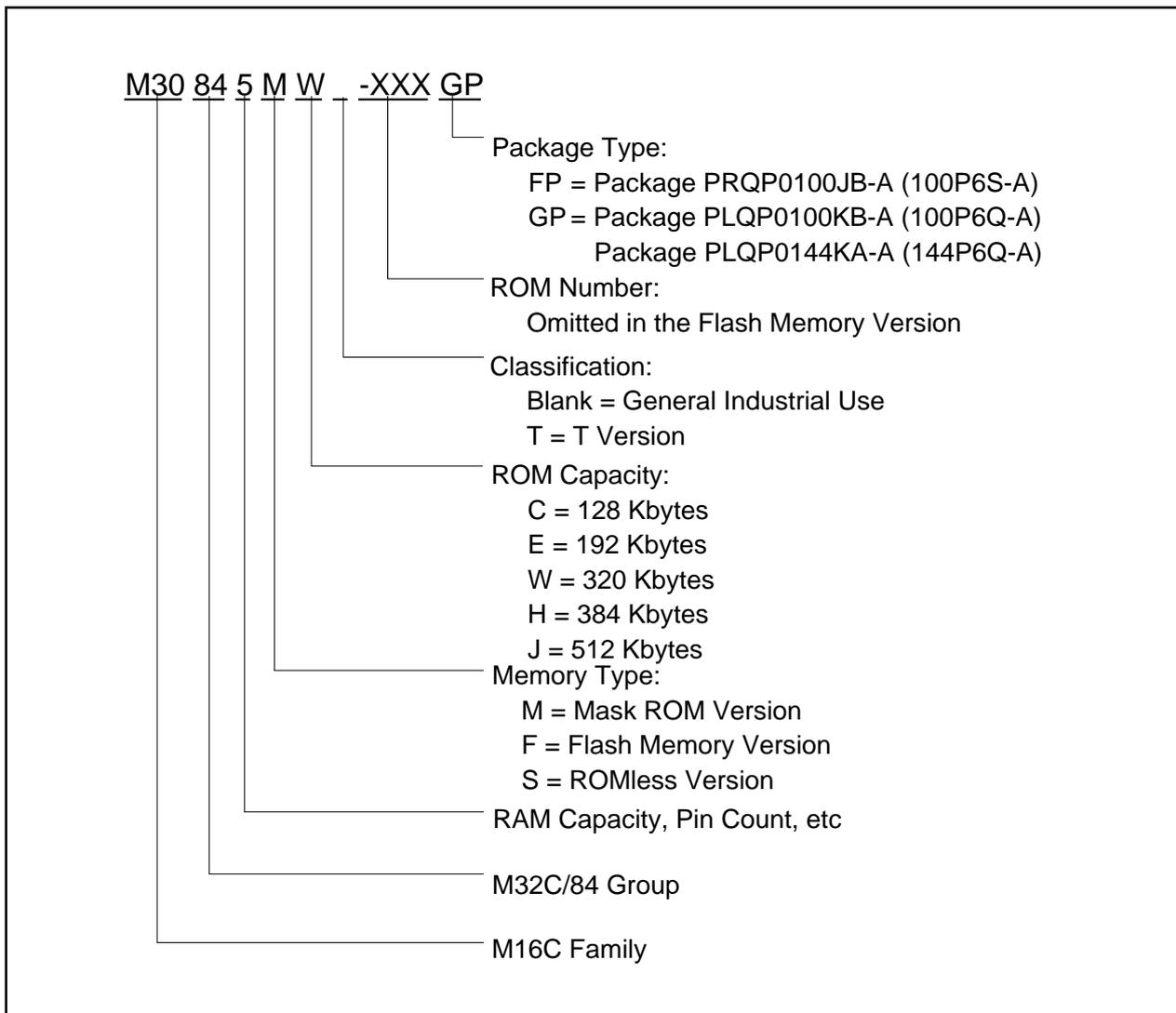


Figure 1.2 Product Numbering System

1.5 Pin Assignments and Descriptions

Figures 1.3 to 1.5 show pin assignments (top view).

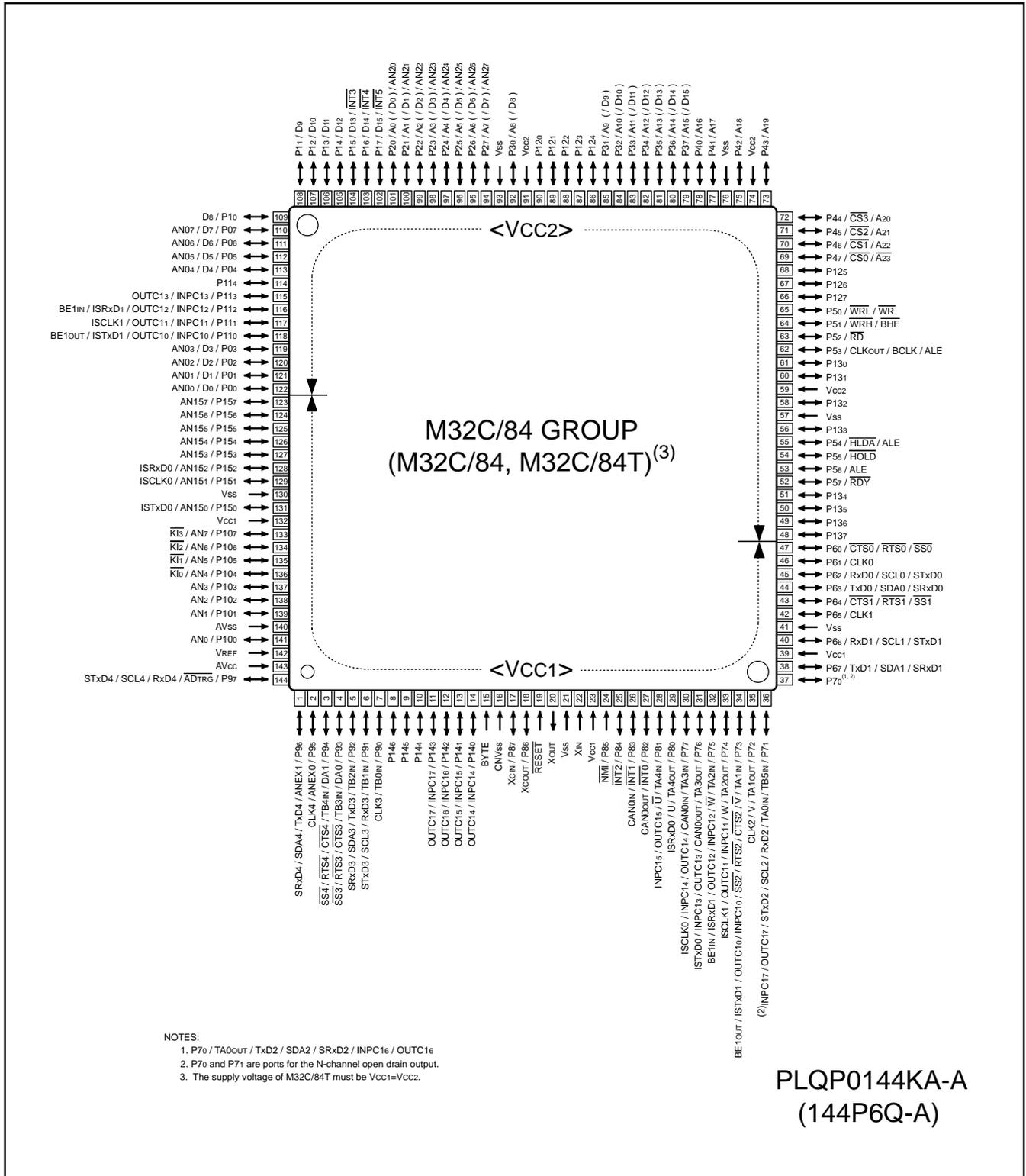


Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
1		P96			TxD4/SDA4/SRx4D4		ANEX1	
2		P95			CLK4		ANEX0	
3		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5		P92		TB2IN	TxD3/SDA3/SRx3D3			
6		P91		TB1IN	RxD3/SCL3/STxD3			
7		P90		TB0IN	CLK3			
8		P146						
9		P145						
10		P144						
11		P143				INPC17/OUTC17		
12		P142				INPC16/OUTC16		
13		P141				INPC15/OUTC15		
14		P140				INPC14/OUTC14		
15	BYTE							
16	CNVSS							
17	X _{CIN}	P87						
18	X _{COU}	P86						
19	RESET							
20	X _{OUT}							
21	V _{SS}							
22	X _{IN}							
23	V _{CC1}							
24		P85	NMI					
25		P84	INT2					
26		P83	INT1		CAN0IN			
27		P82	INT0		CAN0OUT			
28		P81		TA4IN/U		INPC15/OUTC15		
29		P80		TA4OUT/U		ISRxD0		
30		P77		TA3IN	CAN0IN	INPC14/OUTC14/ISCLK0		
31		P76		TA3OUT	CAN0OUT	INPC13/OUTC13/ISTxD0		
32		P75		TA2IN/W		INPC12/OUTC12/ISRxD1/BE1IN		
33		P74		TA2OUT/W		INPC11/OUTC11/ISCLK1		
34		P73		TA1IN/V	CTS2/RTS2/SS2	INPC10/OUTC10/ISTxD1/BE1OUT		
35		P72		TA1OUT/V	CLK2			
36		P71		TB5IN/TA0IN	RxD2/SCL2/STxD2	INPC17/OUTC17		
37		P70		TA0OUT	TxD2/SDA2/SRx2D2	INPC16/OUTC16		
38		P67			TxD1/SDA1/SRx1D1			
39	V _{CC1}							
40		P66			RxD1/SCL1/STxD1			
41	V _{SS}							
42		P65			CLK1			
43		P64			CTS1/RTS1/SS1			
44		P63			TxD0/SDA0/SRx0D0			
45		P62			RxD0/SCL0/STxD0			
46		P61			CLK0			
47		P60			CTS0/RTS0/SS0			
48		P137						

NOTES:

1. Bus control pins in M32C/84T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
49		P13 ₆						
50		P13 ₅						
51		P13 ₄						
52		P5 ₇						$\overline{\text{RDY}}$
53		P5 ₆						$\overline{\text{ALE}}$
54		P5 ₅						$\overline{\text{HOLD}}$
55		P5 ₄						$\overline{\text{HLDA/ALE}}$
56		P13 ₃						
57	V _{SS}							
58		P13 ₂						
59	V _{CC2}							
60		P13 ₁						
61		P13 ₀						
62		P5 ₃						$\overline{\text{CLKOUT/BCLK/ALE}}$
63		P5 ₂						$\overline{\text{RD}}$
64		P5 ₁						$\overline{\text{WRH/BHE}}$
65		P5 ₀						$\overline{\text{WRL/WR}}$
66		P12 ₇						
67		P12 ₆						
68		P12 ₅						
69		P4 ₇						$\overline{\text{CS0/A23}}$
70		P4 ₆						$\overline{\text{CS1/A22}}$
71		P4 ₅						$\overline{\text{CS2/A21}}$
72		P4 ₄						$\overline{\text{CS3/A20}}$
73		P4 ₃						A ₁₉
74	V _{CC2}							
75		P4 ₂						A ₁₈
76	V _{SS}							
77		P4 ₁						A ₁₇
78		P4 ₀						A ₁₆
79		P3 ₇						A ₁₅ (/D ₁₅)
80		P3 ₆						A ₁₄ (/D ₁₄)
81		P3 ₅						A ₁₃ (/D ₁₃)
82		P3 ₄						A ₁₂ (/D ₁₂)
83		P3 ₃						A ₁₁ (/D ₁₁)
84		P3 ₂						A ₁₀ (/D ₁₀)
85		P3 ₁						A ₉ (/D ₉)
86		P12 ₄						
87		P12 ₃						
88		P12 ₂						
89		P12 ₁						
90		P12 ₀						
91	V _{CC2}							
92		P3 ₀						A ₈ (/D ₈)
93	V _{SS}							
94		P2 ₇					AN2 ₇	A ₇ (/D ₇)
95		P2 ₆					AN2 ₆	A ₆ (/D ₆)
96		P2 ₅					AN2 ₅	A ₅ (/D ₅)

NOTES:

1. Bus control pins in M32C/84T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
97		P24					AN24	A4(/D4)
98		P23					AN23	A3(/D3)
99		P22					AN22	A2(/D2)
100		P21					AN21	A1(/D1)
101		P20					AN20	A0(/D0)
102		P17	$\overline{\text{INT5}}$					D15
103		P16	$\overline{\text{INT4}}$					D14
104		P15	$\overline{\text{INT3}}$					D13
105		P14						D12
106		P13						D11
107		P12						D10
108		P11						D9
109		P10						D8
110		P07					AN07	D7
111		P06					AN06	D6
112		P05					AN05	D5
113		P04					AN04	D4
114		P114						
115		P113				INPC13/OUTC13		
116		P112				INPC12/OUTC12/ISRxD1/BE1IN		
117		P111				INPC11/OUTC11/ISCLK1		
118		P110				INPC10/OUTC10/ISTxD1/BE1OUT		
119		P03					AN03	D3
120		P02					AN02	D2
121		P01					AN01	D1
122		P00					AN00	D0
123		P157					AN157	
124		P156					AN156	
125		P155					AN155	
126		P154					AN154	
127		P153					AN153	
128		P152				ISRxD0	AN152	
129		P151				ISCLK0	AN151	
130	Vss							
131		P150				ISTxD0	AN150	
132	VCC1							
133		P107	$\overline{\text{KI3}}$				AN7	
134		P106	$\overline{\text{KI2}}$				AN6	
135		P105	$\overline{\text{KI1}}$				AN5	
136		P104	$\overline{\text{KI0}}$				AN4	
137		P103					AN3	
138		P102					AN2	
139		P101					AN1	
140	AVss							
141		P100					AN0	
142	VREF							
143	AVCC							
144		P97			RxD4/SCL4/STxD4		$\overline{\text{ADTRG}}$	

NOTES:

1. Bus control pins in M32C/84T cannot be used.

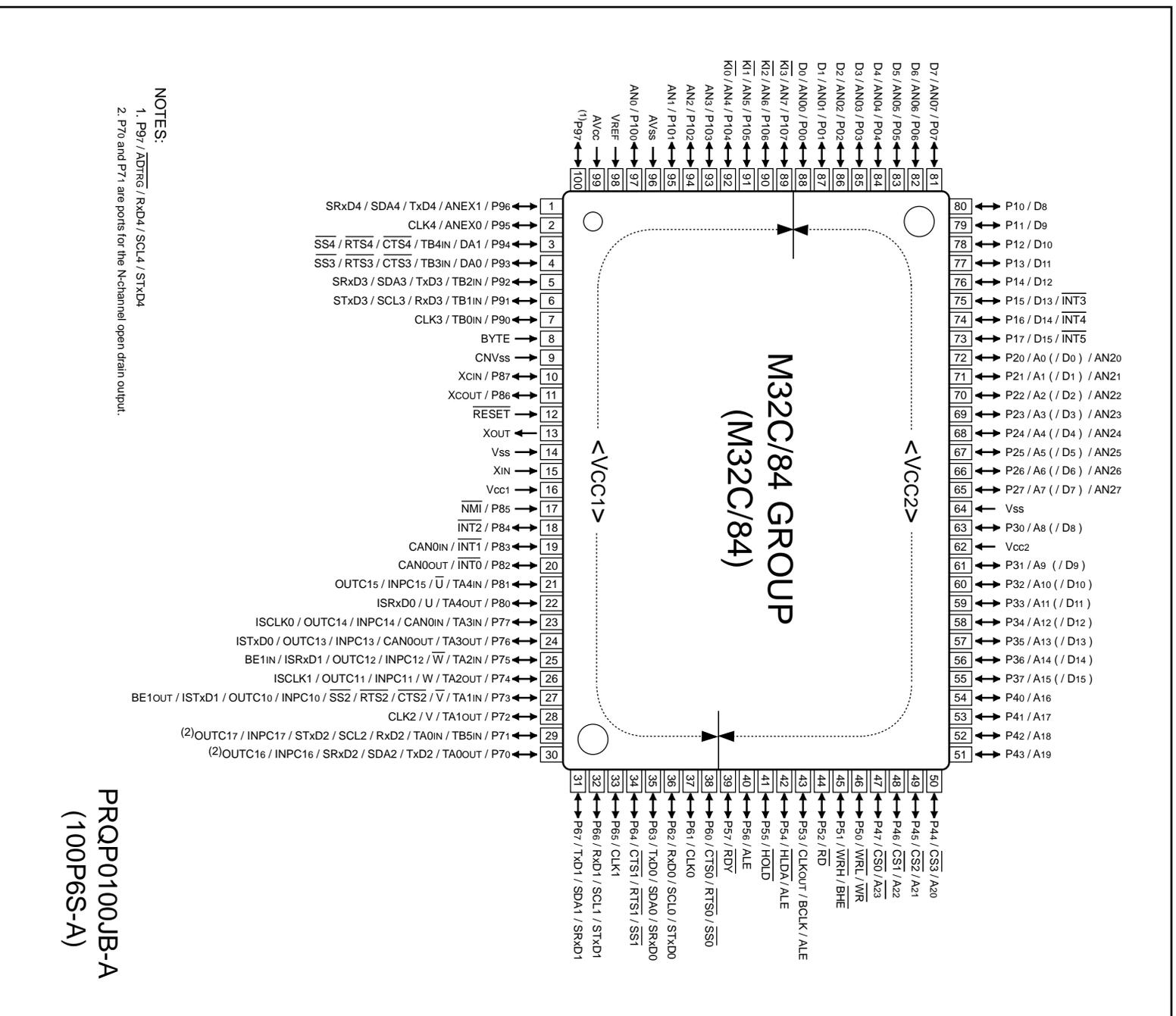


Figure 1.4 Pin Assignment for 100-Pin Package

**PRQP0100JB-A
(100P6S-A)**

NOTES:

1. P97 / ADTRG / RxD4 / SCL4 / STxD4
2. P70 and P71 are ports for the N-channel open drain output.

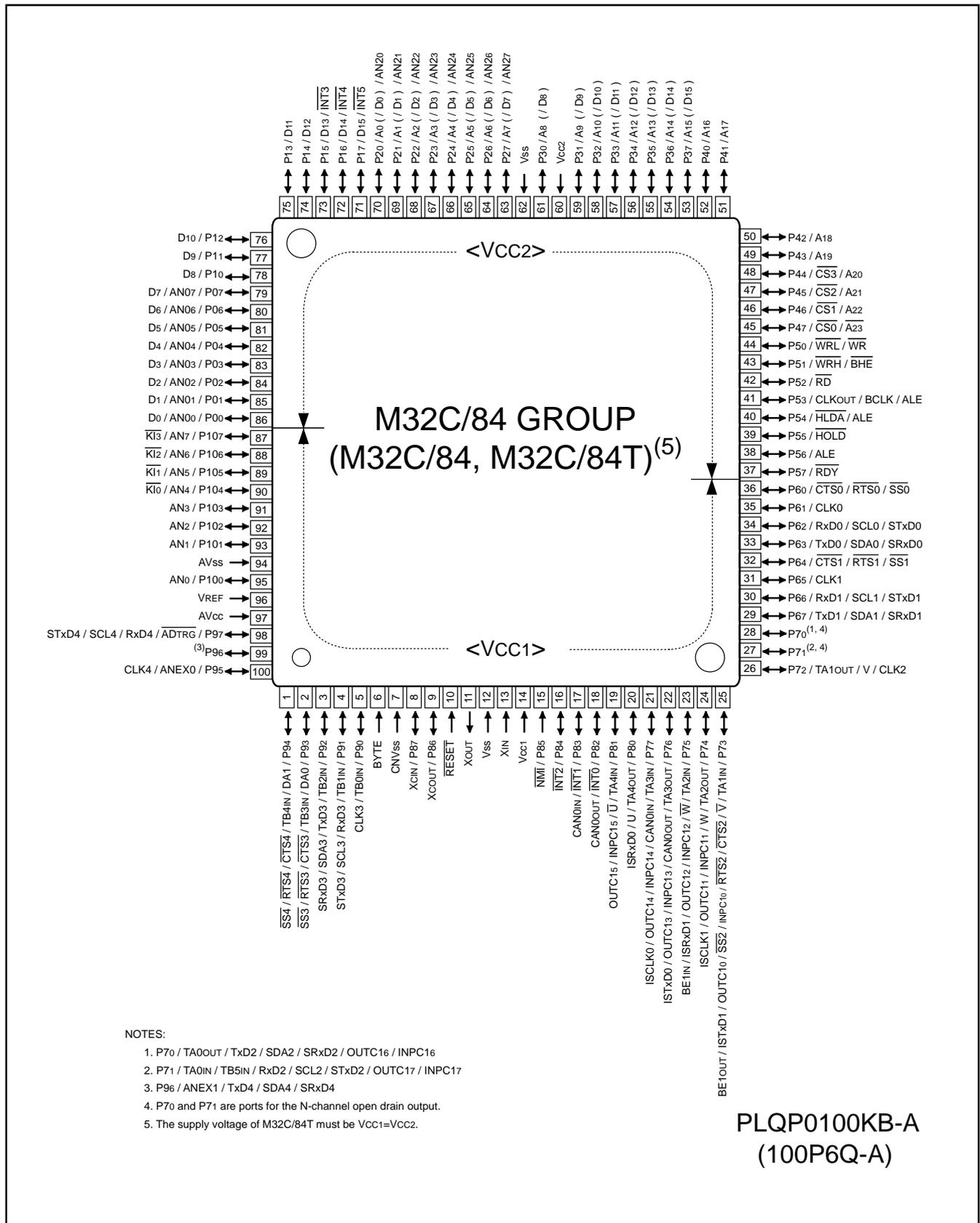


Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
FP	GP								
1	99		P96			TxD4/SDA4/SRx4D4		ANEX1	
2	100		P95			CLK4		ANEX0	
3	1		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P92		TB2IN	TxD3/SDA3/SRx4D3			
6	4		P91		TB1IN	RxD3/SCL3/STxD3			
7	5		P90		TB0IN	CLK3			
8	6	BYTE							
9	7	CNV _{SS}							
10	8	XCIN	P87						
11	9	XCOUT	P86						
12	10	RESET							
13	11	XOUT							
14	12	V _{SS}							
15	13	XIN							
16	14	V _{CC1}							
17	15		P85	NMI					
18	16		P84	INT2					
19	17		P83	INT1		CAN0IN			
20	18		P82	INT0		CAN0OUT			
21	19		P81		TA4IN/ \bar{U}		INPC15/OUTC15		
22	20		P80		TA4OUT/U		ISRxD0		
23	21		P77		TA3IN	CAN0IN	INPC14/OUTC14/ISCLK0		
24	22		P76		TA3OUT	CAN0OUT	INPC13/OUTC13/ISTxD0		
25	23		P75		TA2IN/ \bar{W}		INPC12/OUTC12/ISRxD1/BE1IN		
26	24		P74		TA2OUT/W		INPC11/OUTC11/ISCLK1		
27	25		P73		TA1IN/ \bar{V}	CTS2/RTS2/SS2	INPC10/OUTC10/ISTxD1/BE1OUT		
28	26		P72		TA1OUT/V	CLK2			
29	27		P71		TB5IN/TA0IN	RxD2/SCL2/STxD2	INPC17/OUTC17		
30	28		P70		TA0OUT	TxD2/SDA2/SRx4D2	INPC16/OUTC16		
31	29		P67			TxD1/SDA1/SRx4D1			
32	30		P66			RxD1/SCL1/STxD1			
33	31		P65			CLK1			
34	32		P64			CTS1/RTS1/SS1			
35	33		P63			TxD0/SDA0/SRx4D0			
36	34		P62			RxD0/SCL0/STxD0			
37	35		P61			CLK0			
38	36		P60			CTS0/RTS0/SS0			
39	37		P57						RDY
40	38		P56						ALE
41	39		P55						HOLD
42	40		P54						HLD/ALE
43	41		P53						CLKOUT/BCLK/ALE
44	42		P52						RD
45	43		P51						WRH/BHE
46	44		P50						WRL/WR
47	45		P47						CS0/A23
48	46		P46						CS1/A22
49	47		P45						CS2/A21
50	48		P44						CS3/A20

NOTES:

1. Bus control pins in M32C/84T cannot be used.

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
51	49		P43						A19
52	50		P42						A18
53	51		P41						A17
54	52		P40						A16
55	53		P37						A15(/D15)
56	54		P36						A14(/D14)
57	55		P35						A13(/D13)
58	56		P34						A12(/D12)
59	57		P33						A11(/D11)
60	58		P32						A10(/D10)
61	59		P31						A9(/D9)
62	60	Vcc2							
63	61		P30						A8(/D8)
64	62	Vss							
65	63		P27				AN27		A7(/D7)
66	64		P26				AN26		A6(/D6)
67	65		P25				AN25		A5(/D5)
68	66		P24				AN24		A4(/D4)
69	67		P23				AN23		A3(/D3)
70	68		P22				AN22		A2(/D2)
71	69		P21				AN21		A1(/D1)
72	70		P20				AN20		A0(/D0)
73	71		P17	$\overline{\text{INT5}}$					D15
74	72		P16	$\overline{\text{INT4}}$					D14
75	73		P15	$\overline{\text{INT3}}$					D13
76	74		P14						D12
77	75		P13						D11
78	76		P12						D10
79	77		P11						D9
80	78		P10						D8
81	79		P07				AN07		D7
82	80		P06				AN06		D6
83	81		P05				AN05		D5
84	82		P04				AN04		D4
85	83		P03				AN03		D3
86	84		P02				AN02		D2
87	85		P01				AN01		D1
88	86		P00				AN00		D0
89	87		P107	$\overline{\text{KI3}}$			AN7		
90	88		P106	$\overline{\text{KI2}}$			AN6		
91	89		P105	$\overline{\text{KI1}}$			AN5		
92	90		P104	$\overline{\text{KI0}}$			AN4		
93	91		P103				AN3		
94	92		P102				AN2		
95	93		P101				AN1		
96	94	AVss							
97	95		P100				AN0		
98	96	VREF							
99	97	AVcc							
100	98		P97			RxD4/SCL4/STxD4	$\overline{\text{ADTRG}}$		

NOTES:

1. Bus control pins in M32C/84T cannot be used.

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Classification	Symbol	I/O Type	Supply Voltage	Function
Power Supply	VCC1, VCC2 VSS	I	–	Apply 3.0 to 5.5V to both VCC1 and VCC2 pins. Apply 0V to the VSS pin. $V_{CC1} \geq V_{CC2}$ ^(1, 2)
Analog Power Supply	AVCC AVSS	I	VCC1	Supplies power to the A/D converter. Connect the AVCC pin to VCC1 and the AVSS pin to VSS
Reset Input	RESET	I	VCC1	The microcomputer is in a reset state when "L" is applied to the RESET pin
CNVss	CNVss	I	VCC1	Switches processor mode. Connect the CNVss pin to VSS to start up in single-chip mode or to VCC1 to start up in microprocessor mode
Input to Switch External Data Bus Width ⁽³⁾	BYTE	I	VCC1	Switches data bus width in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when it is held "H". Set to either. Connect the BYTE pin to VSS to use the microcomputer in single-chip mode
Bus Control Pins ⁽³⁾	D0 to D7	I/O	VCC2	Inputs and outputs data (D0 to D7) while accessing an external memory space with separate bus
	D8 to D15	I/O	VCC2	Inputs and outputs data (D8 to D15) while accessing an external memory space with 16-bit separate bus
	A0 to A22	O	VCC2	Outputs address bits A0 to A22
	$\overline{A}23$	O	VCC2	Outputs inversed address bit A23
	A0/D0 to A7/D7	I/O	VCC2	Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	VCC2	Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing while accessing an external memory space with 16-bit multiplexed bus
	CS0 to CS3	O	VCC2	Outputs CS0 to CS3 that are chip-select signals specifying an external space
	$\overline{W}RL$ / $\overline{W}R$ $\overline{W}RH$ / $\overline{B}HE$ $\overline{R}D$	O	VCC2	Outputs $\overline{W}RL$, $\overline{W}RH$, ($\overline{W}R$, $\overline{B}HE$) and $\overline{R}D$ signals. $\overline{W}RL$ and $\overline{W}RH$ can be switched with $\overline{W}R$ and $\overline{B}HE$ by program <ul style="list-style-type: none"> ■ $\overline{W}RL$, $\overline{W}RH$ and $\overline{R}D$ selected: If external data bus is 16 bits wide, data is written to an even address in external memory space when $\overline{W}RL$ is held "L". Data is written to an odd address when $\overline{W}RH$ is held "L". Data is read when $\overline{R}D$ is held "L". ■ $\overline{W}R$, $\overline{B}HE$ and $\overline{R}D$ selected: Data is written to external memory space when $\overline{W}R$ is held "L". Data in an external memory space is read when $\overline{R}D$ is held "L". An odd address is accessed when $\overline{B}HE$ is held "L". Select $\overline{W}R$, $\overline{B}HE$ and $\overline{R}D$ for external 8-bit data bus.
	ALE	O	VCC2	ALE is a signal latching the address
	HOLD	I	VCC2	The microcomputer is placed in a hold state while the HOLD pin is held "L"
HLDA	O	VCC2	Outputs an "L" signal while the microcomputer is placed in a hold state	
RDY	I	VCC2	Bus is placed in a wait state while the $\overline{R}DY$ pin is held "L"	

I : Input O : Output I/O : Input and output

NOTES:

1. VCC1 is hereinafter referred to as VCC unless otherwise noted.
2. Apply 4.2 to 5.5V to the VCC1 and VCC2 pins when using M32C/84T. $V_{CC1}=V_{CC2}$.
3. Bus control pins in M32C/84T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Supply Voltage	Function
Main Clock Input	XIN	I	VCC1	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open
Main Clock Output	XOUT	O	VCC1	
Sub Clock Input	XCIN	I	VCC1	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and Xcout. To apply external clock, apply it to XCIN and leave Xcout open
Sub Clock Output	Xcout	O	VCC1	
BCLK Output ⁽¹⁾	BCLK	O	VCC2	Outputs BCLK signal
Clock Output	CLKOUT	O	VCC2	Outputs the clock having the same frequency as fc, f8 or f32
INT Interrupt Input	INT0 to INT2	I	VCC1	Input pins for the INT interrupt
	INT3 to INT5	I	VCC2	
NMI Interrupt Input	NMI	I	VCC1	Input pin for the NMI interrupt
Key Input Interrupt	KI0 to KI3	I	VCC1	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	Input pins for the timer A0 to A4
Timer B	TB0IN to TB5IN	I	VCC1	Input pins for the timer B0 to B5
Three-phase Motor Control Timer Output	U, \bar{U} , V, \bar{V} , W, \bar{W}	O	VCC1	Output pins for the three-phase motor control timer
Serial I/O	CTS0 to CTS4	I	VCC1	Input pins for data transmission control
	RTS0 to RTS4	O	VCC1	Output pins for data reception control
	CLK0 to CLK4	I/O	VCC1	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	VCC1	Inputs serial data
	TxD0 to TxD4	O	VCC1	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I ² C Mode	SDA0 to SDA4	I/O	VCC1	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4	I/O	VCC1	Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)
Serial I/O Special Function	STxD0 to STxD4	O	VCC1	Outputs serial data when slave mode is selected (STxD2 is a pin for the N-channel open drain output.)
	SRxD0 to SRxD4	I	VCC1	Inputs serial data when slave mode is selected
	SS0 to SS4	I	VCC1	Input pins to control serial I/O special function

I : Input O : Output I/O : Input and output

NOTES:

1. Bus control pins in M32C/84T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Supply Voltage	Function
Reference Voltage Input	VREF	I	-	Applies reference voltage to the A/D converter and D/A converter
A/D Converter	AN0 to AN7 AN00 to AN07 AN20 to AN27	I	VCC1	Analog input pins for the A/D converter
	ADTRG	I	VCC1	Input pin for an external A/D trigger
	ANEX0	I/O	VCC1	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode
	ANEX1	I	VCC1	Extended analog input pin for the A/D converter
	D/A Converter	DA0, DA1	O	VCC1
Intelligent I/O	INPC10 to INPC13	I	VCC1/VCC2 ⁽¹⁾	Input pins for the time measurement function
	INPC14 to INPC17	I	VCC1	
	OUTC10 to OUTC13	O	VCC1/VCC2 ⁽¹⁾	Output pins for the waveform generating function (OUTC16 and OUTC17 assigned to P70 and P71 are pins for the N-channel open drain output.)
	OUTC14 to OUTC17	O	VCC1	
	ISCLK0	I/O	VCC1	Inputs and outputs the clock for the intelligent I/O communication function
	ISCLK1	I/O	VCC1/VCC2 ⁽¹⁾	
	ISRXD0	I	VCC1	Inputs data for the intelligent I/O communication function
	ISRXD1	I	VCC1/VCC2 ⁽¹⁾	
	ISTXD0	O	VCC1	Outputs data for the intelligent I/O communication function
	ISTXD1	O	VCC1/VCC2 ⁽¹⁾	
	BE1IN	I	VCC1/VCC2 ⁽¹⁾	Inputs data for the intelligent I/O communication function
	BE1OUT	O	VCC1/VCC2 ⁽¹⁾	Outputs data for the intelligent I/O communication function
CAN	CAN0IN	I	VCC1	Input pin for the CAN communication function
	CAN0OUT	O	VCC1	Output pin for the CAN communication function
I/O Ports	P00 to P07 P10 to P17 P20 to P27 P30 to P37 P40 to P47 P50 to P57	I/O	VCC2	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units
	P60 to P67 P70 to P77 P90 to P97 P100 to P107	I/O	VCC1	I/O ports having equivalent functions to P0 (P70 and P71 are ports for the N-channel open drain output.)
	P80 to P84 P86, P87	I/O	VCC1	I/O ports having equivalent functions to P0
Input Port	P85	I	VCC1	Shares a pin with NMI. NMI input state can be got by reading P85

I : Input O : Output I/O : Input and output

NOTES:

1. VCC2 is not available in the 100-pin package. VCC1 only available.

Table 1.6 Pin Description (144-Pin Package only) (Continued)

Classification	Symbol	I/O Type	Supply Voltage	Function
A/D Converter	AN150 to AN157	I	VCC1	Analog input pins for the A/D converter
I/O Ports	P110 to P114 P120 to P127 P130 to P137	I/O	VCC2	I/O ports having equivalent functions to P0
	P140 to P146 P150 to P157	I/O	VCC1	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.

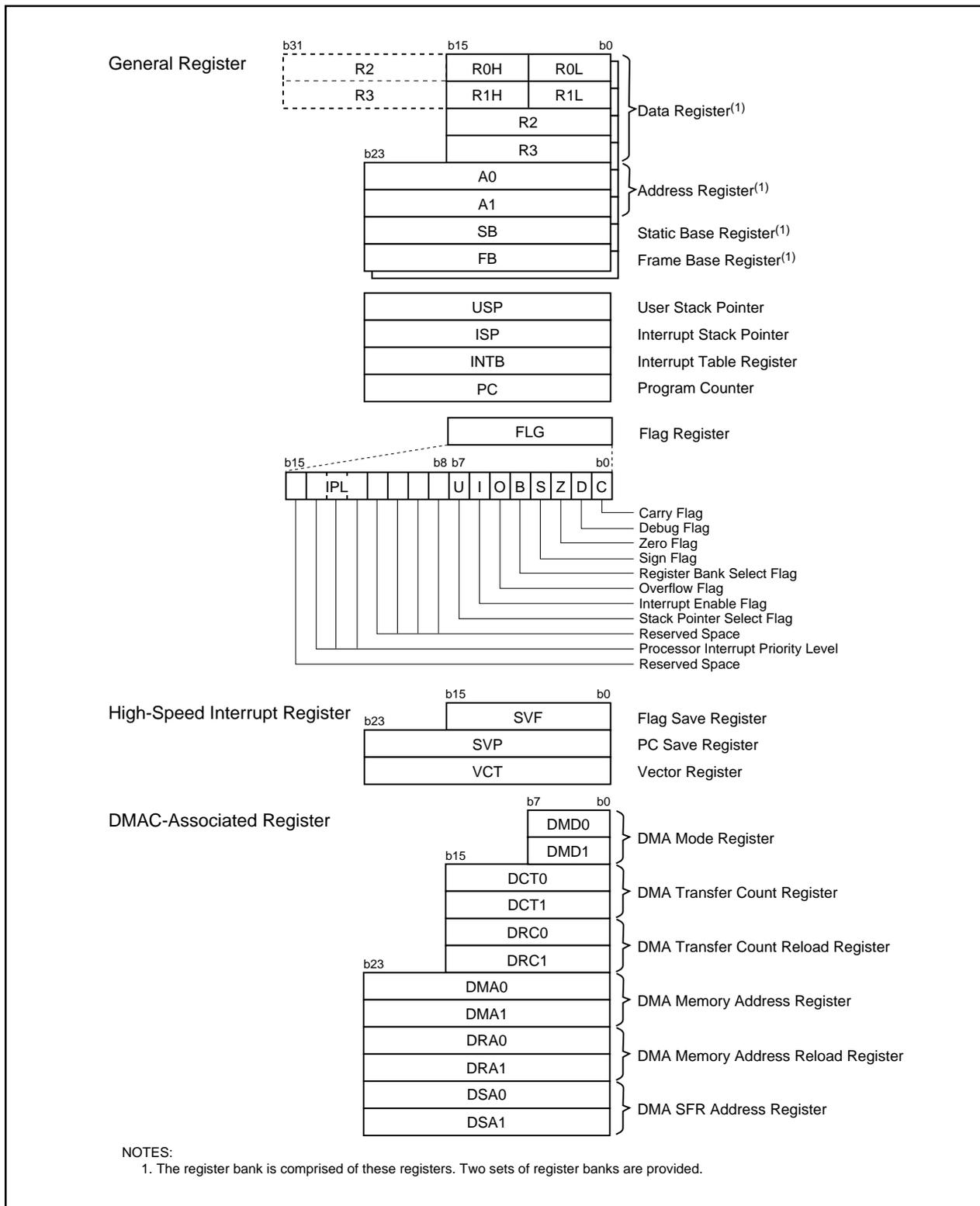


Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an relocatable interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic operation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic operation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

Interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".

The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When reading, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

Refer to **11.4 High-Speed Interrupt** for details.

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows:

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

Refer to **13. DMAC** for details.

3. Memory

Figure 3.1 shows a memory map of the M32C/84 group (M32C/84, M32C/84T).

The M32C/84 group (M32C/84, M32C/84T) provides 16-Mbyte address space from addresses 000000_{16} to $FFFFFF_{16}$.

The internal ROM is allocated lower addresses beginning with address $FFFFFF_{16}$. For example, a 64-Kbyte internal ROM is allocated in addresses $FF0000_{16}$ to $FFFFFF_{16}$.

The fixed interrupt vectors are allocated addresses $FFFFDC_{16}$ to $FFFFFF_{16}$. It stores the starting address of each interrupt routine. Refer to **11. Interrupt** for details.

The internal RAM is allocated higher addresses beginning with address 000400_{16} . For example, a 10-Kbyte internal RAM is allocated addresses 000400_{16} to $002BFF_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, and timers, is allocated addresses 000000_{16} to $0003FF_{16}$. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vectors are allocated addresses $FFFE00_{16}$ to $FFFFDB_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M32C/80 Series Software Manual** for details. In memory expansion mode and microprocessor mode, some spaces are reserved and cannot be accessed by users.

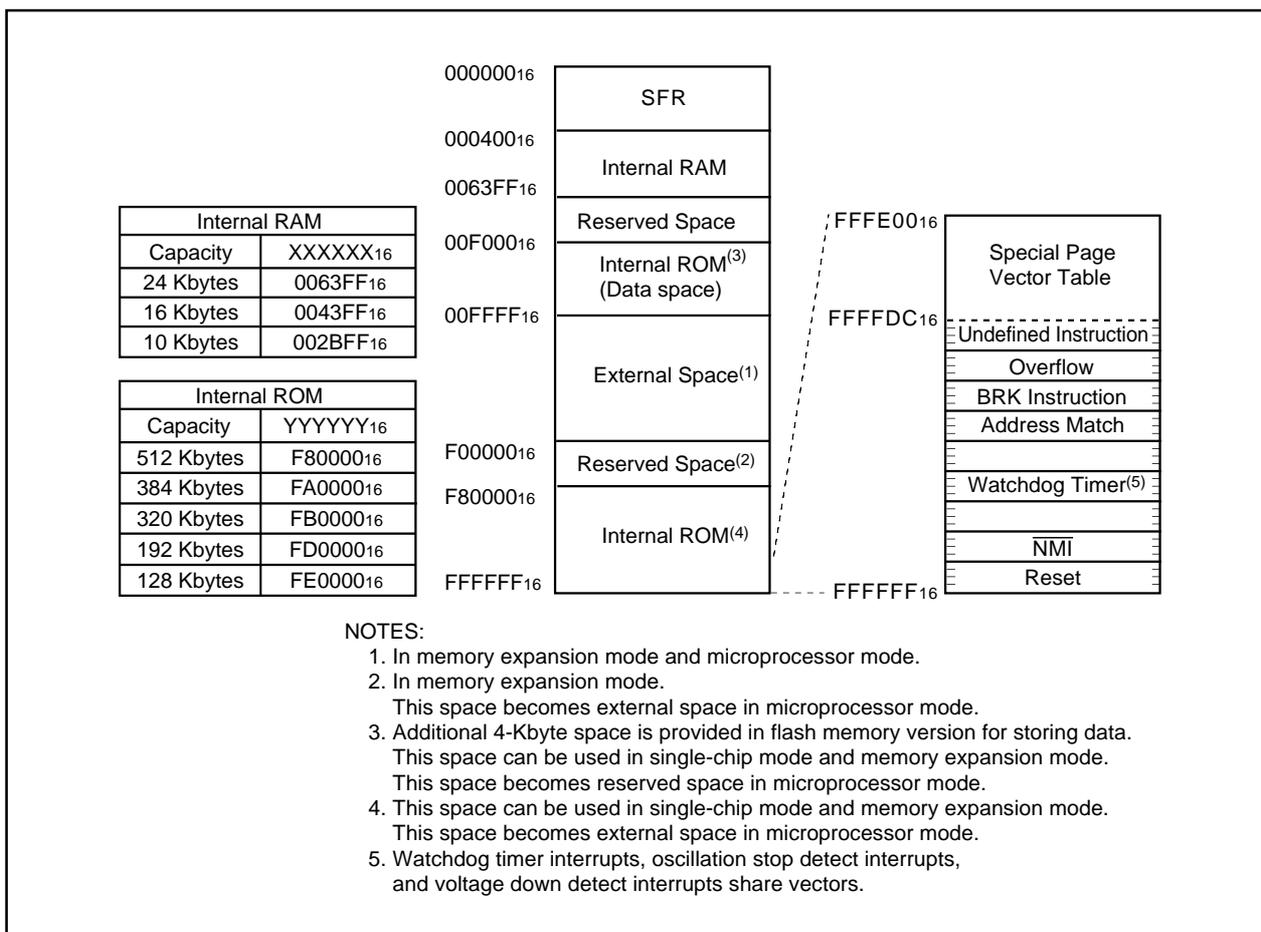


Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor Mode Register 0 ⁽¹⁾	PM0	1000 0000 ₂ (CNVss pin ="L") 0000 0011 ₂ (CNVss pin ="H")
0005 ₁₆	Processor Mode Register 1	PM1	00 ₁₆
0006 ₁₆	System Clock Control Register 0	CM0	0000 1000 ₂
0007 ₁₆	System Clock Control Register 1	CM1	0010 0000 ₂
0008 ₁₆			
0009 ₁₆	Address Match Interrupt Enable Register	AIER	00 ₁₆
000A ₁₆	Protect Register	PRCR	XXXX 0000 ₂
000B ₁₆	External Data Bus Width Control Register ⁽²⁾	DS	XXXX 1000 ₂ (BYTE pin ="L") XXXX 0000 ₂ (BYTE pin ="H")
000C ₁₆	Main Clock Division Register	MCD	XXX0 1000 ₂
000D ₁₆	Oscillation Stop Detection Register	CM2	00 ₁₆
000E ₁₆	Watchdog Timer Start Register	WDTS	XX ₁₆
000F ₁₆	Watchdog Timer Control Register	WDC	000X XXXX ₂
0010 ₁₆			
0011 ₁₆			
0012 ₁₆	Address Match Interrupt Register 0	RMAD0	000000 ₁₆
0013 ₁₆	Processor Mode Register 2	PM2	00 ₁₆
0014 ₁₆			
0015 ₁₆			
0016 ₁₆	Address Match Interrupt Register 1	RMAD1	000000 ₁₆
0017 ₁₆	Voltage Detection Register 2 ⁽²⁾	VCR2	00 ₁₆
0018 ₁₆			
0019 ₁₆			
001A ₁₆	Address Match Interrupt Register 2	RMAD2	000000 ₁₆
001B ₁₆	Voltage Detection Register 1 ⁽²⁾	VCR1	0000 1000 ₂
001C ₁₆			
001D ₁₆			
001E ₁₆	Address Match Interrupt Register 3	RMAD3	000000 ₁₆
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆	PLL Control Register 0	PLC0	0001 X010 ₂
0027 ₁₆	PLL Control Register 1	PLC1	000X 0000 ₂
0028 ₁₆			
0029 ₁₆			
002A ₁₆	Address Match Interrupt Register 4	RMAD4	000000 ₁₆
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆	Address Match Interrupt Register 5	RMAD5	000000 ₁₆
002F ₁₆	Voltage Down Detection Interrupt Register ⁽²⁾	D4INT	00 ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The PM01 and PM00 bits in the PM1 register maintain values set before reset even if software reset or watchdog timer reset is performed.
2. These registers in M32C/84T cannot be used.

Address	Register	Symbol	Value after RESET
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆ 0039 ₁₆ 003A ₁₆	Address Match Interrupt Register 6	RMAD6	000000 ₁₆
003B ₁₆			
003C ₁₆ 003D ₁₆ 003E ₁₆	Address Match Interrupt Register 7	RMAD7	000000 ₁₆
003F ₁₆			
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆			
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆	External Space Wait Control Register 0 ⁽¹⁾	EWCR0	X0X0 0011 ₂
0049 ₁₆	External Space Wait Control Register 1 ⁽¹⁾	EWCR1	X0X0 0011 ₂
004A ₁₆	External Space Wait Control Register 2 ⁽¹⁾	EWCR2	X0X0 0011 ₂
004B ₁₆	External Space Wait Control Register 3 ⁽¹⁾	EWCR3	X0X0 0011 ₂
004C ₁₆	Page Mode Wait Control Register 0 ⁽²⁾	PWCR0	0001 0001 ₂
004D ₁₆	Page Mode Wait Control Register 1 ⁽²⁾	PWCR1	0001 0001 ₂
004E ₁₆			
004F ₁₆			
0050 ₁₆			
0051 ₁₆			
0052 ₁₆			
0053 ₁₆			
0054 ₁₆			
0055 ₁₆	Flash Memory Control Register 1	FMR1	0000 0101 ₂
0056 ₁₆			
0057 ₁₆	Flash Memory Control Register 0	FMRO	0000 0001 ₂ (Flash memory version) XXXX XXX0 ₂ (Masked ROM version)
0058 ₁₆			
0059 ₁₆			
005A ₁₆			
005B ₁₆			
005C ₁₆			
005D ₁₆			
005E ₁₆			
005F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. These registers in M32C/84T cannot be used.
2. These registers can be used only in the ROMless version.

Address	Register	Symbol	Value after RESET
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆	DMA0 Interrupt Control Register	DM0IC	XXXX X0002
0069 ₁₆	Timer B5 Interrupt Control Register	TB5IC	XXXX X0002
006A ₁₆	DMA2 Interrupt Control Register	DM2IC	XXXX X0002
006B ₁₆	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X0002
006C ₁₆	Timer A0 Interrupt Control Register	TA0IC	XXXX X0002
006D ₁₆	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X0002
006E ₁₆	Timer A2 Interrupt Control Register	TA2IC	XXXX X0002
006F ₁₆	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X0002
0070 ₁₆	Timer A4 Interrupt Control Register	TA4IC	XXXX X0002
0071 ₁₆	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X0002
0072 ₁₆	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X0002
0073 ₁₆	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X0002
0074 ₁₆	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X0002
0075 ₁₆	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X0002
0076 ₁₆	Timer B1 Interrupt Control Register	TB1IC	XXXX X0002
0077 ₁₆	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X0002
0078 ₁₆	Timer B3 Interrupt Control Register	TB3IC	XXXX X0002
0079 ₁₆	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X0002
007A ₁₆	INT5 Interrupt Control Register	INT5IC	XX00 X0002
007B ₁₆			
007C ₁₆	INT3 Interrupt Control Register	INT3IC	XX00 X0002
007D ₁₆	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X0002
007E ₁₆	INT1 Interrupt Control Register	INT1IC	XX00 X0002
007F ₁₆	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC CAN1IC	XXXX X0002
0080 ₁₆			
0081 ₁₆	CAN Interrupt 2 Control Register	CAN2IC	XXXX X0002
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆			
0087 ₁₆			
0088 ₁₆	DMA1 Interrupt Control Register	DM1IC	XXXX X0002
0089 ₁₆	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X0002
008A ₁₆	DMA3 Interrupt Control Register	DM3IC	XXXX X0002
008B ₁₆	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X0002
008C ₁₆	Timer A1 Interrupt Control Register	TA1IC	XXXX X0002
008D ₁₆	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X0002
008E ₁₆	Timer A3 Interrupt Control Register	TA3IC	XXXX X0002
008F ₁₆	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0090 ₁₆	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X0002
0091 ₁₆	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X0002
0092 ₁₆	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X0002
0093 ₁₆	Key Input Interrupt Control Register	KUPIC	XXXX X0002
0094 ₁₆	Timer B0 Interrupt Control Register	TB0IC	XXXX X0002
0095 ₁₆	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X0002
0096 ₁₆	Timer B2 Interrupt Control Register	TB2IC	XXXX X0002
0097 ₁₆	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X0002
0098 ₁₆	Timer B4 Interrupt Control Register	TB4IC	XXXX X0002
0099 ₁₆			
009A ₁₆	INT4 Interrupt Control Register	INT4IC	XX00 X0002
009B ₁₆			
009C ₁₆	INT2 Interrupt Control Register	INT2IC	XX00 X0002
009D ₁₆	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC CAN0IC	XXXX X0002
009E ₁₆	INT0 Interrupt Control Register	INT0IC	XX00 X0002
009F ₁₆	Exit Priority Control Register	RLVL	XXXX 00002
00A0 ₁₆	Interrupt Request Register 0	IIO0IR	0000 000X2
00A1 ₁₆	Interrupt Request Register 1	IIO1IR	0000 000X2
00A2 ₁₆	Interrupt Request Register 2	IIO2IR	0000 000X2
00A3 ₁₆	Interrupt Request Register 3	IIO3IR	0000 000X2
00A4 ₁₆	Interrupt Request Register 4	IIO4IR	0000 000X2
00A5 ₁₆			
00A6 ₁₆			
00A7 ₁₆			
00A8 ₁₆	Interrupt Request Register 8	IIO8IR	0000 000X2
00A9 ₁₆	Interrupt Request Register 9	IIO9IR	0000 000X2
00AA ₁₆	Interrupt Request Register 10	IIO10IR	0000 000X2
00AB ₁₆	Interrupt Request Register 11	IIO11IR	0000 000X2
00AC ₁₆			
00AD ₁₆			
00AE ₁₆			
00AF ₁₆			
00B0 ₁₆	Interrupt Enable Register 0	IIO0IE	00 ₁₆
00B1 ₁₆	Interrupt Enable Register 1	IIO1IE	00 ₁₆
00B2 ₁₆	Interrupt Enable Register 2	IIO2IE	00 ₁₆
00B3 ₁₆	Interrupt Enable Register 3	IIO3IE	00 ₁₆
00B4 ₁₆	Interrupt Enable Register 4	IIO4IE	00 ₁₆
00B5 ₁₆			
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆	Interrupt Enable Register 8	IIO8IE	00 ₁₆
00B9 ₁₆	Interrupt Enable Register 9	IIO9IE	00 ₁₆
00BA ₁₆	Interrupt Enable Register 10	IIO10IE	00 ₁₆
00BB ₁₆	Interrupt Enable Register 11	IIO11IE	00 ₁₆
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0 ¹⁶			
00C1 ¹⁶			
00C2 ¹⁶			
00C3 ¹⁶			
00C4 ¹⁶			
00C5 ¹⁶			
00C6 ¹⁶			
00C7 ¹⁶			
00C8 ¹⁶			
00C9 ¹⁶			
00CA ¹⁶			
00CB ¹⁶			
00CC ¹⁶			
00CD ¹⁶			
00CE ¹⁶			
00CF ¹⁶			
00D0 ¹⁶			
00D1 ¹⁶			
00D2 ¹⁶			
00D3 ¹⁶			
00D4 ¹⁶			
00D5 ¹⁶			
00D6 ¹⁶			
00D7 ¹⁶			
00D8 ¹⁶			
00D9 ¹⁶			
00DA ¹⁶			
00DB ¹⁶			
00DC ¹⁶			
00DD ¹⁶			
00DE ¹⁶			
00DF ¹⁶			
00E0 ¹⁶			
00E1 ¹⁶			
00E2 ¹⁶			
00E3 ¹⁶			
00E4 ¹⁶			
00E5 ¹⁶			
00E6 ¹⁶			
00E7 ¹⁶			
00E8 ¹⁶ 00E9 ¹⁶	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX ₂ X000 XXXX ₂
00EA ¹⁶ 00EB ¹⁶	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX ₁₆
00EC ¹⁶	Receive Input Register 0	G0RI	XX ₁₆
00ED ¹⁶	SI/O Communication Mode Register 0	G0MR	00 ₁₆
00EE ¹⁶	Transmit Output Register 0	G0TO	XX ₁₆
00EF ¹⁶	SI/O Communication Control Register 0	G0CR	0000 X011 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F0 ₁₆	Data Compare Register 00	G0CMP0	XX ₁₆
00F1 ₁₆	Data Compare Register 01	G0CMP1	XX ₁₆
00F2 ₁₆	Data Compare Register 02	G0CMP2	XX ₁₆
00F3 ₁₆	Data Compare Register 03	G0CMP3	XX ₁₆
00F4 ₁₆	Data Mask Register 00	G0MSK0	XX ₁₆
00F5 ₁₆	Data Mask Register 01	G0MSK1	XX ₁₆
00F6 ₁₆	Communication Clock Select Register	CCS	XXXX 0000 ₂
00F7 ₁₆			
00F8 ₁₆ 00F9 ₁₆	Receive CRC Code Register 0	G0RCRC	XX ₁₆ XX ₁₆
00FA ₁₆ 00FB ₁₆	Transmit CRC Code Register 0	G0TCRC	00 ₁₆ 00 ₁₆
00FC ₁₆	SI/O Extended Mode Register 0	G0EMR	00 ₁₆
00FD ₁₆	SI/O Extended Receive Control Register 0	G0ERC	00 ₁₆
00FE ₁₆	SI/O Special Communication Interrupt Detect Register 0	G0IRF	00 ₁₆
00FF ₁₆	SI/O Extended Transmit Control Register 0	G0ETC	0000 0XXX ₂
0100 ₁₆ 0101 ₁₆	Time Measurement/Waveform Generating Register 10	G1TM0/G1PO0	XX ₁₆ XX ₁₆
0102 ₁₆ 0103 ₁₆	Time Measurement/Waveform Generating Register 11	G1TM1/G1PO1	XX ₁₆ XX ₁₆
0104 ₁₆ 0105 ₁₆	Time Measurement/Waveform Generating Register 12	G1TM2/G1PO2	XX ₁₆ XX ₁₆
0106 ₁₆ 0107 ₁₆	Time Measurement/Waveform Generating Register 13	G1TM3/G1PO3	XX ₁₆ XX ₁₆
0108 ₁₆ 0109 ₁₆	Time Measurement/Waveform Generating Register 14	G1TM4/G1PO4	XX ₁₆ XX ₁₆
010A ₁₆ 010B ₁₆	Time Measurement/Waveform Generating Register 15	G1TM5/G1PO5	XX ₁₆ XX ₁₆
010C ₁₆ 010D ₁₆	Time Measurement/Waveform Generating Register 16	G1TM6/G1PO6	XX ₁₆ XX ₁₆
010E ₁₆ 010F ₁₆	Time Measurement/Waveform Generating Register 17	G1TM7/G1PO7	XX ₁₆ XX ₁₆
0110 ₁₆	Waveform Generating Control Register 10	G1POCR0	0000 X000 ₂
0111 ₁₆	Waveform Generating Control Register 11	G1POCR1	0X00 X000 ₂
0112 ₁₆	Waveform Generating Control Register 12	G1POCR2	0X00 X000 ₂
0113 ₁₆	Waveform Generating Control Register 13	G1POCR3	0X00 X000 ₂
0114 ₁₆	Waveform Generating Control Register 14	G1POCR4	0X00 X000 ₂
0115 ₁₆	Waveform Generating Control Register 15	G1POCR5	0X00 X000 ₂
0116 ₁₆	Waveform Generating Control Register 16	G1POCR6	0X00 X000 ₂
0117 ₁₆	Waveform Generating Control Register 17	G1POCR7	0X00 X000 ₂
0118 ₁₆	Time Measurement Control Register 10	G1TMCR0	00 ₁₆
0119 ₁₆	Time Measurement Control Register 11	G1TMCR1	00 ₁₆
011A ₁₆	Time Measurement Control Register 12	G1TMCR2	00 ₁₆
011B ₁₆	Time Measurement Control Register 13	G1TMCR3	00 ₁₆
011C ₁₆	Time Measurement Control Register 14	G1TMCR4	00 ₁₆
011D ₁₆	Time Measurement Control Register 15	G1TMCR5	00 ₁₆
011E ₁₆	Time Measurement Control Register 16	G1TMCR6	00 ₁₆
011F ₁₆	Time Measurement Control Register 17	G1TMCR7	00 ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0120 ₁₆ 0121 ₁₆	Base Timer Register 1	G1BT	XX ₁₆ XX ₁₆
0122 ₁₆	Base Timer Control Register 10	G1BCR0	00 ₁₆
0123 ₁₆	Base Timer Control Register 11	G1BCR1	X000 000X ₂
0124 ₁₆	Time Measurement Prescaler Register 16	G1TPR6	00 ₁₆
0125 ₁₆	Time Measurement Prescaler Register 17	G1TPR7	00 ₁₆
0126 ₁₆	Function Enable Register 1	G1FE	00 ₁₆
0127 ₁₆	Function Select Register 1	G1FS	00 ₁₆
0128 ₁₆ 0129 ₁₆	SI/O Receive Buffer Register 1	G1RB	XXXX XXXX ₂ X000 XXXX ₂
012A ₁₆ 012B ₁₆	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX ₁₆
012C ₁₆	Receive Input Register 1	G1RI	XX ₁₆
012D ₁₆	SI/O Communication Mode Register 1	G1MR	00 ₁₆
012E ₁₆	Transmit Output Register 1	G1TO	XX ₁₆
012F ₁₆	SI/O Communication Control Register 1	G1CR	0000 X011 ₂
0130 ₁₆	Data Compare Register 10	G1CMP0	XX ₁₆
0131 ₁₆	Data Compare Register 11	G1CMP1	XX ₁₆
0132 ₁₆	Data Compare Register 12	G1CMP2	XX ₁₆
0133 ₁₆	Data Compare Register 13	G1CMP3	XX ₁₆
0134 ₁₆	Data Mask Register 10	G1MSK0	XX ₁₆
0135 ₁₆	Data Mask Register 11	G1MSK1	XX ₁₆
0136 ₁₆			
0137 ₁₆			
0138 ₁₆ 0139 ₁₆	Receive CRC Code Register 1	G1RCRC	XX ₁₆ XX ₁₆
013A ₁₆ 013B ₁₆	Transmit CRC Code Register 1	G1TCRC	00 ₁₆ 00 ₁₆
013C ₁₆	SI/O Extended Mode Register 1	G1EMR	00 ₁₆
013D ₁₆	SI/O Extended Receive Control Register 1	G1ERC	00 ₁₆
013E ₁₆	SI/O Special Communication Interrupt Detect Register 1	G1IRF	00 ₁₆
013F ₁₆	SI/O Extended Transmit Control Register 1	G1ETC	0000 0XXX ₂
0140 ₁₆			
0141 ₁₆			
0142 ₁₆			
0143 ₁₆			
0144 ₁₆			
0145 ₁₆			
0146 ₁₆			
0147 ₁₆			
0148 ₁₆			
0149 ₁₆			
014A ₁₆			
014B ₁₆			
014C ₁₆			
014D ₁₆			
014E ₁₆			
014F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0150 ₁₆			
0151 ₁₆			
0152 ₁₆			
0153 ₁₆			
0154 ₁₆			
0155 ₁₆			
0156 ₁₆			
0157 ₁₆			
0158 ₁₆			
0159 ₁₆			
015A ₁₆			
015B ₁₆			
015C ₁₆			
015D ₁₆			
015E ₁₆			
015F ₁₆			
0160 ₁₆			
0161 ₁₆			
0162 ₁₆			
0163 ₁₆			
0164 ₁₆			
0165 ₁₆			
0166 ₁₆			
0167 ₁₆			
0168 ₁₆			
0169 ₁₆			
016A ₁₆			
016B ₁₆			
016C ₁₆			
016D ₁₆			
016E ₁₆			
016F ₁₆			
0170 ₁₆			
0171 ₁₆			
0172 ₁₆			
0173 ₁₆			
0174 ₁₆			
0175 ₁₆			
0176 ₁₆			
0177 ₁₆			
0178 ₁₆	Input Function Select Register	IPS	00 ₁₆
0179 ₁₆	Input Function Select Register A	IPSA	00 ₁₆
017A ₁₆			
017B ₁₆			
017C ₁₆			
017D ₁₆ to 01DF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
01E0 ₁₆	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX ₁₆
01E1 ₁₆	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX ₁₆
01E2 ₁₆	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX ₁₆
01E3 ₁₆	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX ₁₆
01E4 ₁₆	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX ₁₆
01E5 ₁₆	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX ₁₆
01E6 ₁₆	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX ₁₆
01E7 ₁₆	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX ₁₆
01E8 ₁₆	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX ₁₆
01E9 ₁₆	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX ₁₆
01EA ₁₆	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX ₁₆
01EB ₁₆	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX ₁₆
01EC ₁₆	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX ₁₆
01ED ₁₆	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX ₁₆
01EE ₁₆	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX ₁₆
01EF ₁₆	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX ₁₆
01F0 ₁₆	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX ₁₆
01F1 ₁₆	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX ₁₆
01F2 ₁₆	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX ₁₆
01F3 ₁₆	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX ₁₆
01F4 ₁₆	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX ₁₆
01F5 ₁₆	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX ₁₆
01F6 ₁₆	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX ₁₆
01F7 ₁₆	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX ₁₆
01F8 ₁₆	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX ₁₆
01F9 ₁₆	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX ₁₆
01FA ₁₆	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX ₁₆
01FB ₁₆	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX ₁₆
01FC ₁₆	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX ₁₆
01FD ₁₆	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX ₁₆
01FE ₁₆	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX ₁₆
01FF ₁₆	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX ₁₆
0200 ₁₆ 0201 ₁₆	CAN0 Control Register 0	C0CTRL0	XX01 0X01 ₂ ⁽¹⁾ XXXX 0000 ₂ ⁽¹⁾
0202 ₁₆ 0203 ₁₆	CAN0 Status Register	C0STR	0000 0000 ₂ ⁽¹⁾ X000 0X01 ₂ ⁽¹⁾
0204 ₁₆ 0205 ₁₆	CAN0 Extended ID Register	C0IDR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
0206 ₁₆ 0207 ₁₆	CAN0 Configuration Register	C0CONR	0000 XXXX ₂ ⁽¹⁾ 0000 0000 ₂ ⁽¹⁾
0208 ₁₆ 0209 ₁₆	CAN0 Time Stamp Register	C0TSR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
020A ₁₆	CAN0 Transmit Error Count Register	C0TEC	00 ₁₆ ⁽¹⁾
020B ₁₆	CAN0 Receive Error Count Register	C0REC	00 ₁₆ ⁽¹⁾
020C ₁₆ 020D ₁₆	CAN0 Slot Interrupt Status Register	C0SISTR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
020E ₁₆			
020F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0210 ₁₆	CAN0 Slot Interrupt Mask Register	C0SIMKR	00 ₁₆ ⁽²⁾
0211 ₁₆			00 ₁₆ ⁽²⁾
0212 ₁₆			
0213 ₁₆			
0214 ₁₆	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000 ₂ ⁽²⁾
0215 ₁₆	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000 ₂ ⁽²⁾
0216 ₁₆	CAN0 Error Cause Register	C0EFR	00 ₁₆ ⁽²⁾
0217 ₁₆	CAN0 Baud Rate Prescaler	C0BRP	0000 0001 ₂ ⁽²⁾
0218 ₁₆			
0219 ₁₆	CAN0 Mode Register	C0MDR	XXXX XX00 ₂ ⁽²⁾
021A ₁₆			
021B ₁₆			
021C ₁₆			
021D ₁₆			
021E ₁₆			
021F ₁₆			
0220 ₁₆	CAN0 Single-Shot Control Register	C0SSCTLR	00 ₁₆ ⁽²⁾
0221 ₁₆			00 ₁₆ ⁽²⁾
0222 ₁₆			
0223 ₁₆			
0224 ₁₆	CAN0 Single-Shot Status Register	C0SSSTR	00 ₁₆ ⁽²⁾
0225 ₁₆			00 ₁₆ ⁽²⁾
0226 ₁₆			
0227 ₁₆			
0228 ₁₆	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000 ₂ ⁽²⁾
0229 ₁₆	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000 ₂ ⁽²⁾
022A ₁₆	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000 ₂ ⁽²⁾
022B ₁₆	CAN0 Global Mask Register Extended ID1	C0GMR3	00 ₁₆ ⁽²⁾
022C ₁₆	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000 ₂ ⁽²⁾
022D ₁₆			
022E ₁₆			
022F ₁₆			
0230 ₁₆	CAN0 Message Slot 0 Control Register /	C0MCTL0/	0000 0000 ₂ ⁽²⁾
	CAN0 Local Mask Register A Standard ID0	C0LMAR0	XXX0 0000 ₂ ⁽²⁾
0231 ₁₆	CAN0 Message Slot 1 Control Register /	C0MCTL1/	0000 0000 ₂ ⁽²⁾
	CAN0 Local Mask Register A Standard ID1	C0LMAR1	XX00 0000 ₂ ⁽²⁾
0232 ₁₆	CAN0 Message Slot 2 Control Register /	C0MCTL2/	0000 0000 ₂ ⁽²⁾
	CAN0 Local Mask Register A Extended ID0	C0LMAR2	XXXX 0000 ₂ ⁽²⁾
0233 ₁₆	CAN0 Message Slot 3 Control Register /	C0MCTL3/	00 ₁₆ ⁽²⁾
	CAN0 local Mask Register A Extended ID1	C0LMAR3	00 ₁₆ ⁽²⁾
0234 ₁₆	CAN0 Message Slot 4 Control Register /	C0MCTL4/	0000 0000 ₂ ⁽²⁾
	CAN0 Local Mask Register A Extended ID2	C0LMAR4	XX00 0000 ₂ ⁽²⁾
0235 ₁₆	CAN0 Message Slot 5 Control Register	C0MCTL5	00 ₁₆ ⁽²⁾
0236 ₁₆	CAN0 Message Slot 6 Control Register	C0MCTL6	00 ₁₆ ⁽²⁾
0237 ₁₆	CAN0 Message Slot 7 Control Register	C0MCTL7	00 ₁₆ ⁽²⁾
0238 ₁₆	CAN0 Message Slot 8 Control Register /	C0MCTL8/	0000 0000 ₂ ⁽²⁾
	CAN0 Local Mask Register B Standard ID0	C0LMBR0	XXX0 0000 ₂ ⁽²⁾

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0239 ₁₆	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
023A ₁₆	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾
023B ₁₆	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾
023C ₁₆	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
023D ₁₆	CAN0 Message Slot 13 Control Register	C0MCTL13	00 ₁₆ ⁽²⁾
023E ₁₆	CAN0 Message Slot 14 Control Register	C0MCTL14	00 ₁₆ ⁽²⁾
023F ₁₆	CAN0 Message Slot 15 Control Register	C0MCTL15	00 ₁₆ ⁽²⁾
0240 ₁₆	CAN0 Slot Buffer Select Register	C0SBS	00 ₁₆ ⁽²⁾
0241 ₁₆	CAN0 Control Register 1	C0CTLR1	X000 00XX ₂ ⁽²⁾
0242 ₁₆	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0 ₂
0243 ₁₆			
0244 ₁₆	CAN0 Acceptance Filter Support Register	C0AFS	00 ₁₆ ⁽²⁾
0245 ₁₆			01 ₁₆ ⁽²⁾
0246 ₁₆			
0247 ₁₆			
0248 ₁₆			
0249 ₁₆			
024A ₁₆			
024B ₁₆			
024C ₁₆			
024D ₁₆			
024E ₁₆			
024F ₁₆			
0250 ₁₆			
0251 ₁₆			
0252 ₁₆			
0253 ₁₆			
0254 ₁₆			
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆			
025B ₁₆			
025C ₁₆			
025D ₁₆ to 02BF ₁₆			

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
02C0 ₁₆ 02C1 ₁₆	X0 Register Y0 Register	X0R,Y0R	XX ₁₆ XX ₁₆
02C2 ₁₆ 02C3 ₁₆	X1 Register Y1 Register	X1R,Y1R	XX ₁₆ XX ₁₆
02C4 ₁₆ 02C5 ₁₆	X2 Register Y2 Register	X2R,Y2R	XX ₁₆ XX ₁₆
02C6 ₁₆ 02C7 ₁₆	X3 Register Y3 Register	X3R,Y3R	XX ₁₆ XX ₁₆
02C8 ₁₆ 02C9 ₁₆	X4 Register Y4 Register	X4R,Y4R	XX ₁₆ XX ₁₆
02CA ₁₆ 02CB ₁₆	X5 Register Y5 Register	X5R,Y5R	XX ₁₆ XX ₁₆
02CC ₁₆ 02CD ₁₆	X6 Register Y6 Register	X6R,Y6R	XX ₁₆ XX ₁₆
02CE ₁₆ 02CF ₁₆	X7 Register Y7 Register	X7R,Y7R	XX ₁₆ XX ₁₆
02D0 ₁₆ 02D1 ₁₆	X8 Register Y8 Register	X8R,Y8R	XX ₁₆ XX ₁₆
02D2 ₁₆ 02D3 ₁₆	X9 Register Y9 Register	X9R,Y9R	XX ₁₆ XX ₁₆
02D4 ₁₆ 02D5 ₁₆	X10 Register Y10 Register	X10R,Y10R	XX ₁₆ XX ₁₆
02D6 ₁₆ 02D7 ₁₆	X11 Register Y11 Register	X11R,Y11R	XX ₁₆ XX ₁₆
02D8 ₁₆ 02D9 ₁₆	X12 Register Y12 Register	X12R,Y12R	XX ₁₆ XX ₁₆
02DA ₁₆ 02DB ₁₆	X13 Register Y13 Register	X13R,Y13R	XX ₁₆ XX ₁₆
02DC ₁₆ 02DD ₁₆	X14 Register Y14 Register	X14R,Y14R	XX ₁₆ XX ₁₆
02DE ₁₆ 02DF ₁₆	X15 Register Y15 Register	X15R,Y15R	XX ₁₆ XX ₁₆
02E0 ₁₆	X/Y Control Register	XYC	XXXX XX00 ₂
02E1 ₁₆			
02E2 ₁₆			
02E3 ₁₆			
02E4 ₁₆	UART1 Special Mode Register 4	U1SMR4	00 ₁₆
02E5 ₁₆	UART1 Special Mode Register 3	U1SMR3	00 ₁₆
02E6 ₁₆	UART1 Special Mode Register 2	U1SMR2	00 ₁₆
02E7 ₁₆	UART1 Special Mode Register	U1SMR	00 ₁₆
02E8 ₁₆	UART1 Transmit/Receive Mode Register	U1MR	00 ₁₆
02E9 ₁₆	UART1 Bit Rate Register	U1BRG	XX ₁₆
02EA ₁₆ 02EB ₁₆	UART1 Transmit Buffer Register	U1TB	XX ₁₆ XX ₁₆
02EC ₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000 ₂
02ED ₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010 ₂
02EE ₁₆ 02EF ₁₆	UART1 Receive Buffer Register	U1RB	XX ₁₆ XX ₁₆

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Address	Register	Symbol	Value after RESET
02F0 ₁₆			
02F1 ₁₆			
02F2 ₁₆			
02F3 ₁₆			
02F4 ₁₆	UART4 Special Mode Register 4	U4SMR4	00 ₁₆
02F5 ₁₆	UART4 Special Mode Register 3	U4SMR3	00 ₁₆
02F6 ₁₆	UART4 Special Mode Register 2	U4SMR2	00 ₁₆
02F7 ₁₆	UART4 Special Mode Register	U4SMR	00 ₁₆
02F8 ₁₆	UART4 Transmit/Receive Mode Register	U4MR	00 ₁₆
02F9 ₁₆	UART4 Bit Rate Register	U4BRG	XX ₁₆
02FA ₁₆	UART4 Transmit Buffer Register	U4TB	XX ₁₆
02FB ₁₆			XX ₁₆
02FC ₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000 ₂
02FD ₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010 ₂
02FE ₁₆	UART4 Receive Buffer Register	U4RB	XX ₁₆
02FF ₁₆			XX ₁₆
0300 ₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX ₂
0301 ₁₆			
0302 ₁₆	Timer A1-1 Register	TA11	XX ₁₆
0303 ₁₆			XX ₁₆
0304 ₁₆	Timer A2-1 Register	TA21	XX ₁₆
0305 ₁₆			XX ₁₆
0306 ₁₆	Timer A4-1 Register	TA41	XX ₁₆
0307 ₁₆			XX ₁₆
0308 ₁₆	Three-Phase PWM Control Register 0	INVC0	00 ₁₆
0309 ₁₆	Three-Phase PWM Control Register 1	INVC1	00 ₁₆
030A ₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111 ₂
030B ₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111 ₂
030C ₁₆	Dead Time Timer	DTT	XX ₁₆
030D ₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX ₁₆
030E ₁₆			
030F ₁₆			
0310 ₁₆	Timer B3 Register	TB3	XX ₁₆
0311 ₁₆			XX ₁₆
0312 ₁₆	Timer B4 Register	TB4	XX ₁₆
0313 ₁₆			XX ₁₆
0314 ₁₆	Timer B5 Register	TB5	XX ₁₆
0315 ₁₆			XX ₁₆
0316 ₁₆			
0317 ₁₆			
0318 ₁₆			
0319 ₁₆			
031A ₁₆			
031B ₁₆	Timer B3 Mode Register	TB3MR	00XX 0000 ₂
031C ₁₆	Timer B4 Mode Register	TB4MR	00XX 0000 ₂
031D ₁₆	Timer B5 Mode Register	TB5MR	00XX 0000 ₂
031E ₁₆			
031F ₁₆	External Interrupt Cause Select Register	IFSR	00 ₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0320 ₁₆			
0321 ₁₆			
0322 ₁₆			
0323 ₁₆			
0324 ₁₆	UART3 Special Mode Register 4	U3SMR4	00 ₁₆
0325 ₁₆	UART3 Special Mode Register 3	U3SMR3	00 ₁₆
0326 ₁₆	UART3 Special Mode Register 2	U3SMR2	00 ₁₆
0327 ₁₆	UART3 Special Mode Register	U3SMR	00 ₁₆
0328 ₁₆	UART3 Transmit/Receive Mode Register	U3MR	00 ₁₆
0329 ₁₆	UART3 Bit Rate Register	U3BRG	XX ₁₆
032A ₁₆	UART3 Transmit Buffer Register	U3TB	XX ₁₆
032B ₁₆			XX ₁₆
032C ₁₆	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000 ₂
032D ₁₆	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010 ₂
032E ₁₆	UART3 Receive Buffer Register	U3RB	XX ₁₆
032F ₁₆			XX ₁₆
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 Special Mode Register 4	U2SMR4	00 ₁₆
0335 ₁₆	UART2 Special Mode Register 3	U2SMR3	00 ₁₆
0336 ₁₆	UART2 Special Mode Register 2	U2SMR2	00 ₁₆
0337 ₁₆	UART2 Special Mode Register	U2SMR	00 ₁₆
0338 ₁₆	UART2 Transmit/Receive Mode Register	U2MR	00 ₁₆
0339 ₁₆	UART2 Bit Rate Register	U2BRG	XX ₁₆
033A ₁₆	UART2 Transmit Buffer Register	U2TB	XX ₁₆
033B ₁₆			XX ₁₆
033C ₁₆	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000 ₂
033D ₁₆	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010 ₂
033E ₁₆	UART2 Receive Buffer Register	U2RB	XX ₁₆
033F ₁₆			XX ₁₆
0340 ₁₆	Count Start Flag	TABSR	00 ₁₆
0341 ₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-Shot Start Flag	ONSF	00 ₁₆
0343 ₁₆	Trigger Select Register	TRGSR	00 ₁₆
0344 ₁₆	Up/Down Flag	UDF	00 ₁₆
0345 ₁₆			
0346 ₁₆	Timer A0 Register	TA0	XX ₁₆
0347 ₁₆			XX ₁₆
0348 ₁₆	Timer A1 Register	TA1	XX ₁₆
0349 ₁₆			XX ₁₆
034A ₁₆	Timer A2 Register	TA2	XX ₁₆
034B ₁₆			XX ₁₆
034C ₁₆	Timer A3 Register	TA3	XX ₁₆
034D ₁₆			XX ₁₆
034E ₁₆	Timer A4 Register	TA4	XX ₁₆
034F ₁₆			XX ₁₆

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Address	Register	Symbol	Value after RESET
0350 ₁₆ 0351 ₁₆	Timer B0 Register	TB0	XX ₁₆ XX ₁₆
0352 ₁₆ 0353 ₁₆	Timer B1 Register	TB1	XX ₁₆ XX ₁₆
0354 ₁₆ 0355 ₁₆	Timer B2 Register	TB2	XX ₁₆ XX ₁₆
0356 ₁₆	Timer A0 Mode Register	TA0MR	00 ₁₆
0357 ₁₆	Timer A1 Mode Register	TA1MR	00 ₁₆
0358 ₁₆	Timer A2 Mode Register	TA2MR	00 ₁₆
0359 ₁₆	Timer A3 Mode Register	TA3MR	00 ₁₆
035A ₁₆	Timer A4 Mode Register	TA4MR	00 ₁₆
035B ₁₆	Timer B0 Mode Register	TB0MR	00XX 0000 ₂
035C ₁₆	Timer B1 Mode Register	TB1MR	00XX 0000 ₂
035D ₁₆	Timer B2 Mode Register	TB2MR	00XX 0000 ₂
035E ₁₆	Timer B2 Special Mode Register	TB2SC	XXXX XXX0 ₂
035F ₁₆	Count Source Prescaler Register ⁽¹⁾	TCSPR	0XXX 0000 ₂
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆	UART0 Special Mode Register 4	U0SMR4	00 ₁₆
0365 ₁₆	UART0 Special Mode Register 3	U0SMR3	00 ₁₆
0366 ₁₆	UART0 Special Mode Register 2	U0SMR2	00 ₁₆
0367 ₁₆	UART0 Special Mode Register	U0SMR	00 ₁₆
0368 ₁₆	UART0 Transmit/Receive Mode Register	U0MR	00 ₁₆
0369 ₁₆	UART0 Bit Rate Register	U0BRG	XX ₁₆
036A ₁₆ 036B ₁₆	UART0 Transmit Buffer Register	U0TB	XX ₁₆ XX ₁₆
036C ₁₆	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000 ₂
036D ₁₆	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010 ₂
036E ₁₆ 036F ₁₆	UART0 Receive Buffer Register	U0RB	XX ₁₆ XX ₁₆
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆			
0375 ₁₆			
0376 ₁₆			
0377 ₁₆			
0378 ₁₆	DMA0 Request Source Select Register	DM0SL	0X00 0000 ₂
0379 ₁₆	DMA1 Request Source Select Register	DM1SL	0X00 0000 ₂
037A ₁₆	DMA2 Request Source Select Register	DM2SL	0X00 0000 ₂
037B ₁₆	DMA3 Request Source Select Register	DM3SL	0X00 0000 ₂
037C ₁₆ 037D ₁₆	CRC Data Register	CRCD	XX ₁₆ XX ₁₆
037E ₁₆ 037F ₁₆	CRC Input Register	CRCIN	XX ₁₆ XX ₁₆

X: Indeterminate

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NOTES:

1. The TCSPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
0380 ₁₆ 0381 ₁₆	A/D0 Register 0	AD00	XXXX XXXX ₂ 0000 0000 ₂
0382 ₁₆ 0383 ₁₆	A/D0 Register 1	AD01	XX ₁₆ XX ₁₆
0384 ₁₆ 0385 ₁₆	A/D0 Register 2	AD02	XX ₁₆ XX ₁₆
0386 ₁₆ 0387 ₁₆	A/D0 Register 3	AD03	XX ₁₆ XX ₁₆
0388 ₁₆ 0389 ₁₆	A/D0 Register 4	AD04	XX ₁₆ XX ₁₆
038A ₁₆ 038B ₁₆	A/D0 Register 5	AD05	XX ₁₆ XX ₁₆
038C ₁₆ 038D ₁₆	A/D0 Register 6	AD06	XX ₁₆ XX ₁₆
038E ₁₆ 038F ₁₆	A/D0 Register 7	AD07	XX ₁₆ XX ₁₆
0390 ₁₆			
0391 ₁₆			
0392 ₁₆	A/D0 Control Register 4	AD0CON4	XXXX 00XX ₂
0393 ₁₆			
0394 ₁₆	A/D0 Control Register 2	AD0CON2	XX0X X000 ₂
0395 ₁₆	A/D0 Control Register 3	AD0CON3	XXXX X000 ₂
0396 ₁₆	A/D0 Control Register 0	AD0CON0	00 ₁₆
0397 ₁₆	A/D0 Control Register 1	AD0CON1	00 ₁₆
0398 ₁₆	D/A Register 0	DA0	XX ₁₆
0399 ₁₆			
039A ₁₆	D/A Register 1	DA1	XX ₁₆
039B ₁₆			
039C ₁₆	D/A Control Register	DACON	XXXX XX00 ₂
039D ₁₆			
039E ₁₆			
039F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin Package>

Address	Register	Symbol	Value after RESET
03A0 ₁₆	Function Select Register A8	PS8	X000 0000 ₂
03A1 ₁₆	Function Select Register A9	PS9	00 ₁₆
03A2 ₁₆			
03A3 ₁₆			
03A4 ₁₆			
03A5 ₁₆			
03A6 ₁₆			
03A7 ₁₆	Function Select Register D1	PSD1	X0XX XX00 ₂
03A8 ₁₆			
03A9 ₁₆			
03AA ₁₆			
03AB ₁₆			
03AC ₁₆	Function Select Register C2	PSC2	XXXX X00X ₂
03AD ₁₆	Function Select Register C3	PSC3	X0XX XXXX ₂
03AE ₁₆			
03AF ₁₆	Function Select Register C	PSC	00X0 0000 ₂
03B0 ₁₆	Function Select Register A0	PS0	00 ₁₆
03B1 ₁₆	Function Select Register A1	PS1	00 ₁₆
03B2 ₁₆	Function Select Register B0	PSL0	00 ₁₆
03B3 ₁₆	Function Select Register B1	PSL1	00 ₁₆
03B4 ₁₆	Function Select Register A2	PS2	00X0 0000 ₂
03B5 ₁₆	Function Select Register A3	PS3	00 ₁₆
03B6 ₁₆	Function Select Register B2	PSL2	00X0 0000 ₂
03B7 ₁₆	Function Select Register B3	PSL3	00 ₁₆
03B8 ₁₆			
03B9 ₁₆	Function Select Register A5	PS5	XXX0 0000 ₂
03BA ₁₆			
03BB ₁₆			
03BC ₁₆			
03BD ₁₆			
03BE ₁₆			
03BF ₁₆			
03C0 ₁₆	Port P6 Register	P6	XX ₁₆
03C1 ₁₆	Port P7 Register	P7	XX ₁₆
03C2 ₁₆	Port P6 Direction Register	PD6	00 ₁₆
03C3 ₁₆	Port P7 Direction Register	PD7	00 ₁₆
03C4 ₁₆	Port P8 Register	P8	XX ₁₆
03C5 ₁₆	Port P9 Register	P9	XX ₁₆
03C6 ₁₆	Port P8 Direction Register	PD8	00X0 0000 ₂
03C7 ₁₆	Port P9 Direction Register	PD9	00 ₁₆
03C8 ₁₆	Port P10 Register	P10	XX ₁₆
03C9 ₁₆	Port P11 Register	P11	XX ₁₆
03CA ₁₆	Port P10 Direction Register	PD10	00 ₁₆
03CB ₁₆	Port P11 Direction Register	PD11	XXX0 0000 ₂
03CC ₁₆	Port P12 Register	P12	XX ₁₆
03CD ₁₆	Port P13 Register	P13	XX ₁₆
03CE ₁₆	Port P12 Direction Register	PD12	00 ₁₆
03CF ₁₆	Port P13 Direction Register	PD13	00 ₁₆

X: Indeterminate

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<144-pin Package>

Address	Register	Symbol	Value after RESET
03D0 ₁₆	Port P14 Register	P14	XX ₁₆
03D1 ₁₆	Port P15 Register	P15	XX ₁₆
03D2 ₁₆	Port P14 Direction Register	PD14	X000 0000 ₂
03D3 ₁₆	Port P15 Direction Register	PD15	00 ₁₆
03D4 ₁₆			
03D5 ₁₆			
03D6 ₁₆			
03D7 ₁₆			
03D8 ₁₆			
03D9 ₁₆			
03DA ₁₆	Pull-Up Control Register 2	PUR2	00 ₁₆
03DB ₁₆	Pull-Up Control Register 3	PUR3	00 ₁₆
03DC ₁₆	Pull-Up Control Register 4	PUR4	XXXX 0000 ₂
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆	Port P0 Register	P0	XX ₁₆
03E1 ₁₆	Port P1 Register	P1	XX ₁₆
03E2 ₁₆	Port P0 Direction Register	PD0	00 ₁₆
03E3 ₁₆	Port P1 Direction Register	PD1	00 ₁₆
03E4 ₁₆	Port P2 Register	P2	XX ₁₆
03E5 ₁₆	Port P3 Register	P3	XX ₁₆
03E6 ₁₆	Port P2 Direction Register	PD2	00 ₁₆
03E7 ₁₆	Port P3 Direction Register	PD3	00 ₁₆
03E8 ₁₆	Port P4 Register	P4	XX ₁₆
03E9 ₁₆	Port P5 Register	P5	XX ₁₆
03EA ₁₆	Port P4 Direction Register	PD4	00 ₁₆
03EB ₁₆	Port P5 Direction Register	PD5	00 ₁₆
03EC ₁₆			
03ED ₁₆			
03EE ₁₆			
03EF ₁₆			
03F0 ₁₆	Pull-Up Control Register 0	PUR0	00 ₁₆
03F1 ₁₆	Pull-Up Control Register 1	PUR1	XXXX 0000 ₂
03F2 ₁₆			
03F3 ₁₆			
03F4 ₁₆			
03F5 ₁₆			
03F6 ₁₆			
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆			
03FD ₁₆			
03FE ₁₆			
03FF ₁₆	Port Control Register	PCR	XXXX XXX0 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin Package>

Address	Register	Symbol	Value after RESET
03A0 ₁₆			
03A1 ₁₆			
03A2 ₁₆			
03A3 ₁₆			
03A4 ₁₆			
03A5 ₁₆			
03A6 ₁₆			
03A7 ₁₆	Function Select Register D1	PSD1	X0XX XX00 ₂
03A8 ₁₆			
03A9 ₁₆			
03AA ₁₆			
03AB ₁₆			
03AC ₁₆	Function Select Register C2	PSC2	XXXX X00X ₂
03AD ₁₆	Function Select Register C3	PSC3	X0XX XXXX ₂
03AE ₁₆			
03AF ₁₆	Function Select Register C	PSC	00X0 0000 ₂
03B0 ₁₆	Function Select Register A0	PS0	00 ₁₆
03B1 ₁₆	Function Select Register A1	PS1	00 ₁₆
03B2 ₁₆	Function Select Register B0	PSL0	00 ₁₆
03B3 ₁₆	Function Select Register B1	PSL1	00 ₁₆
03B4 ₁₆	Function Select Register A2	PS2	00X0 0000 ₂
03B5 ₁₆	Function Select Register A3	PS3	00 ₁₆
03B6 ₁₆	Function Select Register B2	PSL2	00X0 0000 ₂
03B7 ₁₆	Function Select Register B3	PSL3	00 ₁₆
03B8 ₁₆			
03B9 ₁₆			
03BA ₁₆			
03BB ₁₆			
03BC ₁₆			
03BD ₁₆			
03BE ₁₆			
03BF ₁₆			
03C0 ₁₆	Port P6 Register	P6	XX ₁₆
03C1 ₁₆	Port P7 Register	P7	XX ₁₆
03C2 ₁₆	Port P6 Direction Register	PD6	00 ₁₆
03C3 ₁₆	Port P7 Direction Register	PD7	00 ₁₆
03C4 ₁₆	Port P8 Register	P8	XX ₁₆
03C5 ₁₆	Port P9 Register	P9	XX ₁₆
03C6 ₁₆	Port P8 Direction Register	PD8	00X0 0000 ₂
03C7 ₁₆	Port P9 Direction Register	PD9	00 ₁₆
03C8 ₁₆	Port P10 Register	P10	XX ₁₆
03C9 ₁₆			
03CA ₁₆	Port P10 Direction Register	PD10	00 ₁₆
03CB ₁₆	Set default value to "FF ₁₆ "		
03CC ₁₆			
03CD ₁₆			
03CE ₁₆	Set default value to "FF ₁₆ "		
03CF ₁₆	Set default value to "FF ₁₆ "		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin Package>

Address	Register	Symbol	Value after RESET
03D0 ₁₆			
03D1 ₁₆			
03D2 ₁₆	Set default value to "FF ₁₆ "		
03D3 ₁₆	Set default value to "FF ₁₆ "		
03D4 ₁₆			
03D5 ₁₆			
03D6 ₁₆			
03D7 ₁₆			
03D8 ₁₆			
03D9 ₁₆			
03DA ₁₆	Pull-Up Control Register 2	PUR2	00 ₁₆
03DB ₁₆	Pull-Up Control Register 3	PUR3	00 ₁₆
03DC ₁₆	Set default value to "00 ₁₆ "		
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆	Port P0 Register	P0	XX ₁₆
03E1 ₁₆	Port P1 Register	P1	XX ₁₆
03E2 ₁₆	Port P0 Direction Register	PD0	00 ₁₆
03E3 ₁₆	Port P1 Direction Register	PD1	00 ₁₆
03E4 ₁₆	Port P2 Register	P2	XX ₁₆
03E5 ₁₆	Port P3 Register	P3	XX ₁₆
03E6 ₁₆	Port P2 Direction Register	PD2	00 ₁₆
03E7 ₁₆	Port P3 Direction Register	PD3	00 ₁₆
03E8 ₁₆	Port P4 Register	P4	XX ₁₆
03E9 ₁₆	Port P5 Register	P5	XX ₁₆
03EA ₁₆	Port P4 Direction Register	PD4	00 ₁₆
03EB ₁₆	Port P5 Direction Register	PD5	00 ₁₆
03EC ₁₆			
03ED ₁₆			
03EE ₁₆			
03EF ₁₆			
03F0 ₁₆	Pull-up Control Register 0	PUR0	00 ₁₆
03F1 ₁₆	Pull-up Control Register 1	PUR1	XXXX 0000 ₂
03F2 ₁₆			
03F3 ₁₆			
03F4 ₁₆			
03F5 ₁₆			
03F6 ₁₆			
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆			
03FD ₁₆			
03FE ₁₆			
03FF ₁₆	Port Control Register	PCR	XXXX XXX0 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

5. Reset

Hardware reset 1, brown-out detection reset (hardware reset 2), software reset and watchdog timer reset are available to reset the microcomputer.

5.1 Hardware Reset 1

Pins, the CPU and SFR are reset by setting the $\overline{\text{RESET}}$ pin. If the supply voltage meets the recommended operating conditions, all pins are reset when a low-level ("L") signal is applied to the $\overline{\text{RESET}}$ pin (see **Table 5.1**). The oscillation circuit is also reset and the main clock starts oscillating. The CPU and SFR are reset when the signal applied to the $\overline{\text{RESET}}$ pin changes "L" to high level ("H"). The microcomputer executes the program in an address indicated by the reset vector. The internal RAM is not reset. When an "L" signal is applied to the $\overline{\text{RESET}}$ pin while writing data to the internal RAM, the internal RAM is in an indeterminate state.

Figure 5.1 shows an example of the reset circuit. Figure 5.2 shows a reset sequence. Table 5.1 lists pin states while the $\overline{\text{RESET}}$ pin is held "L".

5.1.1 Reset on a Stable Supply Voltage

- (1) Apply an "L" signal to the $\overline{\text{RESET}}$ pin
- (2) Provide 20 or more clock cycle inputs into the XIN pin
- (3) Apply an "H" signal to the $\overline{\text{RESET}}$ pin

5.1.2 Power-on Reset

- (1) Apply an "L" signal to the $\overline{\text{RESET}}$ pin
- (2) Raise the supply voltage to the recommended operating level
- (3) Insert $td(P-R)$ ms as wait time for the internal voltage to stabilize
- (4) Provide 20 or more clock cycle inputs into the XIN pin
- (5) Apply an "H" signal to the $\overline{\text{RESET}}$ pin

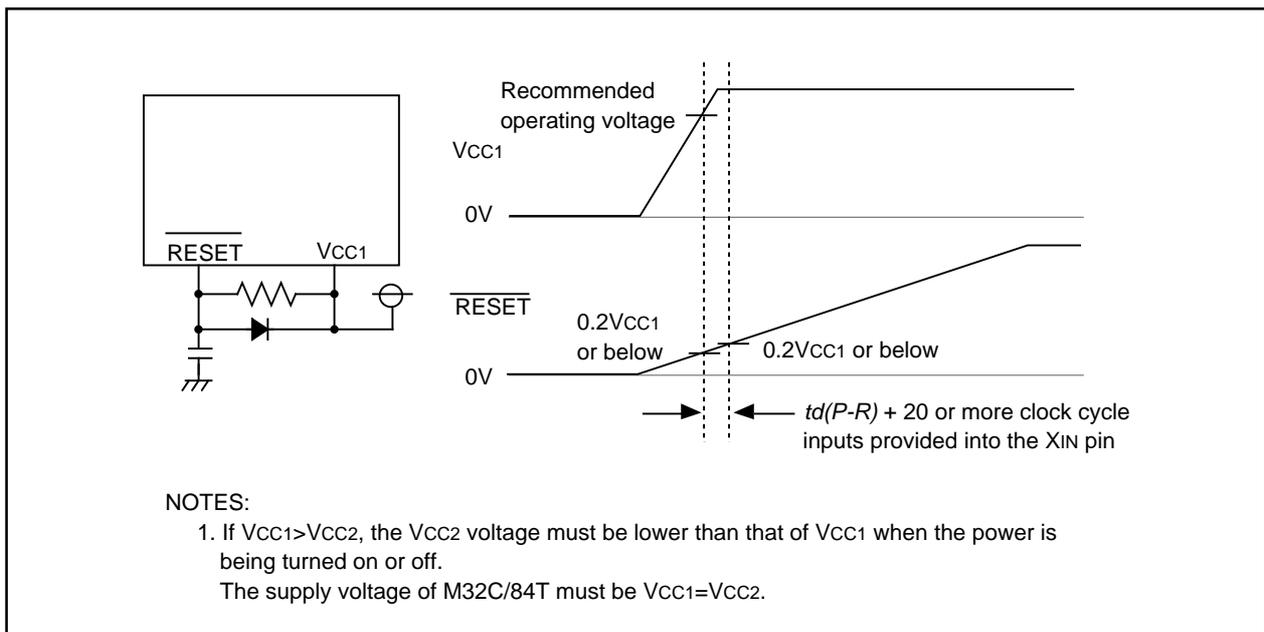


Figure 5.1 Reset Circuit

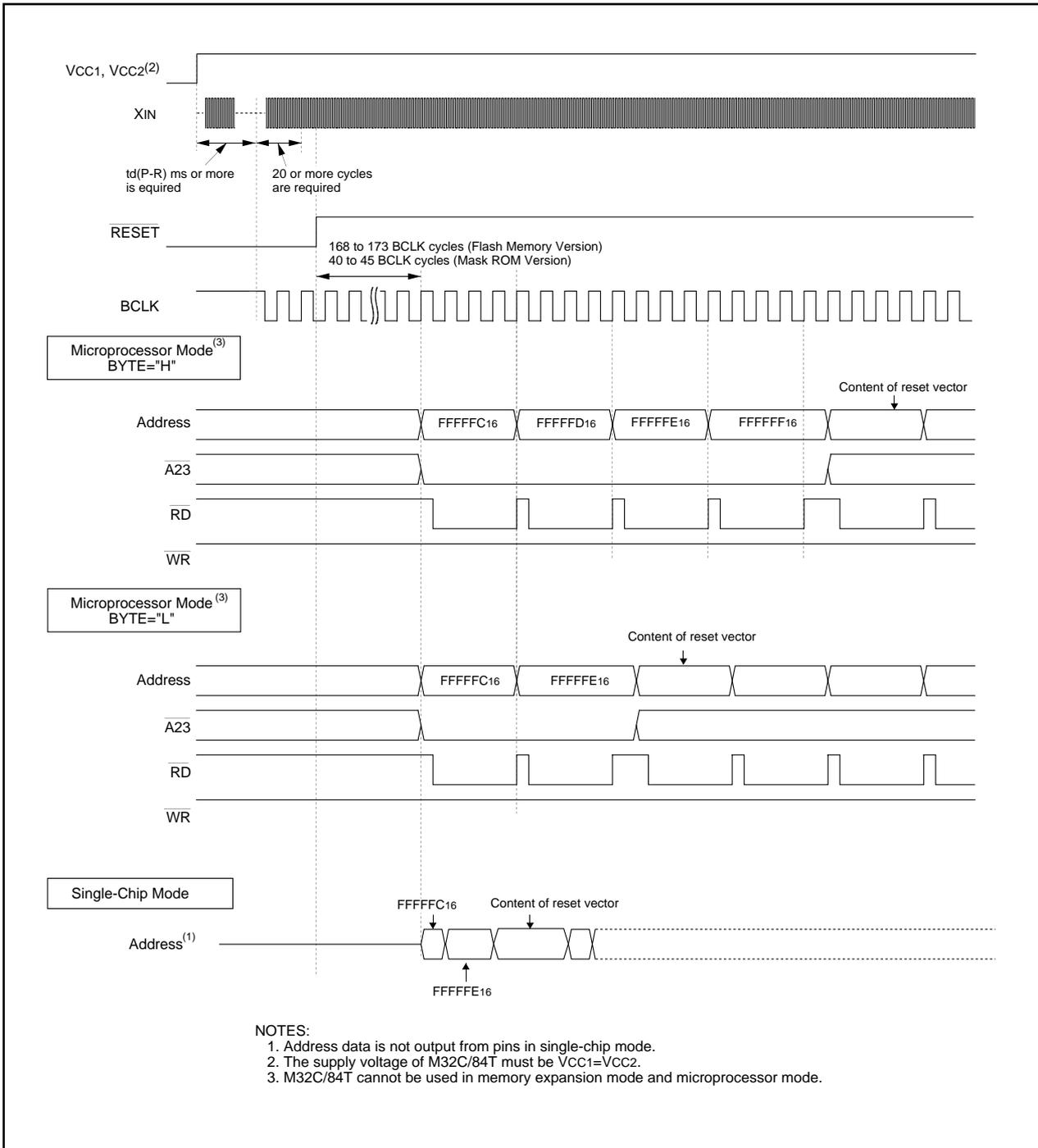


Figure 5.2 Reset Sequence

Table 5.1 Pin States while $\overline{\text{RESET}}$ Pin is Held "L"

Pin Name	Pin States ⁽²⁾		
	CNVss=Vss	CNVss=Vcc	
		BYTE=Vss	BYTE=Vcc
P0	Input port (high-impedance)	Inputs data (high-impedance)	
P1	Input port (high-impedance)	Inputs data (high-impedance)	Input port (high-impedance)
P2, P3, P4	Input port (high-impedance)	Output addresses (indeterminate)	
P50	Input port (high-impedance)	Outputs the $\overline{\text{WR}}$ signal ("H") ⁽³⁾	
P51	Input port (high-impedance)	Outputs the $\overline{\text{BHE}}$ signal (indeterminate)	
P52	Input port (high-impedance)	Outputs the $\overline{\text{RD}}$ signal ("H") ⁽³⁾	
P53	Input port (high-impedance)	Outputs the BCLK ⁽³⁾	
P54	Input port (high-impedance)	Outputs the $\overline{\text{HLD}}\overline{\text{A}}$ signal (Output signal depends on an input signal to the $\overline{\text{HOLD}}$ pin.) ⁽³⁾	
P55	Input port (high-impedance)	Inputs the HOLD signal (high-impedance)	
P56	Input port (high-impedance)	Outputs an "H" signal ⁽³⁾	
P57	Input port (high-impedance)	Inputs the RDY signal (high-impedance)	
P6 to P15 ⁽¹⁾	Input port (high-impedance)	Input port (high-impedance)	

NOTES:

1. Ports P11 to P15 are provided in the 144-pin package only.
2. The availability of pull-up resistors is indeterminate until internal supply voltage stabilizes.
3. Each port is in this state after power is on and internal supply voltage stabilizes, but in an indeterminate state until internal supply voltage stabilizes.

5.2 Brown-Out Detection Reset (Hardware Reset 2)

Pins, the CPU and SFR are reset by using the built-in voltage detection circuit, which monitors the voltage applied to the VCC1 pin.

When the VC26 bit in the VCR2 register is set to "1" (reset level detection circuit enabled), pins, the CPU and SFR are reset as soon as the voltage applied to the VCC1 pin drops to Vdet3 or below.

Then, pins, the CPU and SFR are reset as soon as the voltage applied to the VCC1 pin reaches Vdet3r or above. The microcomputer executes the program in an address determined by the reset vector.

The microcomputer executes the program after detecting Vdet3r and waiting $t_d(S-R)$ ms. The same pins and registers are reset by the hardware reset 1 and brown-out detection reset, and are also placed in the same reset state.

The microcomputer cannot exit stop mode by brown-out detection reset.

Figure 5.3 shows an example of brown-out detection reset operation.

NOTES:

1. Brown-out detection reset cannot be used in M32C/84T.

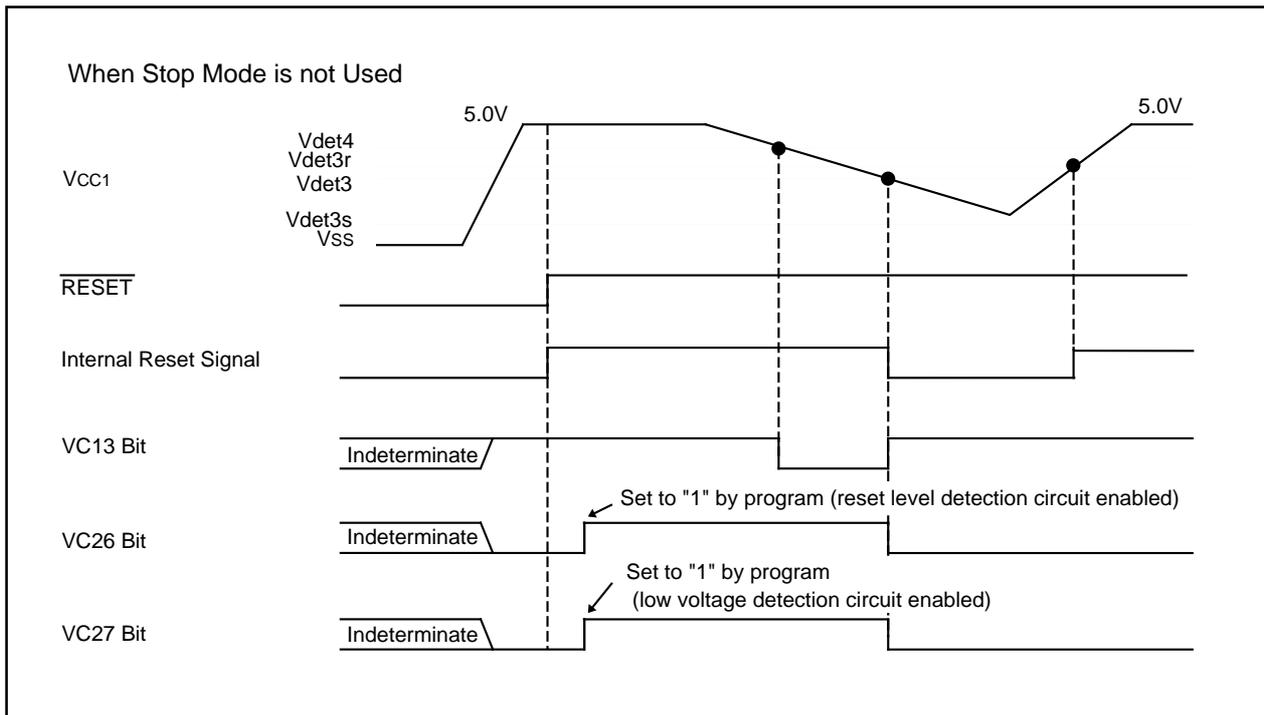


Figure 5.3 Brown-out Detection Reset (Hardware Reset 2)

5.3 Software Reset

Pins, the CPU and SFR are reset when the PM03 bit in the PM0 register is set to "1" (microcomputer reset). Then the microcomputer executes the program in an address determined by the reset vector.

Set the PM03 bit to "1" while the main clock is selected as the CPU clock and the main clock oscillation is stable.

In the software reset, the microcomputer does not reset a part of the SFR. Refer to **4. SFR** for details. Processor mode remains unchanged since the PM01 and PM00 bits in the PM0 register are not reset.

5.4 Watchdog Timer Reset

Pins, the CPU and SFR are reset when the CM06 bit in the CM0 register is set to "1" (reset) and the watchdog timer underflows. Then the microcomputer executes the program in an address determined by the reset vector.

In the watchdog timer reset, the microcomputer does not reset a part of the SFR. Refer to **4. SFR** for details. Processor mode remains unchanged since the PM01 and PM00 bits in the PM0 register are not reset.

5.5 Internal Space

Figure 5.4 shows CPU register states after reset. Refer to 4. SFR for SFR states after reset.

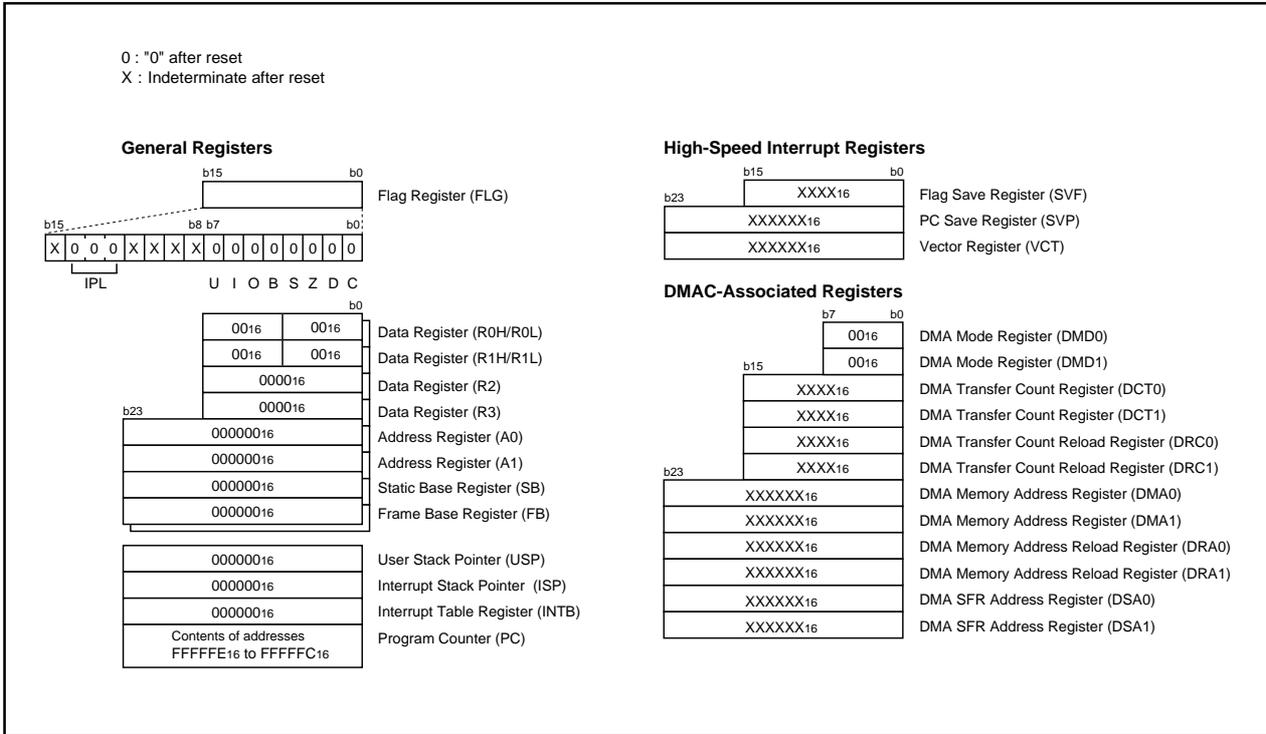


Figure 5.4 CPU Register States after Reset

6. Voltage Detection Circuit

NOTE

The voltage detection circuit in M32C/84T cannot be used.
However, the cold start-up/warm start-up determine function is available.

The voltage detection circuit consists of the reset level detection circuit and the low voltage detection circuit. The reset level detection circuit monitors the voltage applied to the VCC1 pin. The microcomputer is reset if the reset level detection circuit detects VCC1 is Vdet3 or below. This circuit is disabled when the microcomputer is in stop mode.

The voltage detection circuit also monitors the voltage applied to the VCC1 pin. The low voltage detection signal is generated when the low voltage detection circuit detects VCC1 is above or below Vdet4. This signal generates the low voltage detection interrupt. The VC13 bit in the VCR1 register determines whether VCC1 is above or below Vdet4.

The voltage detection circuit is available when VCC1=4.2V to 5.5V.

Figure 6.1 shows a block diagram of the voltage detection circuit.

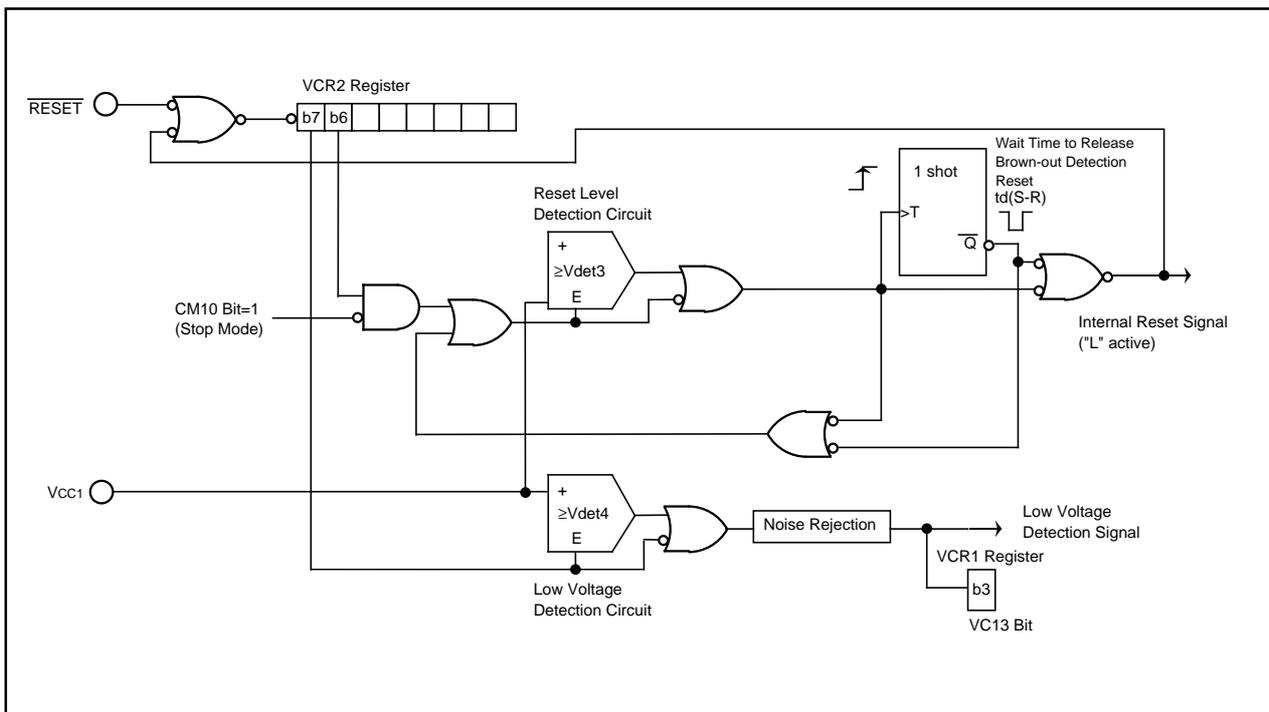


Figure 6.1 Voltage Detection Circuit Block Diagram

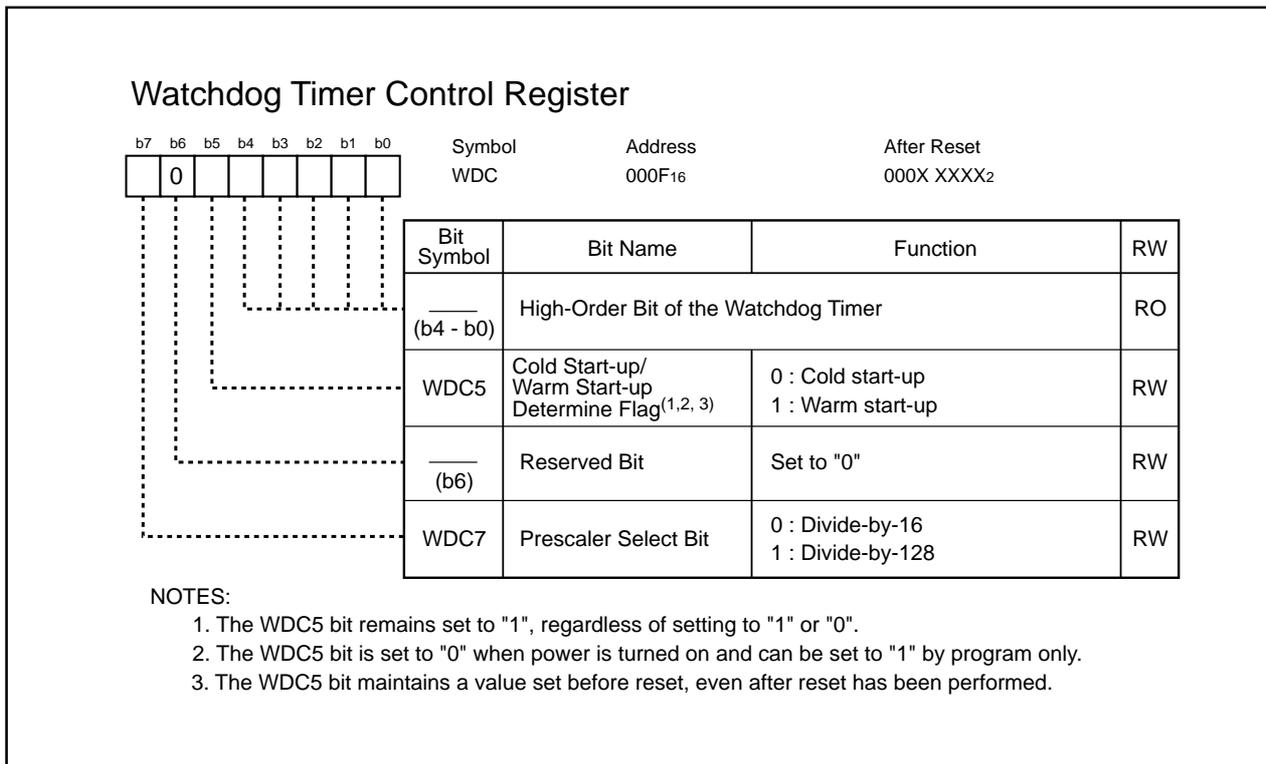


Figure 6.2 WDC Register

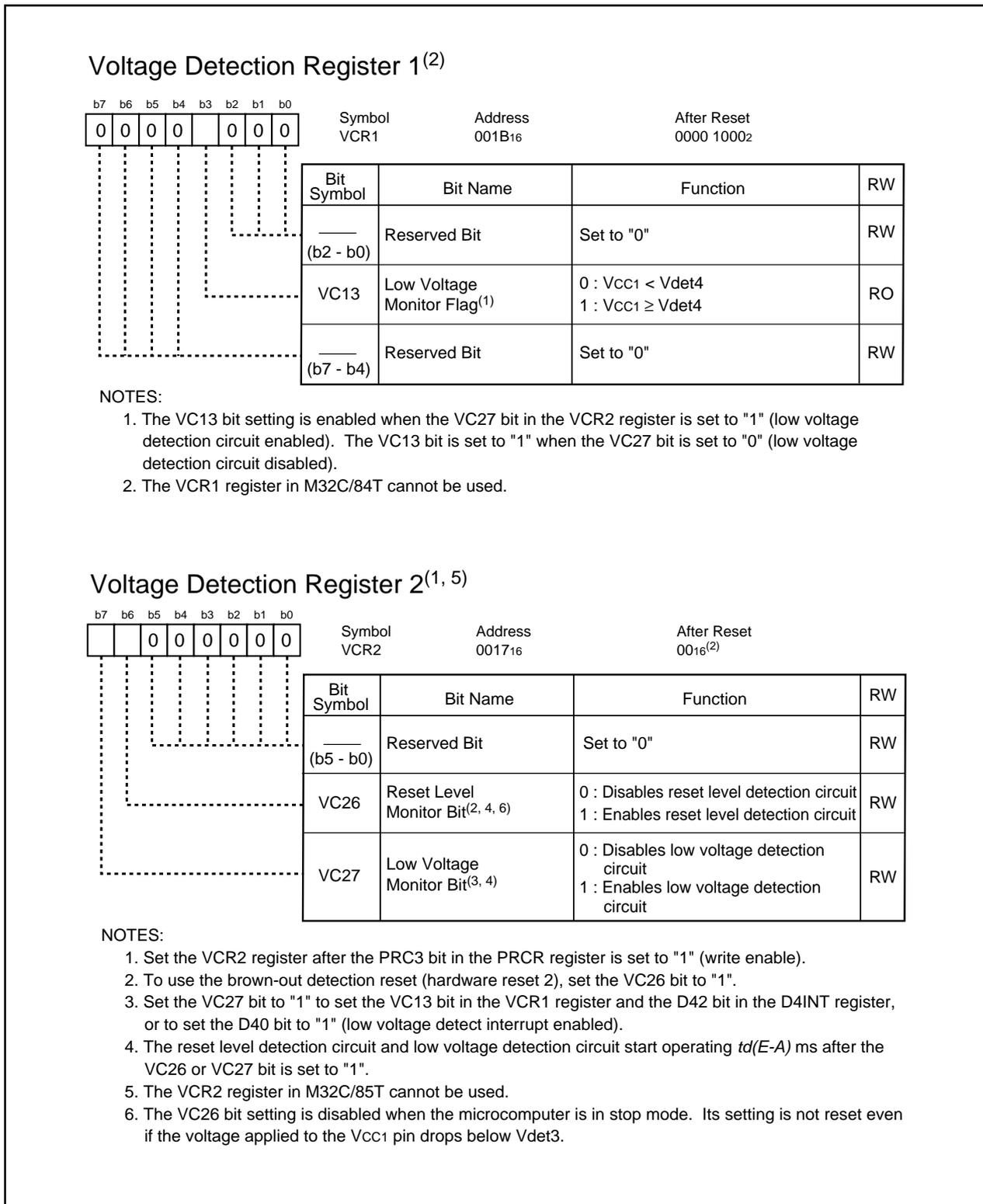


Figure 6.3 VCR1 and VCR2 Registers

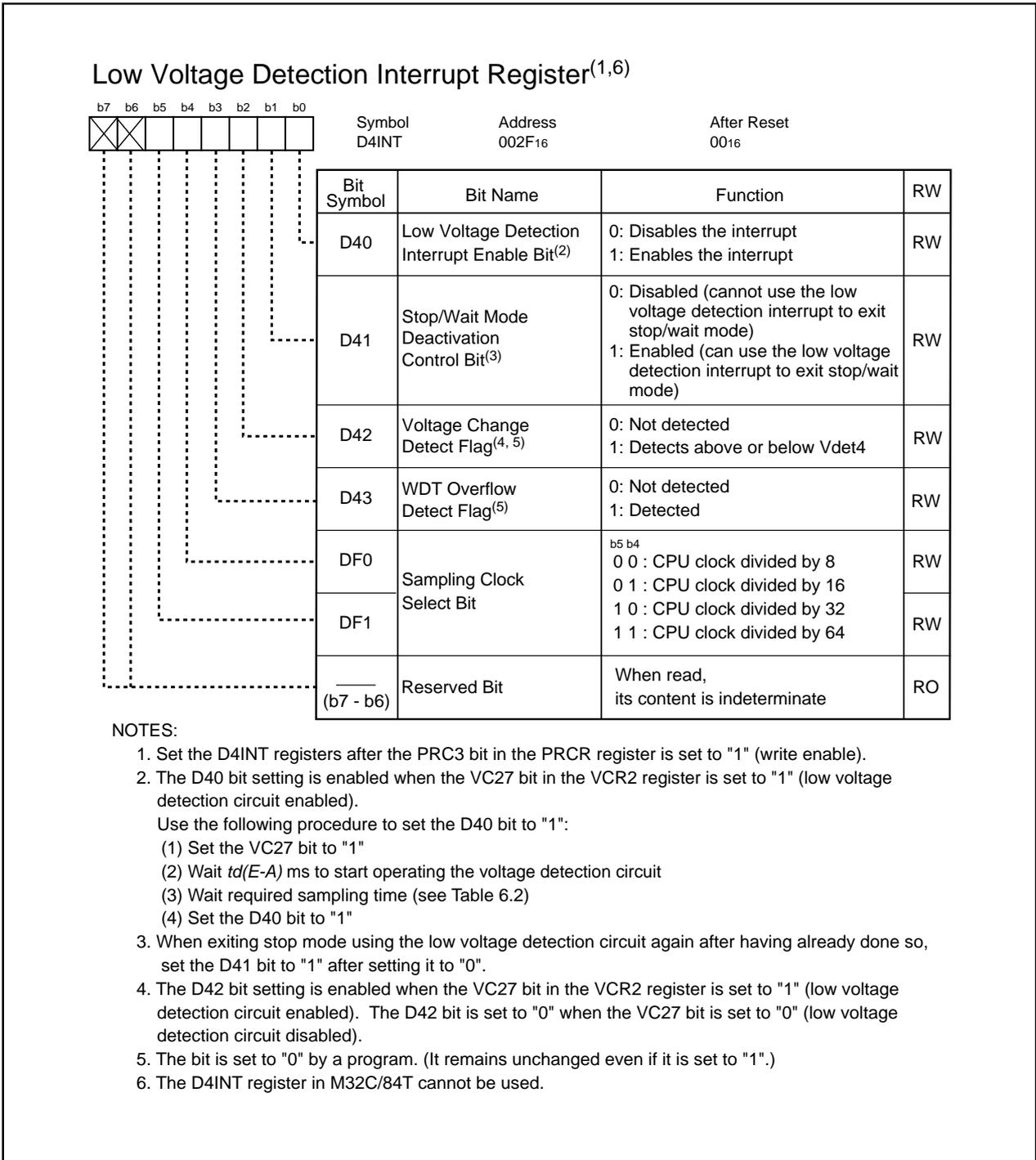


Figure 6.4 D4INT Register

6.1 Low Voltage Detection Interrupt

If the D40 bit in the D4INT register is set to "1" (low voltage detection interrupt enabled), low voltage detection interrupt request is generated when the voltage applied to the VCC1 pin rises above or drops below Vdet4. The low voltage detection interrupt shares the same interrupt vector with the watchdog timer interrupt and oscillation stop detection interrupt. The D42 bit in the D4INT register determines whether the low voltage detection interrupt has been generated. Read the D42 bit using an interrupt routine when using the low voltage detection interrupt at the same time as the watchdog timer interrupt and oscillation stop detection interrupt.

Set the D41 bit in the D4INT register to "1" (enabled) to use the low voltage detection interrupt to exit stop mode or wait mode.

The D42 bit is set to "1" (more or less than Vdet4 detected) as soon as the voltage applied to the VCC1 pin reaches Vdet4 due to the voltage rise and voltage drop. When the D42 bit setting changes "0" to "1", low voltage detection interrupt request is generated. Set the D42 bit to "0" (not detected) by program. However, when the D41 bit is set to "1" and the microcomputer is in stop mode or wait mode, low voltage detection interrupt request is generated, regardless of the D42 bit setting, if the voltage applied to the VCC1 pin is detected to be higher than Vdet4. The microcomputer then exits stop mode or wait mode.

Table 6.1 shows how a low voltage detection interrupt request is generated.

The DF1 and DF0 bits in the D4INT register determine sampling period that detects the voltage applied to the VCC1 pin rises above or drops below Vdet4. Table 6.2 shows the sampling periods.

Table 6.1 Conditions to Generate Low Voltage Detection Interrupt Request

Operating Mode	VC27 Bit	D40 Bit	D41 Bit	D42 Bit ⁽⁴⁾	VC13 Bit ⁽³⁾
Normal Operating Mode ⁽¹⁾	1	1	"0" or "1"	"0" to "1"	"0" to "1" "1" to "0"
Wait Mode ⁽²⁾ , Stop Mode ⁽²⁾			1	-	"0" to "1"

- : "0" or "1"

NOTES:

- All states excluding wait mode and stop mode are handled as normal operating mode. (**Refer to 9. Clock Generation Circuit.**)
- Refer to **6.1.1 Limitations for Exiting Stop/Wait Mode.**
- Sampling begins after the VC13 bit setting changes. An interrupt request is generated after sampling is completed. See Figure 6.6 for details.
- Set to "0" by program before generating an interrupt.

Table 6.2 Sampling Periods

CPU Clock (MHz)	Sampling Clock (μ s)			
	Divide-by-8	Divide-by-16	Divide-by-32	Divide-by-64
16	3.0	6.0	12.0	24.0
32	1.5	3.0	6.0	12.0

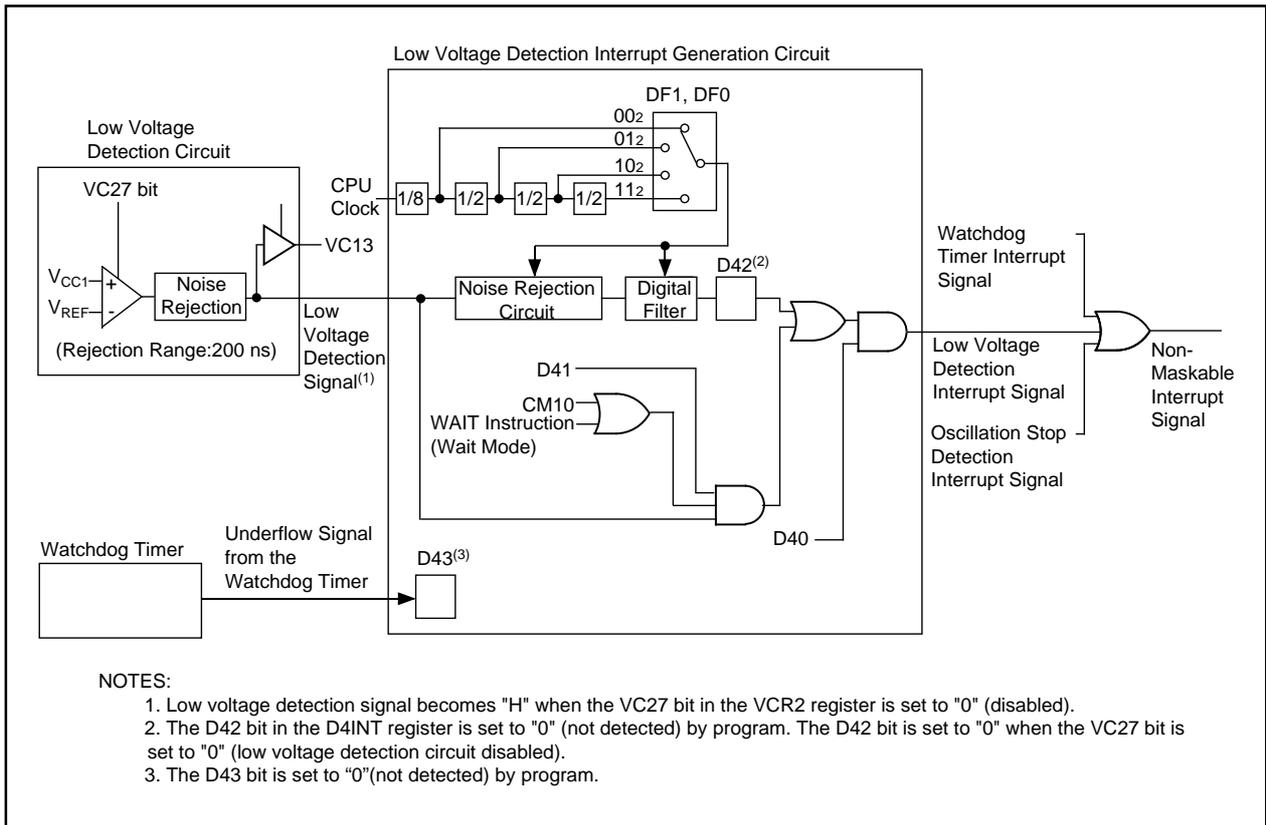


Figure 6.5 Low Voltage Detection Interrupt Generation Circuit

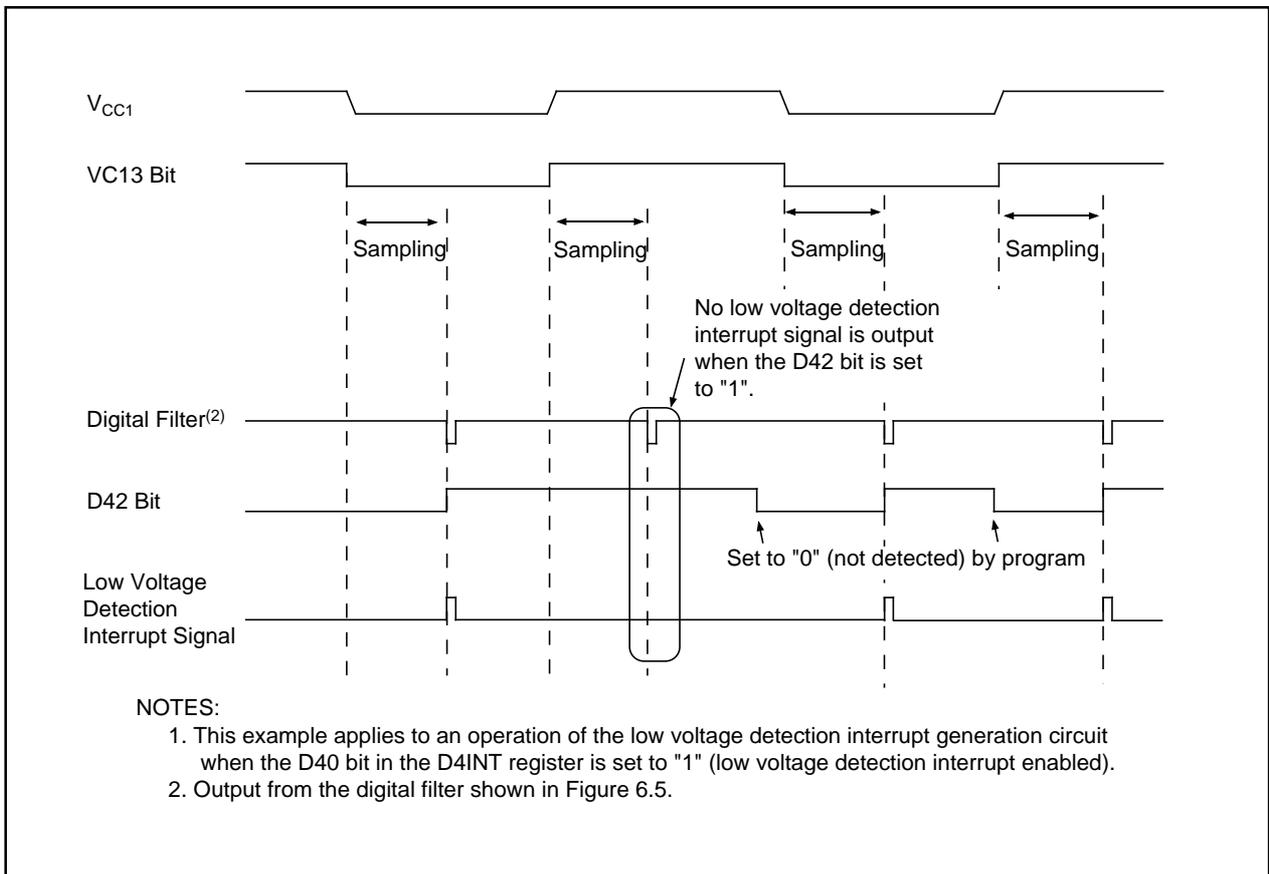


Figure 6.6 Low Voltage Detection Interrupt Generation Circuit Operation Example

6.1.1 Limitations on Exiting Stop/Wait Mode

The low voltage detection interrupt is generated and the microcomputer exits stop mode as soon as the CM10 bit in the CM1 register is set to "1" (all clocks stopped) under the conditions below. Additionally, if WAIT instruction is executed under these same conditions, the low voltage detection interrupt is immediately generated and the microcomputer exits wait mode.

- the VC27 bit in the VCR2 register is set to "1" (low voltage detection circuit enabled),
- the D40 bit in the D4INT register is set to "1" (low voltage detection interrupt enabled),
- the D41 bit in the D4INT register is set to "1" (low voltage detection interrupt is used to exit stop/wait mode), and
- the voltage applied to the VCC1 pin is higher than Vdet4 (the VC13 bit in the VCR1 register is set to "1")

Set the CM10 bit to "1" when the VC13 bit is "0" ($V_{CC1} < V_{det4}$), if the microcomputer is set to enter stop/wait mode when the voltage applied to the VCC1 pin drops below Vdet4 and to exit stop/wait mode when the voltage applied rises to Vdet4 or above.

6.2 Cold Start-up / Warm Start-up Determine Function

The WDC5 bit in the WDC register determines either cold start-up, power-on reset, or warm start-up, reset during the microcomputer running. Default value of the WDC5 bit is "0" (cold start-up) when power-on. It is set to "1" (warm start-up) by writing desired values to the WDC register. The WDC5 bit is not reset, regardless of a software reset or reset signal input.

Figure 6.7 shows a block diagram of the cold start-up/warm start-up determine function. Figure 6.8 shows its operation example.

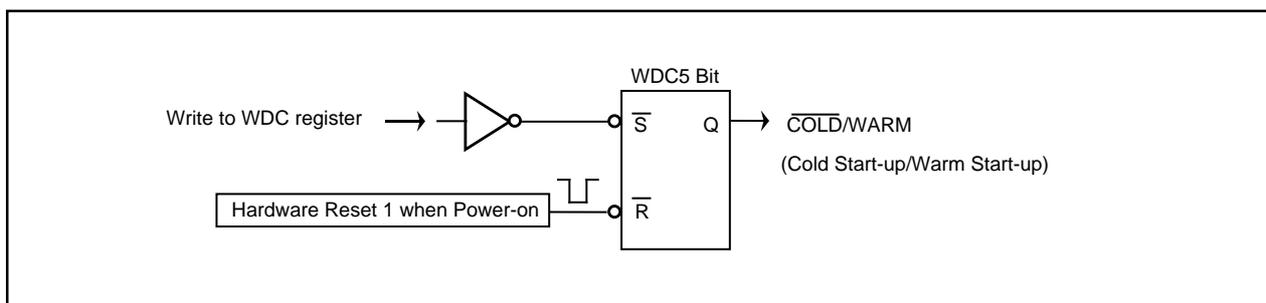


Figure 6.7 Cold Start-up/Warm Start-up Determine Function Block Diagram

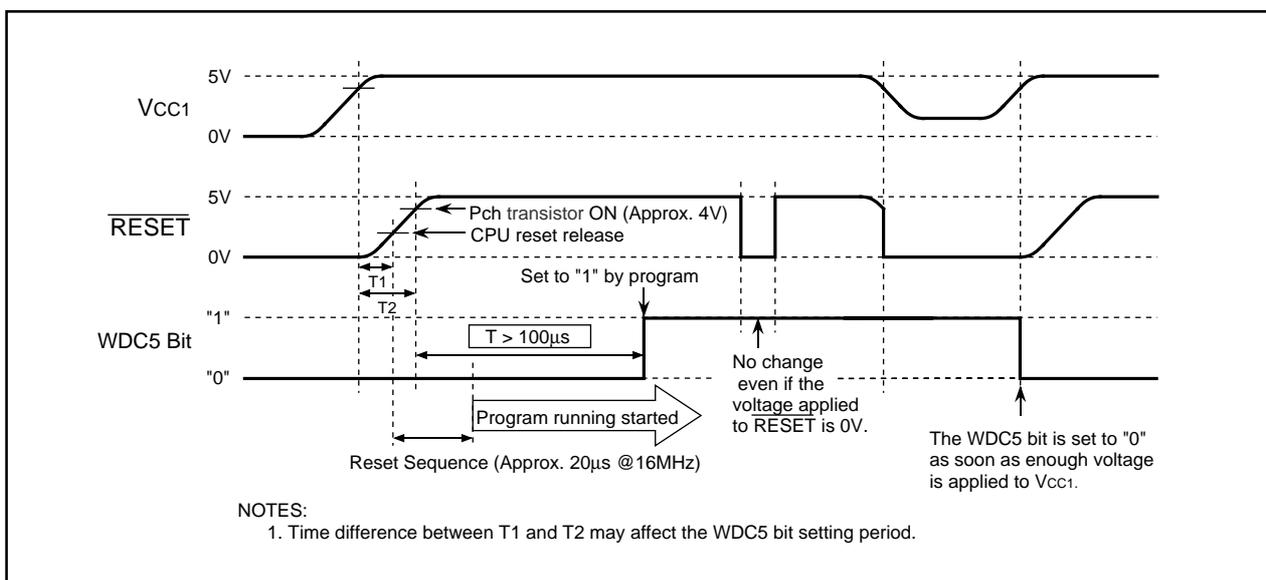


Figure 6.8 Cold Start-up/Warm Start-up Determine Function Operation

7. Processor Mode

NOTE

Use M32C/84T in single-chip mode only.
M32C/84T cannot be used in memory expansion mode and microprocessor mode.

7.1 Types of Processor Mode

Single-chip mode, memory expansion mode or microprocessor mode can be selected as a processor mode. Table 7.1 lists a feature of the processor mode.

Table 7.1 Processor Mode Feature

Processor Mode	Accessable Space	Pin Status as I/O Ports
Single-chip Mode	SFR, Internal RAM, Internal ROM	All pins assigned to I/O ports or to I/O pins for the peripheral functions
Memory Expansion Mode	SFR, Internal RAM, Internal ROM, External Space ⁽¹⁾	Some pins assigned to bus control pins ⁽¹⁾
Microprocessor Mode	SFR, Internal RAM, External Space ⁽¹⁾	Some pins assigned to bus control pins ⁽¹⁾

NOTES:

1. Refer to **8. Bus** for details.

7.2 Setting of Processor Mode

The CNVss pin state and the PM01 and PM00 bit settings in the PM0 register determine which processor mode is selected. Table 7.2 lists processor mode after hardware reset. Table 7.3 lists processor mode selected by PM01 and PM00 bit settings.

Table 7.2 Processor Mode after Hardware Reset

Input Level into the CNVss pin	Processor Mode
Vss	Single-chip Mode
Vcc ₁ ^(1,2)	Microprocessor Mode

NOTES:

1. The internal ROM cannot be accessed, regardless of PM01 and PM00 bit settings, when applying Vcc₁ to the CNVss pin and generating the hardware reset (hardware reset 1 or brown-out detection reset).
2. Multiplex bus cannot be assigned to all CS areas.

Table 7.3 Processor Mode Selected by the PM01 and PM00 bit Settings

PM01 and PM00 Bits	Processor Mode
002	Single-chip Mode
012	Memory Expansion Mode
102	Do not set to this value
112	Microprocessor Mode

If the PM01 and PM00 bits are rewritten, the mode corresponding to the PM01 and PM00 bits is selected regardless of CNVss pin level.

Do not change the PM01 and PM00 bits to "012" (memory expansion mode) or "112" (microprocessor mode) when the PM07 to PM02 bits in the PM0 register are being rewritten.

Do not enter microprocessor mode while the CPU is executing a program in the internal ROM.

Do not enter single-chip mode or memory expansion mode from microprocessor mode while the CPU is executing a program in an external memory space, the same address assigned for the internal ROM.

The internal ROM cannot be accessed, regardless of PM01 and PM00 bit settings, when applying Vcc₁ to the CNVSS pin and generating the hardware reset (hardware reset 1 or low voltage detection reset).

Figures 7.1 and 7.2 show the PM0 register and PM1 register. Figure 7.3 shows a memory map in each processor mode.

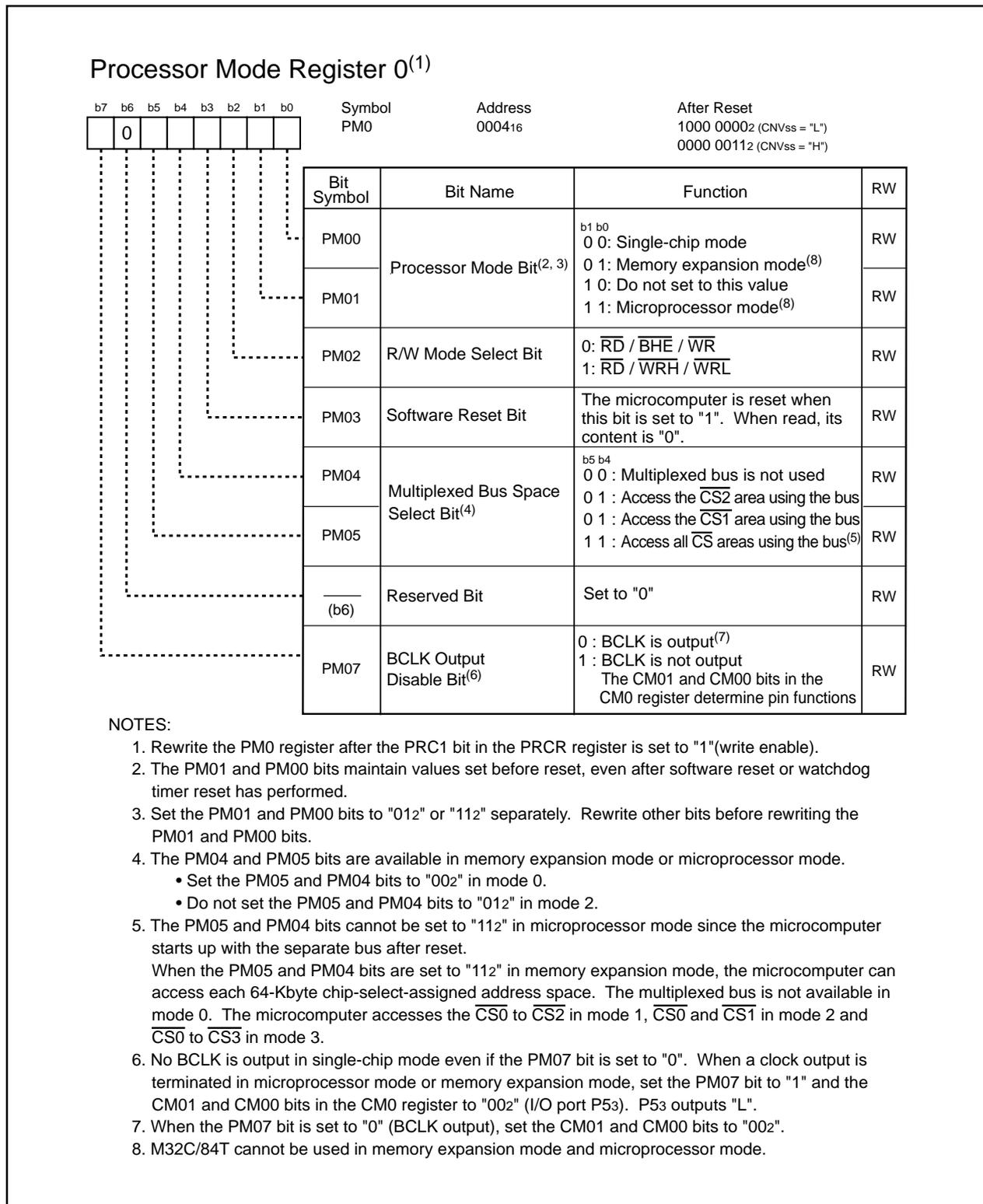
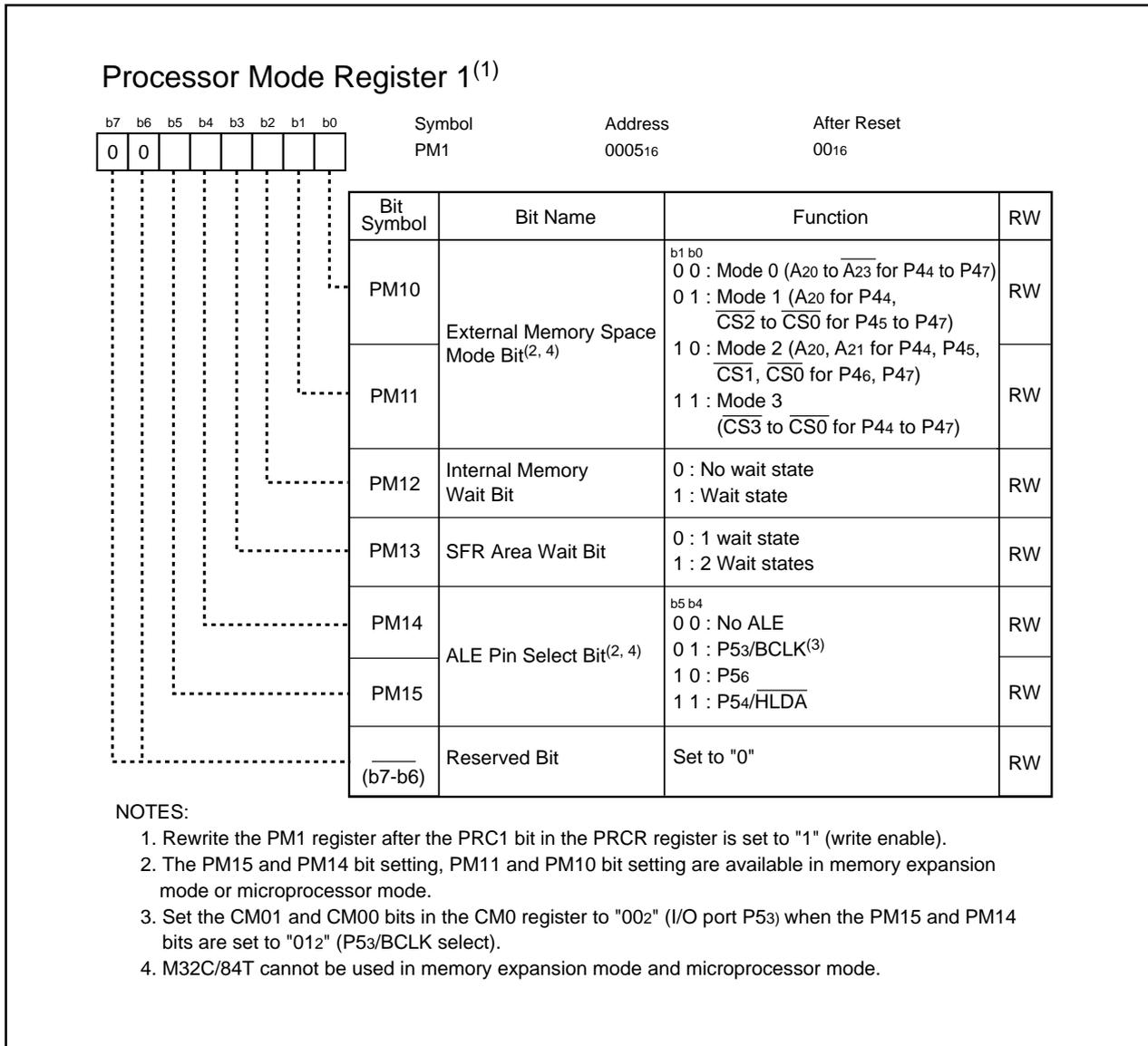


Figure 7.1 PM0 Register

**Figure 7.2 PM1 Register**

	Memory Expansion Mode				Microprocessor Mode			
	Mode 0	Mode 1	Mode 2	Mode 3	Mode 0	Mode 1	Mode 2	Mode 3
000000 ₁₆	SFR	SFR	SFR	SFR	SFR	SFR	SFR	SFR
000400 ₁₆	Internal RAM	Internal RAM	Internal RAM	Internal RAM	Internal RAM	Internal RAM	Internal RAM	Internal RAM
00F000 ₁₆	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space
010000 ₁₆	Block A ⁽³⁾	Block A ⁽³⁾	Block A ⁽³⁾	Block A ⁽³⁾	External Space 0	External Space 0	External Space 0	External Space 0
100000 ₁₆	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0	External Space 0
200000 ₁₆	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1
300000 ₁₆	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1	External Space 1
400000 ₁₆	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2	External Space 2
C00000 ₁₆	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3	External Space 3
D00000 ₁₆	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space
E00000 ₁₆	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space	Reserved Space
F00000 ₁₆	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM
FFFFFF ₁₆	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM	Internal ROM

The EWCRi register (i=0 to 3) can determine how many wait states are inserted for each space CS0 to CS3.

NOTES:

- 200000₁₆ - 010000₁₆=1984 Kbytes. 64K bytes less than 2 Mbytes.
- 400000₁₆ - 010000₁₆=4032 Kbytes. 64K bytes less than 4 Mbytes.
- Additional 4-Kbyte space is provided in the flash memory version for storing data.

Figure 7.3 Memory Map in Each Processor Mode

8. Bus

In memory expansion mode or microprocessor mode, some pins function as bus control pins to control the address bus and data bus. A0 to A22, $\overline{A}23$, D0 to D15, CS0 to CS3, WRL/WR, WRH/BHE, RD, BCLK/ALE, $\overline{HLDA/ALE}$, \overline{HOLD} , ALE, \overline{RDY} are used as bus control pins.

NOTE

Bus control pins in M32C/84T cannot be used.

8.1 Bus Settings

The BYTE pin, the DS register, the PM05 and PM04 bits in the PM0 register and the PM11 and PM10 bits in the PM1 register determine bus settings.

Table 8.1 lists how to change bus settings. Figure 8.1 shows the DS register.

Table 8.1 Bus Settings

Bus Setting	Changed By
Selecting External Address Bus Width	DS register
Setting Bus Width after Reset	BYTE pin (external space 3 only)
Selecting Between Separate Bus or Multiplexed Bus	PM05 and PM04 bits in PM0 register
Number of Chip-Select	PM11 and PM10 bits in PM1 register

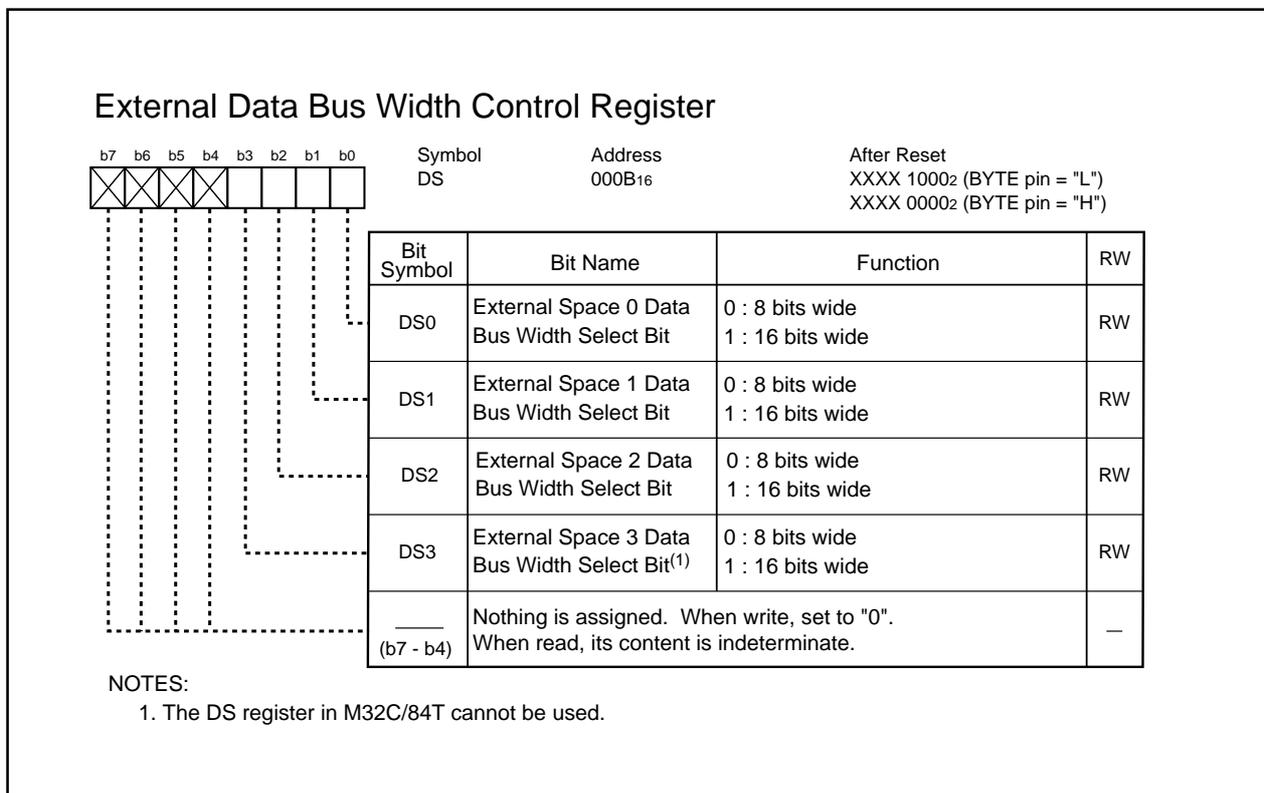


Figure 8.1 DS Register

8.1.1 Selecting External Address Bus

The number of externally-output address buses, the number of chip-select signals and chip-select-assigned address space (\overline{CS} area) vary depending on each external space mode. The PM11 and PM10 bits in the PM1 register determine the external space mode.

8.1.2 Selecting External Data Bus

The DS register selects either external 8-bit or 16-bit data bus per external space. The data bus in the external space 3, after reset, becomes 16 bits wide when a low-level ("L") signal is applied to the BYTE pin and 8 bits wide when a high-level ("H") signal is applied. Keep the BYTE pin input level while the microcomputer is operating. Internal bus is always 16 bits wide.

8.1.3 Selecting Separate/Multiplexed Bus

The PM05 and PM04 bits in the PM0 register determine either separate or multiplexed bus as bus format.

8.1.3.1 Separate Bus

The separate bus is a bus format which allows the microcomputer to input and output data and address separately. The DS register selects 8-bit or 16-bit data bus as the external data bus per external space. If all DS_i bits in the DS register (i=0 to 3) are set to "0" (8-bit data bus), port P0 becomes the data bus and port P1, the programmable I/O port. If one of the DS_i bits is set to "1" (16-bit data bus), ports P0 and P1 become the data bus. Port P1 is indeterminate when the microcomputer accesses a space where the DS_i bit is set to "0".

The EWCR_i register (i=0 to 3) determines the number of software wait states inserted, when the microcomputer accesses space using the separate bus.

8.1.3.2 Multiplexed Bus

The multiplexed bus is a bus format which allow the microcomputer to input and output data and address by timesharing. D₀ to D₇ are multiplexed with A₀ to A₇ in space accessed by the 8-bit data bus. D₀ to D₁₅ are multiplexed with A₀ to A₁₅ in space accessed by the 16-bit data bus. The DS_i bit controls the data bus width. The EWCR_i register (i=0 to 3) controls the number of software wait states inserted, when the microcomputer accesses a space using the multiplexed bus. Refer to **8.2.4 Bus Timing** for details.

The multiplexed bus can be assigned to access the $\overline{CS1}$ area, $\overline{CS2}$ area or all \overline{CS} areas. However, because the microcomputer starts operation using the separate bus after reset, the multiplexed bus cannot be assigned to access all \overline{CS} areas in microprocessor mode. When the PM05 and PM04 bits in the PM0 register are set to "112" (access all \overline{CS} areas with the bus), 16 low-order bits, from A₀ to A₁₅, of an address are output. See **Table 8.2** for details.

Table 8.2 Processor Mode and Port Function

Processor Mode	Single-Chip Mode	Memory Expansion Mode/ Microprocessor Mode				Memory Expansion Mode	
PM05 to PM04 Bits in PM0 Register		"012", "102" (Access CS1 or CS2 using the Multiplexed Bus Access All Other CS Areas using the Separate Bus)		"002" (Access all \overline{CS} Areas using the Separate Bus)		"112" ⁽¹⁾ (Access all \overline{CS} Areas using the Multiplexed Bus)	
Data Bus Width		Access all external space with 8-bit data bus	Access one or more external space with 16-bit data bus	Access all external space with 8-bit data bus	Access one or more external space with 16-bit data bus	Access all external space with 8-bit data bus	Access one or more external space with 16-bit data bus
P00 to P07	I/O port	Data bus D0 to D7	Data bus D0 to D7	Data bus D0 to D7	Data bus D0 to D7	I/O port	I/O port
P10 to P17	I/O port	I/O port	Data bus D8 to D15	I/O port	Data bus D8 to D15	I/O port	I/O port
P20 to P27	I/O port	Address bus Data bus ⁽²⁾ A0/D0 to A7/D7	Address bus Data bus ⁽²⁾ A0/D0 to A7/D7	Address bus A0 to A7	Address bus A0 to A7	Address bus Data bus A0/D0 to A7/D7	Address bus Data bus A0/D0 to A7/D7
P30 to P37	I/O port	Address bus A8 to A15	Address bus/ Data bus ⁽²⁾ A8/D8 to A15/D15	Address bus A8 to A15	Address bus A8 to A15	Address bus A8 to A15	Address bus/ Data bus A8/D8 to A15/D15
P40 to P43	I/O port	Address bus A16 to A19	Address bus A16 to A19	Address bus A16 to A19	Address bus A16 to A19	I/O port	I/O port
P44 to P46	I/O port	\overline{CS} (Chip-select signal) or Address bus (A20 to A22) (Refer to 8.2 Bus Control for details) ⁽⁴⁾					
P47	I/O port	\overline{CS} (Chip-select signal) or Address bus ($\overline{A23}$) (Refer to 8.2 Bus Control for details) ⁽⁴⁾					
P50 to P53	I/O port	Outputs \overline{RD} , \overline{WRL} , \overline{WRH} and BCLK or outputs \overline{RD} , \overline{BHE} , \overline{WR} and BCLK (Refer to 8.2 Bus Control for details) ⁽³⁾					
P54	I/O port	\overline{HDLA} ⁽³⁾	\overline{HDLA} ⁽³⁾	\overline{HDLA} ⁽³⁾	\overline{HDLA} ⁽³⁾	\overline{HDLA} ⁽³⁾	\overline{HDLA} ⁽³⁾
P55	I/O port	\overline{HOLD}	\overline{HOLD}	\overline{HOLD}	\overline{HOLD}	\overline{HOLD}	\overline{HOLD}
P56	I/O port	ALE ⁽³⁾	ALE ⁽³⁾	ALE ⁽³⁾	ALE ⁽³⁾	ALE ⁽³⁾	ALE ⁽³⁾
P57	I/O port	\overline{RDY}	\overline{RDY}	\overline{RDY}	\overline{RDY}	\overline{RDY}	\overline{RDY}

NOTES:

- The PM05 and PM04 bits cannot be set to "112" (access all \overline{CS} areas using multiplexed bus) in microprocessor mode because the microcomputer starts operation using the separate bus after reset.
When the PM05 and PM04 bits are set to "112" in memory expansion mode, the microcomputer accesses 64-Kbyte memory space per chip-select using the address bus .
- These ports become address buses when accessing space using the separate bus.
- The PM15 and PM14 bits in the PM1 register determines which pin outputs the ALE signal. The PM02 bit in the PM0 register selects either " $\overline{WRL}, \overline{WRH}$ " or " $\overline{BHE}, \overline{WR}$ " combination.
P56 provides an indeterminate output when the PM15 and PM14 bits to "002" (no ALE). It cannot be used as an I/O port.
- The PM11 and PM10 bits in the PM1 register determine the CS signal and address bus.

8.2 Bus Control

Signals, required to access external devices, are provided and software wait states are inserted as follows. The signals are available in memory expansion mode and microprocessor mode only.

8.2.1 Address Bus and Data Bus

Address bus is a signal accessing 16-Mbyte space and uses 24 control pins; A0 to A22 and $\overline{A23}$. $\overline{A23}$ is the inversed output signal of the highest-order address bit.

Data bus is a signal for data input and output. The DS register selects an 8-bit data bus from D0 to D7 or a 16-bit data bus from D0 to D15 for each external space. When applying a high-level ("H") signal to the BYTE pin, the data bus accessing the external memory space 3 becomes an 8-bit data bus after reset. When applying a low-level ("L") signal to the BYTE pin, the data bus accessing the external memory space 3 becomes the 16-bit data bus.

When changing single-chip mode to memory expansion mode, the address bus is in an indeterminate state until the microcomputer accesses an external memory space.

8.2.2 Chip-Select Signal

Chip-select signal shares pins with A20 to A22 and $\overline{A23}$. The PM11 and PM10 bits in the PM1 register determine which \overline{CS} area is accessed and how many chip-select signals are output. A maximum of four chip-select signals can be output.

In microprocessor mode, no chip-select signal, aside from $\overline{A23}$ which can perform as a chip-select signal, is output after reset.

The chip-select signal becomes "L" while the microcomputer is accessing the external \overline{CS}_i area (i=0 to 3). It becomes "H" while the microcomputer is accessing other external memory space.

Figure 8.2 shows an example of the address bus and chip-select signal output.

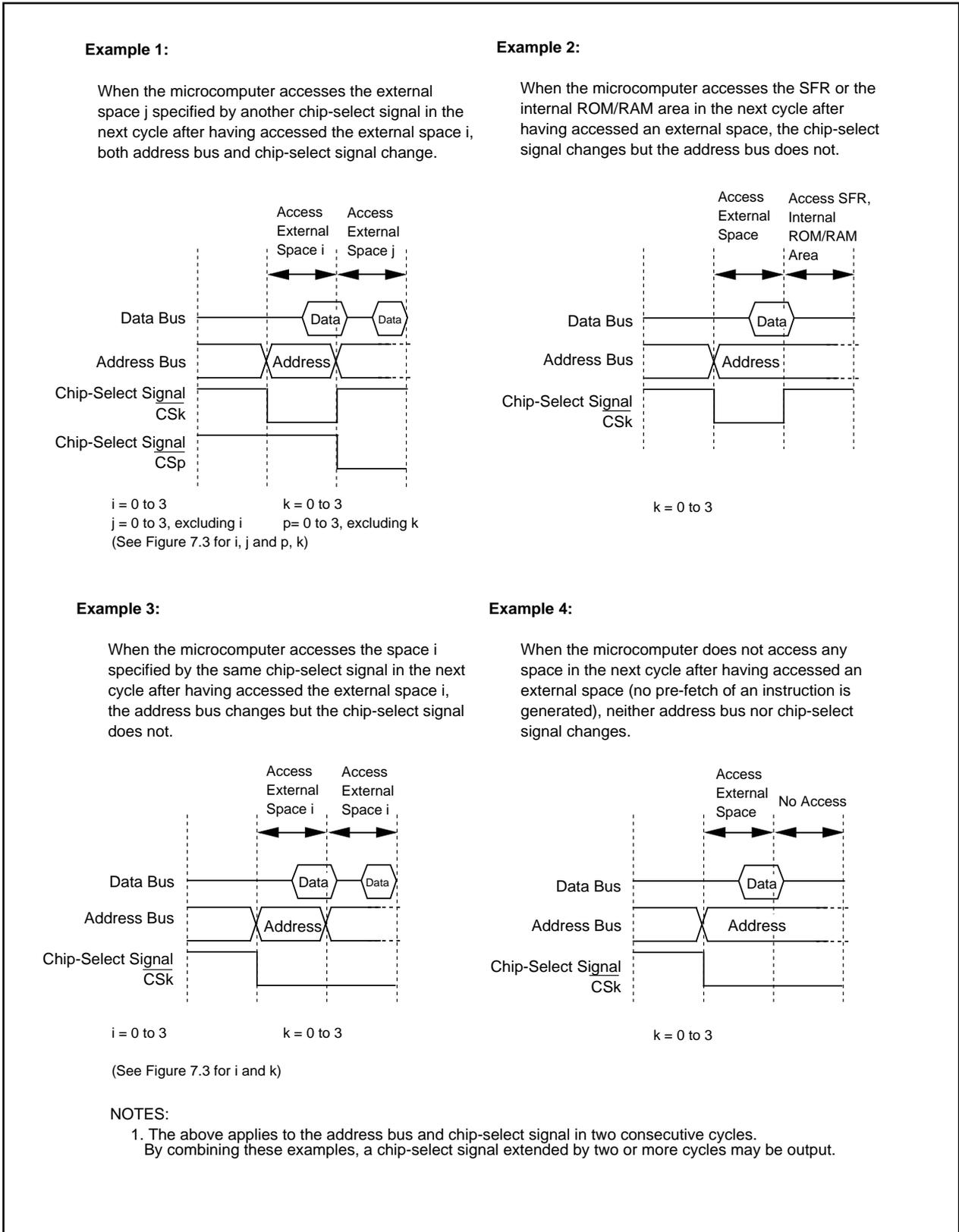


Figure 8.2 Address Bus and Chip-Select Signal Outputs (Separate Bus)

8.2.3 Read and Write Signals

When using a 16-bit data bus, the PM02 bit in the PM0 register selects a combination of the " \overline{RD} , \overline{WR} and \overline{BHE} " signals or the " \overline{RD} , \overline{WRL} and \overline{WRH} " signals to determine the read or write signal. When the DS3 to DS0 bits in the DS register are set to "0" (8-bit data bus), set the PM02 bit to "0" ($\overline{RD}/\overline{WR}/\overline{BHE}$). When any of the DS3 to DS0 bits are set to "1" (16-bit data bus) to access an 8-bit space, the combination of " \overline{RD} , \overline{WR} and \overline{BHE} " is automatically selected regardless of the PM02 bit setting. Tables 8.3 and 8.4 list each signal operation.

The \overline{RD} , \overline{WR} and \overline{BHE} signals are combined for the read or write signal after reset.

When changing the combination of " \overline{RD} , \overline{WRL} and \overline{WRH} ", set the PM02 bit first to write data to an external memory.

Table 8.3 \overline{RD} , \overline{WRL} and \overline{WRH} Signals

Data Bus	\overline{RD}	\overline{WRL}	\overline{WRH}	Status of External Data Bus
16 Bits	L	H	H	Read data
	H	L	H	Write 1-byte data to even address
	H	H	L	Write 1-byte data to odd address
	H	L	L	Write data to both even and odd addresses
8 Bits	H	L ⁽¹⁾	Not used	Write 1-byte data
	L	H ⁽¹⁾	Not used	Read 1-byte data

NOTES:

1. The \overline{WR} signal is used instead of the \overline{WRL} signal.

Table 8.4 \overline{RD} , \overline{WR} and \overline{BHE} Signals

Data Bus	\overline{RD}	\overline{WR}	\overline{BHE}	A0	Status of External Data Bus
16 Bits	H	L	L	H	Write 1-byte data to odd address
	L	H	L	H	Read 1-byte data from odd address
	H	L	H	L	Write 1-byte data to even address
	L	H	H	L	Read 1-byte data from even address
	H	L	L	L	Write data to both even and odd addresses
	L	H	L	L	Read data from both even and odd addresses
8 Bits	H	L	Not used	H / L	Write 1-byte data
	L	H	Not used	H / L	Read 1-byte data

8.2.4 Bus Timing

Bus cycle for the internal ROM and internal RAM is basically one BCLK cycle. When the PM12 bit in the PM1 register is set to "1" (wait state), the bus cycles are two BCLK cycles.

Bus cycles for the SFR are basically two BCLK cycles.

Basic bus cycle for an external space is 2ϕ ($1\phi+1\phi$) to read and to write. Bus cycle is selected by the EWCRi register (i=0 to 3) from 12 types of separate bus settings and 7 types of multiplexed bus settings. If the EWCRi04 to EWCRi00 bits are set to "000112" ($1\phi+3\phi$), bus cycles are four BCLK cycles.

Figure 8.3 shows the EWCRi register. Figures 8.4 to 8.8 show bus timing in an external space.

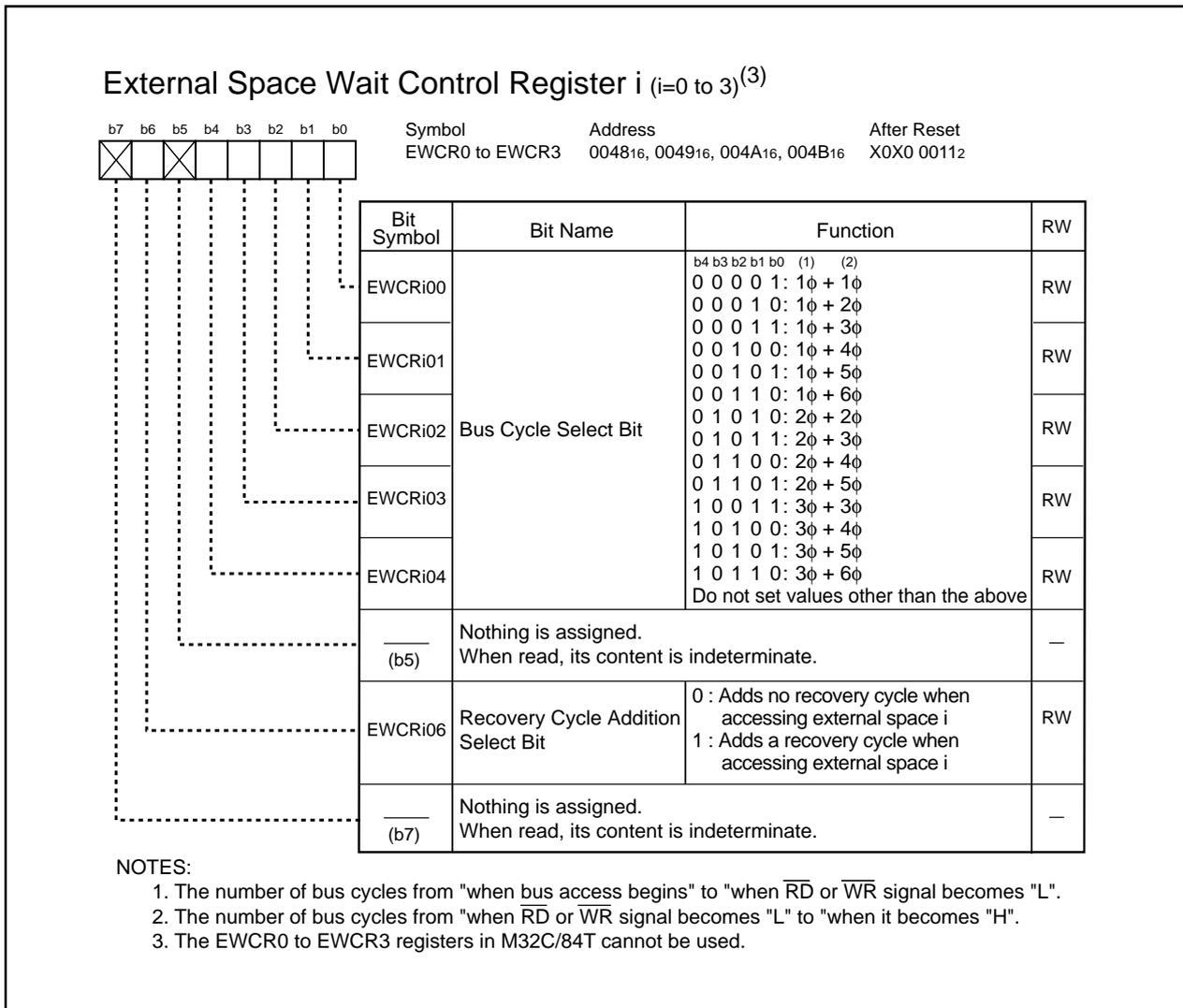


Figure 8.3 EWCR0 to EWCR3 Registers

Table 8.5 Software Wait State and Bus Cycle

Space	External Bus Status	PM1 Register		EWCRi Register (i=0 to 3)	Bus Cycles	
		PM13 Bit	PM12 Bit	EWCRi04 to EWCRi00 Bits		
SFR	---	0	---	---	2 BCLK cycles	
		1			3 BCLK cycles	
Internal ROM/RAM	---	---	0	--	1 BCLK cycles	
			1		2 BCLK cycles	
External Memory	Separate Bus	---	---	000012	2 BCLK cycles	
				000102	3 BCLK cycles	
				000112	4 BCLK cycles	
				001002	5 BCLK cycles	
				001012	6 BCLK cycles	
				001102	7 BCLK cycles	
				010102	4 BCLK cycles	
				010112	5 BCLK cycles	
				011002	6 BCLK cycles	
				100112	6 BCLK cycles	
				101002	7 BCLK cycles	
				101102	9 BCLK cycles	
	Multiplexed Bus	---	---	---	010102	4 BCLK cycles
					010112	5 BCLK cycles
					011012	7 BCLK cycles
					100112	6 BCLK cycles
					101002	7 BCLK cycles
					101012	8 BCLK cycles
				101102	9 BCLK cycles	

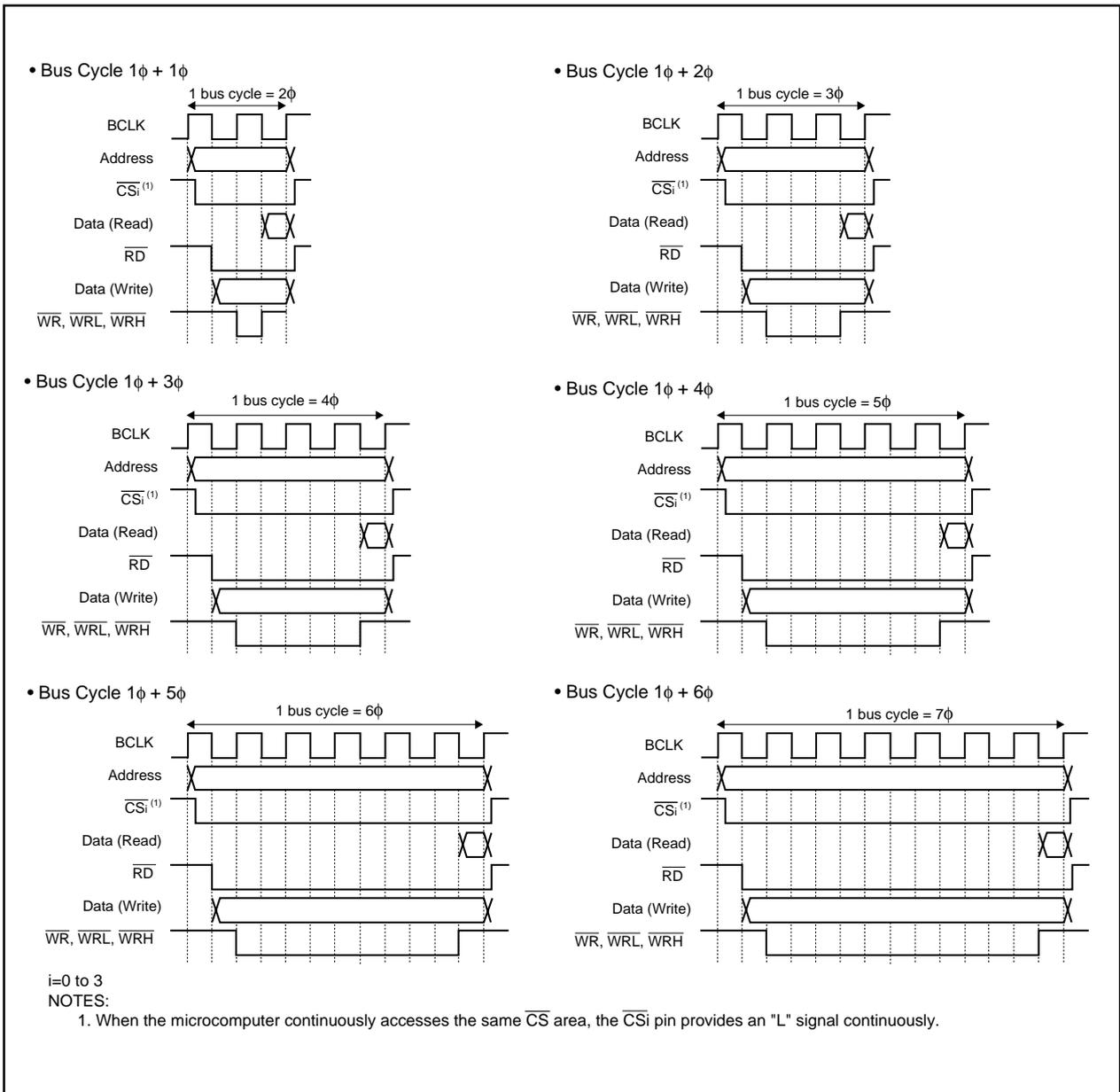


Figure 8.4 Bus Cycle with Separate Bus (1)

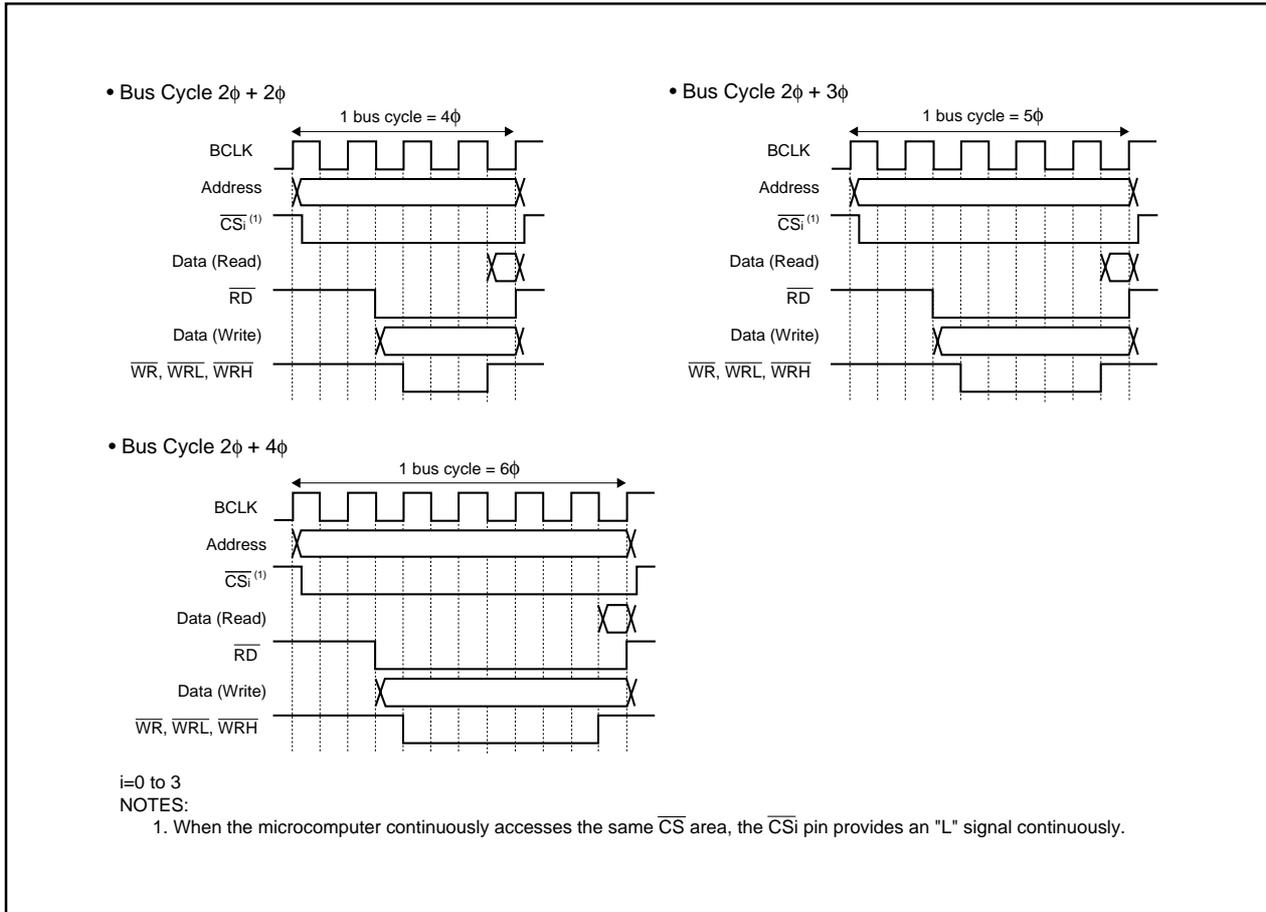


Figure 8.5 Bus Cycle with Separate Bus (2)

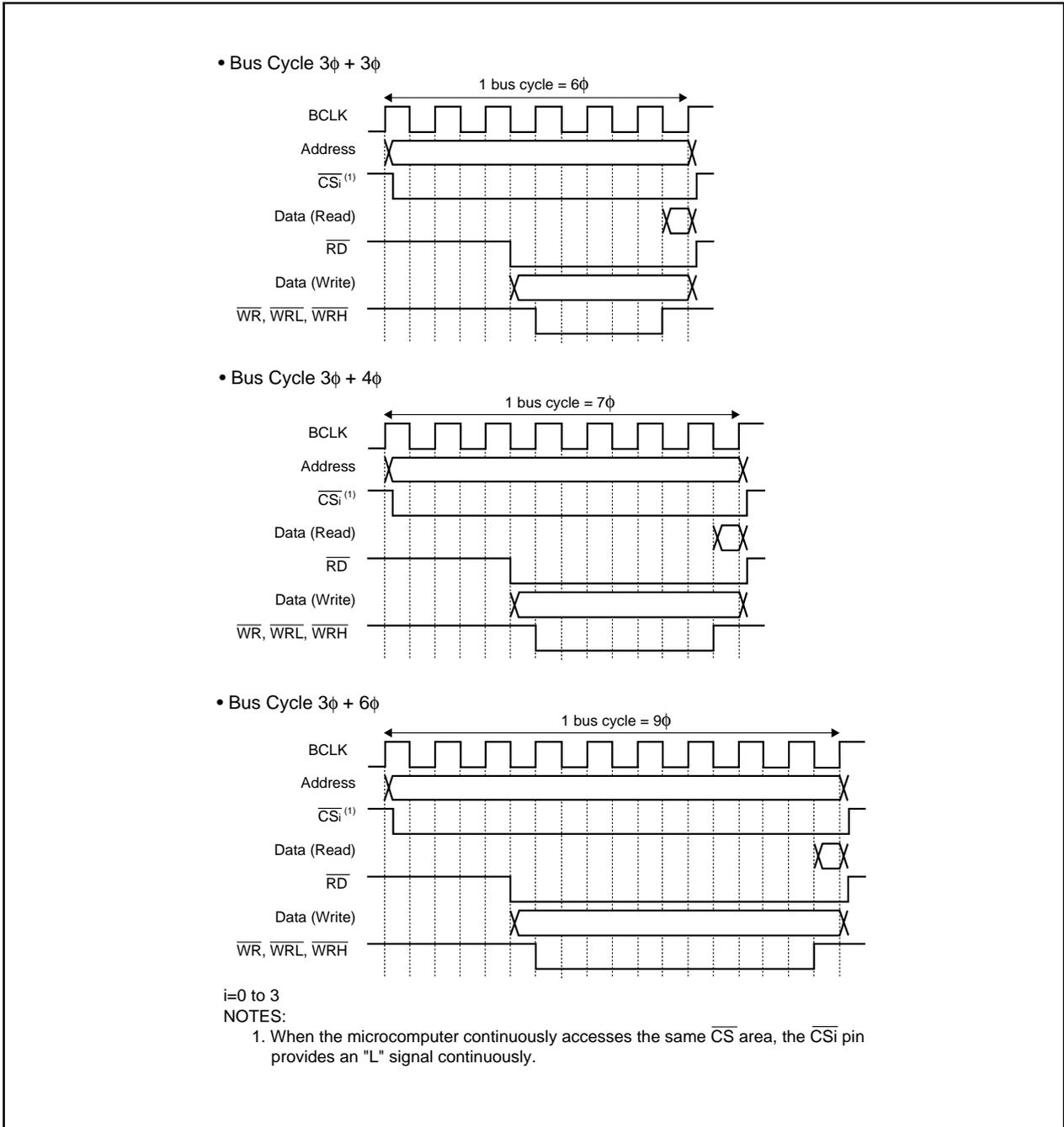


Figure 8.6 Bus Cycle with Separate Bus (3)

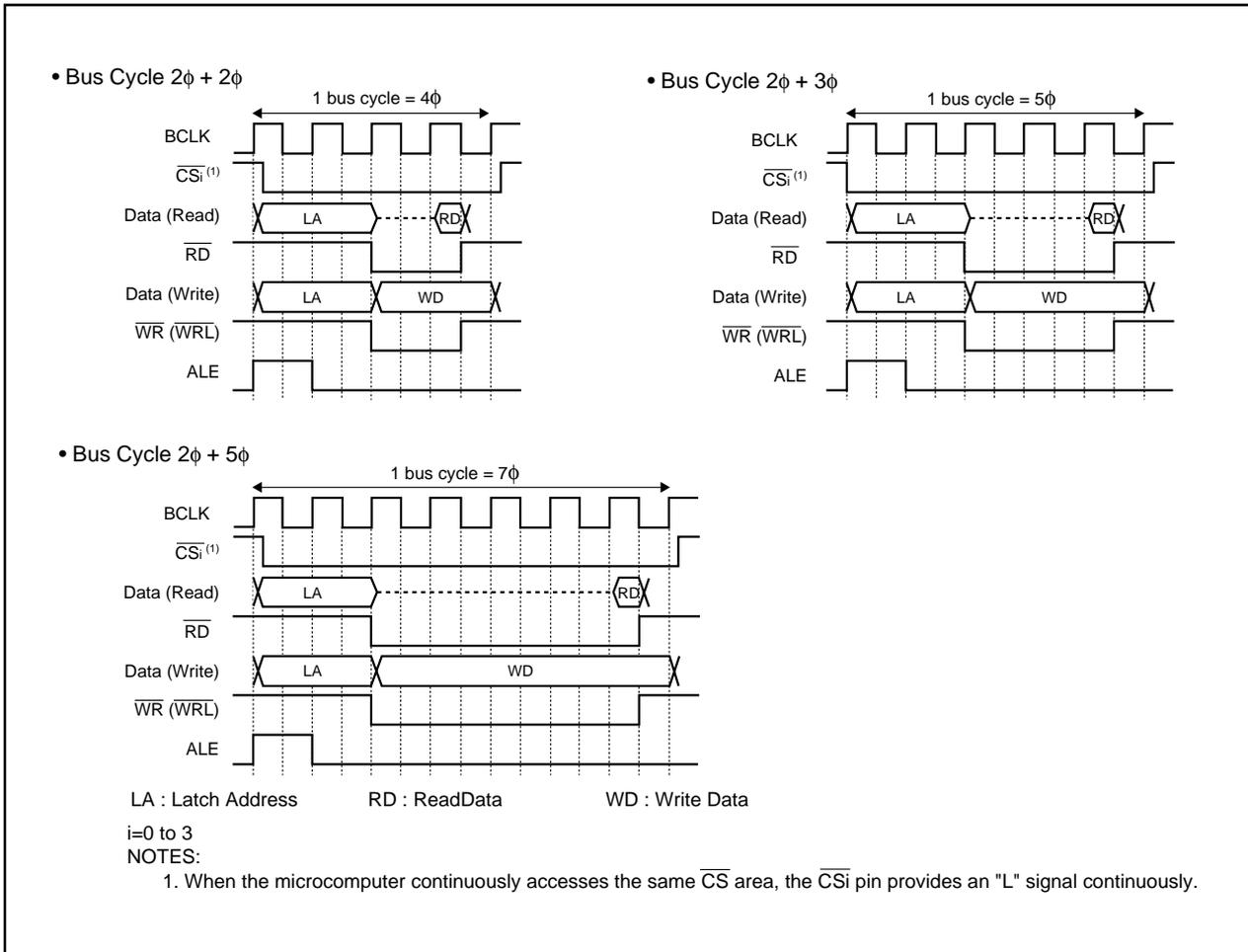


Figure 8.7 Bus Cycle with Multiplexed Bus (1)

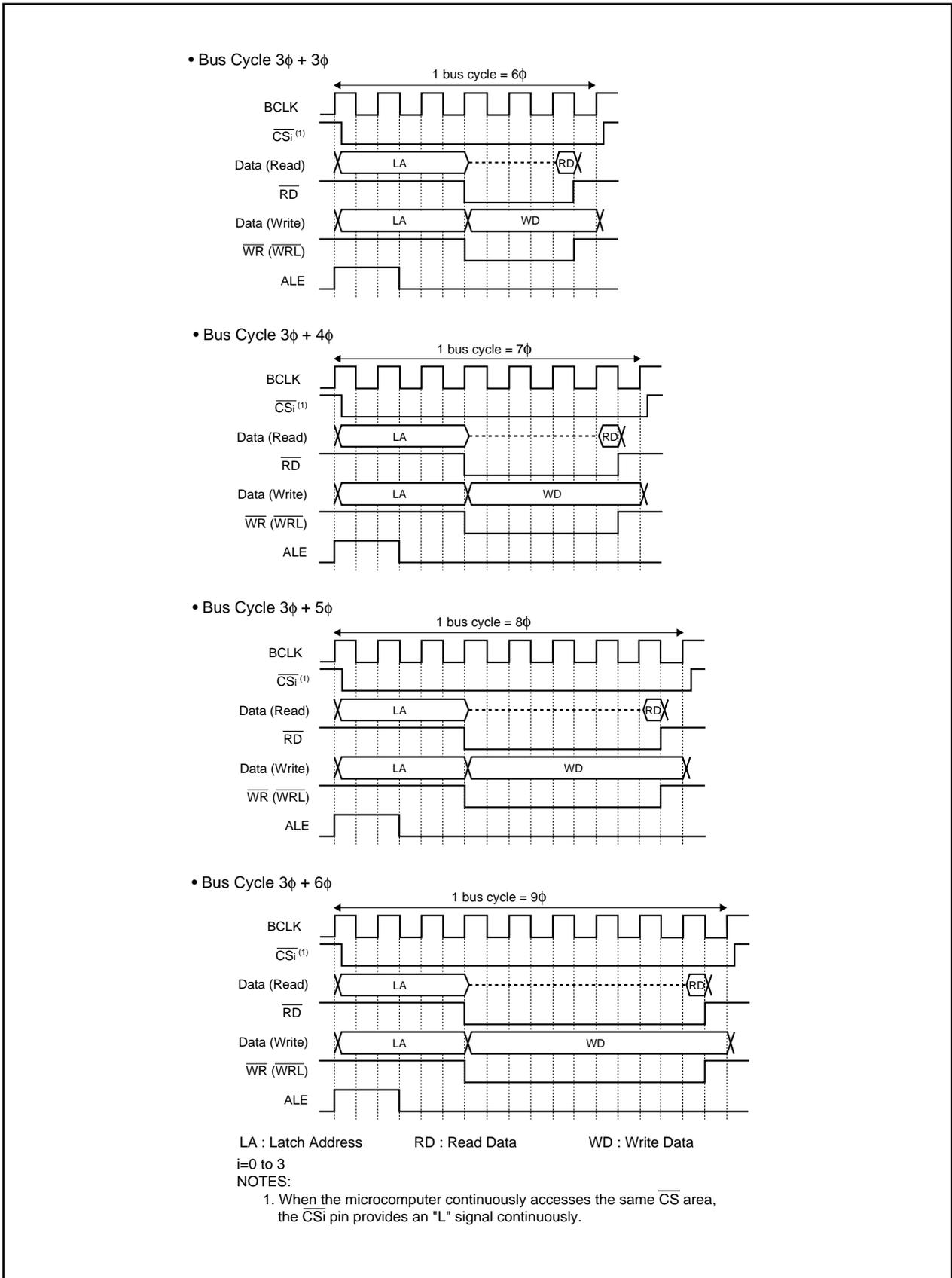


Figure 8.8 Bus Cycle with Multiplexed Bus (2)

8.2.4.1 Bus Cycle with Recovery Cycle Added

The EWCRi06 bit in the EWCRi register (i=0 to 3) determines whether the recovery cycle is added or not. In the recovery cycle, addresses and write data outputs are provided continuously (using the separate bus only). Devices, which take longer address hold time and data hold time to write data, are connectable.

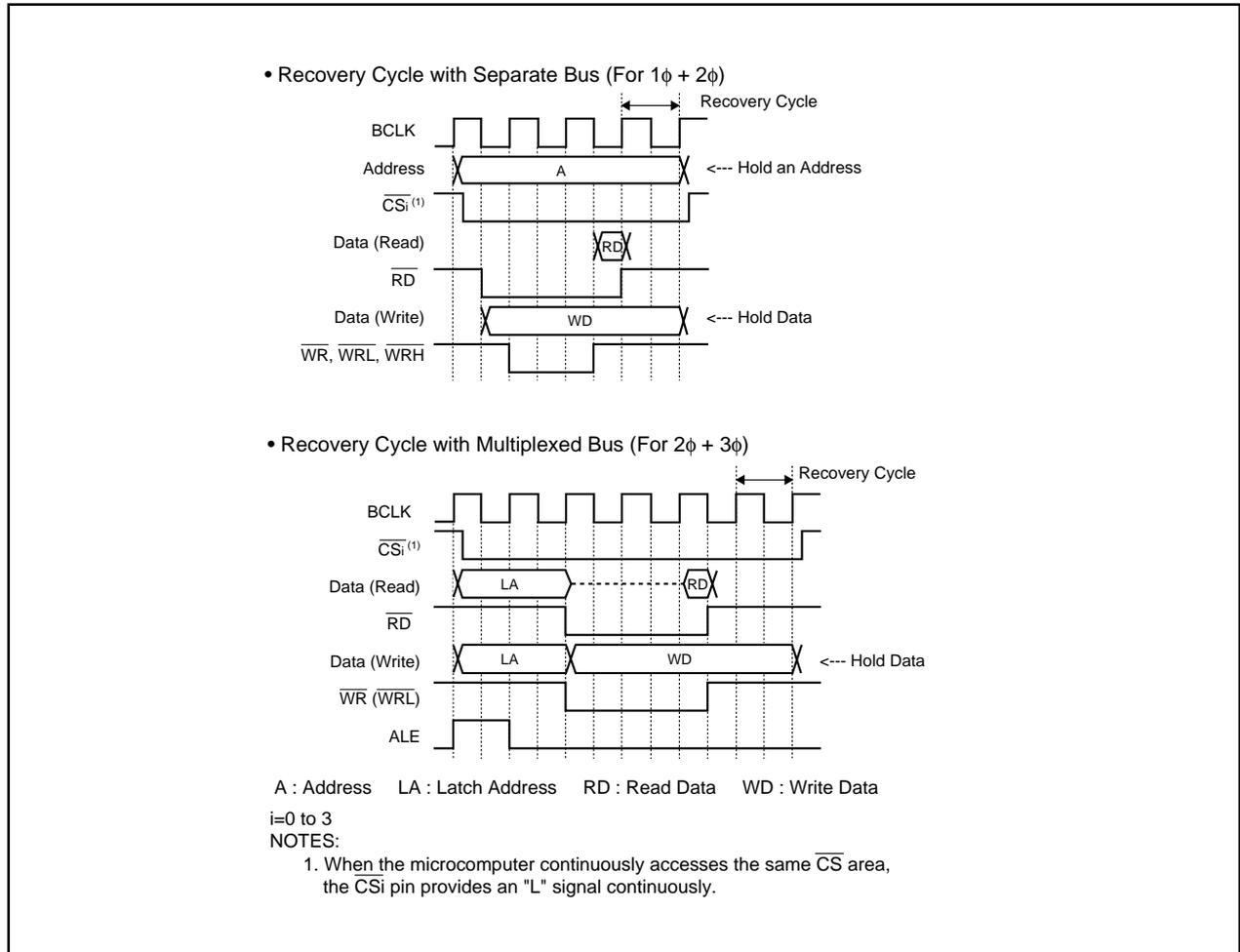


Figure 8.9 Recovery Cycle

8.2.5 ALE Signal

The ALE signal latches an address of the multiplexed bus. Latch an address on the falling edge of the ALE signal. The PM15 and PM14 bits in the PM1 register determine the output pin for the ALE signal. The ALE signal is output to internal space and external space.

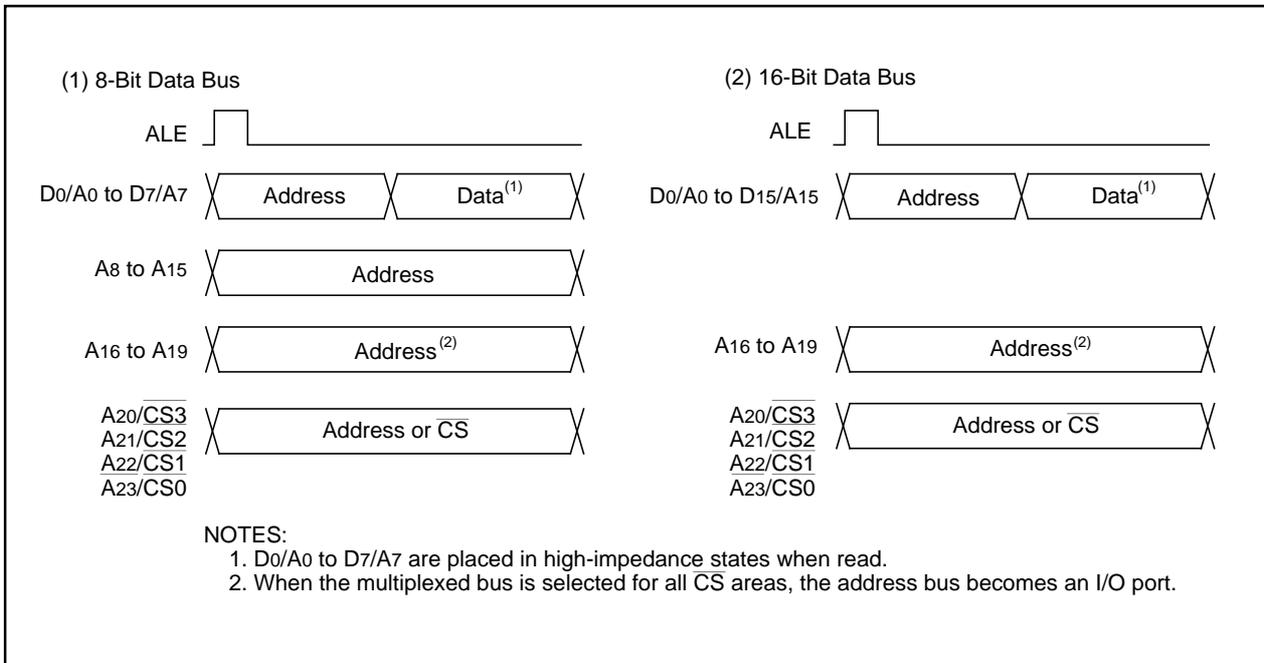


Figure 8.10 ALE Signal and Address/Data Bus

8.2.6 RDY Signal

The $\overline{\text{RDY}}$ signal facilitates access to external devices requiring longer access time. When a low-level ("L") signal is applied to the $\overline{\text{RDY}}$ pin on the falling edge of the last BCLK of the bus cycle, wait states are inserted into the bus cycle. When a high-level ("H") signal is applied to the $\overline{\text{RDY}}$ pin on the falling edge of BCLK, the bus cycle starts running again.

Table 8.6 lists microcomputer states when the $\overline{\text{RDY}}$ signal inserts wait states into the bus cycle. Figure 8.11 shows an example of the $\overline{\text{RD}}$ signal that is extended by the $\overline{\text{RDY}}$ signal.

Table 8.6 Microcomputer States in Wait State⁽¹⁾

Item	State
Oscillation	On
$\overline{\text{RD}}$ Signal, $\overline{\text{WR}}$ Signal, Address Bus, Data Bus, $\overline{\text{CS}}$, ALE Signal, $\overline{\text{HLDA}}$, Programmable I/O Ports	Maintains the same state as when $\overline{\text{RDY}}$ signal was received
Internal Peripheral Circuits	On

NOTES:

1. The $\overline{\text{RDY}}$ signal cannot be accepted immediately before software wait states are inserted.

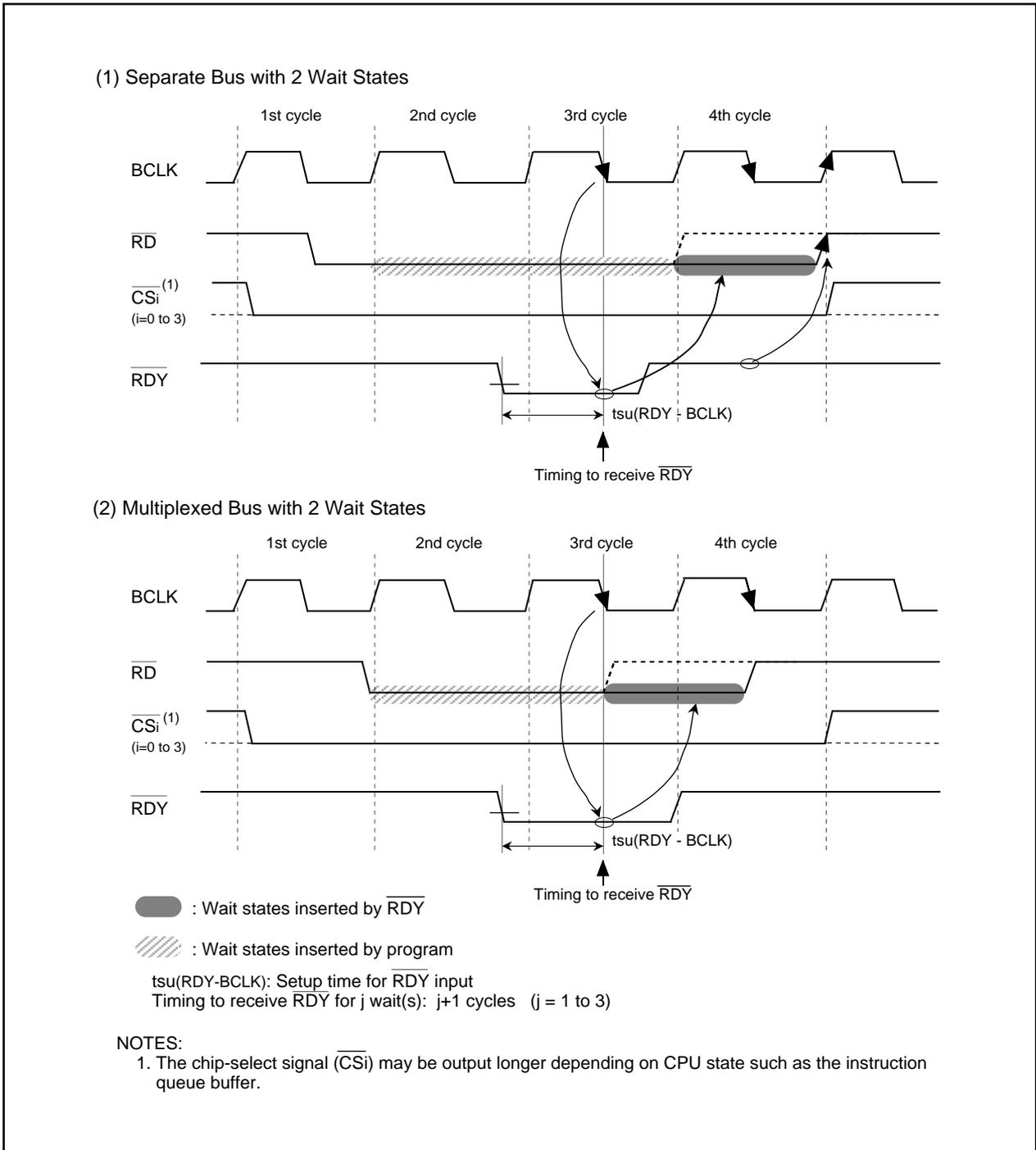


Figure 8.11 \overline{RD} Signal Output Extended by \overline{RDY} Signal

8.2.7 $\overline{\text{HOLD}}$ Signal

The $\overline{\text{HOLD}}$ signal transfers bus privileges from the CPU to external circuits. When a low-level ("L") signal is applied to the $\overline{\text{HOLD}}$ pin, the microcomputer enters a hold state after bus access is completed. While the $\overline{\text{HOLD}}$ pin is held "L", the microcomputer is in a hold state and the $\overline{\text{HLDA}}$ pin outputs an "L" signal.

Table 8.7 shows the microcomputer status in a hold state.

Bus is used in the following priority order: $\overline{\text{HOLD}}$, DMAC, CPU.



Figure 8.12 Bus Priority Order

Table 8.7 Microcomputer Status in Hold State

Item	Status
Oscillation	On
$\overline{\text{RD}}$ Signal, $\overline{\text{WR}}$ Signal, Address Bus, Data Bus, $\overline{\text{CS}}$, $\overline{\text{BHE}}$	High-impedance
Programmable I/O Ports: P0 to P15	Maintains the same state as when $\overline{\text{HOLD}}$ was received
$\overline{\text{HLDA}}$	Outputs "L"
Internal Peripheral Circuits	On (excluding the watchdog timer)
ALE Signal	Outputs "L"

8.2.8 External Bus Status when Accessing Internal Space

Table 8.8 shows external bus states when an internal space is accessed.

Table 8.8 External Bus States when Accessing Internal Space

Item	State when Accessing SFR, Internal ROM, and Internal RAM	
Address Bus	Holds address of external space last accessed	
Data Bus	When Read	High-impedance
	When Write	High-impedance
$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$	Outputs "H"	
$\overline{\text{BHE}}$	Holds state of external space last accessed	
$\overline{\text{CS}}$	Outputs "H"	
ALE	Outputs ALE	

8.2.9 BCLK Output

The CPU clock operates the CPU. P53 outputs the CPU clock signal as BCLK when the PM07 bit in the PM0 register is set to "0" (BCLK) and the CM01 and CM00 bits in the CM0 register are set to "002" (I/O port P53).

No BCLK is output in single-chip mode. Refer to **9. Clock Generation Circuit** for details.

8.3 Page Mode Control Function

NOTE

The page mode control function can be used in the ROMless version only.

The page mode control function allows the microcomputer to be read data in the external memory, associated with page mode, at high speeds. If the 21 high-order bits of consecutive addresses accessed by the microcomputer remains the same, access time to each address following the first access is shortened. The EWCRi (i=0 to 3) registers determine how many wait states are inserted to access the first address. The PWCR0 and PWCR1 registers determine how many wait states are inserted to access the consecutive addresses following the first address.

Use the following procedure to enable the page mode control.

- (1) Set the EWCRi04 to EWCRi00 (i=0 to 3) bits in the EWCRi register
- (2) Set the PWCRj02 to PWCRj00 (j=0, 1) bits and the PWCRj06 to PWCRj04 bits in the PWCRj register
- (3) Set the PWCRj03 and PWCRj07 bits in the PWCRj register to "1" (page mode control enabled)

When using the page mode control, access data in all external space only with the page mode control. It is not allowed to combine the page mode control access and normal access to data in each external space.

Set the PM05 and PM04 bits in the PM0 register to "002" (multiplexed bus not used). The page mode control function and multiplexed bus cannot be used at the same time.

Figure 8.13 shows the PWCR0 register. Figure 8.14 shows the PWCR1 register. Figure 8.15 shows an example of the external bus operation with the page mode control function.

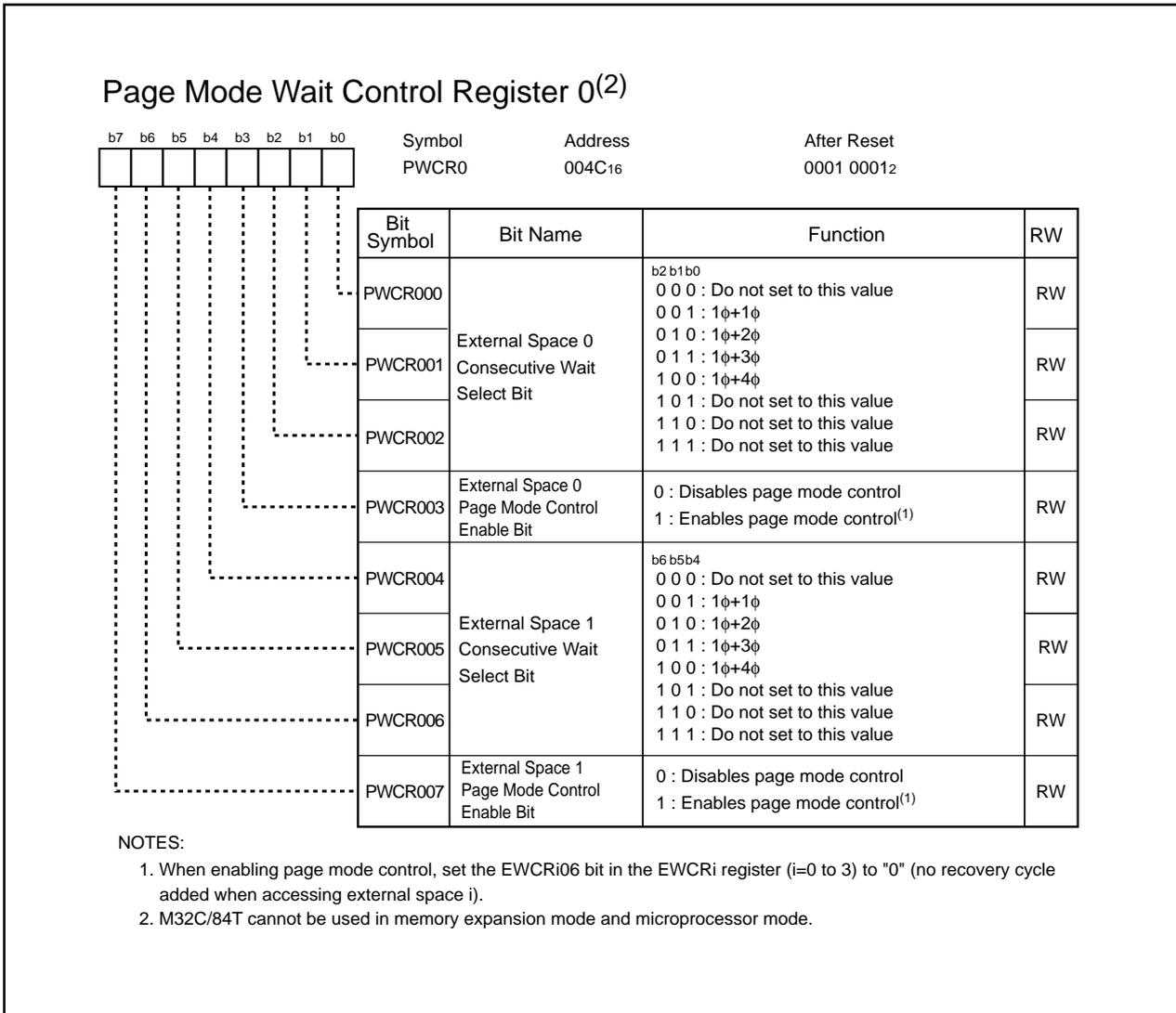


Figure 8.13 PWCR0 Register

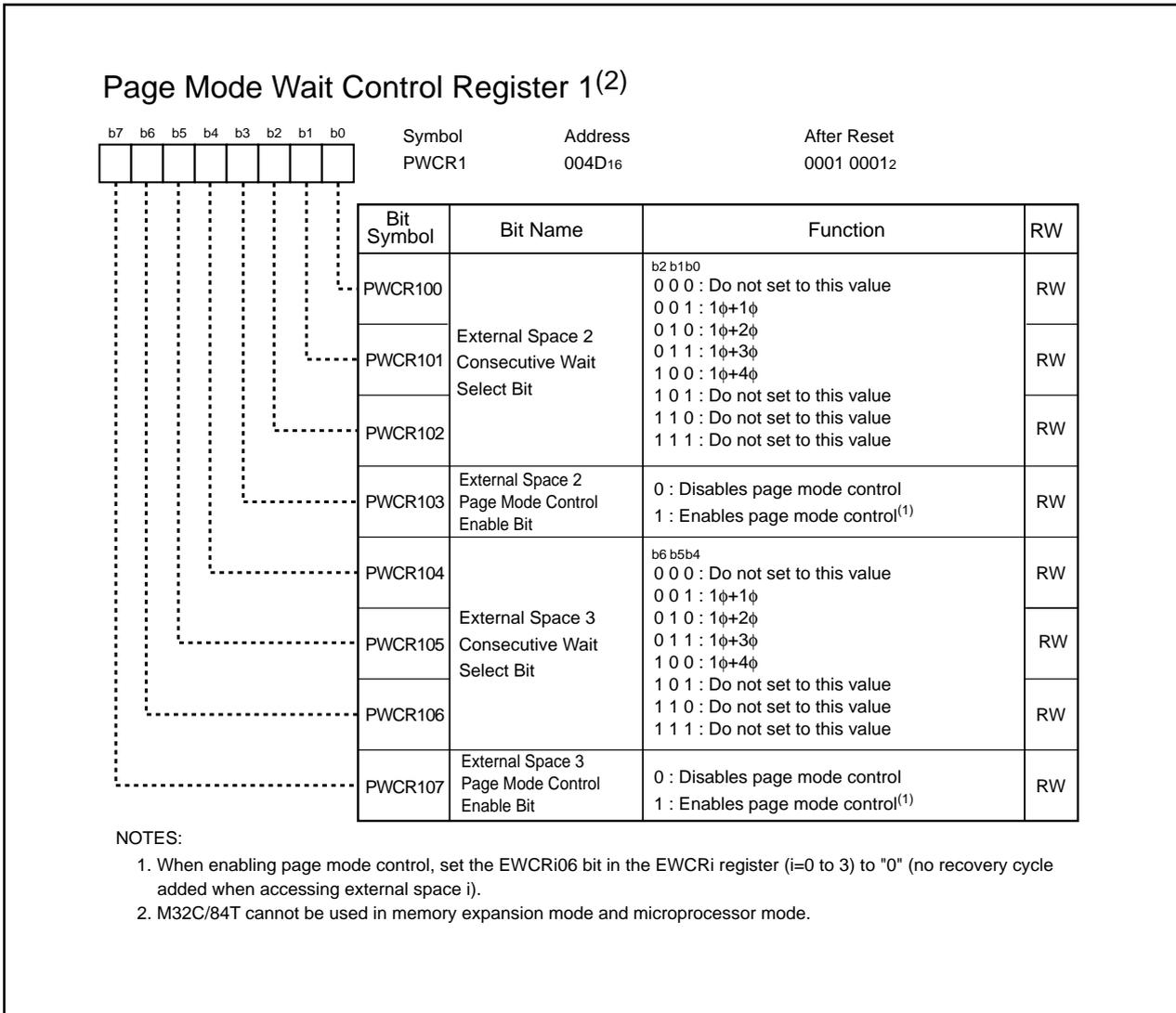


Figure 8.14 PWCR1 Register

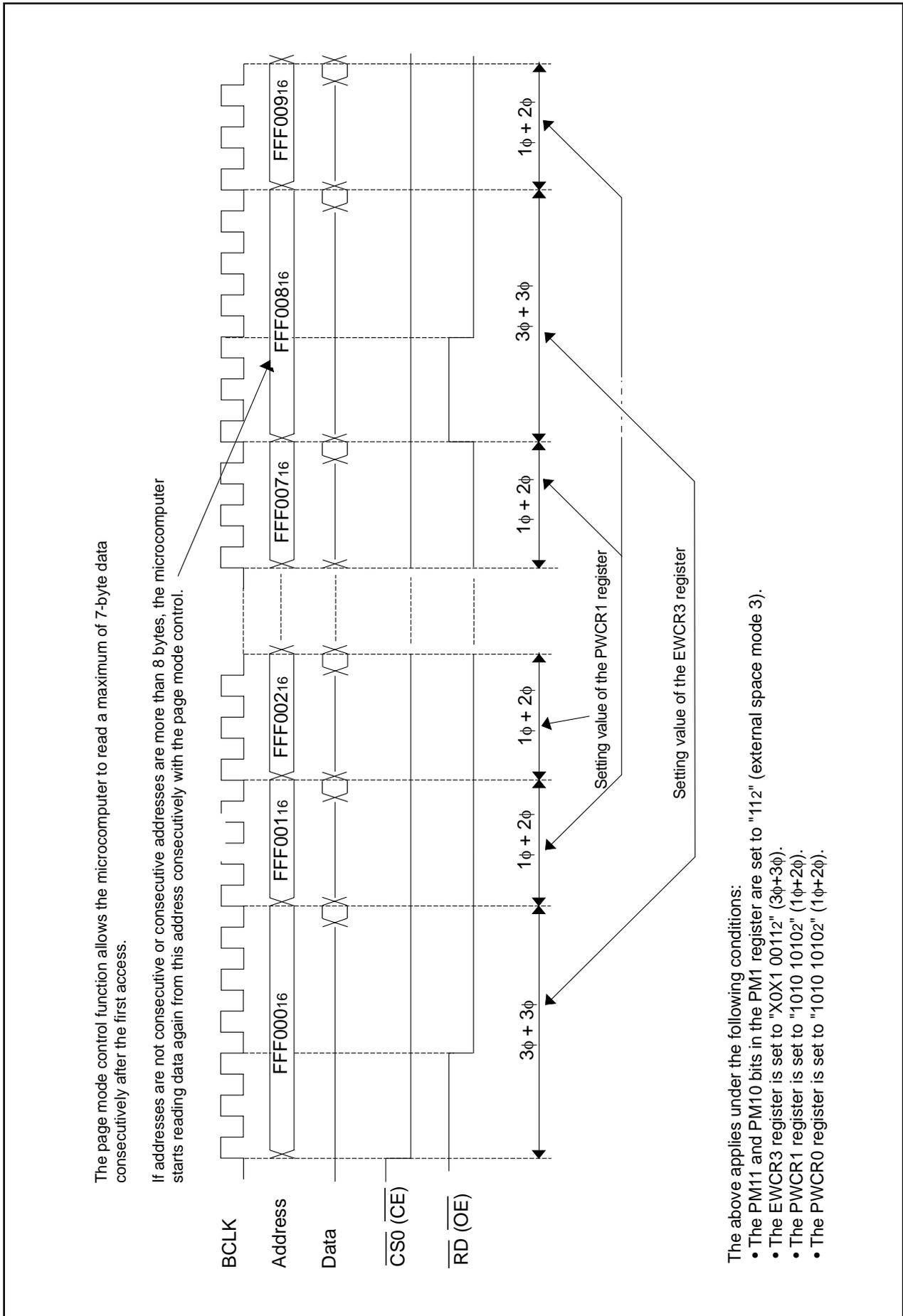


Figure 8.15 External Bus with Page Mode Control Function

9. Clock Generation Circuit

9.1 Types of the Clock Generation Circuit

Four circuits are included to generate the system clock signal:

- Main clock oscillation circuit
- Sub clock oscillation circuit
- On-chip oscillator
- PLL frequency synthesizer

Table 9.1 lists specifications of the clock generation circuit. Figure 9.1 shows a block diagram of the clock generation circuit. Figures 9.2 to 9.8 show registers controlling the clock.

Table 9.1 Clock Generation Circuit Specifications

Item	Main Clock Oscillation Circuit	Sub Clock Oscillation Circuit	On-chip Oscillator	PLL Frequency Synthesizer
Use	CPU clock source, Peripheral function clock source	CPU clock source, Timer A and B clock source	CPU clock source, Peripheral function clock source	CPU clock source, Peripheral function clock source
Clock Frequency	Up to 32 MHz	32.768 kHz	Approx. 1 MHz	Up to 32 MHz (See Table 9.3)
Connectable Oscillator or Additional Circuit	Ceramic resonator Crystal oscillator	Crystal oscillator	---	---
Pins for Oscillator or for Additional Circuit	XIN, XOUT	XCIN, XCOU	---	---
Oscillation Stop / Restart Function	Available	Available	Available	Available
Oscillator State after Reset	Oscillating	Stopped	Stopped	Stopped
Other	Externally generated clock can be applied.	Externally generated clock can be applied.	When the main clock stops oscillating, the on-chip oscillator starts oscillating automatically and becomes clock source for the CPU and peripheral function.	---

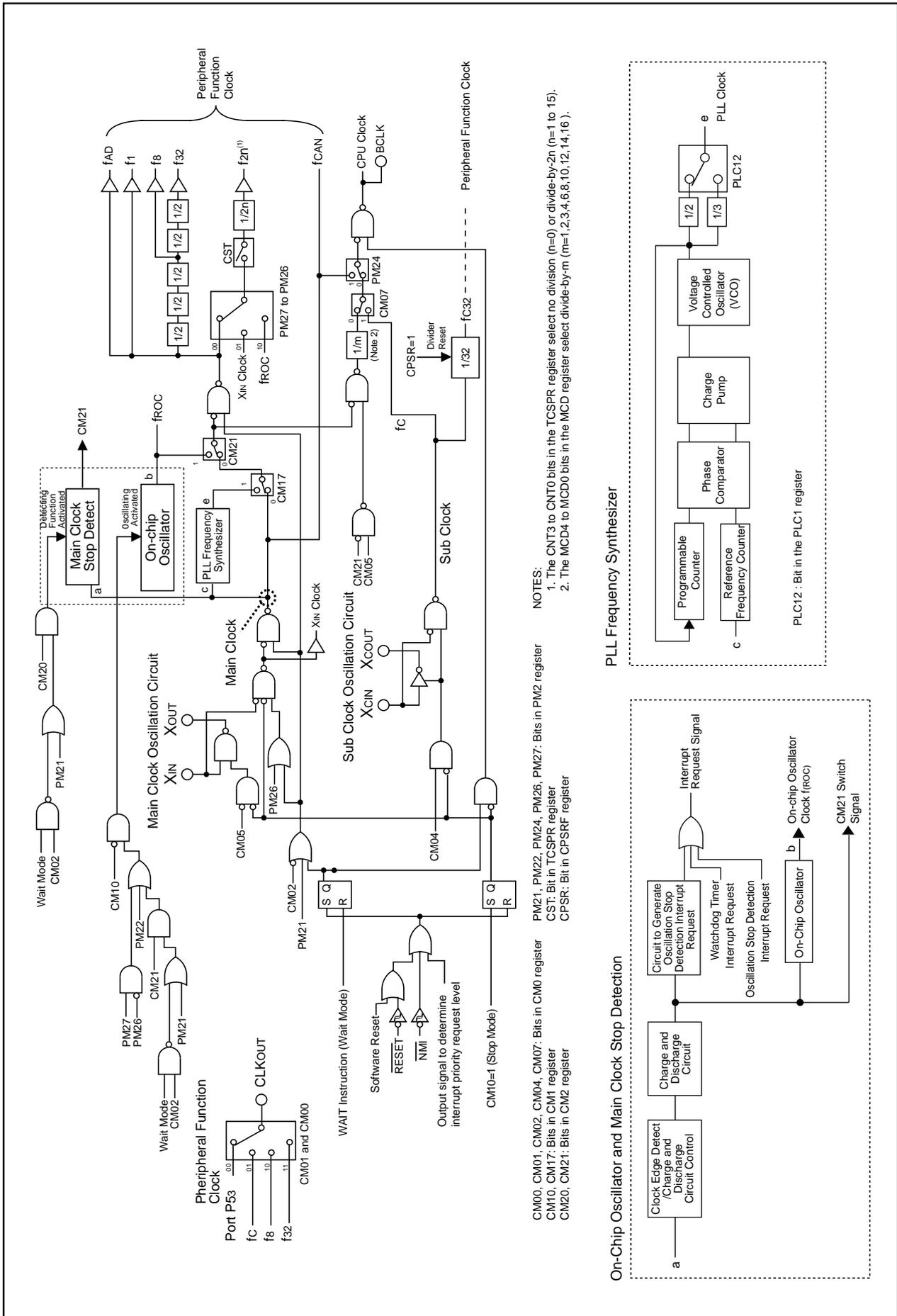


Figure 9.1 Clock Generation Circuit

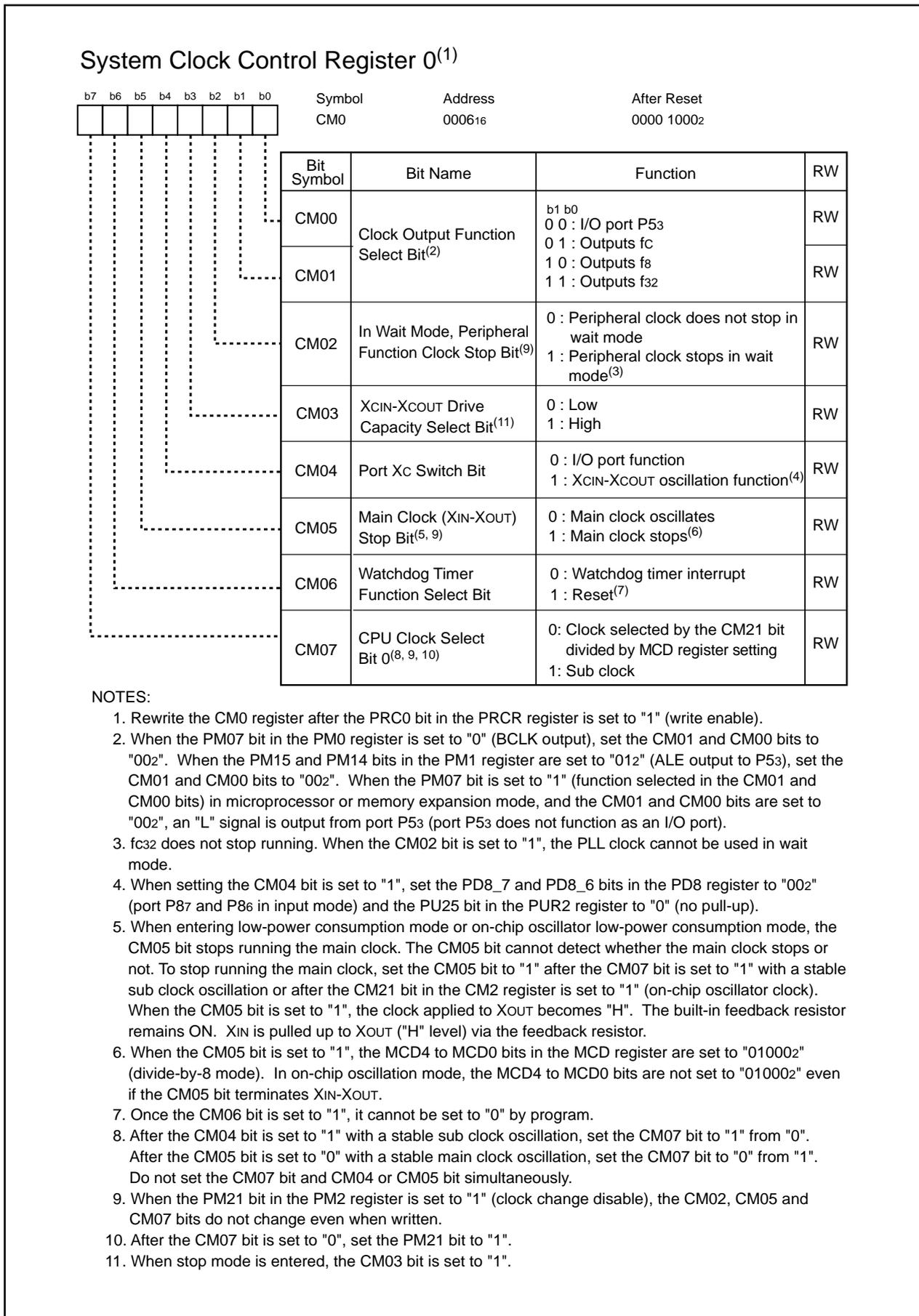


Figure 9.2 CM0 Register

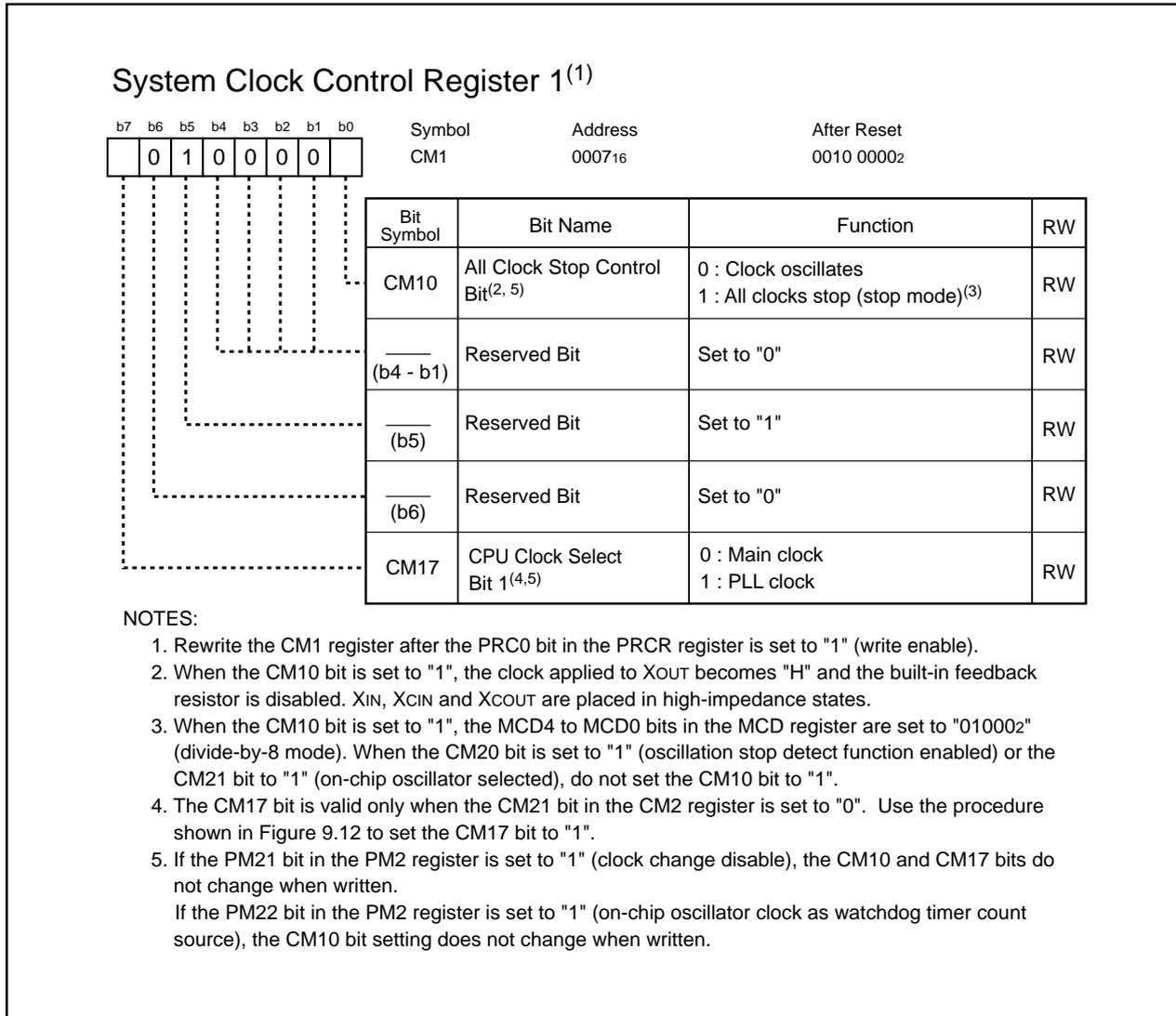


Figure 9.3 CM1 Register

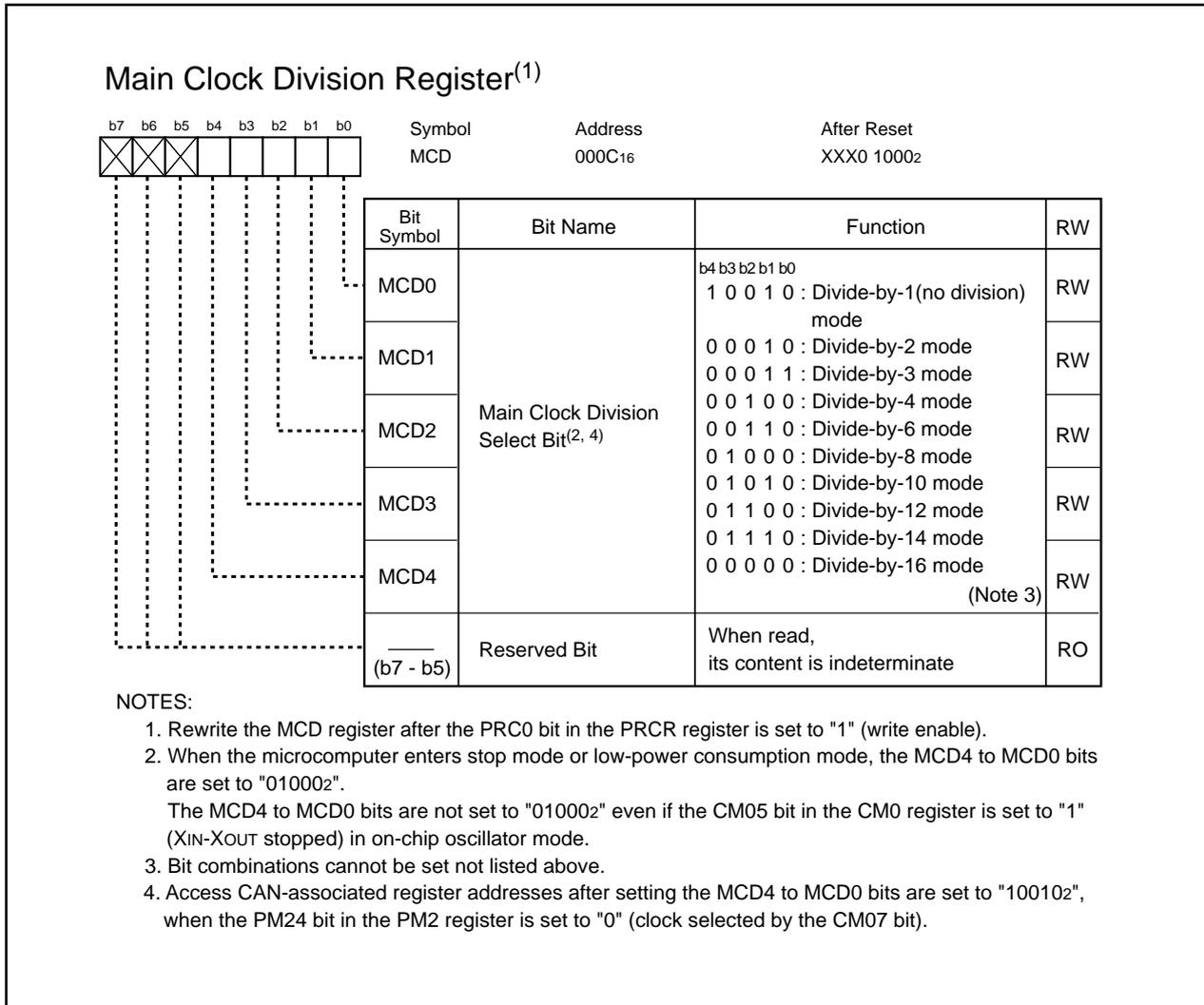


Figure 9.4 MCD Register

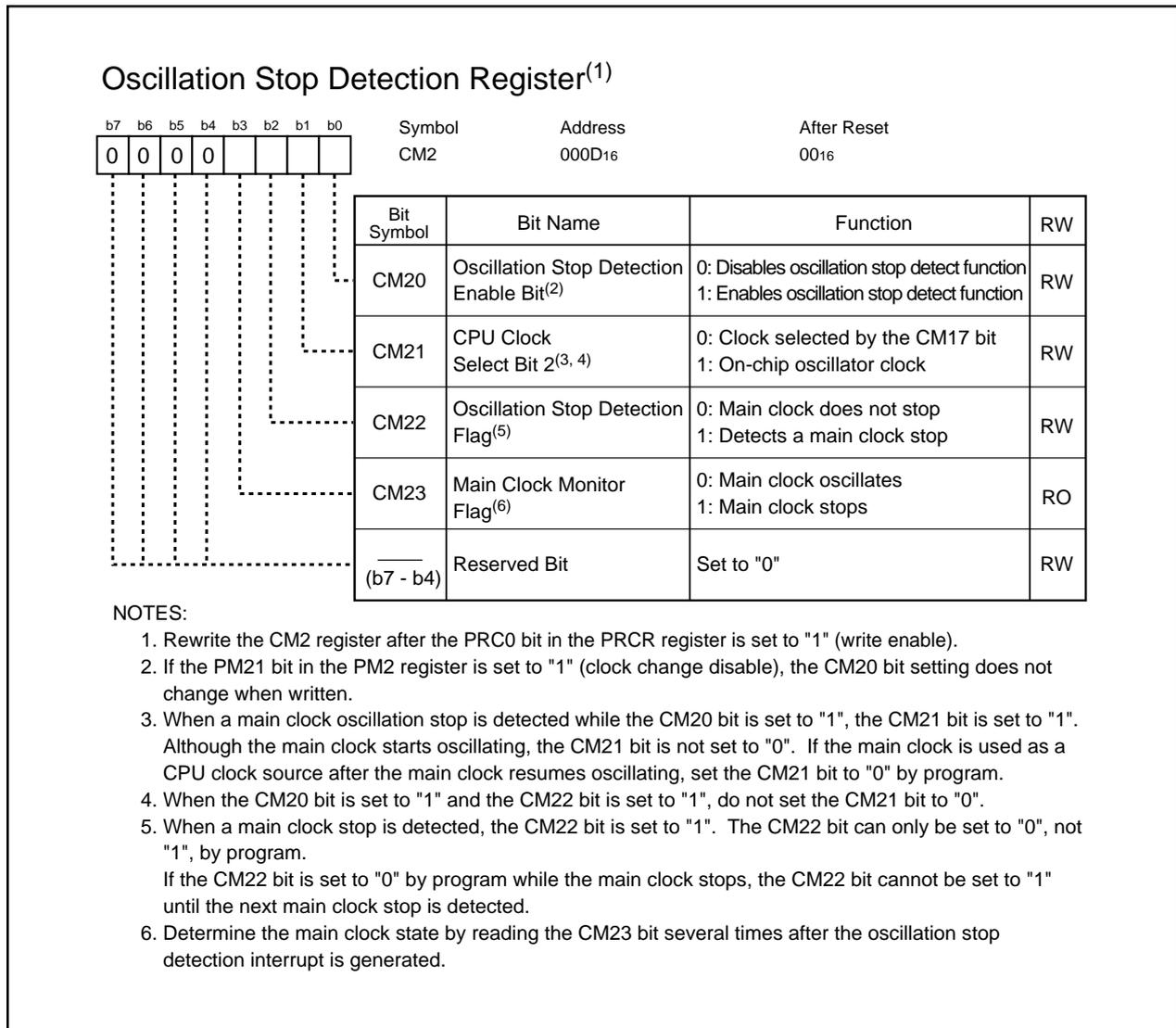


Figure 9.5 CM2 Register

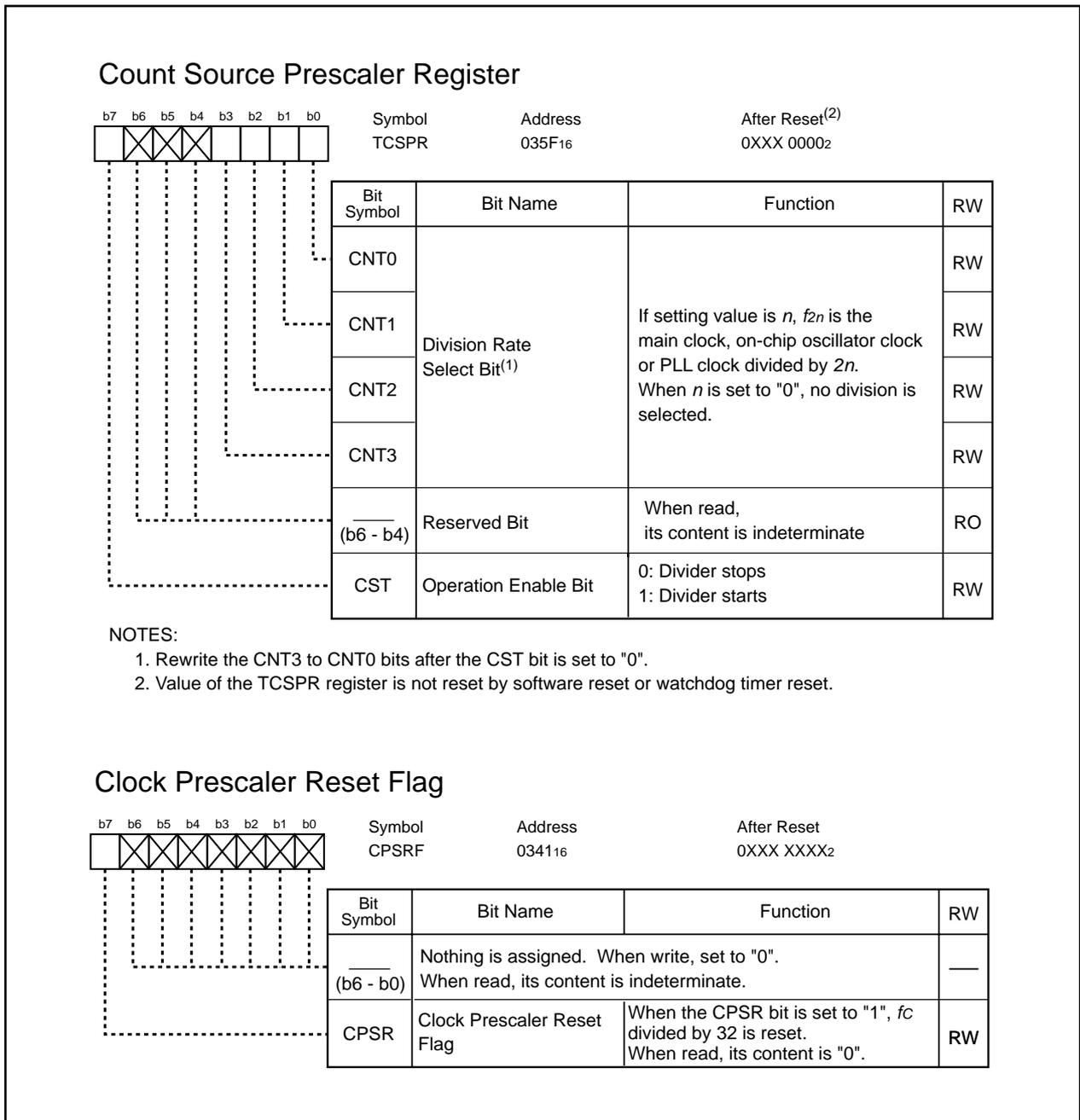


Figure 9.6 TCSR and CPSRF Registers

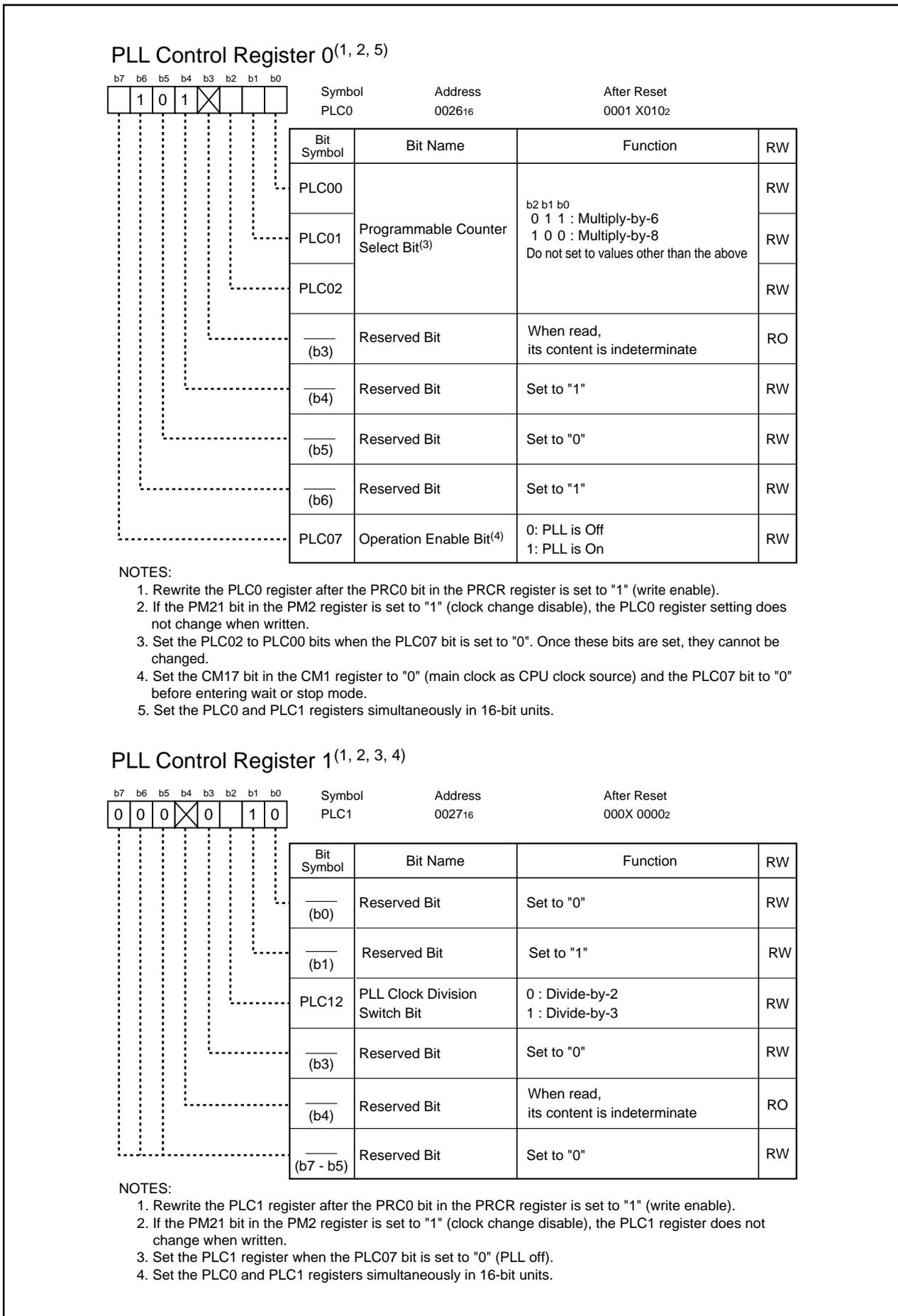
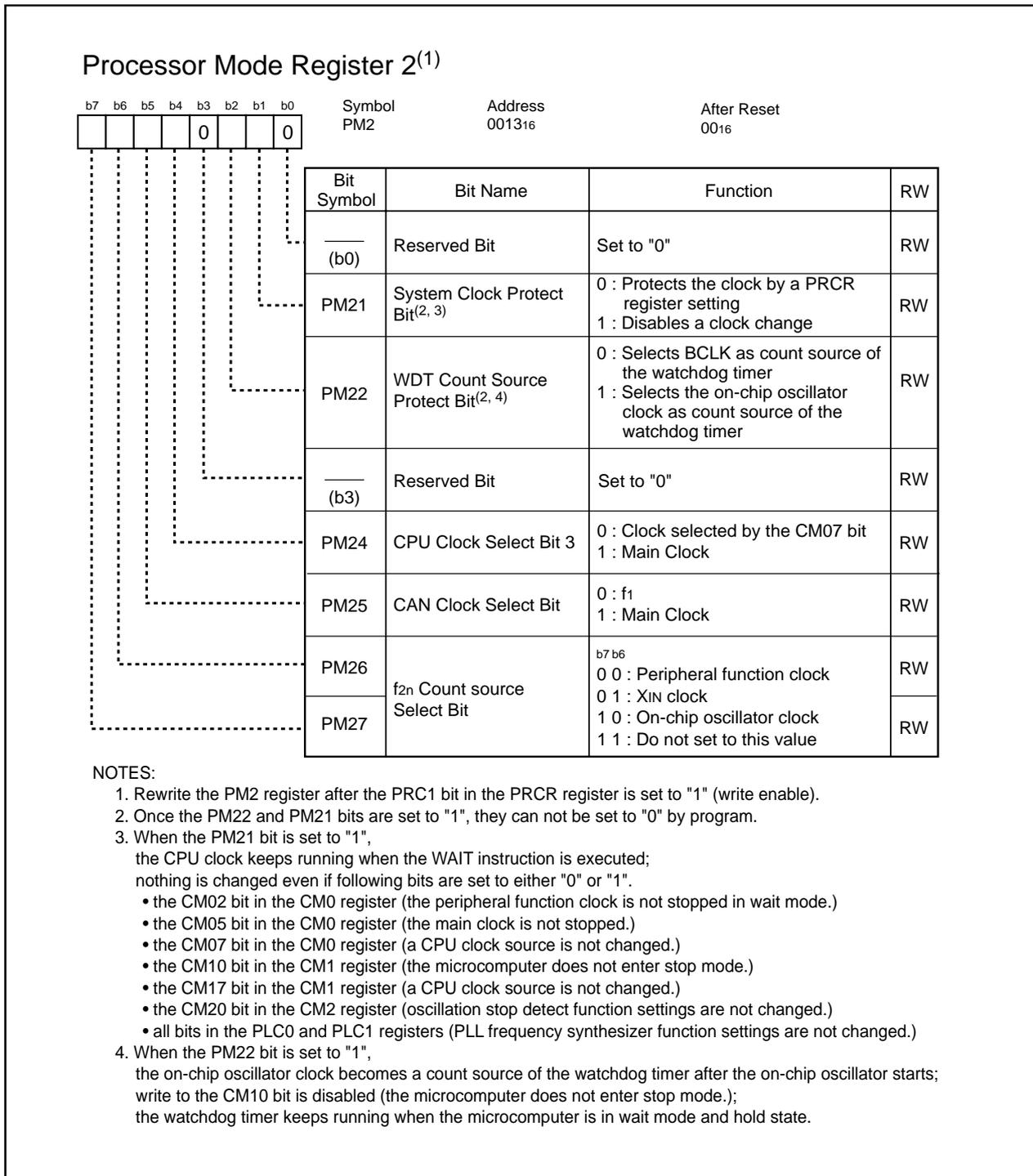


Figure 9.7 PLC0 and PLC1 Registers

**Figure 9.8 PM2 Register**

9.1.1 Main Clock

Main clock oscillation circuit generates the main clock. The main clock becomes clock source of the CPU clock and peripheral function clock.

The main clock oscillation circuit is configured by connecting an oscillator or resonator between the XIN and XOUT pins. The circuit has a built-in feedback resistor. The feedback resistor is separated from the oscillation circuit in stop mode to reduce power consumption. An external clock can be applied to the XIN pin in the main clock oscillation circuit. Figure 9.9 shows an example of a main clock circuit connection. Circuit constants vary depending on each oscillator. Use the circuit constant recommended by each oscillator manufacturer.

The main clock divided-by-eight becomes a CPU clock source after reset.

To reduce power consumption, set the CM05 bit in the CM0 register to "1" (main clock stopped) after switching the CPU clock source to the sub clock or on-chip oscillator clock. In this case, the clock applied to XOUT becomes high ("H"). XIN is pulled up by XOUT via the feedback resistor which remains on. When an external clock is applied to the XIN pin, do not set the CM05 bit to "1".

All clocks, including the main clock, stop in stop mode. Refer to **9.5 Power Consumption Control** for details.

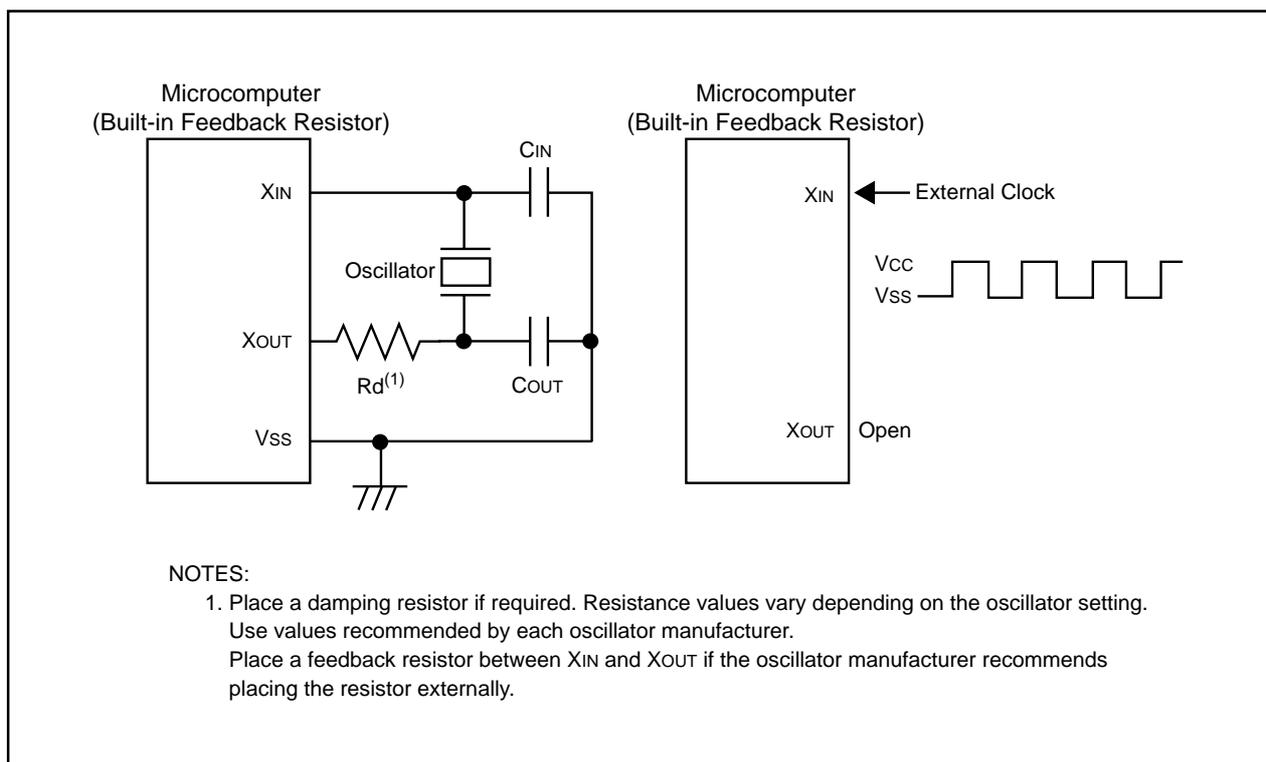


Figure 9.9 Main Clock Circuit Connection

9.1.2 Sub Clock

Sub clock oscillation circuit generates the sub clock. The sub clock becomes clock source of the CPU clock and for the timers A and B. The same frequency, f_c , as the sub clock can be output from the CLKOUT pin.

The sub clock oscillation circuit is configured by connecting a crystal oscillator between the XCIN and XCOUT pins. The circuit has a built-in feedback resistor. The feedback resistor is separated from the oscillation circuit in stop mode to reduce power consumption. An external clock can be applied to the XCIN pin. Figure 9.10 shows an example of a sub clock circuit connection. Circuit constants vary depending on each oscillator. Use the circuit constant recommended by each oscillator manufacturer.

The sub clock stops after reset. The feedback resistor is separated from the oscillation circuit. When the PD8_6 and PD8_7 bits in the PD8 register are set to "0" (input mode) and the PU25 bit in the PUR2 register is set to "0" (no pull-up), set the CM04 bit in the CM0 register to "1" (XCIN-XCOUT oscillation function). The sub clock oscillation circuit starts oscillating. To apply an external clock to the XCIN pin, set the CM04 bit to "1" when the PD8_7 bit is set to "0" and the PU25 bit to "0". The clock applied to the XCIN pin becomes a clock source of the sub clock.

When the CM07 bit in the CM0 register is set to "1" (sub clock) after the sub clock oscillation has stabilized, the sub clock becomes a CPU clock source.

All clocks, including the sub clock, stop in stop mode. Refer to **9.5 Power Consumption Control** for details.

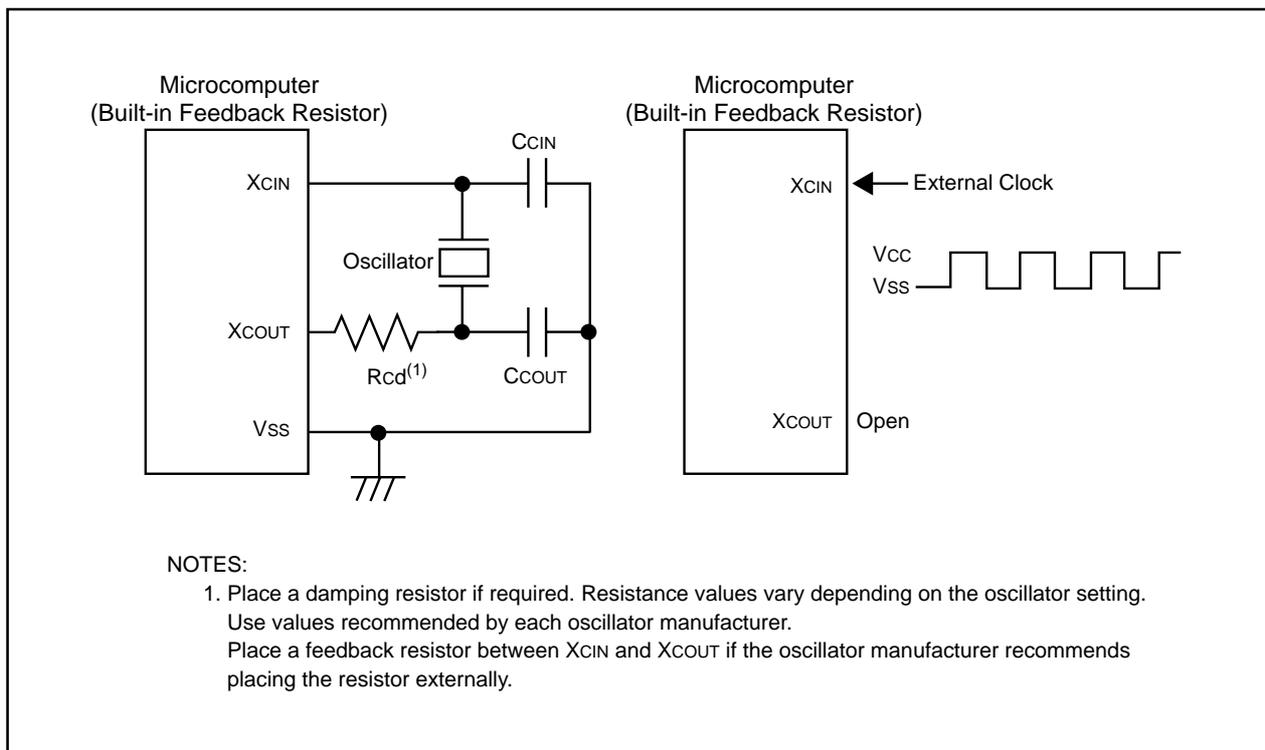


Figure 9.10 Sub Clock Circuit Connection

9.1.3 On-Chip Oscillator Clock

On-chip oscillator generates the on-chip oscillator clock. The 1-MHz on-chip oscillator clock becomes a clock source of the CPU clock and peripheral function clock.

The on-chip oscillator clock stops after reset. When the CM21 bit in the CM2 register is set to "1" (on-chip oscillator clock), the on-chip oscillator starts oscillating. Instead of the main clock, the on-chip oscillator clock becomes clock source of the CPU clock and peripheral function clock.

Table 9.2 shows bit settings for on-chip oscillator start condition.

Table 9.2 Bit Settings for On-Chip Oscillator Start Condition

CM2 Register	PM2 Register		Used as
CM21 Bit	PM22 Bit	PM27 and PM26 Bits	
1	0	0 0	CPU clock source or peripheral function clock source
0	1	0 0	Watchdog timer operating clock source (The clock keeps running when entering stop mode.)
0	0	0 1	f _{2n} count source

9.1.3.1 Oscillation Stop Detect Function

When the main clock is terminated by external source, the on-chip oscillator automatically starts oscillating to generate another clock.

When the CM 20 bit in the CM2 register is set to "1" (oscillation stop detect function enabled), an oscillation stop detection interrupt request is generated as soon as the main clock stops. Simultaneously, the on-chip oscillator starts oscillating. Instead of the main clock, the on-chip oscillator clock becomes clock source for the CPU clock and peripheral function clock. Associated bits are set as follows:

- The CM21 bit is set to "1" (on-chip oscillator clock becomes a clock source of the CPU clock.)
- The CM22 bit is set to "1" (main clock stop is detected.)
- The CM23 bit is set to "1" (main clock stops.) (See **Figure 9.14**)

9.1.3.2 How to Use Oscillation Stop Detect Function

- The oscillation stop detection interrupt shares vectors with the watchdog timer interrupt and the low voltage detection interrupt. When these interrupts are used simultaneously, read the CM22 bit with an interrupt routine to determine if an oscillation stop detection interrupt request has been generated.
- When the main clock resumes running after an oscillation stop is detected, set the main clock as clock source of the CPU clock and peripheral function clock. Figure 9.11 shows the procedure to switch the on-chip oscillator clock to the main clock.
- In low-speed mode, when the main clock is stopped by setting the CM20 bit to "1", the oscillation stop detection interrupt request is generated. Simultaneously, the on-chip oscillator starts oscillating. The sub clock remains the CPU clock source. The on-chip oscillator clock becomes a clock source for the peripheral function clock.
- When the peripheral function clock stops running, the oscillation stop detect function is also disabled. To enter wait mode while the oscillation stop detect function is in use, set the CM02 bit in the CM0 register to "0" (peripheral clock does not stop in wait mode).
- The oscillation stop detect function is provided to handle main clock stop caused by external source. Set the CM20 bit to "0" (oscillation stop detect function disabled) when the main clock is terminated by program, i.e., entering stop mode or setting the CM05 bit to "1" (main clock oscillation stop).
- When the main clock frequency is 2MHz or less, the oscillation stop detect function is not available. Set the CM20 bit to "0".

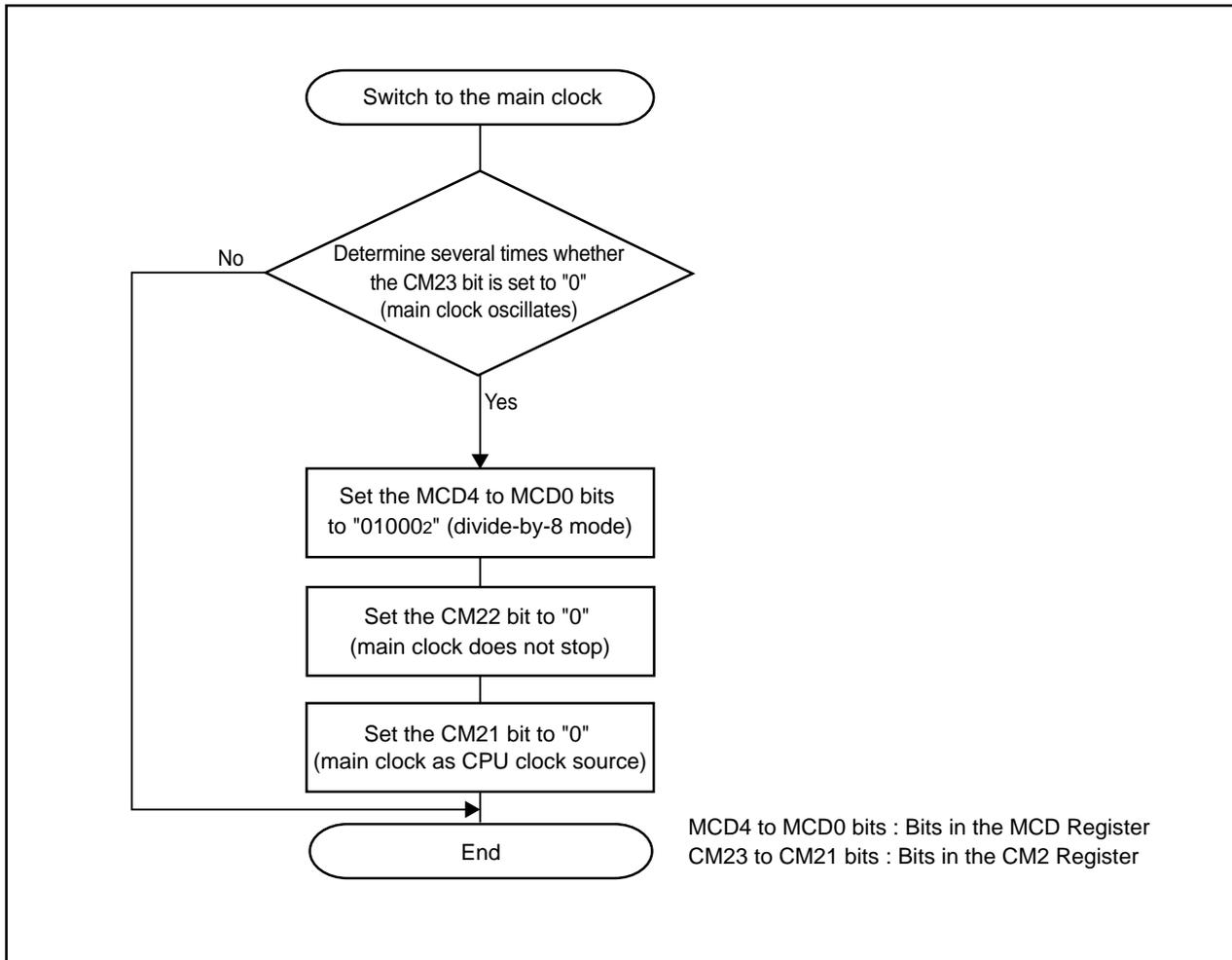


Figure 9.11 Switching Procedure from On-chip Oscillator Clock to Main Clock

9.1.4 PLL Clock

The PLL frequency synthesizer generates the PLL clock based on the main clock. The PLL clock can be used as clock source for the CPU clock and peripheral function clock.

The PLL frequency synthesizer stops after reset. When the PLC07 bit is set to "1" (PLL on), the PLL frequency synthesizer starts operating. Wait $t_{su(PLL)}$ ms for the PLL clock to stabilize.

The PLL clock can either be the clock output from the voltage controlled oscillator (VCO) divided-by-2 or divided-by-3. When the PLL clock is used as a clock source for the CPU clock or peripheral function clock, set each bit as is shown in Table 9.3. Figure 9.12 shows the procedure to use the PLL clock as the CPU clock source.

To enter wait or stop mode, set the CM17 bit to "0" (main clock as CPU clock source), set the PLC07 bit in the PLC0 register to "0" (PLL off) and then enter wait or stop mode.

Table 9.3 Bit Settings to Use PLL Clock as CPU Clock Source

f(XIN)	PLC0 Register			PLC1 Register	PLL Clock
	PLC02 Bit	PLC01 Bit	PLC00 Bit	CM21 Bit	
10 MHz	0	1	1	0	30 MHz
				1	20 MHz
8 MHz	1	0	0	0	32 MHz
				1	21.3 MHz

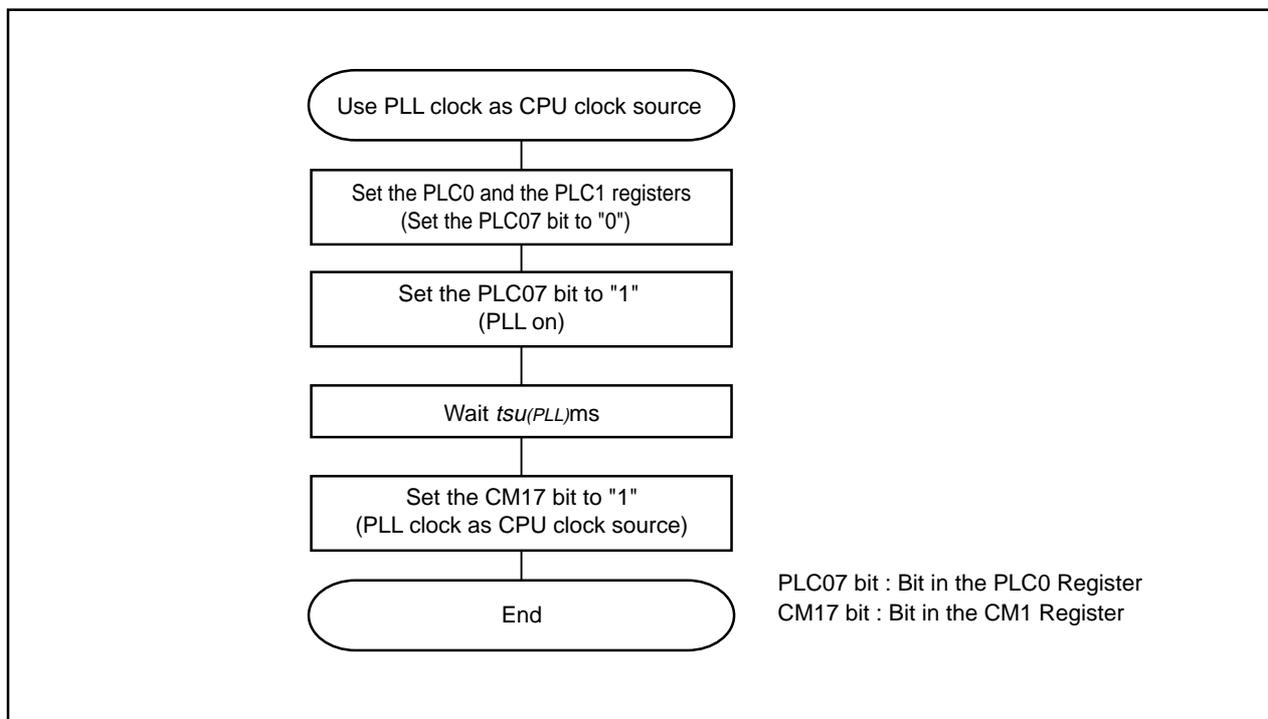


Figure 9.12 Procedure to Use PLL Clock as CPU Clock Source

9.2 CPU Clock and BCLK

The CPU operating clock is referred to as the CPU clock. The CPU clock is also a count source for the watchdog timer. After reset, the CPU clock is the main clock divided-by-8. In memory expansion or micro-processor mode, the clock having the same frequency as the CPU clock can be output from the BCLK pin as BCLK. Refer to **9.4 Clock Output Function** for details.

The main clock, sub clock, on-chip oscillator clock or PLL clock can be selected as a clock source for the CPU clock. Table 9.4 shows CPU clock source and bit settings.

When the main clock, on-chip oscillator clock or PLL clock is selected as a clock source of the CPU clock, the selected clock divided-by-1 (no division), -2, -3, -4, -6, -8, -10, -12, -14 or -16 becomes the CPU clock. The MCD4 to MCD0 bits in the MCD register select the clock division.

When the microcomputer enters stop mode or low-power consumption mode (except when the on-chip oscillator clock is the CPU clock), the MCD4 to MCD0 bits are set to "010002" (divide-by-8 mode). Therefore, when the main clock starts running, the CPU clock enters medium-speed mode (divide-by-8).

Table 9.4 CPU Clock Source and Bit Settings

CPU Clock Source	CM0 Register	CM1 Register	CM2 Register	PM2 Register
	CM07 Bit	CM17 Bit	CM21 Bit	PM24 Bit
Main Clock	0	0	0	0
Main Clock (Main Clock Direct Mode) ⁽¹⁾	0	0	0	1
Sub Clock	1	0	0	0
On-Chip Oscillator Clock	0	0	1	0
PLL Clock	0	1	0	0

NOTES:

1. Refer to **23.2 CAN Clock** for details.

9.3 Peripheral Function Clock

The peripheral function clock becomes an operating clock or count source for peripheral functions excluding the watchdog timer.

9.3.1 f1, f8, f32 and f2n

f1, f8 and f32 are the peripheral function clock, selected by the CM21 bit, divided-by-1, -8, or -32. The PM27 and PM26 bits in the PM2 register selects a f2n count source from the peripheral clock, XIN clock, and the on-chip oscillator clock. The CNT3 to CNT0 bits in the TCSPR register selects a f2n division. (n=1 to 15. No division when n=0.)

f1, f8, f32 and f2n stop when the CM02 bit in the CM0 register to "1" (peripheral function stops in wait mode) to enter wait mode or when in low-power consumption mode.

f1, f8 and f2n are used as an operating clock of the serial I/O and count source of the timers A and B. f1 is also used as an operating clock for the intelligent I/O.

The CLKOUT pin outputs f8 and f32. Refer to **9.4 Clock Output Function** for details.

9.3.2 fAD

fAD is an operating clock for the A/D converter and has the same frequency as either the main clock⁽¹⁾ or the on-chip oscillator clock. The CM21 bit determines which clock is selected.

If the CM02 bit is set to "1" (peripheral function stop in wait mode) to enter wait mode, fAD stops. fAD also stops in low-power consumption mode.

NOTES:

1. The PLL clock, instead of the main clock, when the CM17 bit is set to "1" (PLL clock).

9.3.3 fc32

fc32 is the sub clock divided by 32. fc32 is used as a count source for the timers A and B. fc32 is available when the sub clock is running.

9.3.4 fCAN

fCAN has the same frequency as the main clock. It is a clock for the CAN module only.

9.4 Clock Output Function

The CLKOUT pin outputs fc, f8 or f32.

In memory expansion mode or microprocessor mode, a clock having the same frequency as the CPU clock can be output from the BCLK pin as BCLK.

Table 9.5 lists CLKOUT pin function in single-chip mode. Table 9.6 lists CLKOUT pin function in memory expansion mode and microprocessor mode.

Table 9.5 CLKOUT Pin in Single-Chip Mode

PM0 Register ⁽¹⁾		CM0 Register ⁽²⁾		CLKOUT Pin Function
PM07 Bit		CM01 Bit	CM00 Bit	
—		0	0	P53 I/O port
1		0	1	Outputs fc
1		1	0	Outputs f8
1		1	1	Outputs f32

- : Can be set to either "0" or "1"

NOTES:

1. Rewrite the PM0 register after the PRC1 bit in the PRCR register is set to "1" (write enable).
2. Rewrite the CM0 register after the PRC0 bit in the PRCR register is set to "1" (write enable).

Table 9.6 CLKOUT Pin in Memory Expansion Mode and Microprocessor Mode

PM1 Register ⁽¹⁾		PM0 Register ⁽¹⁾		CM0 Register ⁽²⁾		CLKOUT Pin Function
PM15 Bit	PM14 Bit	PM07 Bit		CM01 Bit	CM00 Bit	
002, 102, 112,		0		0 ⁽³⁾	0 ⁽³⁾	Outputs BCLK
		1		0	0	Outputs "L" (not P53)
		1		0	1	Outputs fc
		1		1	0	Outputs f8
		1		1	1	Outputs f32
0	1	—		0 ⁽³⁾	0 ⁽³⁾	Outputs ALE

- : Can be set to either "0" or "1"

NOTES:

1. Rewrite the PM1 and PM0 registers after the PRC1 bit in the PRCR register is set to "1" (write enable).
2. Rewrite the CM0 register after the PRC0 bit in the PRCR register is set to "1" (write enable).
3. When the PM07 bit is set to "0" (selected in the CM01 and CM00 bits) or the PM15 and PM14 bits are set to "012" (P53/BCLK), set the CM01 and CM00 bits to "002" (I/O port P53).
4. M32C/84T cannot be used in memory expansion mode and microprocessor mode.

9.5 Power Consumption Control

Normal operating mode, wait mode and stop mode are provided as the power consumption control.

All mode states, except wait mode and stop mode, are called normal operating mode in this section. Figure 9.13 shows a block diagram of status transition in wait mode and stop mode. Figure 9.14 shows a block diagram of status transition in all modes.

9.5.1 Normal Operating Mode

The normal operating mode is further separated into six modes.

In normal operating mode, the CPU clock and peripheral function clock are supplied to operate the CPU and peripheral function. The power consumption control is enabled by controlling a CPU clock frequency. The higher the CPU clock frequency is, the more processing power increases. The lower the CPU clock frequency is, the more power consumption decreases. When unnecessary oscillation circuit stops, power consumption is further reduced.

9.5.1.1 High-Speed Mode

The main clock⁽¹⁾ becomes the CPU clock and a clock source of the peripheral function clock. When the sub clock runs, fc32 can be used as a count source for the timers A and B.

9.5.1.2 Medium-Speed Mode

The main clock⁽¹⁾ divided-by-2, -3, -4, -6, -8, -10, -12, -14, or -16 becomes the CPU clock. The main clock⁽¹⁾ is a clock source for the peripheral function clock. When the sub clock runs, fc32 can be used as a count source for the timers A and B.

9.5.1.3 Low-Speed Mode

The sub clock becomes the CPU clock. The main clock⁽¹⁾ is a clock source for the peripheral function clock. fc32 can be used as a count source for the timers A and B.

9.5.1.4 Low-Power Consumption Mode

The microcomputer enters low-power consumption mode when the main clock stops in low-speed mode. The sub clock becomes the CPU clock. Only fc32 can be used as a count source for the timers A and B and the peripheral function clock. In low-power consumption mode, the MCD4 to MCD0 bits in the MCD register are set to "010002" (divide-by-8 mode). Therefore, when the main clock resumes running, the microcomputer is in medium-speed mode (divide-by-8 mode).

9.5.1.5 On-Chip Oscillator Mode

The on-chip oscillator clock divided-by-1 (no division), -2, -3, -4, -6, -8, -10, -12, -14, or -16 becomes the CPU clock. The on-chip oscillator clock is a clock source for the peripheral function clock. When the sub clock runs, fc32 can be used as a count source for the timers A and B.

9.5.1.6 On-Chip Oscillator Low-Power Consumption Mode

The microcomputer enters on-chip oscillator low-power consumption mode when the main clock stops in on-chip oscillator mode. The on-chip oscillator clock divided-by-1 (no division), -2, -3, -4, -6, -8, -10, -12, -14, or -16 becomes the CPU clock. The on-chip oscillator clock is a clock source for the peripheral function clock. When the sub clock runs, fc32 can be used as a count source for the timers A and B.

NOTES:

1. The PLL clock, instead of the main clock, when the CM17 bit is set to "1" (PLL clock).

Switch the CPU clock after the clock to be switched to stabilize. Sub clock oscillation will take longer⁽²⁾ to stabilize. Wait, by program, until the clock stabilizes directly after turning the microcomputer on or exiting stop mode.

To switch the on-chip oscillator clock to the main clock, enter medium-speed mode (divide-by-8) after the main clock is divided by eight in on-chip oscillator mode (the MCD4 to MCD0 bits in the MCD register are set to "010002").

Do not enter on-chip oscillator mode or on-chip oscillator low-power consumption mode from low-speed mode or low-power consumption mode and vice versa.

NOTES:

2. Contact your oscillator manufacturer for oscillation stabilization time.

9.5.2 Wait Mode

In wait mode, the CPU clock stops running. The CPU and watchdog timer, operated by the CPU clock, also stop. When the PM22 bit in the PM2 register is set to "1" (on-chip oscillator clock as watchdog timer count source), the watchdog timer continues operating. Because the main clock, sub clock and on-chip oscillator clock continue running, peripheral functions using these clocks also continue operating.

9.5.2.1 Peripheral Function Clock Stop Function

If the CM02 bit in the CM0 register is set to "1" (peripheral function clock stops in wait mode), f1, f8, f32, f2n (when peripheral clock is selected as a count source), and fAD stop in wait mode. Power consumption can be reduced. f2n, when XIN clock or on-chip oscillator clock is selected as a count source, and fc32 do not stop running.

9.5.2.2 Entering Wait Mode

If wait mode is entered after setting the CM02 bit to "1", set the MCD4 to MCD0 bits in the MCD register to be the 10-MHz or less CPU clock frequency after dividing the main clock.

Enter wait mode after setting the followings.

- Initial Setting

Set each interrupt priority level after setting the exit priority level, required to exit wait mode and controlled by the RLVL2 to RLVL0 bits in the RLVL register, to "7".

- Before Entering Wait Mode

- (1) Set the I flag to "0"
- (2) Set the interrupt priority level of the interrupt being used to exit wait mode
- (3) Set the interrupt priority levels of the interrupts, not being used to exit wait mode, to "0"
- (4) Set IPL in the FLG register. Then set the exit priority level to the same level as IPL
Interrupt priority level of the interrupt used to exit wait mode > IPL = the exit priority level
- (5) Set the PRC0 bit in the PRCR register to "1"
- (6) If the CPU clock source is the PLL clock, set the CM17 bit in the CM1 register to "0" (main clock) and PLC07 bit in the PLC0 register to "0" (PLL off)
- (7) Set the I flag to "1"
- (8) Execute the WAIT instruction

- After Exiting Wait Mode

Set the exit priority level to "7" as soon as exiting wait mode.

9.5.2.3 Pin Status in Wait Mode

Table 9.7 lists pin states in wait mode.

Table 9.7 Pin States in Wait Mode

Pin		Memory Expansion Mode ⁽¹⁾ Microprocessor Mode ⁽¹⁾	Single-Chip Mode
Address Bus, Data Bus, $\overline{CS0}$ to $\overline{CS3}$, BHE		Maintains state immediately before entering wait mode	/
RD, WR, \overline{WRL} , \overline{WRH}		"H"	
HLDA, BCLK		"H"	
ALE		"L"	
Ports		Maintains state immediately before entering wait mode	
CLKOUT	When fc is selected	Outputs clock	
	When f8, f32 are selected	Outputs the clock when the CM02 bit in the CM0 register is set to "0" (peripheral function clock does not stop in wait mode). Maintains state immediately before entering wait mode when the CM02 bit is set to "1" (peripheral function clock stops in wait mode).	

NOTES:

1. M32C/84T cannot be used in memory expansion mode and microprocessor mode.

9.5.2.4 Exiting Wait Mode

Wait mode is exited by the hardware reset, \overline{NMI} interrupt or peripheral function interrupts.

When the hardware reset or \overline{NMI} interrupt, but not the peripheral function interrupts, is used to exit wait mode, set the ILVL2 to ILVL0 bits for the peripheral function interrupts to "0002" (interrupt disabled) before executing the WAIT instruction.

CM02 bit setting affects the peripheral function interrupts. When the CM02 bit in the CM0 register is set to "0" (peripheral function clock does not stop in wait mode), all peripheral function interrupts can be used to exit wait mode. When the CM02 bit is set to "1" (peripheral function clock stops in wait mode), peripheral functions using the peripheral function clock stop. Therefore, the peripheral function interrupts cannot be used to exit wait mode. However, the peripheral function interrupts caused by an external clock, fc32, or f2n whose count source is the XIN clock or on-chip oscillator clock, can be used to exit wait mode.

The CPU clock used when exiting wait mode by the peripheral function interrupts or \overline{NMI} interrupt is the same CPU clock used when the WAIT instruction is executed.

Table 9.8 shows interrupts to be used to exit wait mode and usage conditions.

Table 9.8 Interrupts to Exit Wait Mode

Interrupt	When CM02=0	When CM02=1
NMI Interrupt	Available	Available
Serial I/O Interrupt	Available when the internal and external clocks are used	Available when the external clock or f _{2n} (when X _{IN} clock or on-chip oscillator is selected) is used
Key Input Interrupt	Available	Available
A/D Conversion Interrupt	Available in single or single-sweep mode	Do not use
Timer A Interrupt Timer B Interrupt	Available in all modes	Available in event counter mode or when count source is fc32 or f _{2n} (when X _{IN} clock or on-chip oscillator is selected)
INT Interrupt	Available	Available
Low Voltage Detection Interrupt	Available	Available
CAN Interrupt	Available	Do not use
Intelligent I/O Interrupt	Available	Do not use

9.5.3 Stop Mode

In stop mode, all oscillators and resonators stop. The CPU clock and peripheral function clock, as well as the CPU and peripheral functions operated by these clocks, also stop. The least power required to operate the microcomputer is in stop mode. The internal RAM holds its data when the voltage applied to the VCC1 and VCC2 pins is V_{RAM} or more. If the voltage applied to the VCC1 and VCC2 pins is 2.7V or less, the voltage must be $V_{cc1} \geq V_{cc2} \geq V_{RAM}^{(1)}$.

The following interrupts can be used to exit stop mode:

- \overline{NMI} interrupt
- Key Input Interrupt
- \overline{INT} interrupt
- Timer A and B interrupt (Available when the timer counts external pulse, having its 100Hz or less frequency, in event counter mode)
- Low voltage detection interrupt (Refer to **6.1 Low Voltage Detection Interrupt** for usage conditions)

NOTES:

1. The supply voltage of M32C/84T must be $V_{cc1}=V_{cc2}$.

9.5.3.1 Entering Stop Mode

Stop mode is entered when setting the CM10 bit in the CM10 register to "1" (all clocks stops). The MCD4 to MCD0 bits in the MCD register become set to "010002" (divide-by-8 mode).

Enter stop mode after setting the followings.

- Initial Setting

Set each interrupt priority level after setting the exit priority level, required to exit stop mode, controlled by the RLVL2 to RLVL0 bits in the RLVL register, to "7".

- Before Entering stop mode

- (1) Set the I flag to "0"

- (2) Set the interrupt priority level of the interrupt being used to exit stop mode

- (3) Set the interrupt priority levels of the interrupts, not being used to exit stop mode, to "0"

- (4) Set IPL in the FLG register. Then set the exit priority level to the same level as IPL

Interrupt priority level of the interrupt used to exit stop mode > IPL = the exit priority level

- (5) Set the PRC0 bit in the PRCR register to "1" (write enable)

- (6) Select the main clock as the CPU clock

- When the CPU clock source is the sub clock,

- (a) set the CM05 bit in the CM0 register to "0" (main clock oscillates)

- (b) set the CM07 bit in the CM0 register to "0" (clock selected by the CM21 bit divided by MCD register setting)

- When the CPU clock source is the PLL clock,

- (a) set the CM17 bit in the CM1 register to "0" (main clock)

- (b) set the PLC07 bit in the PLC0 register to "0" (PLL off)

- When main clock direct mode is used,

- (a) set the PRC1 bit in the PRCR register to "1" (write enable)

- (b) set the PM24 bit in the PM2 register to "0" (clock selected by the CM07 bit)

- When the CPU clock source is the on-chip oscillator clock,

- (a) set MCD4 to MCD0 bits to "010002" (divide-by-8 mode)

- (b) set the CM05 bit to "0" (main clock oscillates)

- (c) set the CM21 bit in the CM2 register to "0" (clock selected by the CM17 bit)

- (7) The oscillation stop detect function is used, set the CM20 bit in the CM2 register to "0" (oscillation stop detect function disabled)

- (8) Set the I flag to "1"

- (9) Set the CM10 bit to "1" (all clocks stops)

- After Exiting Stop Mode

Set the exit priority level to "7" as soon as exiting stop mode.

9.5.3.2 Exiting Stop Mode

Stop mode is exited by the hardware reset, $\overline{\text{NMI}}$ interrupt or peripheral function interrupts (key input interrupt and $\overline{\text{INT}}$ interrupt).

When the hardware reset or $\overline{\text{NMI}}$ interrupt, but not the peripheral function interrupts, is used to exit wait mode, set all ILVL2 to ILVL0 bits in the interrupt control registers for the peripheral function interrupt to "0002" (interrupt disabled) before setting the CM10 bit to "1" (all clocks stops).

9.5.3.3 Pin Status in Stop Mode

Table 9.9 lists pin status in stop mode.

Table 9.9 Pin Status in Stop Mode

Pin		Memory Expansion Mode ⁽¹⁾ Microprocessor Mode ⁽¹⁾	Single-Chip Mode
Address Bus, Data Bus, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{BHE}}$		Maintains state immediately before entering stop mode	/
$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$		"H"	
$\overline{\text{HLDA}}$, $\overline{\text{BCLK}}$		"H"	
ALE		"H"	
Ports		Maintains state immediately before entering stop mode	
CLKOUT	When f _c selected	"H"	
	When f ₈ , f ₃₂ selected	Maintains state immediately before entering stop mode	
XIN		Placed in a high-impedance state	
XOUT		"H"	
XCIN, XCOUT		Placed in a high-impedance state	

NOTES:

1. M32C/84T cannot be used in memory expansion mode and microprocessor mode.

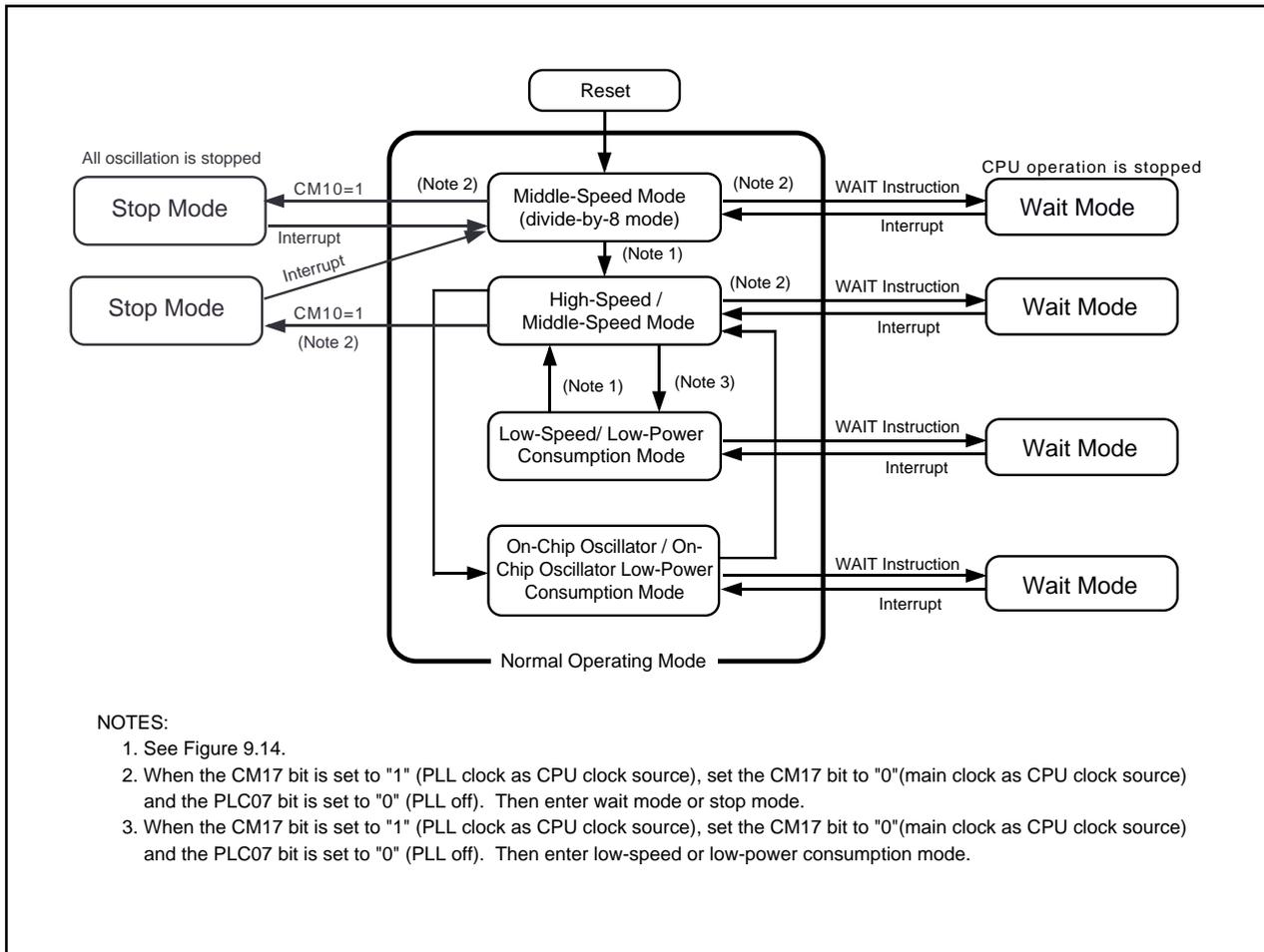


Figure 9.13 Status Transition in Wait Mode and Stop Mode

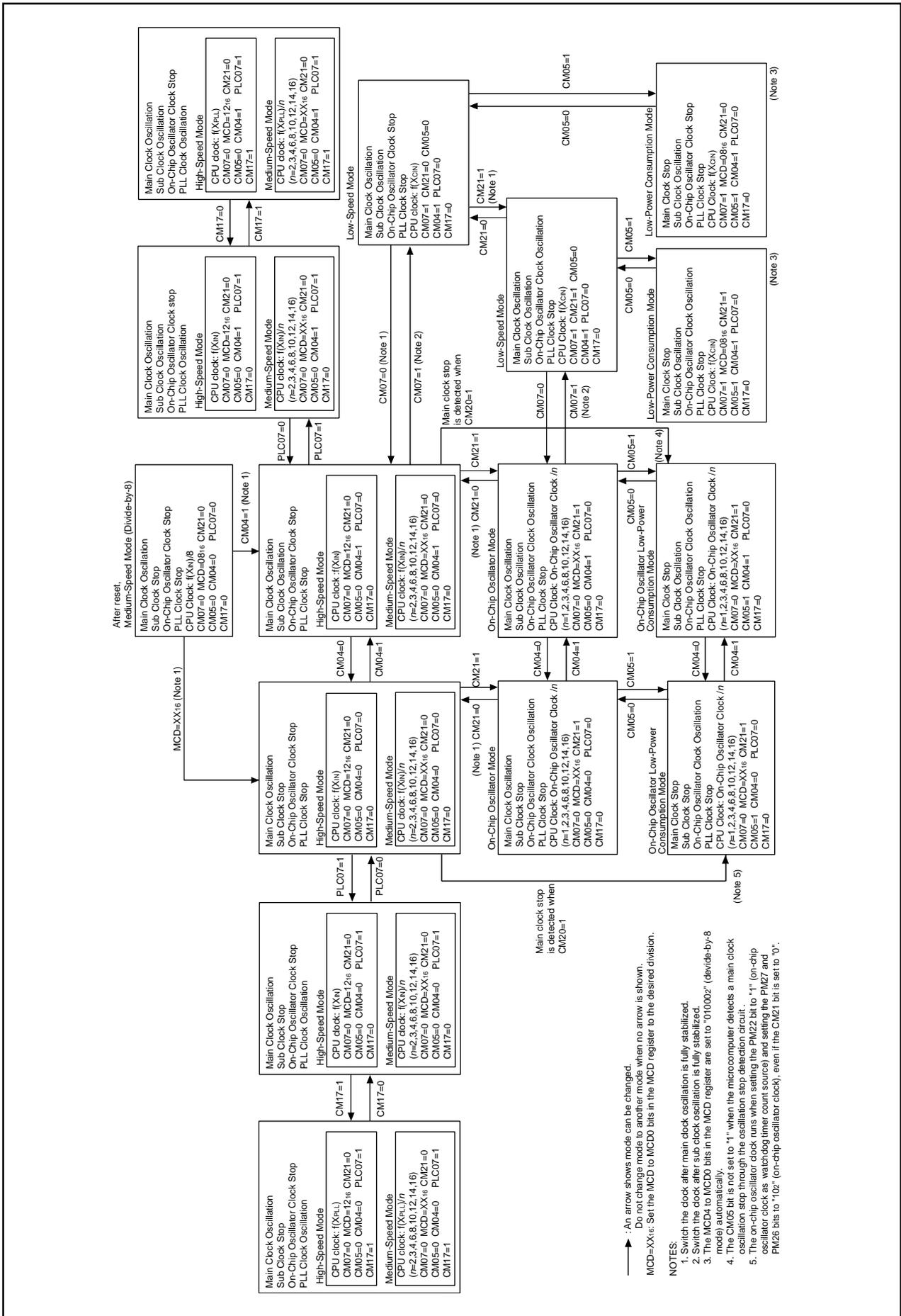


Figure 9.14 Status Transition

9.6 System Clock Protect Function

The system clock protect function prohibits the CPU clock from changing clock sources when the main clock is selected as the CPU clock source. This prevents the CPU clock from stopping the program crash. When the PM21 bit in the PM2 register is set to "1" (clock change disable), the following bits cannot be written to:

- The CM02 bit, CM05 bit and CM07 bit in the CM0 register
- The CM10 bit and CM17 bit in the CM1 register
- The CM20 bit in the CM2 register
- All bits in the PLC0 and PLC1 registers

The CPU clock continues running when the WAIT instruction is executed.

To use the system clock protect function, set the CM05 bit in the CM0 register to "0" (main clock oscillation) and CM07 bit to "0" (main clock as BCLK clock source) and follow the procedure below.

- (1) Set the PRC1 bit in the PRCR register to "1" (write enable).
- (2) Set the PM21 bit in the PM2 register to "1" (protects the clock).
- (3) Set the PRC1 bit in the PRCR register to "0" (write disable).

When the PM21 bit is set to "1", do not execute the WAIT instruction.

10. Protection

The protection function protects important registers from being easily overwritten when a program runs out of control.

Figure 10.1 shows the PRCR register. Each bit in the PRCR register protects the following registers:

- The PRC0 bit protects the CM0, CM1, CM2, MCD, PLC0 and PLC1 registers;
- The PRC1 bit protects the PM0, PM1, PM2, INVC0 and INVC1 registers;
- The PRC2 bit protects the PD9 and PS3 registers;
- The PRC3 bit protects the VCR2 and D4INT registers.

The PRC2 bit is set to "0" (write disable) when data is written to a desired address after setting the PRC2 bit to "1" (write enable). Set the PD9 and PS3 registers immediately after setting the PRC2 bit in the PRCR register to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the following instruction. The PRC0, PRC1 and PRC3 bits are not set to "0" even if data is written to desired addresses. Set the PRC0, PRC1 and PRC3 bits to "0" by program.

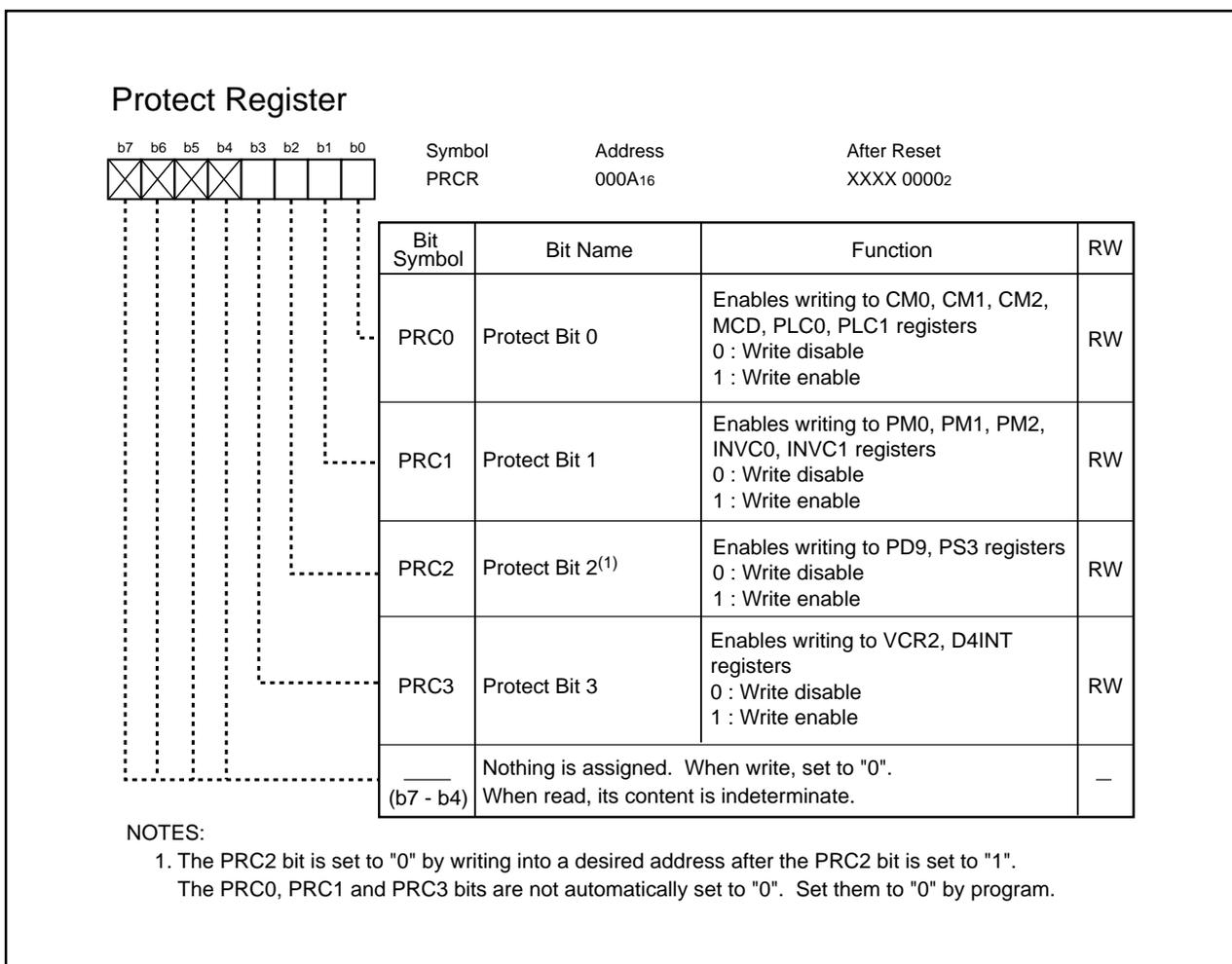


Figure 10.1 PRCR Register

11. Interrupts

11.1 Types of Interrupts

Figure 11.1 shows types of interrupts.

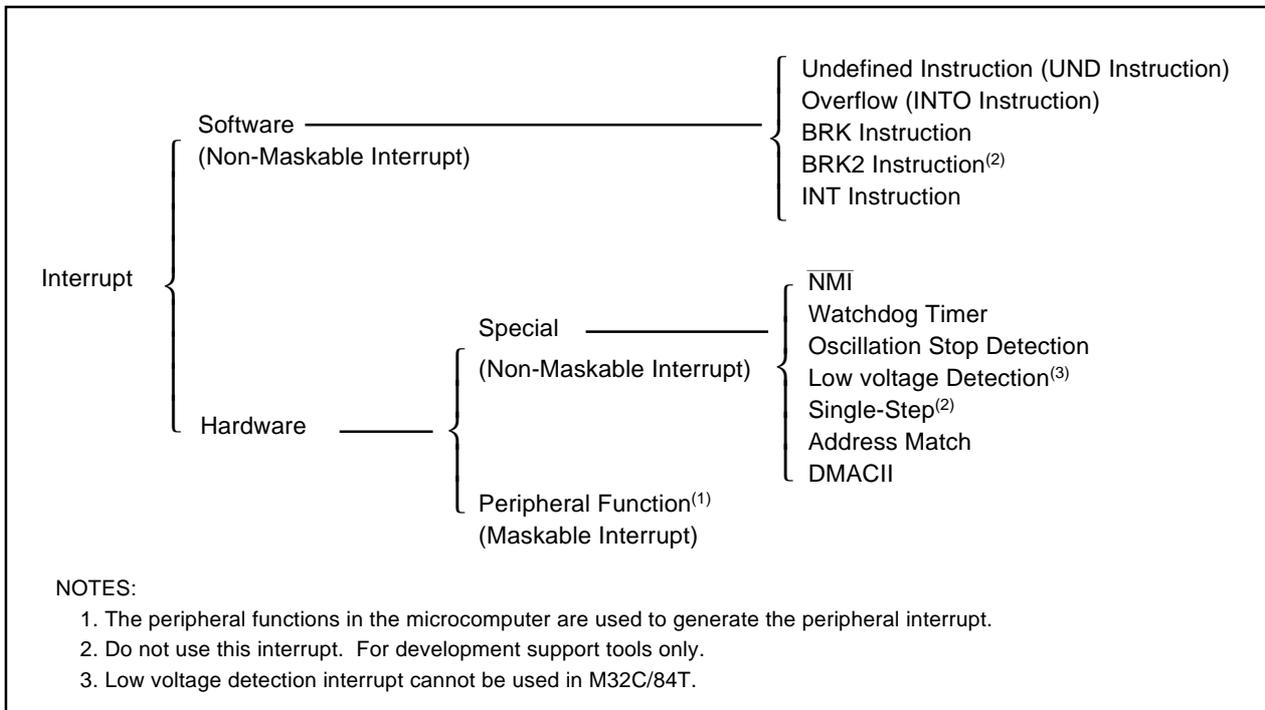


Figure 11.1 Interrupts

- Maskable Interrupt

The I flag enables or disables an interrupt.

The interrupt priority order based on interrupt priority level **can be changed**.

- Non-Maskable Interrupt

The I flag does not enable nor disable an interrupt .

The interrupt priority order based on interrupt priority level **cannot be changed**.

11.2 Software Interrupts

Software interrupt occurs when an instruction is executed. The software interrupts are non-maskable interrupts.

11.2.1 Undefined Instruction Interrupt

The undefined instruction interrupt occurs when the UND instruction is executed.

11.2.2 Overflow Interrupt

The overflow interrupt occurs when the O flag in the FLG register is set to "1" (overflow of arithmetic operation) and the INTO instruction is executed.

Instructions to set the O flag are :

ABS, ADC, ADCF, ADD, ADDX, CMP, CMPX, DIV, DIVU, DIVX, NEG, RMPA, SBB, SCMPU, SHA, SUB, SUBX

11.2.3 BRK Interrupt

The BRK interrupt occurs when the BRK instruction is executed.

11.2.4 BRK2 Interrupt

The BRK2 interrupt occurs when the BRK2 instruction is executed.

Do not use this interrupt. For development support tools only.

11.2.5 INT Instruction Interrupt

The INT instruction interrupt occurs when the INT instruction is executed. The INT instruction can select software interrupt numbers 0 to 63. Software interrupt numbers 8 to 48, 52 to 54 and 57 are assigned to the vector table used for the peripheral function interrupt. Therefore, the microcomputer executes the same interrupt routine when the INT instruction is executed as when a peripheral function interrupt occurs.

When the INT instruction is executed, the FLG register and PC are saved to the stack. PC also stores the relocatable vector of specified software interrupt numbers. Where the stack is saved varies depending on a software interrupt number. ISP is selected as the stack for software interrupt numbers 0 to 31 (setting the U flag to "0"). SP, which is set before the INT instruction is executed, is selected as the stack for software interrupt numbers 32 to 63 (the U flag is not changed).

With the peripheral function interrupt, the FLG register is saved and the U flag is set to "0" (ISP select) when an interrupt request is acknowledged. With software interrupt numbers 32 to 48, 52 to 54 and 57, SP to be used varies depending on whether the interrupt is generated by the peripheral function interrupt request or by the INT instruction.

11.3 Hardware Interrupts

Special interrupts and peripheral function interrupts are available as hardware interrupts.

11.3.1 Special Interrupts

Special interrupts are non-maskable interrupts.

11.3.1.1 $\overline{\text{NMI}}$ Interrupt

The $\overline{\text{NMI}}$ interrupt occurs when a signal applied to the $\overline{\text{NMI}}$ pin changes from a high-level ("H") signal to a low-level ("L") signal. Refer to **11.8 $\overline{\text{NMI}}$ Interrupt** for details.

11.3.1.2 Watchdog Timer Interrupt

The watchdog timer interrupt occurs when a count source of the watchdog timer underflows. Refer to **12. Watchdog Timer** for details.

11.3.1.3 Oscillation Stop Detection Interrupt

The oscillation stop detection interrupt occurs when the microcomputer detects a main clock oscillation stop. Refer to **9. Clock Generation Circuit** for details.

11.3.1.4 Low Voltage Detection Interrupt

The low voltage detection interrupt occurs when the voltage applied to VCC1 is above or below Vdet4. Refer to **6. Voltage Detection Circuit** for details.

NOTES:

1. Low voltage detection interrupt cannot be used in M32C/84T.

11.3.1.5 Single-Step Interrupt

Do not use the single-step interrupt. For development support tool only.

11.3.1.6 Address Match Interrupt

The address match interrupt occurs immediately before executing an instruction that is stored into an address indicated by the RMADi register (i=0 to 7) when the AIERi bit in the AIER register is set to "1" (address match interrupt enabled). Set the starting address of the instruction in the RMADi register. The address match interrupt does not occur when a table data or addresses of the instruction other than the starting address, if the instruction has multiple addresses, is set. Refer to **11.10 Address Match Interrupt** for details.

11.3.2 Peripheral Function Interrupt

The peripheral function interrupt occurs when a request from the peripheral functions in the microcomputer is acknowledged. The peripheral function interrupts and software interrupt numbers 8 to 48, 52 to 54 and 57 for the INT instruction use the same interrupt vector table. The peripheral function interrupt is a maskable interrupt.

See **Table 11.2** about how the peripheral function interrupt occurs. Refer to the descriptions of each function for details.

11.4 High-Speed Interrupt

The high-speed interrupt executes an interrupt sequence in five cycles and returns from the interrupt in three cycles.

When the FSIT bit in the RLVL register is set to "1" (interrupt priority level 7 available for the high-speed interrupt), the ILVL2 to ILVL0 bits in the interrupt control registers can be set to "1112" (level 7) to use the high-speed interrupt.

Only one interrupt can be set as the high-speed interrupt. When using the high-speed interrupt, do not set multiple interrupts to interrupt priority level 7. Set the DMAII bit in the RLVL register to "0" (interrupt priority level 7 available for interrupts).

Set the starting address of the high-speed interrupt routine in the VCT register.

When the high-speed interrupt is acknowledged, the FLG register is saved into the SVF register and PC is saved into the SVP register. The program is executed from an address indicated by the VCT register.

Execute the FREIT instruction to return from the high-speed interrupt routine.

The values saved into the SVF and SVP registers are restored to the FLG register and PC by executing the FREIT instruction.

The high-speed interrupt and the DMA2 and DMA3 use the same register. When using the high-speed interrupt, neither DMA2 nor DMA3 is available. DMA0 and DMA1 can be used.

11.5 Interrupts and Interrupt Vectors

There are four bytes in one vector. Set the starting address of interrupt routine in each vector table. When an interrupt request is acknowledged, the interrupt routine is executed from the address set in the interrupt vectors.

Figure 11.2 shows the interrupt vector.

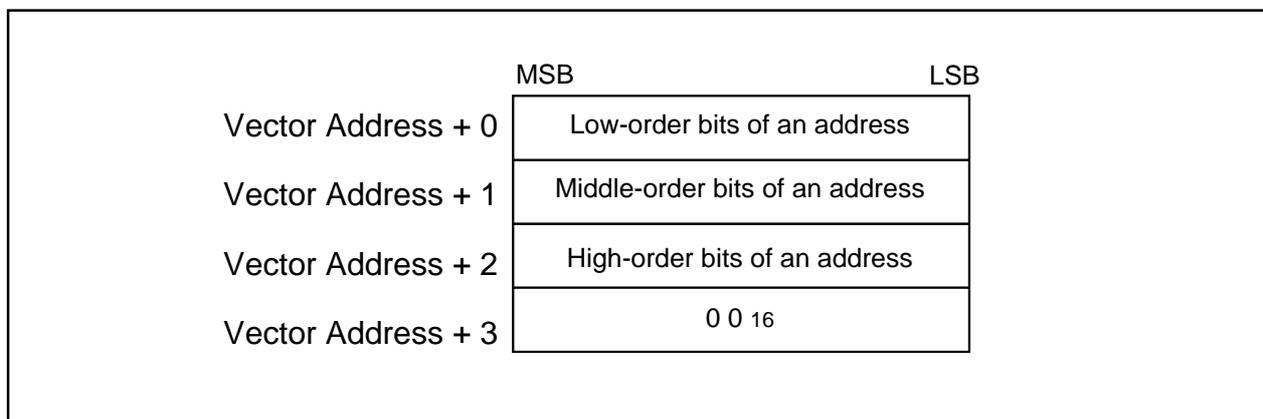


Figure 11.2 Interrupt Vector

11.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses FFFFDC₁₆ to FFFFFFF₁₆. Table 11.1 lists the fixed vector tables. Refer to **25.2 Functions to Prevent Flash Memory from Rewriting** for fixed vectors of flash memory.

Table 11.1 Fixed Vector Table

Interrupt Generated by	Vector Addresses Address (L) to Address (H)	Remarks	Reference
Undefined Instruction	FFFFDC ₁₆ to FFFFDF ₁₆		M32C/80 Series Software Manual
Overflow	FFFFE0 ₁₆ to FFFF E3 ₁₆		
BRK Instruction	FFFFE4 ₁₆ to FFFF E7 ₁₆	If the content of address FFFF E7 ₁₆ is FF ₁₆ , a program is executed from the address stored into software interrupt number 0 in the relocatable vector table	
Address Match	FFFFE8 ₁₆ to FFFF EB ₁₆		
-	FFFFEC ₁₆ to FFFF EF ₁₆	Reserved space	
Watchdog Timer	FFFFF0 ₁₆ to FFFF F3 ₁₆	These addresses are used for the watchdog timer interrupt, oscillation stop detection interrupt, and low voltage detection interrupt ⁽¹⁾	Reset, Clock Generation Circuit, Watchdog Timer
-	FFFFF4 ₁₆ to FFFF F7 ₁₆	Reserved space	
NMI	FFFFF8 ₁₆ to FFFF FB ₁₆		
Reset	FFFFFC ₁₆ to FFFF FF ₁₆		Reset

NOTES:

1. Low voltage detection interrupt cannot be used in M32C/84T.

11.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes from the starting address set in the INTB register. Table 11.2 lists the relocatable vector tables.

Set an even address as the starting address of the vector table set in the INTB register to increase interrupt sequence execution rate.

Table 11.2 Relocatable Vector Tables

Interrupt Generated by	Vector Table Address Address(L) to Address(H) ⁽¹⁾	Software Interrupt Number	Reference
BRK Instruction ⁽²⁾	+0 to +3 (0000 ₁₆ to 0003 ₁₆)	0	M32C/80 Series
Reserved Space	+4 to +31 (0004 ₁₆ to 001F ₁₆)	1 to 7	Software Manual
DMA0	+32 to +35 (0020 ₁₆ to 0023 ₁₆)	8	DMAC
DMA1	+36 to +39 (0024 ₁₆ to 0027 ₁₆)	9	
DMA2	+40 to +43 (0028 ₁₆ to 002B ₁₆)	10	
DMA3	+44 to +47 (002C ₁₆ to 002F ₁₆)	11	
Timer A0	+48 to +51 (0030 ₁₆ to 0033 ₁₆)	12	Timer A
Timer A1	+52 to +55 (0034 ₁₆ to 0037 ₁₆)	13	
Timer A2	+56 to +59 (0038 ₁₆ to 003B ₁₆)	14	
Timer A3	+60 to +63 (003C ₁₆ to 003F ₁₆)	15	
Timer A4	+64 to +67 (0040 ₁₆ to 0043 ₁₆)	16	
UART0 Transmission, NACK ⁽³⁾	+68 to +71 (0044 ₁₆ to 0047 ₁₆)	17	Serial I/O
UART0 Reception, ACK ⁽³⁾	+72 to +75 (0048 ₁₆ to 004B ₁₆)	18	
UART1 Transmission, NACK ⁽³⁾	+76 to +79 (004C ₁₆ to 004F ₁₆)	19	
UART1 Reception, ACK ⁽³⁾	+80 to +83 (0050 ₁₆ to 0053 ₁₆)	20	
Timer B0	+84 to +87 (0054 ₁₆ to 0057 ₁₆)	21	Timer B
Timer B1	+88 to +91 (0058 ₁₆ to 005B ₁₆)	22	
Timer B2	+92 to +95 (005C ₁₆ to 005F ₁₆)	23	
Timer B3	+96 to +99 (0060 ₁₆ to 0063 ₁₆)	24	
Timer B4	+100 to +103 (0064 ₁₆ to 0067 ₁₆)	25	
INT5	+104 to +107 (0068 ₁₆ to 006B ₁₆)	26	Interrupt
INT4	+108 to +111 (006C ₁₆ to 006F ₁₆)	27	
INT3	+112 to +115 (0070 ₁₆ to 0073 ₁₆)	28	
INT2	+116 to +119 (0074 ₁₆ to 0077 ₁₆)	29	
INT1	+120 to +123 (0078 ₁₆ to 007B ₁₆)	30	
INT0	+124 to +127 (007C ₁₆ to 007F ₁₆)	31	
Timer B5	+128 to +131 (0080 ₁₆ to 0083 ₁₆)	32	Timer B
UART2 Transmission, NACK ⁽³⁾	+132 to +135 (0084 ₁₆ to 0087 ₁₆)	33	Serial I/O
UART2 Reception, ACK ⁽³⁾	+136 to +139 (0088 ₁₆ to 008B ₁₆)	34	
UART3 Transmission, NACK ⁽³⁾	+140 to +143 (008C ₁₆ to 008F ₁₆)	35	
UART3 Reception, ACK ⁽³⁾	+144 to +147 (0090 ₁₆ to 0093 ₁₆)	36	
UART4 Transmission, NACK ⁽³⁾	+148 to +151 (0094 ₁₆ to 0097 ₁₆)	37	
UART4 Reception, ACK ⁽³⁾	+152 to +155 (0098 ₁₆ to 009B ₁₆)	38	

Table 11.2 Relocatable Vector Tables (Continued)

Interrupt Generated by	Vector Table Address Address("L") to Address("H") ⁽¹⁾	Software Interrupt Number	Reference
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect (UART2) ⁽³⁾	+156 to +159 (009C ₁₆ to 009F ₁₆)	39	Serial I/O
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect (UART3/UART0) ⁽⁴⁾	+160 to +163 (00A0 ₁₆ to 00A3 ₁₆)	40	
Bus Conflict Detect, Start Condition Select, Stop Condition Detect(UART4/UART1) ⁽⁴⁾	+164 to +167 (00A4 ₁₆ to 00A7 ₁₆)	41	
A/D0	+168 to +171 (00A8 ₁₆ to 00AB ₁₆)	42	A/D Converter
Key Input	+172 to +175 (00AC ₁₆ to 00AF ₁₆)	43	Interrupts
Intelligent I/O Interrupt 0	+176 to +179 (00B0 ₁₆ to 00B3 ₁₆)	44	Intelligent I/O
Intelligent I/O Interrupt 1	+180 to +183 (00B4 ₁₆ to 00B7 ₁₆)	45	
Intelligent I/O Interrupt 2	+184 to +187 (00B8 ₁₆ to 00BB ₁₆)	46	
Intelligent I/O Interrupt 3	+188 to +191 (00BC ₁₆ to 00BF ₁₆)	47	
Intelligent I/O Interrupt 4	+192 to +195 (00C0 ₁₆ to 00C3 ₁₆)	48	
Reserved Space	+196 to +207 (00C4 ₁₆ to 00CF ₁₆)	49 to 51	—
Intelligent I/O Interrupt 8	+208 to +211 (00D0 ₁₆ to 00D3 ₁₆)	52	Intelligent I/O
Intelligent I/O Interrupt 9, CAN 0	+212 to +215 (00D4 ₁₆ to 00D7 ₁₆)	53	Intelligent I/O
Intelligent I/O Interrupt 10, CAN 1	+216 to +219 (00D8 ₁₆ to 00DB ₁₆)	54	CAN
Reserved Space	+220 to +227 (00DC ₁₆ to 00E3 ₁₆)	55, 56	—
CAN 2	+228 to +231 (00E4 ₁₆ to 00E7 ₁₆)	57	CAN
Reserved Space	+232 to +255 (00E8 ₁₆ to 00FF ₁₆)	58 to 63	—
INT Instruction ⁽²⁾	+0 to +3 (0000 ₁₆ to 0003 ₁₆) to +252 to +255 (00FC ₁₆ to 00FF ₁₆)	0 to 63	Interrupts

NOTES:

1. These addresses are relative to those in the INTB register.
2. The I flag does not disable interrupts.
3. In I²C mode, NACK, ACK or start/stop condition detection causes interrupts to be generated.
4. The IFSR6 bit in the IFSR register determines whether these addresses are used for an interrupt in UART0 or in UART3.
The IFSR7 bit in the IFSR register determines whether these addresses are used for an interrupt in UART1 or in UART4.

11.6 Interrupt Request Acknowledgement

Software interrupts and special interrupts occur when conditions to generate an interrupt are met.

The peripheral function interrupts are acknowledged when all conditions below are met.

- I flag = "1"
- IR bit = "1"
- ILVL2 to ILVL0 bits > IPL

The I flag, IPL, IR bit and ILVL2 to ILVL0 bits are independent of each other. The I flag and IPL are in the FLG register. The IR bit and ILVL2 to ILVL0 bits are in the interrupt control register.

11.6.1 I Flag and IPL

The I flag enables or disables maskable interrupts. When the I flag is set to "1" (enable), all maskable interrupts are enabled; when the I flag is set to "0" (disable), they are disabled. The I flag is automatically set to "0" after reset.

IPL, consisting of three bits, indicates the interrupt priority level from level 0 to level 7.

If a requested interrupt has higher priority level than indicated by IPL, the interrupt is acknowledged.

Table 11.3 lists interrupt priority levels associated with IPL.

Table 11.3 Interrupt Priority Levels

IPL2	IPL1	IPL0	Interrupt Priority Levels
0	0	0	Level 1 and above
0	0	1	Level 2 and above
0	1	0	Level 3 and above
0	1	1	Level 4 and above
1	0	0	Level 5 and above
1	0	1	Level 6 and above
1	1	0	Level 7 and above
1	1	1	All maskable interrupts are disabled

11.6.2 Interrupt Control Register and RLVL Register

The peripheral function interrupts use interrupt control registers to control each interrupt. Figures 11.3 and 11.4 show the interrupt control register. Figure 11.5 shows the RLVL register.

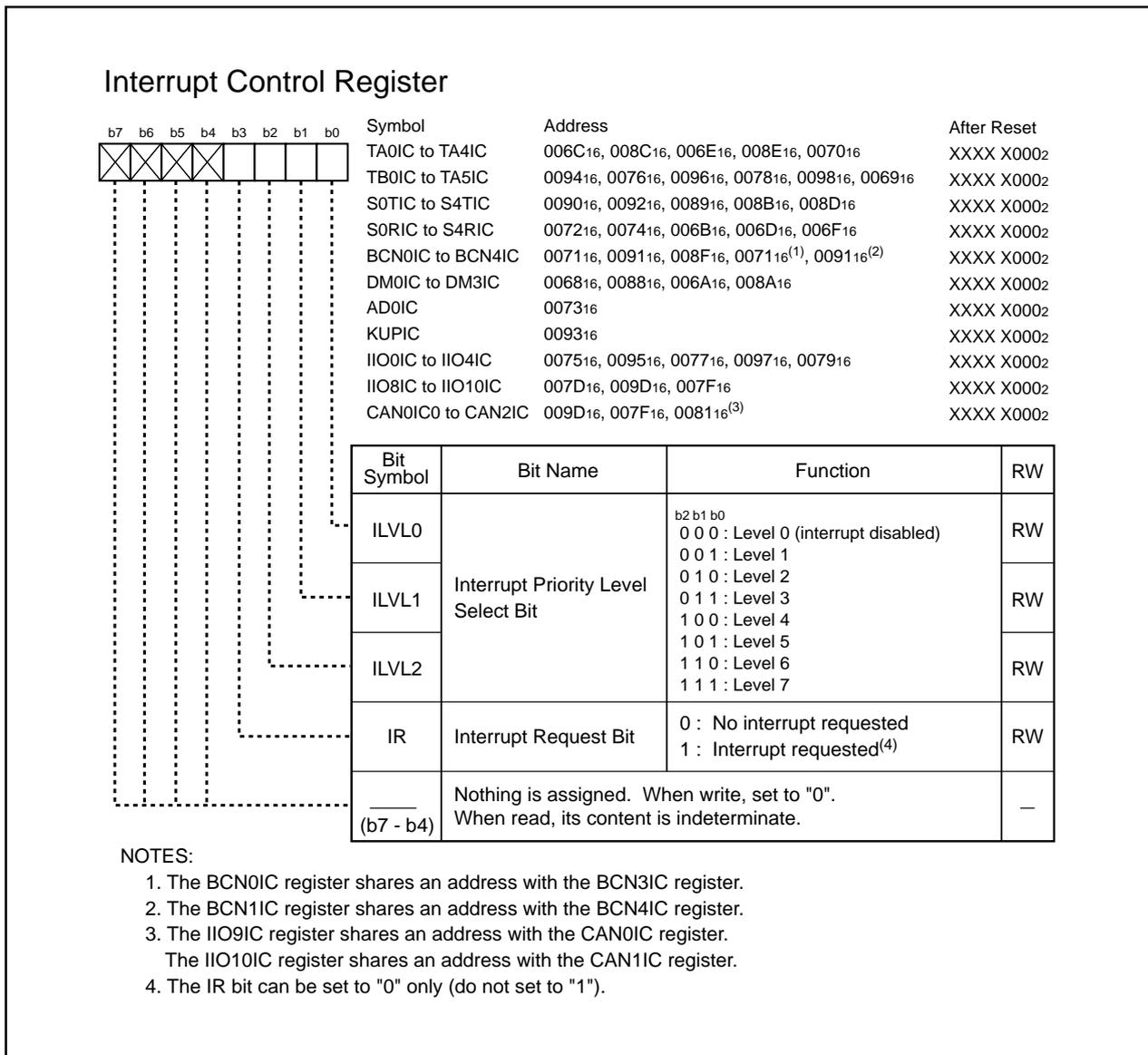


Figure 11.3 Interrupt Control Register (1)

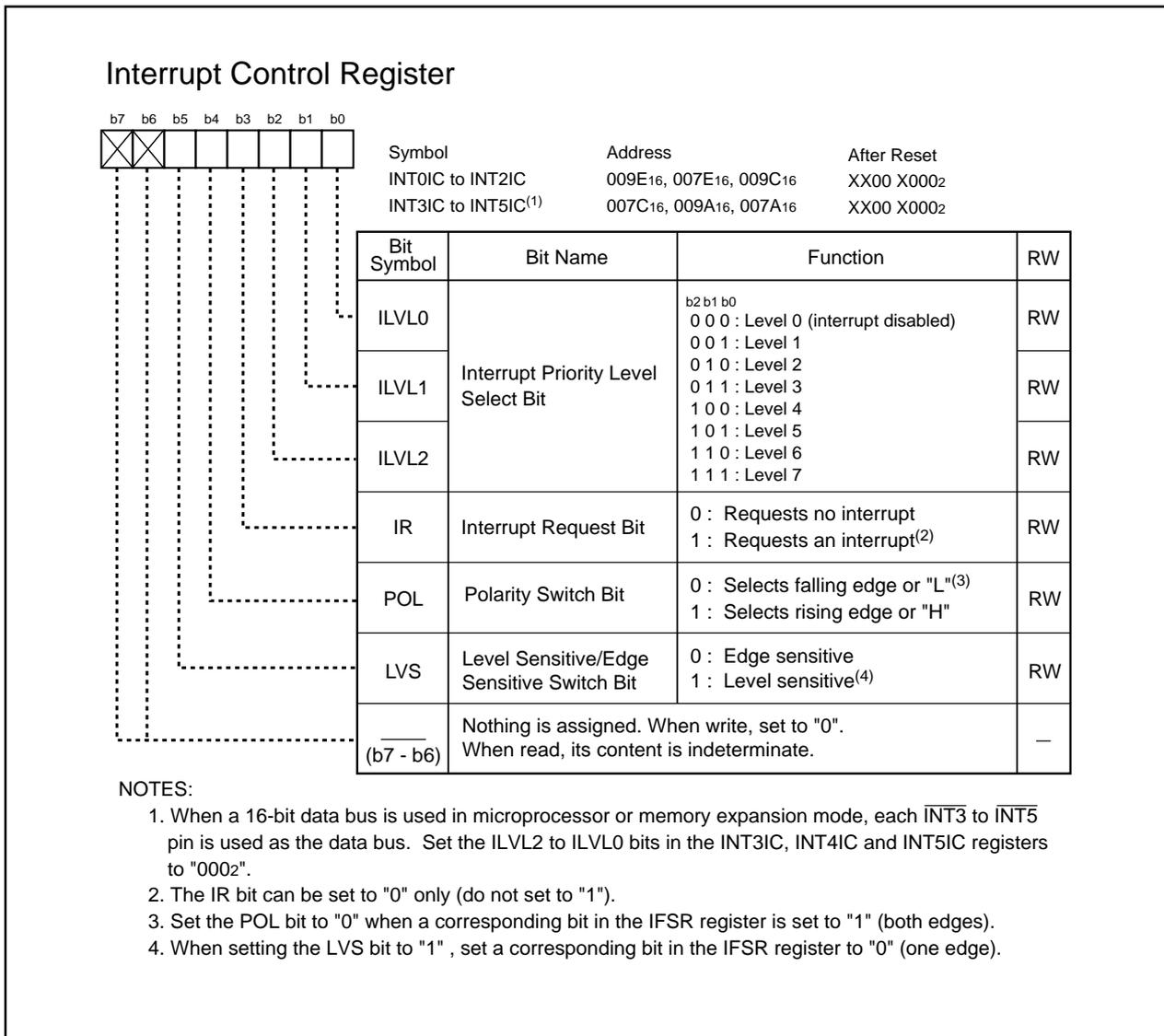


Figure 11.4 Interrupt Control Register (2)

11.6.2.1 ILVL2 to ILVL0 Bits

The ILVL2 to ILVL0 bits determines an interrupt priority level. The higher the interrupt priority level is, the higher the interrupt priority is.

When an interrupt request is generated, its interrupt priority level is compared to IPL. This interrupt is acknowledged only when its interrupt priority level is higher than IPL. When the ILVL2 to ILVL0 bits are set to "0002" (level 0), its interrupt is ignored.

11.6.2.2 IR Bit

The IR bit is automatically set to "1" (interrupt requested) when an interrupt request is generated. The IR bit is automatically set to "0" (no interrupt requested) after an interrupt request is acknowledged and an interrupt routine in the corresponding interrupt vector is executed.

The IR bit can be set to "0" by program. Do not set to "1".

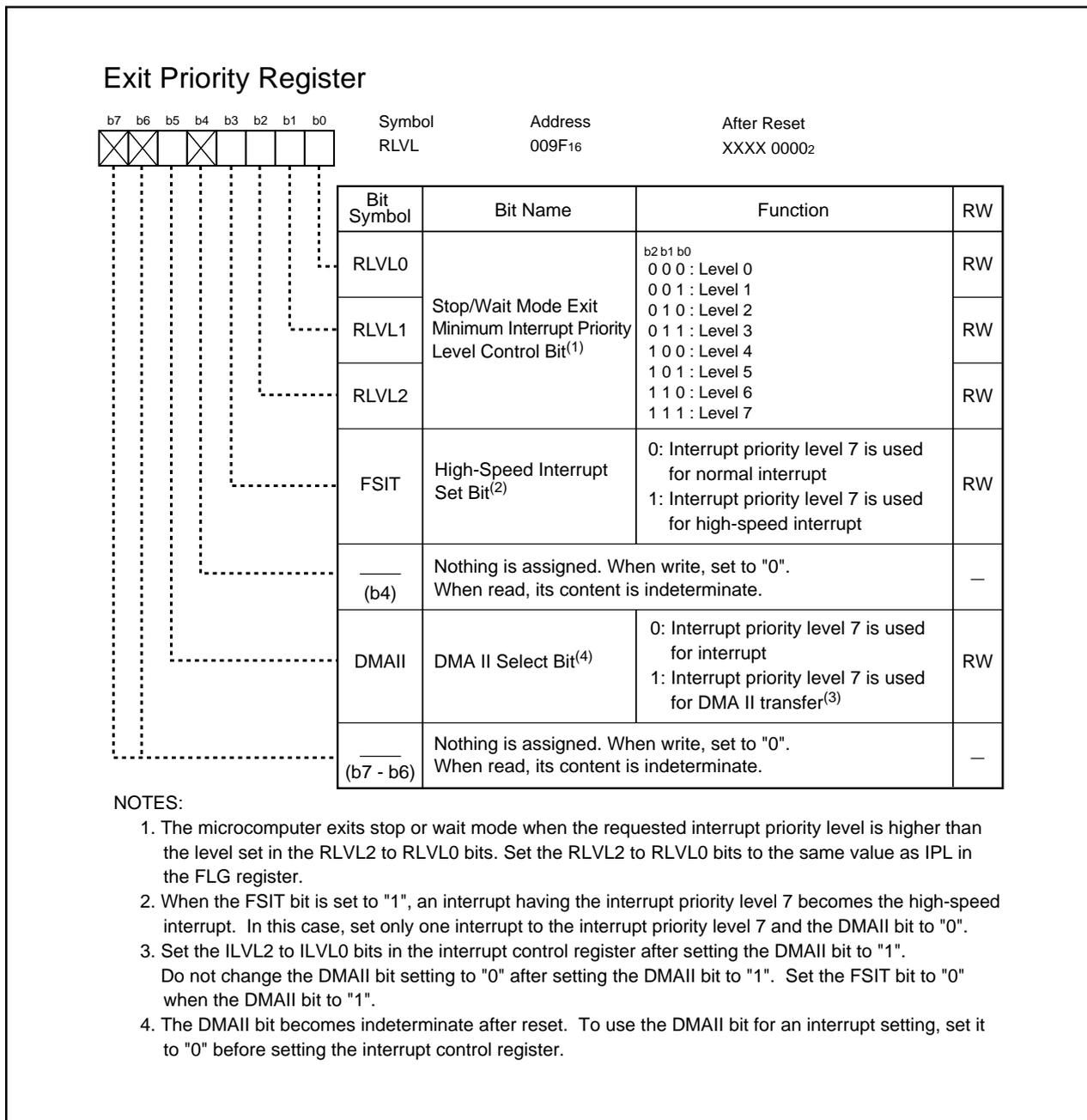


Figure 11.5 RLVL Register

11.6.2.3 RLVL2 to RLVL0 Bits

When using an interrupt to exit stop or wait mode, refer to **9.5.2 Wait Mode** and **9.5.3 Stop Mode** for details.

11.6.3 Interrupt Sequence

The interrupt sequence is performed between an interrupt request acknowledgment and interrupt routine execution.

When an interrupt request is generated while an instruction is executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, in regards to the SCMPU, SIN, SMOVB, SMOVF, SMOVU, SSTR, SOUT or RMPA instruction, if an interrupt request is generated while executing the instruction, the microcomputer suspends the instruction to start the interrupt sequence.

The interrupt sequence is performed as follows:

- (1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 000000₁₆ (address 000002₁₆ for the high-speed interrupt). Then, the IR bit applicable to the interrupt information is set to "0" (interrupt requested).
- (2) The FLG register, prior to an interrupt sequence, is saved to a temporary register⁽¹⁾ within the CPU.
- (3) Each bit in the FLG register is set as follows:
 - The I flag is set to "0" (interrupt disabled)
 - The D flag is set to "0" (single-step disabled)
 - The U flag is set to "0" (ISP selected)
- (4) A temporary register within the CPU is saved to the stack; or to the SVF register for the high-speed interrupt.
- (5) PC is saved to the stack; or to the SVP register for the high-speed interrupt.
- (6) The interrupt priority level of the acknowledged interrupt is set in IPL .
- (7) A relocatable vector corresponding to the acknowledged interrupt is stored into PC.

After the interrupt sequence is completed, an instruction is executed from the starting address of the interrupt routine.

NOTES:

1. Temporary register cannot be modified by users.

11.6.4 Interrupt Response Time

Figure 11.6 shows an interrupt response time. Interrupt response time is the period between an interrupt generation and the execution of the first instruction in an interrupt routine. Interrupt response time includes the period between an interrupt request generation and the completed execution of an instruction ((a) on Figure 11.6) and the period required to perform an interrupt sequence ((b) on Figure 11.6).

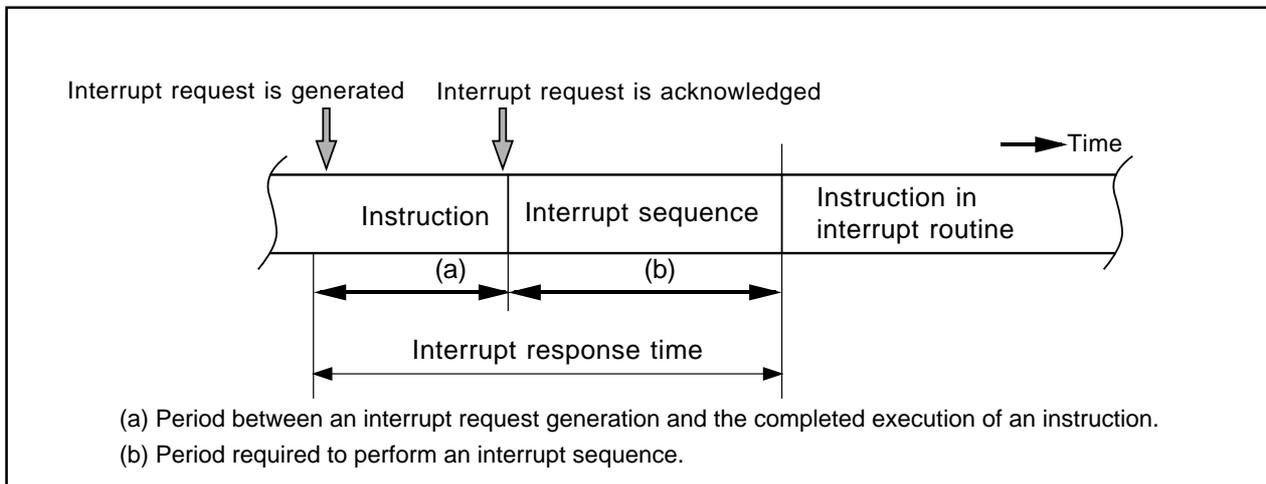


Figure 11.6 Interrupt Response Time

Time (a) varies depending on an instruction being executed. The DIVX instruction requires the longest time (a); 42 cycles when an immediate value or register is set as the divisor.

When the divisor is a value in the memory, the following value is added.

- Normal addressing : $2 + X$
- Index addressing : $3 + X$
- Indirect addressing : $5 + X + 2Y$
- Indirect index addressing : $6 + X + 2Y$

X is the number of wait states for a divisor space. Y is the number of wait states for the space that stores indirect addresses. If X and Y are in an odd address or in 8-bit bus space, the X and Y value must be doubled.

Table 11.4 lists time (b) shown Figure 11.6.

Table 11.4 Interrupt Sequence Execution Time

Interrupt	Interrupt Vector Address	16-Bit Bus	8-Bit Bus
Peripheral Function	Even address	14 cycles	16 cycles
	Odd address ⁽¹⁾	16 cycles	16 cycles
INT Instruction	Even address	12 cycles	14 cycles
	Odd address ⁽¹⁾	14 cycles	14 cycles
NMI Watchdog Timer Undefined Instruction Address Match	Even address ⁽²⁾	13 cycles	15 cycles
Overflow	Even address ⁽²⁾	14 cycles	16 cycles
BRK Instruction (relocatable vector table)	Even address	17 cycles	19 cycles
	Odd address ⁽¹⁾	19 cycles	19 cycles
BRK Instruction (fixed vector table)	Even address ⁽²⁾	19 cycles	21 cycles
High-Speed Interrupt	Vector table is internal register	5 cycles	

NOTES:

1. Allocate interrupt vectors in even addresses.
2. Vectors are fixed to even addresses.

11.6.5 IPL Change when Interrupt Request is Acknowledged

When a peripheral function interrupt request is acknowledged, IPL sets the priority level for the acknowledged interrupt.

Software interrupts and special interrupts have no interrupt priority level. If an interrupt request that has no interrupt priority level is acknowledged, the value shown in Table 11.5 is set in IPL as the interrupt priority level.

Table 11.5 Interrupts without Interrupt Priority Levels and IPL

Interrupt Source	Level Set to IPL
Watchdog Timer, NMI, Oscillation Stop Detection, Low Voltage Detection	7
Reset	0
Software, Address Match	Not changed

NOTES:

1. Low voltage detection interrupt cannot be used in M32C/84T.

11.6.6 Saving a Register

In the interrupt sequence, the FLG register and PC are saved to the stack.

After the FLG register is saved to the stack, 16 high-order bits and 16 low-order bits of PC, extended to 32 bits, are saved to the stack. Figure 11.7 shows stack states before and after an interrupt request is acknowledged.

Other important registers are saved by program at the beginning of an interrupt routine. The PUSHM instruction can save several registers⁽¹⁾ in the register bank used.

Refer to **11.4 High-Speed Interrupt** for the high-speed interrupt.

NOTES:

1. Can be selected from the R0, R1, R2, R3, A0, A1, SB and FB registers.

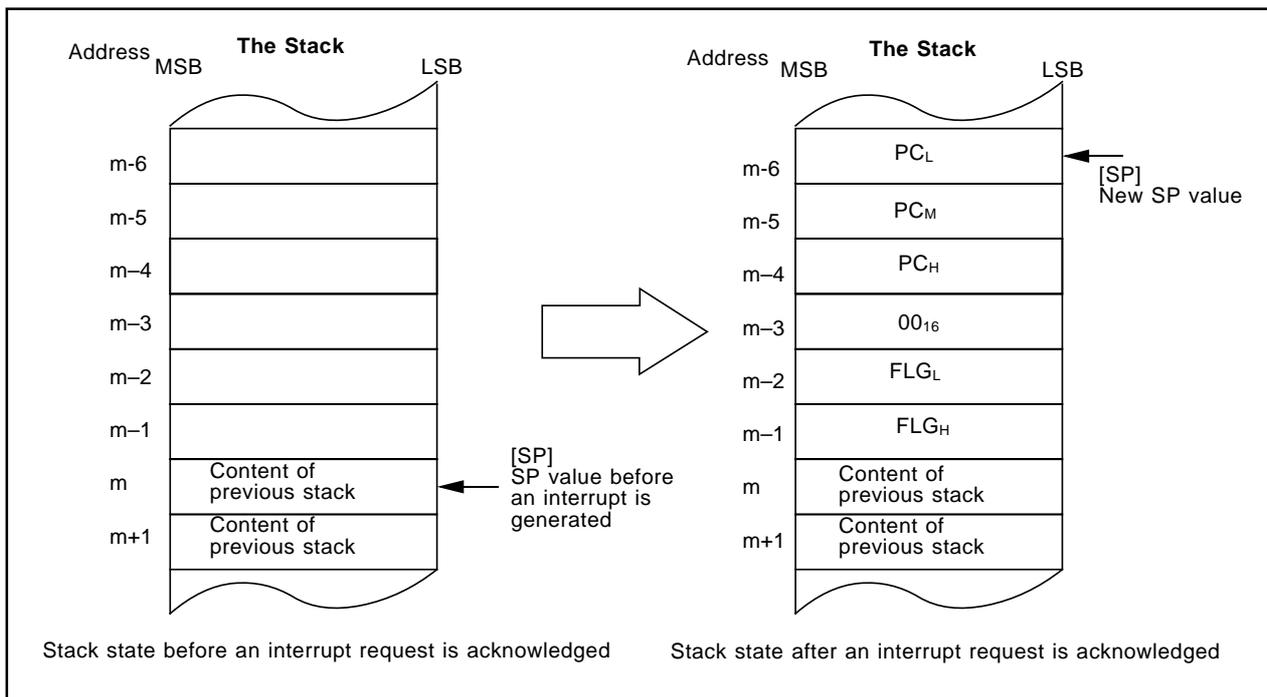


Figure 11.7 Stack States

11.6.7 Restoration from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC before the interrupt sequence is performed, which have been saved to the stack, are automatically restored. The program, executed before an interrupt request was acknowledged, starts running again. Refer to **11.4 High-Speed Interrupt** for the high-speed interrupt.

Restore registers saved by program in an interrupt routine by the POPM instruction or others before the REIT and FREIT instructions. Register bank is switched back to the bank used prior to the interrupt sequence by the REIT or FREIT instruction.

11.6.8 Interrupt Priority

If two or more interrupt requests are existed at the same sampling points (a timing to detect whether an interrupt request is generated or not), the interrupt with the highest priority is acknowledged.

Set the ILVL2 to ILVL0 bits to select the desired priority level for maskable interrupts (peripheral function interrupt).

Priority levels of special interrupts such as reset (reset has the highest priority) and watchdog timer are set by hardware. Figure 11.8 shows priority levels of hardware interrupts.

The interrupt priority does not affect software interrupts. Executing instruction causes the microcomputer to execute an interrupt routine.

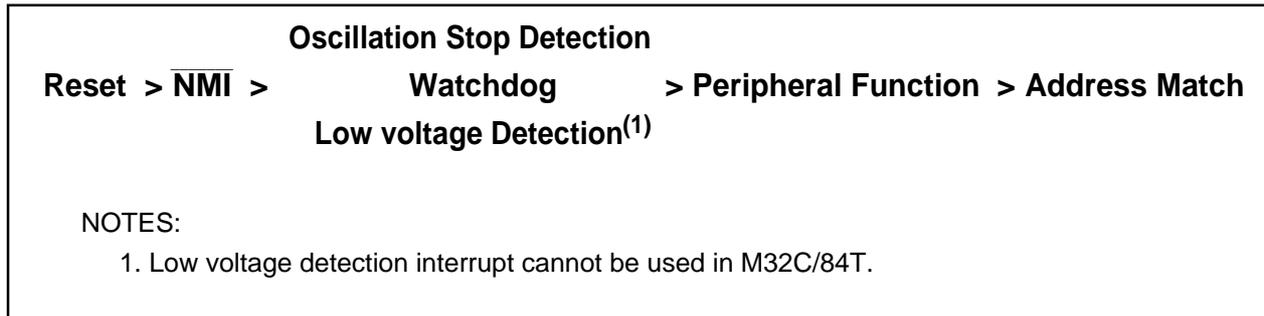


Figure 11.8 Interrupt Priority

11.6.9 Interrupt Priority Level Select Circuit

The interrupt priority level select circuit selects the highest priority interrupt when two or more interrupt requests are existed at the same sampling point.

Figure 11.9 shows the interrupt priority level select circuit.

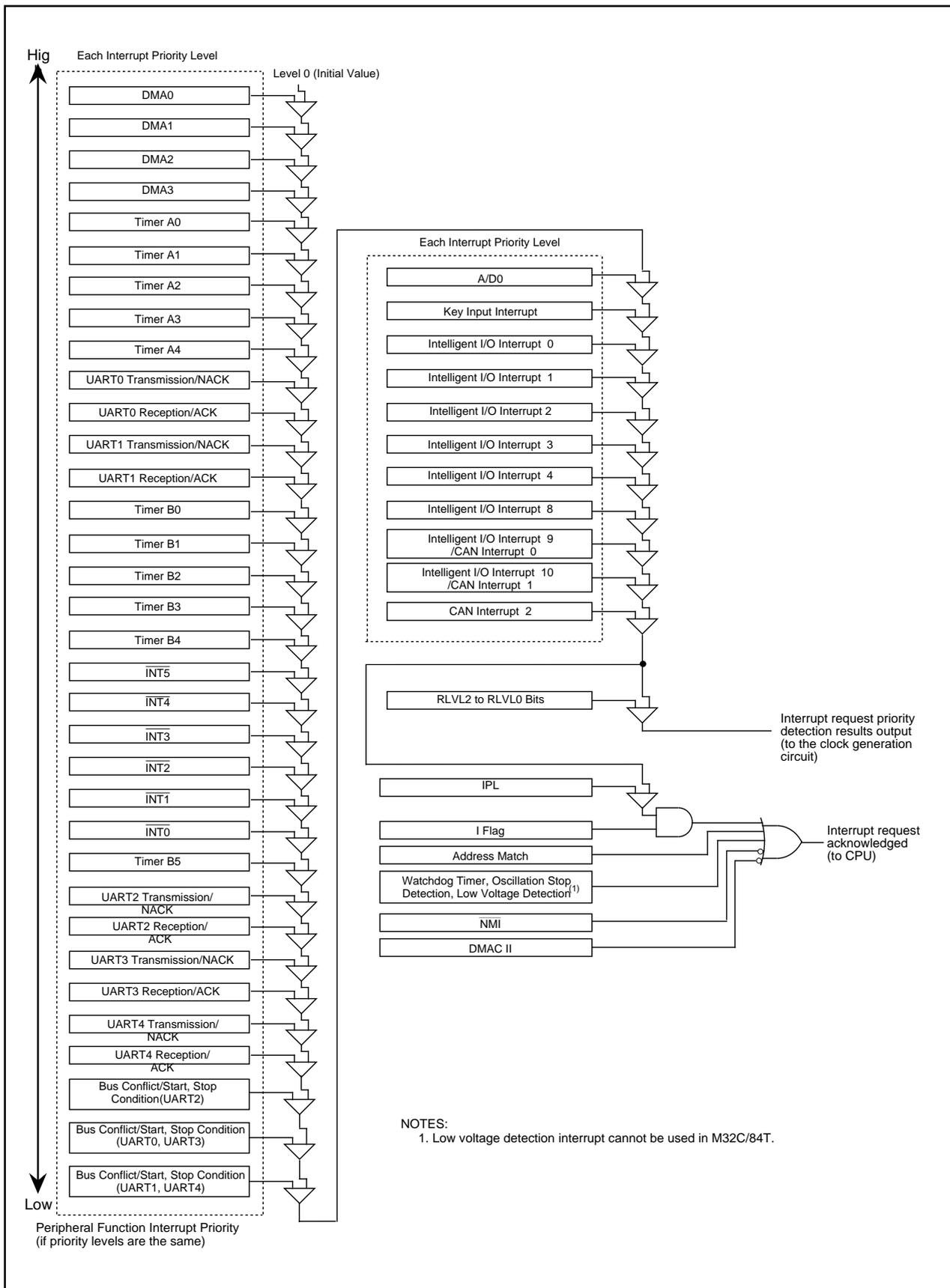


Figure 11.9 Interrupt Priority Level Select Circuit

11.7 $\overline{\text{INT}}$ Interrupt

External input generates the $\overline{\text{INT}}_i$ interrupt ($i = 0$ to 5). The LVS bit in the INTiIC register selects either edge sensitive triggering to generate an interrupt on any edge or level sensitive triggering to generate an interrupt at an applied signal level. The POL bit in the INTiIC register determines the polarity.

For edge sensitive, when the IFSR_i bit in the IFSR register is set to "1", an interrupt occurs on both rising and falling edges of the external input. If the IFSR_i bit is set to "1", set the POL bit in the corresponding register to "0" (falling edge).

For level sensitive, set the IFSR_i bit to "0" (single edge). When the $\overline{\text{INT}}_i$ pin input level reaches the level set in the POL bit, the IR bit in the INTiIC register is set to "1". The IR bit remains unchanged even if the $\overline{\text{INT}}_i$ pin level is changed. The IR bit is set to "0" when the $\overline{\text{INT}}_i$ interrupt is acknowledged or when the IR bit is written to "0" by program.

Figure 11.10 shows the IFSR register.

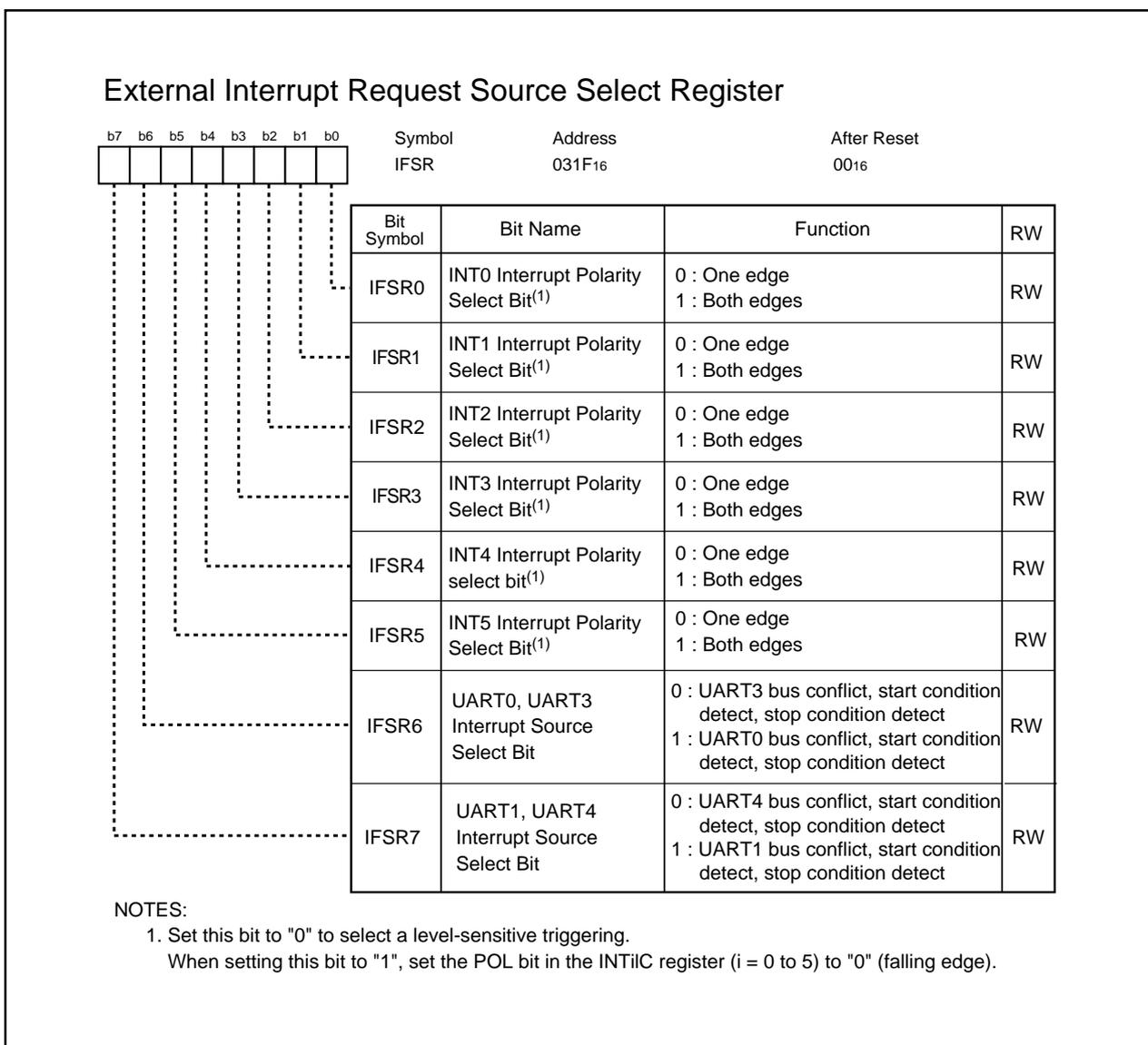


Figure 11.10 IFSR Register

11.8 $\overline{\text{NMI}}$ Interrupt⁽¹⁾

The $\overline{\text{NMI}}$ interrupt occurs when a signal applied to the $\overline{\text{NMI}}$ pin changes from a high-level ("H") signal to a low-level ("L") signal. The $\overline{\text{NMI}}$ interrupt is a non-maskable interrupt. Although the P85/ $\overline{\text{NMI}}$ pin is used as the $\overline{\text{NMI}}$ interrupt input pin, the P8_5 bit in the P8 register indicates the input level for this pin.

NOTES:

1. When the $\overline{\text{NMI}}$ interrupt is not used, connect the $\overline{\text{NMI}}$ pin to VCC1 via a resistor. Because the $\overline{\text{NMI}}$ interrupt cannot be ignored, the pin must be connected.

11.9 Key Input Interrupt

Key input interrupt request is generated when one of the signals applied to the P104 to P107 pins in input mode is on the falling edge. The key input interrupt can be also used as key-on wake-up function to exit wait or stop mode. To use the key input interrupt, do not use P104 to P107 as A/D input ports. Figure 11.11 shows a block diagram of the key input interrupt. When an "L" signal is applied to any pins in input mode, signals applied to other pins are not detected as an interrupt request signal.

When the PSC_7 bit in the PSC register⁽²⁾ is set to "1" (key input interrupt disabled), no key input interrupt occurs regardless of interrupt control register settings. When the PSC_7 bit is set to "1", no input from a port pin is available even when in input mode.

NOTES:

2. Refer to **24. Programmable I/O Ports** about the PSC register.

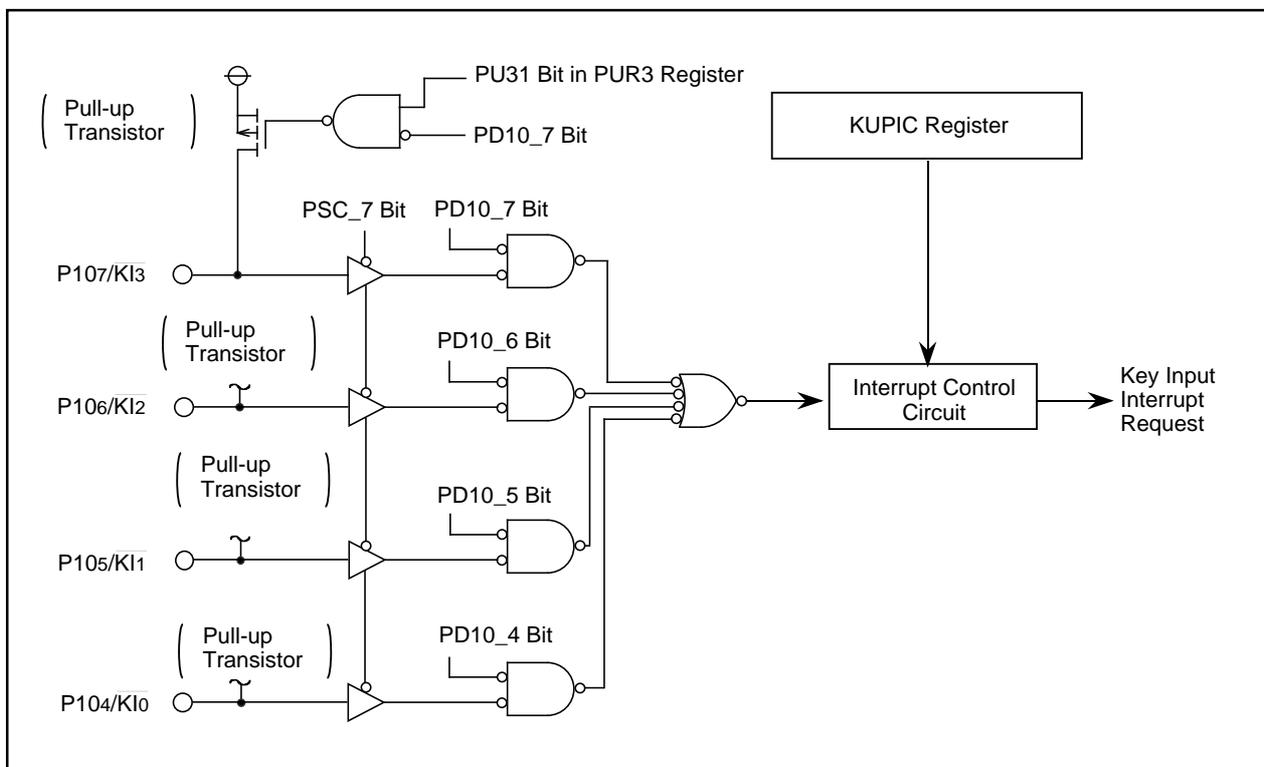


Figure 11.11 Key Input Interrupt

11.10 Address Match Interrupt

The address match interrupt occurs immediately before executing an instruction that is stored into an address indicated by the RMAD_i register (i=0 to 7). The address match interrupt can be set in eight addresses. The AIER_i bit in the AIER register determines whether the interrupt is enabled or disabled. The I flag and IPL do not affect the address match interrupt.

Figure 11.12 shows registers associated with the address match interrupt.

The starting address of an instruction must be set in the RMAD_i register. The address match interrupt does not occur when a table data or addresses other than the starting address of the instruction is set.

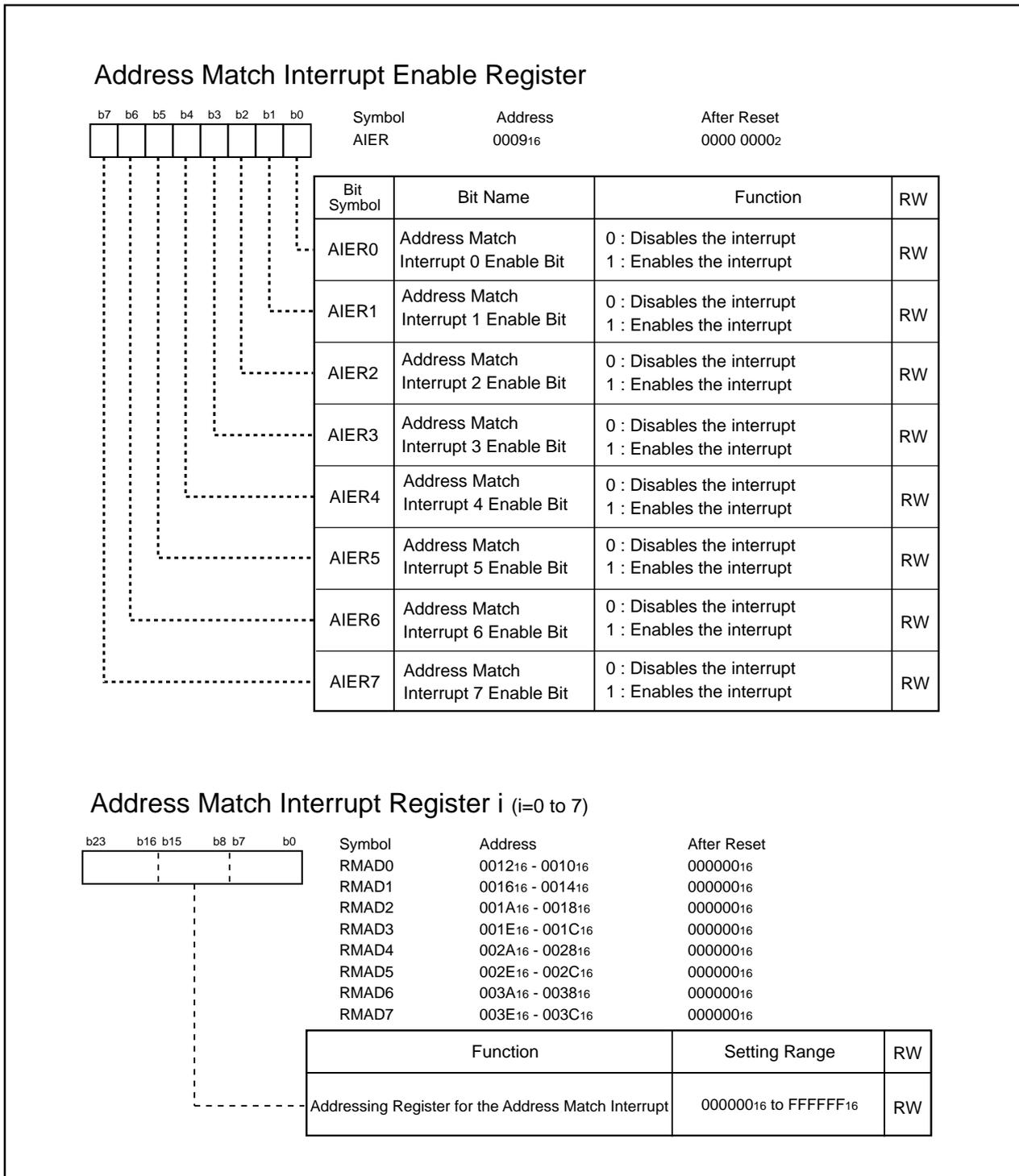


Figure 11.12 AIER Register and RMAD0 to RMAD7 Registers

11.11 Intelligent I/O Interrupt and CAN Interrupt

The intelligent I/O interrupt and CAN interrupt are assigned to software interrupt numbers 44 to 48, 52 to 54, and 57.

When using the intelligent I/O interrupt or CAN interrupt, set the IRLT bit in the IIOiE register ($i = 0$ to 4, 8 to 11) to "1" (interrupt request for interrupt used).

Various interrupt requests cause the intelligent I/O interrupt to occur. When an interrupt request is generated with each intelligent I/O or CAN functions, the corresponding bit in the IIOiR register is set to "1" (interrupt requested). When the corresponding bit in the IIOiE register is set to "1" (interrupt enabled), the IR bit in the corresponding IIOiC register is set to "1" (interrupt requested).

After the IR bit setting changes "0" to "1", the IR bit remains set to "1" when a bit in the IIOiR register is set to "1" by another interrupt request and the corresponding bit in the IIOiE register is set to "1".

Bits in the IIOiR register are not set to "0" automatically, even if an interrupt is acknowledged. Set each bit to "0" by program. If these bit settings are left "1", all generated interrupt requests are ignored.

Figure 11.13 shows a block diagram of the intelligent I/O interrupt and CAN interrupt. Figure 11.14 shows the IIOiR register. Figure 11.15 shows the IIOiE register.

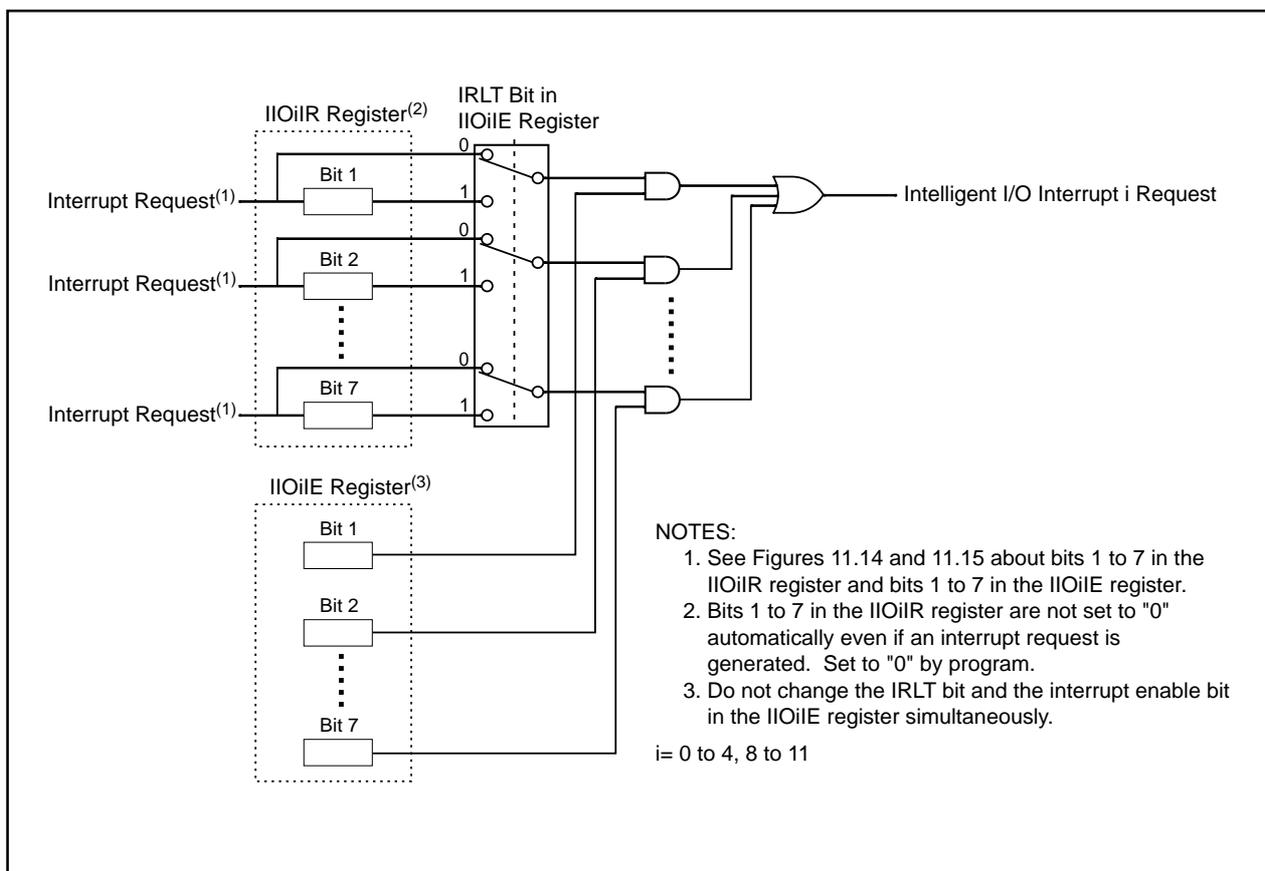


Figure 11.13 Intelligent I/O Interrupt and CAN Interrupt

The CAN0j (j=0 to 2) interrupt is provided as the CAN interrupt. The following registers are required for the CAN interrupts:

- Bits 7 in the IIO9IR to IIO11IR registers and Bits 7 in the IIO9IE to IIO11IE registers for the CAN00 to CAN02 interrupts.

The CAN0IC and CAN1IC registers share addresses with the following registers:

- The CAN0IC register shares an address with the IIO9IC register.
- The CAN1IC register shares an address with the IIO10IC register.

Refer to **23.4 CAN Interrupt** for details.

When using the intelligent I/O interrupt or CAN interrupt to activate DMAC II, set the IRLT bit in the IIOiE register to "0" (interrupt request is used for DMAC, DMAC II) to enable the interrupt request that the IIOiE register requires.

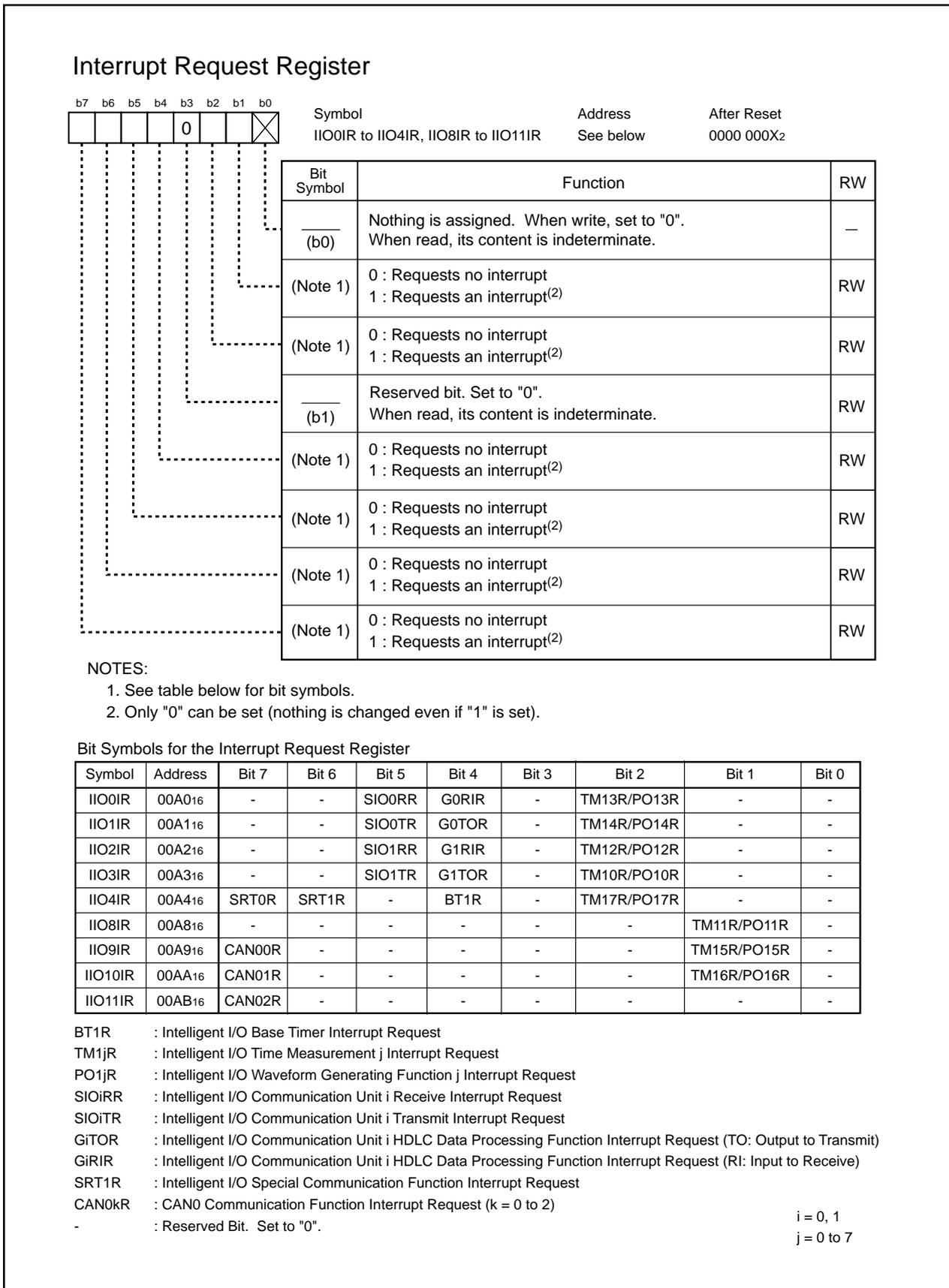


Figure 11.14 IIO0IR to IIO4IR, IIO8IR to IIO11IR Registers

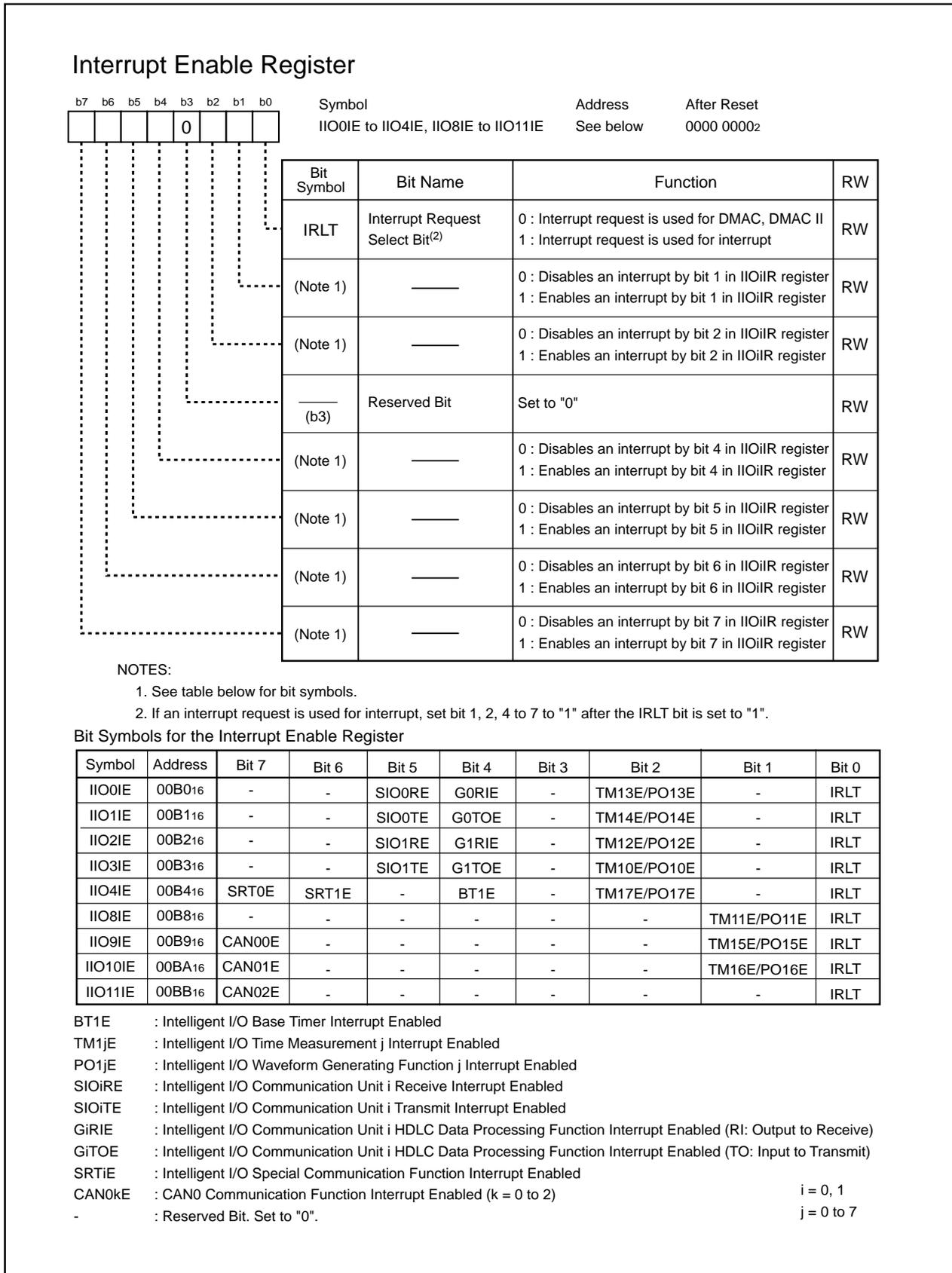


Figure 11.15 IIO0IE to IIO4IE, IIO8IE to IIO11IE Registers

12. Watchdog Timer

The watchdog timer monitors the program executions and detects defective program. It allows the microcomputer to trigger a reset or to generate an interrupt if the program error occurs. The watchdog timer contains a 15-bit counter, which is decremented by the CPU clock that the prescaler divides. The CM06 bit in the CM0 register determines whether a watchdog timer interrupt request or reset is generated if the watchdog timer underflows. The CM06 bit can only be set to "1" (reset). Once the CM06 bit is set to "1", it cannot be changed to "0" (watchdog timer interrupt) by program. The CM06 bit is set to "0" only after reset. When the main clock, on-chip oscillator clock, or PLL clock runs as the CPU clock, the WDC7 bit in the WDC register determine whether the prescaler divides the clock by 16 or by 128. When the sub clock runs as the CPU clock, the prescaler divides the clock by 2 regardless of the WDC7 bit setting. Watchdog timer cycle is calculated as follows. Marginal errors, due to the prescaler, may occur in watchdog timer cycle.

When the main clock, on-chip oscillator clock, or PLL clock is selected as the CPU clock,

$$\text{Watchdog timer cycle} = \frac{\text{Divide-by-16 or -128 prescaler} \times \text{counter value of watchdog timer (32768)}}{\text{CPU clock}}$$

When the sub clock is selected as the CPU clock,

$$\text{Watchdog timer cycle} = \frac{\text{Divide-by-2 prescaler} \times \text{counter value of watchdog timer (32768)}}{\text{CPU clock}}$$

For example, if the CPU clock frequency is 30MHz and the prescaler divides it by 16, the watchdog timer cycle is approximately 17.5 ms.

The watchdog timer is reset when the WDTS register is set and when a watchdog timer interrupt request is generated. The prescaler is reset only when the microcomputer is reset. Both watchdog timer and prescaler stop after reset. They begin counting when the WDTS register is set.

The watchdog timer and prescaler stop in stop mode, wait mode and hold state. They resume counting from the value held when the mode or state is exited.

Figure 12.1 shows a block diagram of the watchdog timer. Figure 12.2 shows registers associated with the watchdog timer.

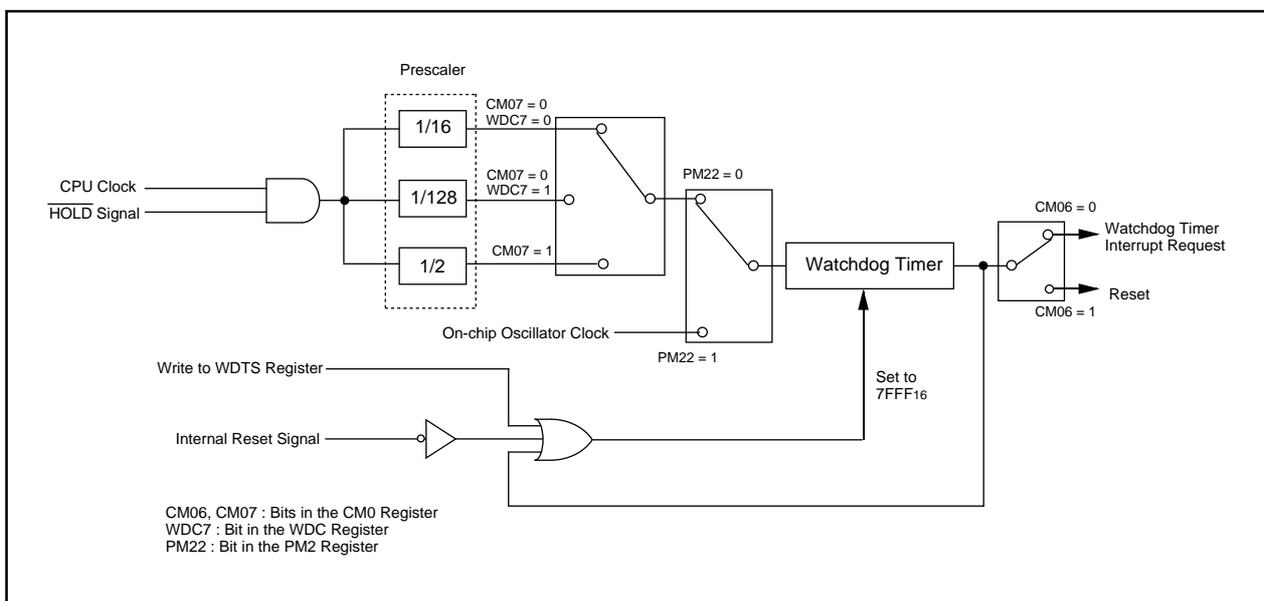


Figure 12.1 Watchdog Timer Block Diagram

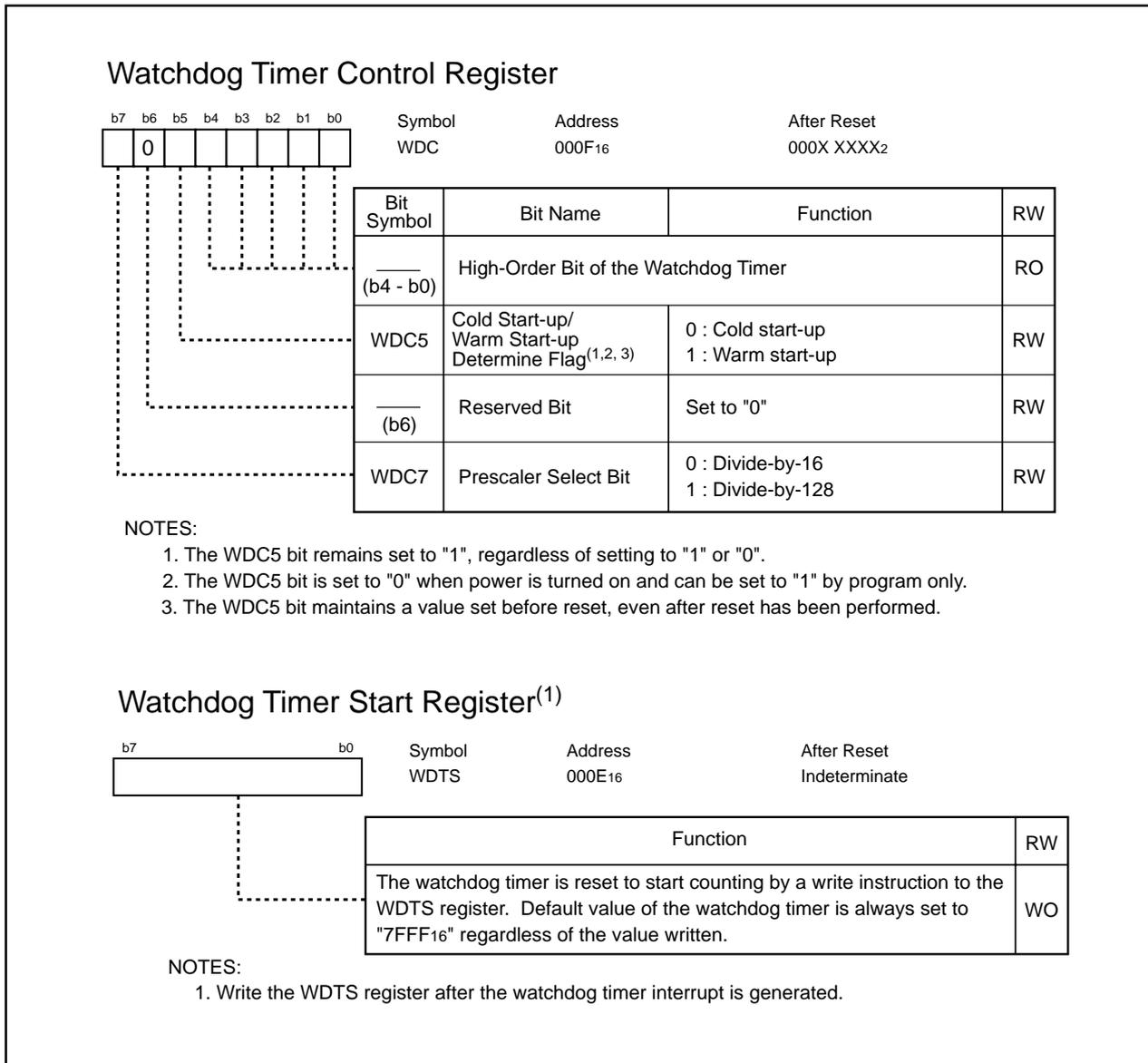


Figure 12.2 WDC Register and WDTS Register

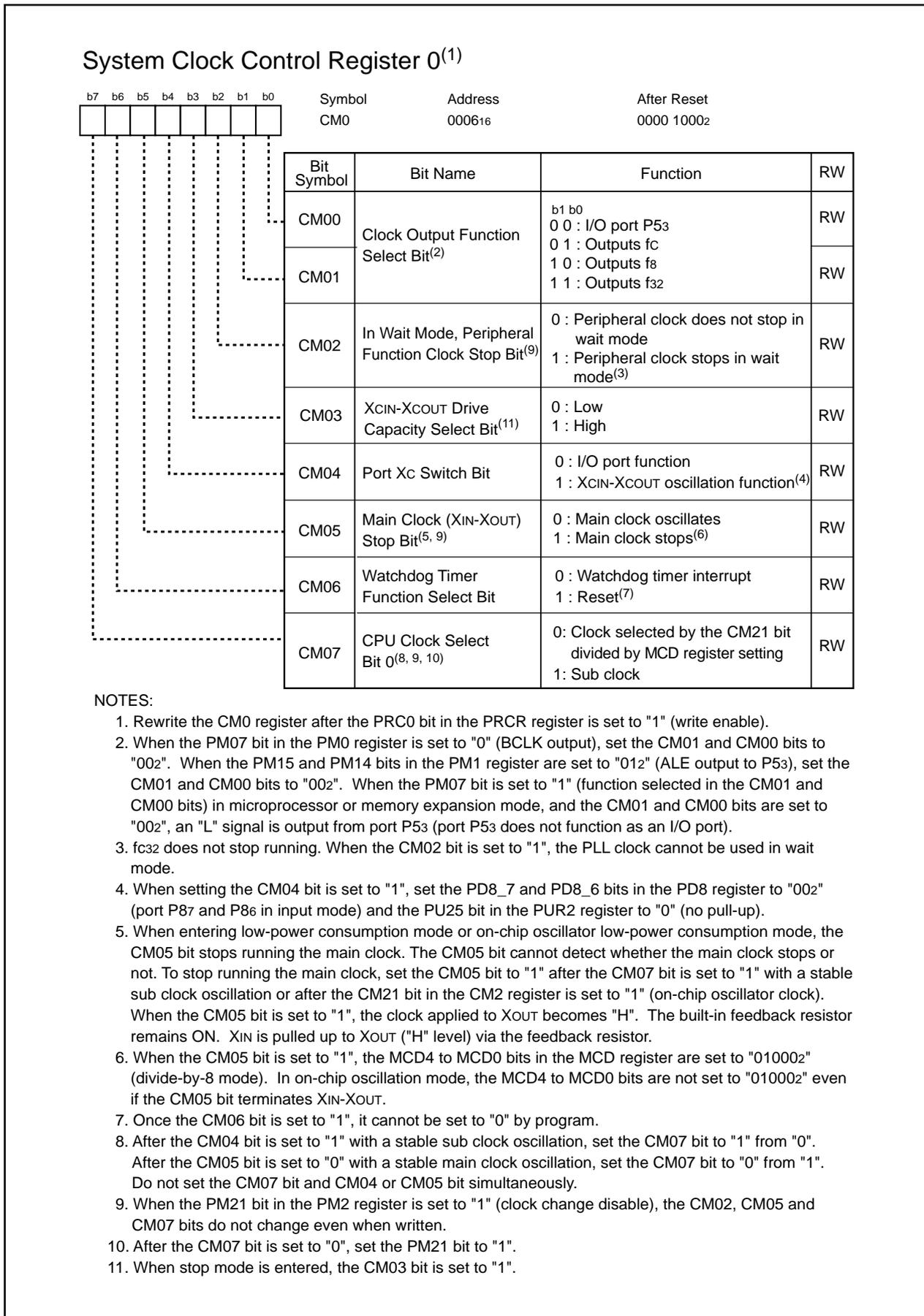


Figure 12.3 CM0 Register

12.1 Count Source Protection Mode

In count source protection mode, the on-chip oscillator clock is used as a count source for the watchdog timer. The count source protection mode allows the on-chip oscillator clock to run continuously, maintaining watchdog timer operation even if the program error occurs and the CPU clock stops running.

Follow the procedures below when using this mode.

- (1) Set the PRC0 bit in the PRCR register to "1" (write to CM0 register enabled)
- (2) Set the PRC1 bit in the PRCR register to "1" (write to PM2 register enabled)
- (3) Set the CM06 bit in the CM0 register to "1" (reset when the watchdog timer overflows)
- (4) Set the PM22 bit in the PM2 register to "1" (the on-chip oscillator clock as a count source of the watchdog timer)
- (5) Set the PRC0 bit to "0" (write to CM0 register disabled)
- (6) Set the PRC1 bit to "0" (write to PM2 register disabled)
- (7) Write to the WDTS register (the watchdog timer starts counting)

The followings will occur when the PM22 bit is set to "1".

- The on-chip oscillator starts oscillating and the on-chip oscillator clock becomes a count source for the watchdog timer.

$$\text{Watchdog timer cycle} = \frac{\text{Counter value of watchdog timer (32768)}}{\text{On-chip oscillator clock}}$$

- Write to the CM10 bit in the CM1 register is disabled. (The bit setting remains unchanged even if set it to "1". The microcomputer does not enter stop mode.)
- In wait mode or hold state, the watchdog timer continues running. However, the watchdog timer interrupt cannot be used to exit wait mode.

13. DMAC

This microcomputer contains four DMAC (direct memory access controller) channels that allow data to be sent to memory without using the CPU. DMAC transmits a 8- or 16-bit data from a source address to a destination address whenever a transmit request occurs. DMA0 and DMA1 must be prioritized if using DMAC. DMA2 and DMA3 share registers required for high-speed interrupts. High-speed interrupts cannot be used when using three or more DMAC channels.

The CPU and DMAC use the same data bus, but DMAC has a higher bus access privilege than the CPU. The cycle-steal method employed on DMAC enables high-speed operation between a transfer request and the complete transmission of 16-bit (word) or 8-bit (byte) data. Figure 13.1 shows a mapping of registers to be used for DMAC. Table 13.1 lists specifications of DMAC. Figures 13.2 to 13.5 show registers associated with DMAC.

Because the registers shown in Figure 13.1 are allocated in the CPU, use the LDC instruction to write to the registers. To set the DCT2, DCT3, DRC2, DRC3, DMA2 and DMA3 registers, set the B flag to "1" (register bank 1) and set the R0 to R3, A0 and A1 registers with the MOV instruction.

To set the DSA2 and DSA3 registers, set the B flag to "1" and set the SB and FB registers with the LDC instruction. To set the DRA2 and DRA3 registers, set the SVP and VCT registers with the LDC instruction.

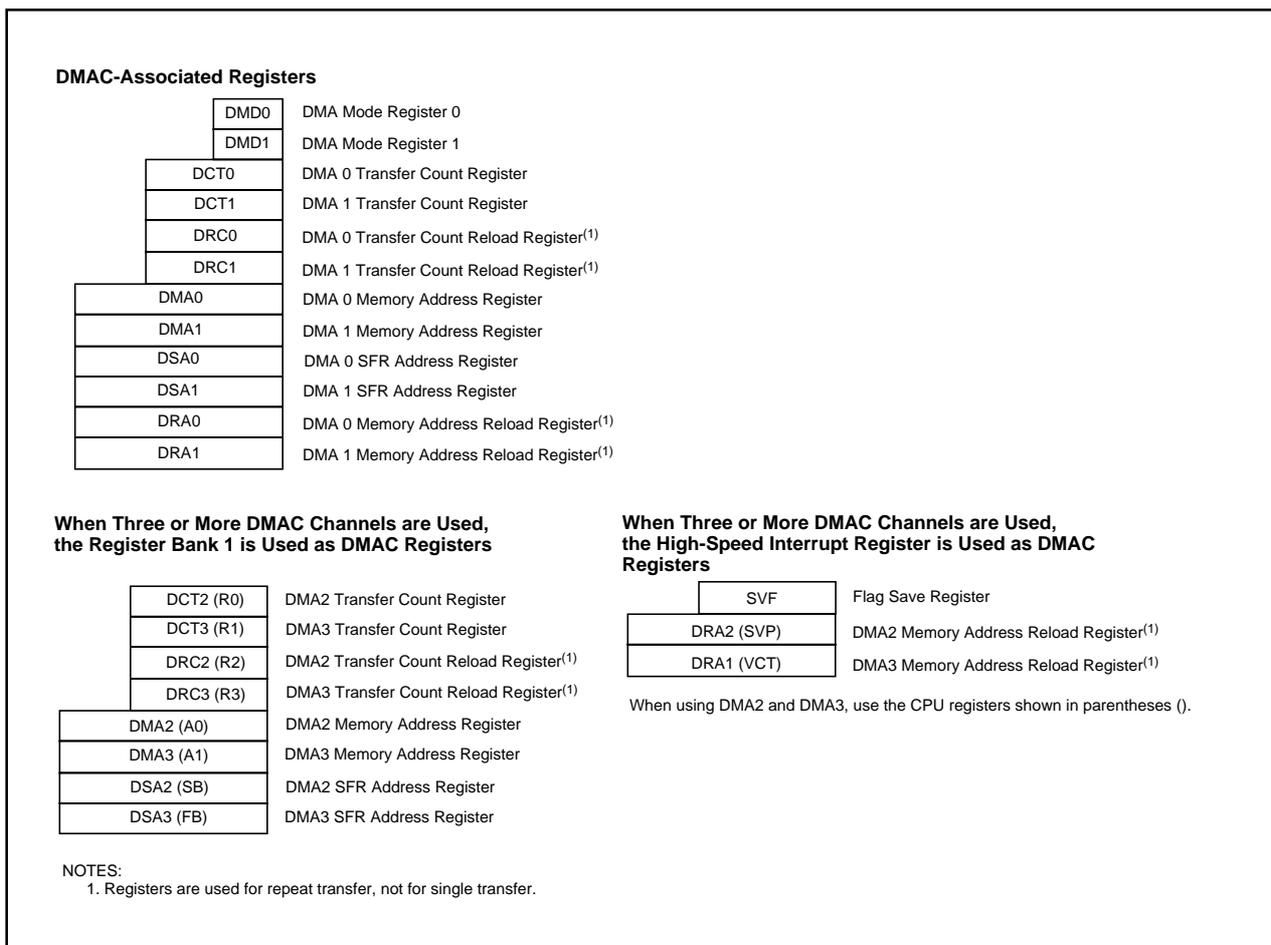


Figure 13.1 Register Mapping for DMAC

DMAC starts a data transfer by setting the DSR bit in the DMiSL register ($i=0$ to 3) or by using an interrupt request, generated by the functions determined by the DSEL 4 to DSEL0 bits in the DMiSL register, as a DMA request. Unlike interrupt requests, the I flag and interrupt control register do not affect DMA. Therefore, a DMA request can be acknowledged even if an interrupt is disabled and cannot be acknowledged. In addition, the IR bit in the interrupt control register does not change when a DMA request is acknowledged.

Table 13.1 DMAC Specifications

Item		Specification
Channels		4 channels (cycle-steal method)
Transfer Memory Space		<ul style="list-style-type: none"> From a desired address in a 16-Mbyte space to a fixed address in a 16-Mbyte space From a fixed address in a 16-Mbyte space to a desired address in a 16-Mbyte space
Maximum Bytes Transferred		128 Kbytes (when a 16-bit data is transferred) or 64 Kbytes (with an 8-bit data is transferred)
DMA Request Source ⁽¹⁾		Falling edge or both edges of signals applied to the INT0 to INT3 pins Timers A0 to A4 interrupt requests Timers B0 to B5 interrupt requests UART0 to UART4 transmit and receive interrupt requests A/D0 conversion interrupt request Intelligent I/O interrupt request CAN interrupt request Software trigger
Channel Priority		DMA0 > DMA1 > DMA2 > DMA3 (DMA0 has highest priority)
Transfer Unit		8 bits, 16 bits
Destination Address		Forward/fixed (forward and fixed directions cannot be specified when specifying source and destination addresses simultaneously)
Transfer Mode	Single Transfer	Transfer is completed when the DCTi register ($i = 0$ to 3) is set to "0000 ₁₆ "
	Repeat Transfer	When the DCTi register is set to "0000 ₁₆ ", the value of the DRCi register is reloaded into the DCTi register and the DMA transfer is continued
DMA Interrupt Request Generation Timing		When the DCTi register changes "0001 ₁₆ " to "0000 ₁₆ "
DMA Startup	Single Transfer	DMA starts when a DMA request is generated after the DCTi register is set to "0001 ₁₆ " or more and the MDi1 and MD0 bits in the DMDj register ($j = 0, 1$) are set to "012" (single transfer)
	Repeat Transfer	DMA starts when a DMA request is generated after the DCTi register is set to "0001 ₁₆ " or more and the MDi1 and MD0 bits are set to "112" (repeat transfer)
DMA Stop	Single Transfer	DMA stops when the MDi1 and MDi0 bits are set to "002" (DMA disabled) and the DCTi register is set to "0000 ₁₆ " (0 DMA transfer) by DMA transfer or write
	Repeat Transfer	DMA stops when the MDi1 and MDi0 bits are set to "002" and the DCTi register is set to "0000 ₁₆ " and the DRCi register set to "0000 ₁₆ "
Reload Timing to the DCTi or DMAi Register		When the DCTi register is set to "0000 ₁₆ " from "0001 ₁₆ " in repeat transfer mode
DMA Transfer Cycles		Minimum 3 cycles between SFR and internal RAM

NOTES:

- The IR bit in the interrupt control register does not change when a DMA request is acknowledged.

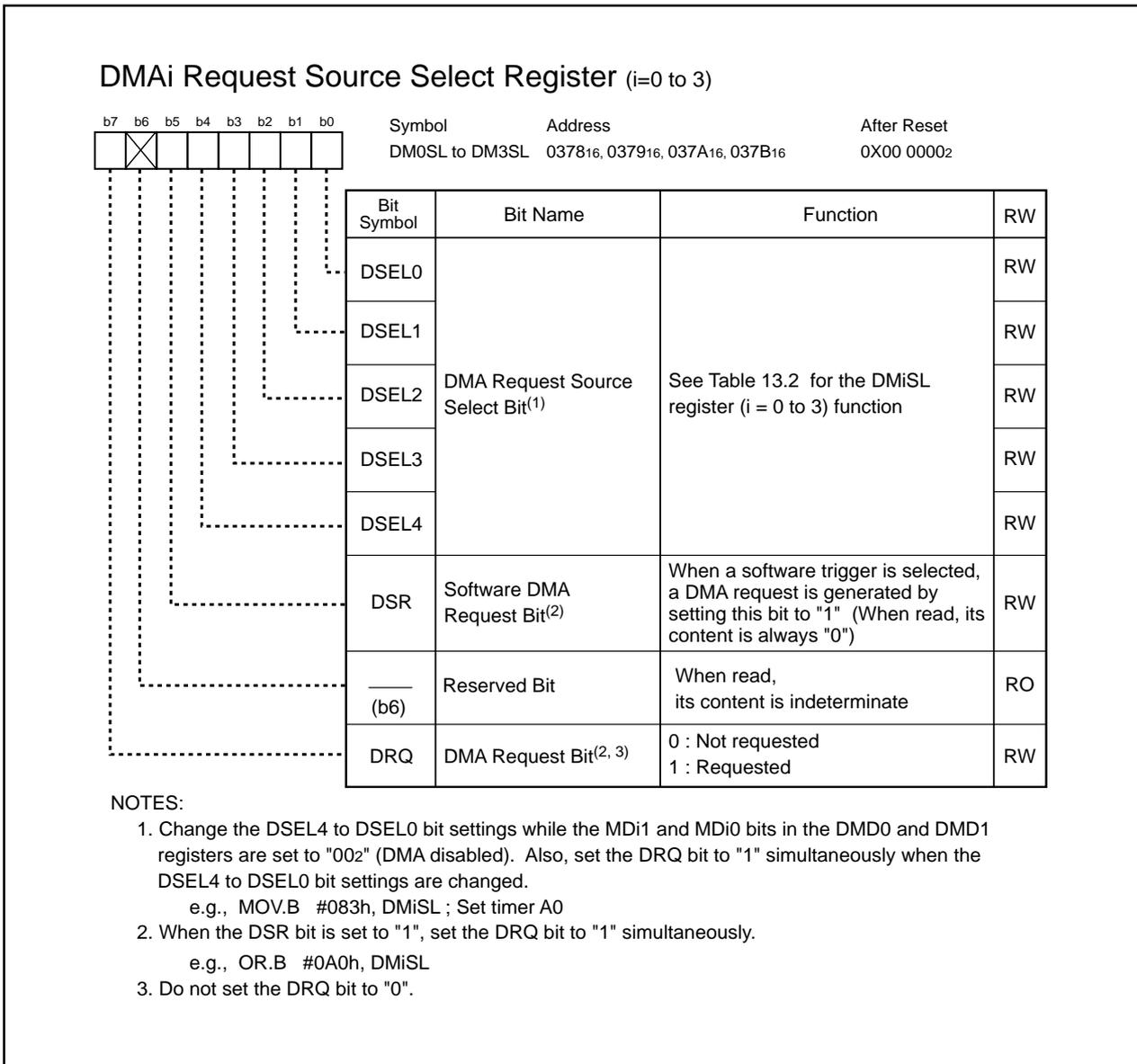


Figure 13.2 DM0SL to DM3SL Registers

Table 13.2 DMiSL Register (i = 0 to 3) Function

Setting Value	DMA Request Source			
b4 b3 b2 b1 b0	DMA0	DMA1	DMA2	DMA3
0 0 0 0 0	Software trigger			
0 0 0 0 1	Falling Edge of INT0	Falling Edge of INT1	Falling Edge of INT2	Falling Edge of INT3 ^(1,2)
0 0 0 1 0	Both Edges of INT0	Both Edges of INT1	Both Edges of INT2	Both Edges of INT3 ^(1,2)
0 0 0 1 1	Timer A0 Interrupt Request			
0 0 1 0 0	Timer A1 Interrupt Request			
0 0 1 0 1	Timer A2 Interrupt Request			
0 0 1 1 0	Timer A3 Interrupt Request			
0 0 1 1 1	Timer A4 Interrupt Request			
0 1 0 0 0	Timer B0 Interrupt Request			
0 1 0 0 1	Timer B1 Interrupt Request			
0 1 0 1 0	Timer B2 Interrupt Request			
0 1 0 1 1	Timer B3 Interrupt Request			
0 1 1 0 0	Timer B4 Interrupt Request			
0 1 1 0 1	Timer B5 Interrupt Request			
0 1 1 1 0	UART0 Transmit Interrupt Request			
0 1 1 1 1	UART0 Receive or ACK Interrupt Request ⁽³⁾			
1 0 0 0 0	UART1 Transmit Interrupt Request			
1 0 0 0 1	UART1 Receive or ACK Interrupt Request ⁽³⁾			
1 0 0 1 0	UART2 Transmit Interrupt Request			
1 0 0 1 1	UART2 Receive or ACK Interrupt Request ⁽³⁾			
1 0 1 0 0	UART3 Transmit Interrupt Request			
1 0 1 0 1	UART3 Receive or ACK Interrupt Request ⁽³⁾			
1 0 1 1 0	UART4 Transmit Interrupt Request			
1 0 1 1 1	UART4 Receive or ACK Interrupt Request ⁽³⁾			
1 1 0 0 0	A/D0 Interrupt Request			
1 1 0 0 1	Intelligent I/O Interrupt 0 Request	—	Intelligent I/O Interrupt 2 Request	Intelligent I/O Interrupt 9 Request ⁽⁴⁾
1 1 0 1 0	Intelligent I/O Interrupt 1 Request	Intelligent I/O Interrupt 8 Request	Intelligent I/O Interrupt 3 Request	Intelligent I/O Interrupt 10 Request ⁽⁵⁾
1 1 0 1 1	Intelligent I/O Interrupt 2 Request	Intelligent I/O Interrupt 9 Request ⁽⁴⁾	Intelligent I/O Interrupt 4 Request	CAN Interrupt 2 Request
1 1 1 0 0	Intelligent I/O Interrupt 3 Request	Intelligent I/O Interrupt 10 Request ⁽⁵⁾	—	Intelligent I/O Interrupt 0 Request
1 1 1 0 1	Intelligent I/O Interrupt 4 Request	CAN Interrupt 2 Request	—	Intelligent I/O Interrupt 1 Request
1 1 1 1 0	—	Intelligent I/O Interrupt 0 Request	—	Intelligent I/O Interrupt 2 Request
1 1 1 1 1	—	Intelligent I/O Interrupt 1 Request	Intelligent I/O Interrupt 8 Request	Intelligent I/O Interrupt 3 Request

NOTES:

1. If the $\overline{\text{INT3}}$ pin is used for data bus in memory expansion mode or microprocessor mode, a DMA3 interrupt request cannot be generated by a signal applied to the $\overline{\text{INT3}}$ pin.
2. The falling edge and both edges of a signal applied to the $\overline{\text{INTj}}$ pin (j=0 to 3) cause a DMA request generation. The $\overline{\text{INT}}$ interrupt (the POL bit in the INTjIC register, the LVS bit, the IFSR register) is not affected and vice versa.
3. Use the UkSMR register and UkSMR2 register (k=0 to 4) to switch between the UARTk receive and the ACK interrupt as a DMA request source.
To use the ACK interrupt for a DMA request, set the IICM bit in the UkSMR register to "1" and the IICM2 bit in the UkSMR2 register to "0".
4. The same setting is used to generate an intelligent I/O interrupt 9 request and a CAN interrupt 0 request.
5. The same setting is used to generate an intelligent I/O interrupt 10 request and a CAN interrupt 1 request.

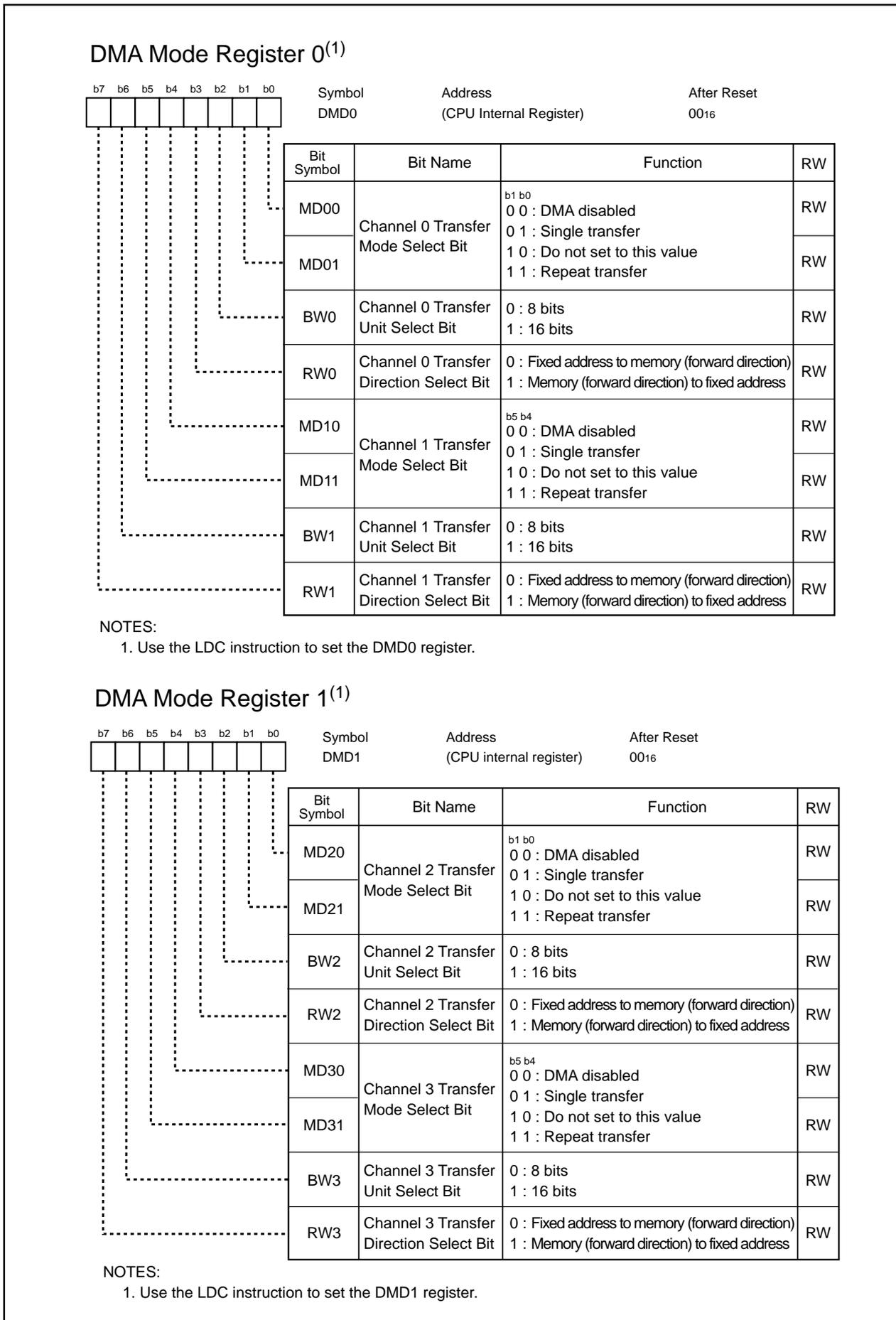


Figure 13.3 DMD0 and DMD1 Registers

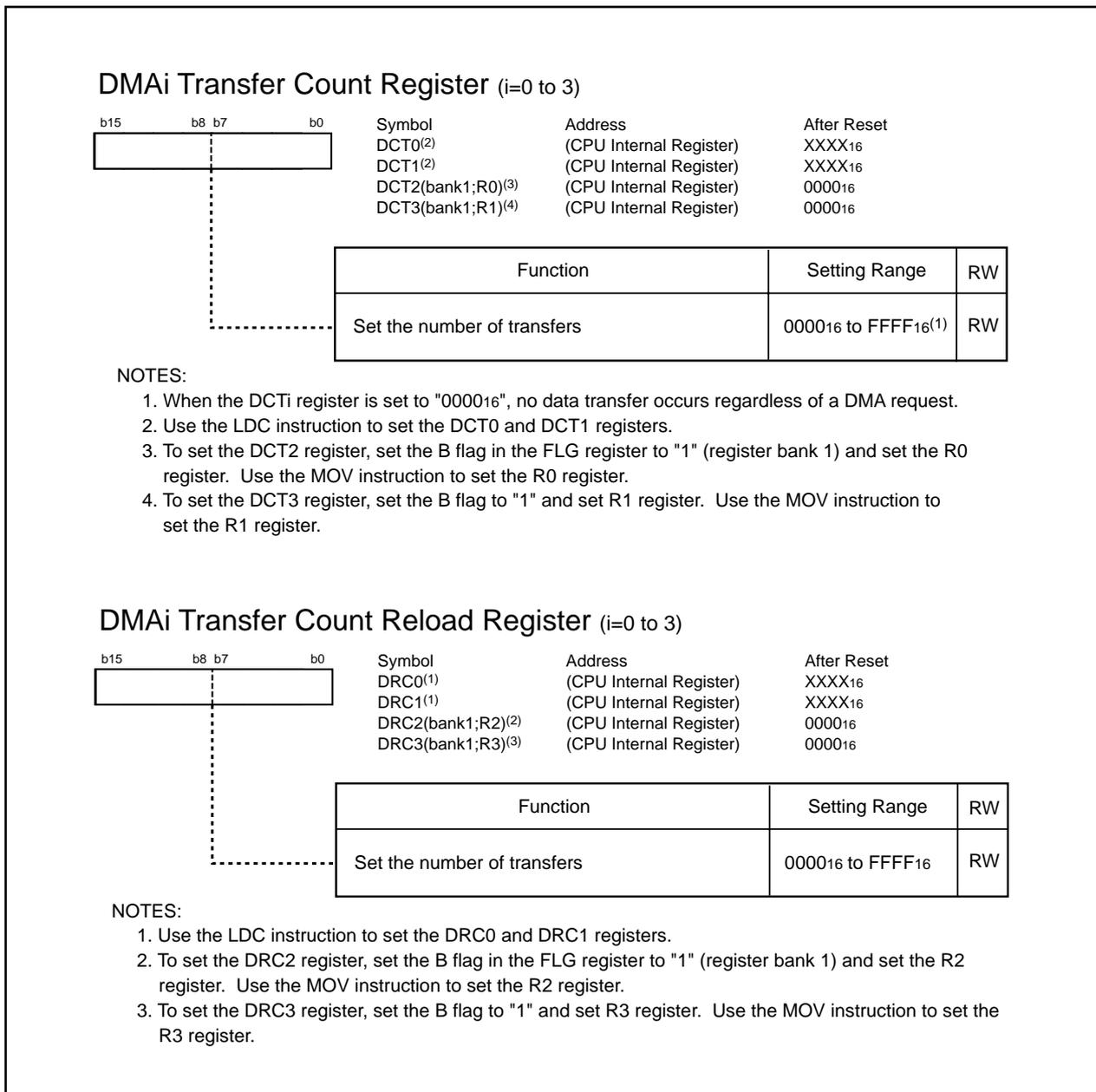


Figure 13.4 DCT0 to DCT3 Registers and DRC0 to DRC3 Registers

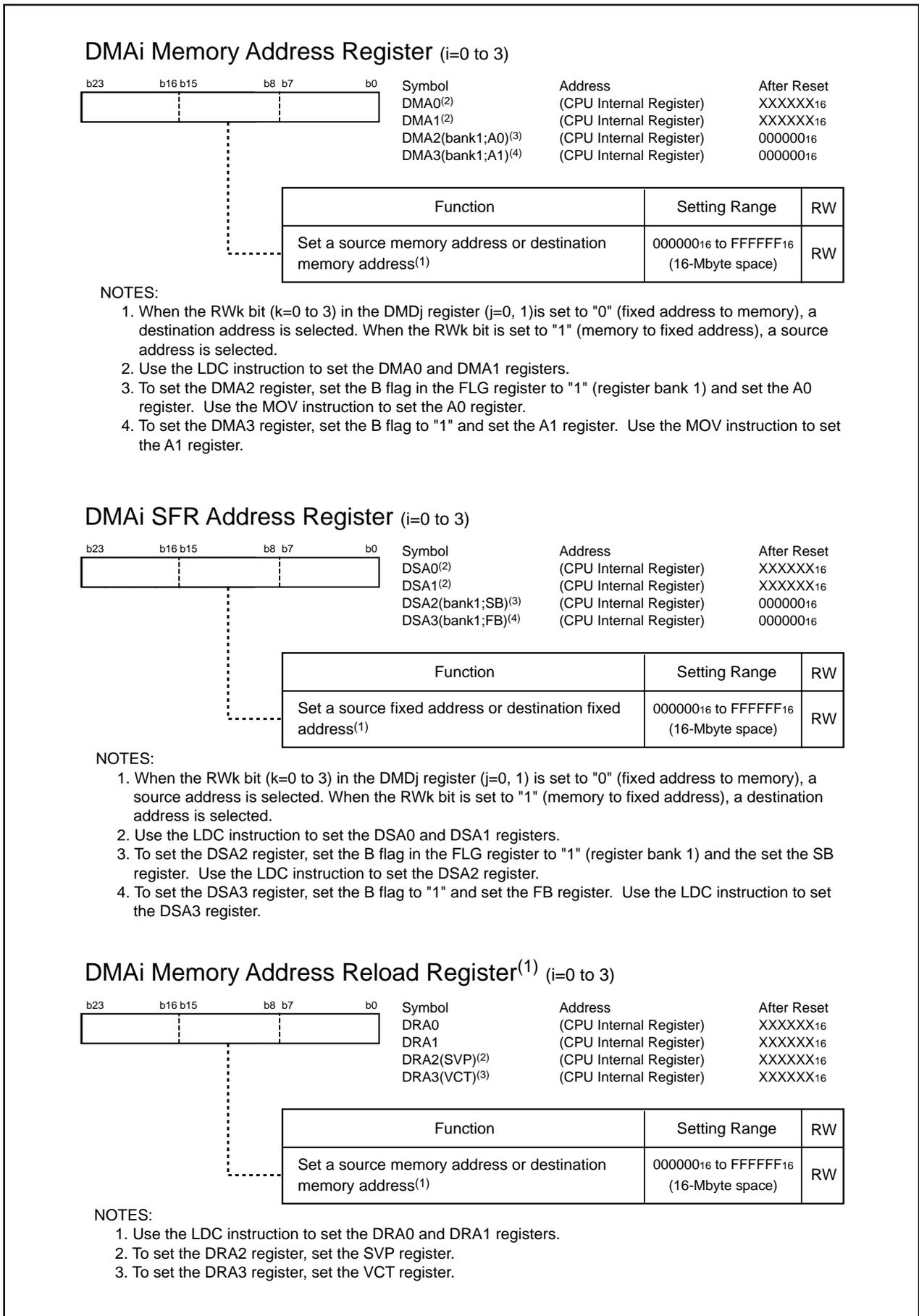


Figure 13.5 DMA0 to DMA3 Registers, DSA0 to DSA3 Registers and DRA0 to DRA3 Registers

13.1 Transfer Cycle

Transfer cycle contains a bus cycle to read data from a memory or the SFR area (source read) and a bus cycle to write data to a memory space or the SFR area (destination write). The number of read and write bus cycles depends on source and destination addresses. In memory expansion mode and microprocessor mode, the number of read and write bus cycles also depends on DS register setting. Software wait state insertion and the $\overline{\text{RDY}}$ signal make a bus cycle longer.

13.1.1 Effect of Source and Destination Addresses

When a 16-bit data is transferred with a 16-bit data bus and a source address starting with an odd address, source read cycle is incremented by one bus cycle, compared to a source address starting with an even address.

When a 16-bit data is transferred with a 16-bit data bus and a destination address starting with an odd address, a destination write cycle is incremented by one bus cycle, compared to a destination address starting with an even address.

13.1.2 Effect of the DS Register

In an external space in memory expansion or microprocessor mode, transfer cycle varies depending on the data bus used at the source and destination addresses. See **Figure 8.1** for details about the DS register.

- When an 8-bit data bus (the DS_i bit in the DS register is set to "0" (i=0 to 3)), accessing both source address and destination address, is used to transfer a 16-bit data, 8-bit data is transferred twice. Therefore, two bus cycles are required to read the data and another two bus cycles to write the data.
- When an 8-bit data bus (the DS_i bit in the DS register is set to "0" (i=0 to 3)), accessing source address, and a 16-bit data bus, accessing destination address, are used to transfer a 16-bit data, 8-bit data is read twice but is written once as 16-bit data. Therefore, two bus cycles are required for reading and one bus cycle is for writing.
- When a 16-bit data bus, accessing source address, and an 8-bit data bus, accessing destination address, are used to transfer a 16-bit data, 16-bit data is read once and 8-bit data is written twice. Therefore, one bus cycle is required for reading and two bus cycles is for writing.

13.1.3 Effect of Software Wait State

When the SFR area or memory space with software wait states is accessed, the number of CPU clock cycles is incremented by software wait states.

Figure 13.6 shows an example of a transfer cycle for the source-read bus cycle. In Figure 13.6, the number of source-read bus cycles is illustrated under different conditions, provided that the destination address is an address of an external space with the destination-write cycle as two CPU clock cycles (=one bus cycle). In effect, the destination-write bus cycle is also affected by each condition and the transfer cycles change accordingly. To calculate a transfer cycle, apply respective conditions to both destination-write bus cycle and source-read bus cycle. As shown in example (2) of Figure 13.6, when an 8-bit data bus, accessing both source and destination addresses, is used to transfer a 16-bit data, two bus cycles each are required for the source-read bus cycle and destination-write bus cycle.

13.1.4 Effect of $\overline{\text{RDY}}$ Signal

In memory expansion or microprocessor mode, the $\overline{\text{RDY}}$ signal affects a bus cycle if a source address or destination address is allocated address in an external space. Refer to **8.2.6 RDY Signal** for details.

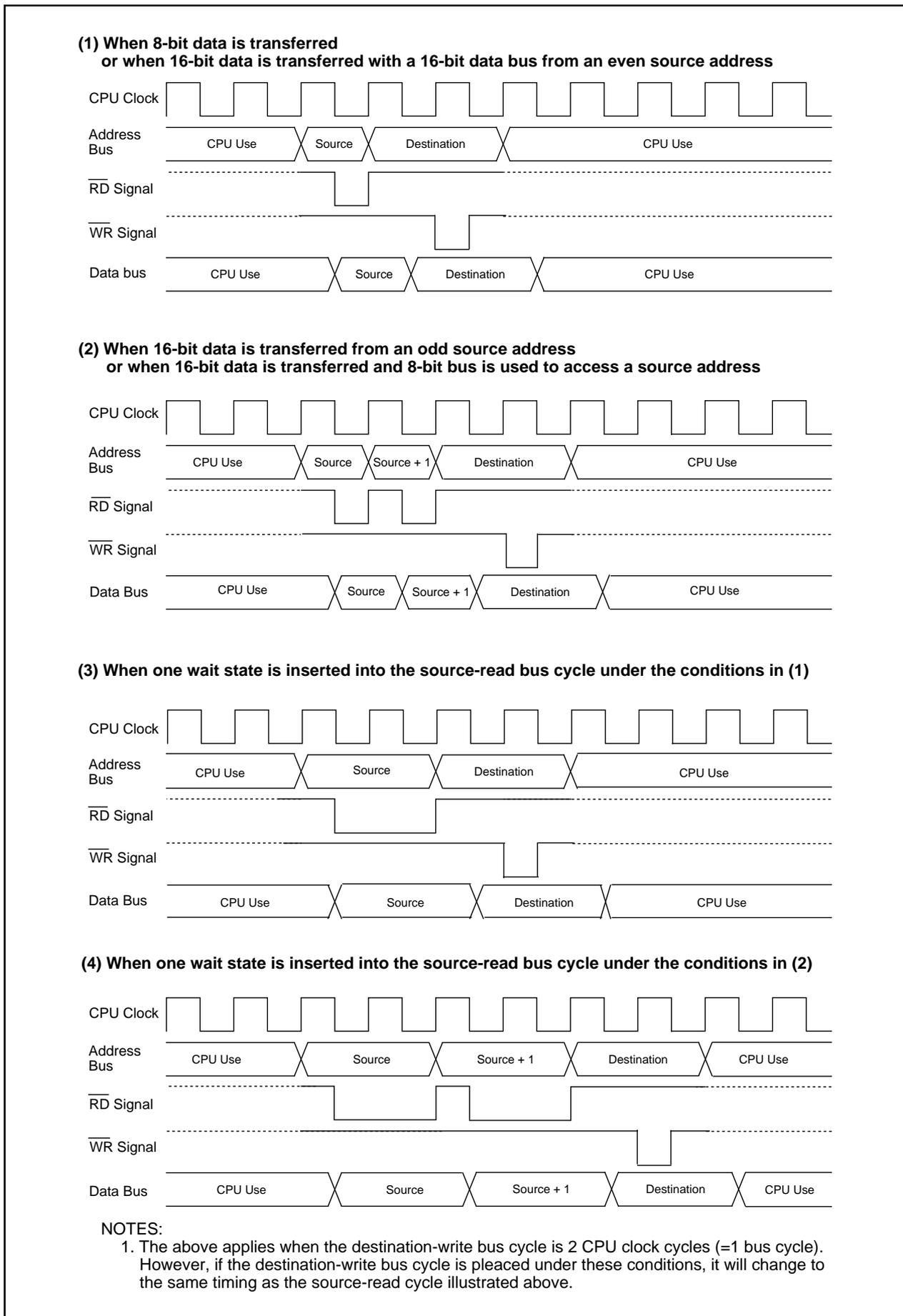


Figure 13.6 Transfer Cycle Examples with the Source-Read Bus Cycle

13.2 DMAC Transfer Cycle

The number of DMAC transfer cycle can be calculated as follows.

Any combination of even or odd transfer read and write addresses are possible. Table 13.3 lists the number of DMAC transfer cycles. Table 13.4 lists coefficient j, k.

$$\text{Transfer cycles per transfer} = \text{Number of read cycle} \times j + \text{Number of write cycle} \times k$$

Table 13.3 DMAC Transfer Cycles

Transfer Unit	Bus Width	Access Address	Single-Chip Mode		Memory Expansion Mode Microprocessor Mode	
			Read Cycle	Write Cycle	Read Cycle	Write Cycle
8-bit transfers (BWi bit in the DMDp register = 0)	16-bit	Even	1	1	1	1
		Odd	1	1	1	1
	8-bit	Even	—	—	1	1
		Odd	—	—	1	1
16-bit transfers (BWi bit = 1)	16-bit	Even	1	1	1	1
		Odd	2	2	2	2
	8-bit	Even	—	—	2	2
		Odd	—	—	2	2

i = 0 to 3, p = 0 to 1

Table 13.4 Coefficient j, k

Internal Space			External Space
Internal ROM or internal RAM	Internal ROM or internal RAM	SFR area	j and k BCLK cycles shown in Table 8.5. Add one cycle to j or k cycles when inserting a recovery cycle.
with no wait state j=1 k=1	with a wait state j=2 k=2	j=2 k=2	

j, k=2 to 9

13.3 Channel Priority and DMA Transfer Timing

When multiple DMA requests are generated in the same sampling period, between the falling edge of the CPU clock and the next falling edge, the DRQ bit in the DMiSL register (i = 0 to 3) is set to "1" (requested) simultaneously. Channel priority in this case is : DMA0 > DMA1 > DMA2 > DMA3.

Figure 13.7 shows an example of the DMA transfer by external source.

In Figure 13.7, the DMA0 request having highest priority is received first to start a transfer when a DMA0 request and DMA1 request are generated simultaneously. After one DMA0 transfer is completed, the bus privilege is returned to the CPU. When the CPU has completed one bus access, the DMA1 transfer starts. After one DMA1 transfer is completed, the privilege is again returned to the CPU.

In addition, DMA requests cannot be counted up since each channel has one DRQ bit. Therefore, when DMA requests, as DMA1 in Figure 13.7, occur more than once before receiving bus privilege, the DRQ bit is set to "0" as soon as privilege is acquired. The bus privilege is returned to the CPU when one transfer is completed.

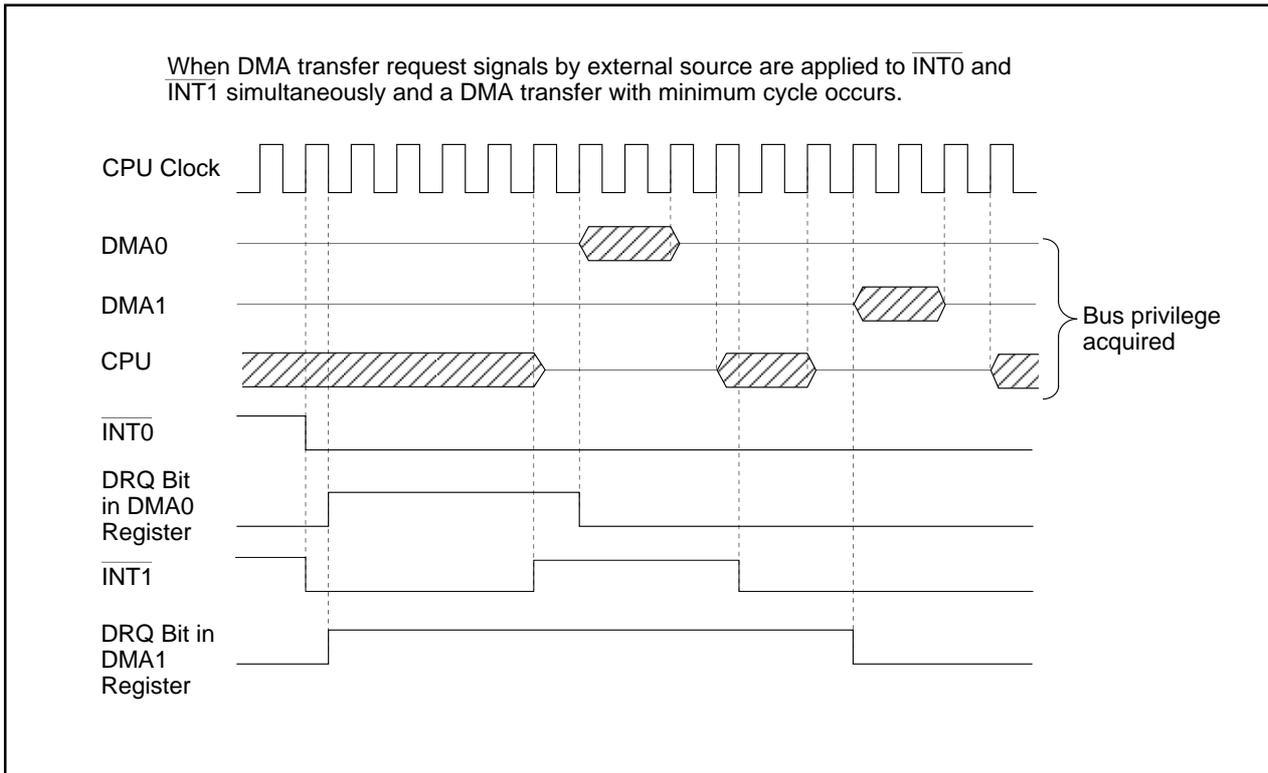


Figure 13.7 DMA Transfer by External Source

14. DMAC II

DMAC II performs memory-to-memory transfer, immediate data transfer and calculation transfer, which transfers the sum of two data added by an interrupt request from any peripheral functions.

Table 14.1 lists specifications of DMAC II.

Table 14.1 DMAC II Specifications

Item	Specification
DMAC II Request Source	Interrupt requests generated by all peripheral functions when the ILVL2 to ILVL0 bits are set to "1112"
Transfer Data	<ul style="list-style-type: none"> • Data in memory is transferred to memory (memory-to-memory transfer) • Immediate data is transferred to memory (immediate data transfer) • Data in memory (or immediate data) + data in memory are transferred to memory (calculation transfer)
Transfer Block	8 bits or 16 bits
Transfer Space	64-Kbyte space in addresses 00000 ₁₆ to 0FFFF ₁₆ ^(1, 2)
Transfer Direction	Fixed or forward address Selected separately for each source address and destination address
Transfer Mode	Single transfer, burst transfer
Chained Transfer Function	Parameters (transfer count, transfer address and other information) are switched when transfer counter reaches zero
End-of-Transfer Interrupt	Interrupt occurs when a transfer counter reaches zero
Multiple Transfer Function	Multiple data can be transferred by a generated request for one DMAC II transfer

NOTES:

1. When transferring a 16-bit data to destination address 0FFFF₁₆, it is transferred to 0FFFF₁₆ and 10000₁₆. The same transfer occurs when the source address is 0FFFF₁₆.
2. The actual space where transfer can occur is limited due to internal RAM capacity.

14.1 DMAC II Settings

DMAC II can be made available by setting up the following registers and tables.

- RLVL register
 - DMAC II Index
 - Interrupt control register of the peripheral function causing a DMAC II request
 - The relocatable vector table of the peripheral function causing a DMAC II request
 - IRLT bit in the IIOiE register (i = 0 to 4, 8 to 11) if using the intelligent I/O or CAN interrupt
- Refer to **11. Interrupts** for details on the IIOiE register.

14.1.1 RLVL Register

When the DMAII bit is set to "1" (DMAC II transfer) and the FSIT bit to "0" (normal interrupt), DMAC II is activated by an interrupt request from any peripheral function with the ILVL2 to ILVL0 bits in the interrupt control register set to "1112" (level 7).

Figure 14.1 shows the RLVL register.

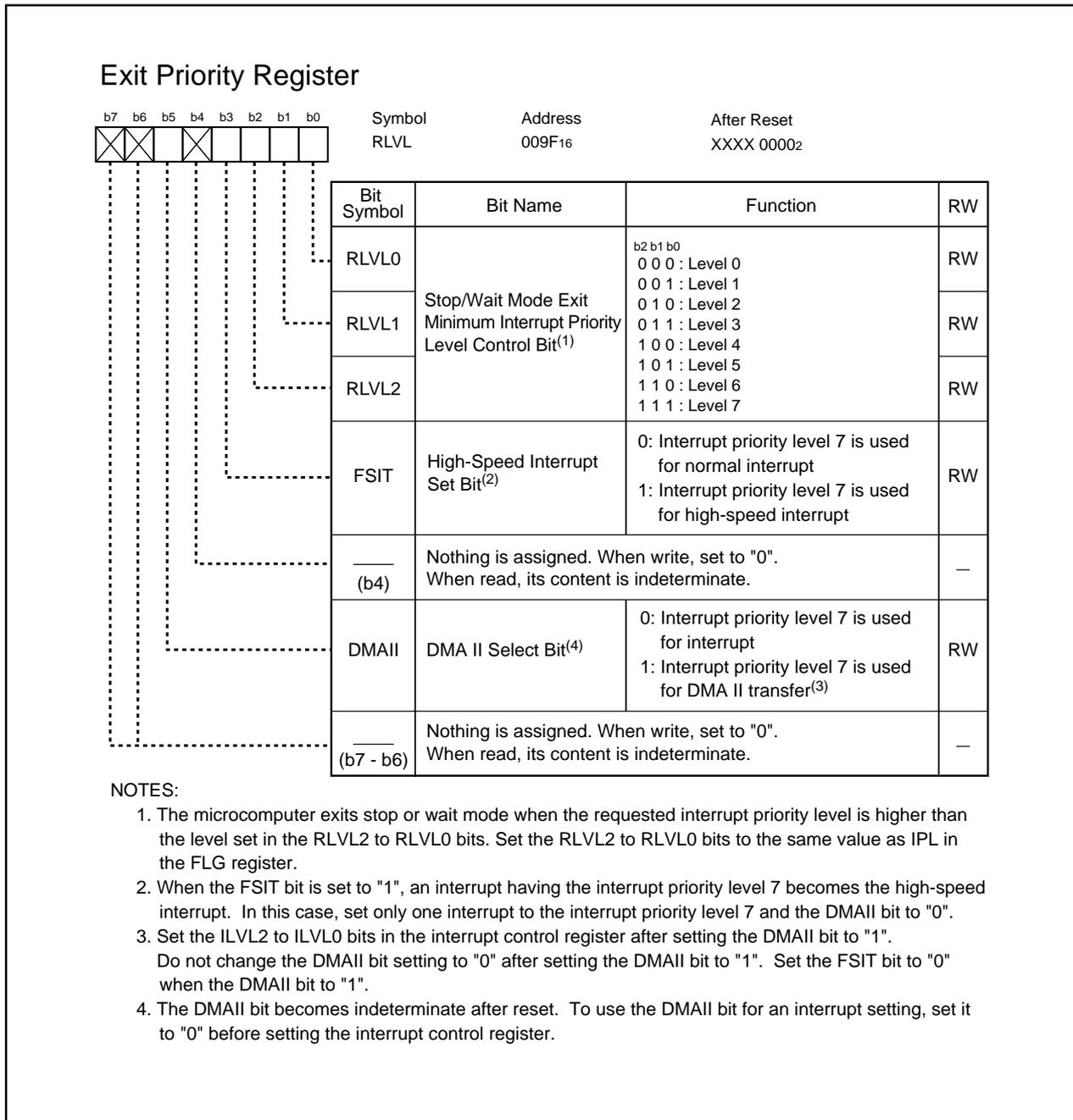


Figure 14.1 RLVL Register

14.1.2 DMAC II Index

The DMAC II index is a data table which comprises 8 to 18 bytes (maximum 32 bytes when the multiple transfer function is selected). The DMAC II index stores parameters for transfer mode, transfer counter, source address (or immediate data), operation address as an address to be calculated, destination address, chained transfer address, and end-of-transfer interrupt address.

This DMAC II index must be located on the RAM area.

Figure 14.2 shows a configuration of the DMAC II index. Table 14.2 lists a configuration of the DMAC II index in transfer mode.

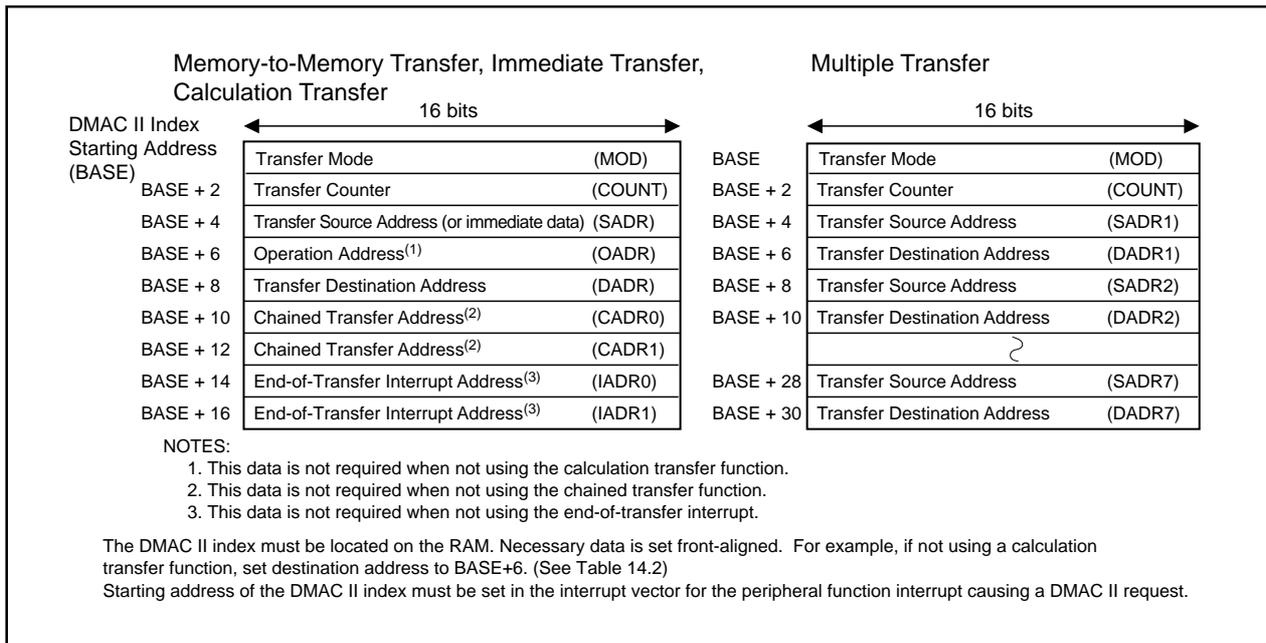


Figure 14.2 DMAC II Index

The followings are details of the DMAC II index. Set these parameters in the specified order listed in Table 14.2, according to DMAC II transfer mode.

- **Transfer mode (MOD)**

Two-byte data is required to set transfer mode. Figure 14.3 shows a configuration for transfer mode.

- **Transfer counter (COUNT)**

Two-byte data is required to set the number of transfer.

- **Transfer source address (SADR)**

Two-byte data is required to set the source memory address or immediate data.

- **Operation address (OADR)**

Two-byte data is required to set a memory address to be calculated. Set this data only when using the calculation transfer function.

- **Transfer destination address (DADR)**

Two-byte data is required to set the destination memory address.

- **Chained transfer address (CADR)**

Four-byte data is required to set the starting address of the DMAC II index for the next transfer. Set this data only when using the chained transfer function.

- **End-of-transfer interrupt address (IADR)**

Four-byte data is required to set a jump address for end-of-transfer interrupt processing. Set this data only when using the end-of-transfer interrupt.

Table 14.2 DMAC II Index Configuration in Transfer Mode

Transfer Data	Memory-to-Memory Transfer /Immediate Data Transfer				Calculation Transfer				Multiple Transfer																																																													
	Not Used	Used	Not Used	Used	Not Used	Used	Not Used	Used																																																														
Chained Transfer	Not Used	Used	Not Used	Used	Not Used	Used	Not Used	Used	Not Available																																																													
End-of-Transfer Interrupt	Not Used	Not Used	Used	Used	Not Used	Not Used	Used	Used	Not Available																																																													
DMAC II Index	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>DADR</td></tr> </table> <p>8 bytes</p>	MOD	COUNT	SADR	DADR	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>DADR</td></tr> <tr><td>CADR0</td></tr> <tr><td>CADR1</td></tr> </table> <p>12 bytes</p>	MOD	COUNT	SADR	DADR	CADR0	CADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>DADR</td></tr> <tr><td>IADR0</td></tr> <tr><td>IADR1</td></tr> </table> <p>12 bytes</p>	MOD	COUNT	SADR	DADR	IADR0	IADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>DADR</td></tr> <tr><td>CADR0</td></tr> <tr><td>CADR1</td></tr> <tr><td>IADR0</td></tr> <tr><td>IADR1</td></tr> </table> <p>16 bytes</p>	MOD	COUNT	SADR	DADR	CADR0	CADR1	IADR0	IADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>OADR</td></tr> <tr><td>DADR</td></tr> </table> <p>10 bytes</p>	MOD	COUNT	SADR	OADR	DADR	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>OADR</td></tr> <tr><td>DADR</td></tr> <tr><td>CADR0</td></tr> <tr><td>CADR1</td></tr> </table> <p>14 bytes</p>	MOD	COUNT	SADR	OADR	DADR	CADR0	CADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>OADR</td></tr> <tr><td>DADR</td></tr> <tr><td>IADR0</td></tr> <tr><td>IADR1</td></tr> </table> <p>14 bytes</p>	MOD	COUNT	SADR	OADR	DADR	IADR0	IADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR</td></tr> <tr><td>DADR</td></tr> <tr><td>OADR</td></tr> <tr><td>DADR</td></tr> <tr><td>CADR0</td></tr> <tr><td>CADR1</td></tr> <tr><td>IADR0</td></tr> <tr><td>IADR1</td></tr> </table> <p>18 bytes</p>	MOD	COUNT	SADR	DADR	OADR	DADR	CADR0	CADR1	IADR0	IADR1	<table border="1"> <tr><td>MOD</td></tr> <tr><td>COUNT</td></tr> <tr><td>SADR1</td></tr> <tr><td>DADR1</td></tr> <tr><td> </td></tr> <tr><td> </td></tr> <tr><td>SADRi</td></tr> <tr><td>DADRi</td></tr> </table> <p>i=1 to 7 max. 32 bytes (when i=7)</p>	MOD	COUNT	SADR1	DADR1			SADRi	DADRi
	MOD																																																																					
COUNT																																																																						
SADR																																																																						
DADR																																																																						
MOD																																																																						
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CADR0																																																																						
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DADRi																																																																						

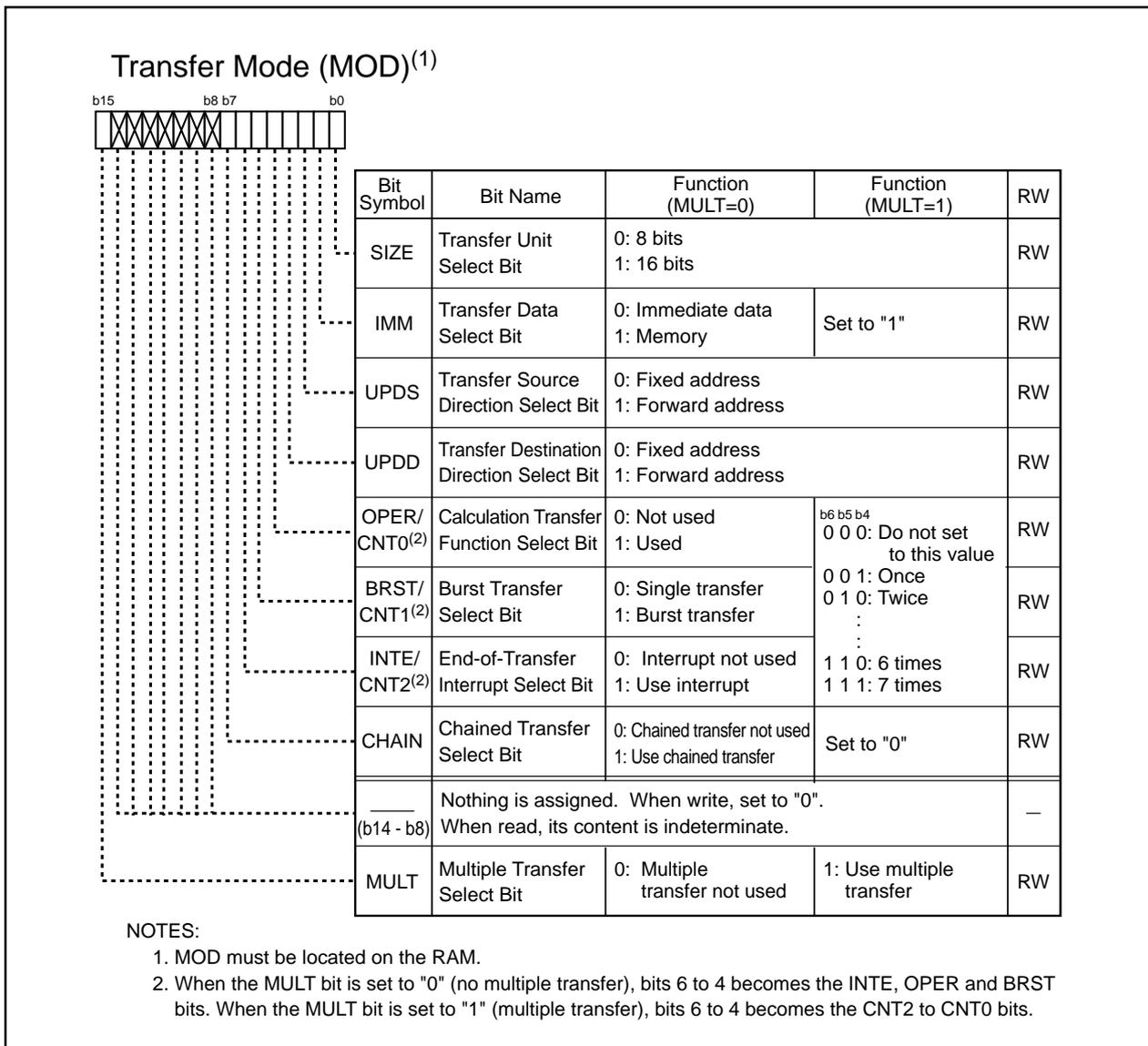


Figure 14.3 MOD

14.1.3 Interrupt Control Register for the Peripheral Function

For the peripheral function interrupt activating DMAC II, set the ILVL2 to ILVL0 bits to "1112" (level 7).

14.1.4 Relocatable Vector Table for the Peripheral Function

Set the starting address of the DMAC II index in the interrupt vector for the peripheral function interrupt activating DMAC II.

When using the chained transfer, the relocatable vector table must be located in the RAM.

14.1.5 IRLT Bit in the IIOiE Register (i=0 to 4, 8 to 11)

When the intelligent I/O interrupt or CAN interrupt is used to activate DMAC II, set the IRLT bit in the IIOiE register of the interrupt to "0".

14.2 DMAC II Performance

Function to activate DMAC II is selected by setting the DMA II bit to "1" (DMAC II transfer). DMAC II is activated by all peripheral function interrupts with the ILVL2 to ILVL0 bits set to "1112" (level 7). These peripheral function interrupt request signals become DMAC II transfer request signals and the peripheral function interrupt cannot be used.

When an interrupt request is generated by setting the ILVL2 to ILVL0 bits to "1112" (level 7), DMAC II is activated regardless of what state the I flag and IPL are in.

14.3 Transfer Data

DMAC II transfers 8-bit or 16-bit data.

- Memory-to-memory transfer : Data is transferred from a desired memory location in a 64-Kbyte space (Addresses 00000_{16} to $0FFFF_{16}$) to another desired memory location in the same space.
- Immediate data transfer : Immediate data is transferred to a desired memory location in a 64-Kbyte space.
- Calculation transfer : Two 8-bit or 16-bit data are added together and the result is transferred to a desired memory location in a 64-Kbyte space.

When a 16-bit data is transferred to the destination address $0FFFF_{16}$, it is transferred to $0FFFF_{16}$ and 10000_{16} . The same transfer occurs when the source address is $0FFFF_{16}$. Actual transferable space varies depending on the internal RAM capacity.

14.3.1 Memory-to-memory Transfer

Data transfer between any two memory locations can be:

- a transfer from a fixed address to another fixed address
- a transfer from a fixed address to a relocatable address
- a transfer from a relocatable address to a fixed address
- a transfer from a relocatable address to another relocatable address

When a relocatable address is selected, the address is incremented, after a transfer, for the next transfer. In a 8-bit transfer, the transfer address is incremented by one. In a 16-bit transfer, the transfer address is incremented by two.

When a source or destination address exceeds address $0FFFF_{16}$ as a result of address incrementation, the source or destination address returns to address 00000_{16} and continues incrementation. Maintain source and destination address at address $0FFFF_{16}$ or below.

14.3.2 Immediate Data Transfer

DMAC II transfers immediate data to any memory location. A fixed or relocatable address can be selected as the destination address. Store the immediate data into SADR. To transfer an 8-bit immediate data, write the data in the low-order byte of SADR (high-order byte is ignored).

14.3.3 Calculation Transfer

After two memory data or an immediate data and memory data are added together, DMAC II transfers calculated result to any memory location. SADR must have one memory location address to be calculated or immediate data and OADR must have the other memory location address to be calculated. Fixed or relocatable address can be selected as source and destination addresses when using a memory + memory calculation transfer. If the transfer source address is relocatable, the operation address also becomes relocatable. Fixed or relocatable address can be selected as the transfer destination address when using an immediate data + memory calculation transfer.

14.4 Transfer Modes

Single and burst transfers are available. The BRST bit in MOD selects transfer method, either single transfer or burst transfer. COUNT determines how many transfers occur. No transfer occurs when COUNT is set to "0000₁₆".

14.4.1 Single Transfer

For every transfer request source, DMAC II transfers one transfer unit of 8-bit or 16-bit data once. When the source or destination address is relocatable, the address is incremented, after a transfer, for the next transfer.

COUNT is decremented every time a transfer occurs. When using the end-of-transfer interrupt, the interrupt is acknowledged when COUNT reaches "0".

14.4.2 Burst Transfer

For every transfer request source, DMAC II continuously transfers data the number of times determined by COUNT. COUNT is decremented every time a transfer occurs. The burst transfer ends when COUNT reaches "0". The end-of-transfer interrupt is acknowledged when the burst transfer ends if using the end-of-transfer interrupt. All interrupts are ignored while the burst transfer is in progress.

14.5 Multiple Transfer

The MULT bit in MOD selects the multiple transfer. When using the multiple transfer, select the memory-to-memory transfer. One transfer request source initiates multiple transfers. The CNT2 to CNT0 bits in MOD selects the number of transfers from "001₂" (once) to "111₂" (7 times). Do not set the CNT2 to CNT0 bits to "000₂".

The transfer source and destination addresses for each transfer must be allocated alternately in addresses following MOD and COUNT. When the multiple transfer is selected, the calculation transfer, burst transfer, end-of-transfer interrupt and chained transfer cannot be used.

14.6 Chained Transfer

The CHAIN bit in MOD selects the chained transfer.

The following process initiates the chained transfer.

- (1) Transfer, caused by a transfer request source, occurs according to the content of the DMAC II index. The vectors of the request source indicates where the DMAC II index is allocated. For each request, the BRST bit selects either single or burst transfer.
- (2) When COUNT reaches "0", the contents of CADR1 and CADR0 are written to the vector of the request source. When the INTE bit in MOD is set to "1", the end-of-transfer interrupt is generated simultaneously.
- (3) When the next DMAC II transfer request is generated, transfer occurs according to the contents of the DMAC II index indicated by the peripheral function interrupt vector rewritten in (2).

Figure 14.4 shows the relocatable vector and DMACII index when the chained transfer is in progress. For the chained transfer, the relocatable vector table must be located in the RAM.

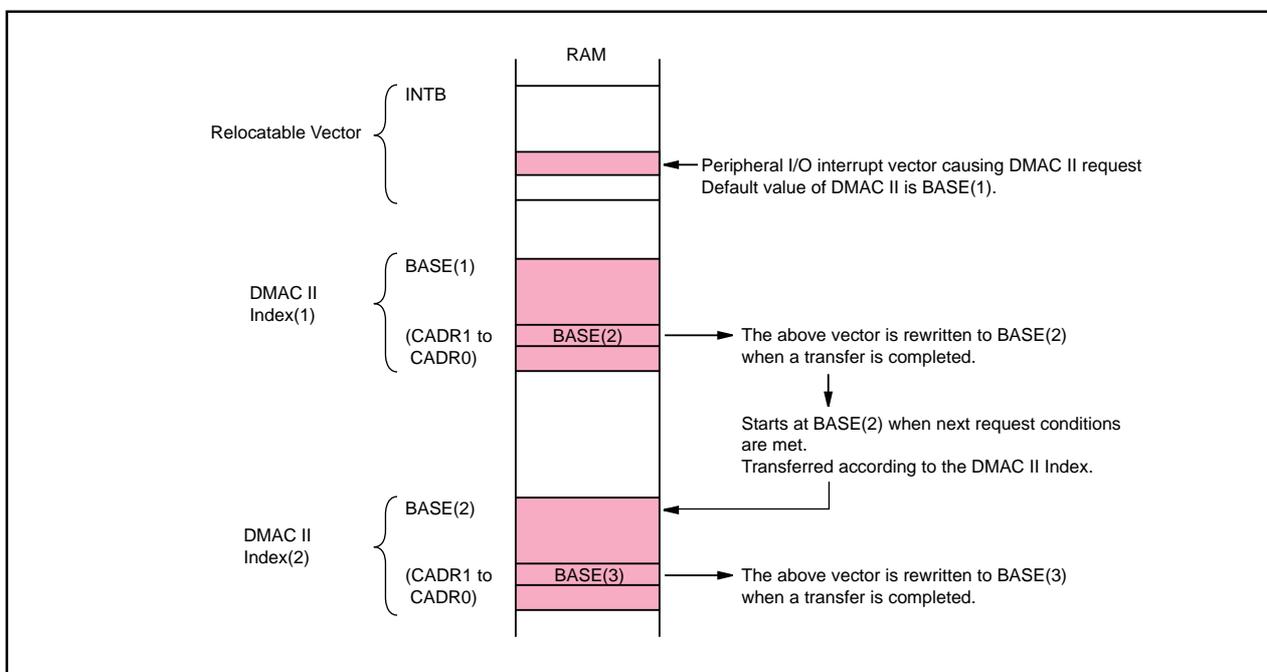


Figure 14.4 Relocatable Vector and DMAC II Index

14.7 End-of-Transfer Interrupt

The INTE bit in MOD selects the end-of-transfer interrupt. Set the starting address of the end-of-transfer interrupt routine in IADR1 and IADR0. The end-of-transfer interrupt is generated when COUNT reaches "0."

14.8 Execution Time

DMAC II execution cycle is calculated by the following equations:

Multiple transfers: $t = 21 + (11 + b + c) \times k$ cycles

Other than multiple transfers: $t = 6 + (26 + a + b + c + d) \times m + (4 + e) \times n$ cycles

- a: If IMM = 0 (source of transfer is immediate data), a = 0;
if IMM = 1 (source of transfer is memory), a = -1
- b: If UPDS = 1 (source transfer address is a relocatable address), b = 0;
if UPDS = 0 (source transfer address is a fixed address), b = 1
- c: If UPDD = 1 (destination transfer address is a relocatable address), c = 0;
if UPDD = 0 (destination transfer address is a fixed address), c = 1
- d: If OPER = 0 (calculation function is not selected), d = 0;
if OPER = 1 (calculation function is selected) and UPDS = 0 (source of transfer is immediate data or fixed address memory), d = 7;
if OPER = 1 (calculation function is selected) and UPDS = 1 (source of transfer is relocatable address memory), d = 8
- e: If CHAIN = 0 (chained transfer is not selected), e = 0; if CHAIN = 1 (chained transfer is selected), e = 4
- m: BRST = 0 (single transfer), m = 1; BRST = 1 (burst transfer), m = the value set in transfer counter
- n: If COUNT = 1, n = 0; if COUNT = 2 or more, n = 1
- k: Number of transfers set in the CNT2 to CNT0 bits

The equations above are approximations. The number of cycles may vary depending on CPU state, bus wait state, and DMAC II index allocation.

The first instruction from the end-of-transfer interrupt routine is executed in the eighth cycle after the DMAC II transfer is completed.

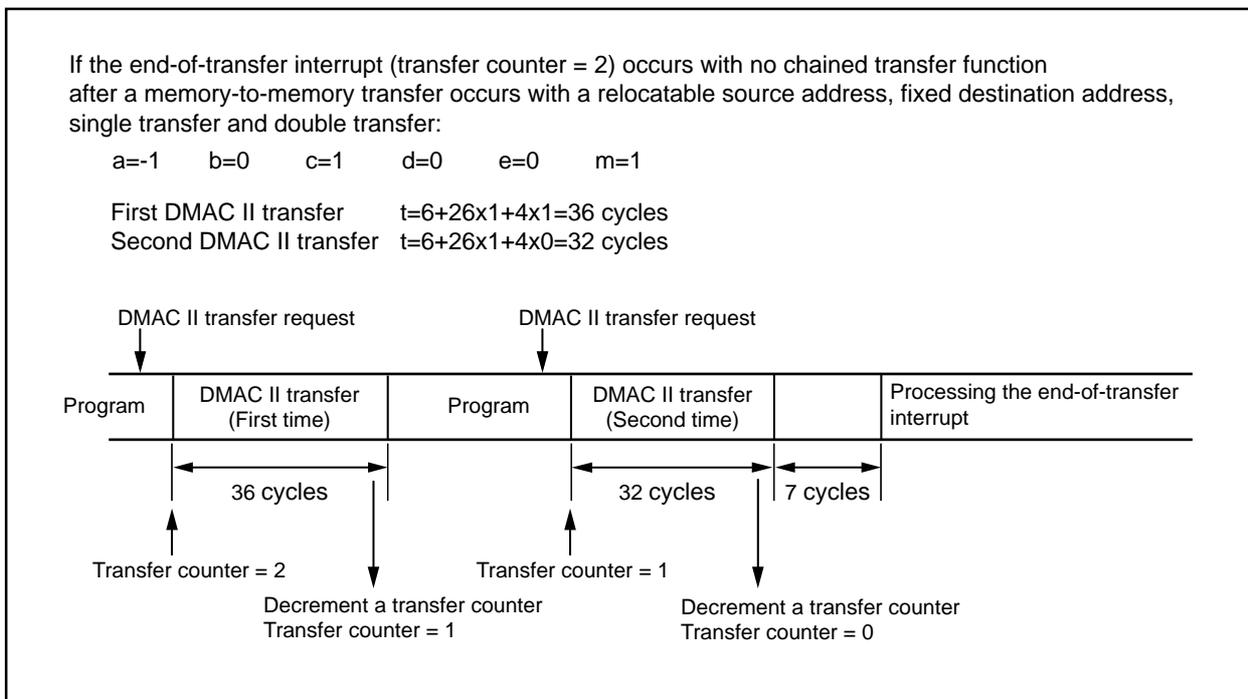


Figure 14.5 Transfer Cycle

When an interrupt request as a DMAC II transfer request source and another interrupt request with higher priority (e.g., $\overline{\text{NMI}}$ or watchdog timer) are generated simultaneously, the interrupt with higher priority takes precedence over the DMAC II transfer. The pending DMAC II transfer starts after the interrupt sequence has been completed.

15. Timer

The microcomputer has eleven 16-bit timers. Five timers A and six timers B have different functions. Each timer functions independently. The count source for each timer becomes the clock for timer operations including counting and reloading, etc. Figures 15.1 and 15.2 show block diagrams of timer A and timer B configuration.

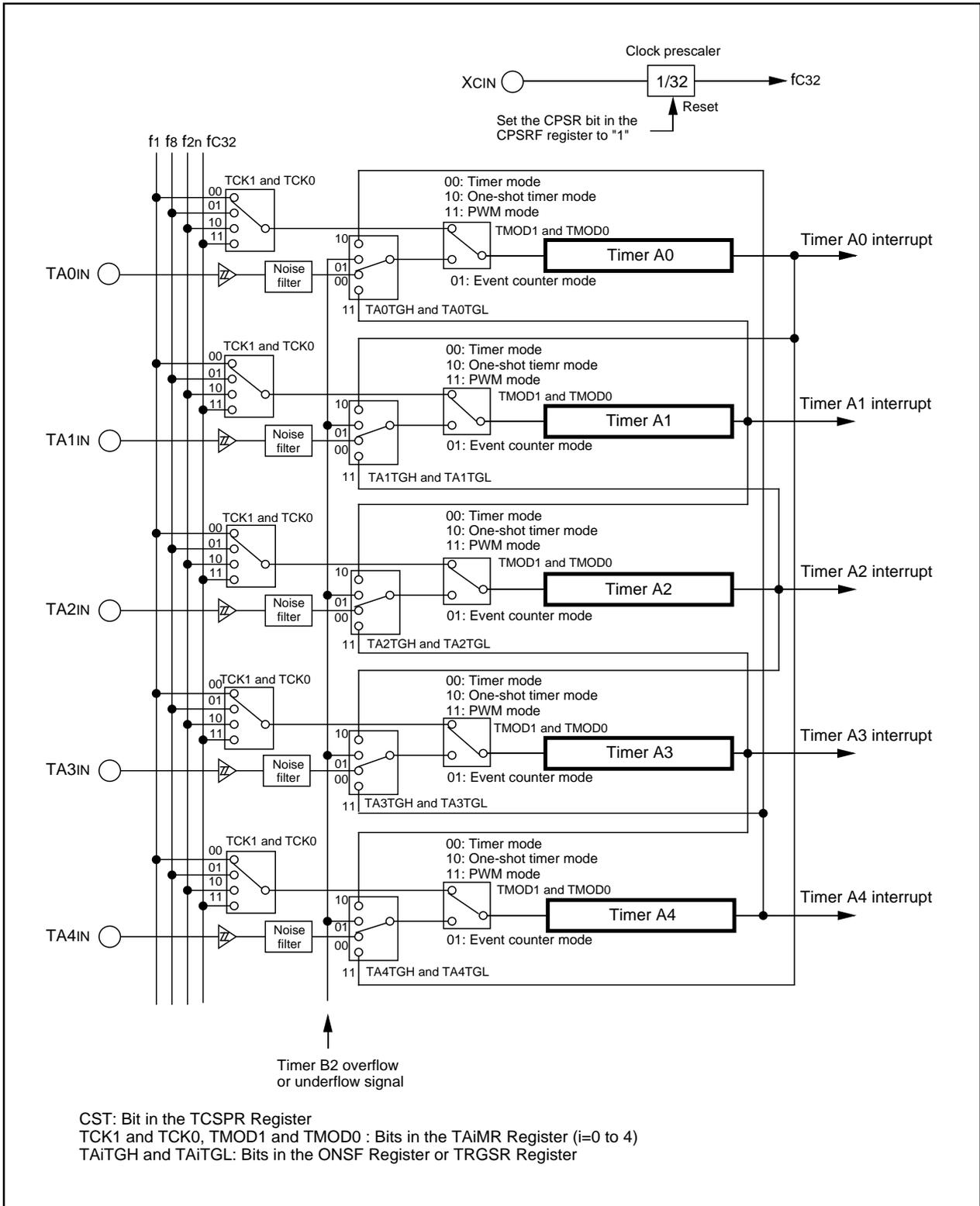


Figure 15.1 Timer A Configuration

15.1 Timer A

Figure 15.3 shows a block diagram of the timer A. Figures 15.4 to 15.7 show registers associated with the timer A.

The timer A supports the following four modes. Except in event counter mode, all timers A0 to A4 have the same function. The TMOD1 and TMOD0 bits in the TAI_iMR register (i=0 to 4) determine which mode is used.

- Timer mode: The timer counts an internal count source.
- Event counter mode: The timer counts an external pulse or an overflow and underflow of other timers.
- One-shot timer mode: The timer outputs one valid pulse until a counter value reaches "000016".
- Pulse width modulation mode: The timer continuously outputs desired pulse widths.

Table 15.1 lists TAI_{OUT} pin settings when used as an output. Table 15.2 lists TAI_{IN} and TAI_{OUT} pin settings when used as an input.

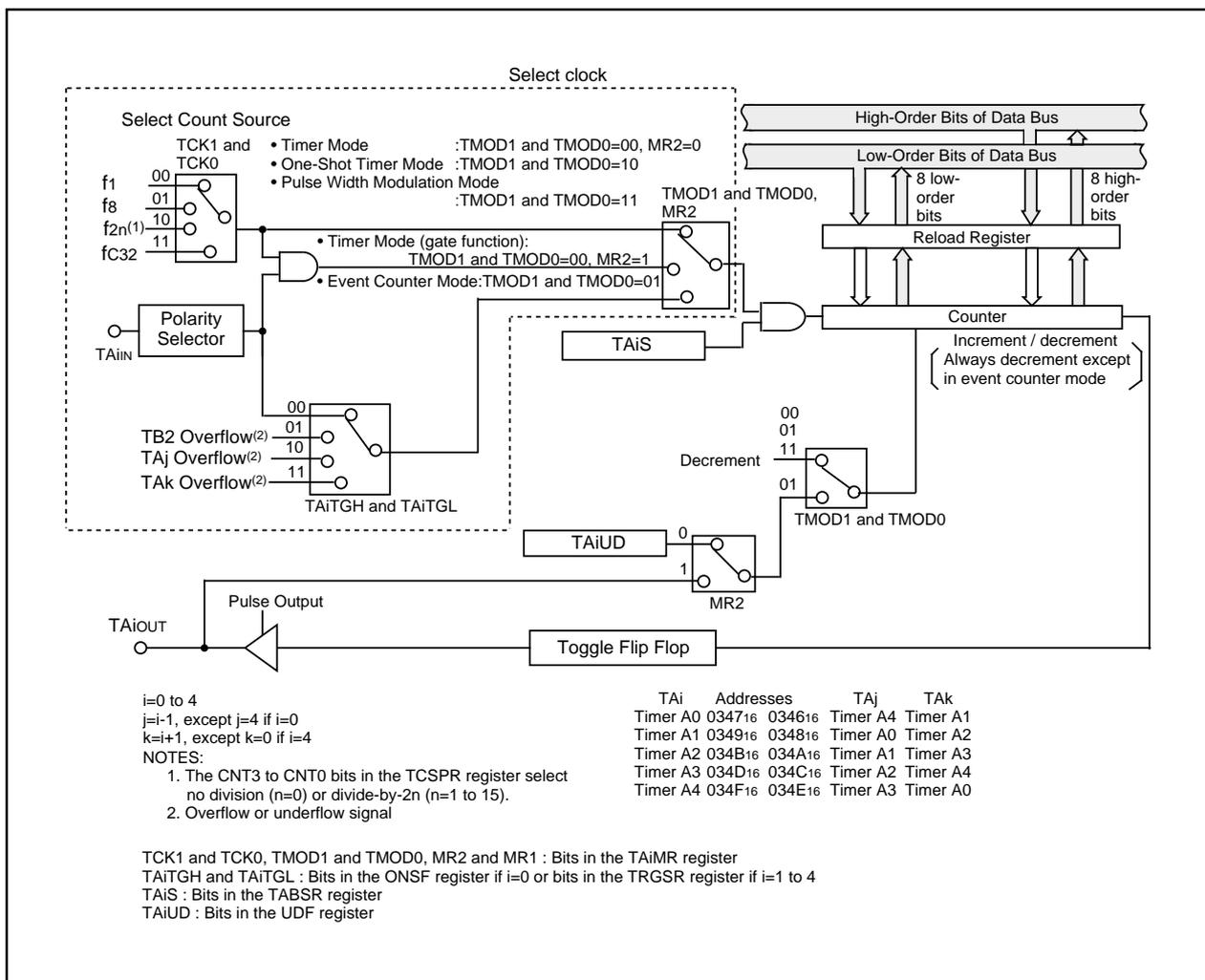


Figure 15.3 Timer A Block Diagram

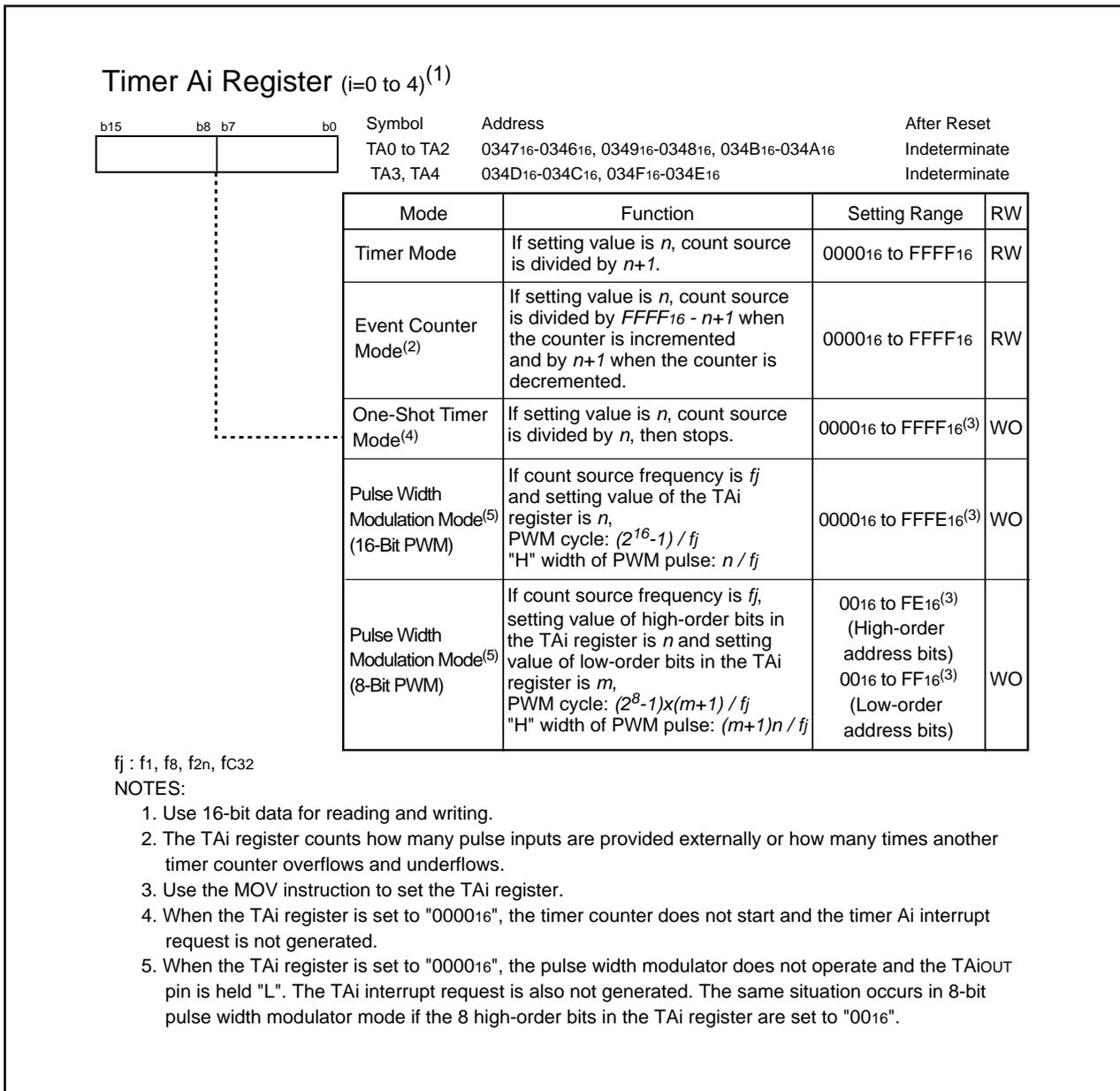


Figure 15.4 TA0 to TA4 Registers

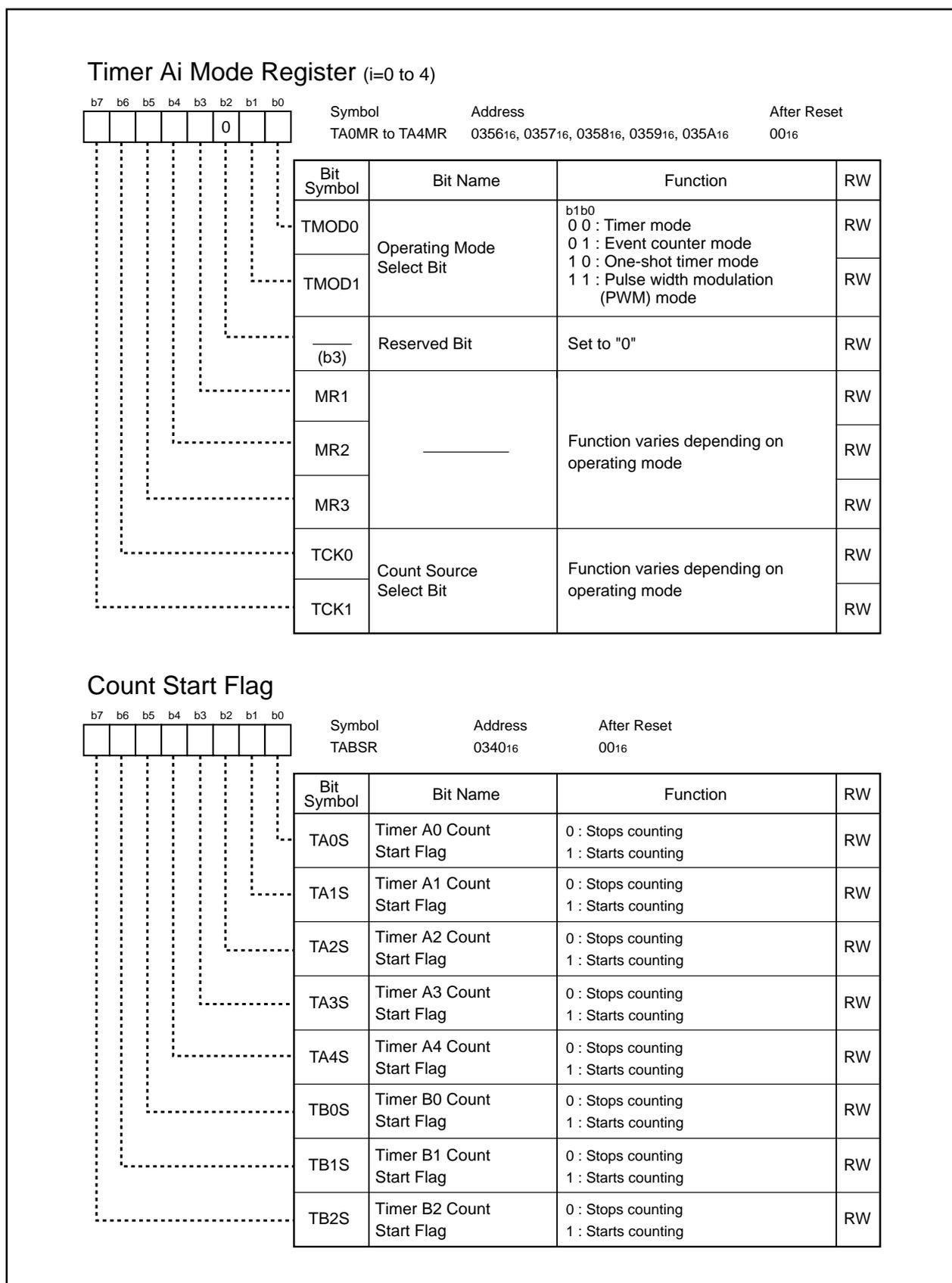


Figure 15.5 TA0MR to TA4MR Registers and TABSR Register

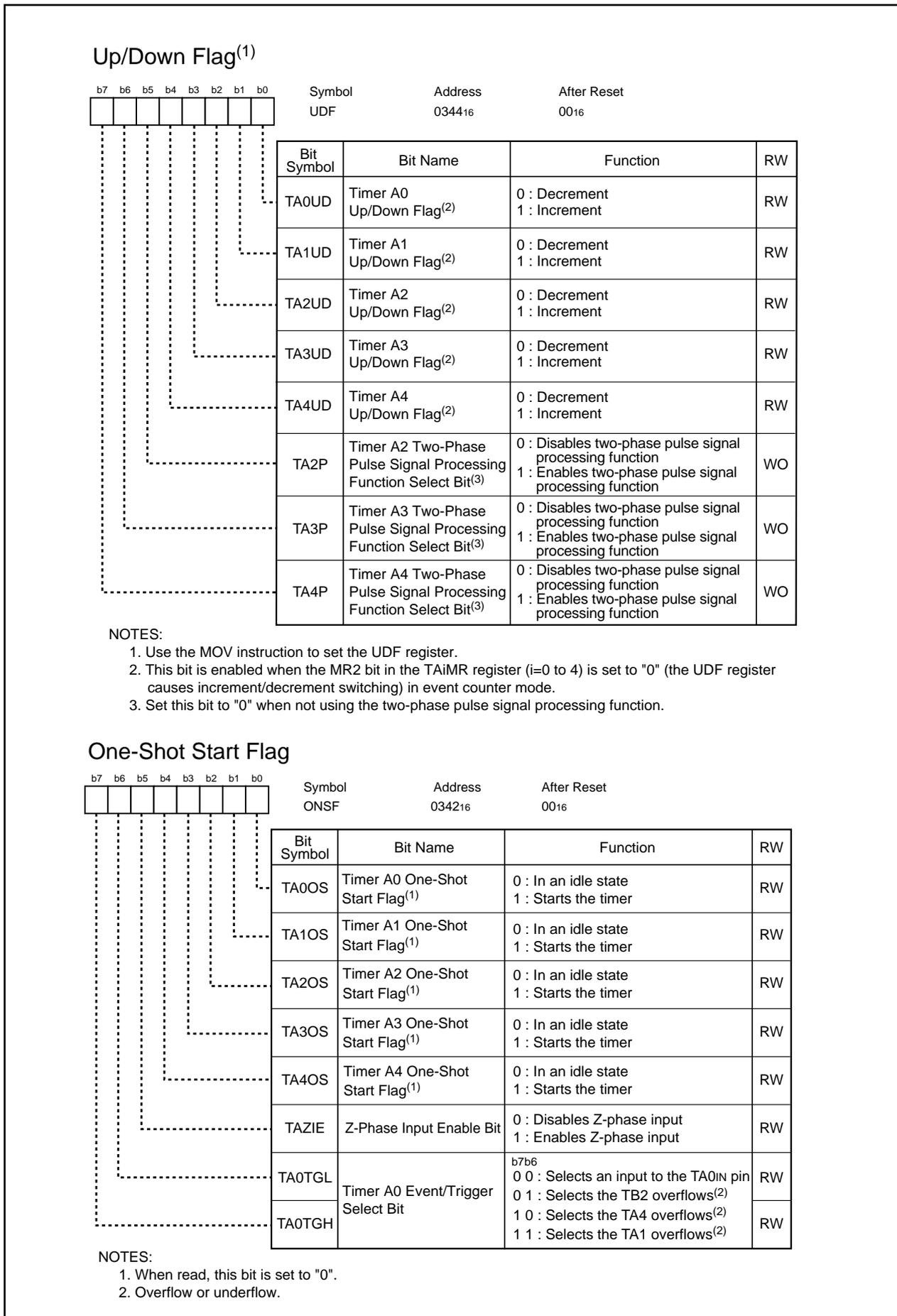


Figure 15.6 UDF Register and ONSF Register

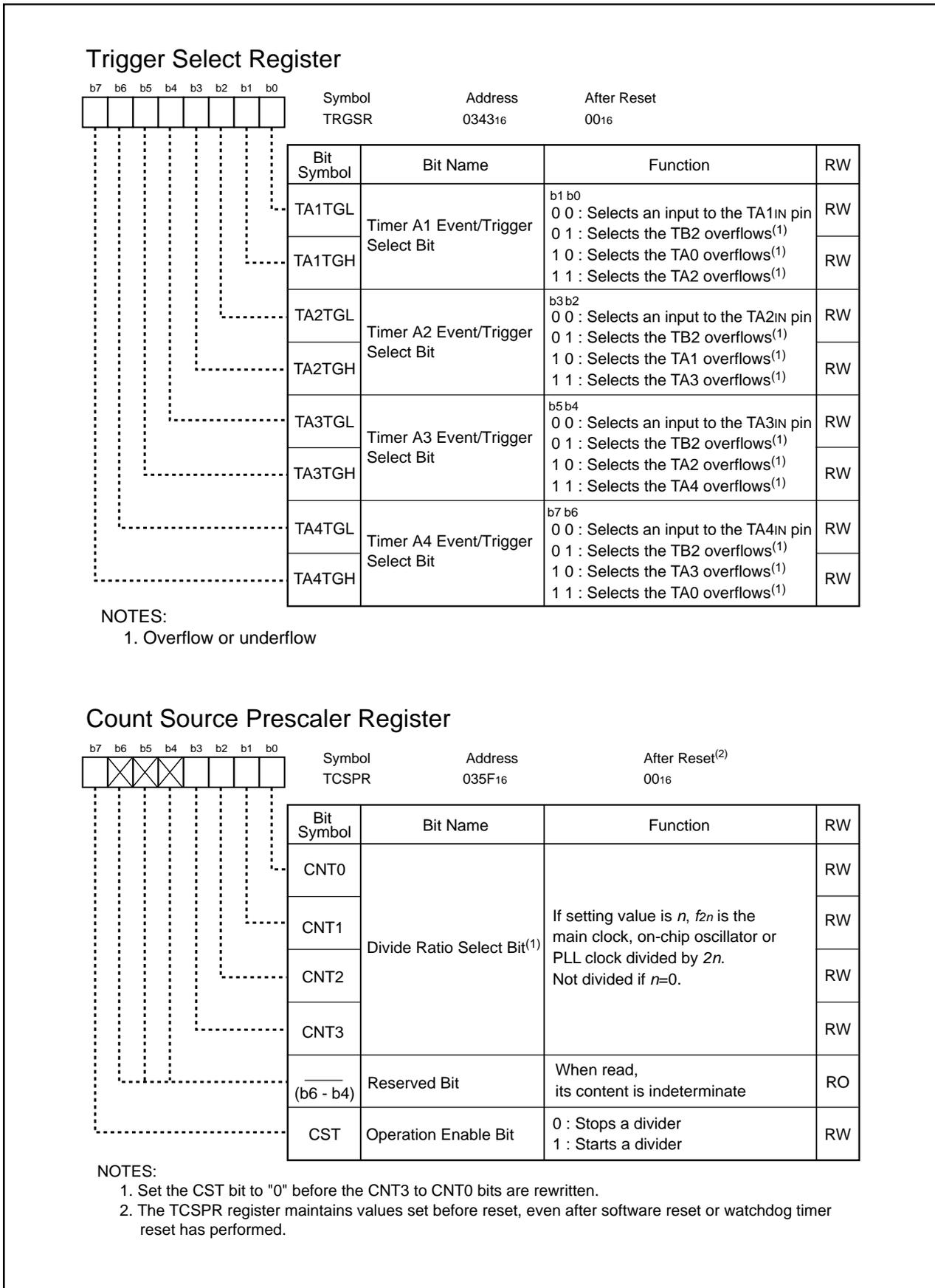


Figure 15.7 TRGSR Register and TCSPR Register

Table 15.1 Pin Settings for Output from TAIOUT Pin (i=0 to 4)

Pin	Setting		
	PS1, PS2 Registers	PSL1, PSL2 Registers	PSC Register
P70/TA0OUT ⁽¹⁾	PS1_0= 1	PSL1_0=1	PSC_0= 0
P72/TA1OUT	PS1_2= 1	PSL1_2=1	PSC_2= 0
P74/TA2OUT	PS1_4= 1	PSL1_4=0	PSC_4= 0
P76/TA3OUT	PS1_6= 1	PSL1_6=1	PSC_6= 0
P80/TA4OUT	PS2_0= 1	PSL2_0=0	–

NOTES:

1. P70/TA0OUT is a port for the N-channel open drain output.

Table 15.2 Pin Settings for Input to TAIIN and TAIOUT Pins (i=0 to 4)

Pin	Setting	
	PS1, PS2 Registers	PD7, PD8 Registers
P70/TA0OUT	PS1_0=0	PD7_0=0
P71/TA0IN	PS1_1=0	PD7_1=0
P72/TA1OUT	PS1_2=0	PD7_2=0
P73/TA1IN	PS1_3=0	PD7_3=0
P74/TA2OUT	PS1_4=0	PD7_4=0
P75/TA2IN	PS1_5=0	PD7_5=0
P76/TA3OUT	PS1_6=0	PD7_6=0
P77/TA3IN	PS1_7=0	PD7_7=0
P80/TA4OUT	PS2_0=0	PD8_0=0
P81/TA4IN	PS2_1=0	PD8_1=0

15.1.1 Timer Mode

In timer mode, the timer counts an internally generated count source (see **Table 15.3**). Figure 15.8 shows the TAI_{MR} register (i=0 to 4) in timer mode.

Table 15.3 Timer Mode Specifications

Item	Specification
Count Source	f1, f8, f2n ⁽¹⁾ , fc32
Counting Operation	<ul style="list-style-type: none"> The timer decrements a counter value When the timer counter underflows, content of the reload register is reloaded into the count register and counting resumes.
Divide Ratio	1/(n+1) n: setting value of the TAI register (i=0 to 4) 0000 ₁₆ to FFFF ₁₆
Counter Start Condition	The TAI _S bit in the TABSR register is set to "1" (starts counting)
Counter Stop Condition	The TAI _S bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer counter underflows
TAI _{IN} Pin Function	Programmable I/O port or gate input
TAI _{OUT} Pin Function	Programmable I/O port or pulse output
Read from Timer	The TAI register indicates counter value
Write to Timer	<ul style="list-style-type: none"> While the timer counter stops, the value written to the TAI register is also written to both reload register and counter While counting, the value written to the TAI register is written to the reload register (It is transferred to the counter at the next reload timing)
Selectable Function	<ul style="list-style-type: none"> Gate function Input signal to the TAI_{IN} pin determines whether the timer counter starts or stops counting Pulse output function The polarity of the TAI_{OUT} pin is inverted whenever the timer counter underflows

NOTES:

- The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2ⁿ (n=1 to 15).

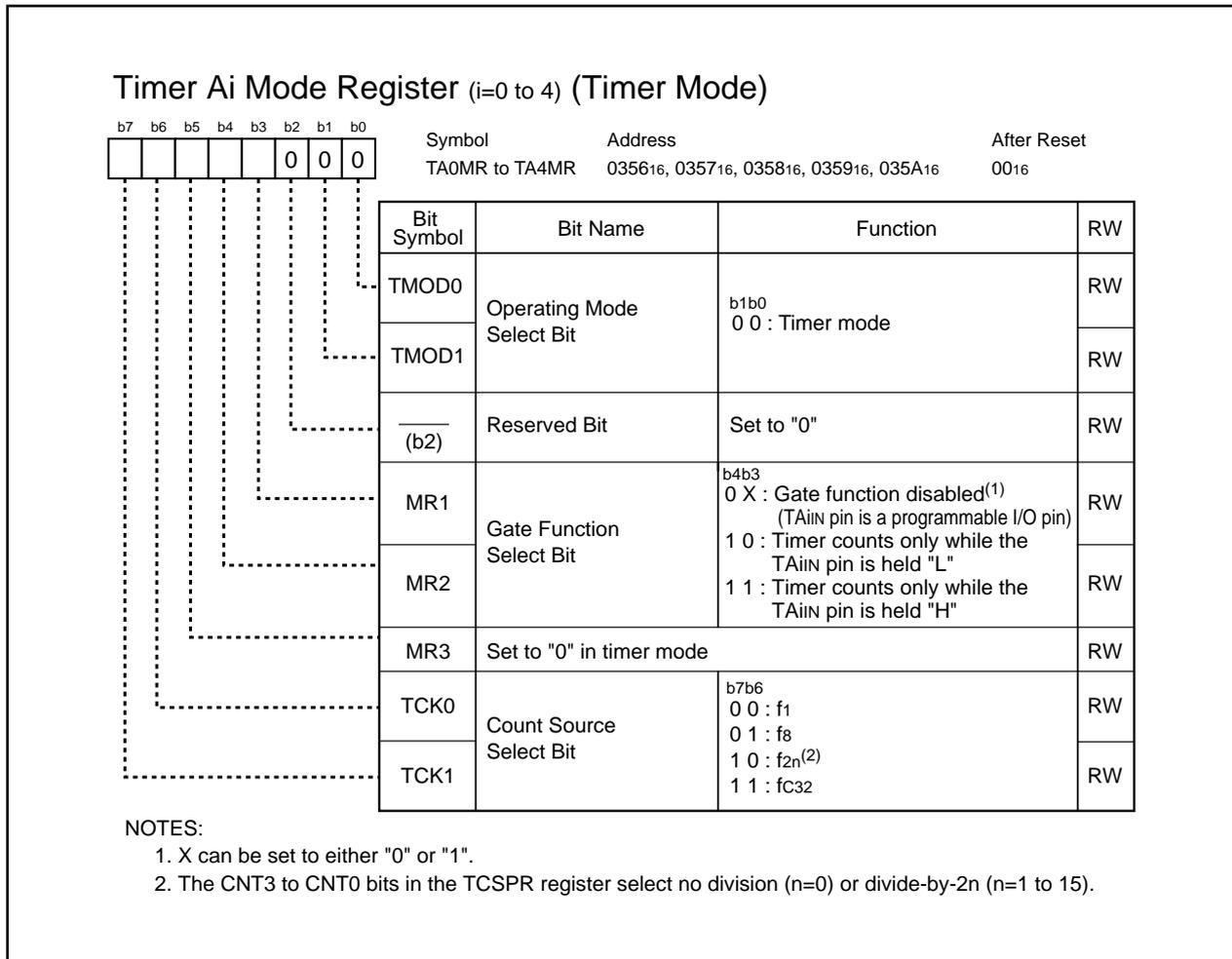


Figure 15.8 TA0MR to TA4MR Registers

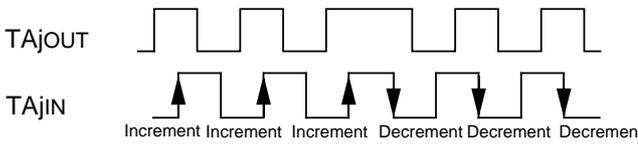
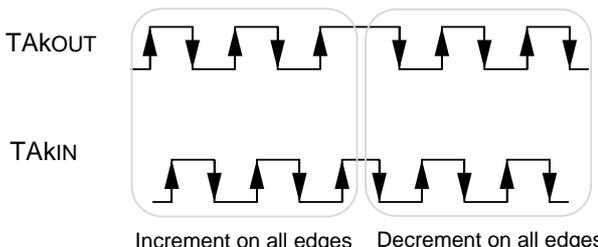
15.1.2 Event Counter Mode

In event counter mode, the timer counts how many external signals are applied or how many times another timer counter overflows and underflows. The timers A2, A3 and A4 can count externally generated two-phase signals. Table 15.4 lists specifications in event counter mode (when not handling a two-phase pulse signal). Table 15.5 lists specifications in event counter mode (when handling a two-phase pulse signal with the timers A2, A3 and A4). Figure 15.9 shows the TAI_{MR} register (i=0 to 4) in event counter mode.

Table 15.4 Event Counter Mode Specifications (When Not Processing Two-phase Pulse Signal)

Item	Specification
Count Source	<ul style="list-style-type: none"> External signal applied to the TAI_{IN} pin (i = 0 to 4) (valid edge can be selected by program) Timer B2 overflow or underflow signal, timer A_j overflow or underflow signal (j=i-1, except j=4 if i=0) and timer A_k overflow or underflow signal (k=i+1, except k=0 if i=4)
Counting Operation	<ul style="list-style-type: none"> External signal and program can determine whether the timer increments or decrements a counter value When the timer counter underflows or overflows, content of the reload register is reloaded into the count register and counting resumes. When the free-running count function is selected, the timer counter continues running without reloading.
Divide Ratio	<ul style="list-style-type: none"> $1/(FFFF_{16} - n + 1)$ for counter increment $1/(n + 1)$ for counter decrement n: setting value of the TAI register 0000_{16} to $FFFF_{16}$
Counter Start Condition	The TAI _S bit in the TABSR register is set to "1" (starts counting)
Counter Stop Condition	The TAI _S bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer counter overflows or underflows
TAI _{IN} Pin Function	Programmable I/O port or count source input
TAI _{OUT} Pin Function	Programmable I/O port, pulse output or input selecting a counter increment or decrement
Read from Timer	The TAI register indicates counter value
Write to Timer	<ul style="list-style-type: none"> When the timer counter stops, the value written to the TAI register is also written to both reload register and counter While counting, the value written to the TAI register is written to the reload register (It is transferred to the counter at the next reload timing)
Selectable Function	<ul style="list-style-type: none"> Free-running count function Content of the reload register is not reloaded even if the timer counter overflows or underflows Pulse output function The polarity of the TAI_{OUT} pin is inversed whenever the timer counter overflows or underflows

Table 15.5 Event Counter Mode Specifications (When Processing Two-phase Pulse Signal on Timer A2, A3 and A4)

Item	Specification
Count Source	Two-phase pulse signal applied to the TAIIN and TAIOUT pins (i = 2 to 4)
Counting Operation	<ul style="list-style-type: none"> Two-phase pulse signal determines whether the timer increments or decrements a counter value When the timer counter overflows or underflows, content of the reload register is reloaded into the count register and counting resumes. With the free-running count function, the timer counter continues running without reloading.
Divide Ratio	<ul style="list-style-type: none"> $1/(FFFF_{16} - n + 1)$ for counter increment $1/(n + 1)$ for counter decrement n: setting value of the TAI register 0000_{16} to $FFFF_{16}$
Counter Start Condition	The TAI _S bit in the TABSR register is set to "1" (starts counting)
Counter Stop Condition	The TAI _S bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer counter overflows or underflows
TAiIN Pin Function	Two-phase pulse signal is applied
TAiOUT Pin Function	Two-phase pulse signal is applied
Read from Timer	The TAI register indicates the counter value
Write to Timer	<ul style="list-style-type: none"> When the timer counter stops, the value written to the TAI register is also written to both reload register and counter While counting, the value written to the TAI register is written to the reload register (It is transferred to the counter at the next reload timing)
Selectable Function ⁽¹⁾	<ul style="list-style-type: none"> Normal processing operation (the timer A2 and timer A3) While a high-level ("H") signal is applied to the TAJOUT pin (j = 2 or 3), the timer increments a counter value on the rising edge of the TAJIN pin or decrements a counter on the falling edge.  <ul style="list-style-type: none"> Multiply-by-4 processing operation (the timer A3 and timer A4) While an "H" signal is applied to the TAKOUT pin (k = 3 or 4) on the rising edge of the TAKIN pin, the timer increments a counter value on the rising and falling edges of the TAKOUT and TAKIN pins. While an "H" signal is applied to the TAKOUT pin on the falling edge of the TAKIN pin, the timer decrements a counter value on the rising and falling edges of the TAKOUT and TAKIN pins. 

NOTES:

- Only timer A3 operation can be selected. The timer A2 is for the normal processing operation. The timer A4 is for the multiply-by-4 operation.

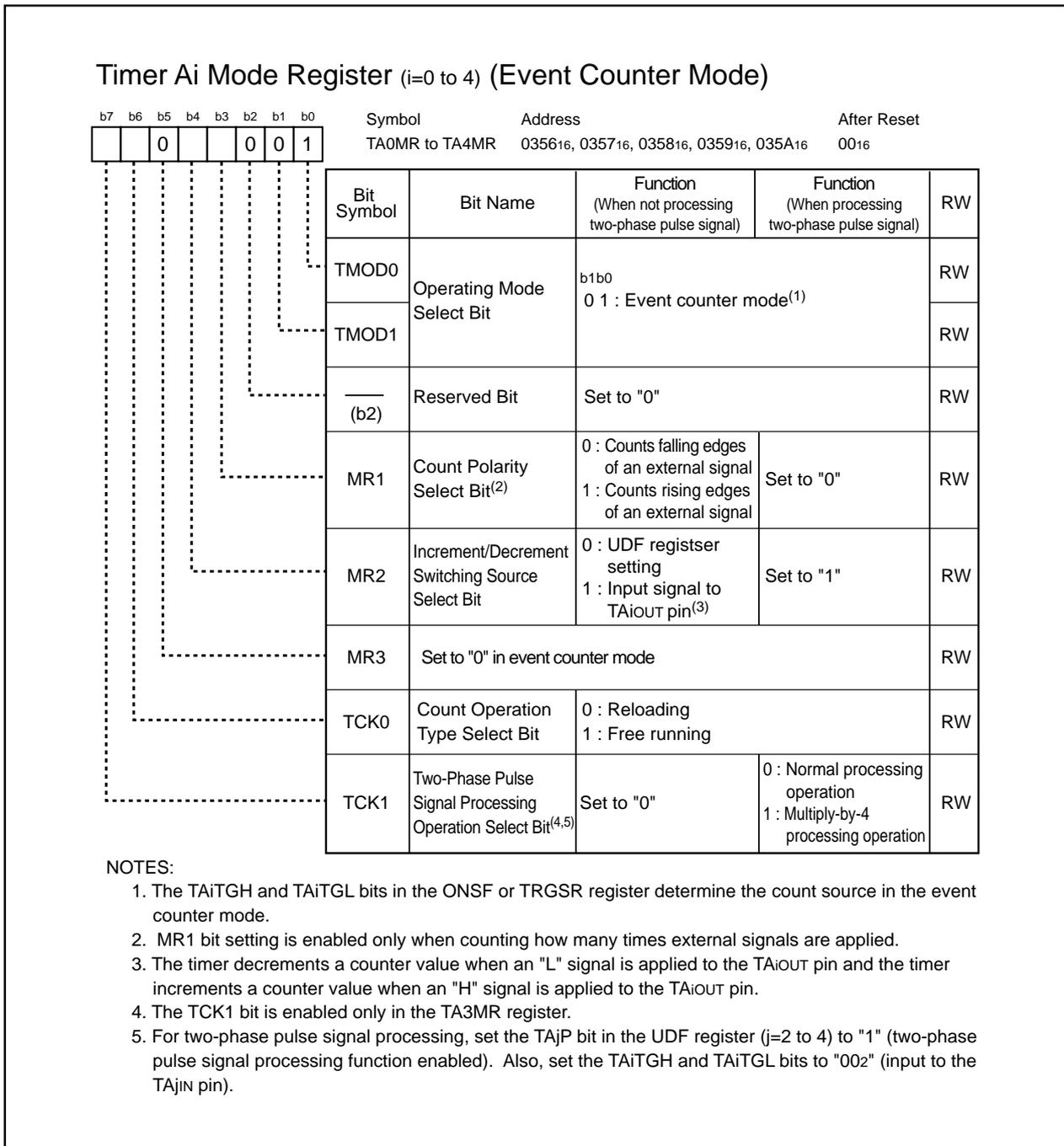


Figure 15.9 TA0MR to TA4MR Registers

15.1.2.1 Counter Reset by Two-Phase Pulse Signal Processing

Z-phase input resets the timer counter when processing a two-phase pulse signal.

This function can be used in timer A3 event counter mode, two-phase pulse signal processing, free-running count operation type or multiply-by-4 processing. The Z-phase signal is applied to the $\overline{\text{INT2}}$ pin. When the TAZIE bit in the ONSF register is set to "1" (Z-phase input enabled), Z-phase input can reset the timer counter. To reset the counter by a Z-phase input, set the TA3 register to "000016" beforehand.

Z-phase input is enabled when the edge of the signal applied to the $\overline{\text{INT2}}$ pin is detected. The POL bit in the INT2IC register can determine edge polarity. The Z-phase must have a pulse width of one timer A3 count source cycle or more. Figure 15.10 shows two-phase pulses (A-phase and B-phase) and the Z-phase.

Z-phase input resets the timer counter in the next count source following Z-phase input. Figure 15.11 shows the counter reset timing.

Timer A3 interrupt request is generated twice continuously when a timer A3 overflow or underflow, and a counter reset by $\overline{\text{INT2}}$ input occur at the same time. Do not use the timer A3 interrupt request when this function is used.

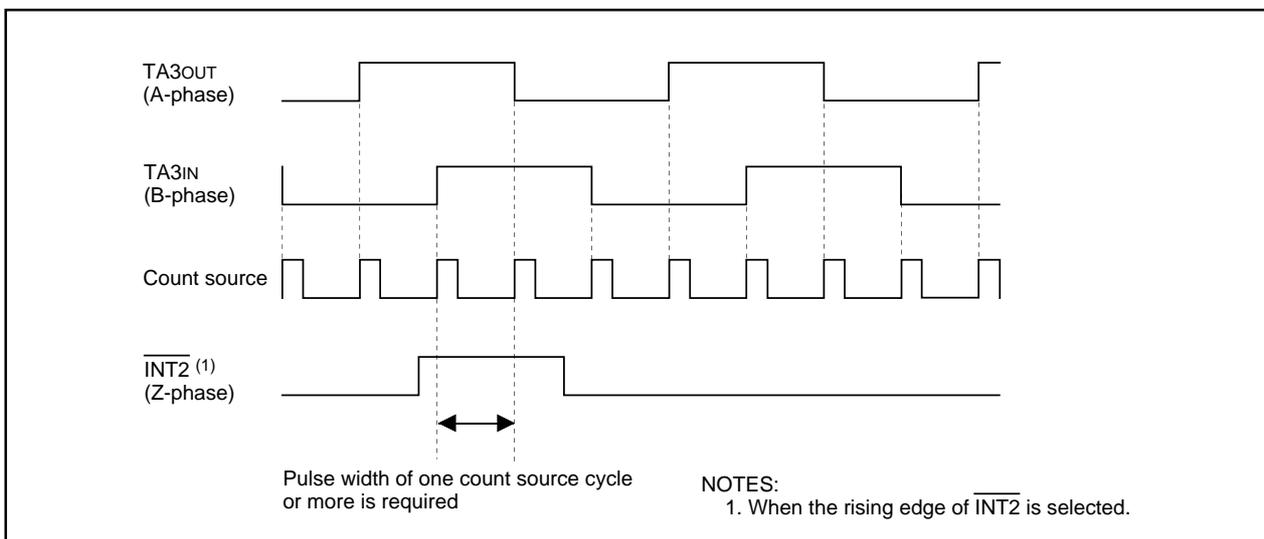


Figure 15.10 Two-Phase Pulse (A-phase and B-phase) and Z-phase

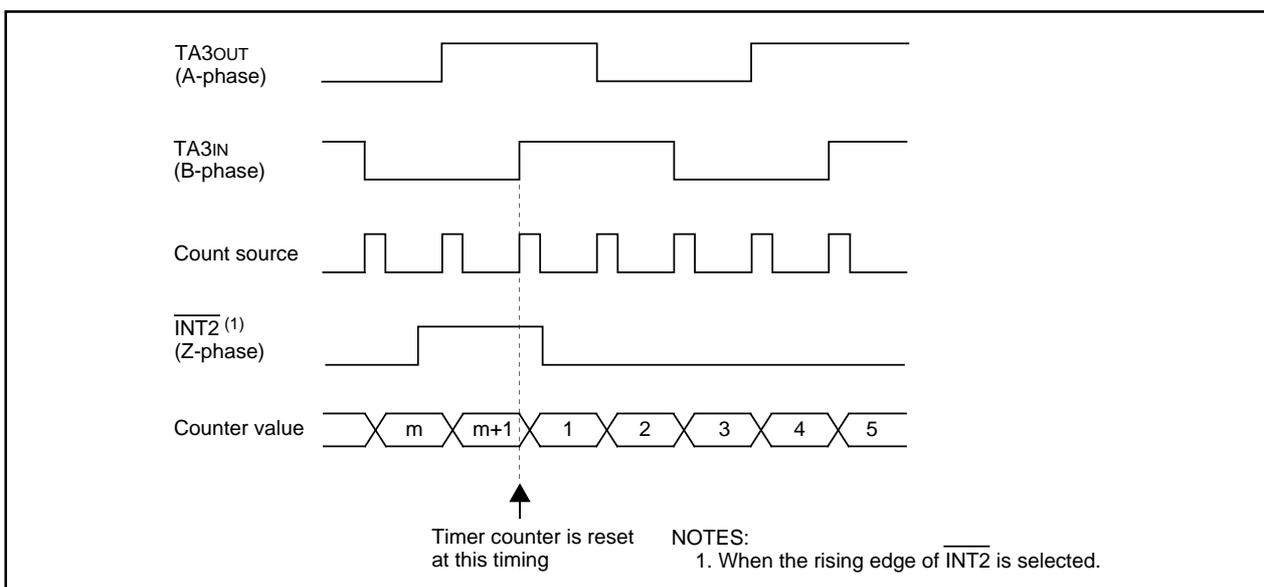


Figure 15.11 Counter Reset Timing

15.1.3 One-Shot Timer Mode

In one-shot timer mode, the timer operates only once for each trigger (see **Table 15.6**). Once a trigger occurs, the timer starts and continues operating for a desired period. Figure 15.12 shows the TAI_MR register (i=0 to 4) in one-shot timer mode.

Table 15.6 One-Shot Timer Mode Specifications

Item	Specification
Count Source	f ₁ , f ₈ , f _{2ⁿ} ⁽¹⁾ , f _{C32}
Counting Operation	<ul style="list-style-type: none"> The timer decrements a counter value When the timer counter reaches "0000 ₁₆ ", it stops counting after reloading. If a trigger occurs while counting, content of the reload register is reloaded into the count register and counting resumes.
Divide Ratio	1/n n: setting value of the TAI register (i=0 to 4) 0000 ₁₆ to FFFF ₁₆ , but the timer counter does not run if n=0000 ₁₆
Counter Start Condition	The TAI _S bit in the TABSR register is set to "1" (starts counting) and following triggers occur: <ul style="list-style-type: none"> External trigger input is provided Timer counter overflows or underflows The TAI_{OS} bit in the ONSF register is set to "1" (timer started)
Counter Stop Condition	<ul style="list-style-type: none"> After the timer counter has reached "0000₁₆" and is reloaded When the TAI_S bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer counter reaches "0000 ₁₆ "
TAI _{IN} Pin Function	Programmable I/O port or trigger input
TAI _{OUT} Pin Function	Programmable I/O port or pulse output
Read from Timer	The value in the TAI register is indeterminate when read
Write to Timer	<ul style="list-style-type: none"> When the timer counter stops, the value written to the TAI register is also written to both reload register and counter While counting, the value written to the TAI register is written to the reload register (It is transferred to the counter at the next reload timing)

NOTES:

- The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2ⁿ (n=1 to 15).

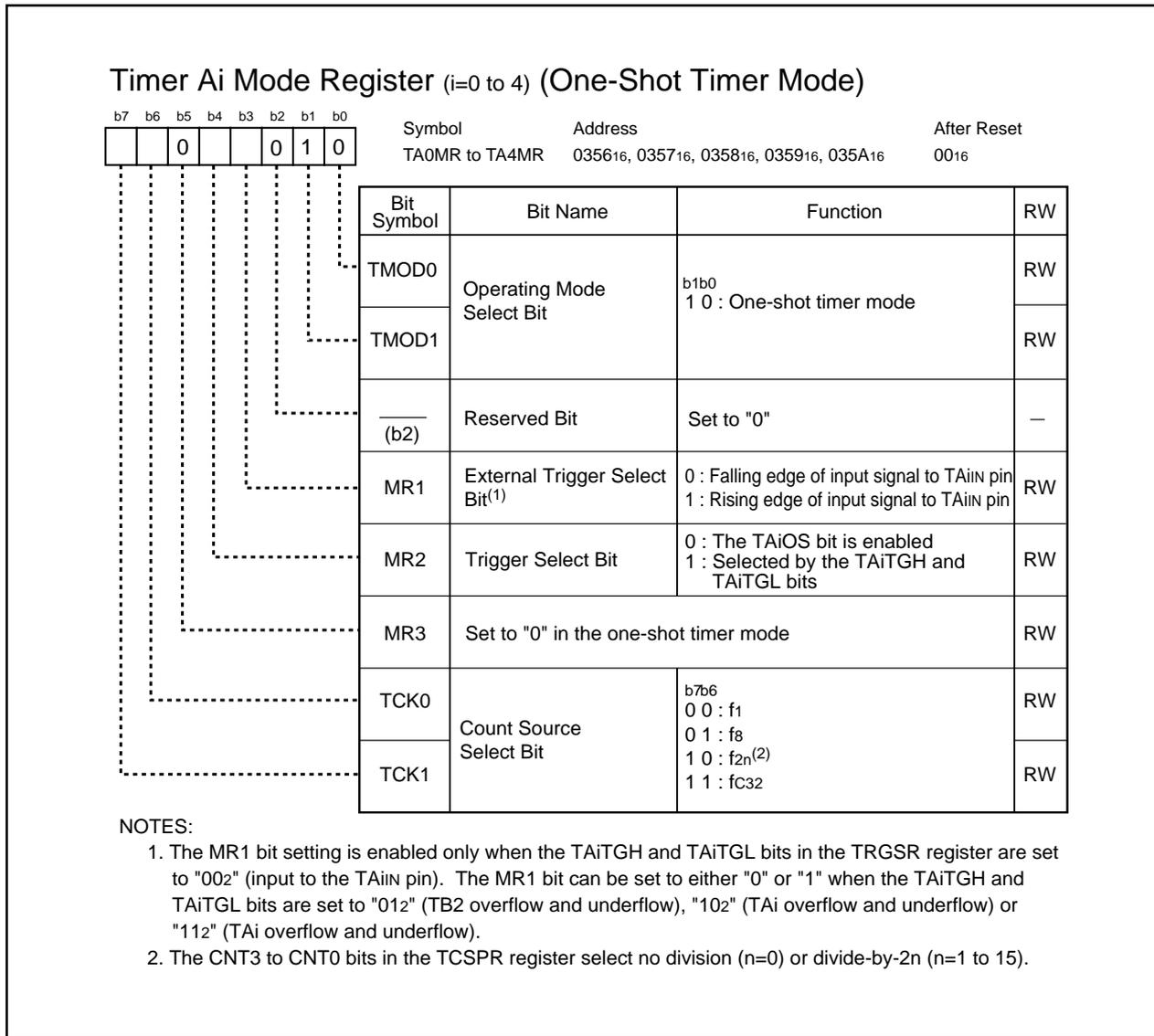


Figure 15.12 TA0MR to TA4MR Registers

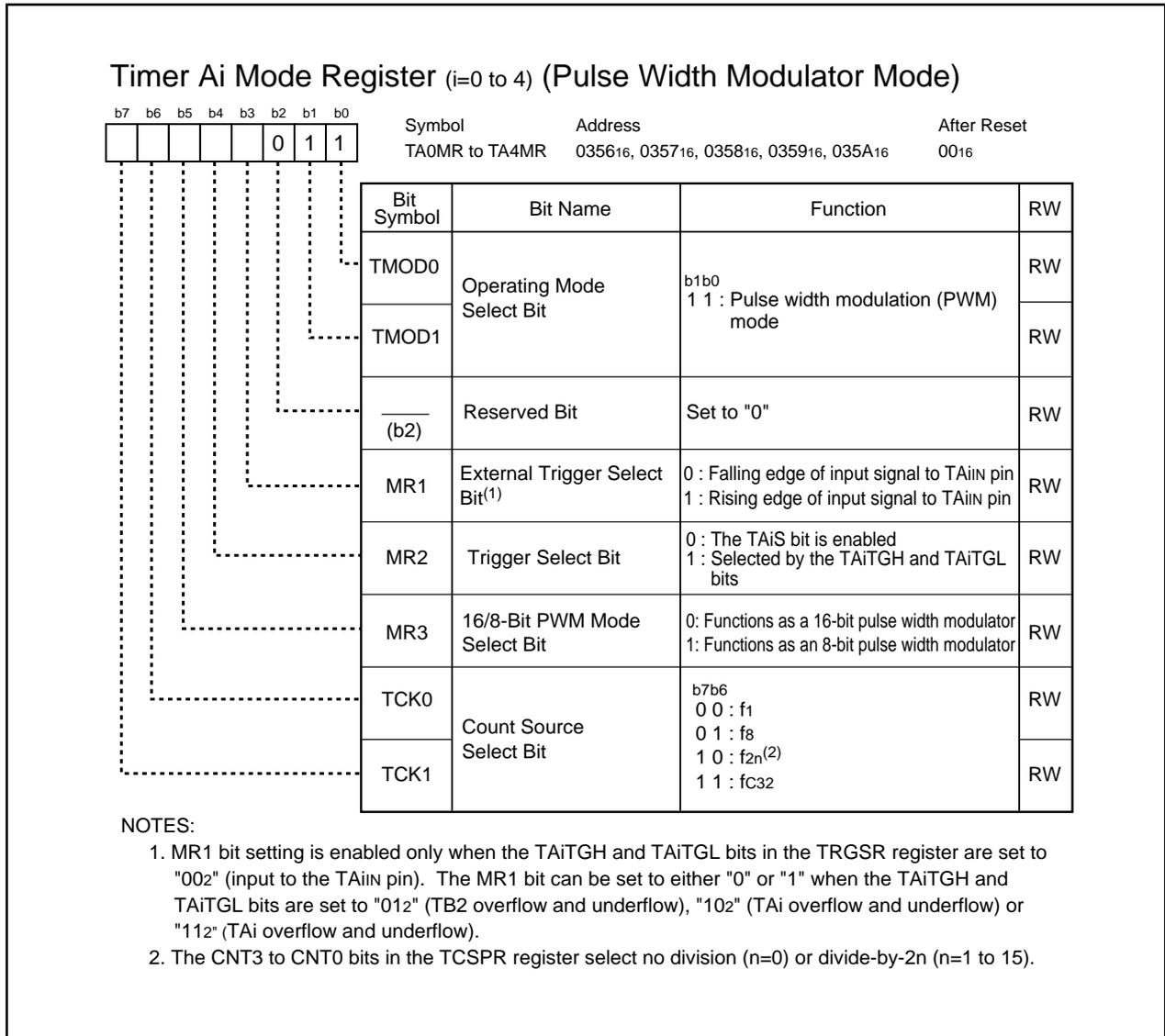


Figure 15.13 TA0MR to TA4MR Registers

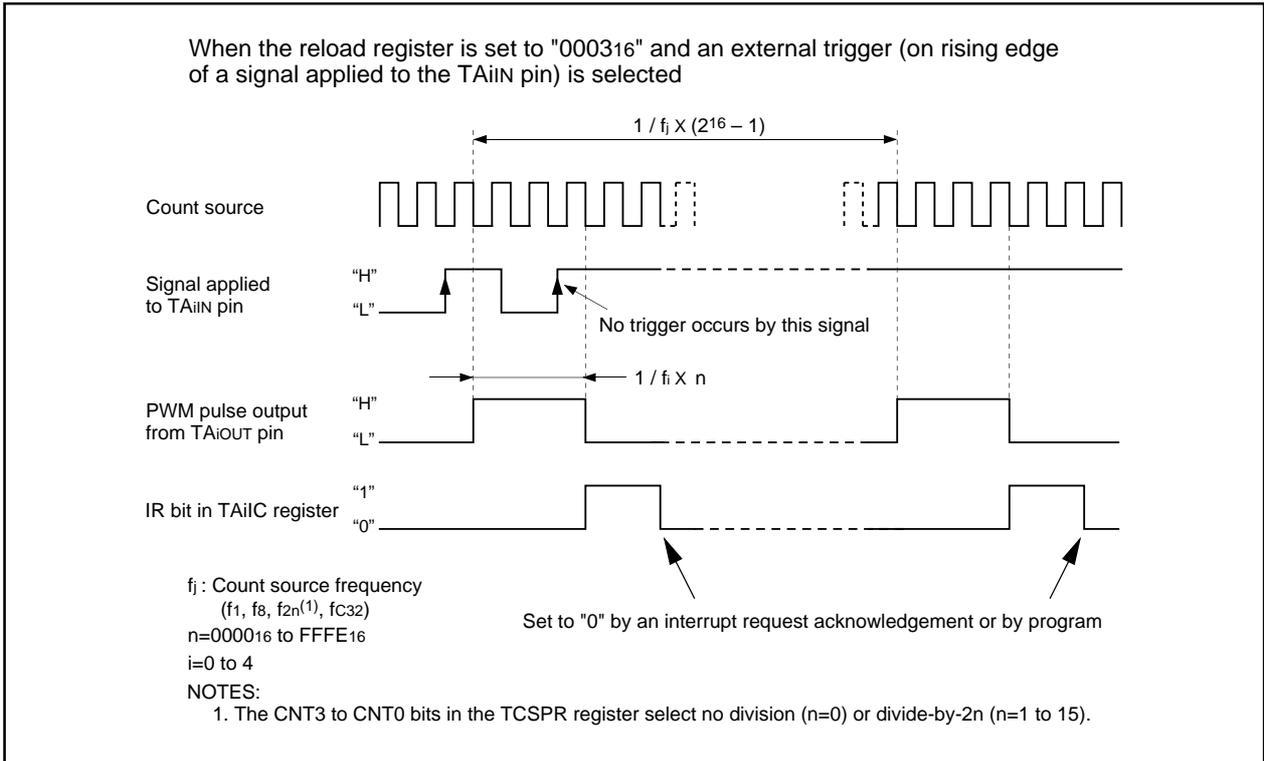


Figure 15.14 16-bit Pulse Width Modulator Operation

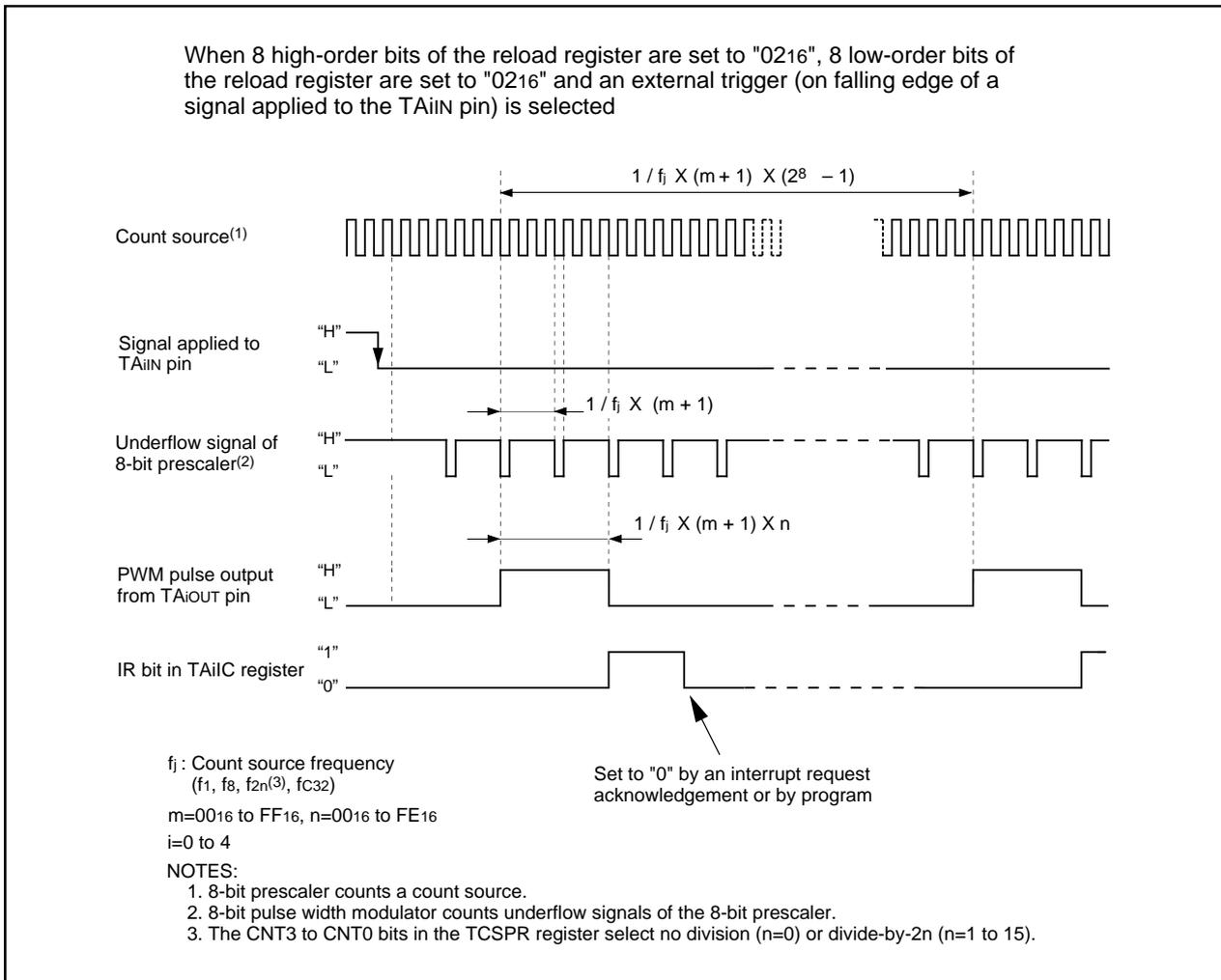


Figure 15.15 8-bit Pulse Width Modulator Operation

15.2 Timer B

Figure 15.16 shows a block diagram of the timer B. Figures 15.17 to 15.19 show registers associated with the timer B. The timer B supports the following three modes. The TMOD1 and TMOD0 bits in the TBiMR register (i=0 to 5) determine which mode is used.

- Timer mode : The timer counts an internal count source.
- Event counter mode : The timer counts pulses from an external source or overflow and underflow of another timer.
- Pulse period/pulse width measurement mode : The timer measures pulse period or pulse width of an external signal.

Table 15.8 lists TBiIN pin settings.

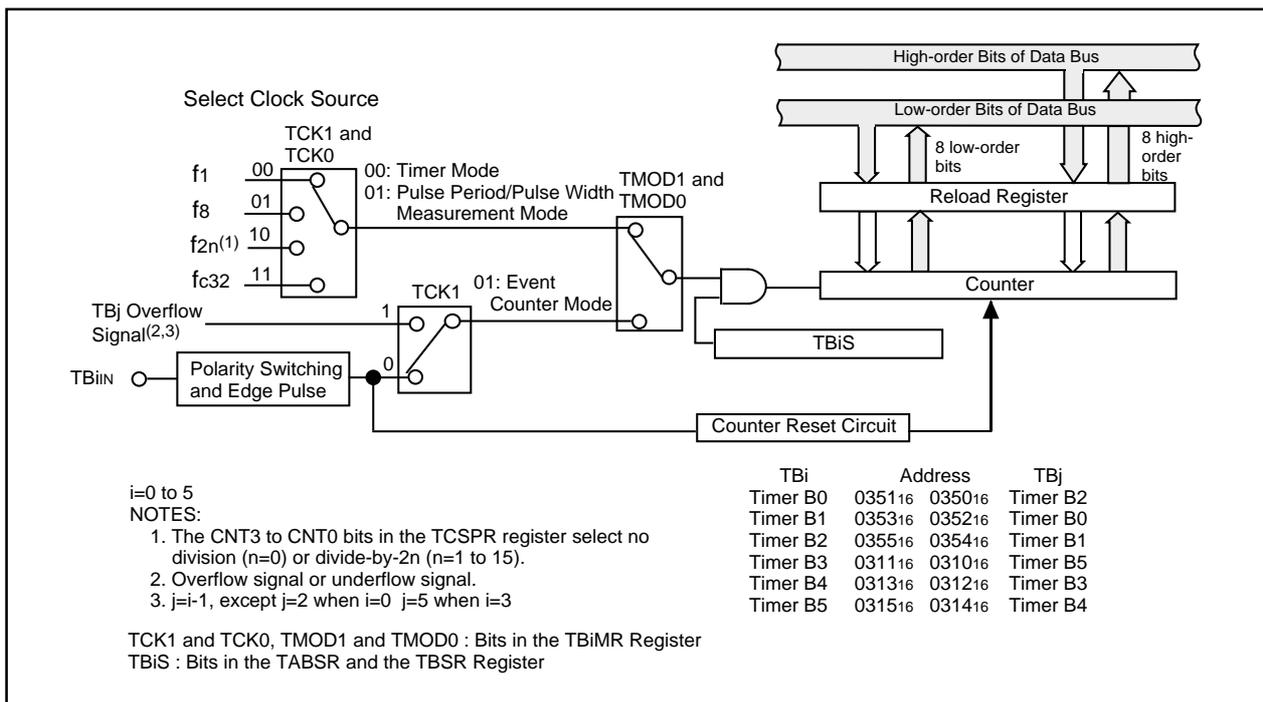


Figure 15.16 Timer B Block Diagram

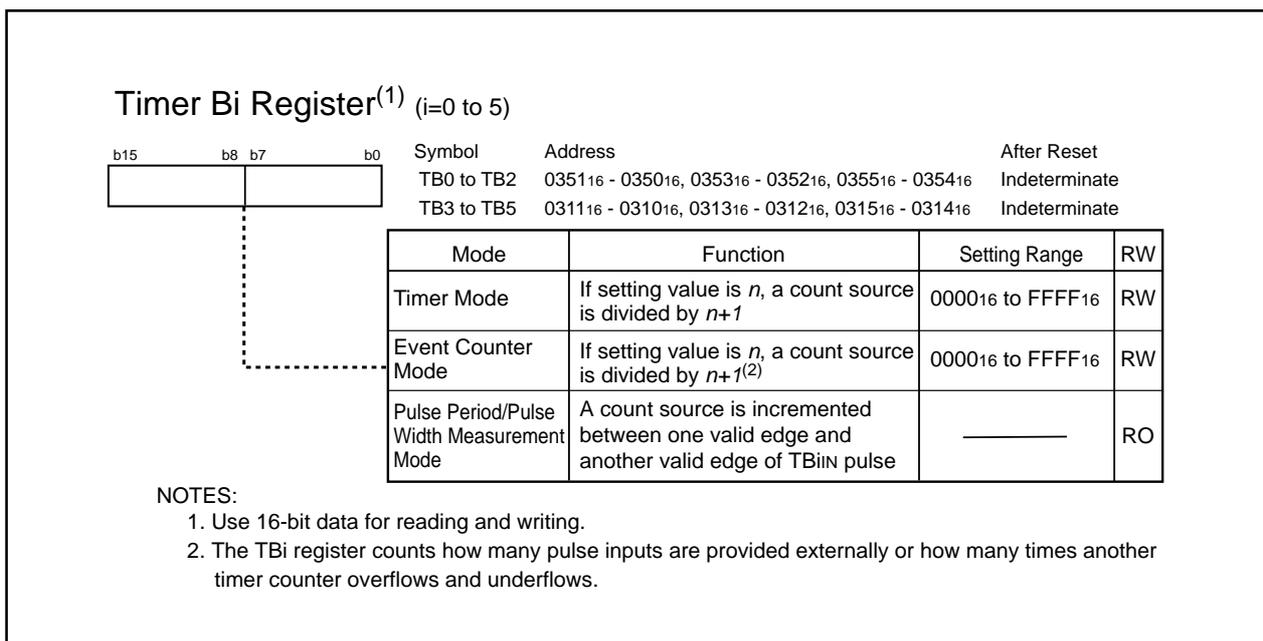


Figure 15.17 TB0 to TB5 Registers

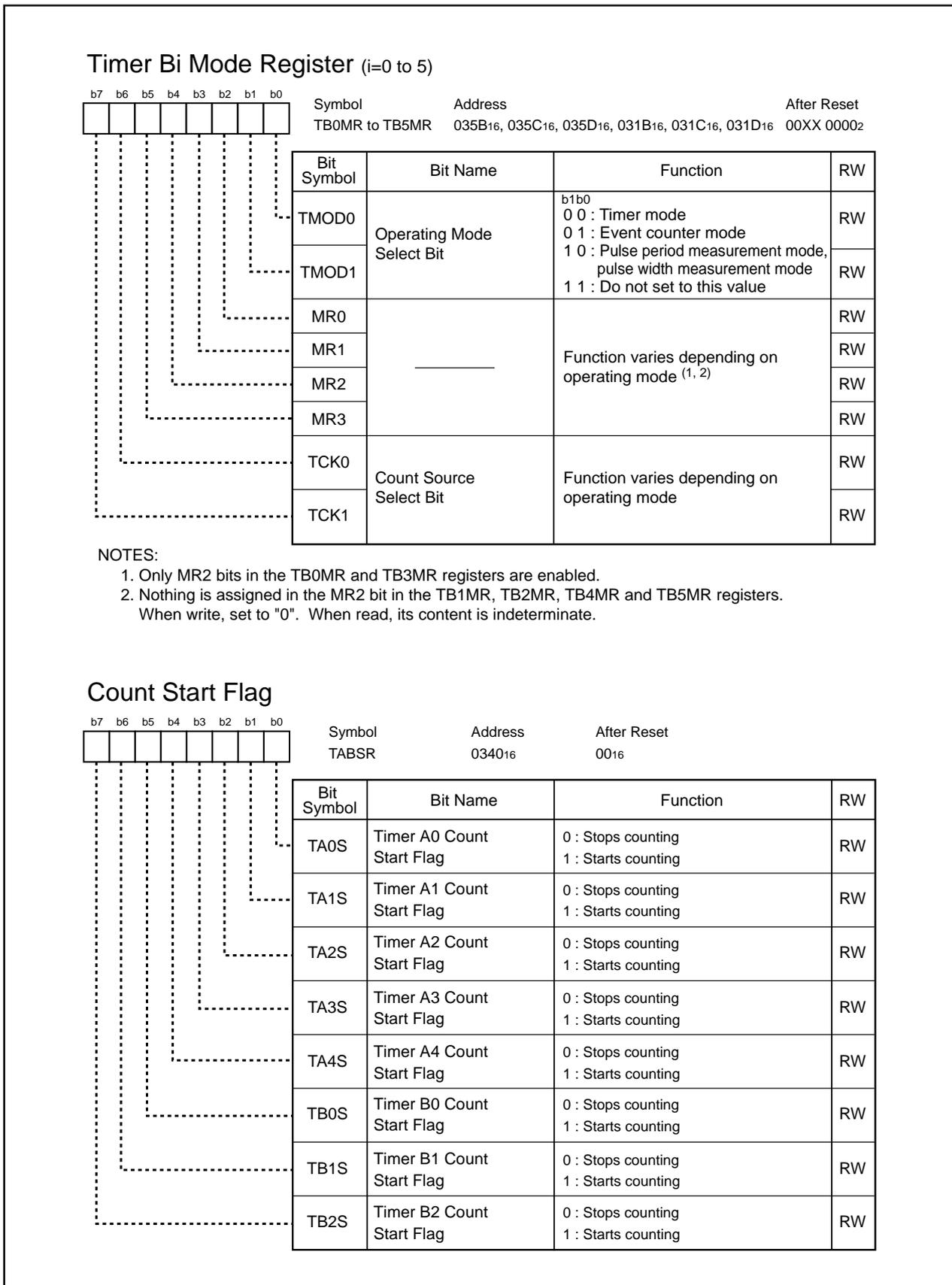
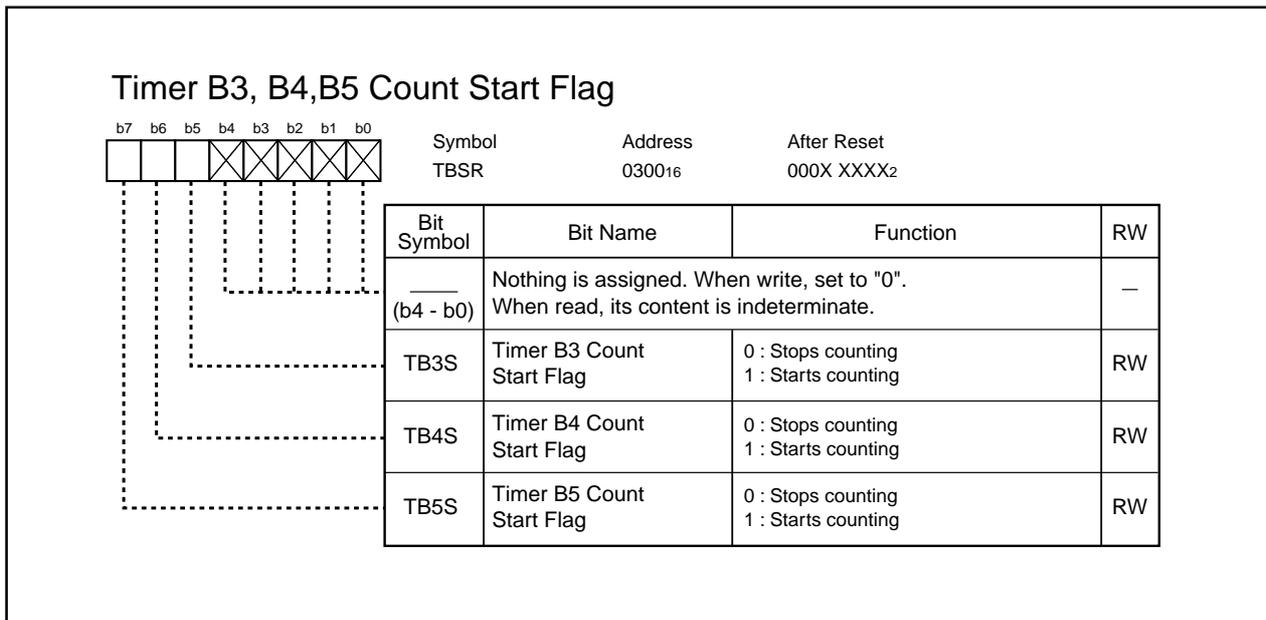


Figure 15.18 TB0MR to TB5MR Registers, TABSR Register

**Figure 15.19 TBSR Register****Table 15.8 Settings for the TB*i*IN Pins (i=0 to 5)**

Port Name	Function	Setting	
		PS1, PS3 ⁽¹⁾ Registers	PD7, PD9 ⁽¹⁾ Registers
P90	TB0IN	PS3_0=0	PD9_0=0
P91	TB1IN	PS3_1=0	PD9_1=0
P92	TB2IN	PS3_2=0	PD9_2=0
P93	TB3IN	PS3_3=0	PD9_3=0
P94	TB4IN	PS3_4=0	PD9_4=0
P71	TB5IN	PS1_1=0	PD7_1=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

15.2.1 Timer Mode

In timer mode, the timer counts an internally generated count source (see **Table 15.9**). Figure 15.20 shows the TBiMR register (i=0 to 5) in timer mode.

Table 15.9 Timer Mode Specifications

Item	Specification
Count Source	f1, f8, f2n ⁽¹⁾ , fc32
Counting Operation	<ul style="list-style-type: none"> The timer decrements a counter value When the timer counter underflows, content of the reload register is reloaded into the count register and counting resumes
Divide Ratio	$1/(n+1)$ <i>n</i> : setting value of the TBi register (i=0 to 5) 0000 ₁₆ to FFFF ₁₆
Counter Start Condition	The TBiS bits in the TABSR and TBSR registers are set to "1" (starts counting)
Counter Stop Condition	The TBiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	Timer counter underflows
TBiIn Pin Function	Programmable I/O port
Read from Timer	The TBi register indicates counter value
Write to Timer	<ul style="list-style-type: none"> When the timer counter stops, the value written to the TBi register is also written to both reload register and counter While counting, the value written to the TBi register is written to the reload register (It is transferred to the counter at the next reload timing)

NOTES:

- The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

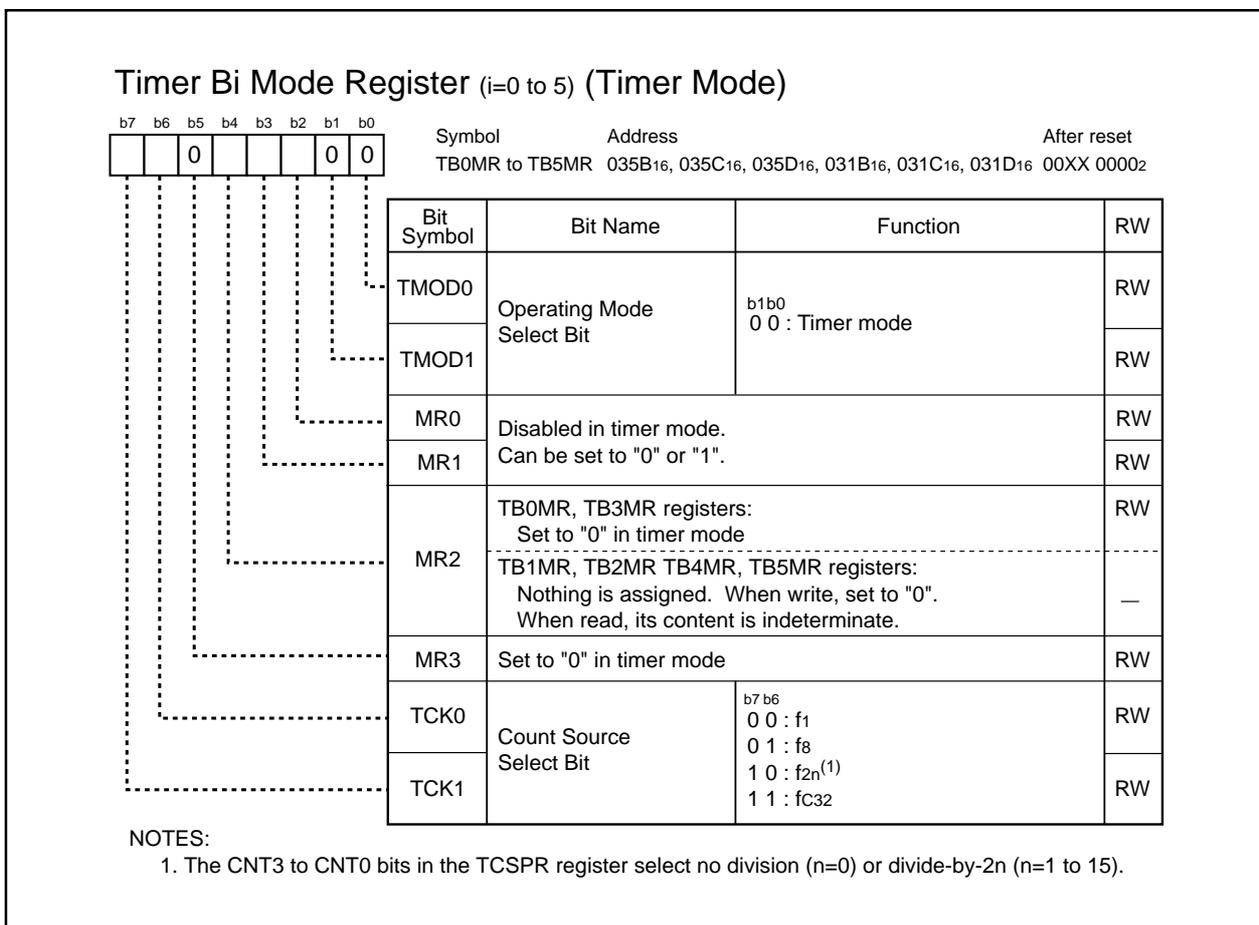


Figure 15.20 TB0MR to TB5MR Registers

15.2.2 Event Counter Mode

In event counter mode, the timer counts how many external signals are applied or how many times another timer overflows and underflows. (See **Table 15.10**) Figure 15.21 shows the TBiMR register (i=0 to 5) in event counter mode.

Table 15.10 Event Counter Mode Specifications

Item	Specification
Count Source	<ul style="list-style-type: none"> External signal applied to the TBiIN pin (i = 0 to 5) (valid edge can be selected by program) TBj overflow or underflow signal (j=i-1, except j=2 when i=0, j=5 when i=3)
Counting Operation	<ul style="list-style-type: none"> The timer decrements a counter value <p>When the timer counter underflows, content of the reload register is reloaded into the count register to continue counting</p>
Divide Ratio	$1/(n+1)$ n : setting value of the TBi register 0000 ₁₆ to FFFF ₁₆
Counter Start Condition	The TBiS bits in the TABSR and TBSR register are set to "1" (starts counting)
Counter Stop Condition	The TBiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	The timer counter underflows
TBiIN Pin Function	Programmable I/O port or count source input
Read from Timer	The TBi register indicates counter value
Write to Timer	<ul style="list-style-type: none"> When the timer counter stops, the value written to the TBi register is also written to both reload register and counter While counting, the value written to the TBi register is written to the reload register (It is transferred to the counter at the next reload timing)

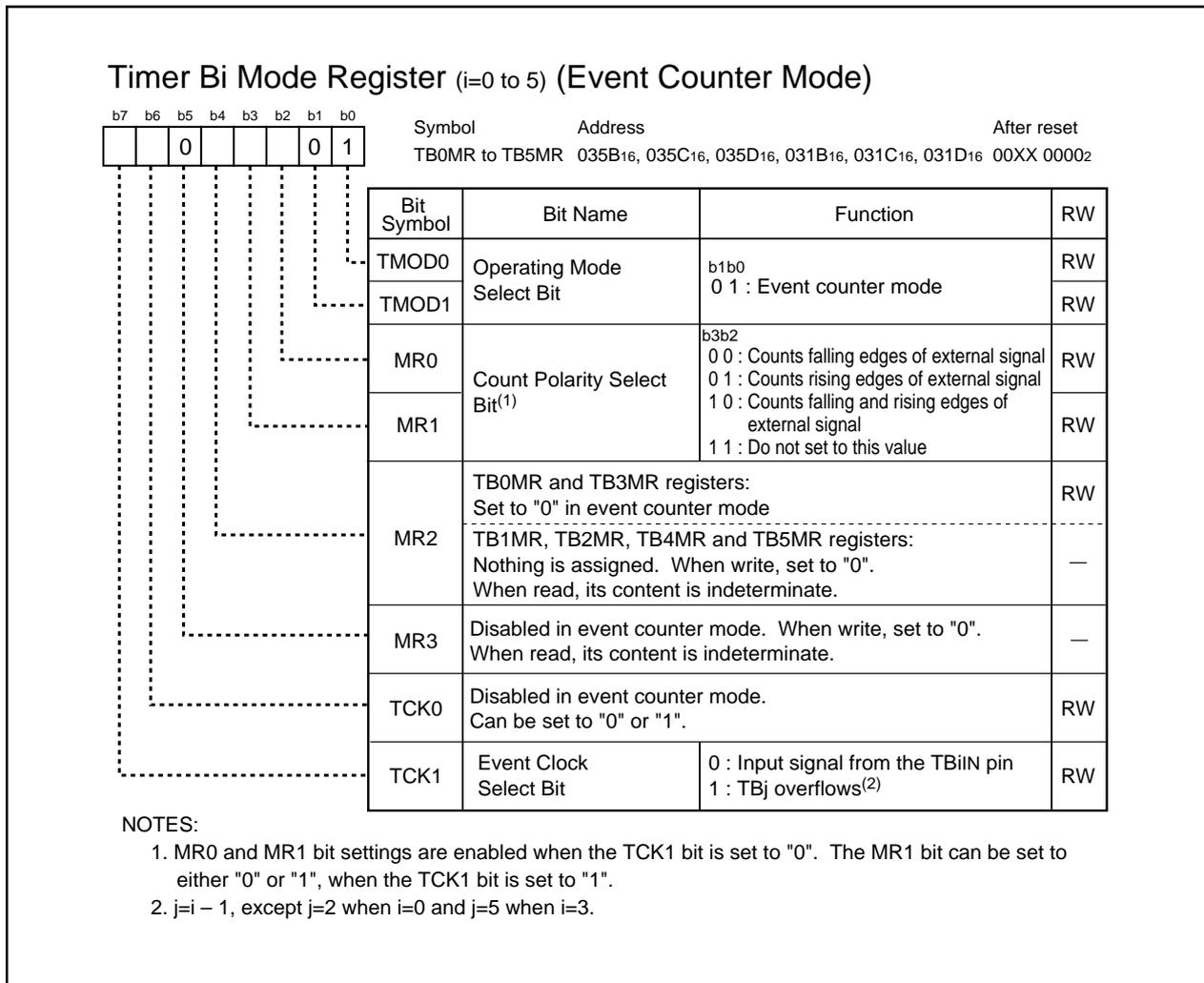


Figure 15.21 TB0MR to TB5MR Registers

15.2.3 Pulse Period/Pulse Width Measurement Mode

In pulse period/pulse width measurement mode, the timer measures pulse period or pulse width of an external signal. (See **Table 15.11**) Figure 15.22 shows the TBiMR register (i=0 to 5) in pulse period/pulse width measurement mode. Figure 15.23 shows an operation example in pulse period measurement mode. Figure 15.24 shows an operation example in the pulse width measurement mode.

Table 15.11 Pulse Period/Pulse Width Measurement Mode Specifications

Item	Specification
Count Source	f1, f8, f2n ⁽³⁾ , fc32
Counting Operation	<ul style="list-style-type: none"> The timer increments a counter value Counter value is transferred to the reload register on the valid edge of a pulse to be measured. It is set to "000016" and the timer continues counting
Counter Start Condition	The TBiS bits (i=0 to 5) in the TABSR and TBSR register are set to "1" (starts counting)
Counter Stop Condition	The TBiS bit is set to "0" (stops counting)
Interrupt Request Generation Timing	<ul style="list-style-type: none"> On the valid edge of a pulse to be measured⁽¹⁾ The timer counter overflows The MR3 bit in the TBiMR register is set to "1" (overflow) simultaneously. When the TBiS bit is set to "1" (start counting) and the next count source is counted after setting the MR3 bit to "1" (overflow), the MR3 bit can be set to "0" (no overflow) by writing to the TBiMR register.
TBiIN Pin Function	Input for a pulse to be measured
Read from Timer	The TBi register indicates reload register values (measurement results) ⁽²⁾
Write to Timer	Value written to the TBi register can be written to neither reload register nor counter

NOTES:

- No interrupt request is generated when the pulse to be measured is on the first valid edge after the timer has started counting.
- The TBi register is in an indeterminate state until the pulse to be measured is on the second valid edge after the timer has started counting.
- The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

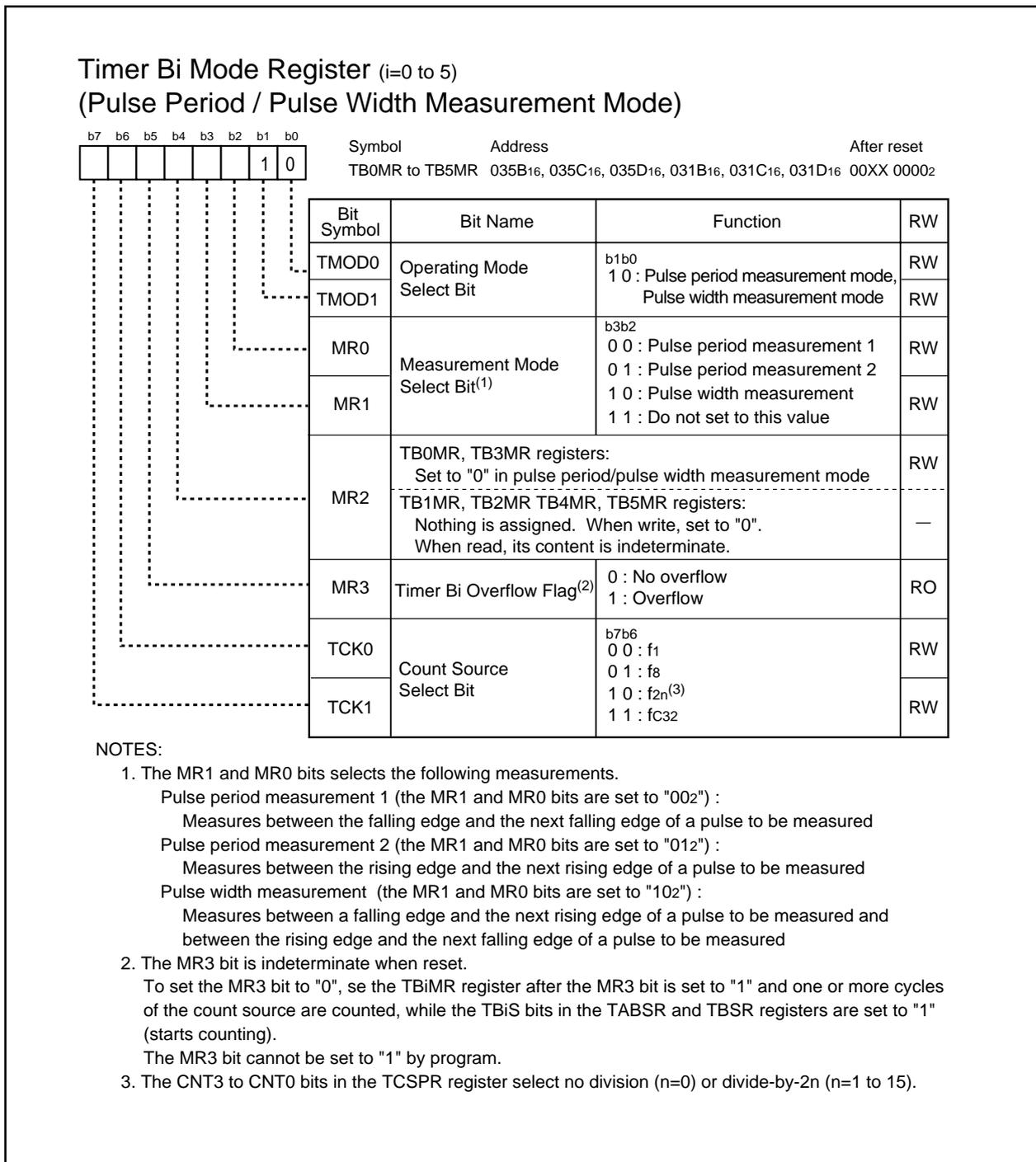


Figure 15.22 TB0MR to TB5MR Registers

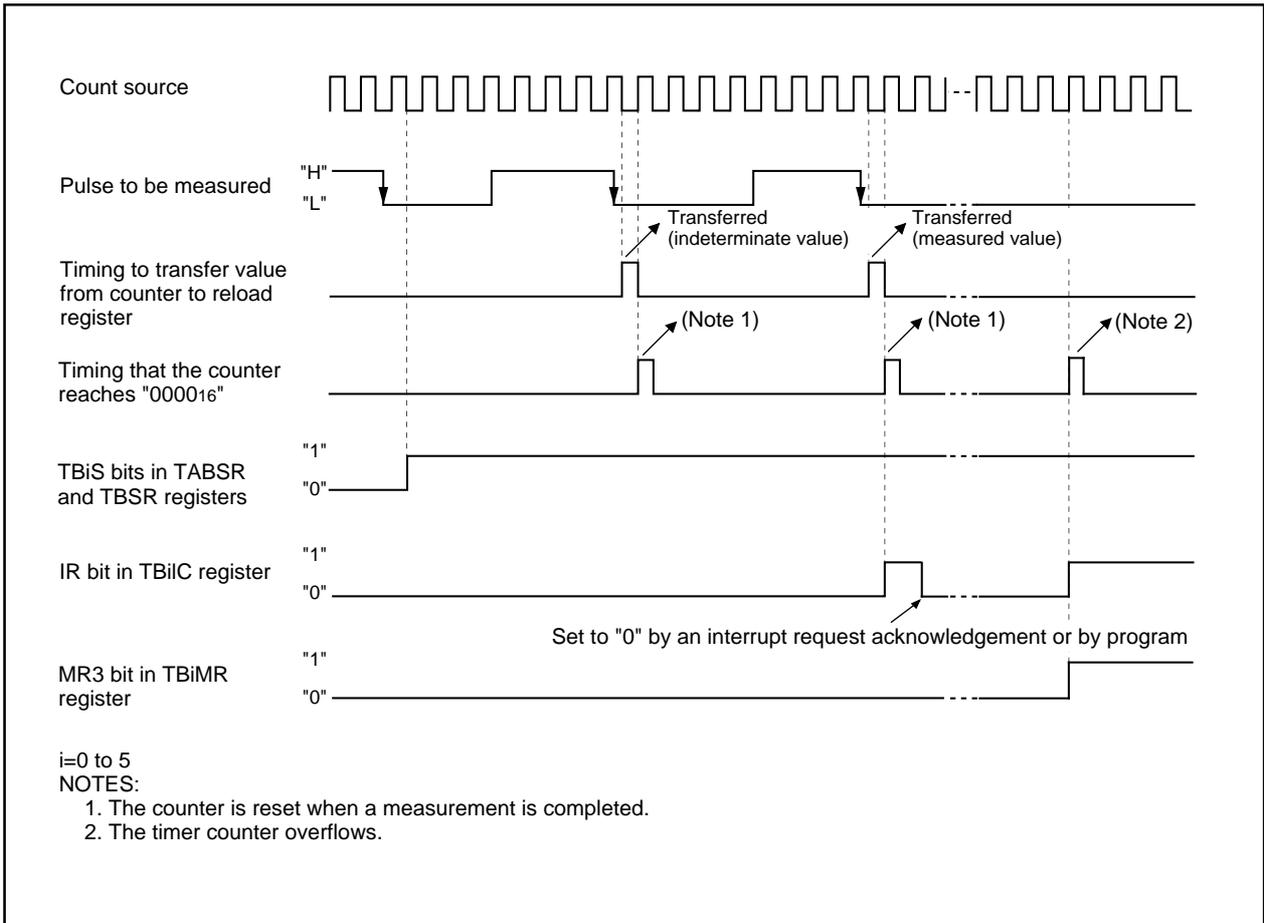


Figure 15.23 Operation Example in Pulse Period Measurement Mode

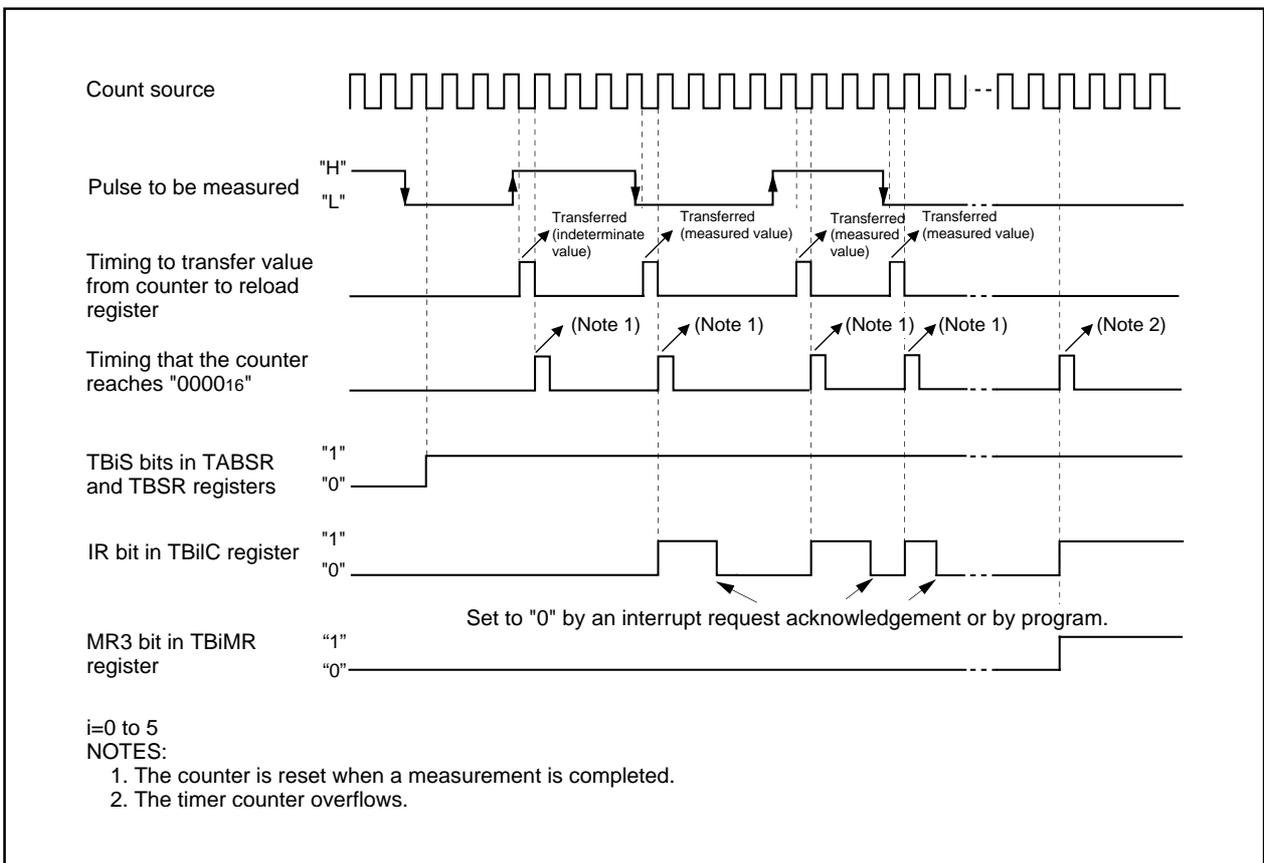


Figure 15.24 Operation Example in Pulse Width Measurement Mode

16. Three-Phase Motor Control Timer Functions

Three-phase motor driving waveform can be output by using the timers A1, A2, A4 and B2. Table 16.1 lists specifications of the three-phase motor control timer functions. Table 16.2 lists pin settings. Figure 16.1 shows a block diagram. Figures 16.2 to 16.7 show registers associated with the three-phase motor control timer functions.

Table 16.1 Three-Phase Motor Control Timer Functions Specification

Item	Specification
Three-Phase Waveform Output Pin	Six pins (U, \bar{U} , V, \bar{V} , W, \bar{W})
Forced Cutoff ⁽¹⁾	Apply a low-level ("L") signal to the NMI pin
Timers to be Used	Timer A4, A1, A2 (used in one-shot timer mode): Timer A4: U- and \bar{U} -phase waveform control Timer A1: V- and \bar{V} -phase waveform control Timer A2: W- and \bar{W} -phase waveform control Timer B2 (used in timer mode): Carrier wave cycle control Dead time timer (three 8-bit timers share reload register): Dead time control
Output Waveform	Triangular wave modulation, Sawtooth wave modulation Can output a high-level waveform or a low-level waveform for one cycle; Can set positive-phase level and negative-phase level separately
Carrier Wave Cycle	Triangular wave modulation: $count\ source \times (m+1) \times 2$ Sawtooth wave modulation: $count\ source \times (m+1)$ m : setting value of the TB2 register, 0000 ₁₆ to FFFF ₁₆ Count source: f ₁ , f ₈ , f _{2n} ⁽²⁾ , f _{c32}
Three-Phase PWM Output Width	Triangular wave modulation: $count\ source \times n \times 2$ Sawtooth wave modulation: $count\ source \times n$ n : setting value of the TA4, TA1 and TA2 register (of the TA4, TA41, TA1, TA11, TA2 and TA21 registers when setting the INV11 bit to "1"), 0001 ₁₆ to FFFF ₁₆ Count source: f ₁ , f ₈ , f _{2n} ⁽²⁾ , f _{c32}
Dead Time	$Count\ source \times p$, or no dead time p : setting value of the DTT register, 01 ₁₆ to FF ₁₆ Count source: f ₁ , or f ₁ divided by 2
Active Level	Selected from a high level ("H") or low level ("L")
Positive- and Negative-Phase Concurrent Active Disable Function	Positive and negative-phases concurrent active disable function Positive and negative-phases concurrent active detect function
Interrupt Frequency	For the timer B2 interrupt, one carrier wave cycle-to-cycle basis through 15 time- carrier wave cycle-to-cycle basis can be selected

NOTES:

1. Forced cutoff by the signal applied to the \bar{NMI} pin is available when the INV02 bit is set to "1" (three-phase motor control timer functions) and the INV03 bit is set to "1" (three-phase motor control timer output enabled).
2. The CNT3 to CNT0 bits in the TCSPPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Table 16.2 Pin Settings

Pin	Setting		
	PS1, PS2 Registers ⁽¹⁾	PSL1, PSL2 Registers	PSC Register
P72/V	PS1_2 =1	PSL1_2 =0	PSC_2 =1
P73/ \bar{V}	PS1_3 =1	PSL1_3 =1	PSC_3 =0
P74/W	PS1_4 =1	PSL1_4 =1	PSC_4 =0
P75/ \bar{W}	PS1_5 =1	PSL1_5 =0	—
P80/U	PS2_0 =1	PSL2_0 =1	—
P81/ \bar{U}	PS2_1 =1	PSL2_1 =0	—

NOTES:

1. Set the PS1_5 to PS1_2 bits and PS2_1 and PS2_0 bits in the PS1 and PS2 registers to "1" after the INV02 bit is set to "1".

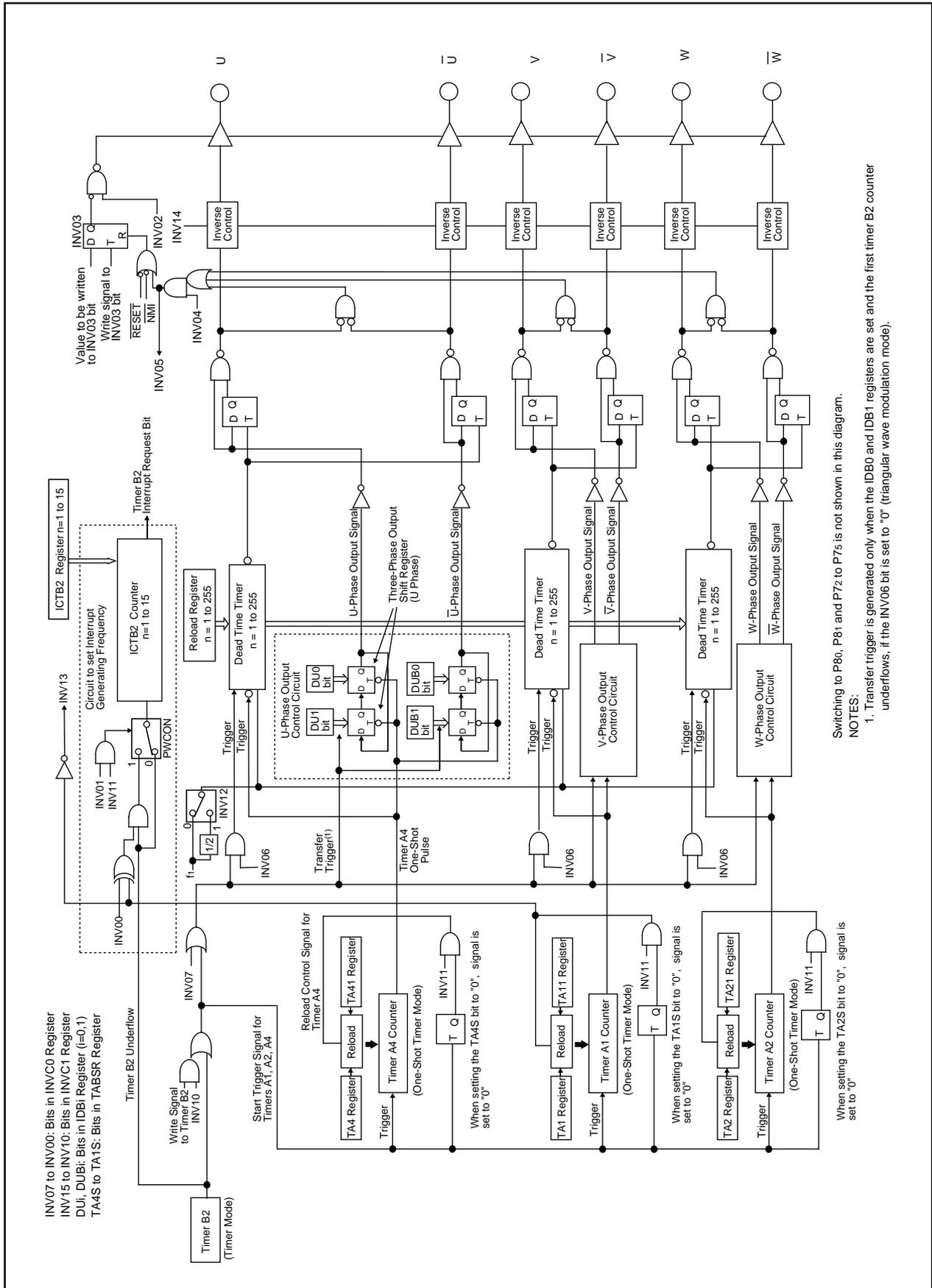


Figure 16.1 Three-Phase Motor Control Timer Functions Block Diagram

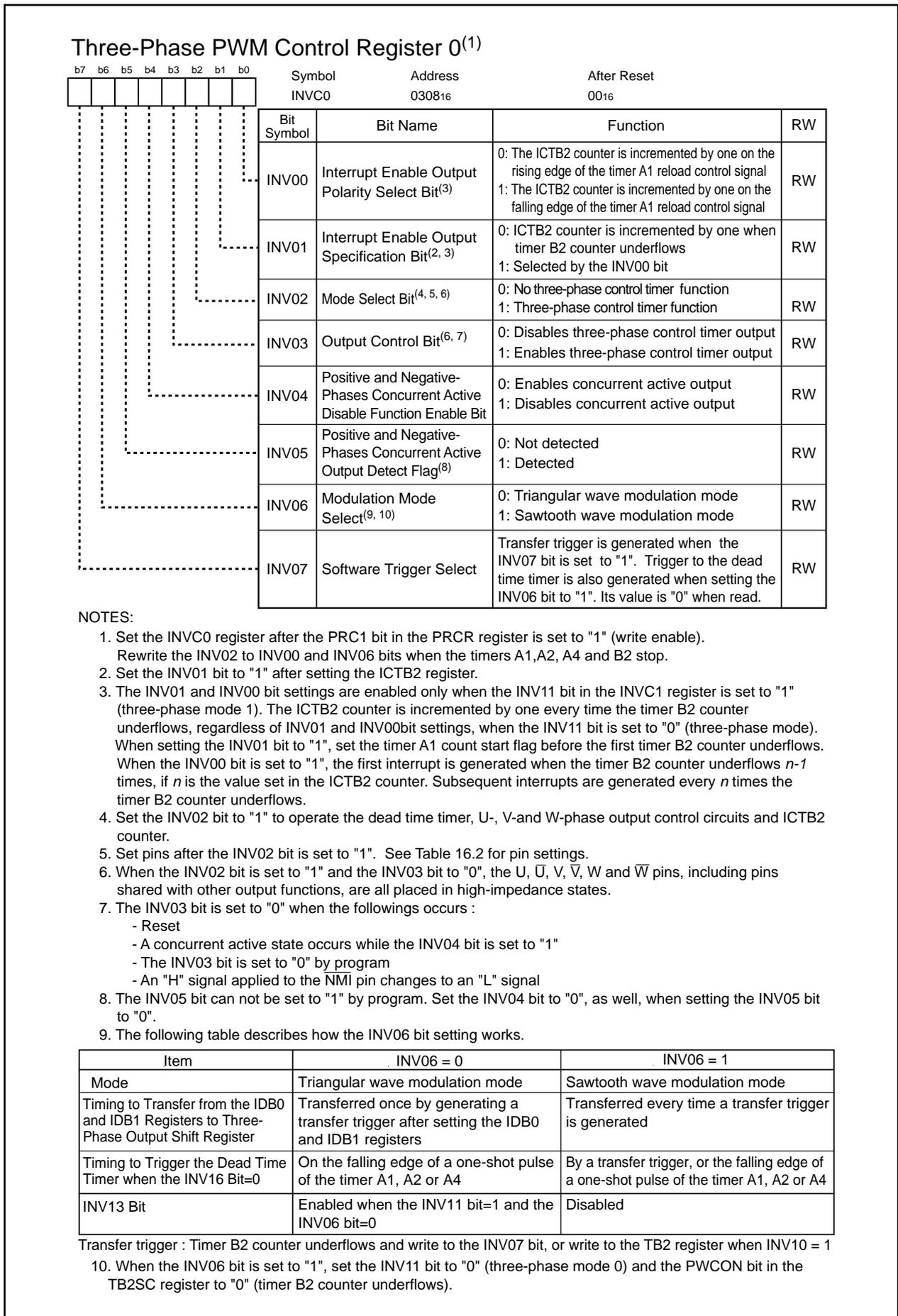


Figure 16.2 INVC0 Register

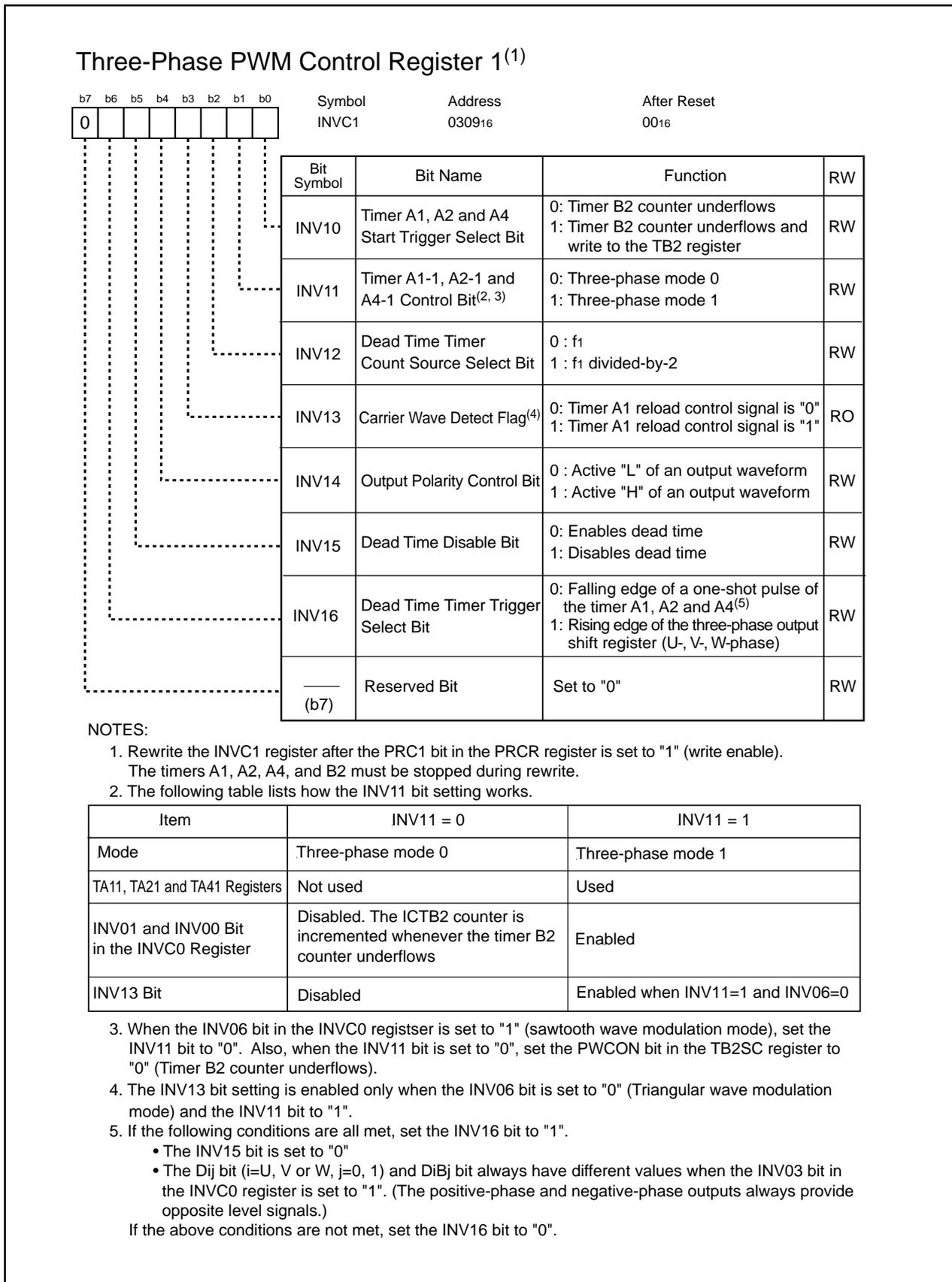


Figure 16.3 INVC1 Register

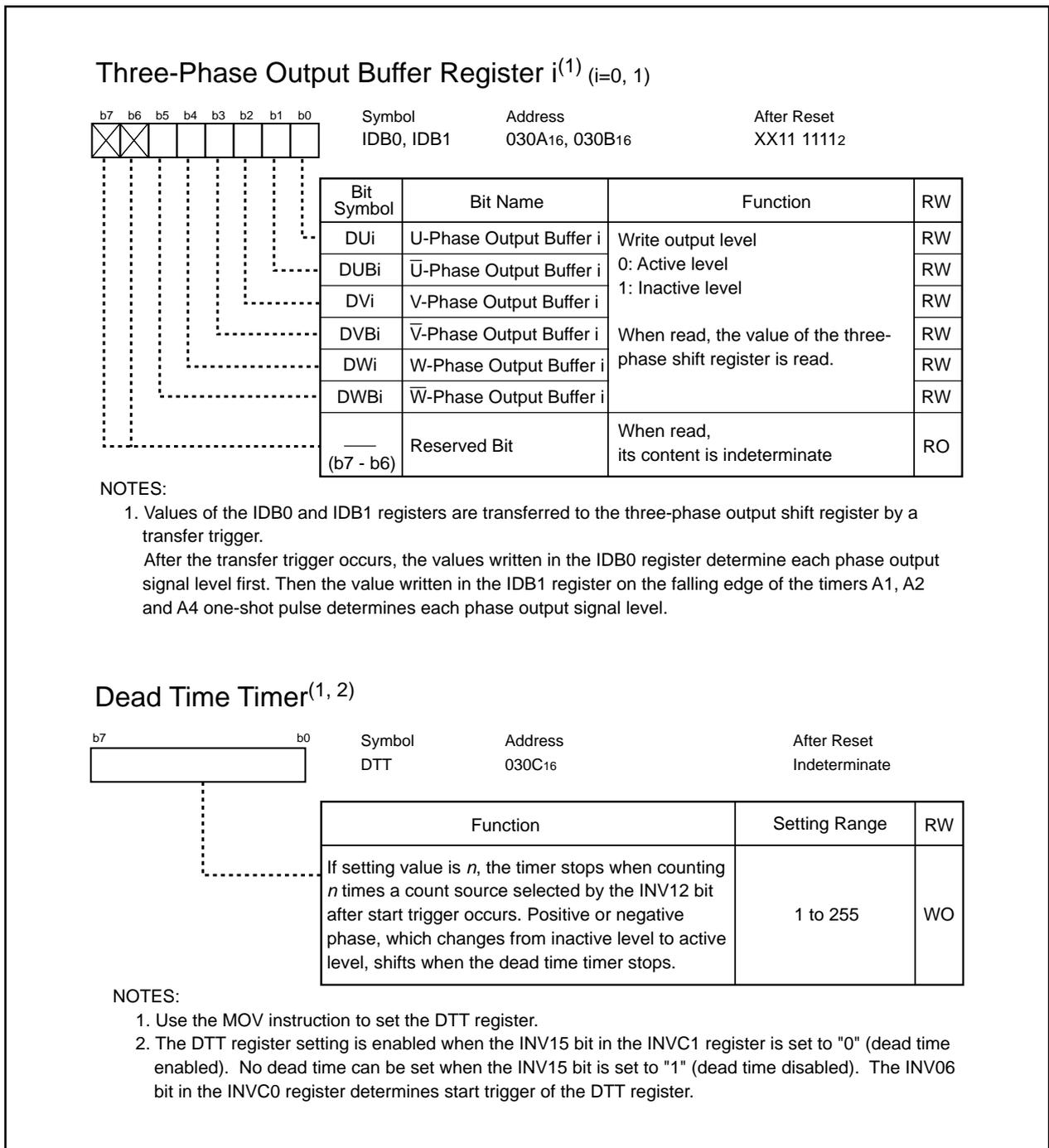


Figure 16.4 IDB0 and IDB1 registers, DTT Register

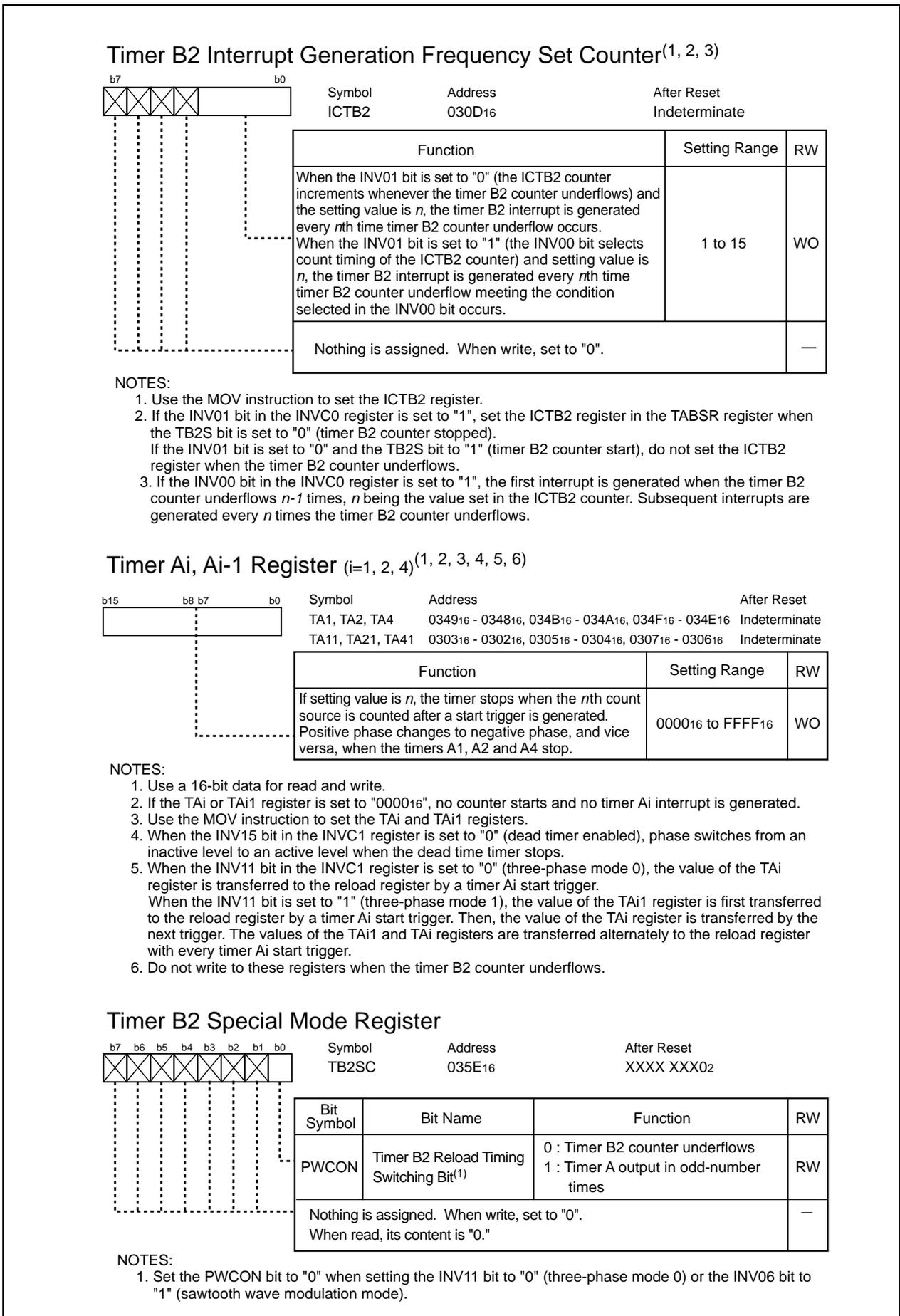


Figure 16.5 ICTB2 Register, TA1, TA2, TA4, TA11, TA21 and TA41 Registers, TB2SC Register

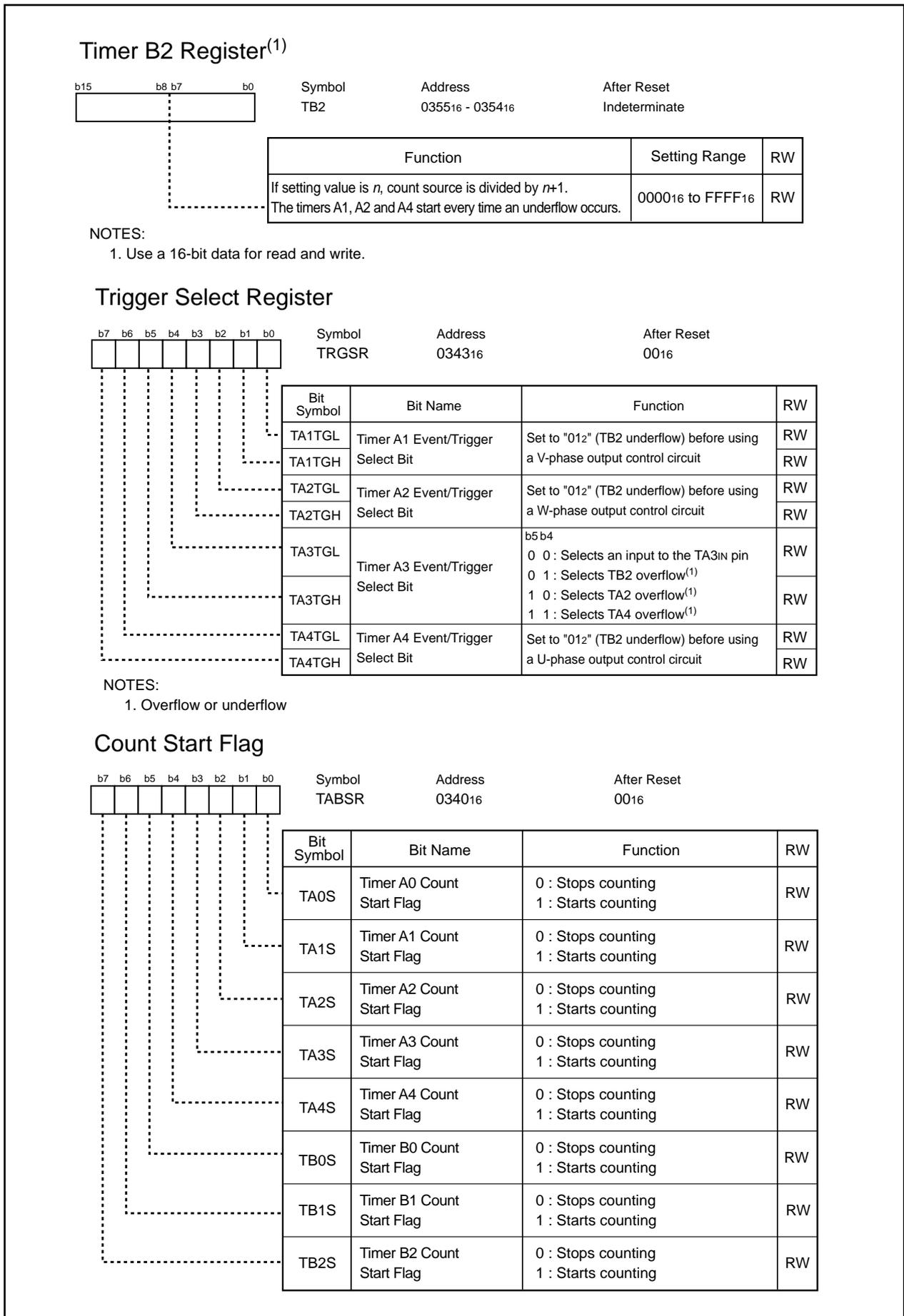


Figure 16.6 TB2, TRGSR and TABSR Registers

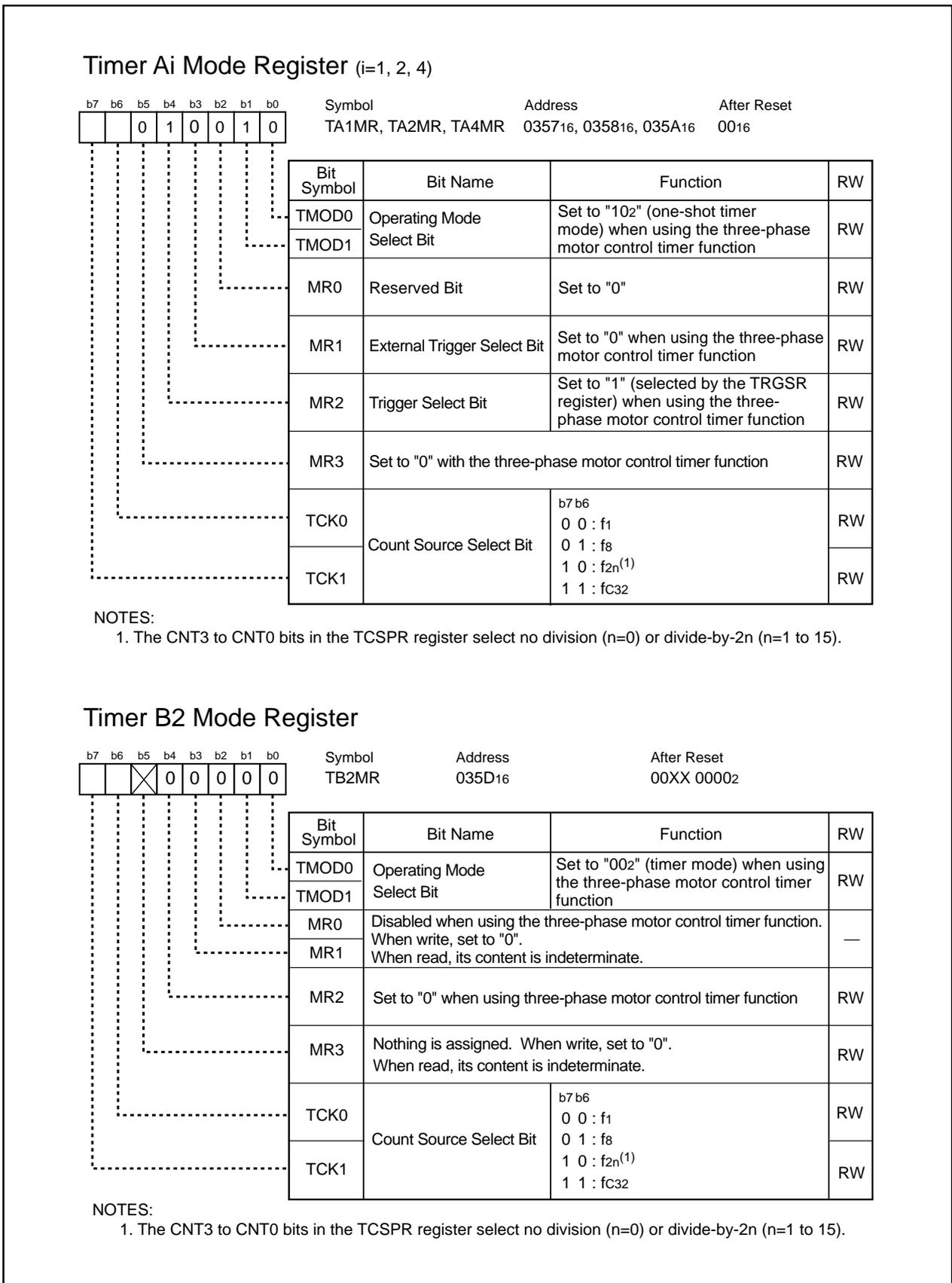


Figure 16.7 TA1MR, TA2MR and TA4MR Registers, TB2MR Register

The three-phase motor control timer function is available by setting the INV02 bit in the INVC0 register to "1". The timer B2 is used for carrier wave control and the timers A1, A2, A4 for three-phase PWM output (U, \bar{U} , V, \bar{V} , W, \bar{W}) control. An exclusive dead time timer controls dead time. Figure 16.8 shows an example of the triangular modulation waveform. Figure 16.9 shows an example of the sawtooth modulation waveform.

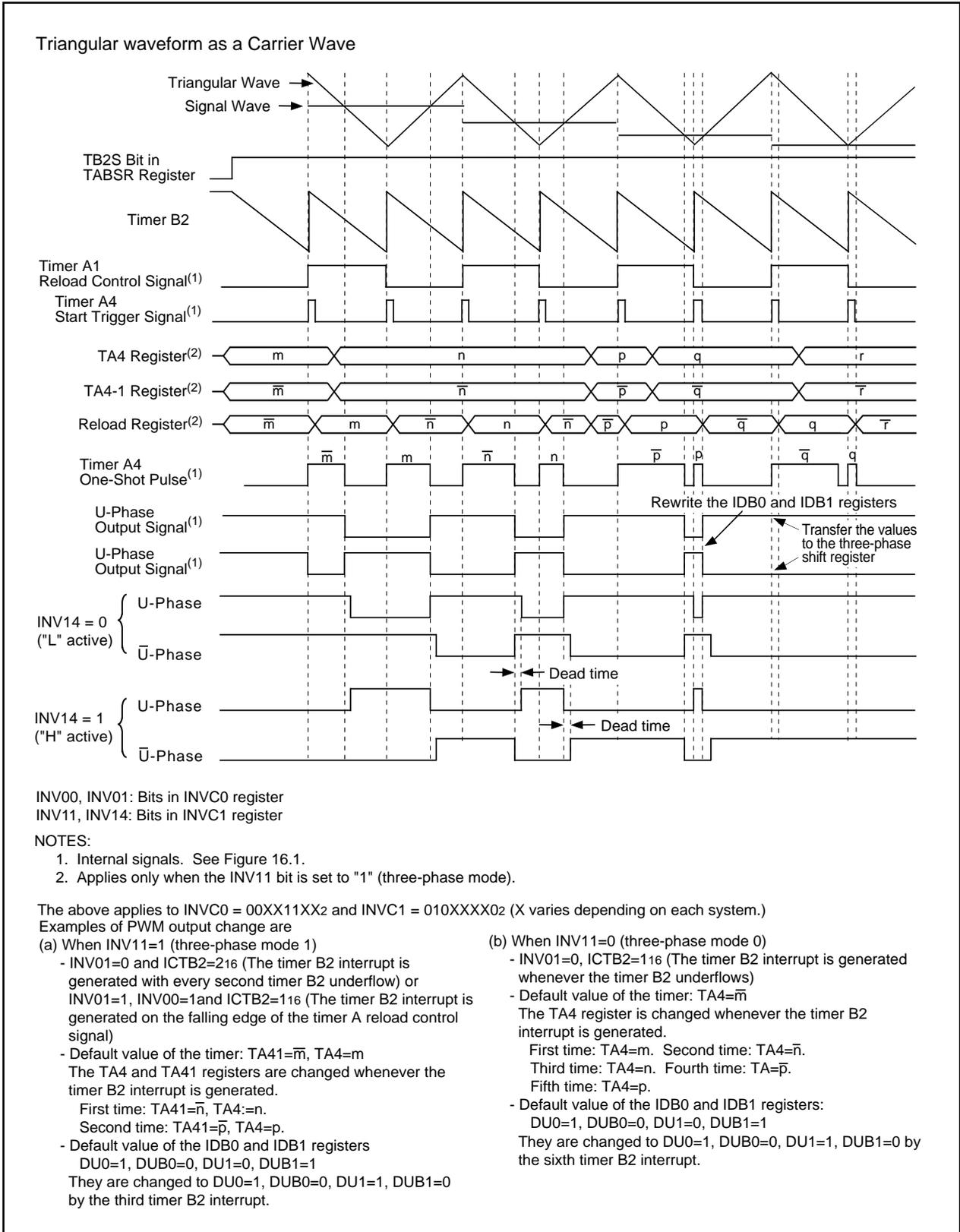


Figure 16.8 Triangular Wave Modulation Operation

17. Serial I/O

Serial I/O consists of five channels (UART0 to UART4).

Each UART_i (i=0 to 4) has an exclusive timer to generate the transfer clock and operates independently.

Figure 17.1 shows a UART_i block diagram.

UART_i supports the following modes :

- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode)
- Special mode 1 (I²C mode)
- Special mode 2
- Special mode 3 (Clock-divided synchronous function, GCI mode)
- Special mode 4 (Bus conflict detect function, IE mode)
- Special mode 5 (SIM mode)

Figures 17.2 to 17.9 show registers associated with UART_i.

Refer to the tables listing each mode for register and pin settings.

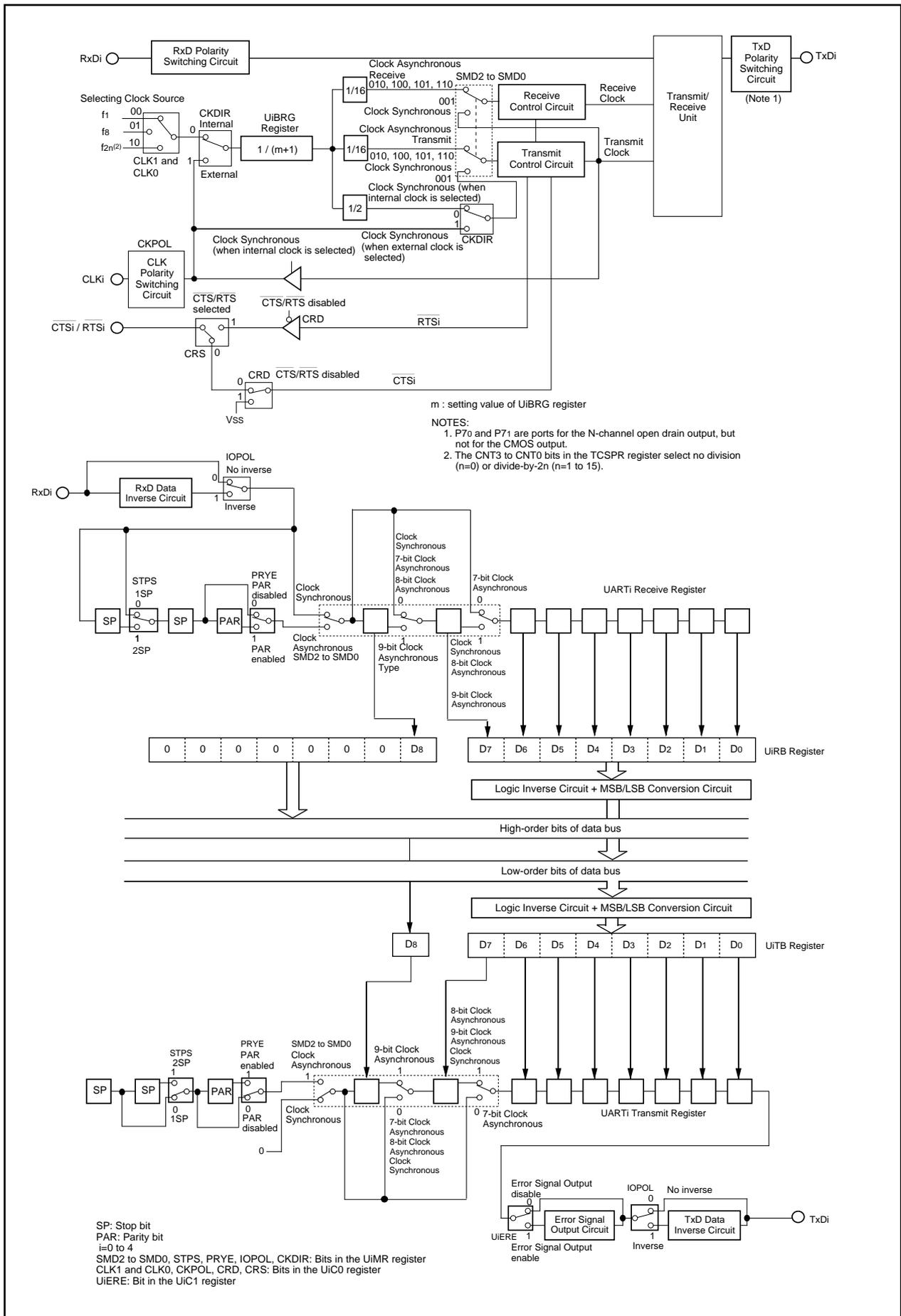


Figure 17.1 UARTi Block Diagram

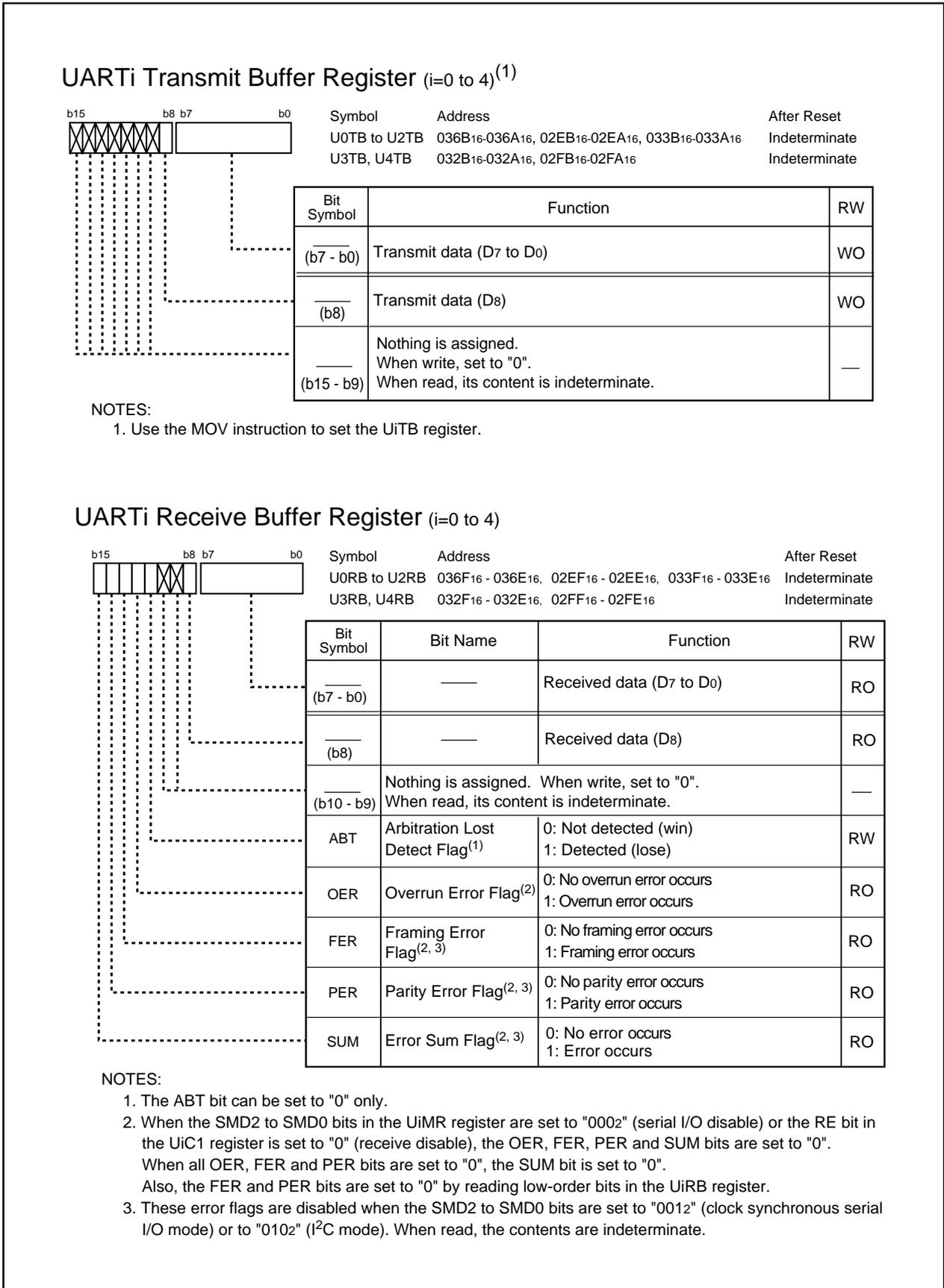


Figure 17.2 U0TB to U4TB Registers and U0RB to U4RB Registers

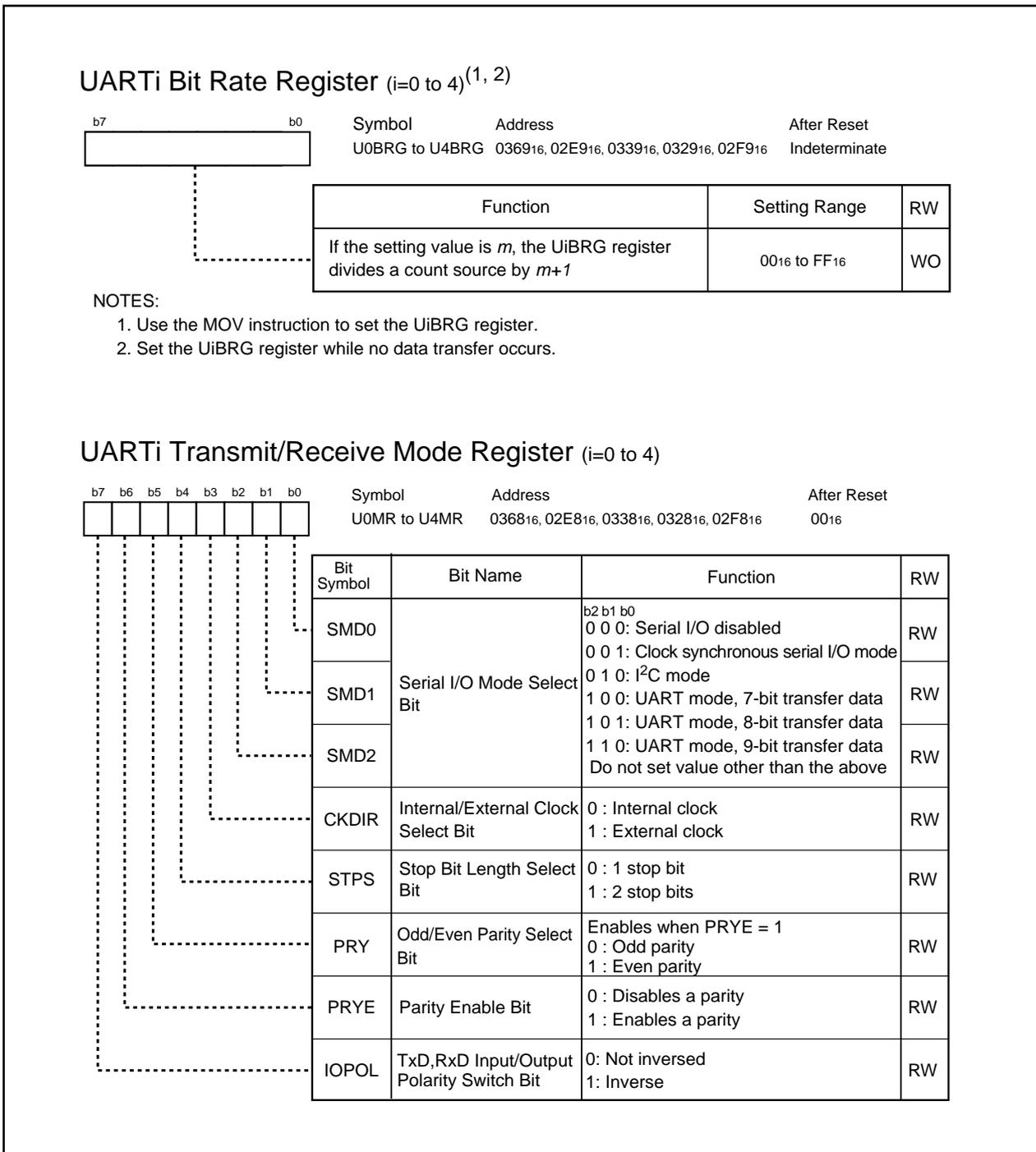


Figure 17.3 U0BRG to U4BRG Registers and U0MR to U4MR Registers

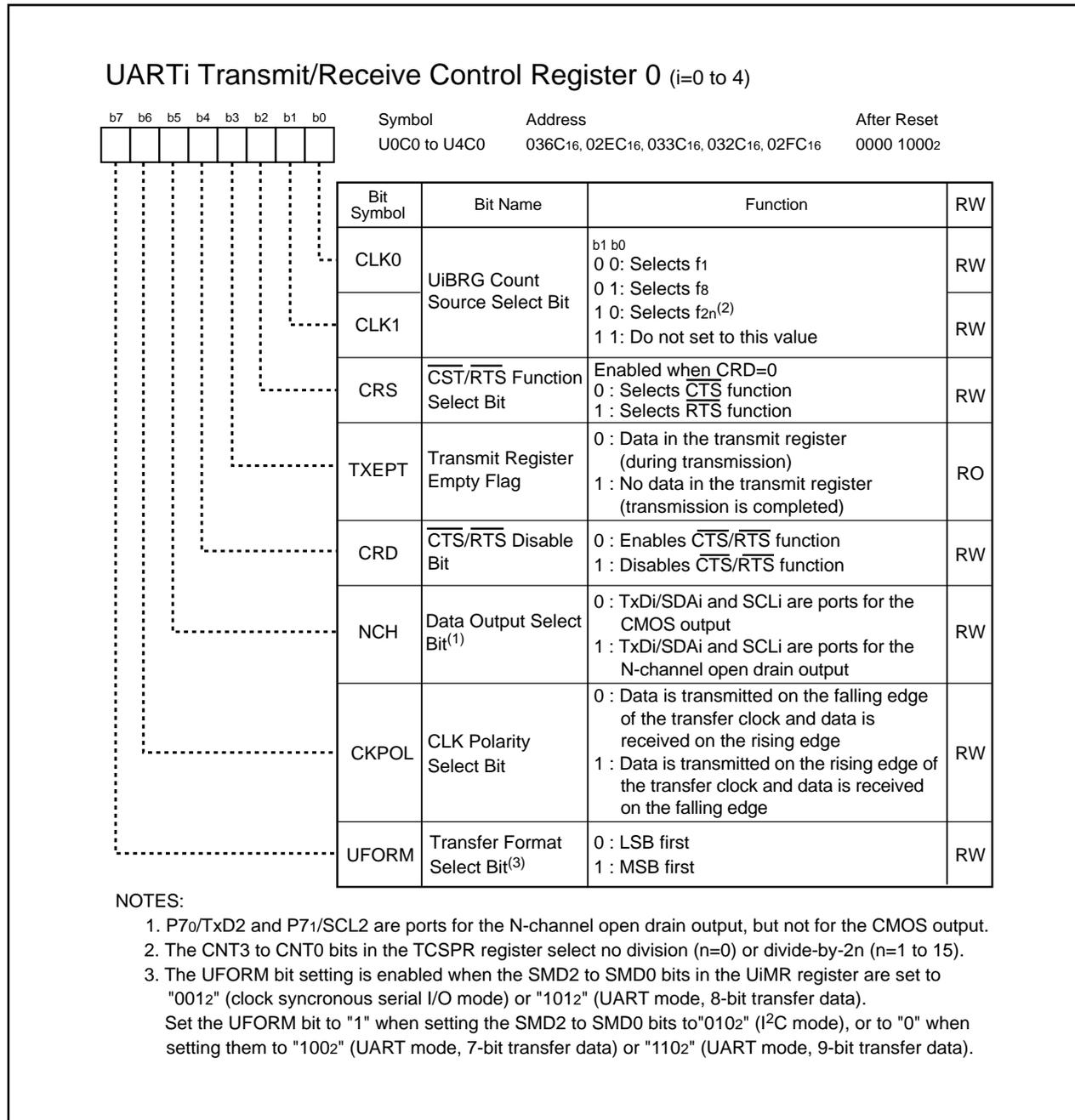


Figure 17.4 U0C0 to U4C0 Registers

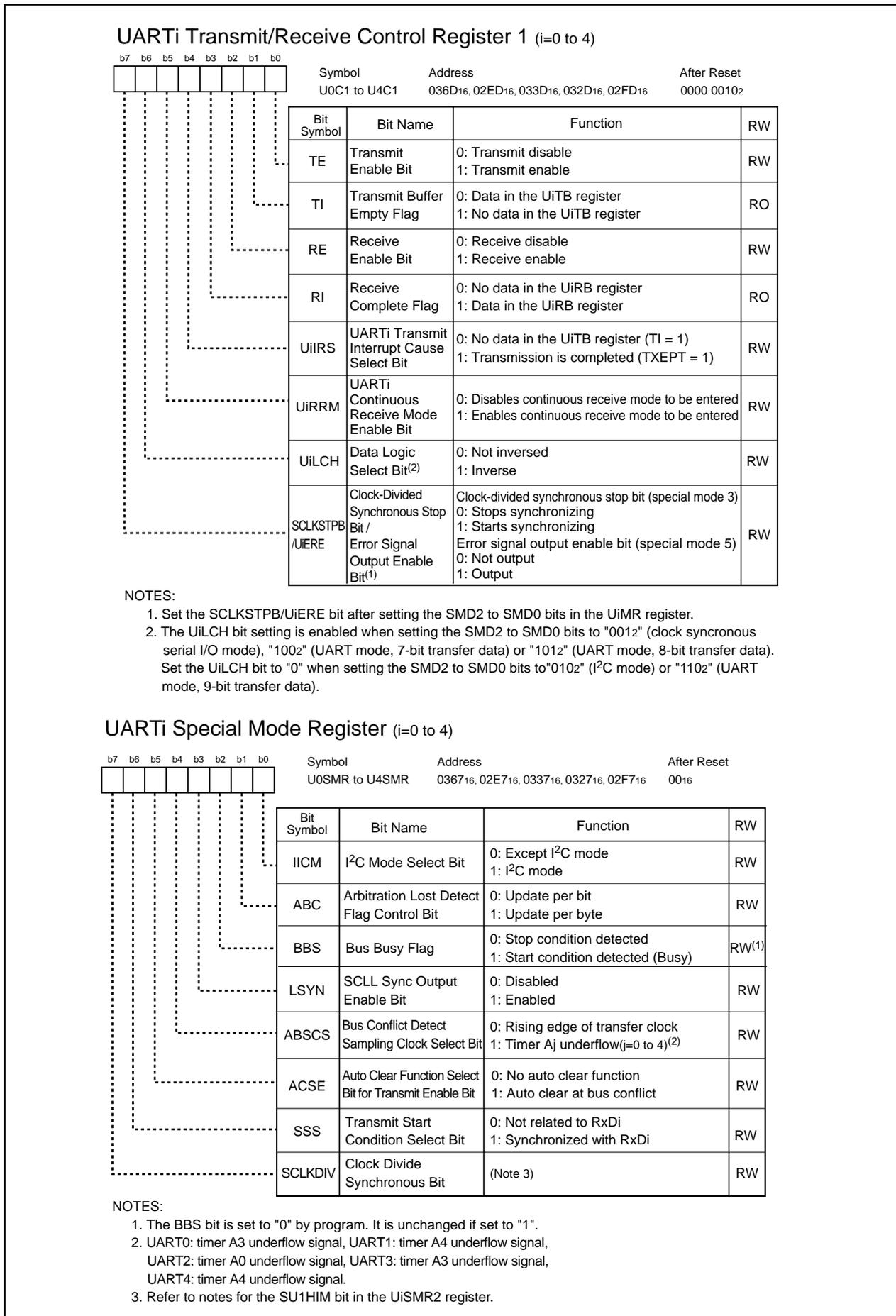


Figure 17.5 U0C1 to U4C1 Registers and U0SMR to U4SMR Registers

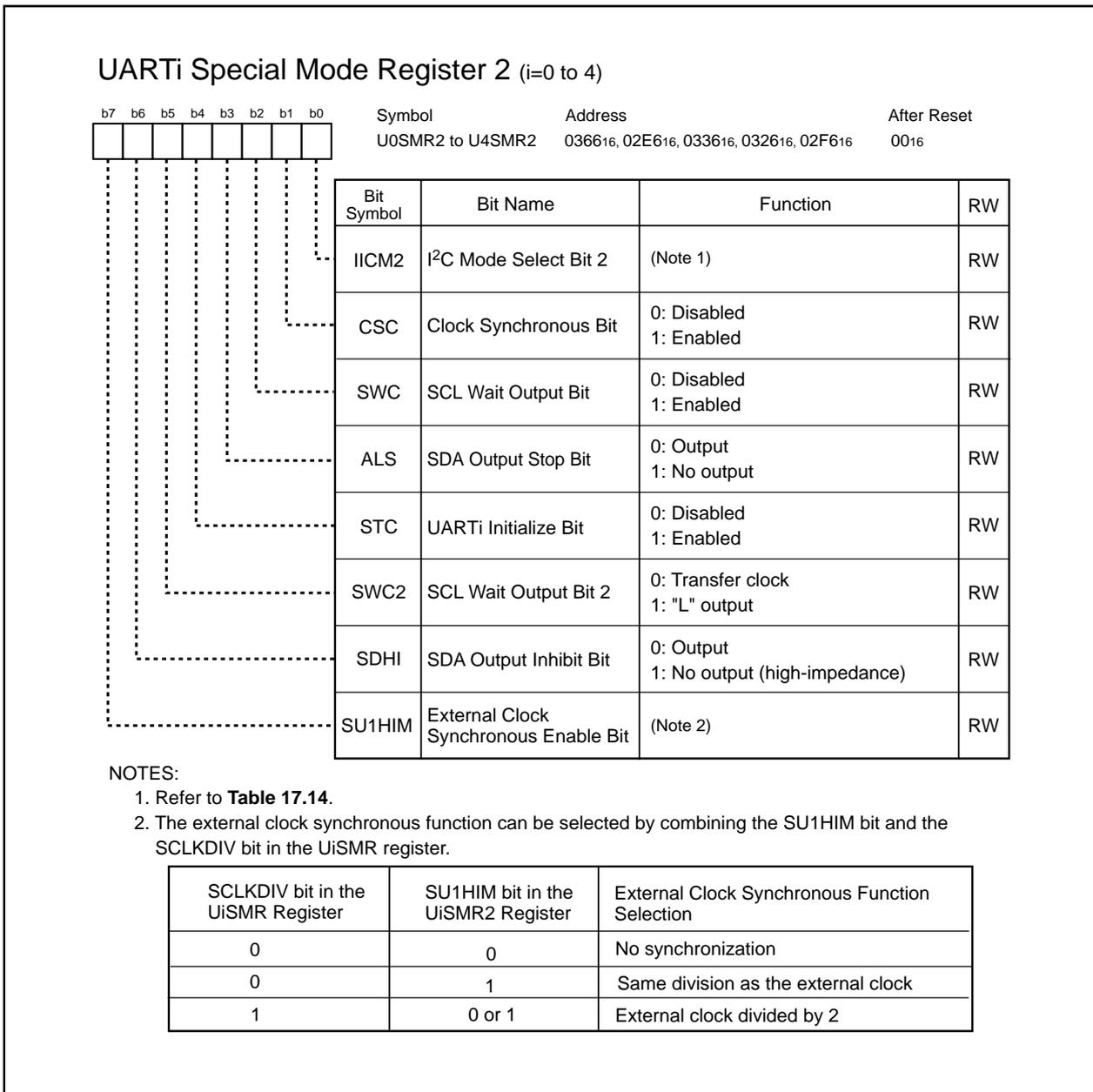


Figure 17.6 U0SMR2 to U4SMR2 Registers

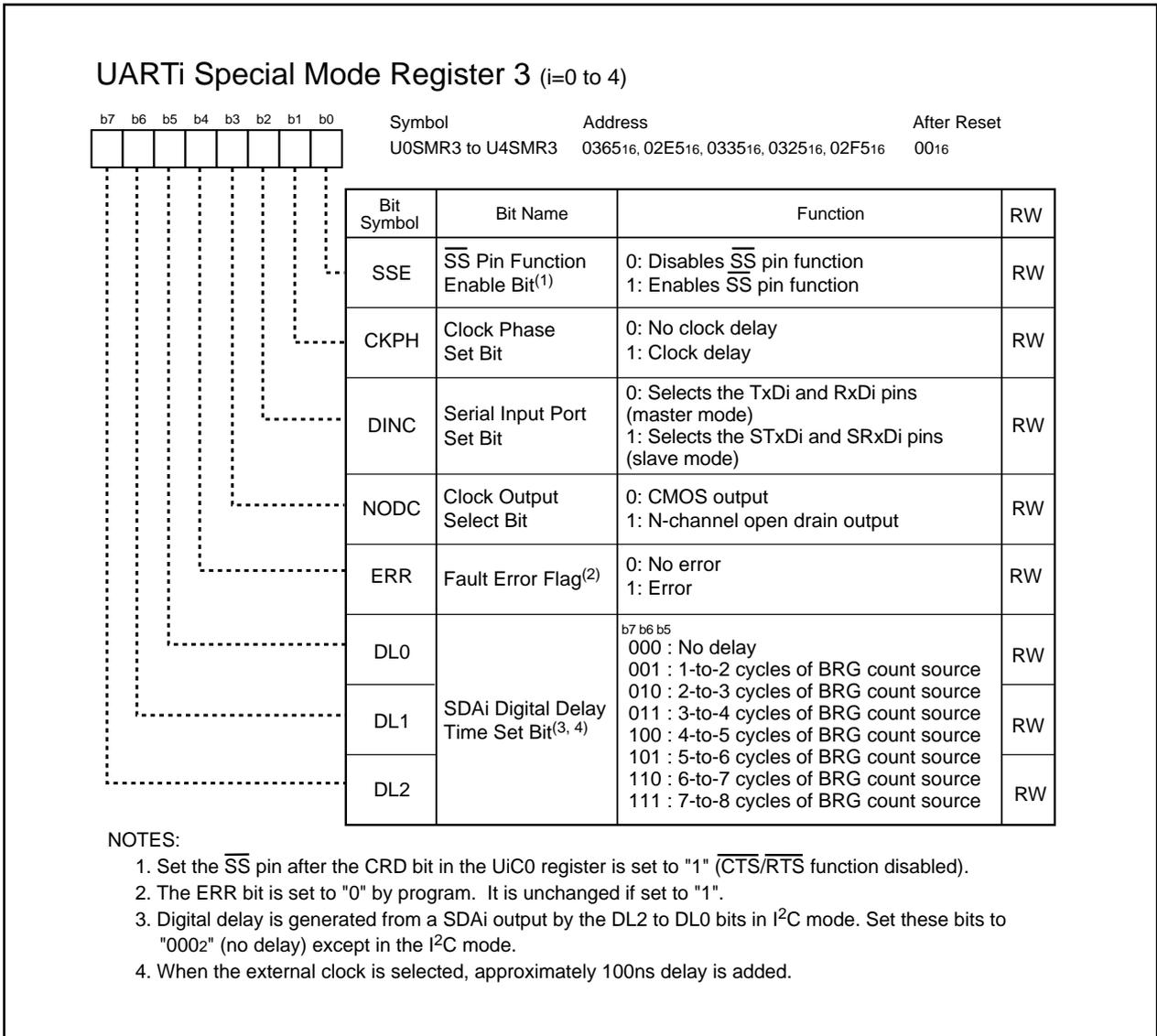


Figure 17.7 U0SMR3 to U4SMR3 Registers

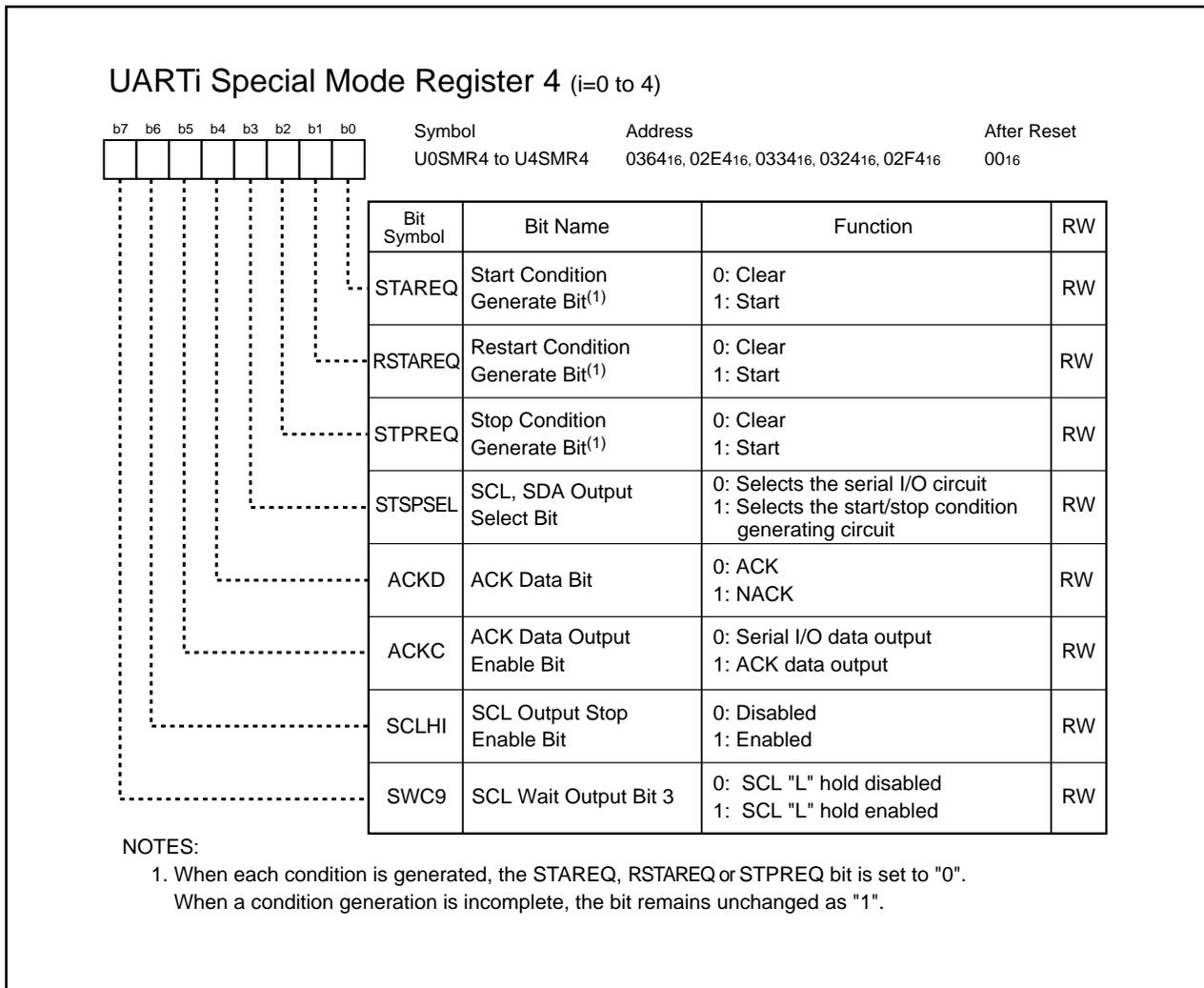


Figure 17.8 U0SMR4 to U4SMR4 Registers

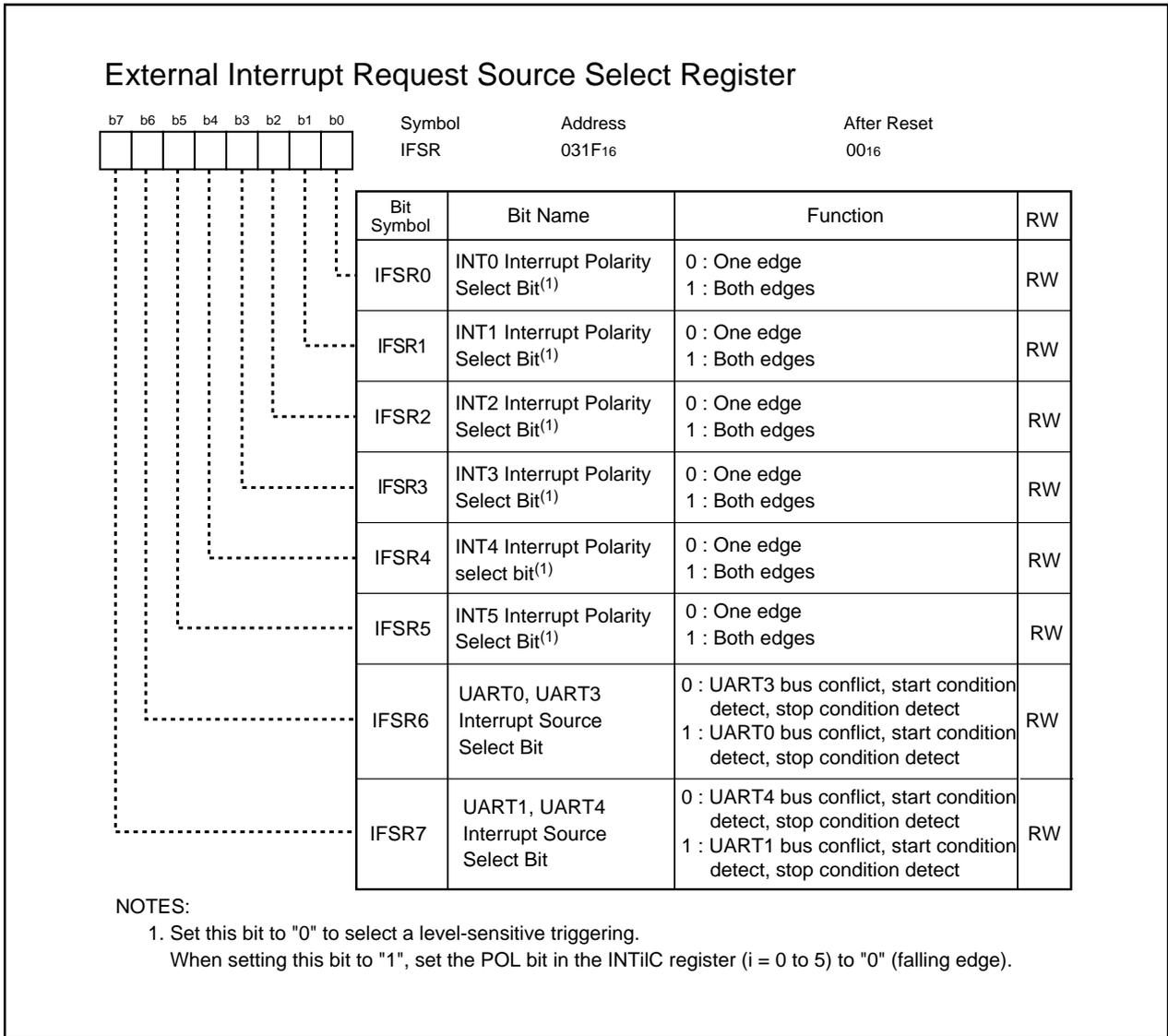


Figure 17.9 IFSR Register

17.1 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received with the transfer clock. Table 17.1 lists specifications of clock synchronous serial I/O mode. Table 17.2 lists register settings. Tables 17.3 to 17.5 list pin settings. When UART_i (i=0 to 4) operating mode is selected, the Tx_{Di} pin outputs a high-level ("H") signal before transfer starts (the Tx_{Di} pin is in a high-impedance state when the N-channel open drain output is selected). Figure 17.10 shows transmit and receive timings in clock synchronous serial I/O mode.

Table 17.1 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer Data Format	Transfer data : 8 bits long
Transfer Clock	<ul style="list-style-type: none"> The CKDIR bit in the UiMR register (i=0 to 4) is set to "0" (internal clock selected): $\frac{f}{2^{(m+1)}} \quad f=f_1, f_8, f_{2^n} \quad m:\text{setting value of the UiBRG register, } 00_{16} \text{ to } FF_{16}$ The CKDIR bit is set to "1" (external clock selected) : an input from the CLK_i pin
Transmit/Receive Control	Selected from the CTS function, RTS function or CTS/RTS function disabled
Transmit Start Condition	To start transmitting, the following requirements must be met ⁽²⁾ : <ul style="list-style-type: none"> - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the TI bit in the UiC1 register to "0" (data in the UiTB register) - Apply a low-level ("L") signal to the CTS_i pin when the CTS function is selected
Receive Start Condition	To start receiving, the following requirements must be met ⁽²⁾ : <ul style="list-style-type: none"> - Set the RE bit in the UiC1 register to "1" (receive enable) - Set the TE bit to "1" (transmit enable) - Set the TI bit to "0" (data in the UiTB register)
Interrupt Request Generation Timing	<ul style="list-style-type: none"> • While transmitting, the following conditions can be selected: <ul style="list-style-type: none"> - The UiIRS bit in the UiC1 register is set to "0" (no data in the transmit buffer): when data is transferred from the UiTB register to the UART_i transmit register (transfer started) - The UiIRS bit is set to "1" (transmission completed): when a data transfer from the UART_i transmit register is completed • While receiving When data is transferred from the UART_i receive register to the UiRB register (reception completed)
Error Detect	Overrun error ⁽³⁾ This error occurs when the seventh bit of the next received data is read before reading the UiRB register
Selectable Function	<ul style="list-style-type: none"> • CLK polarity Transferred data output and input are provided on either the rising edge or falling edge of the transfer clock • LSB first or MSB first Data is transmitted or received in either bit 0 or in bit 7 • Continuous receive mode Data can be received simultaneously by reading the UiRB register • Serial data logic inverse This function inverses transmitted/received data logically

NOTES:

1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2ⁿ (n=1 to 15).
2. To start transmission/reception when selecting the external clock, these conditions must be met after the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and data is received on the rising edge) and the CLK_i pin is held "H", or when the CKPOL bit is set to "1" (data is transmitted on the rising edge of the transfer clock and data is received on the falling edge) and the CLK_i pin is held "L".
3. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register does not change to "1" (interrupt requested).

Table 17.2 Register Settings in Clock Synchronous Serial I/O Mode

Register	Bit	Function
UiTB	7 to 0	Set transmit data
UiRB	7 to 0	Received data can be read
	OER	Overrun error flag
UiBRG	7 to 0	Set bit rate
UiMR	SMD2 to SMD0	Set to "0012"
	CKDIR	Select the internal clock or external clock
	IOPOL	Set to "0"
UiC0	CLK1, CLK0	Select count source for the UiBRG register
	CRS	Select $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ when using either
	TXEPT	Transmit register empty flag
	CRD	Enables or disables the CTS or RTS function
	NCH	Select output format of the TxDi pin
	CKPOL	Select transmit clock polarity
	UFORM	Select either LSB first or MSB first
UiC1	TE	Set to "1" to enable data transmission and reception
	TI	Transmit buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select what causes the UARTi transmit interrupt to be generated
	UiRRM	Set to "1" when using continuous receive mode
	UiLCH	Set to "1" when using data logic inverse
	SCLKSTPB	Set to "0"
UiSMR	7 to 0	Set to "0016"
UiSMR2	7 to 0	Set to "0016"
UiSMR3	2 to 0	Set to "0002"
	NODC	Select clock output format
	7 to 4	Set to "00002"
UiSMR4	7 to 0	Set to "0016"

i=0 to 4

Table 17.3 Pin Settings in Clock Synchronous Serial I/O Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	CTS0 input	PS0_0=0	-	PD6_0=0
	RTS0 output	PS0_0=1	-	-
P61	CLK0 input	PS0_1=0	-	PD6_1=0
	CLK0 output	PS0_1=1	-	-
P62	RxD0 input	PS0_2=0	-	PD6_2=0
P63	TxD0 output	PS0_3=1	-	-
P64	CTS1 input	PS0_4=0	-	PD6_4=0
	RTS1 output	PS0_4=1	PSL0_4=0	-
P65	CLK1 input	PS0_5=0	-	PD6_5=0
	CLK1 output	PS0_5=1	-	-
P66	RxD1 input	PS0_6=0	-	PD6_6=0
P67	TxD1 output	PS0_7=1	-	-

Table 17.4 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	-
P71 ⁽¹⁾	RxD2 input	PS1_1=0	-	-	PD7_1=0
P72	CLK2 input	PS1_2=0	-	-	PD7_2=0
	CLK2 output	PS1_2=1	PSL1_2=0	PSC_2=0	-
P73	CTS2 input	PS1_3=0	-	-	PD7_3=0
	RTS2 output	PS1_3=1	PSL1_3=0	PSC_3=0	-

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 17.5 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P90	CLK3 input	PS3_0=0	-	PD9_0=0
	CLK3 output	PS3_0=1	-	-
P91	RxD3 input	PS3_1=0	-	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	-
P93	CTS3 input	PS3_3=0	PSL3_3=0	PD9_3=0
	RTS3 output	PS3_3=1	-	-
P94	CTS4 input	PS3_4=0	PSL3_4=0	PD9_4=0
	RTS4 output	PS3_4=1	-	-
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
	CLK4 output	PS3_5=1	-	-
P96	TxD4 output	PS3_6=1	-	-
P97	RxD4 input	PS3_7=0	-	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

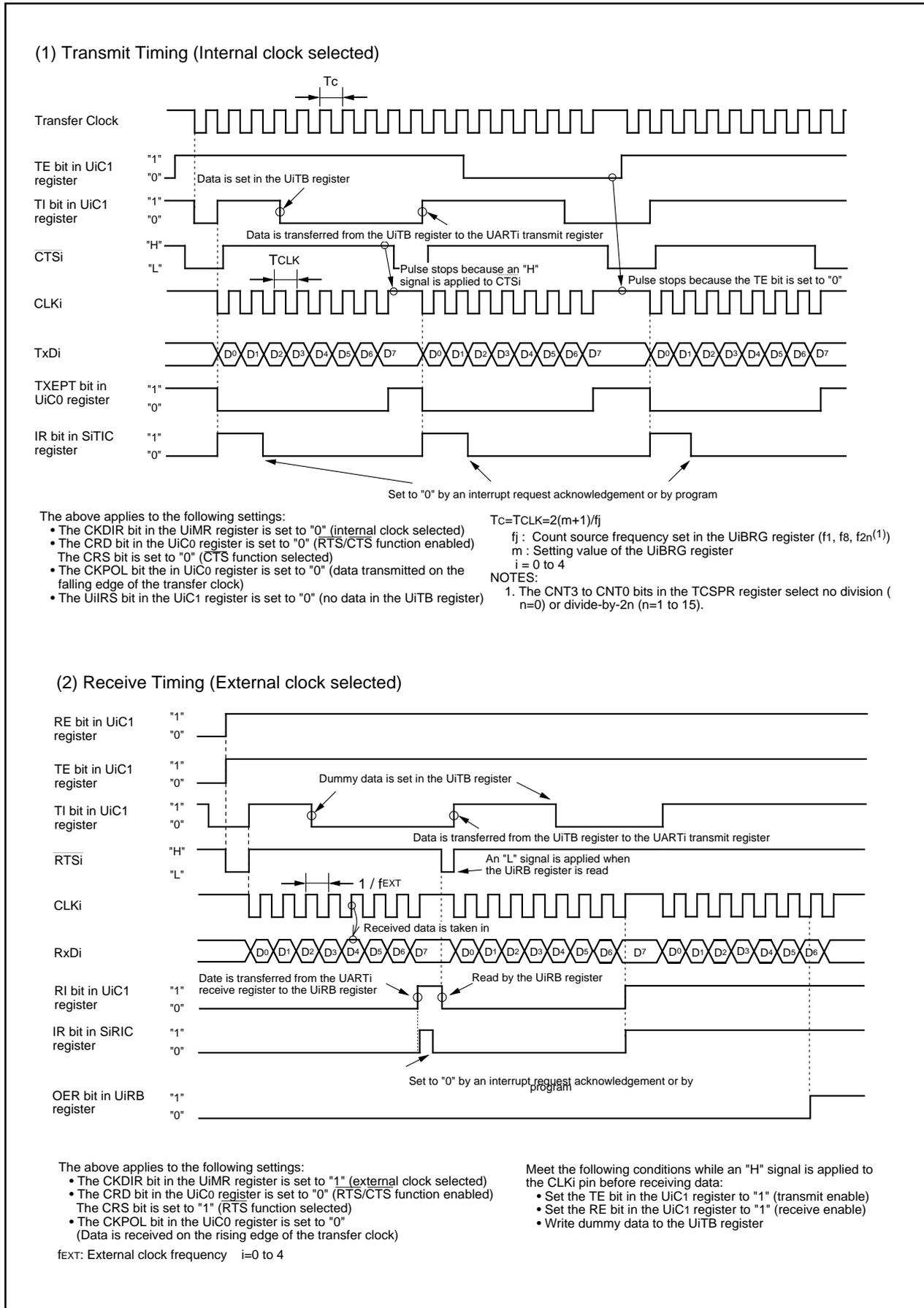


Figure 17.10 Transmit and Receive Operation

17.1.1 Selecting CLK Polarity Selecting

As shown in Figure 17.11, the CKPOL bit in the UiC0 register (i=0 to 4) determines the polarity of the transfer clock.

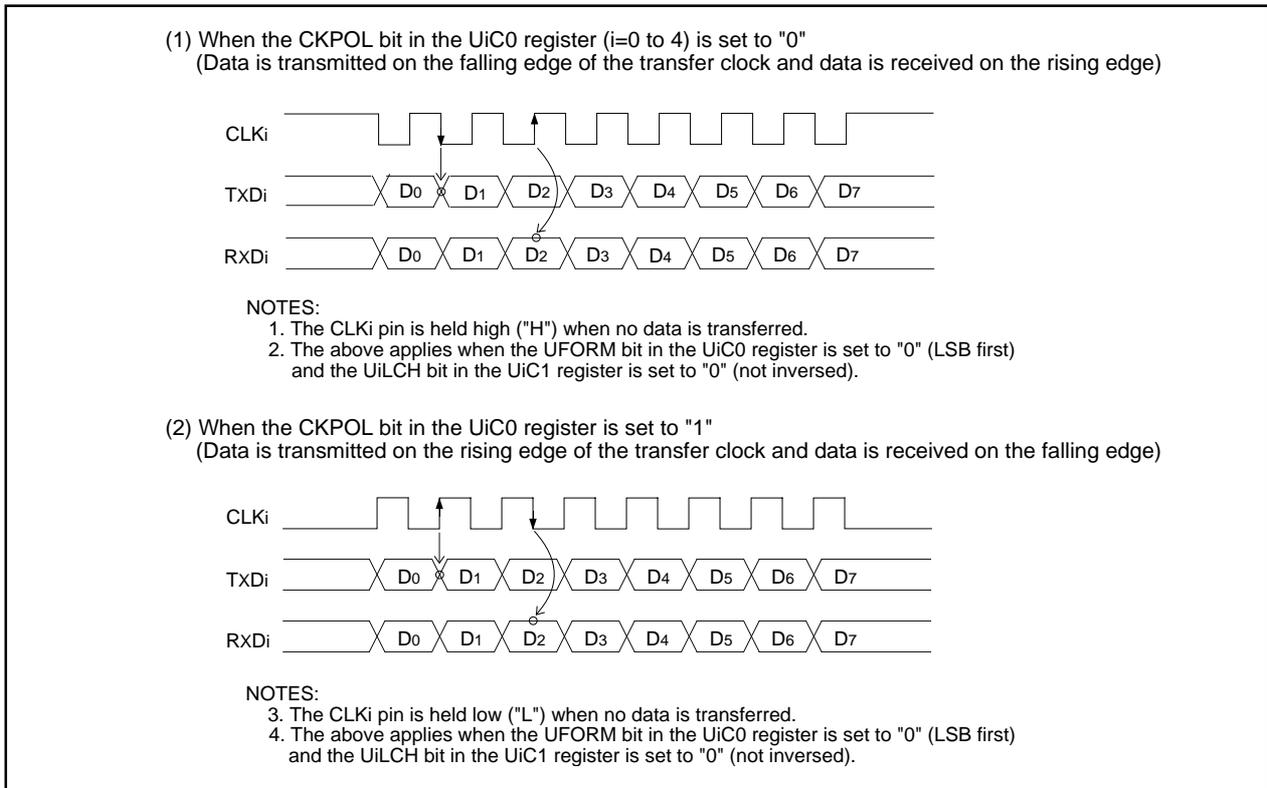


Figure 17.11 Transfer Clock Polarity

17.1.2 Selecting LSB First or MSB First

As shown in Figure 17.12, the UFORM bit in the UiC0 register (i=0 to 4) determines a data transfer format.

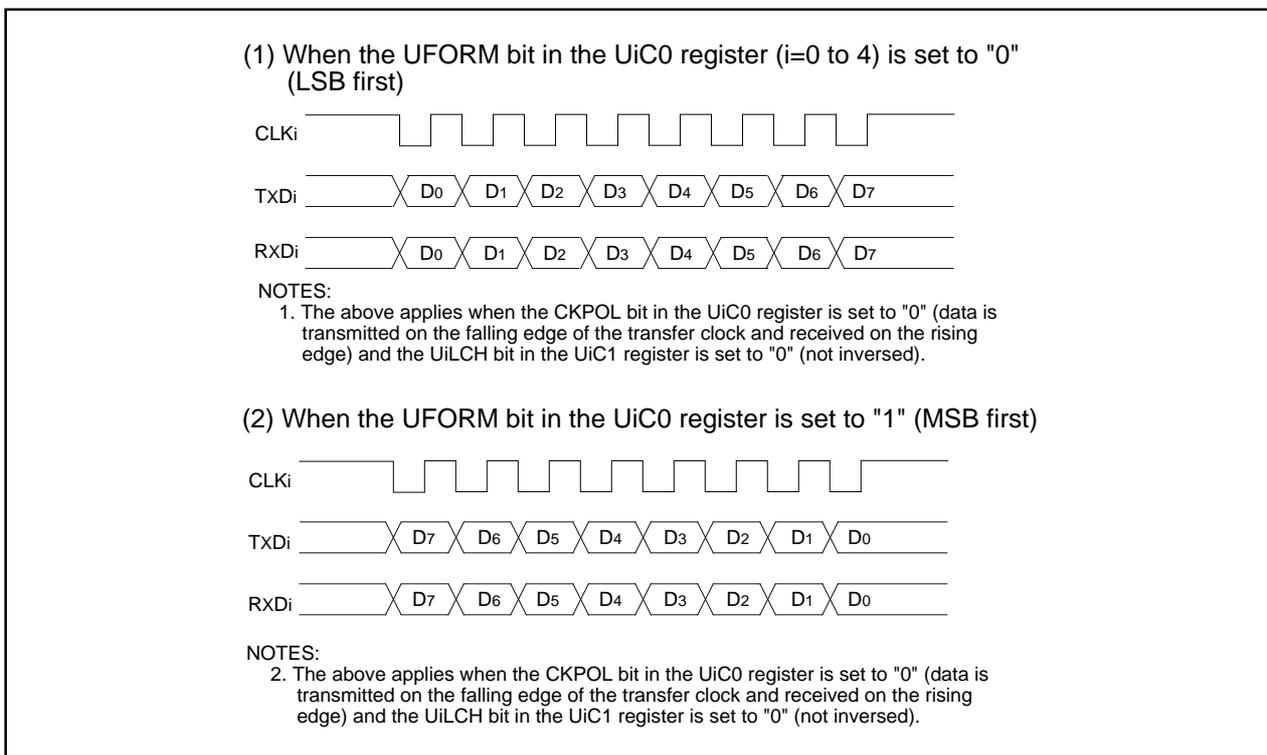


Figure 17.12 Transfer Format

17.1.3 Continuous Receive Mode

When the UiRRM bit in the UiC1 register (i=0 to 4) is set to "1" (continuous receive mode), the TI bit is set to "0" (data in the UiTB register) by reading the UiRB register. When the UiRRM bit is set to "1", do not set dummy data in the UiTB register by program.

17.1.4 Serial Data Logic Inverse

When the UiLCH bit (i=0 to 4) in the UiC1 register is set to "1" (inverse), data logic written in the UiTB register is inverted when transmitted. The inverted receive data logic can be read by reading the UiRB register. Figure 17.13 shows a switching example of the serial data logic.

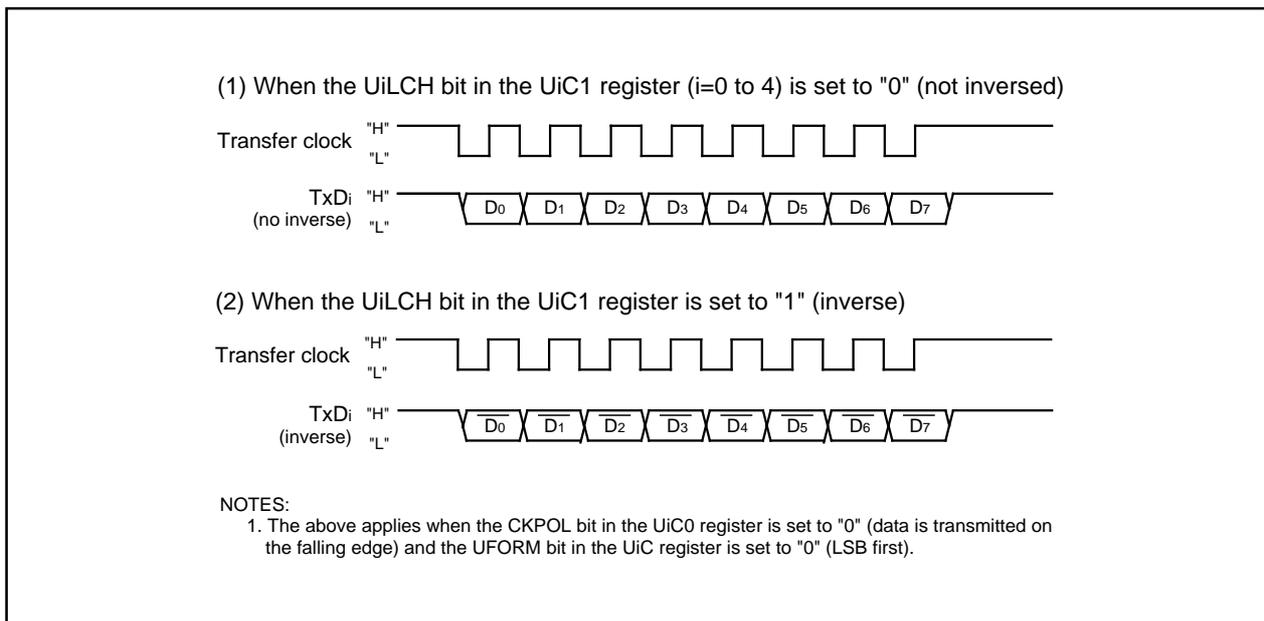


Figure 17.13 Serial Data Logic Inverse

17.2 Clock Asynchronous Serial I/O (UART) Mode

In UART mode, data is transmitted and received after setting a desired bit rate and data transfer format. Table 17.6 lists specifications of UART mode.

Table 17.6 UART Mode Specifications

Item	Specification
Transfer Data Format	<ul style="list-style-type: none"> • Character bit (transfer data) : selected from 7 bits, 8 bits, or 9 bits long • Start bit: 1 bit long • Parity bit: selected from odd, even, or none • Stop bit: selected from 1 bit or 2 bits long
Transfer Clock	<ul style="list-style-type: none"> • The CKDIR bit in the UiMR register is set to "0" (internal clock selected): $f_j/16(m+1)$ $f_j = f_1, f_8, f_{2n}^{(1)}$ m: setting value of the UiBRG register, 0016 to FF16 • The CKDIR bit is set to "1" (external clock selected): $f_{EXT}/16(m+1)$ f_{EXT}: clock applied to the CLKi pin
Transmit/Receive Control	Select from CTS function, RTS function or CTS/RTS function disabled
Transmit Start Condition	To start transmitting, the following requirements must be met: <ul style="list-style-type: none"> - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the TI bit in the UiC1 register to "0" (data in the UiTB register) - Apply a low-level ("L") signal to the CTSi pin when the CTS function is selected
Receive Start Condition	To start receiving, the following requirements must be met: <ul style="list-style-type: none"> - Set the RE bit in the UiC1 register to "1" (receive enable) - The start bit is detected
Interrupt Request Generation Timing	<p>While transmitting, the following condition can be selected:</p> <ul style="list-style-type: none"> - The UiIRS bit in the UiC1 register is set to "0" (no data in the UiTB register): when data is transferred from the UiTB register to the UARTi transmit register (transfer started) - The UiIRS bit is set to "1" (transmission completed): when data transmission from the UARTi transfer register is completed <p>While receiving</p> <ul style="list-style-type: none"> - when data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detect	<ul style="list-style-type: none"> • Overrun error⁽²⁾ This error occurs when the bit before the last stop bit of the next received data is read prior to reading the UiRB register (the first stop bit when selecting 2 stop bits) • Framing error This error occurs when the number of stop bits set is not detected • Parity error When parity is enabled, this error occurs when the number of "1" in parity and character bits does not match the number of "1" set • Error sum flag This flag is set to "1" when any of an overrun, framing or parity errors occur
Selectable Function	<ul style="list-style-type: none"> • LSB first or MSB first Data is transmitted or received in either bit 0 or in bit 7 • Serial data logic inverse Logic values of data to be transmitted and received data are inversed. The start bit and stop bit are not inversed • TxD and RxD I/O polarity Inverse TxD pin output and RxD pin input are inversed. All I/O data levels are also inversed

NOTES:

1. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).
2. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register remains unchanged as "1" (interrupt requested).

Table 17.7 lists register settings. Tables 17.8 to 17.10 list pin settings. When UART_i (i=0 to 4) operating mode is selected, the TxD_i pin outputs a high-level ("H") signal before transfer is started (the TxD_i pin is in a high-impedance state when the N-channel open drain output is selected). Figure 17.14 shows an example of a transmit operation in UART mode. Figure 17.15 shows an example of a receive operation in UART mode.

Table 17.7 Register Settings in UART Mode

Register	Bit	Function
UiTB	8 to 0	Set transmit data ⁽¹⁾
UiRB	8 to 0	Received data can be read ⁽¹⁾
	OER, FER, PER, SUM	Error flags
UiBRG	7 to 0	Set bit rate
UiMR	SMD2 to SMD0	Set to "1002" when transfer data is 7 bits long Set to "1012" when transfer data is 8 bits long Set to "1102" when transfer data is 9 bits long
	CKDIR	Select the internal clock or external clock
	STPS	Select stop bit length
	PRY, PRYE	Select parity enable or disable, odd or even
	IOPOL	Select TxD and RxD I/O polarity
UiC0	CLK1, CLK0	Select count source for the UiBRG register
	CRS	Select either $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ when using either
	TXEPT	Transfer register empty flag
	CRD	Enables or disables the CTS or RTS function
	NCH	Select output format of the TxD _i pin
	CKPOL	Set to "0"
	UFORM	Select the LSB first or MSB first when a transfer data is 8 bits long Set to "0" when transfer data is 7 bits or 9 bits long
UiC1	TE	Set to "1" to enable data transmission
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select what causes the UART _i transmit interrupt to be generated
	UiRRM	Set to "0"
	UiLCH	Select whether data logic is inversed or not inversed when a transfer data is 7 bits or 8 bits long. Set to "0" when transfer data is 9 bits long
	UiERE	Set to either "0" or "1"
UiSMR	7 to 0	Set to "0016"
UiSMR2	7 to 0	Set to "0016"
UiSMR3	7 to 0	Set to "0016"
UiSMR4	7 to 0	Set to "0016"

NOTES:

1. Use bits 0 to 6 when transfer data is 7 bits long, bits 0 to 7 when 8 bits long, bits 0 to 8 when 9 bits long.

Table 17.8 Pin Settings in UART Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	CTS0 input	PS0_0=0	–	PD6_0=0
	RTS0 output	PS0_0=1	–	–
P61	CLK0 input	PS0_1=0	–	PD6_1=0
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P64	CTS1 input	PS0_4=0	–	PD6_4=0
	RTS1 output	PS0_4=1	PSL0_4=0	–
P65	CLK1 input	PS0_5=0	–	PD6_5=0
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

Table 17.9 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71 ⁽¹⁾	RxD2 input	PS1_1=0	–	–	PD7_1=0
P72	CLK2 input	PS1_2=0	–	–	PD7_2=0
P73	CTS2 input	PS1_3=0	–	–	PD7_3=0
	RTS2 output	PS1_3=1	PSL1_3=0	PSC_3=0	–

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 17.10 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P90	CLK3 input	PS3_0=0	–	PD9_0=0
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P93	CTS3 input	PS3_3=0	PSL3_3=0	PD9_3=0
	RTS3 output	PS3_3=1	–	–
P94	CTS4 input	PS3_4=0	PSL3_4=0	PD9_4=0
	RTS4 output	PS3_4=1	–	–
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers set immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

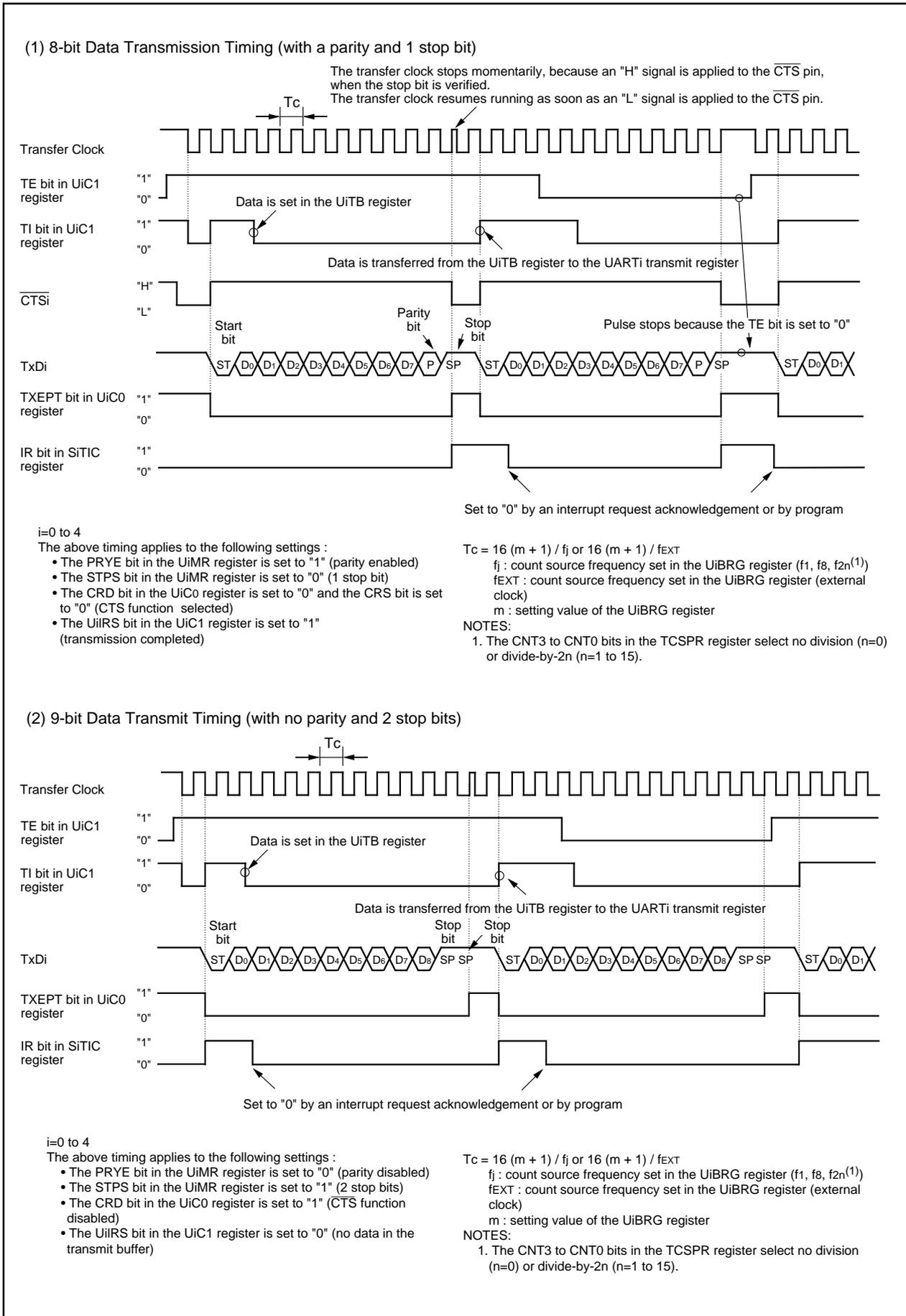


Figure 17.14 Transmit Operation

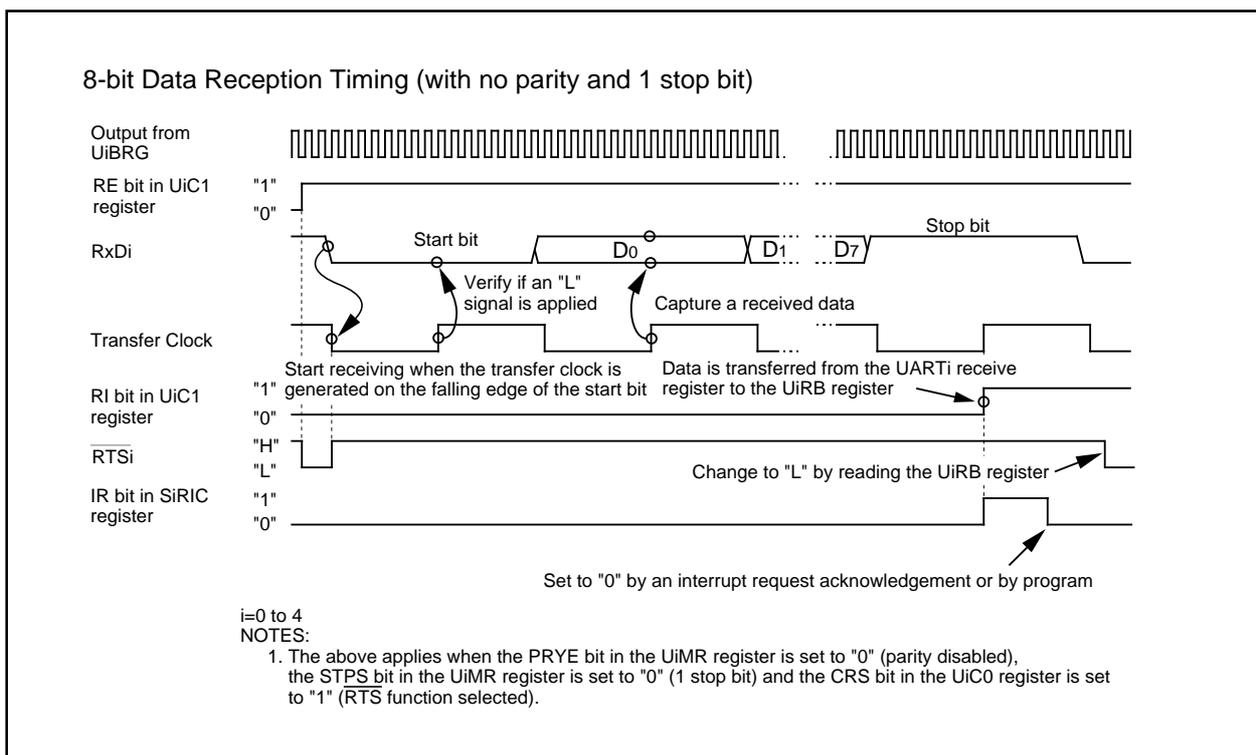


Figure 17.15 Receive Operation

17.2.1 Transfer Speed

In UART mode, transfer speed is clock frequency which is divided by a setting value of the UiBRG (i=0 to 4) register and again divided by 16. Table 17.11 lists an example of transfer speed setting.

Table 17.11 Transfer Speed

Bit Rate (bps)	Count Source of UiBRG	Peripheral Function Clock: 16MHz		Peripheral Function Clock: 24MHz		Peripheral Function Clock: 32MHz	
		Setting Value of UiBRG: <i>n</i>	Actual Bit Rate (bps)	Setting Value of UiBRG: <i>n</i>	Actual Bit Rate (bps)	Setting Value of UiBRG: <i>n</i>	Actual Bit Rate (bps)
1200	f8	103 (67h)	1202	155 (96h)	1202	207 (CFh)	1202
2400	f8	51 (33h)	2404	77 (46h)	2404	103 (67h)	2404
4800	f8	25 (19h)	4808	38 (26h)	4808	51 (33h)	4808
9600	f1	103 (67h)	9615	155 (96h)	9615	207 (CFh)	9615
14400	f1	68 (44h)	14493	103 (67h)	14423	138 (8Ah)	14388
19200	f1	51 (33h)	19231	77 (46h)	19231	103 (67h)	19231
28800	f1	34 (22h)	28571	51 (33h)	28846	68 (44h)	28986
31250	f1	31 (1Fh)	31250	47 (2Fh)	31250	63 (3Fh)	31250
38400	f1	25 (19h)	38462	38 (26h)	38462	51 (33h)	38462
51200	f1	19 (13h)	50000	28 (1Ch)	51724	38 (26h)	51282

17.2.2 Selecting LSB First or MSB First

As shown in Figure 17.16, the UFORM bit in the UiC0 register (i=0 to 4) determines data transfer format. This function is available for 8-bit transfer data.

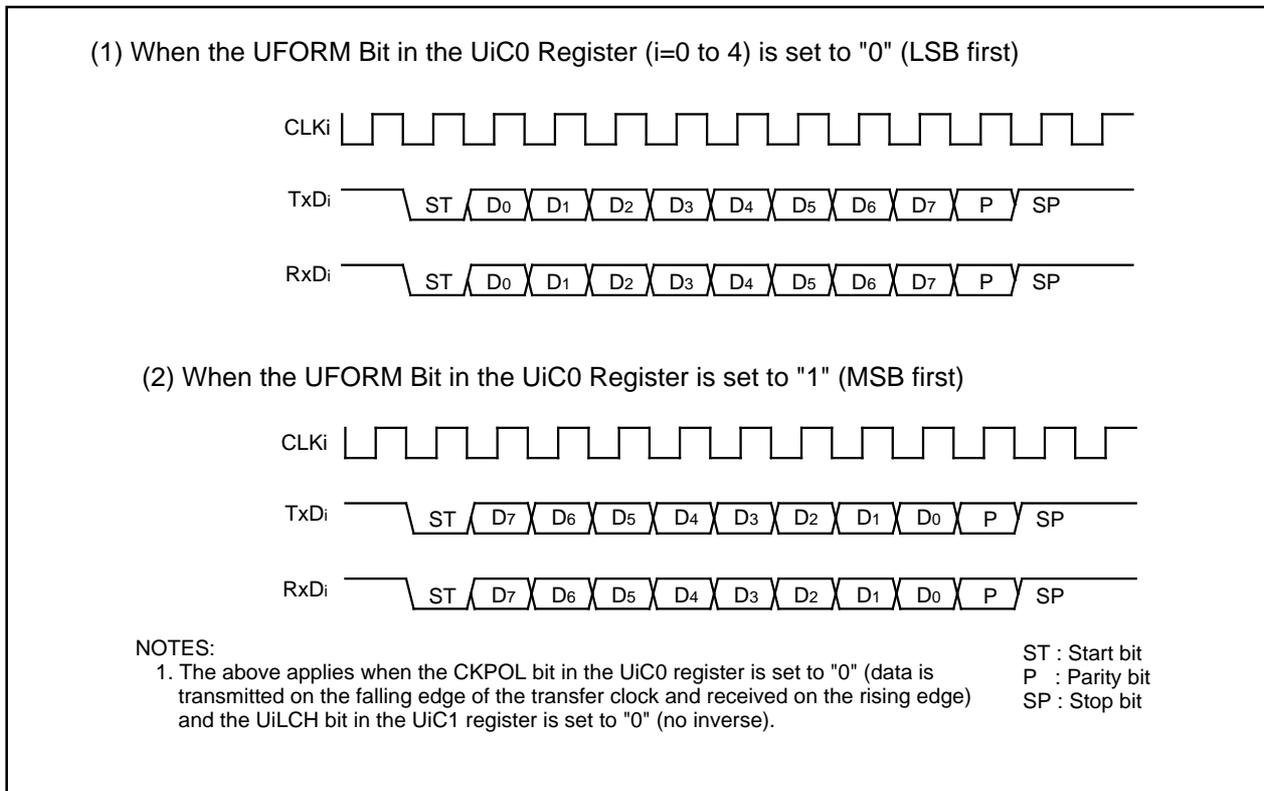


Figure 17.16 Transfer Format

17.2.3 Serial Data Logic Inverse

When the UiLCH bit (i=0 to 4) in the UiC1 register is set to "1" (inverse), data logic written in the UiTB register is inverted when transmitted. The inverted receive data logic can be read by reading the UiRB register. Figure 17.17 shows a switching example of the serial data logic.

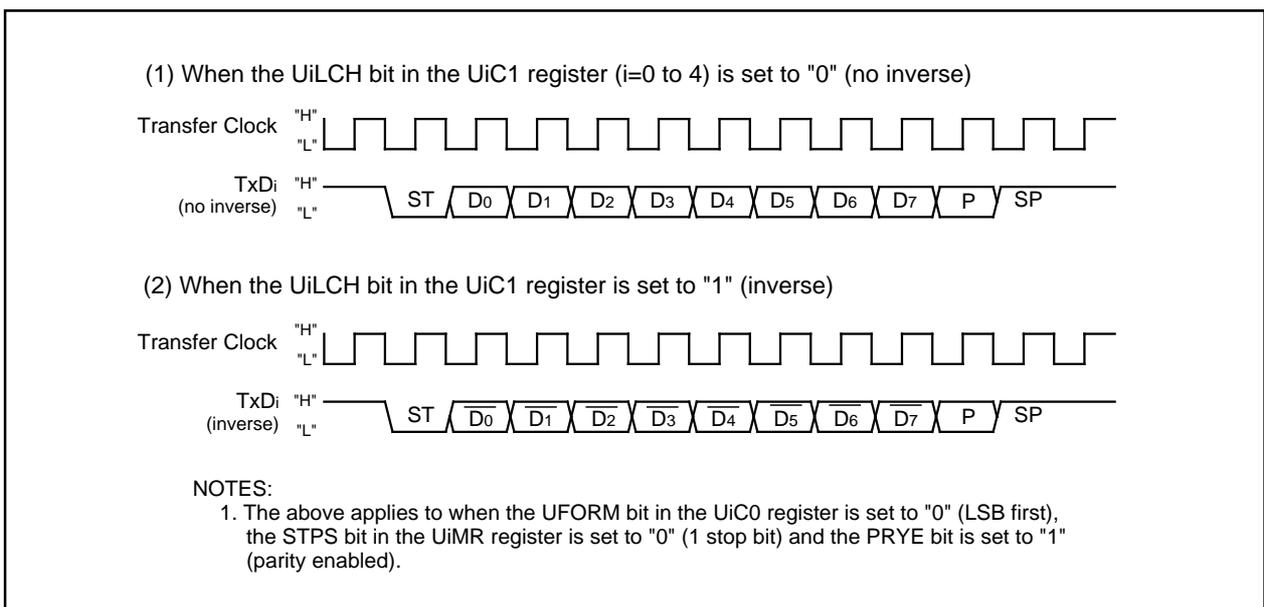


Figure 17.17 Serial Data Logic Inverse

17.2.4 TxD and RxD I/O Polarity Inverse

TxD pin output and RxD pin input are inverted. All I/O data level, including the start bit, stop bit and parity bit, are inverted. Figure 17.18 shows TxD and RxD I/O polarity inverse.

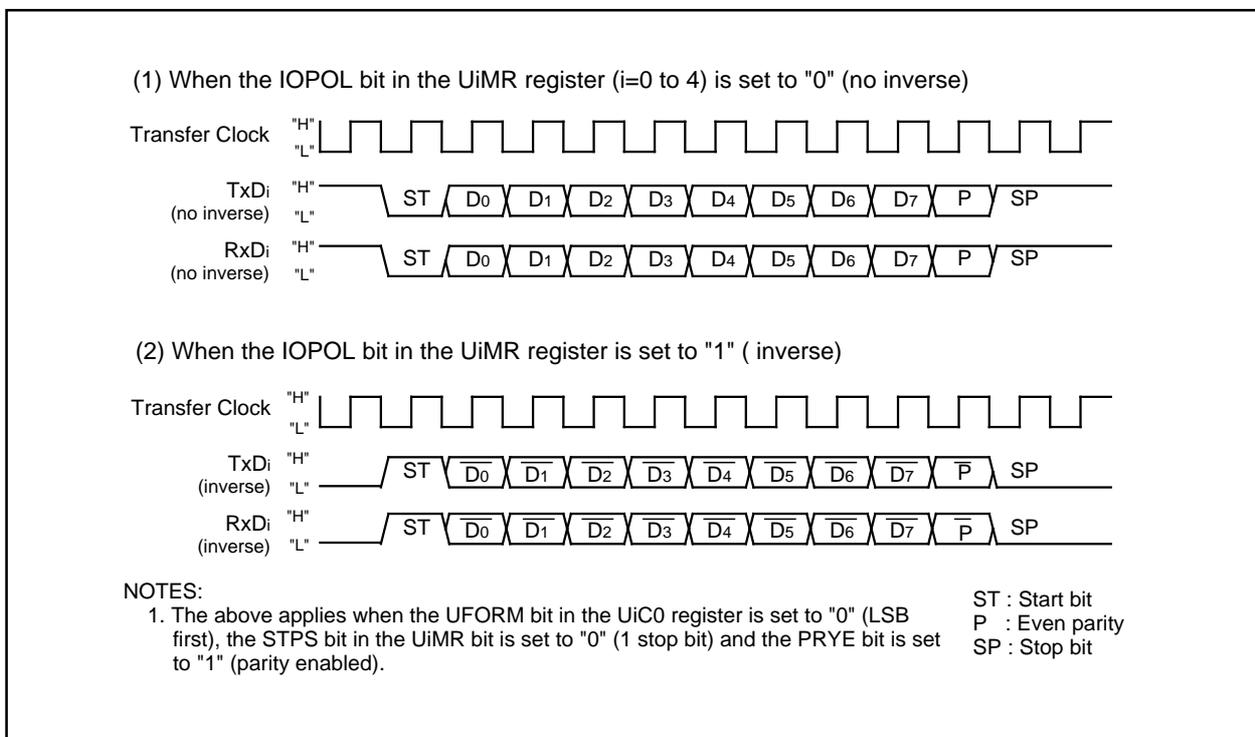


Figure 17.18 TxD and RxD I/O Polarity Inverse

17.3 Special Mode 1 (I²C Mode)

I²C mode is a mode to communicate with external devices with a simplified I²C. Table 17.12 lists specifications of I²C mode. Table 17.13 lists register settings, Table 17.14 lists each function. Figure 17.19 shows a block diagram of I²C mode. Figure 17.20 shows timings for transfer to the UiRB register and interrupts. Tables 17.15 to 17.17 list pin settings.

As shown in Table 17.12, I²C mode is entered when the SMD2 to SMD0 bits in the UiMR register is set to "0102" and the IICM bit in the UiSMR register is set to "1". Output signal from the SDAi pin changes after the SCLi pin level becomes low ("L") and stabilizes due to a SDAi transmit output via the delay circuit.

Table 17.12 I²C Mode Specifications

Item	Specifications
Interrupt	Start condition detect, stop condition detect, no acknowledgment detect, acknowledgment detect
Selectable Function	<ul style="list-style-type: none"> • Arbitration lost The update timing of the ABT bit in the UiRB register can be selected. Refer to 17.3.3 Arbitration • SDAi digital delay Selected from no digital delay or 2 to 8 cycle delay of the count source of the UiBRG register. Refer to 17.3.5 SDA Output • Clock phase setting Selected from clock delay or no clock delay. Refer to 17.3.4 Transfer clock

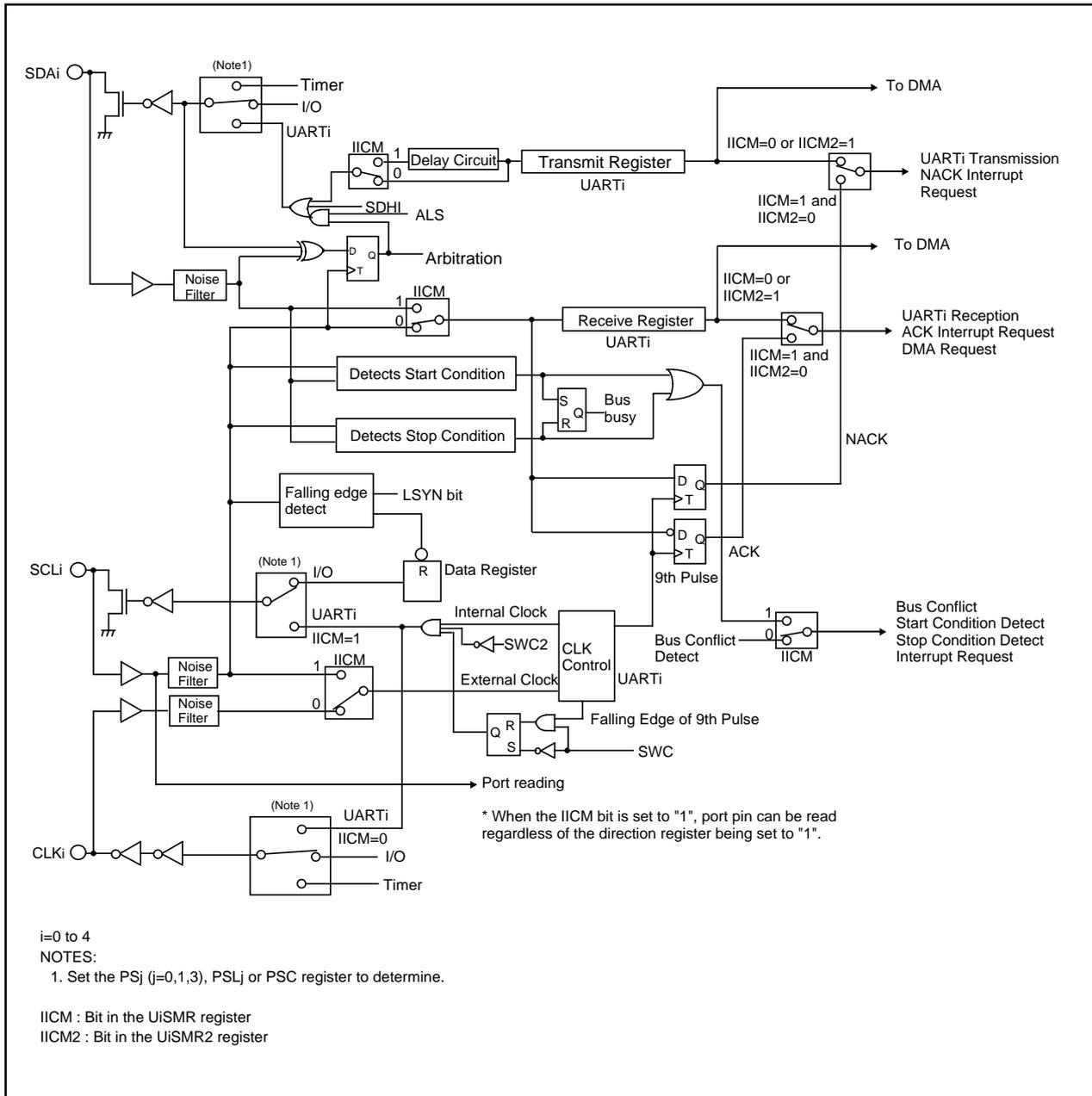


Figure 17.19 I²C Mode Block Diagram

Table 17.13 Register Settings in I²C Mode

Register	Bit	Function	
		Master	Slave
UiTB	7 to 0	Set transmit data	
UiRB	7 to 0	Received data can be read	
	8	ACK or NACK bit can be read	
	ABT	Arbitration lost detect flag	Disabled
	OER	Overrun error flag	
UiBRG	7 to 0	Set bit rate	Disabled
UiMR	SMD2 to SMD0	Set to "0102"	
	CKDIR	Set to "0"	Set to "1"
	IOPOL	Set to "0"	
UiC0	CLK1, CLK0	Select count source of the UiBRG register	Disabled
	CRS	Disabled because the CRD bit is set to "1"	
	TXEPT	Transfer register empty flag	
	CRD, NCH	Set to "1"	
	CKPOL	Set to "0"	
	UFORM	Set to "1"	
UiC1	TE	Set to "1" to enable data transmission	
	TI	Transfer buffer empty flag	
	RE	Set to "1" to enable data reception	
	RI	Reception complete flag	
	UiRRM, UiLCH, UIERE	Set to "0"	
UiSMR	IICM	Set to "1"	
	ABC	Select an arbitration lost detect timing	Disabled
	BBS	Bus busy flag	
	7 to 3	Set to "000002"	
UiSMR2	IICM2	See Table 17.14	
	CSC	Set to "1" to enable clock synchronization	Set to "0"
	SWC	Set to "1" to fix an "L" signal output from SCLi on the falling edge of the ninth bit of the transfer clock	
	ALS	Set to "1" to terminate SDAi output when detecting the arbitration lost	Not used. Set to "0"
	STC	Not used. Set to "0"	Set to "1" to reset UARTi by detecting the start condition
	SWC2	Set to "1" for an "L" signal output from SCL forcibly	
	SDHI	Set to "1" to disable SDA output	
	SU1HIM	Set to "0"	
UiSMR3	SSE	Set to "0"	
	CKPH	See Table 17.14	
	DINC, NODC, ERR	Set to "0"	
	DL2 to DL0	Set digital delay value	
UiSMR4	STAREQ	Set to "1" when generating a start condition	Not used. Set to "0"
	RSTAREQ	Set to "1" when generating a restart condition	
	STPREQ	Set to "1" when generating a stop condition	
	STSPSEL	Set to "1" when using a condition generating function	
	ACKD	Select ACK or NACK	
	ACKC	Set to "1" for ACK data output	
	SCLHI	Set to "1" to enable SCL output stop when detecting stop condition	Not used. Set to "0"
	SWC9	Not used. Set to "0"	Set to "1" to fix an "L" signal output from SCLi on the falling edge of the ninth bit of the transfer clock
IFSR	IFSR6, IFSR7	Set to "1"	

i=0 to 4

Table 17.14 I²C Mode Functions

Function	Clock Synchronous Serial I/O Mode (SMD2 to SMD0=0012, IICM=0)	I ² C Mode (SMD2 to SMD0=0102, IICM=1)			
		IICM2=0 (NACK/ACK interrupt)		IICM2=1 (UART transmit / UART receive interrupt)	
		CKPH=0 (No clock delay)	CKPH=1 (Clock delay)	CKPH=0 (No clock delay)	CKPH=1 (Clock delay)
Interrupt Numbers 39 to 41 Generated ⁽¹⁾ (See Figure 17.20)	-	Start condition or stop condition detect (See Table 17.18)			
Interrupt Number 17, 19, 33, 35 and 37 Generated ⁽¹⁾ (See Figure 17.20)	UARTi Transmission - Transmission started or completed (selected by the UiIRS register)	No Acknowledgement Detection (NACK) - Rising edge of 9th bit of SCLi	UARTi Transmission - Rising edge of 9th bit of SCLi	UARTi Transmission - Next falling edge after the 9th bit of SCLi	
Interrupt Numbers 18, 20, 34, 36 and 38 Generated ⁽¹⁾ (See Figure 17.20)	UARTi Reception - Receiving at 8th bit CKPOL=0(rising edge) CKPOL=1(falling edge)	Acknowledgement Detection (ACK) - Rising edge of 9th bit of SCLi	UARTi Reception - Falling edge of 9th bit of SCLi		
Data Transfer Timing from the UART Receive Shift Register to the UiRB Register	CKPOL=0(rising edge) CKPOL=1(falling edge)	Rising edge of 9th bit of SCLi	Falling edge of 9th bit of SCLi	Falling edge and rising edge of 9th bit of SCLi	
UARTi Transmit Output Delay	No delay	Delay			
P63, P67, P70, P92, P96 Pin Functions	TxDi output	SDAi input and output			
P62, P66, P71, P91, P97 Pin Functions	RxDi input	SCLi input and output			
P61, P65, P72, P90, P95 Pin Functions	Select CLKi input or output	- (Not used in I ² C mode)			
Noise Filter Width	15ns	200ns			
Reading RxDi and SCLi Pin Levels	Can be read if port direction bit is set to "0"	Can be read regardless of the port direction bit			
Default Value of TxDi, SDAi Output	CKPOL=0 (H) CKPOL=1 (L)	Values set in the port register before entering I ² C mode ⁽²⁾			
SCLi Default and End Value	-	H	L	H	L
DMA Generated (See Figure 17.20)	UARTi reception	Acknowledgement detection (ACK)		UARTi Reception - Falling edge of 9th bit of SCLi	
Store Received Data	1st to 8th bits of the received data are stored into bits 7 to 0 in the UiRB register	1st to 8th bits of the received data are stored into bits 7 to 0 in the UiRB register	1st to 7th bits of the received data are stored into bits 6 to 0 in the UiRB register. 8th bit is stored into bit 8 in the UiRB register.		
			1st to 8th bits are stored into bits 7 to 0 in the UiRB register ⁽³⁾		
Reading Received Data	The UiRB register status is read	Bits 6 to 0 in the UiRB registers ⁽⁴⁾ are read as bit 7 to 1. Bit 8 in the UiRB register is read as bit 0			

i=0 to 4

NOTES:

- Follow the procedures below to change what causes an interrupt to be generated.
 - Disable interrupt of corresponding interrupt number.
 - Change what causes an interrupt to be generated.
 - Set the IR bit of a corresponding interrupt number to "0" (no interrupt requested).
 - Set the ILVL2 to ILVL0 bits of a corresponding interrupt number.
- Set default value of the SDAi output when the SMD2 to SMD0 bits in the UiMR register are set to "0002" (serial I/O disabled).
- Second data transfer to the UiRB register (on the rising edge of the ninth bit of SCLi).
- First data transfer to the UiRB register (on the falling edge of the ninth bit of SCLi).

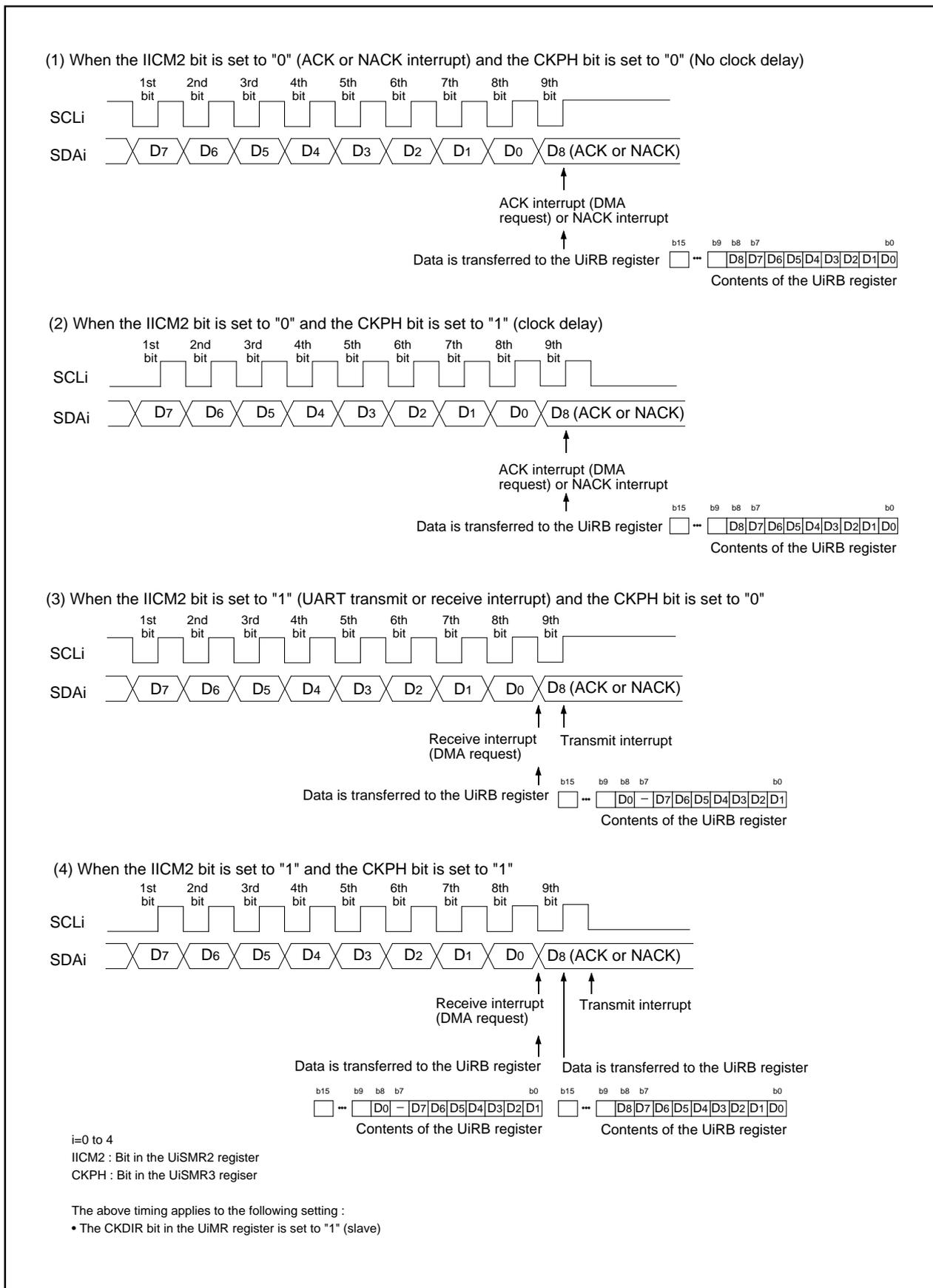


Figure 17.20 SCLi Timing

Table 17.15 Pin Settings in I²C Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P62	SCL0 output	PS0_2=1	PSL0_2=0	-
	SCL0 input	PS0_2=0	-	PD6_2=0
P63	SDA0 output	PS0_3=1	-	-
	SDA0 input	PS0_3=0	-	PD6_3=0
P66	SCL1 output	PS0_6=1	PSL0_6=0	-
	SCL1 input	PS0_6=0	-	PD6_6=0
P67	SDA1 output	PS0_7=1	-	-
	SDA1 input	PS0_7=0	-	PD6_7=0

Table 17.16 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	SDA2 output	PS1_0=1	PSL1_0=0	PSC_0=0	-
	SDA2 input	PS1_0=0	-	-	PD7_0=0
P71 ⁽¹⁾	SCL2 output	PS1_1=1	PSL1_1=1	PSC_1=0	-
	SCL2 input	PS1_1=0	-	-	PD7_1=0

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 17.17 Pin Settings (3)

Port	Function	Setting			
		PS3 Register ⁽¹⁾	PSL3 Register	PSC3 Register	PD9 Register ⁽¹⁾
P91	SCL3 output	PS3_1=1	PSL3_1=0	-	-
	SCL3 input	PS3_1=0	-	-	PD9_1=0
P92	SDA3 output	PS3_2=1	PSL3_2=0	-	-
	SDA3 input	PS3_2=0	-	-	PD9_2=0
P96	SDA4 output	PS3_6=1	-	PSC3_6=0	-
	SDA4 input	PS3_6=0	-	-	PD9_6=0
P97	SCL4 output	PS3_7=1	PSL3_7=0	-	-
	SCL4 input	PS3_7=0	-	-	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

17.3.1 Detecting Start Condition and Stop Condition

The microcomputer detects either a start condition or stop condition. The start condition detect interrupt is generated when the SCLi (i=0 to 4) pin level is held high ("H") and the SDAi pin level changes "H" to low ("L"). The stop condition detect interrupt is generated when the SCLi pin level is held "H" and the SDAi pin level changes "L" to "H". The start condition detect interrupt shares interrupt control registers and vectors with the stop condition detect interrupt. The BBS bit in the UiSMR register determines which interrupt is requested.

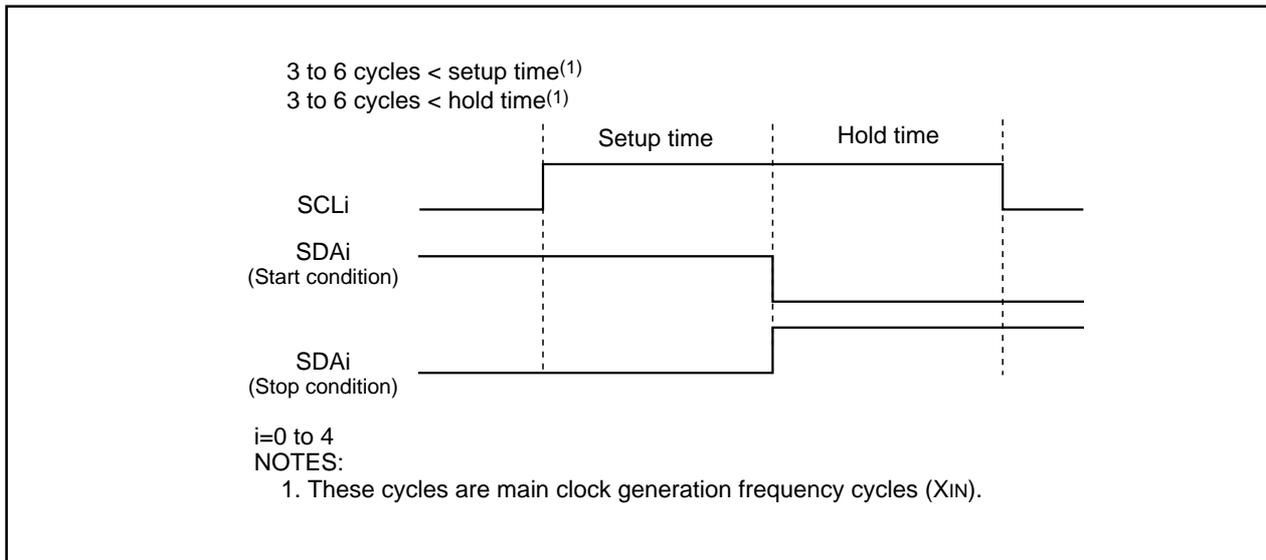


Figure 17.21 Start Condition or Stop Condition Detecting

17.3.2 Start Condition or Stop Condition Output

The start condition is generated when the STAREQ bit in the UiSMR4 register (i=0 to 4) is set to "1" (start). The restart condition is generated when the RSTAREQ bit in the UiSMR4 register is set to "1" (start). The stop condition is generated the STPREQ bit in the UiSMR4 is set to "1" (start).

The start condition is output when the STAREQ bit is set to "1" and the STSPSEL bit in the UiSMR4 register is set to "1" (start or stop condition generating circuit selected). The restart condition output is provided when the RSTAREQ bit and STSPSEL bit are set to "1". The stop condition output is provided when the STPREQ bit and the STSPSEL bit are set to "1".

When the start condition, stop condition or restart condition is output, do not generate an interrupt between the instruction to set the STAREQ bit, STPREQ bit or RSTAREQ bit to "1" and the instruction to set the STSPSEL bit to "1". When the start condition is output, set the STAREQ bit to "1" before the STSPSEL bit is set to "1".

Table 17.18 lists function of the STSPSEL bit. Figure 17.22 shows functions of the STSPSEL bit.

Table 17.18 STSPSEL Bit Function

Function	STSPSEL = 0	STSPSEL = 1
Start condition and stop condition output	Program with ports determines how the start condition or stop condition output is provided	The STAREQ bit, RSTAREQ bit and STPREQ bit determine how the start condition or stop condition output is provided
Timing to generate start condition and stop condition interrupt requests	The start condition and stop condition are detected	Start condition and stop condition generation are completed

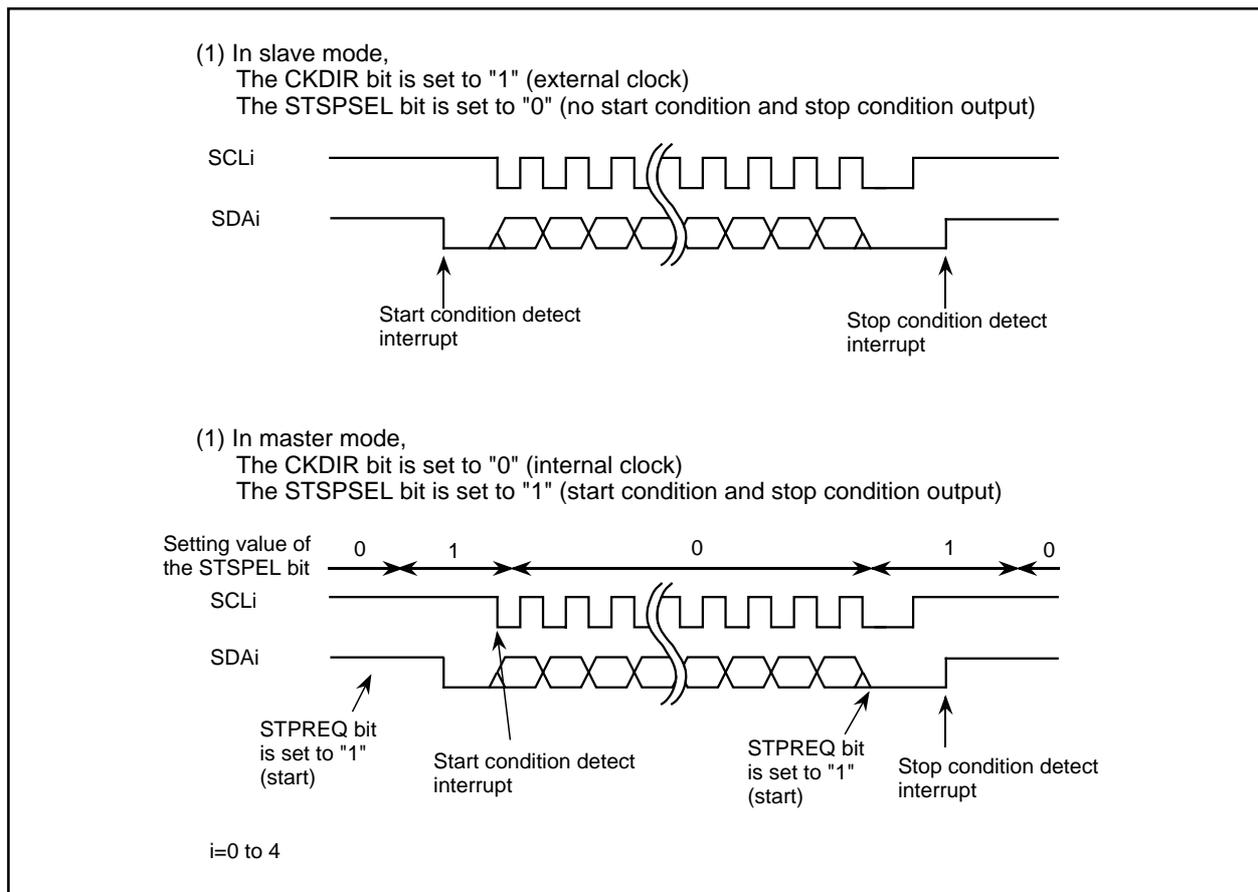


Figure 17.22 STSPSEL Bit Function

17.3.3 Arbitration

The ABC bit in the UiSMR register (i=0 to 4) determines an update timing for the ABT bit in the UiRB register. On the rising edge of the SCLi pin, the microcomputer determines whether a transmit data matches data input to the SDAi pin.

When the ABC bit is set to "0" (update per bit), the ABT bit is set to "1" (detected-arbitration is lost) as soon as a data discrepancy is detected. The ABT bit is set to "0" (not detected-arbitration is won) if not detected. When the ABC bit is set to "1" (update per byte), the ABT bit is set to "1" on the falling edge of the ninth bit of the transfer clock if any discrepancy is detected. When the ABT bit is updated per byte, set the ABT bit to "0" between an ACK detection in the first byte data and the next byte data to be transferred. When the ALS bit in the UiSMR2 register is set to "1" (SDA output stop enabled), the arbitration lost occurs. As soon as the ABT bit is set to "1", the SDAi pin is placed in a high-impedance state.

17.3.4 Transfer Clock

The transfer clock transmits and receives data as is shown in Figure 17.20.

The CSC bit in the UiSMR2 register (i=0 to 4) synchronizes an internally generated clock (internal SCLi) with the external clock applied to the SCLi pin. When the CSC bit is set to "1" (clock synchronous enabled) and the internal SCLi is held high ("H"), the internal SCLi become low ("L") if signal applied to the SCLi pin is on the falling edge. Value of the UiBRG register is reloaded to start counting for low level. A counter stops when the SCLi pin is held "L" and then the internal SCLi changes "L" to "H". Counting is resumed when the SCLi pin become "H". The transfer clock of UARTi is equivalent to the AND for signals from the internal SCLi and the SCLi pin.

The transfer clock is synchronized between a half cycle before the falling edge of first bit of the internal SCLi and the rising edge of the ninth bit. Select the internal clock as the transfer clock while the CSC bit is set to "1".

The SWC bit in the UiSMR2 register determines whether the SCLi pin is fixed to be an "L" signal output on the falling edge of the ninth cycle of the transfer clock or not.

When the SCLHI bit in the UiSMR4 register is set to "1" (enabled), a SCLi output stops when a stop condition is detected (high-impedance).

When the SWC2 bit in the UiSMR2 register is set to "1" (0 output), the SCLi pin forcibly outputs an "L" signal while transmitting and receiving. The fixed "L" signal applied to the SCLi pin is cancelled by setting the SWC2 bit to "0" (transfer clock) and the transfer clock input to and output from the SCLi pin are provided.

When the CKPH bit in the UiSMR3 register is set to "1" and the SWC9 bit in the UiSMR4 register is set to "1" (SCL "L" hold enabled), the SCLi pin is fixed to be an "L" signal output on the next falling edge after the ninth bit of the clock. The fixed "L" signal applied to the SCLi pin is cancelled by setting the SWC9 bit to "0" (SCL "L" hold disabled).

17.3.5 SDA Output

Values output set in bits 7 to 0 (D7 to D0) in the UiTB register (i=0 to 4) are provided in descending order from D7. The ninth bit (D8) is ACK or NACK.

Set the default value of SDAi transmit output when the IICM bit is set to "1" (I²C mode) and the SMD2 to SMD0 bits in the UiMR register are set to "0002" (serial I/O disabled).

The DL2 to DL0 bits in the UiSMR3 register determine no delay in the SDAi output or a delay of 2 to 8 UiBRG register count source cycles.

When the SDHI bit in the UiSMR2 register is set to "1" (SDA output disabled), the SDAi pin is forcibly placed in a high-impedance state. Do not set the SDHI bit on the rising edge of the UARTi transfer clock. The ABT bit in the UiRB register may be set to "1" (detected).

17.3.6 SDA Input

When the IICM2 bit in the UiSMR2 register (i=0 to 4) is set to "0", the first eight bits of received data are stored into bits 7 to 0 (D7 to D0) in the UiRB register. The ninth bit (D8) is ACK or NACK.

When the IICM2 bit is set to "1", the first seven bits (D7 to D1) of received data are stored into bits 6 to 0 in the UiRB register. Store the eighth bit (D0) into bit 8 in the UiRB register.

If the IICM2 bit is set to "1" and the CKPH bit in the UiSMR3 register is set to "1", the same data as that of when setting the IICM2 bit to "0" can be read. To read the data, read the UiRB register after the rising edge of the ninth bit of the transfer clock.

17.3.7 ACK, NACK

When the STPSEL bit in the UiSMR4 register (i=0 to 4) is set to "0" (serial I/O circuit selected) and the ACKC bit in the UiSMR4 register is set to "1" (ACK data output), the SDAi pin provides the value output set in the ACKD bit in the UiSMR4 register.

If the IICM2 bit is set to "0", the NACK interrupt request is generated when the SDAi pin is held high ("H") on the rising edge of the ninth bit of the transfer clock. The ACK interrupt request is generated when the SDAi pin is held low ("L") on the rising edge of the ninth bit of the transfer clock.

When ACK is selected to generate a DMA request, the DMA transfer is activated by an ACK detection.

17.3.8 Transmit and Receive Reset

When the STC bit in the UiSMR2 register (i=0 to 4) is set to "1" (UARTi initialization enabled) and a start condition is detected,

- the transmit shift register is reset and the content of the UiTB register is transferred to the transmit shift register. The first bit starts transmitting when the next clock is input. UARTi output value remains unchanged between when the clock is applied and when the first bit data output is provided. The value remains the same as when start condition was detected.
- the receive shift register is reset and the first bit start receiving when the next clock is applied.
- the SWC bit is set to "1" (SCL wait output enabled). The SCLi pin becomes "L" on the falling edge of the ninth bit of the transfer clock.

If UARTi transmission and reception are started with this function, the TI bit in the UiC1 register remains unchanged. Select the external clock as the transfer clock when using this function.

17.4 Special Mode 2

In special mode 2, serial communication between one or multiple masters and multiple slaves is available. The \overline{SSi} input pin ($i=0$ to 4) controls the serial bus communication. Table 17.19 lists specifications of special mode 2. Table 17.20 lists register settings. Tables 17.21 to 17.23 list pin settings.

Table 17.19 Special Mode 2 Specifications

Item	Specification
Transfer Data Format	Transfer data : 8 bits long
Transfer Clock	<ul style="list-style-type: none"> The CKDIR bit in the UiMR register ($i=0$ to 4) is set to "0" (internal clock selected): $f_j/2(m+1)$ $f_j = f_1, f_8, f_{2n}^{(1)}$ m: setting value of the UiBRG register, 0016 to FF16 The CKDIR bit to "1" (external clock selected) : input from the CLKi pin
Transmit/Receive Control	\overline{SSi} input pin function
Transmit Start Condition	To start transmitting, the following requirements must be met ⁽²⁾ : <ul style="list-style-type: none"> - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the TI bit in the UiC1 register to "0" (data in the UiTB register)
Receive Start Condition	To start receiving, the following requirement must be met ⁽²⁾ : <ul style="list-style-type: none"> - Set the RE bit in the UiC1 register to "1" (receive enable) - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the TI bit in the UiC1 register to "0" (data in the UiTB register)
Interrupt Request Generation Timing	<ul style="list-style-type: none"> While transmitting, the following conditions can be selected: <ul style="list-style-type: none"> - The UiIRS bit in the UiC1 register is set to "0" (no data in a transmit buffer) : when data is transferred from the UiTB register to the UARTi transmit register (transmission started) - The UiIRS register is set to "1" (transmission completed): when data transmission from UARTi transfer register is completed While receiving When data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detection	<ul style="list-style-type: none"> • Overrun error⁽³⁾ This error occurs when the seventh bit of the next received data is read before reading the UiRB register • Fault error In master mode, the fault error occurs an "L" signal is applied to the \overline{SSi} pin
Selectable Function	<ul style="list-style-type: none"> • CLK polarity Select from the rising edge or falling edge of the transfer clock when transferred data is output and input are provided • LSB first or MSB first Data is transmitted or received in either bit 0 or in bit 7 • Continuous receive mode Reception is enabled simultaneously by reading the UiRB register • Serial data logic inverse This function inverses transmitted or received data logically • TxD and RxD I/O polarity inverse TxD pin output and RxD pin input are inversed. All I/O data levels are also inversed • Clock phase Select from one of 4 combinations of transfer data polarity and phases • \overline{SSi} input pin function Output pin is placed in a high-impedance state to avoid data conflict between master and other masters or slaves

NOTES:

- The CNT3 to CNT0 bits in the TCSPPR register select no division ($n=0$) or divide-by-2 n ($n=1$ to 15).
- To start transmission/reception when selecting the external clock, these conditions must be met after the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and data is received on the rising edge) and the CLKi pin is held high ("H"), or when the CKPOL bit is set to "1" (Data is transmitted on the rising edge of the transfer clock and data is received on the falling edge) and the CLKi pin is held low ("L").
- If an overrun error occurs, the UiRB register is in an indeterminate state. The IR bit in the SiRIC register does not change to "1" (interrupt requested).

Table 17.20 Register Settings in Special Mode 2

Register	Bit	Function
UiTB	7 to 0	Set transmit data
UiRB	7 to 0	Received data can be read
	OER	Overflow error flag
UiBRG	7 to 0	Set bit rate
UiMR	SMD2 to SMD0	Set to "0012"
	CKDIR	Set to "0" in master mode or "1" in slave mode
	IOPOL	Set to "0"
UiC0	CLK1, CLK0	Select count source for the UiBRG register
	CRS	Disabled because the CRD bit is set to "1"
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Select the output format of the TxDi pin
	CKPOL	Clock phase can be set by the combination of the CKPOL bit and the CKPH bit in the UiSMR3 register
	UFORM	Select either LSB first or MSB first
UiC1	TE	Set to "1" to enable data transmission and reception
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UIRS	Select what causes the UARTi transmit interrupt to be generated
	UiRRM	Set to "1" to enable continuous receive mode
	UiLCH, SCLKSTPB	Set to "0"
UiSMR	7 to 0	Set to "0016"
UiSMR2	7 to 0	Set to "0016"
UiSMR3	SSE	Set to "1"
	CKPH	Clock phase can be set by the combination of the CKPH bit and the CKPOL bit in the UiC0 register
	DINC	Set to "0" in master mode or "1" in slave mode
	NODC	Set to "0"
	ERR	Fault error flag
	7 to 5	Set to "0002"
UiSMR4	7 to 0	Set to "0016"

i=0 to 4

Table 17.21 Pin Settings in Special Mode 2 (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	SS0 input	PS0_0=0	–	PD6_0=0
P61	CLK0 input (slave)	PS0_1=0	–	PD6_1=0
	CLK0 output (master)	PS0_1=1	–	–
P62	RxD0 input (master)	PS0_2=0	–	PD6_2=0
	STxD0 output (slave)	PS0_2=1	PSL0_2=1	–
P63	TxD0 output (master)	PS0_3=1	–	–
	SRxD0 input (slave)	PS0_3=0	–	PD6_3=0
P64	SS1 input	PS0_4=0	–	PD6_4=0
P65	CLK1 input (slave)	PS0_5=0	–	PD6_5=0
	CLK1 output (master)	PS0_5=1	–	–
P66	RxD1 input (master)	PS0_6=0	–	PD6_6=0
	STxD1 output (slave)	PS0_6=1	PSL0_6=1	–
P67	TxD1 output (master)	PS0_7=1	–	–
	SRxD1 input (slave)	PS0_7=0	–	PD6_7=0

Table 17.22 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output (master)	PS1_0=1	PSL1_0=0	PSC_0=0	–
	SRxD2 input (slave)	PS1_0=0	–	–	PD7_0=0
P71 ⁽¹⁾	RxD2 input (master)	PS1_1=0	–	–	PD7_1=0
	STxD2 output (slave)	PS1_1=1	PSL1_1=1	PSC_1=0	–
P72	CLK2 input (slave)	PS1_2=0	–	–	PD7_2=0
	CLK2 output (master)	PS1_2=1	PSL1_2=0	PSC_2=0	–
P73	SS2 input	PS1_3=0	–	–	PD7_3=0

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 17.23 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P90	CLK3 input (slave)	PS3_0=0	–	PD9_0=0
	CLK3 output (master)	PS3_0=1	–	–
P91	RxD3 input (master)	PS3_1=0	–	PD9_1=0
	STxD3 output (slave)	PS3_1=1	PSL3_1=1	–
P92	TxD3 output (master)	PS3_2=1	PSL3_2=0	–
	SRxD3 input (slave)	PS3_2=0	–	PD9_2=0
P93	SS3 input	PS3_3=0	PSL3_3=0	PD9_3=0
P94	SS4 input	PS3_4=0	PSL3_4=0	PD9_4=0
P95	CLK4 input (slave)	PS3_5=0	PSL3_5=0	PD9_5=0
	CLK4 output (master)	PS3_5=1	–	–
P96	TxD4 output (master)	PS3_6=1	–	–
	SRxD4 input (slave)	PS3_6=0	PSL3_6=0	PD9_6=0
P97	RxD4 input (master)	PS3_7=0	–	PD9_7=0
	STxD4 output (slave)	PS3_7=1	PSL3_7=1	–

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

17.4.1 \overline{SS}_i Input Pin Function (i=0 to 4)

When the SSE bit in the UiSMR3 register is set to "1" (\overline{SS} function enabled), the special mode 2 is selected, activating the pin function.

The DINC bit in the UiSMR3 register determines which microcomputer performs as master or slave. When multiple microcomputers perform as the masters (multi-master system), the \overline{SS}_i pin setting determines which master microcomputer is active and when.

17.4.1.1 When Setting the DINC Bit to "1" (Slave Mode)

When a high-level ("H") signal is applied to the \overline{SS}_i pin, the STxDi and SRxDi pins are placed in a high-impedance state and the transfer clock applied to the CLKi pin is ignored. When a low-level ("L") signal is applied to the \overline{SS}_i input pin, the transfer clock input is valid and serial communication is enabled.

17.4.1.2 When Setting the DINC Bit to "0" (Master Mode)

When using the \overline{SS}_i pin function in master mode, set the UiIRS bit in the UiC1 register to "1" (transmission completed).

When an "H" signal is applied to the \overline{SS}_i pin, serial communication is available due to transmission privilege. The master provides the transfer clock output. When an "L" signal is applied to the \overline{SS}_i pin, it indicates that another master is active. The TxDi and CLKi pins are placed in high-impedance states and the ERR bit in the UiSMR3 register is set to "1" (fault error). Use the transmit complete interrupt routine to verify the ERR bit state.

To resume the serial communication after the fault error occurs, set the ERR bit to "0" while applying the "H" signal to the \overline{SS}_i pin. The TxDi and CLKi pins become ready for signal outputs.

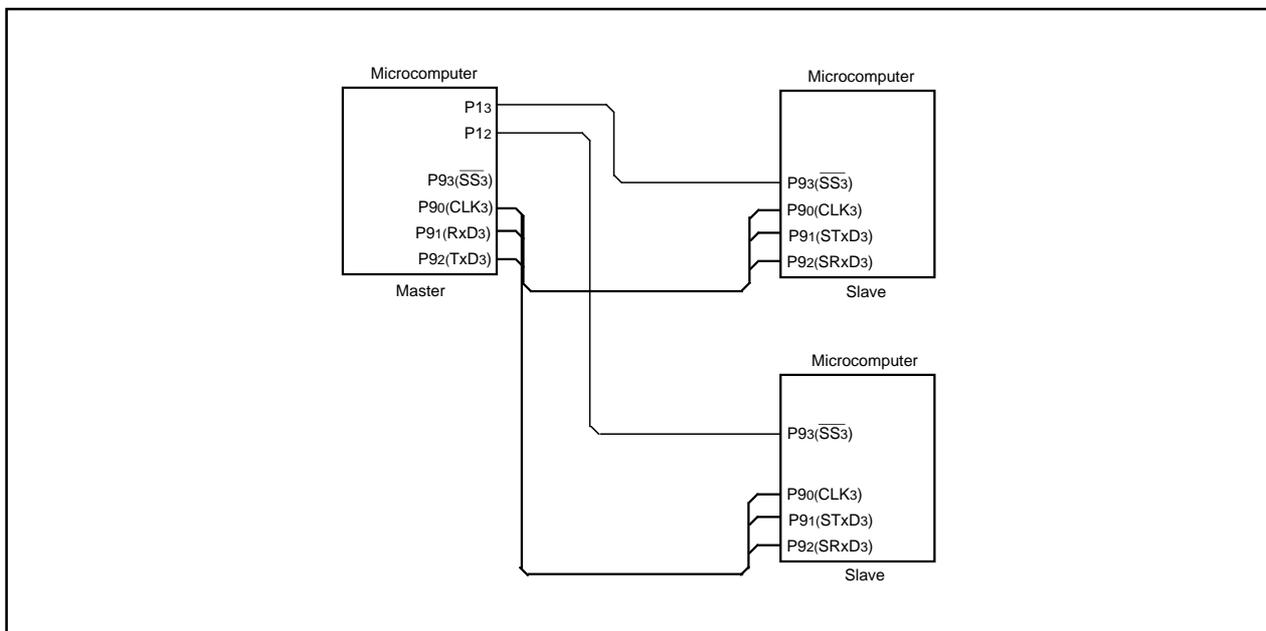


Figure 17.23 Serial Bus Communication Control with SS Pin

17.4.2 Clock Phase Setting Function

The CKPH bit in the UiSMR3 register (i=0 to 4) and the CKPOL bit in the UiC0 register select one of four combinations of transfer clock polarity and phases.

The transfer clock phase and polarity must be the same between the master and the slave involved in the transfer.

17.4.2.1 When setting the DINC Bit to "0" (Master (Internal Clock))

Figure 17.24 shows transmit and receive timing.

17.4.2.2 When Setting the DINC Bit to "1" (Slave (External Clock))

When the CKPH bit is set to "0" (no clock delay) and the \overline{SSi} input pin is held high ("H"), the STxDi pin is placed in a high-impedance state. When the \overline{SSi} input pin becomes low ("L"), conditions to start a serial transfer are met, but output is indeterminate. The serial transmission is synchronized with the transfer clock. Figure 17.25 shows the transmit and receive timing.

When the CKPH bit is set to "1" (clock delay) and the \overline{SSi} input pin is held high, the STxDi pin is placed in a high-impedance state. When the \overline{SSi} pin becomes low, the first data is output. The serial transmission is synchronized with the transfer clock. Figure 17.26 shows the transmit and receive timing.

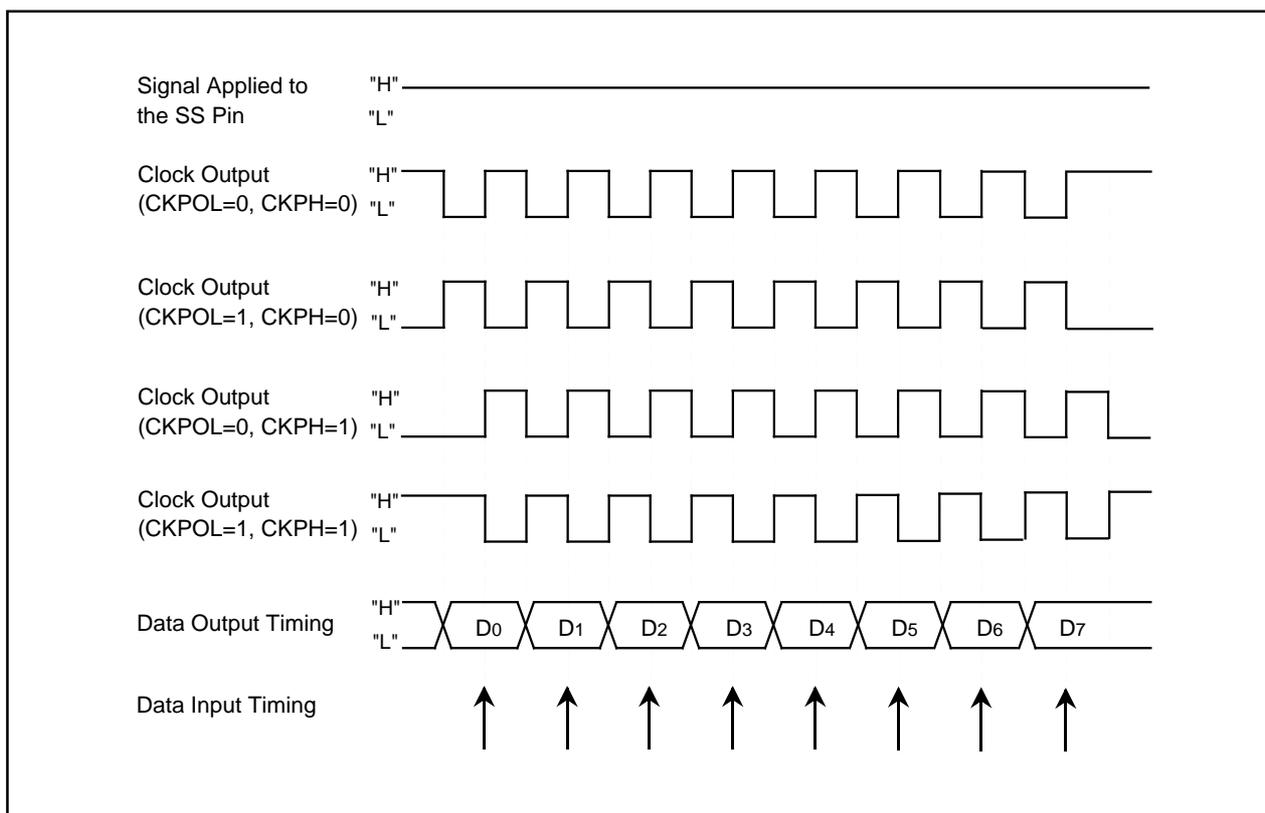


Figure 17.24 Transmit and Receive Timing in Master Mode (Internal Clock)

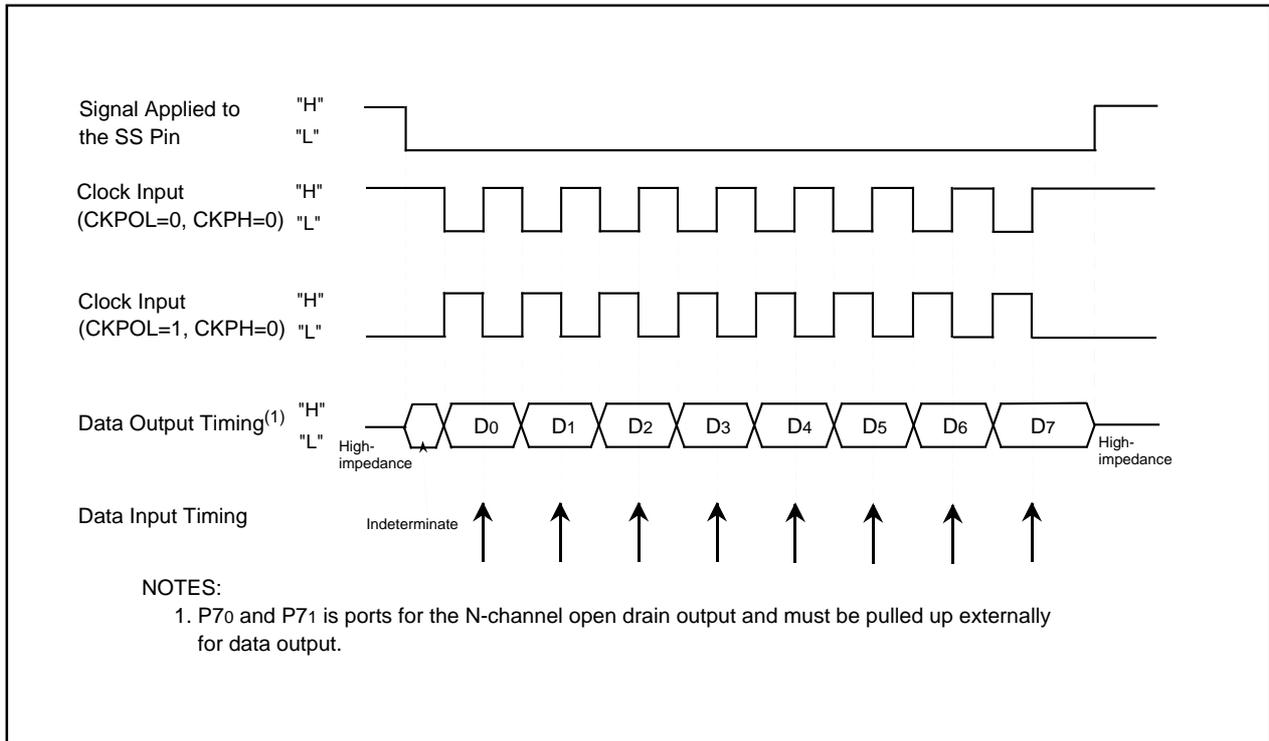


Figure 17.25 Transmit and Receive Timing in Slave Mode (External Clock) (CKPH=0)

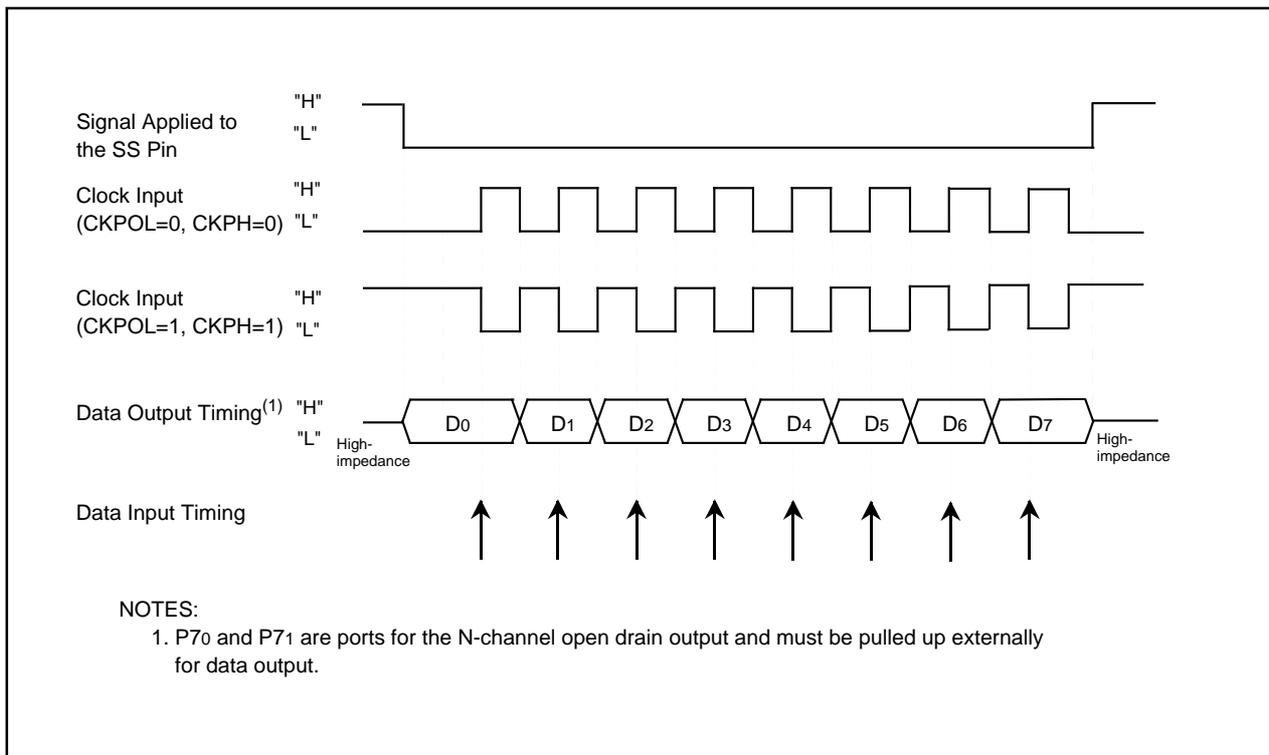


Figure 17.26 Transmit and Receive Timing in Slave Mode (External Clock) (CKPH=1)

17.5 Special Mode 3 (GCI Mode)

In GCI mode, the external clock is synchronized with the transfer clock used in the clock synchronous serial I/O mode.

Table 17.24 lists specifications of GCI mode. Table 17.25 lists registers settings. Tables 17.26 to 17.28 list pin settings.

Table 17.24 GCI Mode Specifications

Item	Specification
Transfer Data Format	Transfer data : 8 bits long
Transfer Clock	The CKDIR bit in the UiMR register (i=0 to 4) is set to "1" (external clock selected): input from the CLKi pin
Clock Synchronization Function	Trigger signal input from the $\overline{\text{CTS}}_i$ pin
Transmit/Receive Start Condition	To start data transmission and reception, meet the following conditions and then apply a trigger signal to the $\overline{\text{CTS}}_i$ pin: <ul style="list-style-type: none"> - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the RE bit in the UiC1 register to "1" (receive enable) - Set the TI bit in the UiC1 register to "0" (Data in the UiTB register)
Interrupt Request Generation Timing	<ul style="list-style-type: none"> • While transmitting, the following condition can be selected: <ul style="list-style-type: none"> - The UiIRS bit in the UiC1 register is set to "0" (UiTB register empty): when data is transferred from the UiTB register to the UARTi transmit register (transmission started) - The UiIRS bit is set to "1" (Transmit completed): when a data transmission from the UARTi transfer register is completed • While receiving, when data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detection	Overrun error ⁽¹⁾ This error occurs when the seventh bit of the next received data is read before reading the UiRB register.

NOTES:

1. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register does not change to "1" (interrupt requested).

Table 17.25 Register Settings in GCI Mode

Register	Bit	Function
UiTB	7 to 0	Set transmit data
UiRB	7 to 0	Received data
	OER	Overflow error flag
UiBRG	7 to 0	Set to "0016"
UiMR	SMD2 to SMD0	Set to "0012"
	CKDIR	Set to "1"
	IOPOL	Set to "0"
UiC0	CLK1, CLK0	Set to "002"
	CRS	Disabled because the CRD bit is set to "1"
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Select the output format of the TxDi pin
	CKPOL	Set to "0"
	UFORM	Set to "0"
UiC1	TE	Set to "1" to enable data transmission and reception
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select what causes the UARTi transmit interrupt to be generated
	UiRRM, UiLCH	Set to "0"
	SCLKSTPB	Set to "0"
UiSMR	6 to 0	Set to "00000002"
	SCLKDIV	See Table 17.29
UiSMR2	6 to 0	Set to "00000002"
	SU1HIM	See Table 17.29
UiSMR3	2 to 0	Set to "0002"
	NODC	Set to "0"
	7 to 4	Set to "00002"
UiSMR4	7 to 0	Set to "0016"

i=0 to 4

Table 17.26 Pin Settings in GCI Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P60	$\overline{\text{CTS0}}$ input ⁽¹⁾	PS0_0=0	–	PD6_0=0
P61	CLK0 input	PS0_1=0	–	PD6_1=0
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P64	$\overline{\text{CTS1}}$ input ⁽¹⁾	PS0_4=0	–	PD6_4=0
P65	CLK1 input	PS0_5=0	–	PD6_5=0
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

NOTES:

1. CTS input is used as a trigger signal input.

Table 17.27 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71 ⁽¹⁾	RxD2 input	PS1_1=0	–	–	PD7_1=0
P72	CLK2 input	PS1_2=0	–	–	PD7_2=0
P73	$\overline{\text{CTS2}}$ input ⁽²⁾	PS1_3=0	–	–	PD7_3=0

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.
2. CTS input is used as a trigger signal input.

Table 17.28 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P90	CLK3 input	PS3_0=0	–	PD9_0=0
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P93	$\overline{\text{CTS3}}$ input ⁽²⁾	PS3_3=0	PSL3_3=0	PD9_3=0
P94	$\overline{\text{CTS4}}$ input ⁽²⁾	PS3_4=0	PSL3_4=0	PD9_4=0
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.
2. CTS input is used for a trigger signal input.

To generate the internal clock synchronized with the external clock, set the SU1HIM bit in the UiSMR2 register (i=0 to 4) and the SCLKDIV bit in the UiSMR register to values shown in Table 17.29. Then apply a trigger signal to the $\overline{\text{CTS}}_i$ pin. Either the same clock cycle as the external clock or external clock divided by two can be selected as the transfer clock. The SCLKSTPB bit in the UiC1 register controls the transfer clock. Set the SCLKSTPB bit accordingly, to start or stop the transfer clock during an external clock operation. Figure 17.27 shows an example of the clock-divided synchronous function.

Table 17.29 Clock-Divided Synchronous Function Select

SCLKDIV Bit in UiSMR Register	SU1HIM Bit in UiSMR2 Register	Clock-Divided Synchronous Function	Example of Waveform
0	0	Not synchronized	-
0	1	Same division as the external clock	A in Figure 17.27
1	0 or 1	Same division as the external clock divided by 2	B in Figure 17.27

i=0 to 4

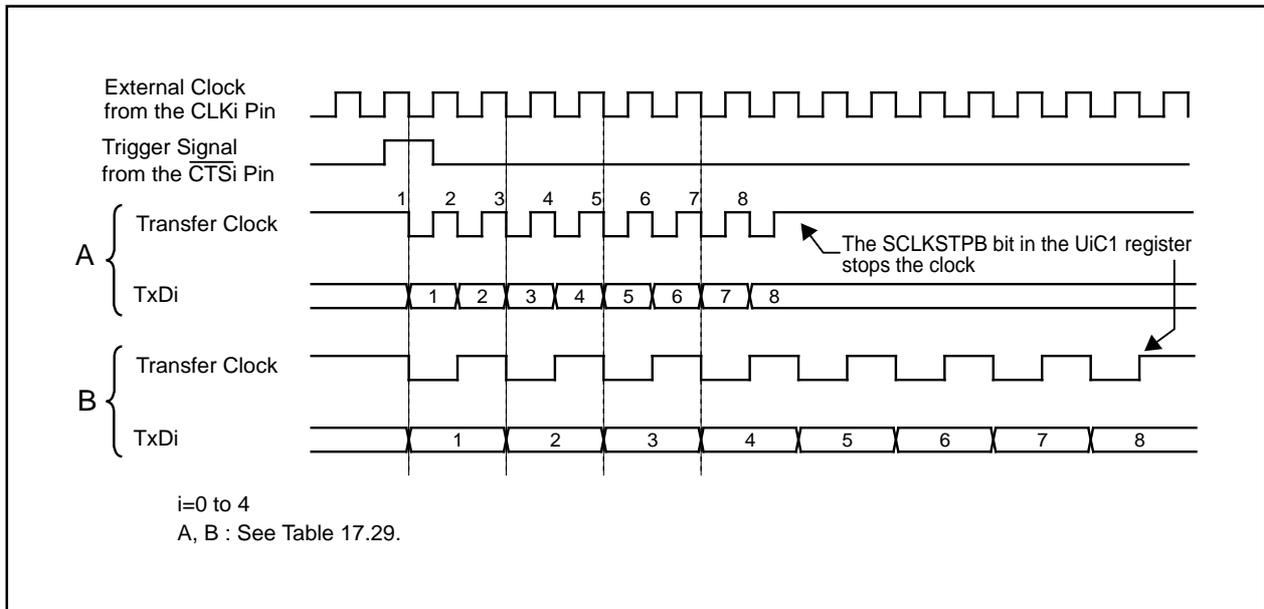


Figure 17.27 Clock-Divided Synchronous Function

17.6 Special Mode 4 (IE Mode)

In IE mode, devices connected with the IEBus can communicate in UART mode.

Table 17.30 lists register settings. Tables 17.31 to 17.33 list pin settings.

Table 17.30 Register Settings in IE Mode

Register	Bit	Function
UiTB	8 to 0	Set transmit data
UiRB	8 to 0	Received data can be read
	OER, FER, PER, SUM	Error flags
UiBRG	7 to 0	Set bit rate
UiMR	SMD2 to SMD0	Set to "1102"
	CKDIR	Select the internal clock or external clock
	STPS	Set to "0"
	PRY	Disabled because the PRYE bit is set to "0"
	PRYE	Set to "0"
	IOPOL	Select TxD and RxD I/O polarity
UiC0	CLK1, CLK0	Select count source for the UiBRG register
	CRS	Disabled because the CRD bit is set to "1"
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Select output format of the TxDi pin
	CKPOL	Set to "0"
	UFORM	Set to "0"
UiC1	TE	Set to "1" to enable data transmission
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Select what causes the UARTi transmit interrupt to be generated
	UiRRM, UiLCH, SCLKSTPB	Set to "0"
UiSMR	3 to 0	Set to "00002"
	ABSCS	Select bus conflict detect sampling timing
	ACSE	Set to "1" to automatically clear the transmit enable bit
	SSS	Select transmit start condition
	SCLKDIV	Set to "0"
UiSMR2	7 to 0	Set to "0016"
UiSMR3	7 to 0	Set to "0016"
UiSMR4	7 to 0	Set to "0016"
IFSR	IFSR6, IFSR7	Select how the bus conflict interrupt occurs

i=0 to 4

Table 17.31 Pin Settings in IE Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P61	CLK0 input	PS0_1=0	–	PD6_1=0
	CLK0 output	PS0_1=1	–	–
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P65	CLK1 input	PS0_5=0	–	PD6_5=0
	CLK1 output	PS0_5=1	–	–
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

Table 17.32 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71 ⁽¹⁾	RxD2 input	PS1_1=0	–	–	PD7_1=0
P72	CLK2 input	PS1_2=0	–	–	PD7_2=0
	CLK2 output	PS1_2=1	PSL1_2=0	PSC_2=0	–

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 17.33 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P90	CLK3 input	PS3_0=0	–	PD9_0=0
	CLK3 output	PS3_0=1	–	–
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P95	CLK4 input	PS3_5=0	PSL3_5=0	PD9_5=0
	CLK4 output	PS3_5=1	–	–
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

If the output signal level of the TxDi pin (i=0 to 4) differs from the input signal level of the RxDi pin, an interrupt request is generated.

UART0 and UART3 are assigned software interrupt number 40. UART1 and UART4 are assigned number 41. When using the bus conflict detect function of UART0 or UART3, of UART1 or UART4, set the IFSR6 bit and the IFSR7 bit in the IFSR register accordingly.

When the ABSCS bit in the UiSMR register is set to "0" (rising edge of the transfer clock), it is determined, on the rising edge of the transfer clock, if the output level of the TxD pin and the input level of the RxD pin match. When the ABSCS bit is set to "1" (timer Aj underflow), it is determined when the timer Aj (timer A3 in UART0, timer A4 in UART1, timer A0 in UART2, timer A3 in UART3, the timer A4 in UART4) counter overflows. Use the timer Aj in one-shot timer mode.

When the ACSE bit in the UiSMR register is set to "1" (automatic clear at bus conflict) and the IR bit in the BCNiIC register to "1" (discrepancy detected), the TE bit in the UiC1 register is set to "0" (transmit disable).

When the SSS bit in the UiSMR register is set to "1" (synchronized with RxDi), data is transmitted from the TxDi pin on the falling edge of the RxDi pin. Figure 17.28 shows bits associated with the bus conflict detect function.

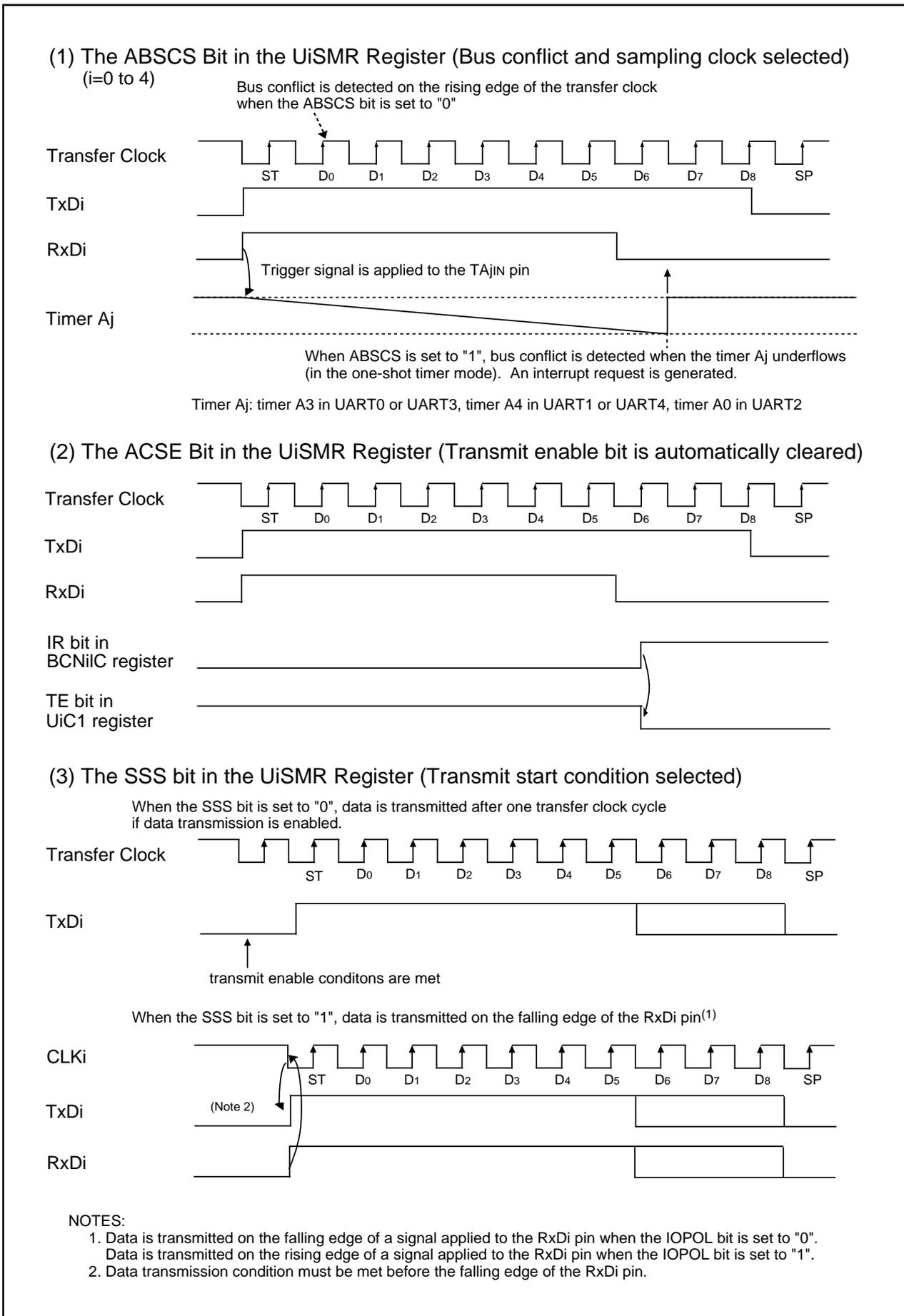


Figure 17.28 Bit Function Related Bus Conflict Detection

17.7 Special Mode 5 (SIM Mode)

In SIM mode, SIM interface devices can communicate in UART mode. Both direct and inverse formats are available and a low-level ("L") signal output can be provided from the TxDi pin (i=0 to 4) when a parity error is detected.

Table 17.34 lists specifications of SIM mode. Table 17.35 lists register settings. Tables 17.36 to 17.38 list pin settings.

Table 17.34 SIM Mode Specifications

Item	Specification
Transfer Data Format	<ul style="list-style-type: none"> • Transfer data: 8-bit UART mode • In direct format Parity: Even Data logic: Direct Transfer format: LSB first
	<ul style="list-style-type: none"> • One stop bit • In inverse format Parity: Odd Data logic: Inverse Transfer format: MSB first
Transfer Clock	<ul style="list-style-type: none"> • The CKDIR bit in the UiMR register (i=0 to 4) is "0" (internal clock selected): $f_i/16(m+1)^{f_1}$ $f_j = f_1, f_8, f_{2n}^{(2)}$ m: setting value of the UiBRG register, 00₁₆ to FF₁₆ Do not set the CKDIR bit to "1" (external clock selected)
Transmit/Receive Control	The CRD bit in the UiC0 register is set to "1" ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$ function disabled)
Other Setting Items	The UiIRS bit in the UiC1 register is set to "1" (transmission completed)
Transmit Start Condition	To start transmitting, the following requirements must be met: <ul style="list-style-type: none"> - Set the TE bit in the UiC1 register to "1" (transmit enable) - Set the TI bit in the UiC1 register to "0" (data in the UiTB register)
Receive Start Condition	To start receiving, the following requirements must be met: <ul style="list-style-type: none"> - Set the RE bit in the UiC1 register to "1" (receive enable) - Detect the start bit
Interrupt Request Generation Timing	<ul style="list-style-type: none"> • While transmitting, <ul style="list-style-type: none"> -The UiIRS bit is set to "1" (transmission completed): when data transmission from the UARTi transfer register is completed • While receiving, <ul style="list-style-type: none"> when data is transferred from the UARTi receive register to the UiRB register (reception completed)
Error Detection	<ul style="list-style-type: none"> • Overrun error⁽¹⁾ <ul style="list-style-type: none"> This error occurs when the eighth bit of the next data is received before reading the UiRB register • Framing error <ul style="list-style-type: none"> This error occurs when the number of the stop bit set is not detected • Parity error <ul style="list-style-type: none"> This error occurs when the number of "1" in parity bit and character bits differs from the number set • Error sum flag <ul style="list-style-type: none"> The SUM bit is set to "1" when an overrun error, framing error or parity error occurs

NOTES:

1. If an overrun error occurs, the UiRB register is indeterminate. The IR bit in the SiRIC register does not change to "1" (interrupt requested).
2. The CNT3 to CNT0 bits in the TCSPR register select no division (n=0) or divide-by-2n (n=1 to 15).

Table 17.35 Register Settings in SIM Mode

Register	Bit	Function
UiTB	7 to 0	Set transmit data
UiRB	7 to 0	Received data can be read
	OER, FER, PER, SUM	Error flags
UiBRG	7 to 0	Set bit rate
UiMR	SMD2 to SMD0	Set to "1012"
	CKDIR	Set to "0"
	STPS	Set to "0"
	PRY	Set to "1" for direct format or "0" for inverse format
	PRYE	Set to "1"
	IOPOL	Set to "0"
UiC0	CLK1, CLK0	Select count source for the UiBRG register
	CRS	Disabled because the CRD bit is set to "1"
	TXEPT	Transfer register empty flag
	CRD	Set to "1"
	NCH	Set to "1"
	CKPOL	Set to "0"
	UFORM	Set to "0" for direct format or "1" for inverse format
UiC1	TE	Set to "1" to enable data transmission
	TI	Transfer buffer empty flag
	RE	Set to "1" to enable data reception
	RI	Reception complete flag
	UiIRS	Set to "1"
	UiRRM	Set to "0"
	UiLCH	Set to "0" for direct format or "1" for inverse format
	UiERE	Set to "1"
UiSMR	7 to 0	Set to "0016"
UiSMR2	7 to 0	Set to "0016"
UiSMR3	7 to 0	Set to "0016"
UiSMR4	7 to 0	Set to "0016"

i=0 to 4

Table 17.36 Pin Settings in SIM Mode (1)

Port	Function	Setting		
		PS0 Register	PSL0 Register	PD6 Register
P62	RxD0 input	PS0_2=0	–	PD6_2=0
P63	TxD0 output	PS0_3=1	–	–
P66	RxD1 input	PS0_6=0	–	PD6_6=0
P67	TxD1 output	PS0_7=1	–	–

Table 17.37 Pin Settings (2)

Port	Function	Setting			
		PS1 Register	PSL1 Register	PSC Register	PD7 Register
P70 ⁽¹⁾	TxD2 output	PS1_0=1	PSL1_0=0	PSC_0=0	–
P71 ⁽¹⁾	RxD2 input	PS1_1=0	–	–	PD7_1=0

NOTES:

1. P70 and P71 are ports for the N-channel open drain output.

Table 17.38 Pin Settings (3)

Port	Function	Setting		
		PS3 Register ⁽¹⁾	PSL3 Register	PD9 Register ⁽¹⁾
P91	RxD3 input	PS3_1=0	–	PD9_1=0
P92	TxD3 output	PS3_2=1	PSL3_2=0	–
P96	TxD4 output	PS3_6=1	–	–
P97	RxD4 input	PS3_7=0	–	PD9_7=0

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set to the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

Figure 17.29 shows an example of a SIM interface operation. Figure 17.30 shows an example of a SIM interface connection. Connect the TxDi pin to the RxDi pin for a pull-up.

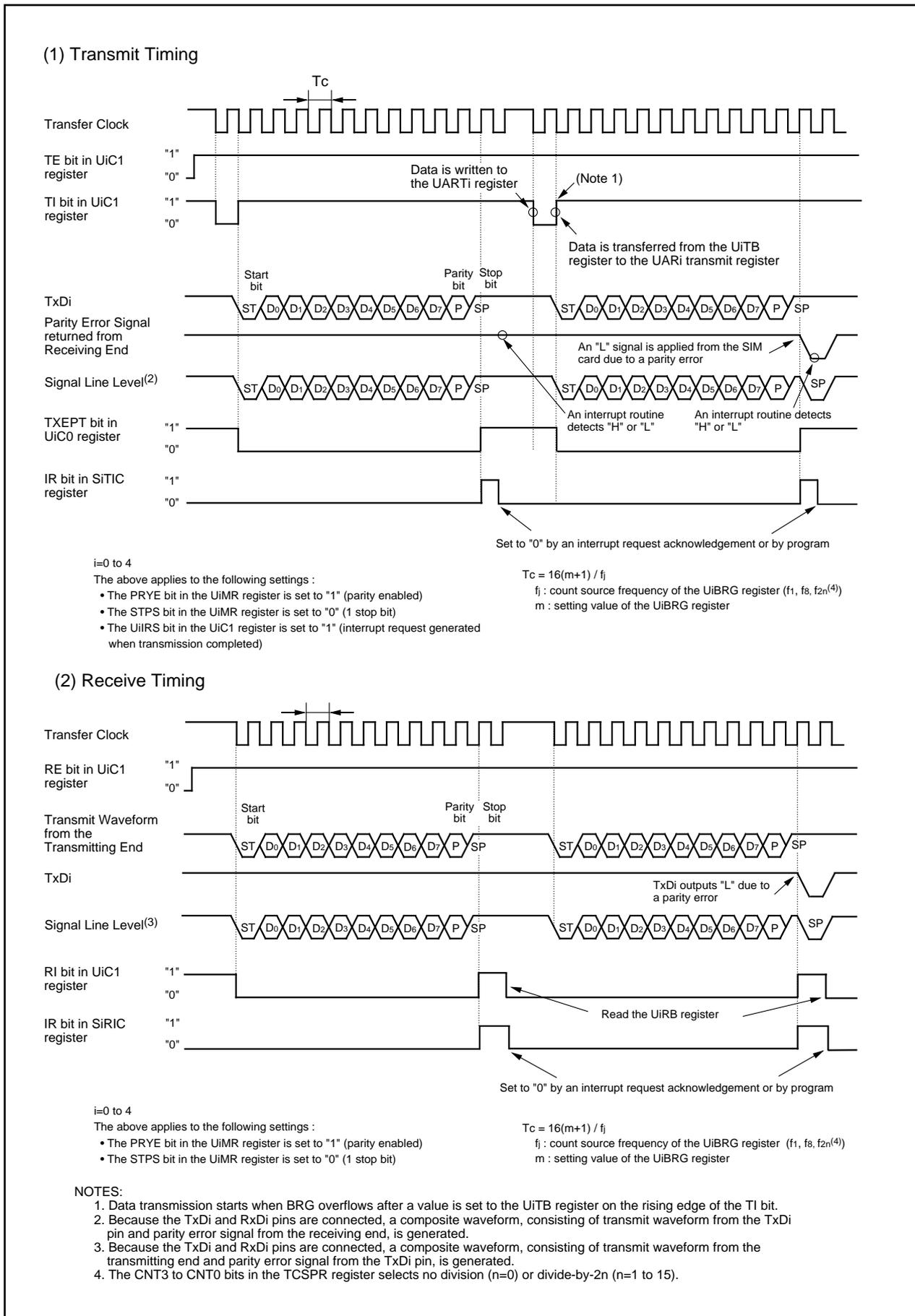


Figure 17.29 SIM Interface Operation

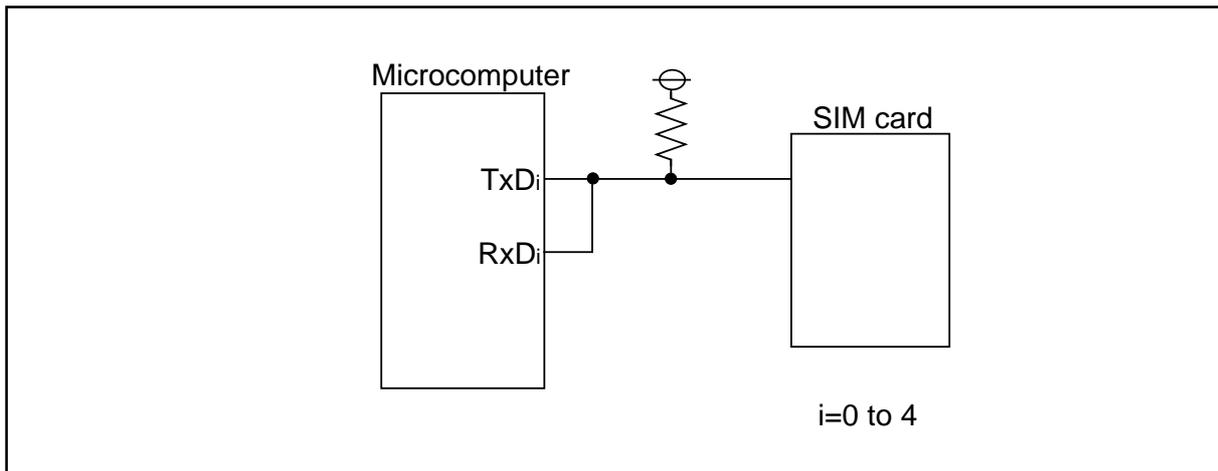


Figure 17.30 SIM Interface Connection

17.7.1 Parity Error Signal

17.7.1.1 Parity Error Signal Output Function

When the UiERE bit in the UiC1 register (i=0 to 4) is set to "1", the parity error signal output can be provided. The parity error signal output is provided when a parity error is detected upon receiving data. A low-level ("L") signal output is provided from the TxDi pin in the timing shown in Figure 17.31. When reading the UIRB register during a parity error output, the PER bit in the UIRB register is set to "0" and a high-level ("H") signal output is again provided simultaneously.

17.7.1.2 Parity Error Signal

To determine whether the parity error signal is output, the port that shares a pin with the RxDi pin is read by using an end-of-transmit interrupt routine.

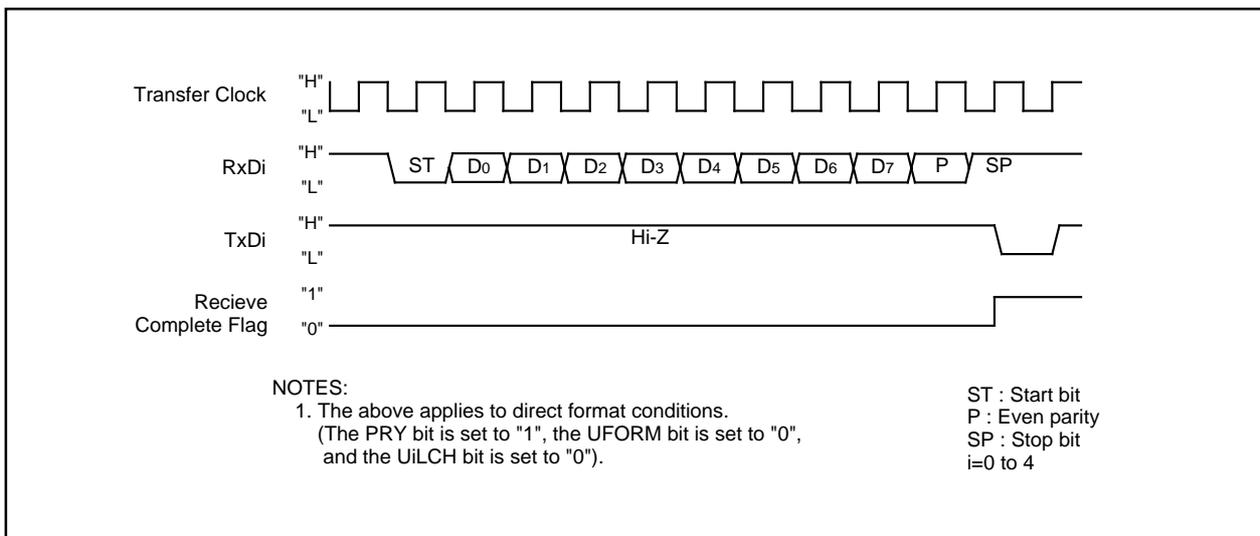


Figure 17.31 Parity Error Signal Output Timing (LSB First)

17.7.2 Format

17.7.2.1 Direct Format

Set the PRYE bit in the UiMR register (i=0 to 4) to "1" (parity enabled), the PRY bit to "1" (even parity), the UFORM bit in the UiC0 register to "0" (LSB first) and the UiLCH bit in the UiC1 register to "0" (not inverted). When data are transmitted, data set in the UiTB register are transmitted with the even-numbered parity, starting from D0. When data are received, received data are stored in the UiRB register, starting from D0. The even-numbered parity determines whether a parity error occurs.

17.7.2.2 Inverse Format

Set the PRYE bit to "1", the PRY bit to "0" (odd parity), the UFORM bit to "1" (MSB first) and the UiLCH bit to "1" (inverted). When data are transmitted, values set in the UiTB register are logically inverted and are transmitted with the odd-numbered parity, starting from D7. When data are received, received data are logically inverted to be stored in the UiRB register, starting from D7. The odd-numbered parity determines whether a parity error occurs.

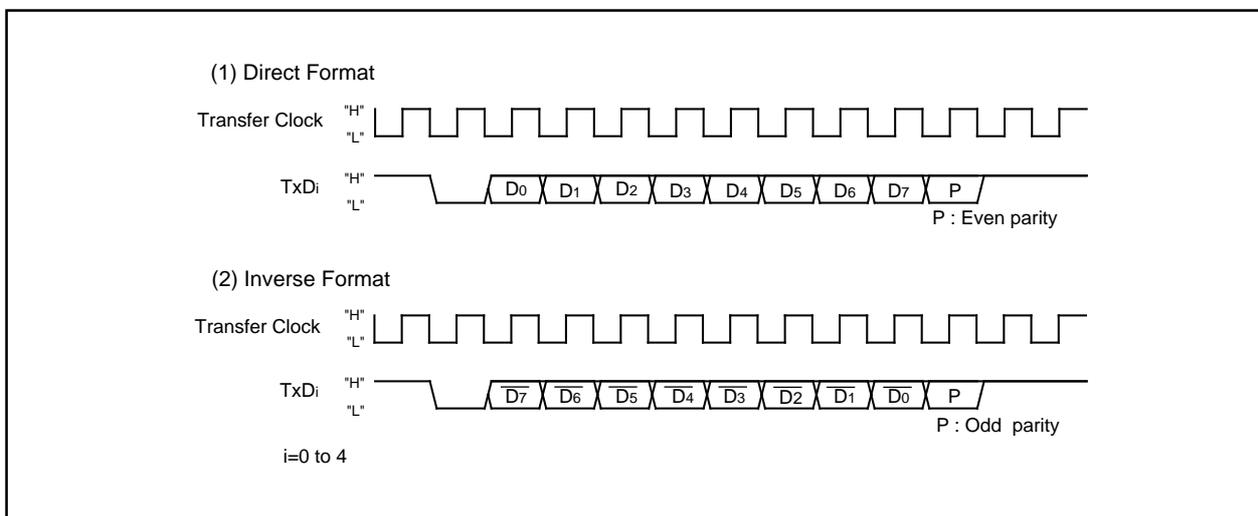


Figure 17.32 SIM Interface Format

18. A/D Converter

The A/D converter consists of one 10-bit successive approximation A/D converter with a capacitive coupling amplifier.

The result of an A/D conversion is stored into the A/D registers corresponding to selected pins. It is stored into the AD00 register only when DMAC operating mode is entered.

Table 18.1 lists specifications of the A/D converter. Figure 18.1 shows a block diagram of the A/D converter. Figures 18.2 to 18.6 show registers associated with the A/D converter.

NOTE

This section is described in the 144-pin package only as an example.
The AN150 to AN157 pins are not included in the 100-pin package.

Table 18.1 A/D Converter Specifications

Item	Specification
A/D Conversion Method	Successive approximation (with a capacitive coupling amplifier)
Analog Input Voltage ⁽¹⁾	0V to AVCC (VCC1)
Operating Clock, ϕ_{AD} ⁽²⁾	fAD, fAD/2, fAD/3, fAD/4, fAD/6, fAD/8
Resolution	Select from 8 bits or 10 bits
Operating Mode	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, repeat sweep mode 1, multi-port single sweep mode, multi-port repeat sweep mode 0
Analog Input Pins ⁽³⁾	34 pins 8 pins each for AN (AN0 to AN7), AN0 (AN00 to AN07), AN2 (AN20 to AN27), AN15 (AN150 to AN157) 2 extended input pins (ANEX0 and ANEX1)
A/D Conversion Start Condition	<ul style="list-style-type: none"> • Software trigger The ADST bit in the AD0CON0 register is set to "1" (A/D conversion started) by program • External trigger (re-trigger is enabled) When a falling edge is applied to the \overline{ADTRG} pin after the ADST bit is set to "1" by program • Hardware trigger (re-trigger is enabled) The timer B2 interrupt request of the three-phase motor control timer functions (after the ICTB2 counter completes counting) is generated after the ADST bit is set to "1" by program
Conversion Rate Per Pin	<ul style="list-style-type: none"> • Without the sample and hold function 8-bit resolution : 49 ϕ_{AD} cycles 10-bit resolution : 59 ϕ_{AD} cycles • With the sample and hold function 8-bit resolution : 28 ϕ_{AD} cycles 10-bit resolution : 33 ϕ_{AD} cycles

NOTES:

1. Analog input voltage is not affected by the sample and hold function status.
2. ϕ_{AD} frequency must be under 16 MHz when VCC1=5V.
 ϕ_{AD} frequency must be under 10 MHz when VCC1=3.3V.
Without the sample and hold function, the ϕ_{AD} frequency is 250 kHz or more.
With the sample and hold function, the ϕ_{AD} frequency is 1 MHz or more.
3. AVCC = VREF = VCC1 \geq VCC2, A/D input voltage (for AN0 to AN7, AN150 to AN157, ANEX0 and ANEX1) \leq VCC1, A/D input voltage (for AN00 to AN07 and AN20 to AN27) \leq VCC2.

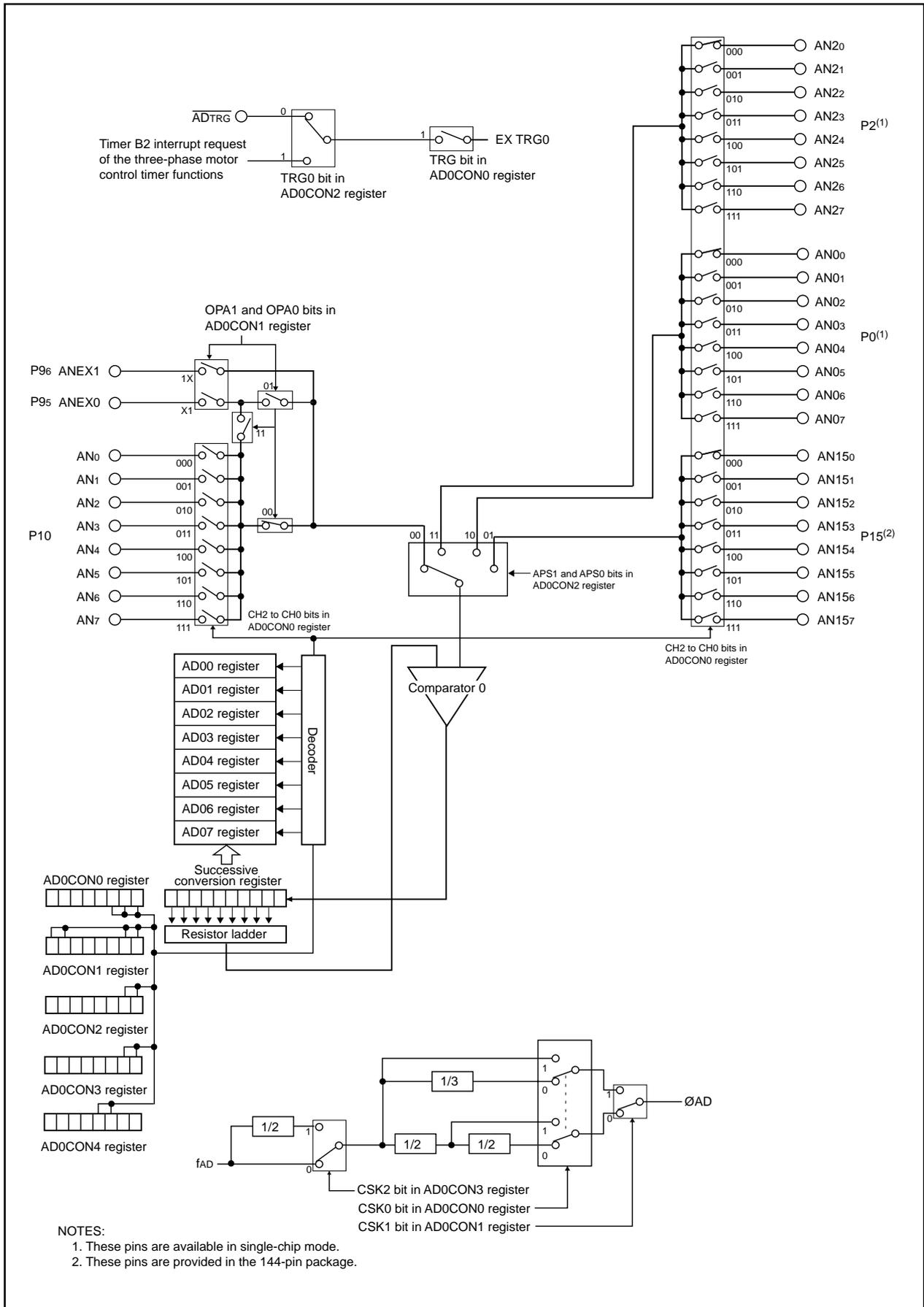


Figure 18.1 A/D Converter Block Diagram

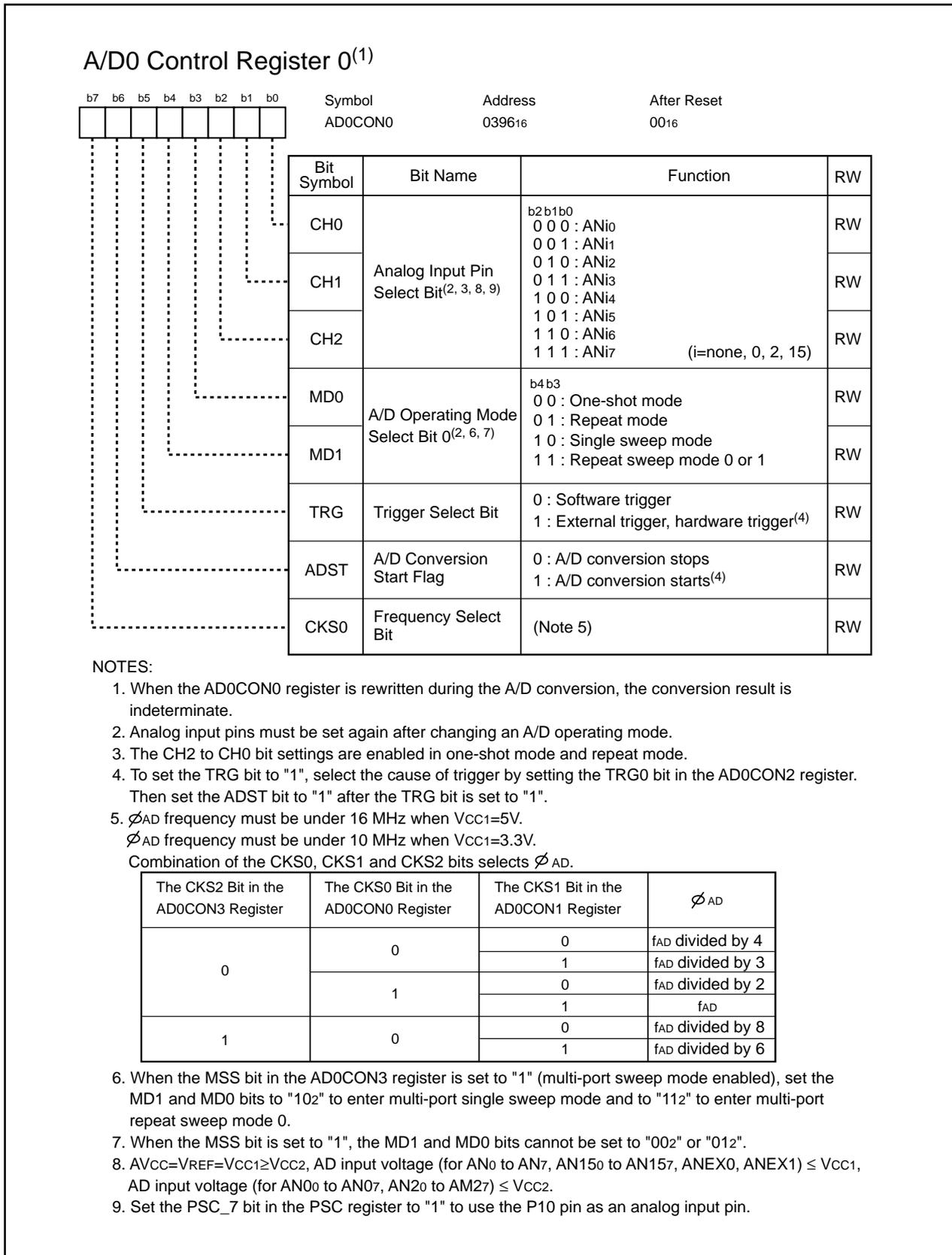


Figure 18.2 AD0CON0 Register

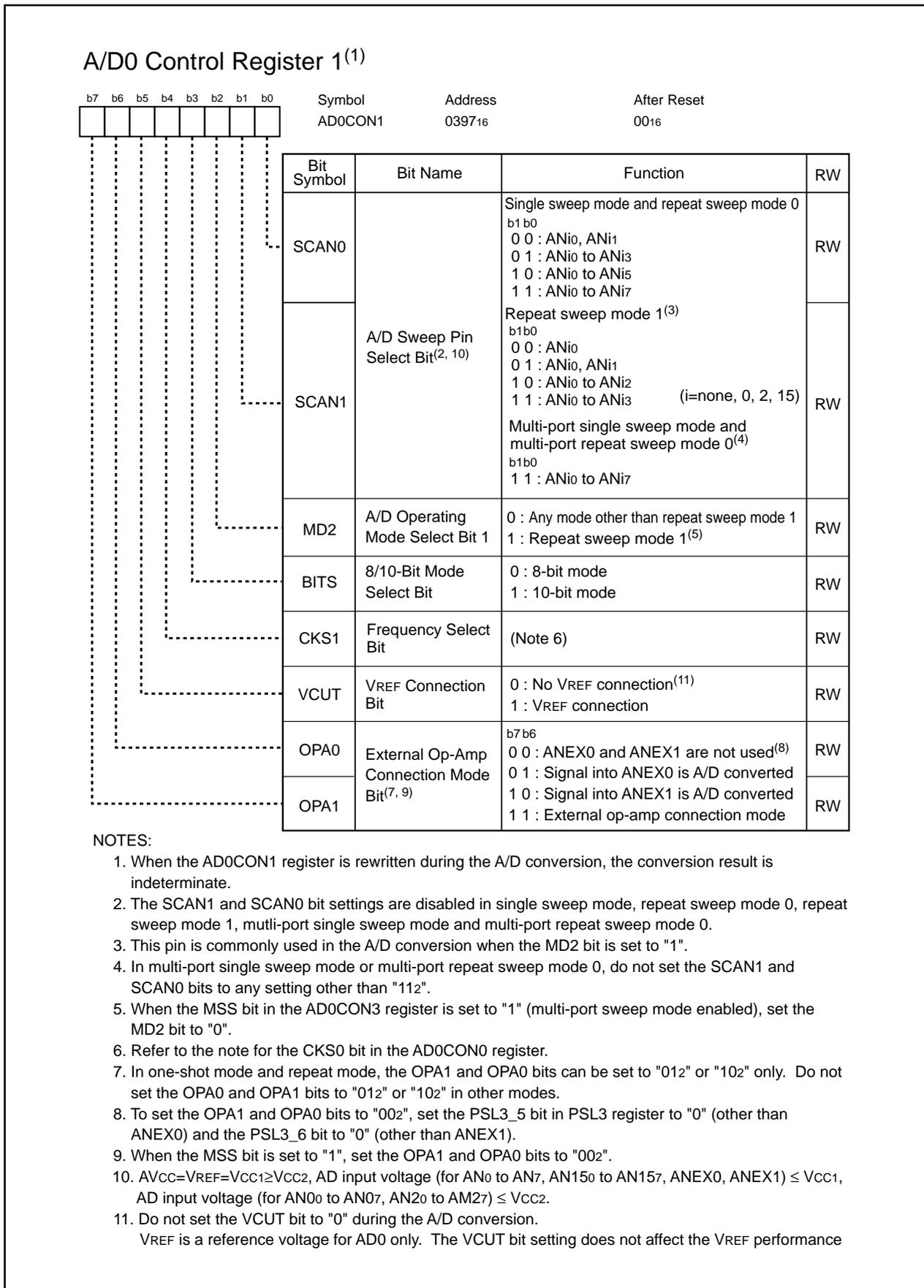


Figure 18.3 AD0CON1 Register

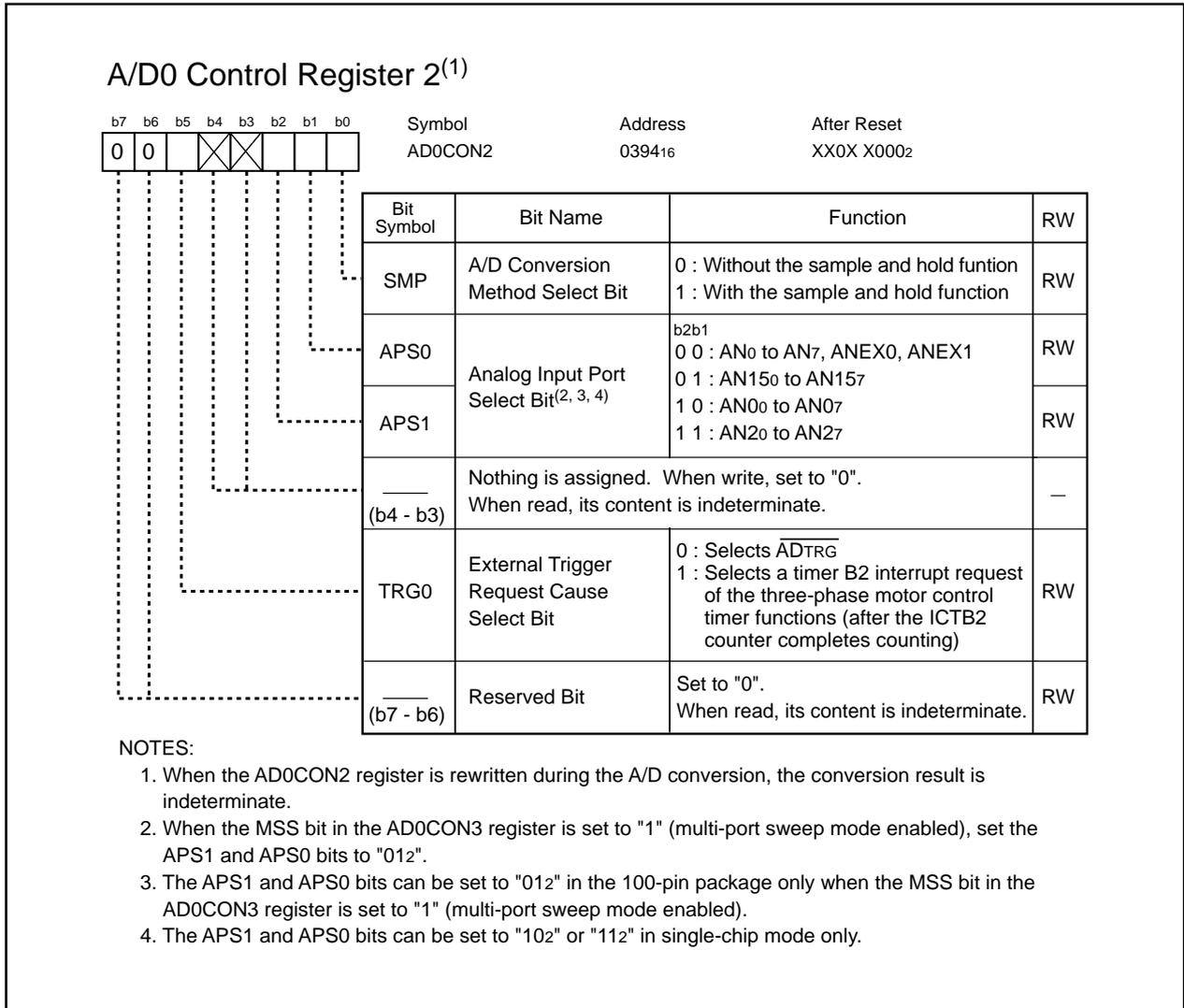


Figure 18.4 AD0CON2 Register

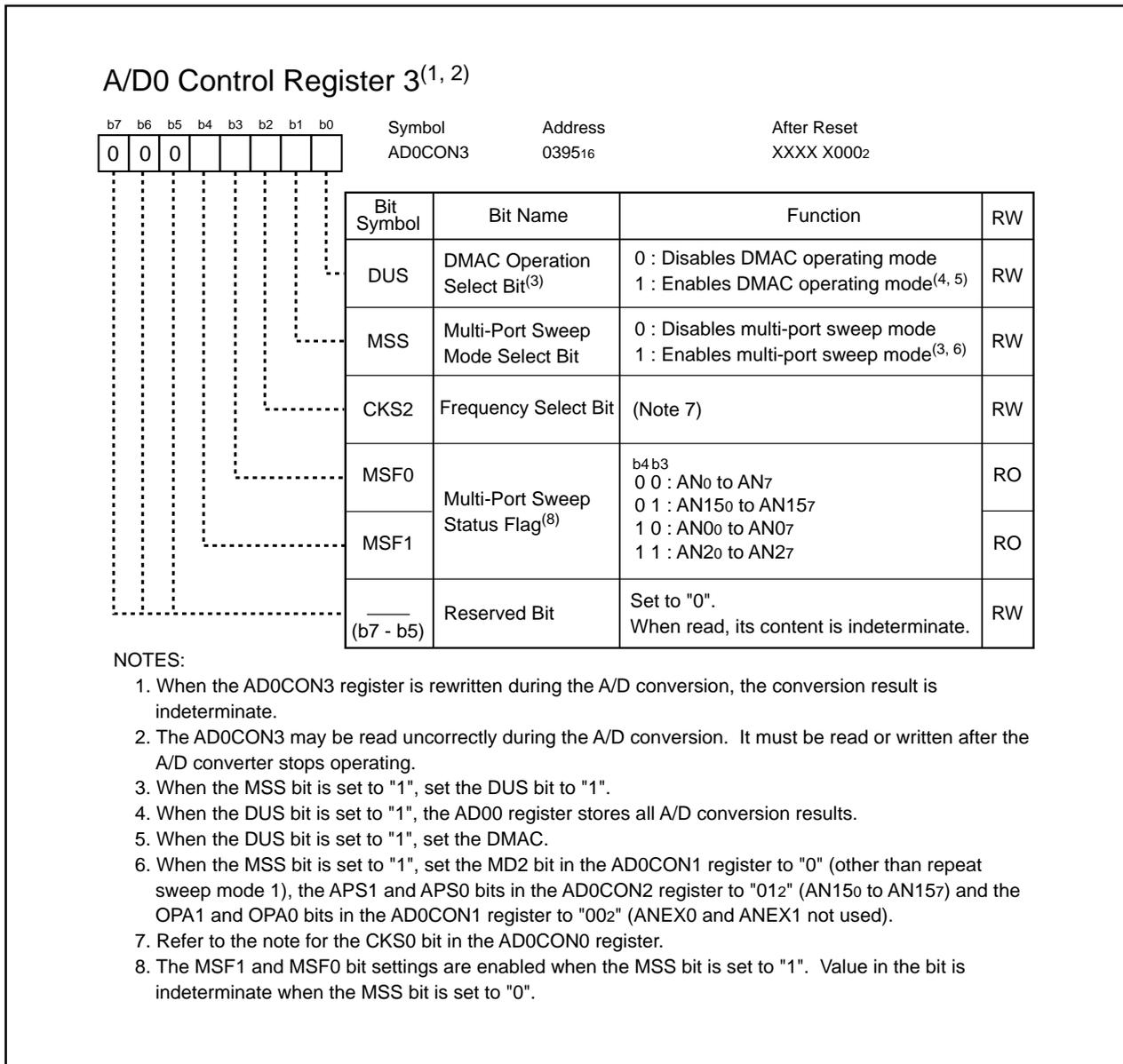


Figure 18.5 AD0CON3 Register

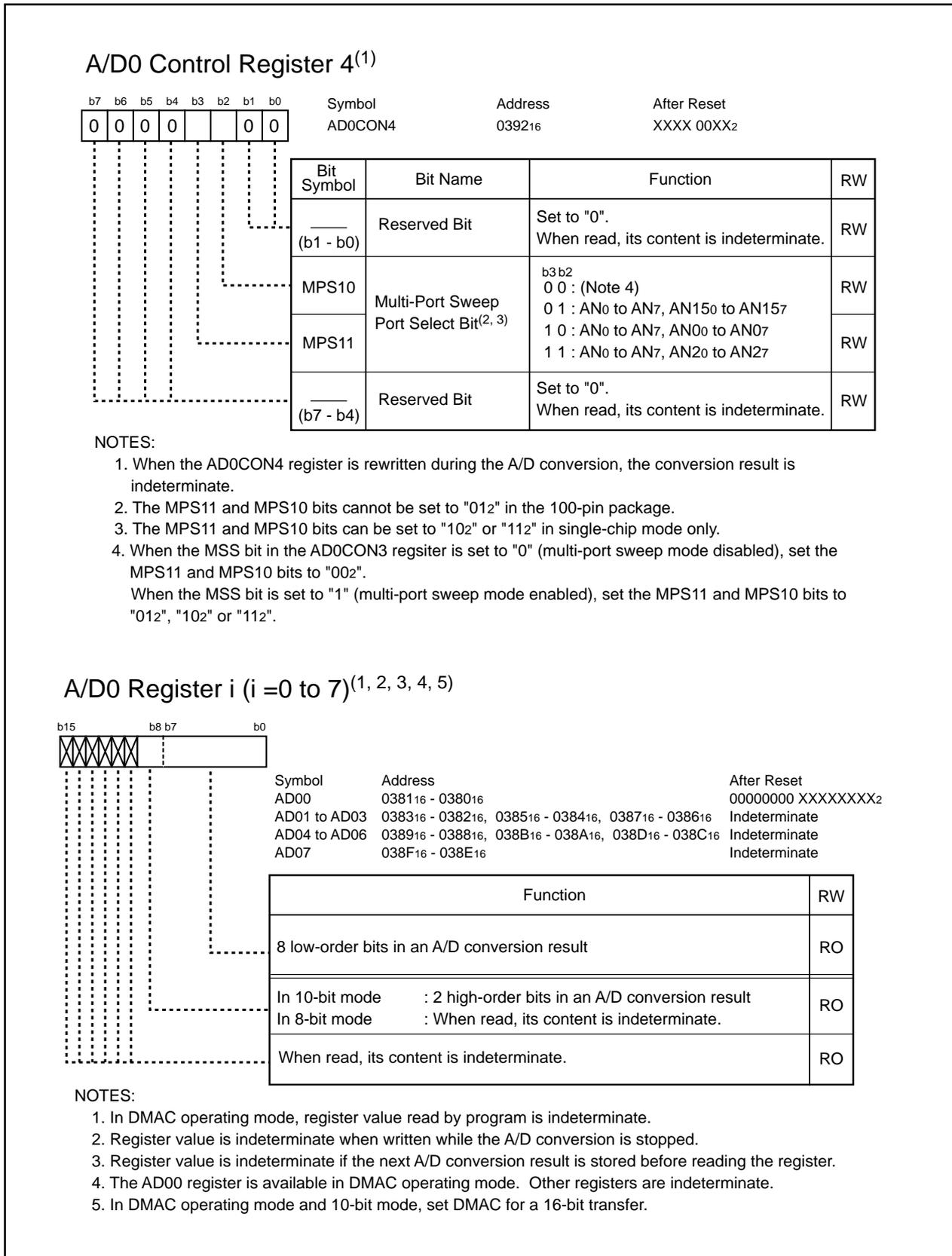


Figure 18.6 AD0CON4 Register and AD00 to AD07 Registers

18.1 Mode Description

18.1.1 One-shot Mode

In one-shot mode, analog voltage applied to a selected pin is converted to a digital code once. Table 18.2 lists specifications of one-shot mode.

Table 18.2 One-shot Mode Specifications

Item	Specification
Function	The CH2 to CH0 bits in the AD0CON0 register, the OPA1 and OPA0 bits in the AD0CON1 register and the APS1 and APS0 bits in the AD0CON2 register select a pin. Analog voltage applied to the pin is converted to a digital code once
Start Condition	<ul style="list-style-type: none"> • When the TRG bit in the AD0CON0 register is set to "0" (software trigger), the ADST bit in the AD0CON0 register is set to "1" (A/D conversion starts) by program • When the TRG bit is set to "1" (external trigger, hardware trigger): <ul style="list-style-type: none"> - a falling edge is applied to the \overline{ADTRG} pin after the ADST bit is set to "1" by program - The timer B2 interrupt request of three-phase motor control timer functions (after the ICTB2 register counter completes counting) is generated after the ADST bit is set to "1" by program
Stop Condition	<ul style="list-style-type: none"> • A/D conversion is completed (the ADST bit is set to "0" when the software trigger is selected) • The ADST bit is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	A/D conversion is completed
Analog Voltage Input Pins	Select one pin from ANi0 to ANi7 (i=none, 0, 2, 15), ANEX0 or ANEX1
Reading of A/D Conversion Result	<ul style="list-style-type: none"> • When the DUS bit in the AD0CON3 register is set to "0" (DMAC operating mode disabled), the microcomputer reads the AD0j register (j=0 to 7) corresponding to selected pin • When the DUS bit is set to "1" (DMAC operating mode enabled), do not read the AD00 register. A/D conversion result is stored in the AD00 register after the A/D conversion is completed. DMAC transfers the conversion result to any memory space. Refer to 13. DMAC for DMAC settings

18.1.2 Repeat Mode

In repeat mode, analog voltage applied to a selected pin is repeatedly converted to a digital code. Table 18.3 lists specifications of repeat mode.

Table 18.3 Repeat Mode Specifications

Item	Specification
Function	The CH2 to CH0 bits in the AD0CON0 register, the OPA1 and OPA0 bits in the AD0CON1 register and the APS1 and APS0 bits in the AD0CON2 register select a pin. Analog voltage applied to the pin is repeatedly converted to a digital code
Start Condition	Same as one-shot mode
Stop Condition	The ADST bit in the AD0CON0 register is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	<ul style="list-style-type: none"> • When the DUS bit in the AD0CON3 register is set to "0" (DMAC operating mode disabled), no interrupt request is generated. • When DUS bit is set to "1" (DMAC operating mode enabled), an interrupt request is generated every time an A/D conversion is completed.
Analog Voltage Input Pins	Select one pin from ANi0 to ANi7 (i=none, 0, 2, 15), ANEX0 or ANEX1
Reading of A/D Conversion Result	<ul style="list-style-type: none"> • When the DUS bit is set to "0", the microcomputer reads the AD0j register (j=0 to 7) corresponding to the selected pin. • When DUS bit is set to "1", do not read the AD00 register. A/D conversion result is stored in the AD00 register after the A/D conversion is completed. DMAC transfers the conversion result to any memory space. <p>Refer to 13. DMAC for DMAC settings</p>

18.1.3 Single Sweep Mode

In single sweep mode, analog voltage that is applied to selected pins is converted one-by-one to a digital code. Table 18.4 lists specifications of single sweep mode.

Table 18.4 Single Sweep Mode Specifications

Item	Specification
Function	The SCAN1 and SCAN0 bits in the AD0CON1 register and the APS1 and APS0 bits in the AD0CON2 register select pins. Analog voltage applied to the pin is converted one-by-one to a digital code
Start Condition	Same as one-shot mode
Stop Condition	Same as one-shot mode
Interrupt Request Generation Timing	<ul style="list-style-type: none"> • When the DUS bit in the AD0CON3 register is set to "0" (DMAC operating mode disabled), an interrupt request is generated after a sweep is completed. • When DUS bit is set to "1" (DMAC operating mode enabled), an interrupt request is generated every time an A/D conversion is completed
Analog Voltage Input Pins	Select from ANi0 and ANi1 (2 pins) (i=none, 0, 2, 15), ANi0 to ANi3 (4 pins), ANi0 to ANi5 (6 pins) or ANi0 to ANi7 (8 pins)
Reading of A/D Conversion Result	<ul style="list-style-type: none"> • When the DUS bit is set to "0", the microcomputer reads the AD0j register corresponding to selected pins • When DUS bit is set to "1", do not read the AD00 register. A/D conversion result is stored in the AD00 register after the A/D conversion is completed. DMAC transfers the conversion result to any memory space. Refer to 13. DMAC for DMAC settings

18.1.4 Repeat Sweep Mode 0

In repeat sweep mode 0, analog voltage applied to selected pins is repeatedly converted to a digital code. Table 18.5 lists specifications of repeat sweep mode 0.

Table 18.5 Repeat Sweep Mode 0 Specifications

Item	Specification
Function	The SCAN1 and SCAN0 bits in the AD0CON1 register and the APS1 and APS0 bits in the AD0CON2 register select pins. Analog voltage applied to the pins is repeatedly converted to a digital code
Start Condition	Same as one-shot mode
Stop Condition	The ADST bit in the AD0CON0 register is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	<ul style="list-style-type: none"> • When the DUS bit in the AD0CON3 register is set to "0" (DMAC operating mode disabled), no interrupt request is generated • When DUS bit is set to "1" (DMAC operating mode enabled), an interrupt request is generated every time an A/D conversion is completed
Analog Voltage Input Pins	Select from ANi0 and ANi1 (2 pins) (i=none, 0, 2, 15), ANi0 to ANi3 (4 pins), ANi0 to ANi5 (6 pins) or ANi0 to ANi7 (8 pins)
Reading of A/D Conversion Result	<ul style="list-style-type: none"> • When the DUS bit is set to "0", the microcomputer reads the AD0j register (j=0 to 7) corresponding to selected pins • When the DUS bit is set to "1", do not read the AD00 register. A/D conversion result is stored in the AD00 register after the A/D conversion is completed. DMAC transfers the conversion result to any memory space. Refer to 13. DMAC for DMAC settings

18.1.5 Repeat Sweep Mode 1

In repeat sweep mode 1, analog voltage selectively applied to eight pins is repeatedly converted to a digital code. Table 18.6 lists specifications of repeat sweep mode 1.

Table 18.6 Repeat Sweep Mode 1 Specifications

Item	Specification
Function	The SCAN1 and SCAN0 bits in the AD0CON1 register and the APS1 and APS0 bits in the AD0CON2 register select 8 pins. Analog voltage selectively applied to 8 pins is repeatedly converted to a digital code e.g., When ANi0 is selected (i =none, 0, 2, 15), analog voltage is converted to a digital code in the following order: ANi0 → ANi1 → ANi0 → ANi2 → ANi0 → ANi3 etc.
Start Condition	Same as one-shot mode (Any trigger generated during an A/D conversion is invalid)
Stop Condition	The ADST bit is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	<ul style="list-style-type: none"> • When the DUS bit in the AD0CON3 register is set to "0" (DMAC operating mode disabled), no interrupt request is generated • When DUS bit is set to "1" (DMAC operating mode enabled), an interrupt request is generated every time an A/D conversion is completed
Analog Voltage Input Pins	ANi0 to ANi7 (8 pins)
Prioritized Pins	ANi0 (1 pin), ANi0 and ANi1 (2 pins), ANi0 to ANi2 (3 pins) or ANi0 to ANi3 (4 pins)
Reading of A/D Conversion Result	<ul style="list-style-type: none"> • When the DUS bit is set to "0", the microcomputer reads the AD0j register (j=0 to 7) corresponding to selected pins • When the DUS bit is set to "1", do not read the AD00 register. A/D conversion result is stored in the AD00 register after the A/D conversion is completed. DMAC transfers the conversion result to any memory space. Refer to 13. DMAC for DMAC settings

18.1.6 Multi-Port Single Sweep Mode

In multi-port single sweep mode, analog voltage applied to 16 selected pins is converted one-by-one to a digital code. Set the DUS bit in the AD0CON3 register to "1" (DMAC operating mode enabled). Table 18.7 lists specifications of multi-port single sweep mode.

Table 18.7 Multi-Port Single Sweep Mode Specifications

Item	Specification
Function	The MPS11 and MPS10 bits in the AD0CON4 register select 16 pins. Analog voltage applied to 16 pins is converted one-by-one to a digital code in the following order: AN ₀ to AN ₇ → AN _{i0} to AN _{i7} (i=0, 2, 15) e.g., When the MPS11 and MPS10 bits are set to "102" (AN ₀ to AN ₇ , AN ₀₀ to AN ₀₇), analog voltage is converted to a digital code in the following order: AN ₀ → AN ₁ → AN ₂ → AN ₃ → AN ₄ → AN ₅ → AN ₆ → AN ₇ → AN ₀₀ → AN ₀₁ → → AN ₀₆ → AN ₀₇
Start Condition	Same as one-shot mode
Stop Condition	The ADST bit in the AD0CON0 register is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	An interrupt request is generated every time A/D conversion is completed (Set the DUS bit to "1")
Analog Voltage Input Pins	Select from AN ₀ to AN ₇ → AN ₁₅₀ to AN ₁₅₇ , AN ₀ to AN ₇ → AN ₀₀ to AN ₀₇ or AN ₀ to AN ₇ → AN ₂₀ to AN ₂₇
Reading of A/D Conversion Result	Do not read the AD00 register. A/D conversion result is stored in the AD00 register after the A/D conversion is completed. DMAC transfers the conversion result to any memory space. Refer to 13. DMAC for DMAC settings (Set the DUS bit to "1")

18.1.7 Multi-Port Repeat Sweep Mode 0

In multi-port repeat sweep mode 0, analog voltage that is applied to 16 selected pins is repeatedly converted to a digital code. Set the DUS bit in the AD0CON3 register to "1" (DMAC operating mode enabled). Table 18.8 lists specifications of multi-port repeat sweep mode 0.

Table 18.8 Multi-Port Repeat Sweep Mode 0 Specifications

Item	Specification
Function	The MPS11 and MPS10 bits in the AD0CON4 register select 16 pins. Analog voltage applied to the 16 pins is repeatedly converted to a digital code in the following order: AN ₀ to AN ₇ → AN _{i0} to AN _{i7} (i=0, 2, 15) e.g., When the MPS11 and MPS10 bits are set to "102" (AN ₀ to AN ₇ , AN ₀₀ to AN ₀₇), analog voltage is repeatedly converted to a digital code in the following order: AN ₀ → AN ₁ → AN ₂ → AN ₃ → AN ₄ → AN ₅ → AN ₆ → AN ₇ → AN ₀₀ → AN ₀₁ → → AN ₀₆ → AN ₀₇
Start Condition	Same as one-shot mode
Stop Condition	The ADST bit is set to "0" (A/D conversion stopped) by program
Interrupt Request Generation Timing	An interrupt request is generated after each A/D conversion is completed (Set the DUS bit to "1")
Analog Voltage Input Pins	Selectable from AN ₀ to AN ₇ → AN ₁₅₀ to AN ₁₅₇ , AN ₀ to AN ₇ → AN ₀₀ to AN ₀₇ or AN ₀ to AN ₇ → AN ₂₀ to AN ₂₇
Reading of A/D Conversion Result	Do not read the AD00 register. A/D conversion result is stored in the AD00 register after the A/D conversion is completed. DMAC transfers the conversion result to any memory space. Refer to 13. DMAC for DMAC settings (Set the DUS bit to "1")

18.2 Functions

18.2.1 Resolution Select Function

The BITS bit in the AD0CON1 register determines the resolution. When the BITS bit is set to "1" (10-bit precision), the A/D conversion result is stored into bits 9 to 0 in the AD0j register (j = 0 to 7). When the BITS bit is set to "0" (8-bit precision), the A/D conversion result is stored into bits 7 to 0 in the AD0j register.

18.2.2 Sample and Hold Function

When the SMP bit in the AD0CON2 register is set to "1" (with the sample and hold function), A/D conversion rate per pin increases to $28 \varnothing_{AD}$ cycles for 8-bit resolution and $33 \varnothing_{AD}$ cycles for 10-bit resolution. The sample and hold function is available in all operating modes. Start the A/D conversion after selecting whether the sample and hold function is to be used or not.

18.2.3 Trigger Select Function

The TRG bit in the AD0CON0 register and the TRG0 bit in the AD0CON2 register select the trigger to start the A/D conversion. Table 18.9 lists settings of the trigger select function.

Table 18.9 Trigger Select Function Settings

Bit and Setting		Trigger
AD0CON0 Register	AD0CON2 Register	
TRG = 0	-	Software trigger The A/D0 starts the A/D conversion when the ADST bit in the AD0CON0 register is set to "1"
TRG = 1 ⁽¹⁾	TRG0 = 0	External trigger ⁽²⁾ Falling edge of a signal applied to \overline{ADTRG}
	TRG0 = 1	Hardware trigger ⁽²⁾ The timer B2 interrupt request of three-phase motor control timer functions (after the ICTB2 counter completes counting)

NOTES:

1. A/D0 starts the A/D conversion when the ADST bit is set to "1" (A/D conversion started) and a trigger is generated.
2. The A/D conversion is restarted if an external trigger or a hardware trigger is inserted during the A/D conversion. (The A/D conversion in process is aborted.)

18.2.4 DMAC Operating Mode

DMAC operating mode is available with all operating modes. When the A/D converter is in multi-port single sweep mode or multi-port repeat sweep mode 0, the DMAC operating mode must be used. When the DUS bit in the AD0CON3 register is set to "1" (DMAC operating mode enabled), all A/D conversion results are stored into the AD00 register. DMAC transfers data from the AD00 register to any memory space every time an A/D conversion is completed in each pin. 8-bit DMA transfer must be selected for 8-bit resolution and 16-bit DMA transfer for 10-bit resolution. Refer to **13. DMAC** for instructions.

18.2.5 Extended Analog Input Pins

In one-shot mode and repeat mode, the ANEX0 and ANEX1 pins can be used as analog input pins. The OPA1 and OPA0 bits in the AD0CON1 register select which pins to use as analog input pins. An A/D conversion result for the ANEX0 pin is stored into the AD00 register. The result for the ANEX1 pin is stored into the AD01 register, but is stored into the AD00 register when the DUS bit in the AD0CON3 register is set to "1" (DMAC operating mode enabled).

Set the APS1 and APS0 bits in the AD0CON2 register to "002" (AN₀ to AN₇, ANEX0, ANEX1) and the MSS bit in the AD0CON3 register to "0" (multi-port sweep mode disabled).

18.2.6 External Operating Amplifier (Op-Amp) Connection Mode

In external op-amp connection mode, multiple analog voltage can be amplified by one external op-amp using extended analog input pins ANEX0 and ANEX1.

When the OPA1 and OPA0 bits in the AD0CON1 register are set to "112" (external op-amp connection), voltage applied to the AN₀ to AN₇ pins are output from ANEX0. Amplify this output signal by an external op-amp and apply it to ANEX1.

Analog voltage applied to ANEX1 is converted to a digital code and the A/D conversion result is stored into the corresponding AD0j register (j=0 to 7). A/D conversion rate varies depending on the response of the external op-amp. The ANEX0 pin cannot be connected to the ANEX1 pin directly.

Set the APS1 and APS0 bits in the AD0CON2 register to "002" (AN₀ to AN₇, ANEX0, ANEX1).

Figure 18.7 shows an example of an external op-amp connection.

Table 18.10 Extended Analog Input Pin Settings

AD0CON1 Register		ANEX0 Function	ANEX1 Function
OPA1 Bit	OPA0 Bit		
0	0	Not used	Not used
0	1	P95 as an analog input	Not used
1	0	Not used	P96 as an analog input
1	1	Output to an external op-amp	Input from an external op-amp

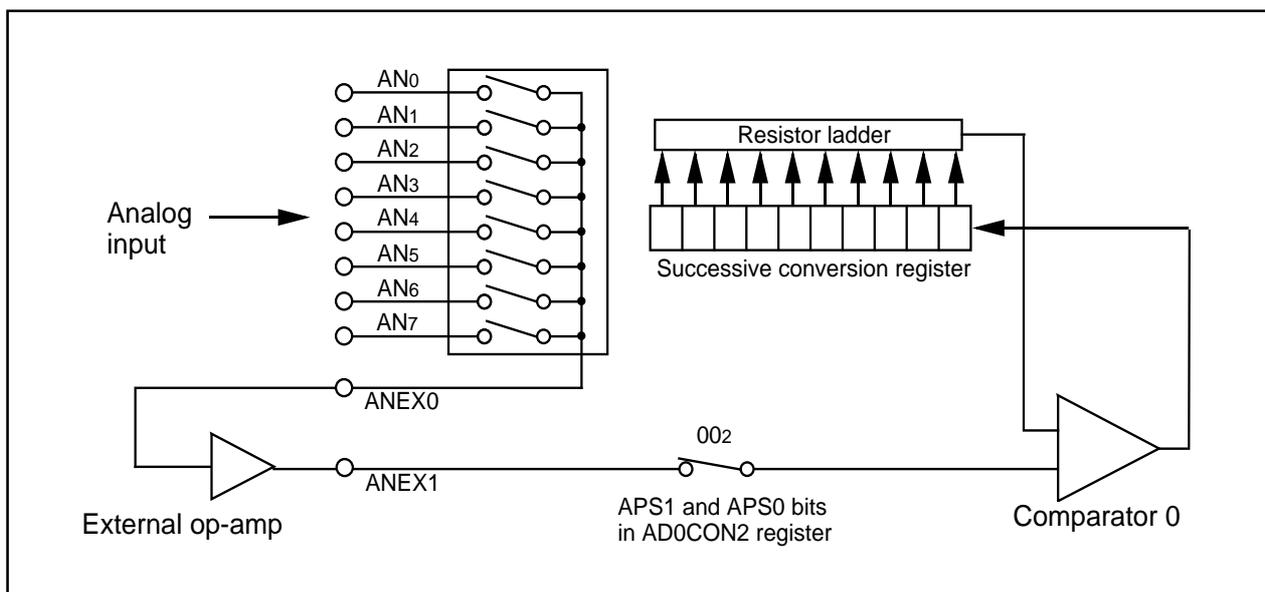


Figure 18.7 External Op-Amp Connection

18.2.7 Power Consumption Reducing Function

When the A/D converter is not used, the VCUT bit in the AD0CON1 register isolates the resistor ladder of the A/D converter from the reference voltage input pin (VREF). Power consumption is reduced by shutting off any current flow into the resistor ladder from the VREF pin.

When using the A/D converter, set the VCUT bit to "1" (VREF connection) before setting the ADST bit in the AD0CON0 register to "1" (A/D conversion started). Do not set the ADST bit and VCUT bit to "1" simultaneously, nor set the VCUT bit to "0" (no VREF connection) during the A/D conversion. The VCUT bit does not affect the VREF performance of the D/A converter.

18.2.8 Output Impedance of Sensor Equivalent Circuit under A/D Conversion

For perfect A/D converter performance, complete internal capacitor (C) charging, shown in Figure 18.8, for the specified period (T) as sampling time. Output Impedance of the sensor equivalent circuit (R₀) is determined by the following equations:

$$V_C = V_{IN} \left\{ 1 - e^{-\frac{1}{C(R_0 + R)} t} \right\}$$

$$\text{When } t = T, \quad V_C = V_{IN} - \frac{X}{Y} V_{IN} = V_{IN} \left(1 - \frac{X}{Y} \right)$$

$$e^{-\frac{1}{C(R_0 + R)} T} = \frac{X}{Y}$$

$$-\frac{1}{C(R_0 + R)} T = \ln \frac{X}{Y}$$

$$R_0 = -\frac{T}{C \cdot \ln \frac{X}{Y}} - R$$

where:

V_C = Voltage between pins

R = Internal resistance of the microcomputer

X = Precision (error) of the A/D converter

Y = Resolution of the A/D converter (1024 in 10-bit mode, and 256 in 8-bit mode)

Figure 18.8 shows analog input pin and external sensor equivalent circuit. The impedance (R₀) can be obtained if the voltage between pins (V_C) changes from 0 to V_{IN} - (0.1/1024) V_{IN} in the time (T), when the difference between V_{IN} and V_C becomes 0.1LSB.

(0.1/1024) means that A/D precision drop, due to insufficient capacitor charge, is held to 0.1LSB at time of A/D conversion in the 10-bit mode. Actual error, however, is the value of absolute precision added to 0.1LSB. When ØAD = 10 MHz, T = 0.3 µs in the A/D conversion mode with the sample and hold function. Output impedance (R₀) for sufficiently charging capacitor (C) in the time (T) is determined by the following equation:

Using T = 0.3 µs, R = 7.8 kΩ, C = 1.5 pF, X = 0.1, Y = 1024,

$$R_0 = -\frac{0.3 \times 10^{-6}}{1.5 \times 10^{-12} \cdot \ln \frac{0.1}{1024}} - 7.8 \times 10^3 = 13.9 \times 10^3$$

Thus, the allowable output impedance of the sensor equivalent circuit, making the precision (error) 0.1LSB or less, is approximately 13.9 kΩ maximum.

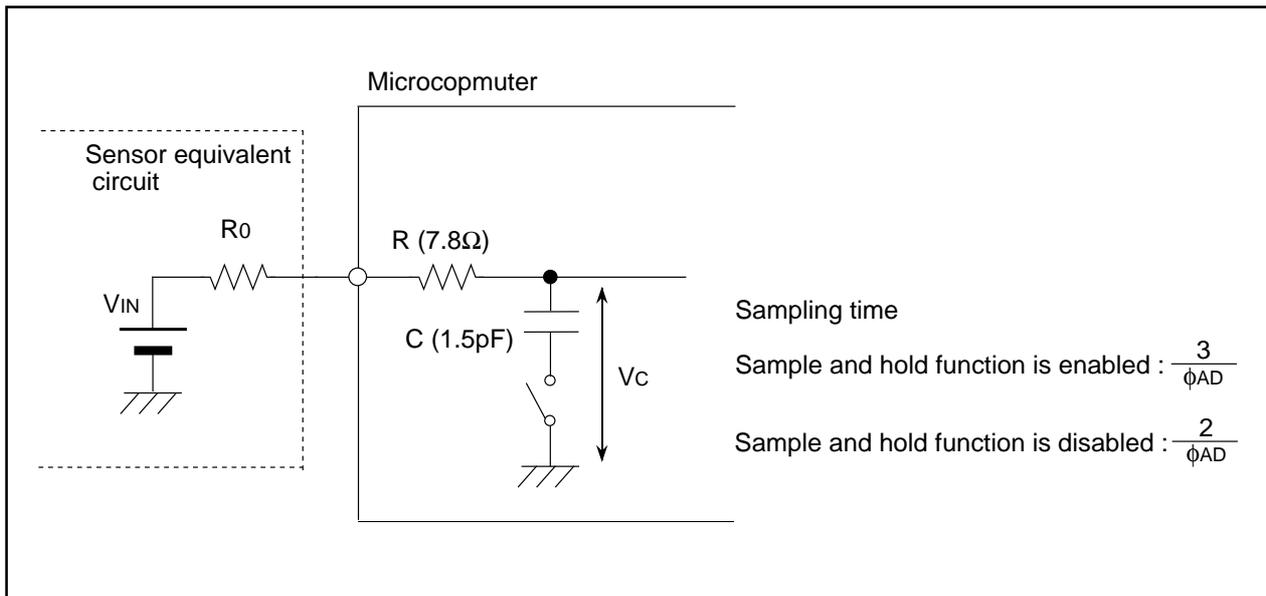


Figure 18.8 Analog Input Pin and External Sensor Equivalent Circuit

19. D/A Converter

The D/A converter consists of two separate 8-bit R-2R ladder D/A converters.

Digital code is converted to an analog voltage when a value is written to the corresponding DA_i registers (i=0,1). The DA_iE bit in the DACON register determines whether the D/A conversion result output is provided or not. Set the DA_iE bit to "1" (output enabled) to disable a pull-up of a corresponding port.

Output analog voltage (V) is calculated from value n (n =decimal) set in the DA_i register.

$$V = \frac{V_{REF} \times n}{256} \quad (n = 0 \text{ to } 255)$$

V_{REF} : reference voltage (not related to VCUT bit setting in the AD0CON1 register)

Table 19.1 lists specifications of the D/A converter. Table 19.2 lists pin setting of the DA0 and DA1 pins. Figure 19.1 shows a block diagram of the D/A converter. Figure 19.2 shows the D/A control register. Figure 19.3 shows a D/A converter equivalent circuit.

When the D/A converter is not used, set the DA_i register to "0016" and the DA_iE bit to "0" (output disabled).

Table 19.1 D/A Converter Specifications

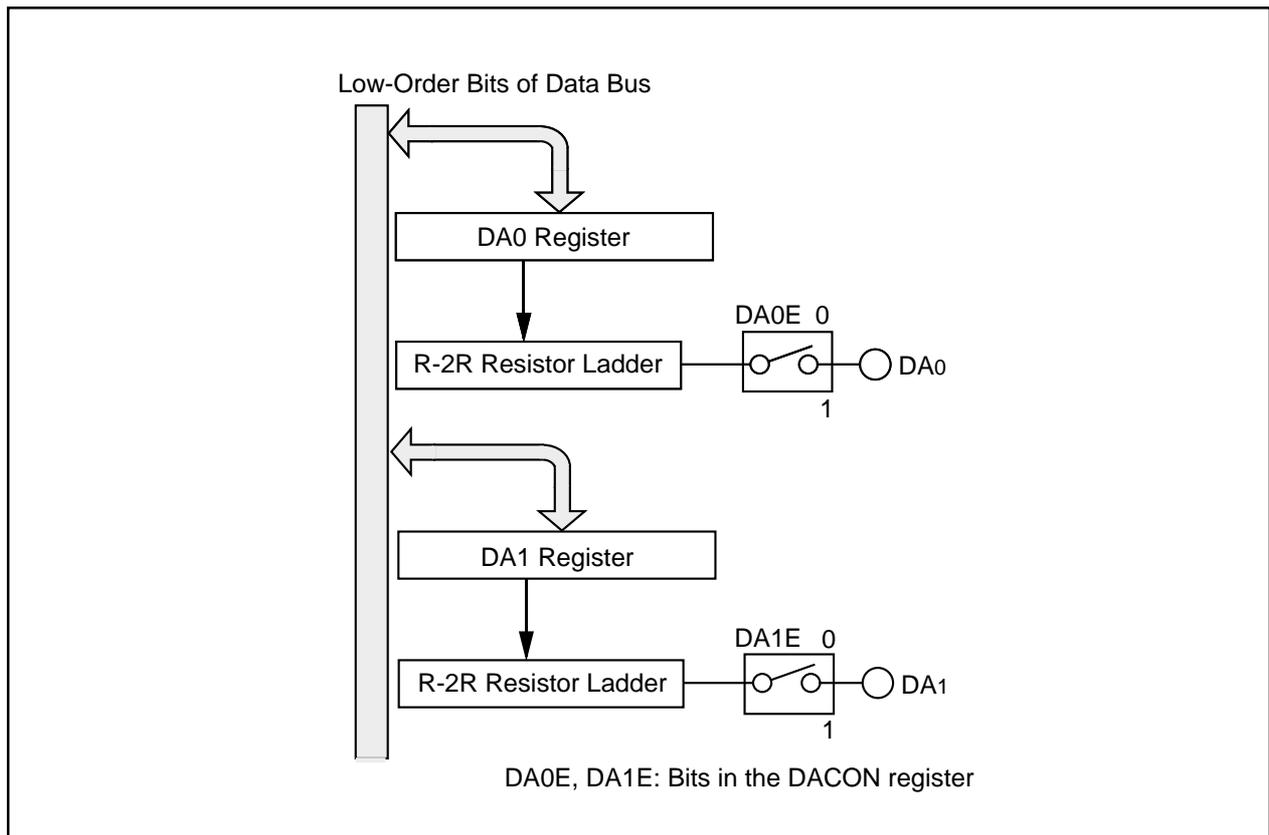
Item	Specification
D/A Conversion Method	R-2R
Resolution	8 bits
Analog Output Pin	2 channels

Table 19.2 Pin Settings

Port	Function	Bit and Setting		
		PD9 Register ⁽¹⁾	PS3 Register ⁽¹⁾	PSL3 Register
P93	DA0 output	PD9_3=0	PS3_3=0	PSL3_3=1
P94	DA1 output	PD9_4=0	PS3_4=0	PSL3_4=1

NOTES:

1. Set the PD9 and PS3 registers immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the instruction to set the PD9 and PS3 registers.

**Figure 19.1 D/A Converter**

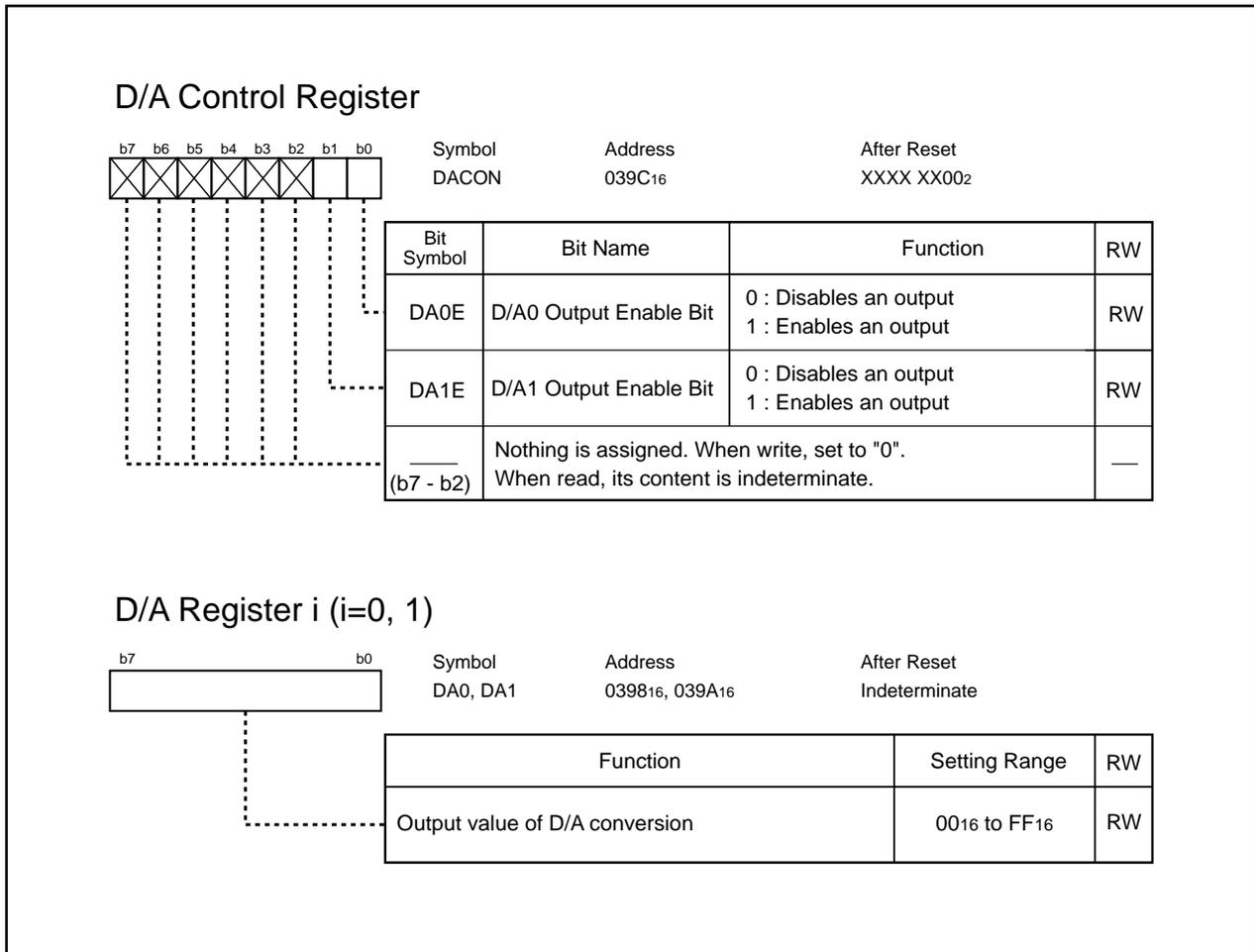


Figure 19.2 DACON Register, DA0 and DA1 Registers

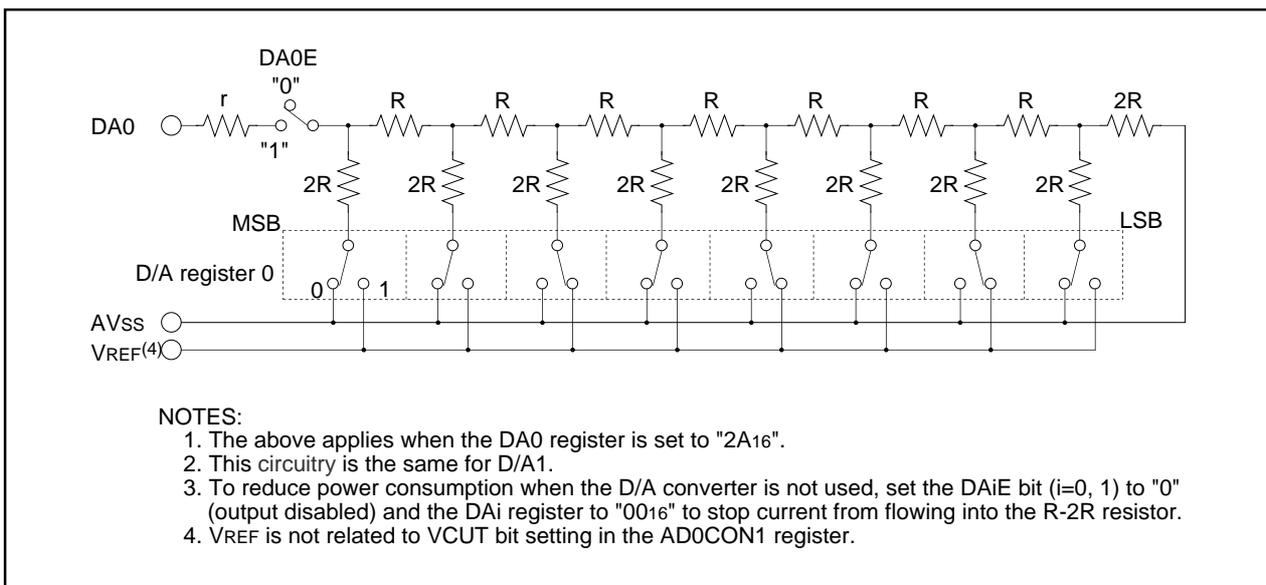


Figure 19.3 D/A Converter Equivalent Circuit

20. CRC Calculation

The CRC (Cyclic Redundancy Check) calculation detects an error in data blocks. A generator polynomial of CRC_CCITT ($X^{16} + X^{12} + X^5 + 1$) generates CRC code.

The CRC code is a 16-bit code generated for a block of data of desired length. This block of data is in 8-bit units. The CRC code is set in the CRCD register every time one-byte data is transferred to the CRCIN register after a default value is written to the CRCD register. CRC code generation for one-byte data is completed in two cycles.

Figure 20.1 shows a block diagram of a CRC circuit. Figure 20.2 shows associated registers. Figure 20.3 shows an example of the CRC calculation.

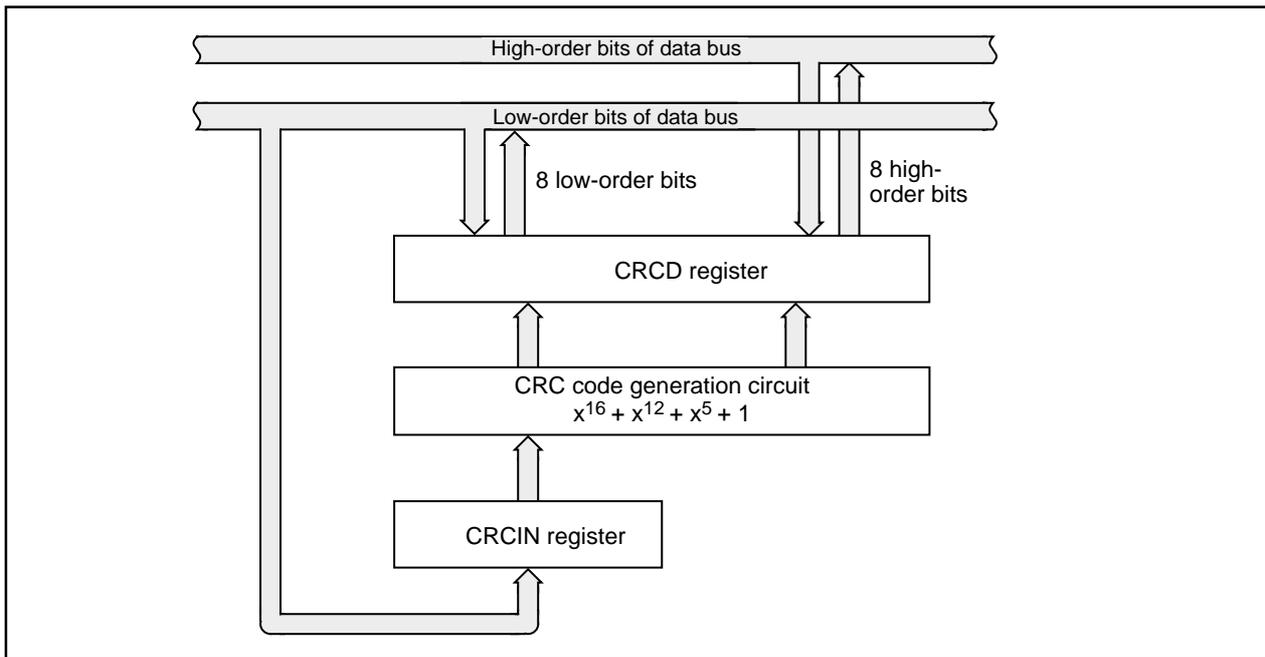


Figure 20.1 CRC Calculation Block Diagram

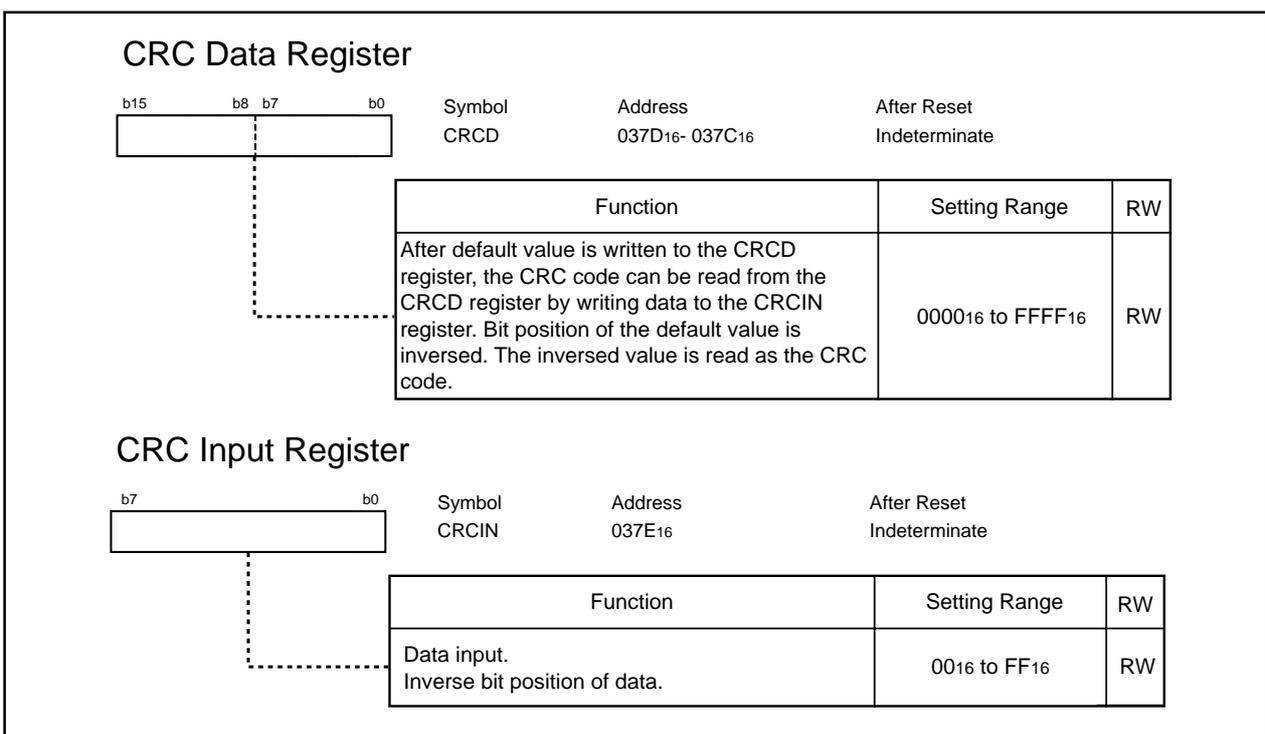


Figure 20.2 CRCD Register and CRCIN Register

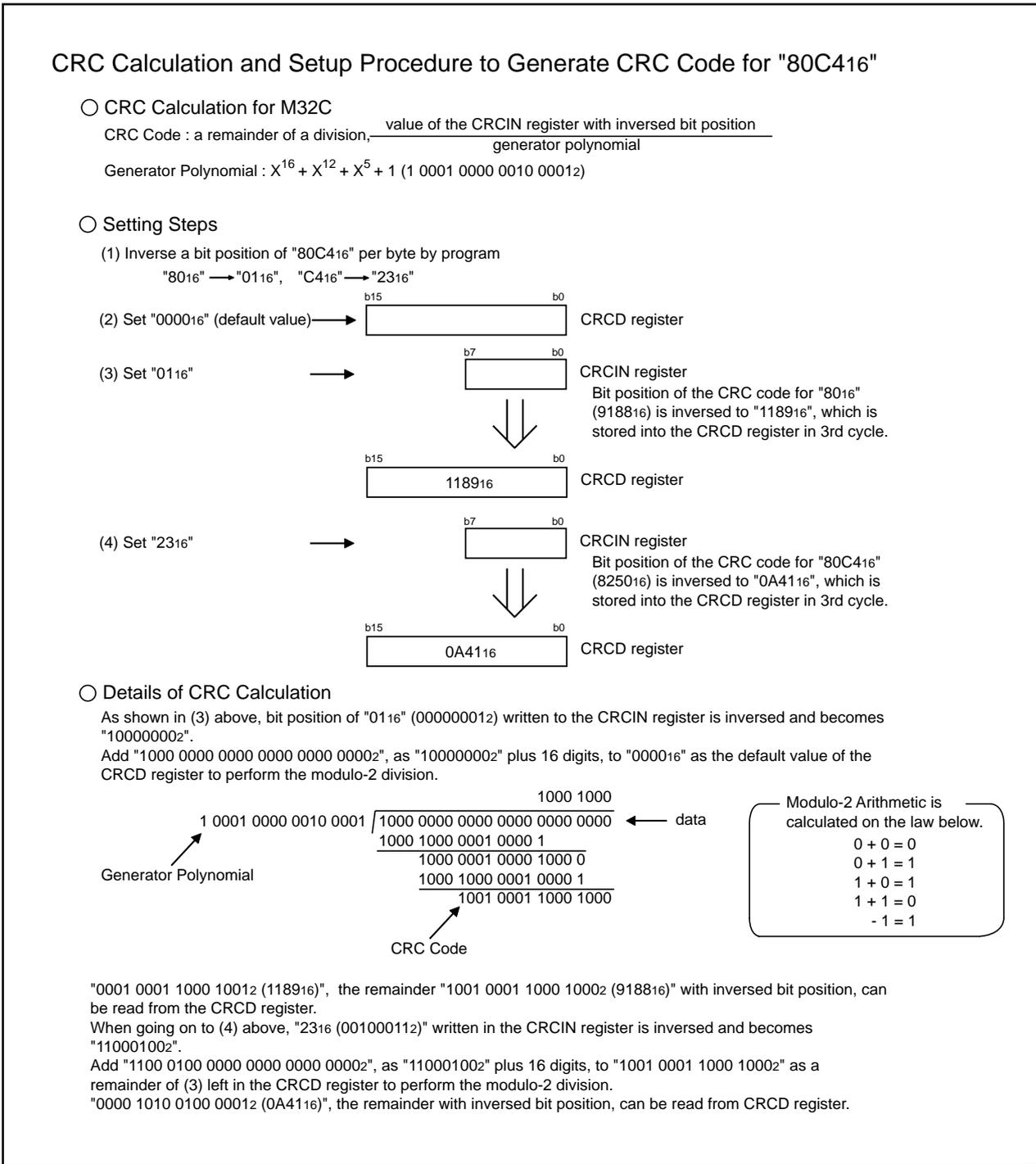


Figure 20.3 CRC Calculation

21. X/Y Conversion

The X/Y conversion rotates a 16 x 16 matrix data by 90 degrees and inverses high-order bits and low-order bits of a 16-bit data. Figure 21.1 shows the XYC register.

The 16-bit XiR register (i=0 to 15) and 16-bit YjR register (j=0 to 15) are allocated to the same address. The XiR register is a write-only register, while the YjR register is a read-only register. Access the XiR and YjR registers from an even address in 16-bit units. Performance cannot be guaranteed if the XiR and YiR registers are accessed in 8-bit units.

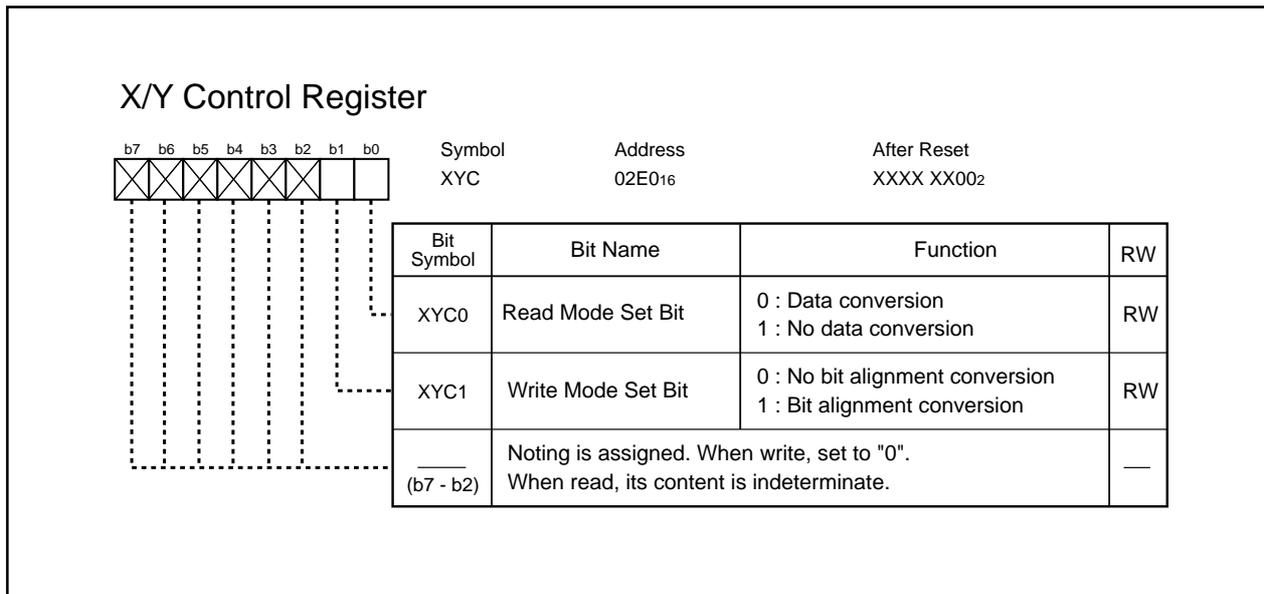


Figure 21.1 XYC Register

The XYC0 bit in the XYC register determines how to read the YjR register.

By reading the YjR register when the XYC0 bit is set to "0" (data conversion), bit j in the X0R to X15R registers can be read simultaneously.

For example, bit 0 in the X0R register can be read if reading bit 0 in the Y0R register, bit 0 in the X1R register if reading bit 1 in the Y0R register..., bit 0 in the X14R register if reading bit 14 in the Y0R register and bit 0 in the X15R register if reading bit 15 in the Y0R register.

Figure 21.2 shows the conversion table when the XYC0 bit is set to "0". Figure 21.3 shows an example of the X/Y conversion.

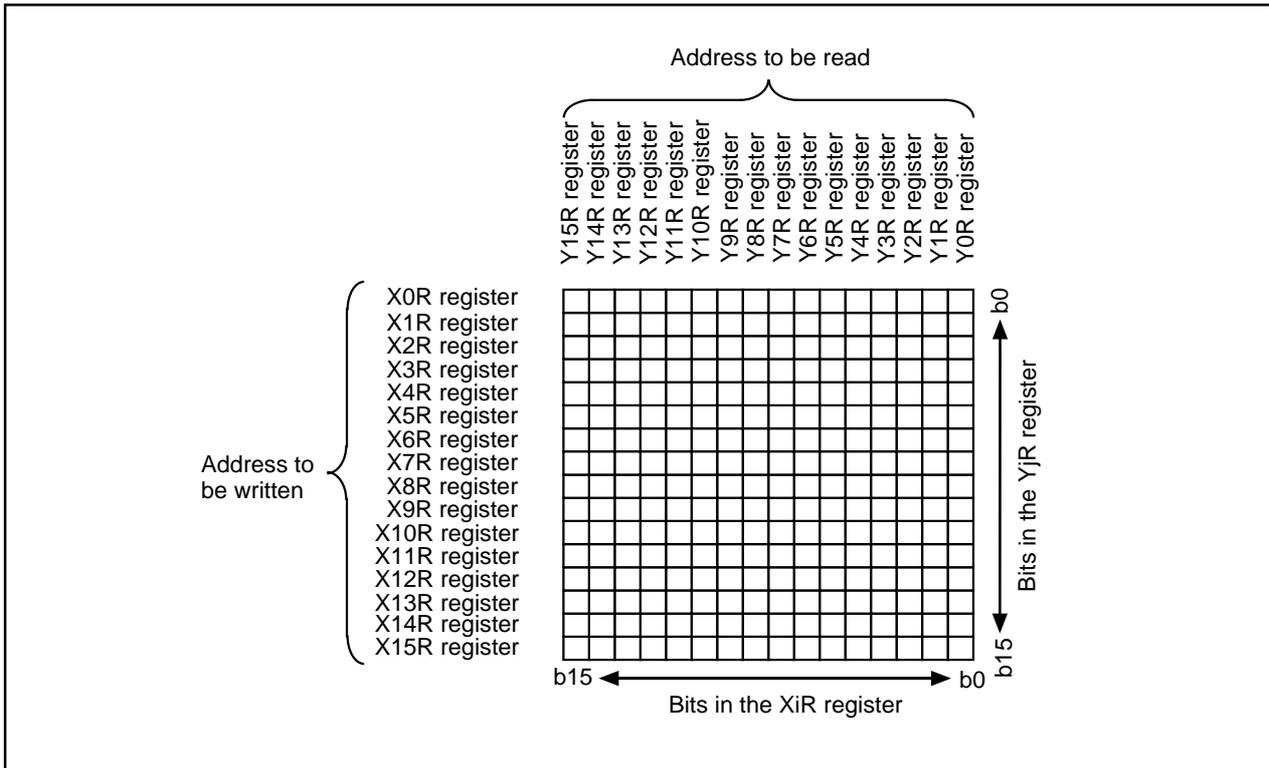


Figure 21.2 Conversion Table when Setting the XYC0 Bit to "0"

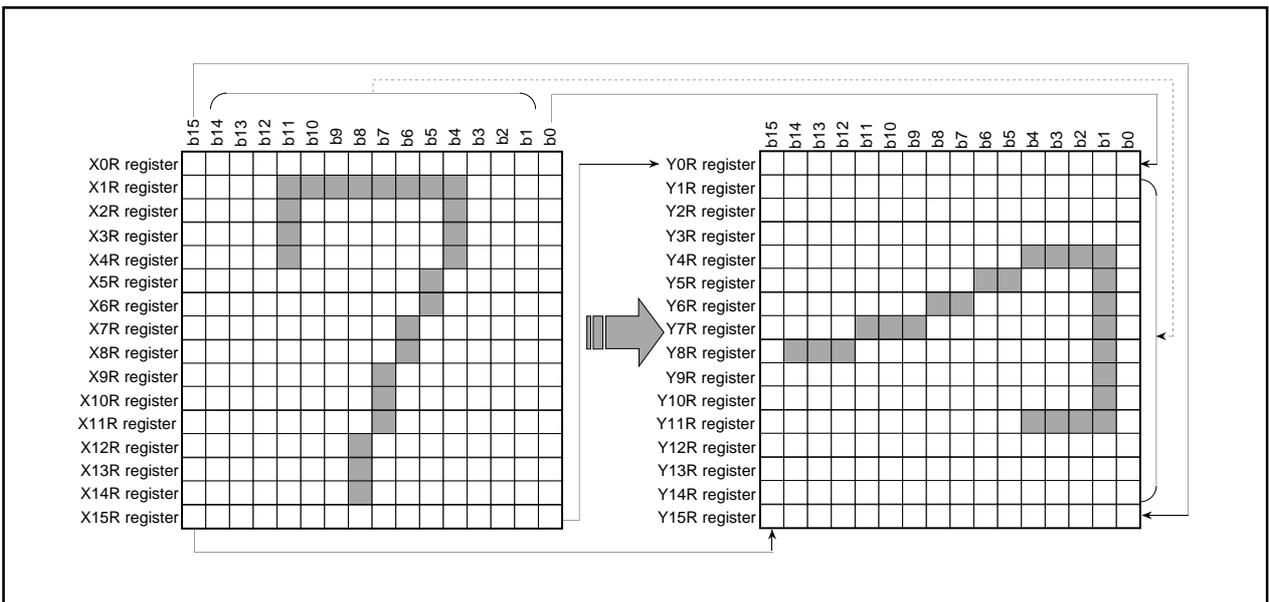


Figure 21.3 X/Y Conversion

By reading the YjR register when the XYC0 bit in the XYC register is set to "1" (no data conversion), the value written to the XiR register can be read directly. Figure 21.4 shows the conversion table when the XYC0 bit is set to "1."

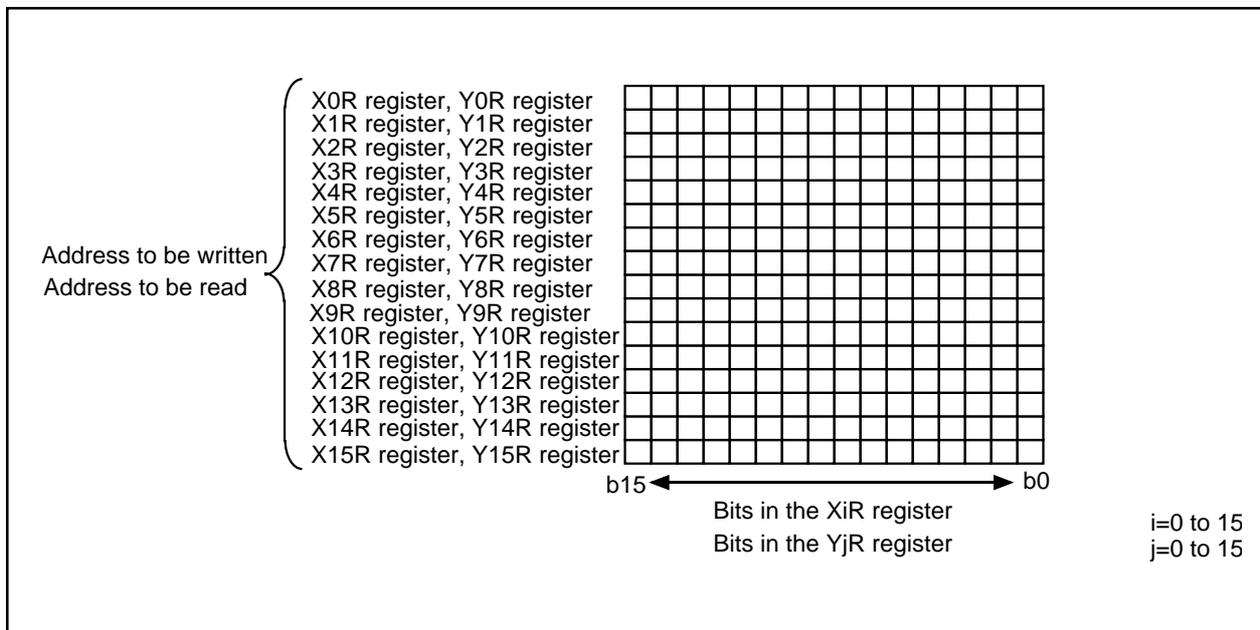


Figure 21.4 Conversion Table when Setting the XYC0 Bit to "1"

The XYC1 bit in the XYC register selects bit alignment of the value in the XiR register.

By writing to the XiR register while the XYC1 bit is set to "0" (no bit alignment conversion), bit alignment is written as is. By writing to the XiR register while the XYC1 bit is set to "1" (bit sequence replaced), bit alignment is written inversed.

Figure 21.5 shows the conversion table when the XYC1 bit is set to "1".

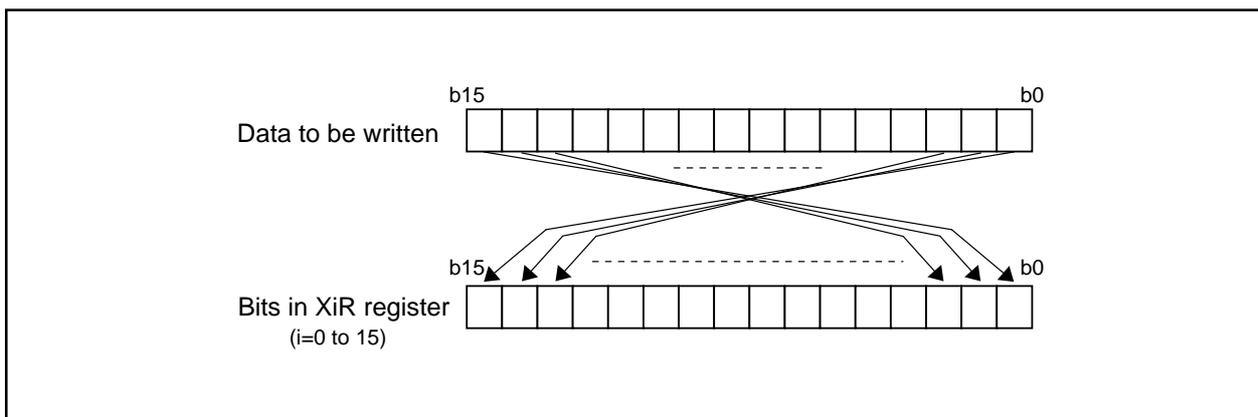


Figure 21.5 Conversion Table when Setting the XYC1 Bit to "1"

22. Intelligent I/O

The intelligent I/O is a multifunctional I/O port for time measurement, waveform generating, clock synchronous serial I/O, clock asynchronous serial I/O (UART), HDLC data processing and more.

The intelligent I/O has one 16-bit base timer for free-running operation, eight 16-bit registers for time measurement and waveform generating and two sets of two 8-bit shift registers for communications.

Table 22.1 lists functions and channels of the intelligent I/O.

Table 22.1 Intelligent I/O Functions and Channels

Function	Description	
Time Measurement ⁽¹⁾	8 channels	
Digital Filter	8 channels	
Trigger Input Prescaler	2 channels (channel 6 and channel 7)	
Trigger Input Gate	2 channels (channel 6 and channel 7)	
Waveform Generating ⁽¹⁾	8 channels	
Single-Phase Waveform Output Mode	8 channels	
Phase-Delayed Waveform Output Mode	8 channels	
SR Waveform Output Mode	8 channels	
Communication	Communication unit 0	Communication unit 1
Clock Synchronous Serial I/O Mode	Available	Available
UART Mode	Not Available	
HDLC Data Processing Mode	Available	

NOTES:

1. The time measurement function and the waveform generating function share a pin.

The time measurement function and waveform generating function can be selected for each channel.

The communication function is available by a combining multiple channels.

Figure 22.1 shows a block diagram of the intelligent I/O. Figure 22.2 shows a block diagram of the intelligent I/O communication.

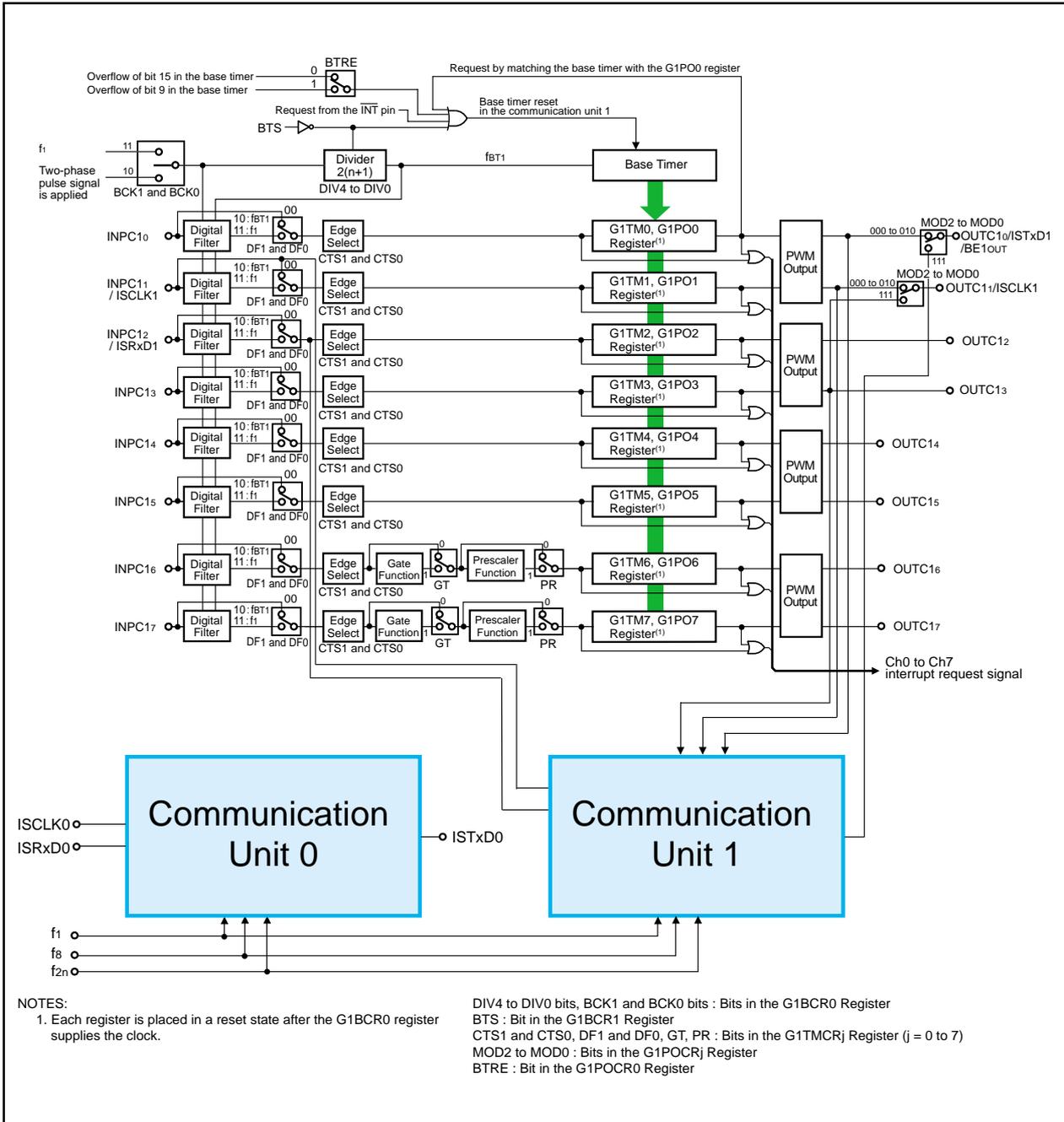


Figure 22.1 Intelligent I/O Block Diagram

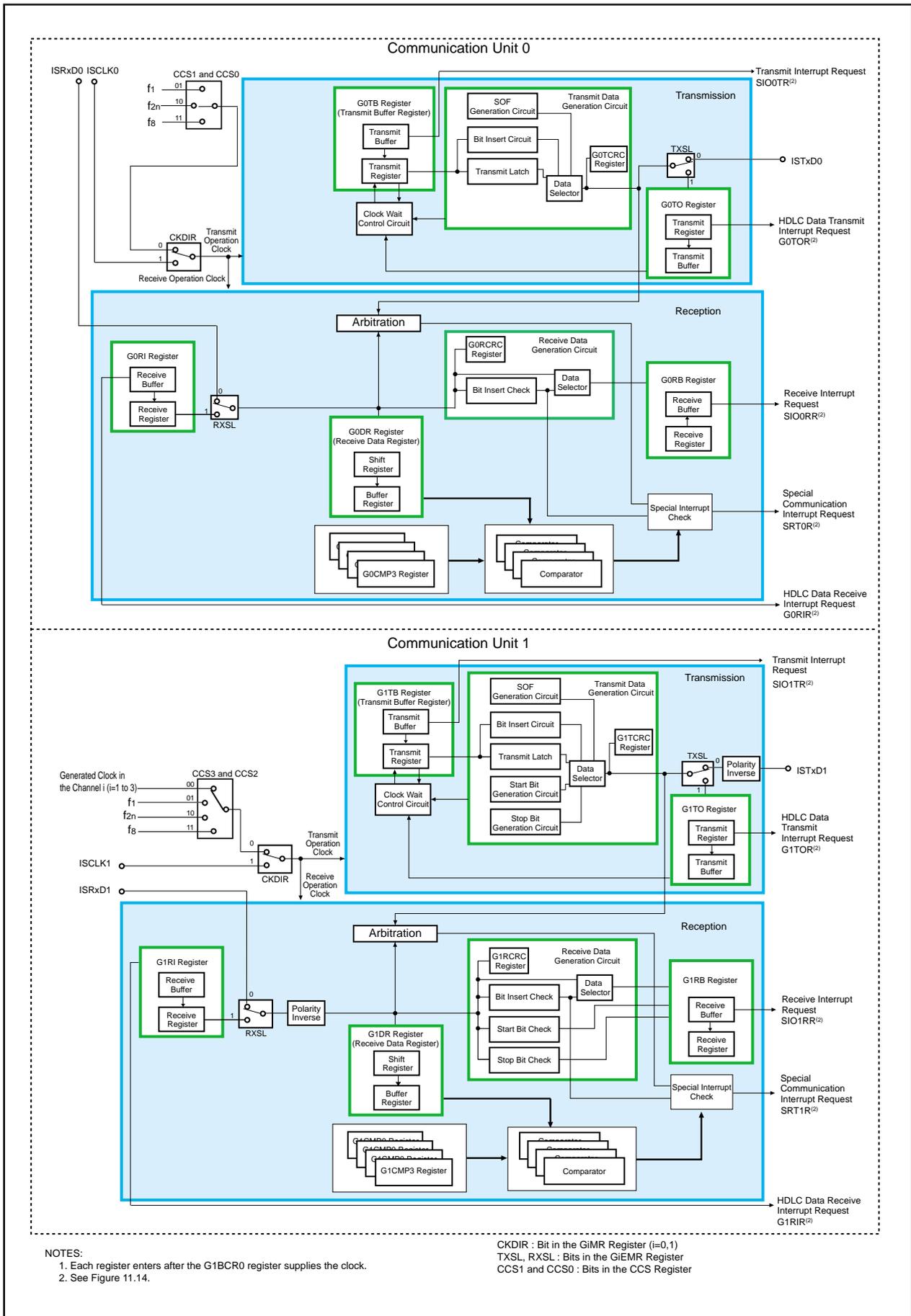


Figure 22.2 Intelligent I/O Communication Block Diagram

Figures 22.3 to 22.8 show registers associated with the intelligent I/O base timer, the time measurement function and waveform generating function. (For registers associated with the communication function, see Figures 22.19 to 22.28.)

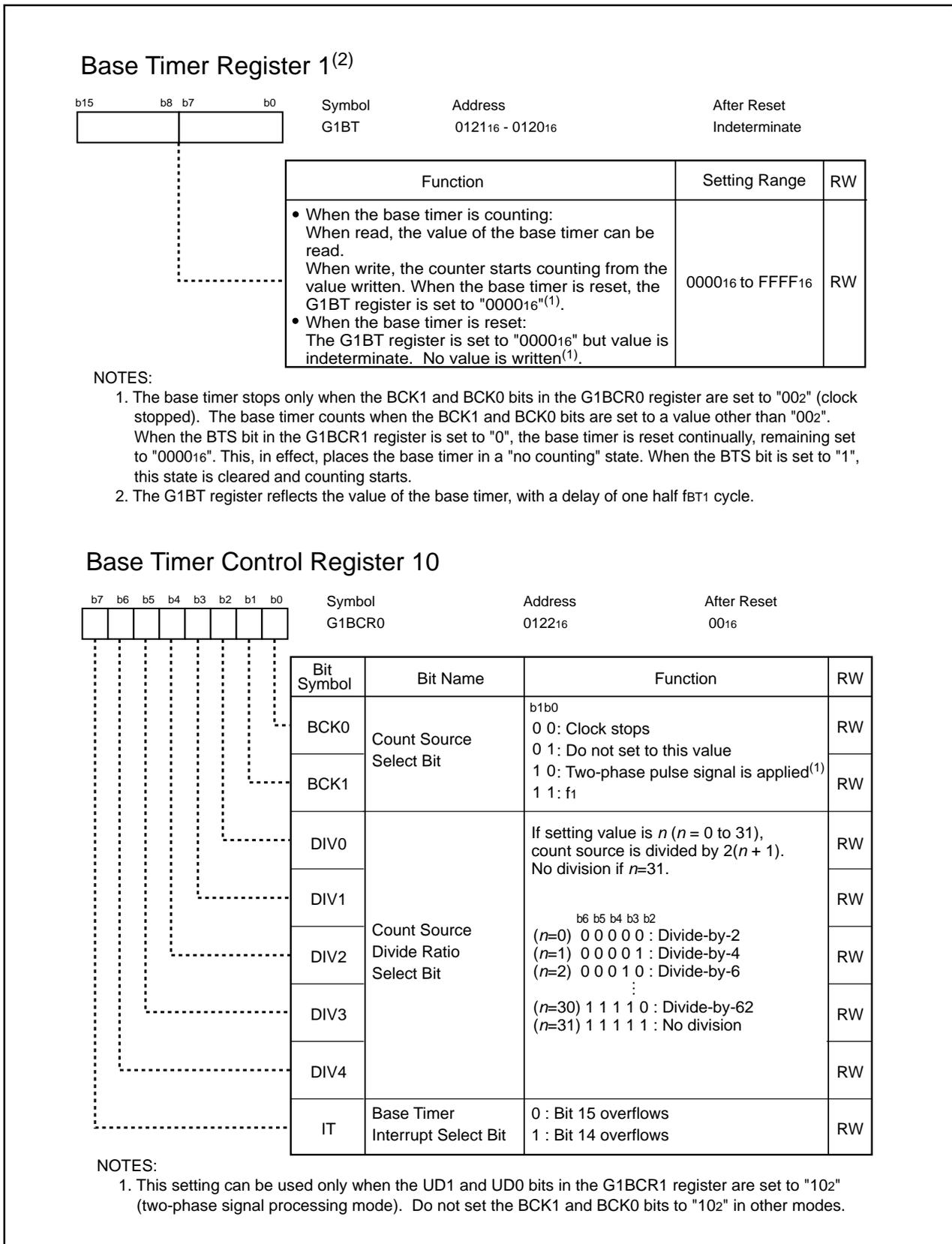


Figure 22.3 G1BT Register and G1BCR0 Register

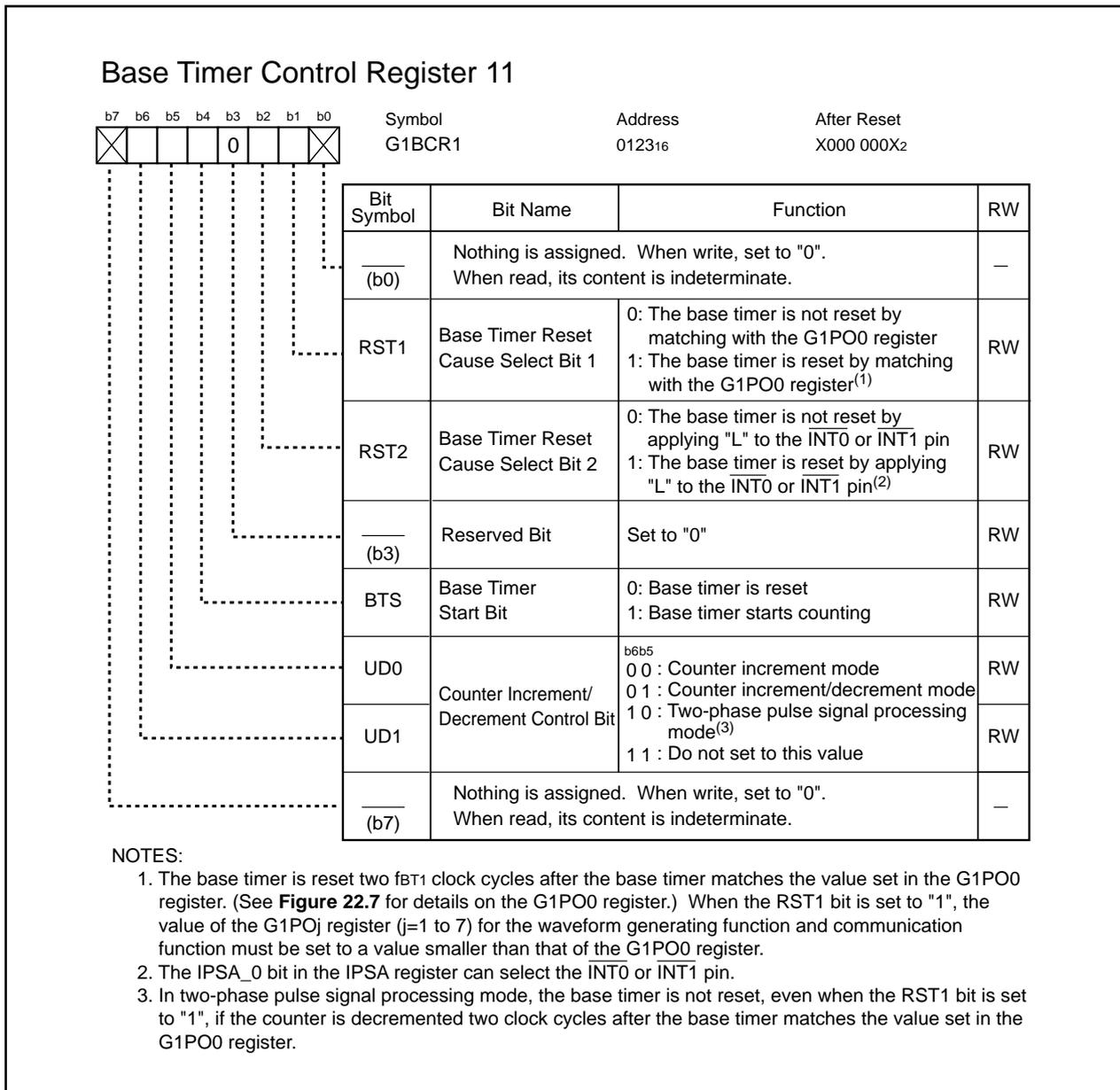


Figure 22.4 G1BCR1 Register

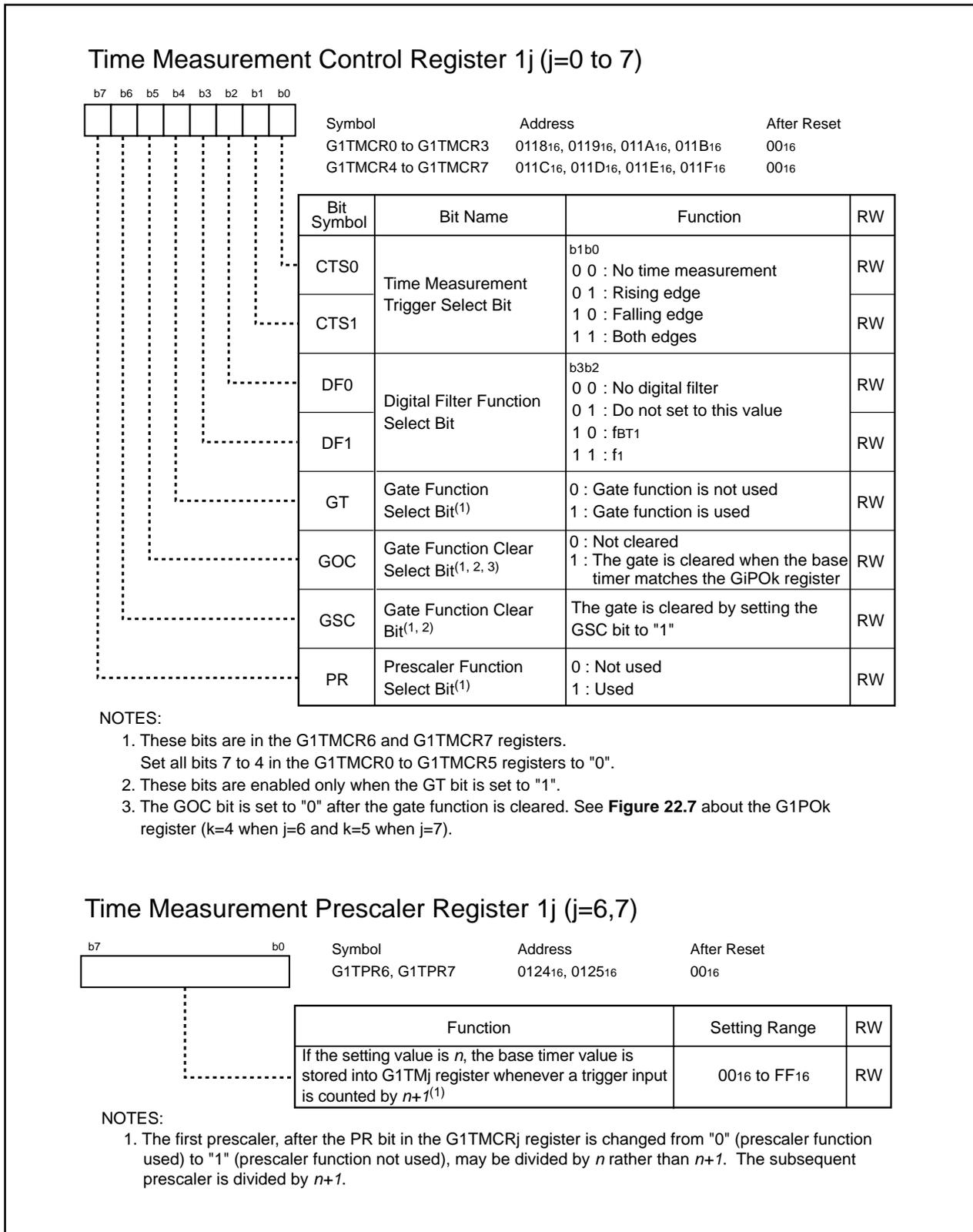


Figure 22.5 G1TMCR0 to G1TMCR7 Registers, G1TPR6 and G1TPR7 Registers

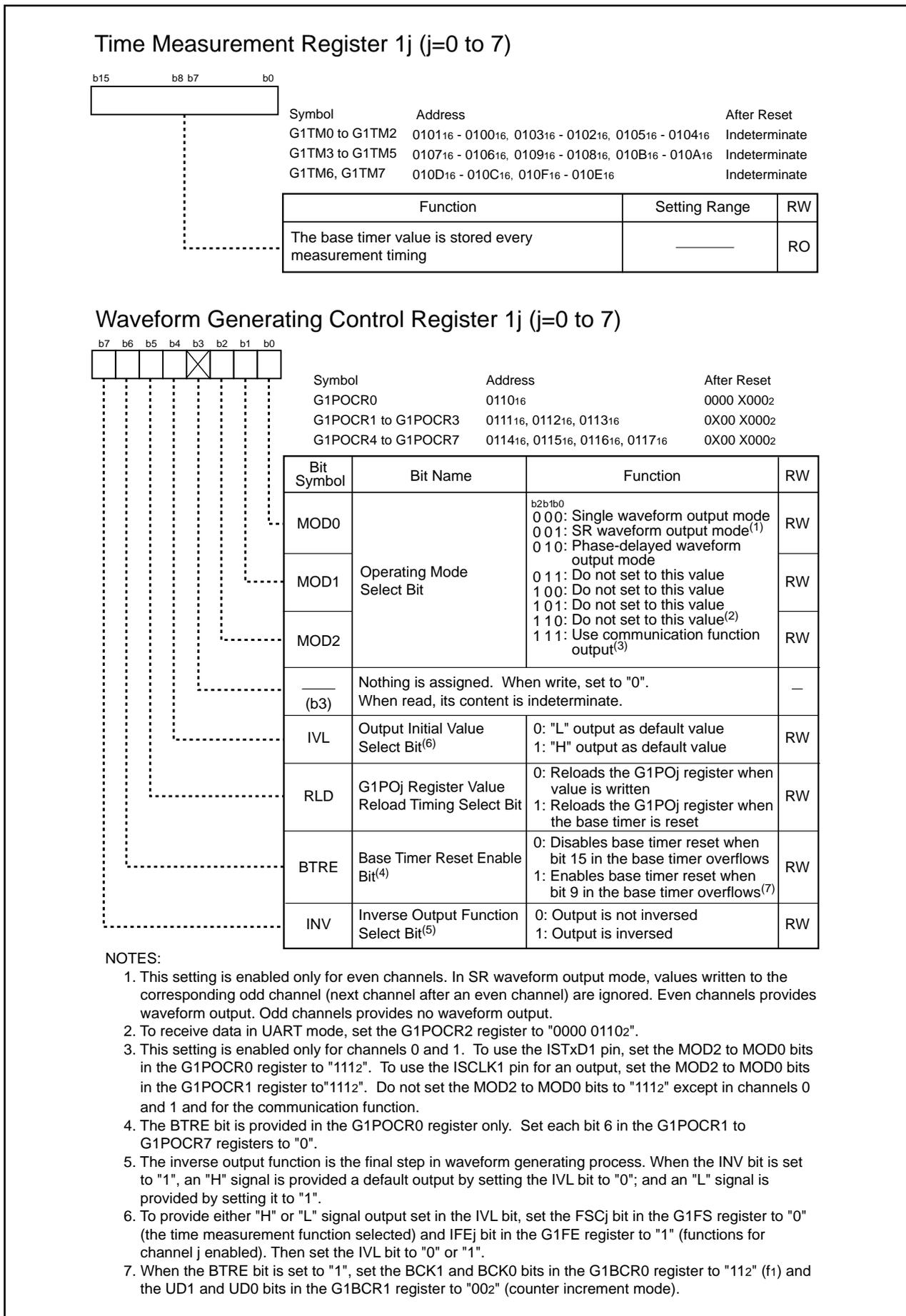


Figure 22.6 G1TM0 to G1TM7 Registers and G1POCR0 to G1POCR7 Registers

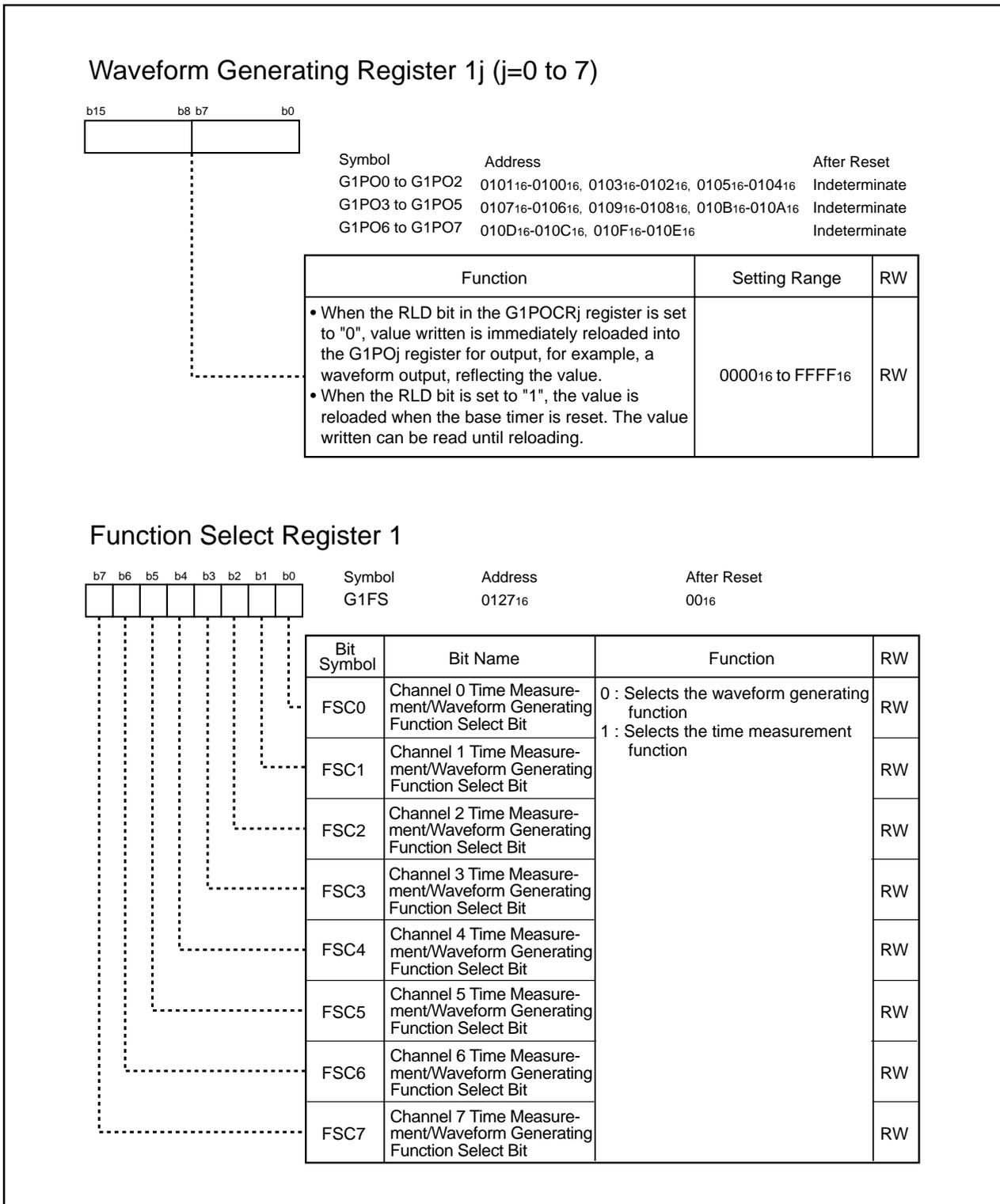


Figure 22.7 G1PO0 to G1PO7 Registers and G1FS Register

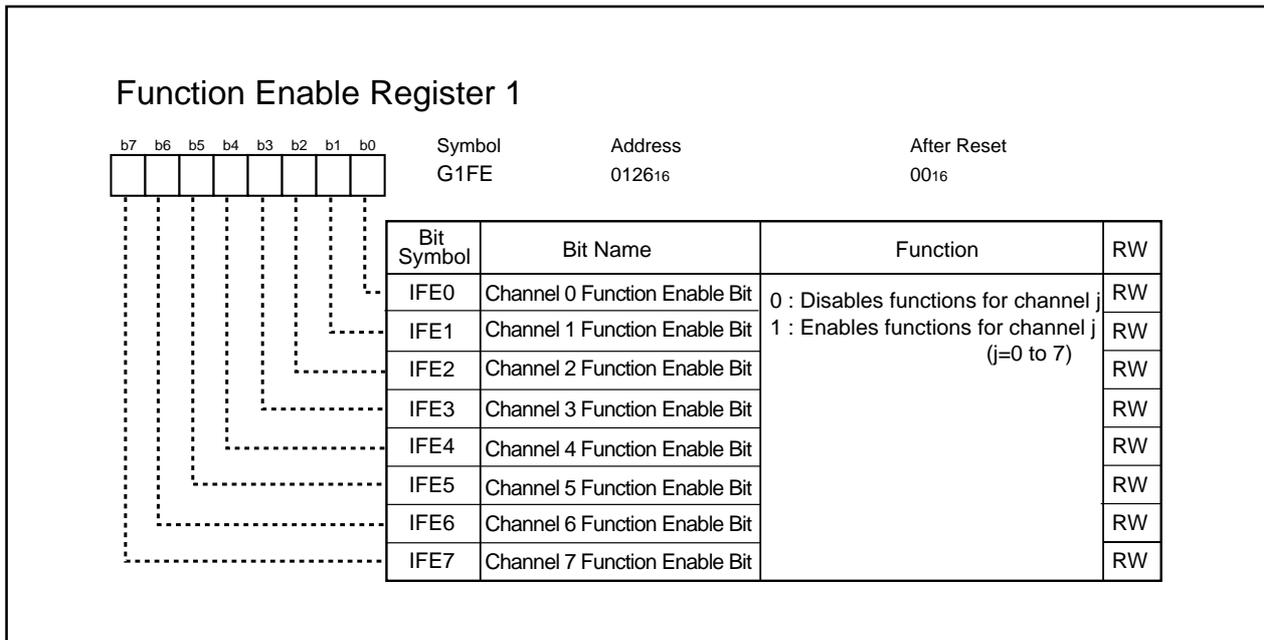


Figure 22.8 G1FE Register

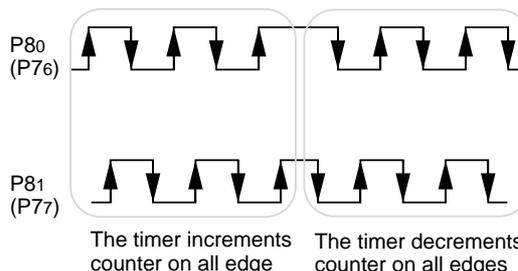
22.1 Base Timer

The base timer is a free-running counter that counts an internally generated count source.

Table 22.2 lists specifications of the base timer. Figures 22.3 and 22.4 show registers associated with the base timer. Figure 22.9 shows a block diagram of the base timer. Figure 22.10 shows an example of the base timer in counter increment mode. Figure 22.11 shows an example of the base timer in counter increment/decrement mode. Figure 22.12 shows an example of two-phase pulse signal processing mode.

Table 22.2 Base Timer Specifications

Item	Specification
Count Source (fBT1)	f1 divided by $2^{(n+1)}$, two-phase pulse input divided by $2^{(n+1)}$ n : determined by the DIV4 to DIV0 bits in the G1BCR0 register $n=0$ to 31; however no division when $n=31$
Counting Operation	The base timer increments the counter value The base timer increments and decrements the counter value Two-phase pulse signal processing
Counter Start Condition	The BTS bit in the G1BCR1 register is set to "1" (base timer starts counting)
Counter Stop Condition	The BTS bit in the G1BCR1 register is set to "0" (base timer reset)
Base Timer Reset Condition	<ul style="list-style-type: none"> The value of the base timer matches the value of the G1PO0 register An low-level ("L") signal is applied to the $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ pin Bit 15 or bit 9 in the base timer overflows
Value when the Base Timer is Reset	"0000 ₁₆ "
Interrupt Request	The BT1R bit in the IIO4IR register is set to "1" (interrupt requested) when bit 9, bit 14 or bit 15 in the base timer overflows (See Figure 11.14.)
Read from Base Timer	<ul style="list-style-type: none"> The G1BT register indicates the counter value while the base timer is running The G1BT register is indeterminate when the base timer is reset
Write to Base Timer	When a value is written while the base timer is running, the timer counter immediately starts counting from this value. No value can be written while the base timer is reset
Selectable Function	<ul style="list-style-type: none"> Counter increment/decrement mode The base timer starts counting when the BTS bit is set to "1". After incrementing to "FFFF₁₆", the timer counter is then decremented back to "0000₁₆". If the RST1 bit in the G1BCR1 register is set to "1" (the base timer is reset by matching with the G1PO0 register), the timer counter decrements two counts after the base timer matches the G1PO0 register. The base timer increments the counter value again when the timer counter reaches "0000₁₆." (See Figure 22.11.) Two-phase pulse processing mode Two-phase pulse signals from P76 and P77 pins or P80 and P81 pins are counted as well. (See Figure 22.12.) The IPSA_0 bit in the IPSA register controls input pin selection. (Refer to 24. Programmable I/O Ports)



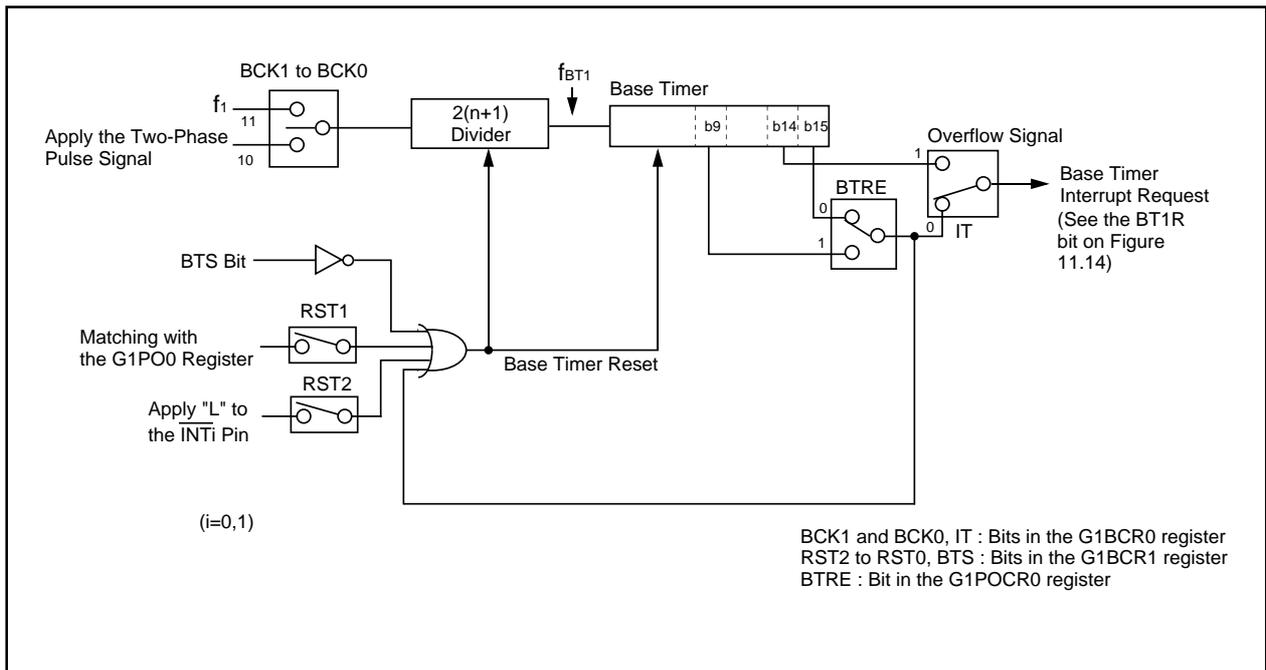


Figure 22.9 Base Timer Block Diagram

Table 22.3 Base Timer Associated Register Settings

(Also applies when using time measurement function, waveform generating function and communication function)

Register	Bit	Function
G1BCR0	BCK1, BCK0	Select count source
	DIV4 to DIV0	Select divide ratio of count source
	IT	Select the base timer interrupt
G1BCR1	RST2, RST1	Select source for a base timer reset
	BTS	Used to start the base timer independently
	UD1, UD0	Select how to count
G1POCR0	BTRE	Select source for a base timer reset
G1BT	-	Read or write base timer value

Set the following registers to set the RST1 bit to "1" (base timer reset by matching the base timer with the G1PO0 register).

G1POCR0	MOD2 to MOD0	Set to "0002" (single-phase waveform output mode)
G1PO0	-	Set reset cycle
G1FS	FSC0	Set to "0" (waveform generating function)
G1FE	IFE0	Set to "1" (channel operation start)

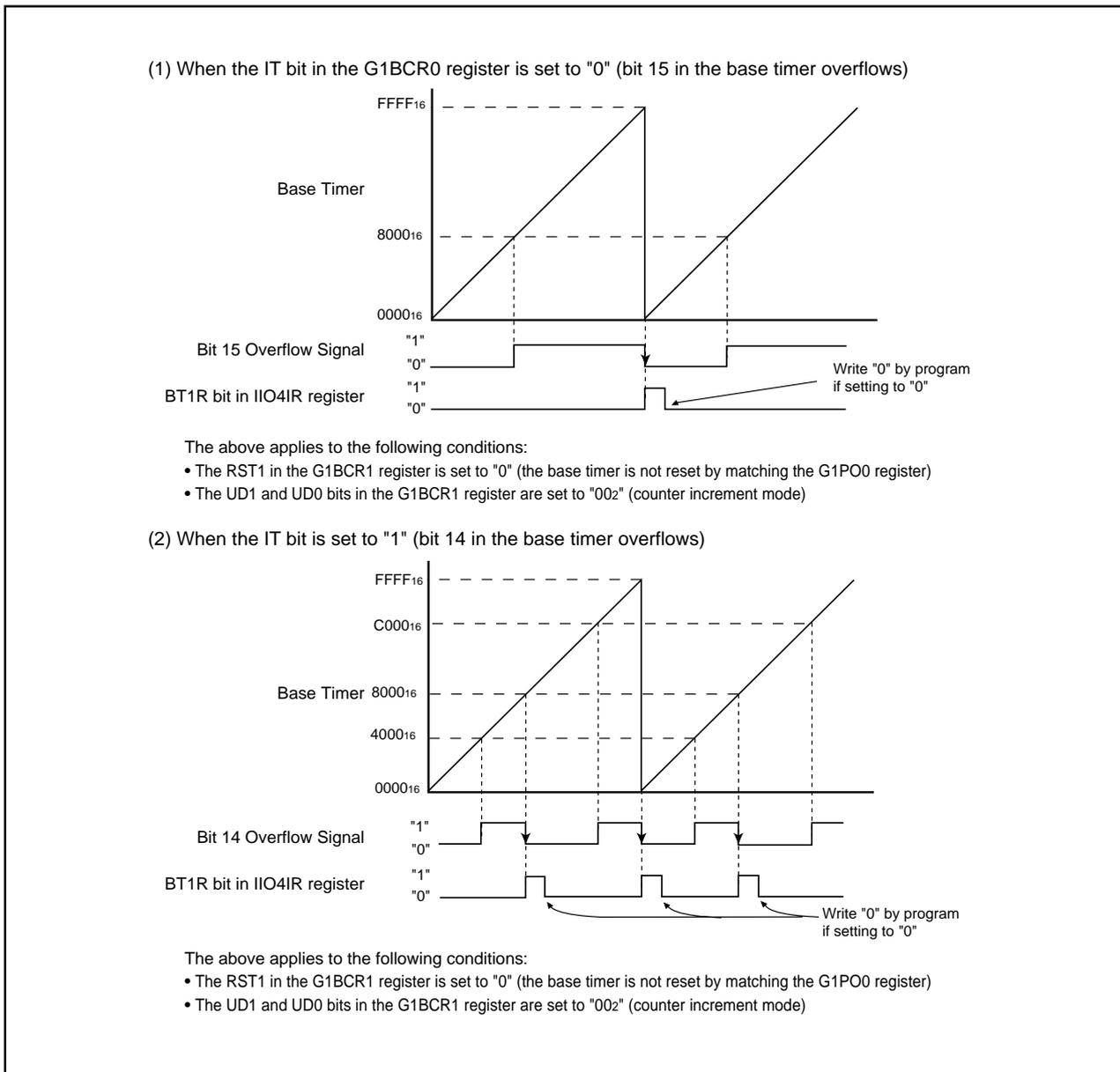


Figure 22.10 Counter Increment Mode

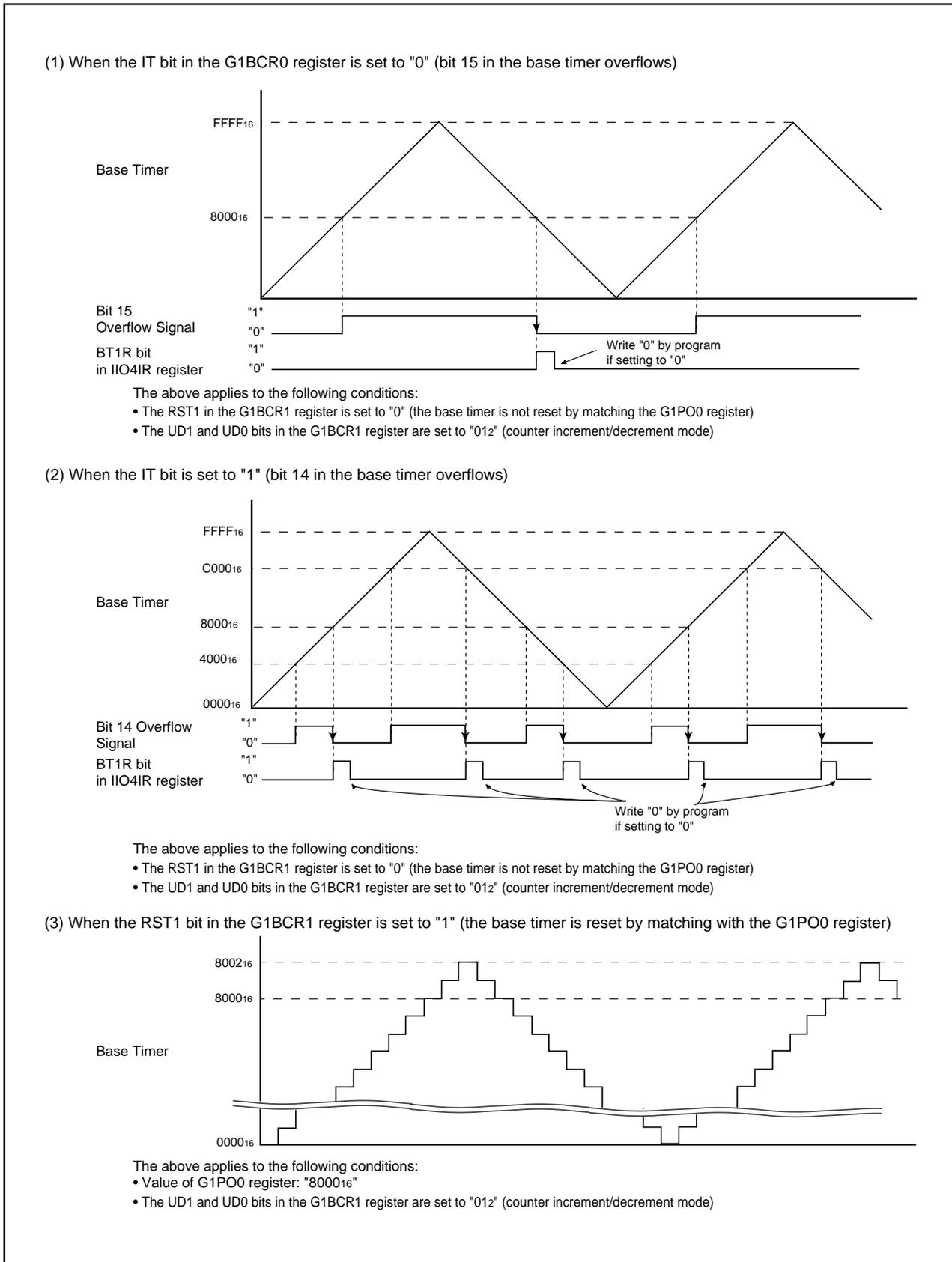


Figure 22.11 Counter Increment/Decrement Mode

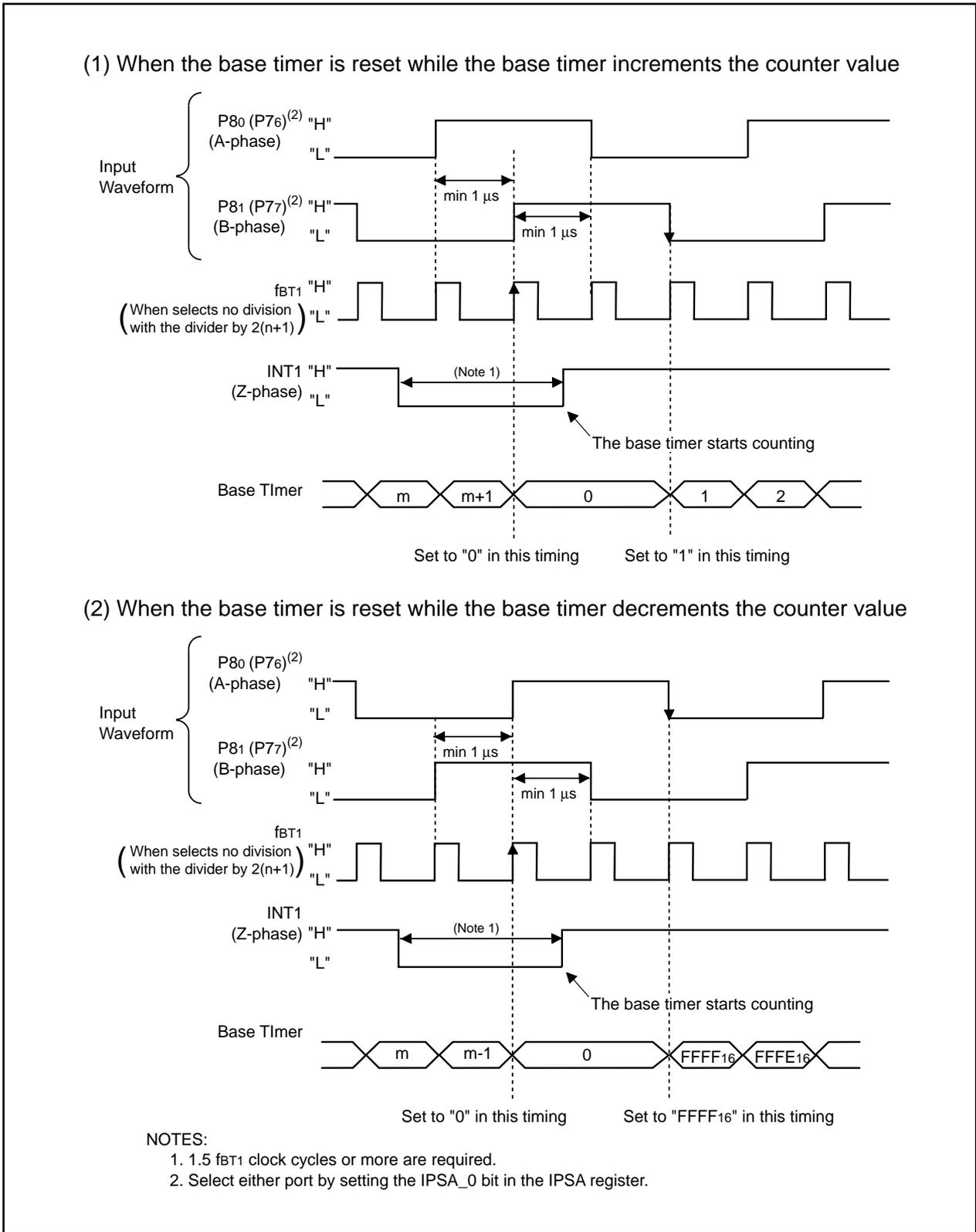


Figure 22.12 Base Timer Operation in Two-phase Pulse Signal Processing Mode

22.2 Time Measurement Function

When external trigger is applied, the value of the base timer is stored into the G1TMj register (j=0 to 7). Table 22.4 shows specifications of the time measurement function. Tables 22.5 and 22.6 list pin settings of the time measurement function. Figures 22.13 and 22.14 show operation examples of the time measurement function. Figure 22.15 shows an operation example of the prescaler function and gate function.

Table 22.4 Time Measurement Function Specifications

Item	Specification
Measurement Channel	Channels 0 to 7
Trigger Input Polarity	Rising edge, falling edge and both edges of the INPC1j pin
Measurement Start Condition	The IFEj bit in the G1FE register is set to "1" (channel j function enabled) when the FSCj bit (j=0 to 7) in the G1FS register is set to "1" (time measurement function selected)
Measurement Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Time Measurement Timing	<ul style="list-style-type: none"> • No prescaler: every time a trigger signal is applied • Prescaler (for channel 6 and channel 7): every <i>G1TPRk register (k=6,7) value +1</i> times a trigger signal is applied
Interrupt Request Generating Timing	The TM1jR bit in the interrupt request register (See Figure 11.14) is set to "1" (interrupt requested) at time measurement timing
INPC1j Pin Function	Trigger input pin
Selectable Function	<ul style="list-style-type: none"> • Digital filter function The digital filter samples a trigger input signal level every f1 or fBT1 cycles and passes pulse signals, matching trigger input signal level, three times • Prescaler function (for channel 6 and channel 7) Time measurement is executed every <i>G1TPRk register value +1</i> times a trigger signal is applied • Gate function (for channel 6 and channel 7) After time measurement by the first trigger input, trigger input cannot be accepted. However, while the GOC bit in the G1TMCRk register is set to "1" (gate cleared by matching the base timer with the G1POp register (p=4 when k=6, p=5 when k=7), trigger input can be accepted again by matching the base timer value with the G1POp register setting or by setting the GSC bit in the G1TMCRk register is set to "1"

Table 22.5 Pin Settings for Time Measurement Function

Pin	Bit and Setting		
	PS1, PS2, PS5, PS8 Registers	PD7, PD8, PD11, PD14 Registers	IPS Register
P70/INPC16	PS1_0 = 0	PD7_0 = 0	IPS1 = 0
P71/INPC17	PS1_1 = 0	PD7_1 = 0	
P73/INPC10	PS1_3 = 0	PD7_3 = 0	
P74/INPC11	PS1_4 = 0	PD7_4 = 0	
P75/INPC12	PS1_5 = 0	PD7_5 = 0	
P76/INPC13	PS1_6 = 0	PD7_6 = 0	
P77/INPC14	PS1_7 = 0	PD7_7 = 0	
P81/INPC15	PS2_1 = 0	PD8_1 = 0	
P110/INPC10 ⁽¹⁾	PS5_0 = 0	PD11_0 = 0	IPS1 = 1
P111/INPC11 ⁽¹⁾	PS5_1 = 0	PD11_1 = 0	
P112/INPC12 ⁽¹⁾	PS5_2 = 0	PD11_2 = 0	
P113/INPC13 ⁽¹⁾	PS5_3 = 0	PD11_3 = 0	
P140/INPC14 ⁽¹⁾	PS8_0 = 0	PD14_0 = 0	
P141/INPC15 ⁽¹⁾	PS8_1 = 0	PD14_1 = 0	
P142/INPC16 ⁽¹⁾	PS8_2 = 0	PD14_2 = 0	
P143/INPC17 ⁽¹⁾	PS8_3 = 0	PD14_3 = 0	

NOTES:

1. This port is provided in the 144-pin package only.

Table 22.6 Time Measurement Function Associated Register Settings

Register	Bit	Function
G1TMCRj	CTS1, CTS0	Select a time measurement trigger
	DF1, DF0	Select the digital filter function
	GT, GOC, GSC	Select the gate function
	PR	Select the prescaler function
G1TPRk	-	Setting value of the prescaler
G1FS	FSCj	Set to "1" (time measurement function)
G1FE	IFEj	Set to "1" (channel j function enabled)

j = 0 to 7 k = 6, 7

Bit configurations and functions vary with channels used.

Registers associated with the time measurement function must be set after setting registers associated with the base timer.

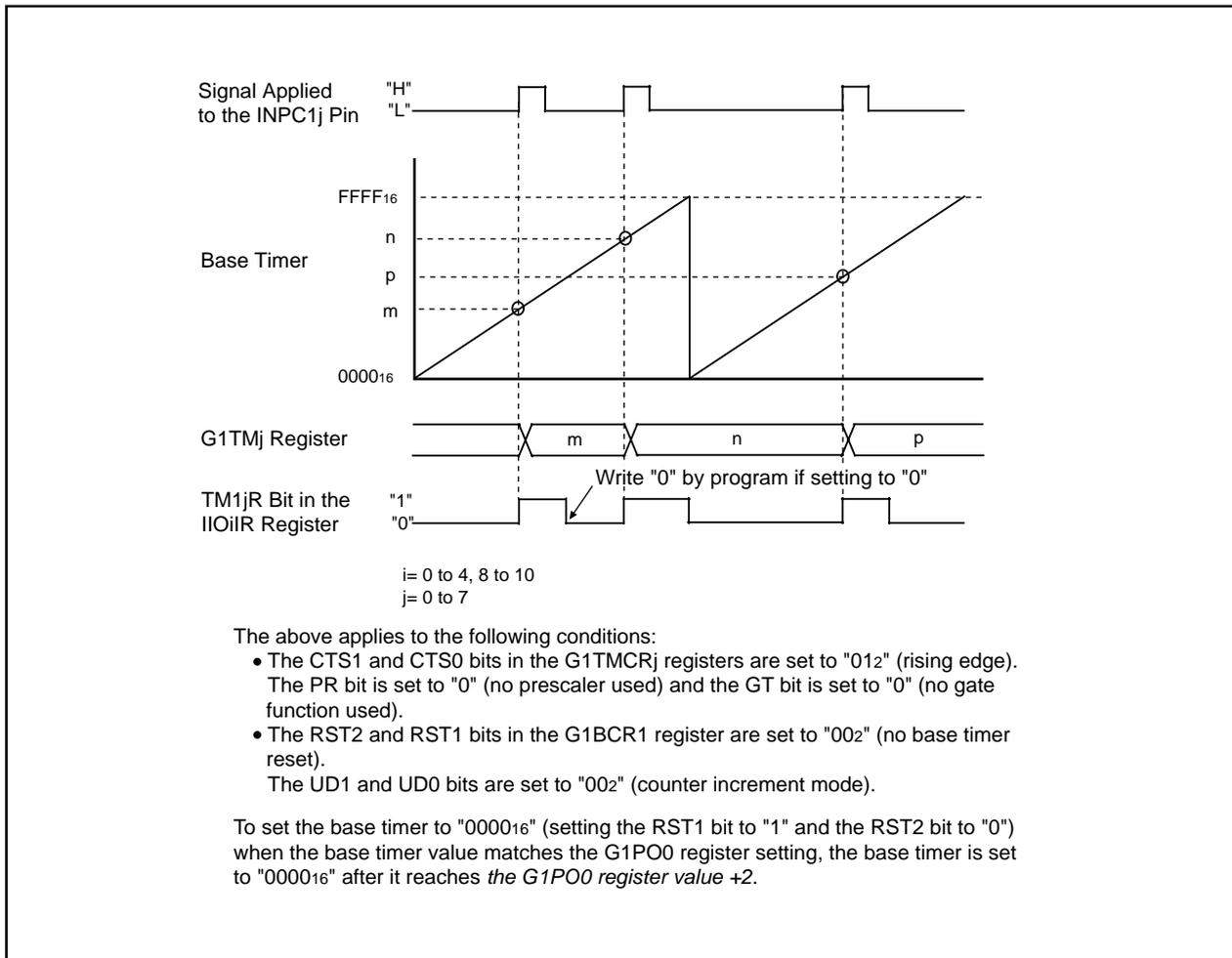


Figure 22.13 Time Measurement Function (1)

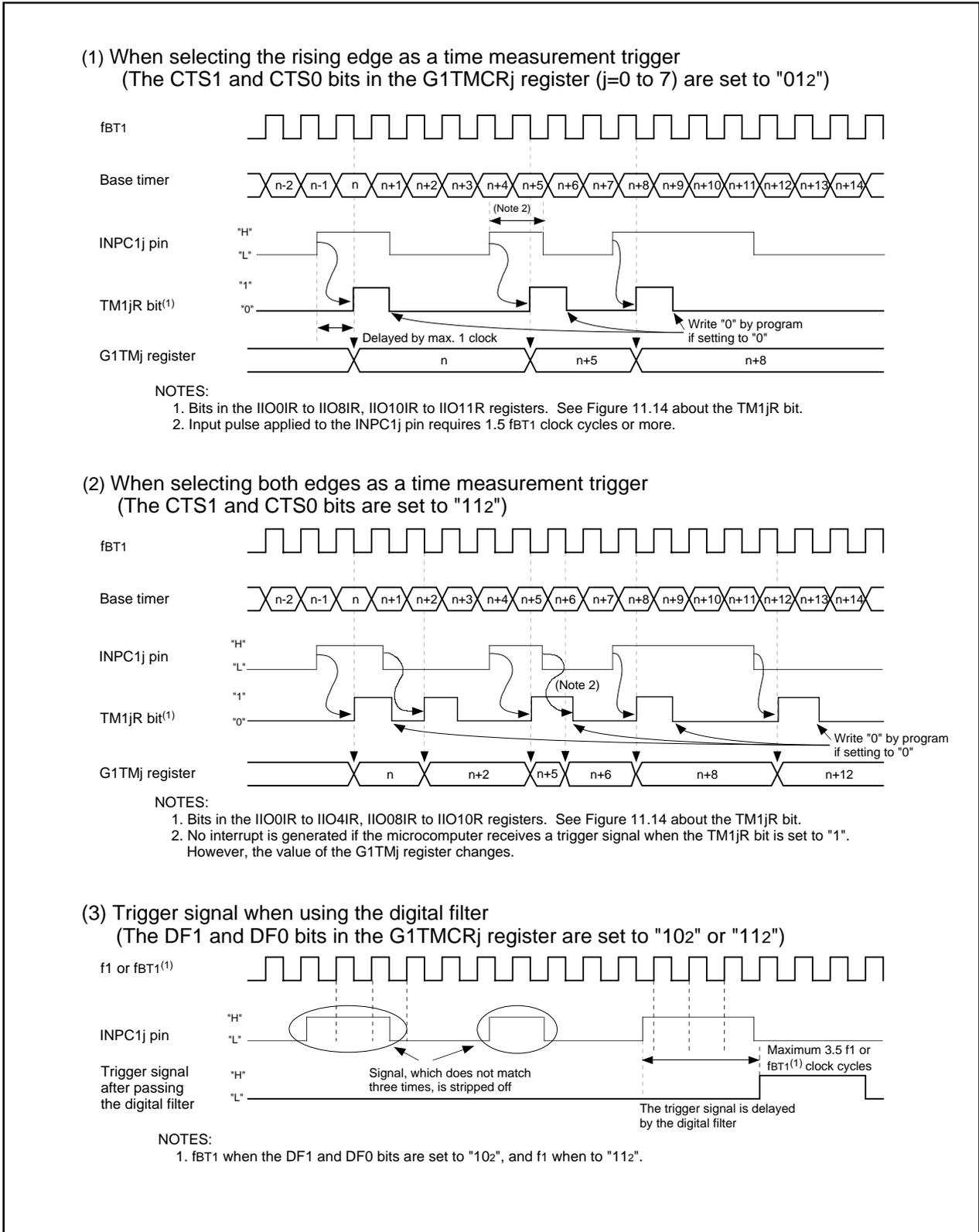


Figure 22.14 Time Measurement Function (2)

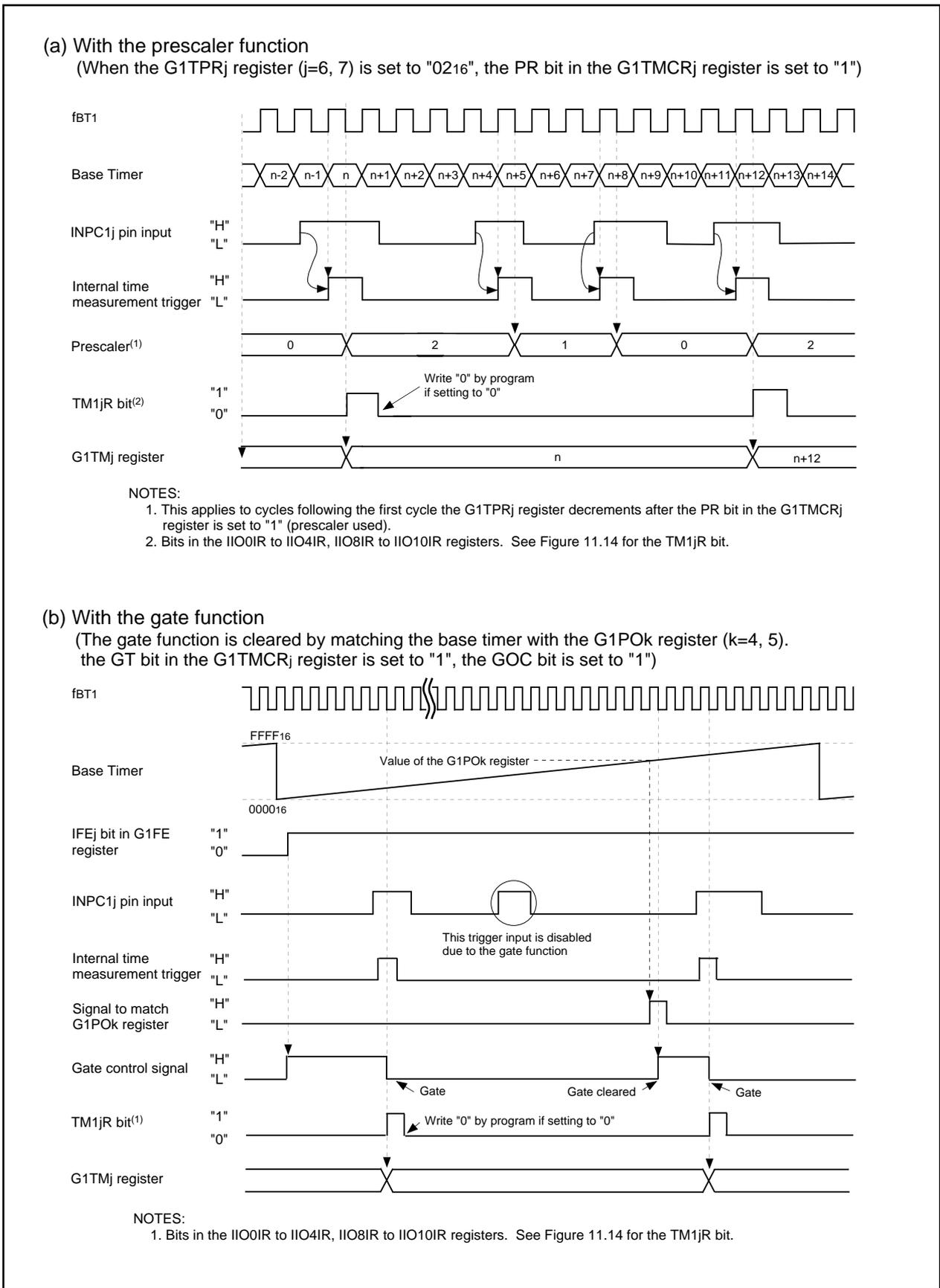


Figure 22.15 Prescaler Function and Gate Function

22.3 Waveform Generating Function

Waveforms are generated when the value of the base timer matches that of the G1POj register (j=0 to 7). The waveform generating function has the following three modes :

- Single-phase waveform output mode
- Phase-delayed waveform output mode
- Set/Reset waveform output (SR waveform output) mode

Table 22.7 lists pin settings of the waveform generating function. Table 22.8 lists registers associated with the waveform generating function.

Table 22.7 Pin Settings for Waveform Generating Function

Pin	Bit and Setting			
	PS1, PS2, PS5 to PS8 Registers	PSL1, PSL2 Registers	PSC, PSC2 Registers	PSD1 Register
P70/OUTC16	PS1_0 = 1	PSL1_0 = 0	PSC_0 = 1	PSD1_0=1
P71/OUTC17	PS1_1 = 1	PSL1_1 = 0	PSC_1 = 1	PSD1_1=1
P73/OUTC10	PS1_3 = 1	PSL1_3 = 0	PSC_3 = 1	-
P74/OUTC11	PS1_4 = 1	PSL1_4 = 0	PSC_4 = 1	-
P75/OUTC12	PS1_5 = 1	PSL1_5 = 1	-	-
P76/OUTC13	PS1_6 = 1	PSL1_6 = 0	PSC_6 = 0	PSD1_6=1
P77/OUTC14	PS1_7 = 1	PSL1_7 = 1	-	-
P81/OUTC15	PS2_1 = 1	PSL2_1 = 1	PSC2_1=1	-
P110/OUTC10 ⁽¹⁾	PS5_0 = 1	-	-	-
P111/OUTC11 ⁽¹⁾	PS5_1 = 1			
P112/OUTC12 ⁽¹⁾	PS5_2 = 1			
P113/OUTC13 ⁽¹⁾	PS5_3 = 1			
P140/OUTC14 ⁽¹⁾	PS8_0 = 1			
P141/OUTC15 ⁽¹⁾	PS8_1 = 1			
P142/OUTC16 ⁽¹⁾	PS8_2 = 1			
P143/OUTC17 ⁽¹⁾	PS8_3 = 1			

NOTES:

1. This port is provided in the 144-pin package only.

Table 22.8 Waveform Generating Function Associated Register Settings

Register	Bit	Function
G1POCRj	MOD2 to MOD0	Select waveform output mode
	IVL	Select default output value
	RLD	Select a timing to reload the value of the G1POj register
	INV	Select if output level is inversed
G1POj	-	Select when output waveform is inversed
G1FS	FSCj	Set to "0" (waveform generating function)
G1FE	IFEj	Set to "1" (enables a function on channel j)

j = 0 to 7

Bit configurations and functions vary with channels used.

Registers associated with the waveform generating measurement function must be set after setting registers associated with the base timer.

22.3.1 Single-Phase Waveform Output Mode

Output signal level of the OUTC1j pin becomes high ("H") when the value of the base timer matches that of the G1POj register (j=0 to 7). The "H" signal switches to a low-level ("L") signal when the base timer reaches "0000₁₆". If the IVL bit in the G1POCRj register is set to "1" ("H" output as default value), an "H" signal output is provided when waveform output starts. If the INV bit is set to "1" (output inverted), the level of the waveform output is inverted. See Figure 22.16 for details on single-phase waveform output mode operation. Table 22.9 lists specifications of single-phase waveform output mode.

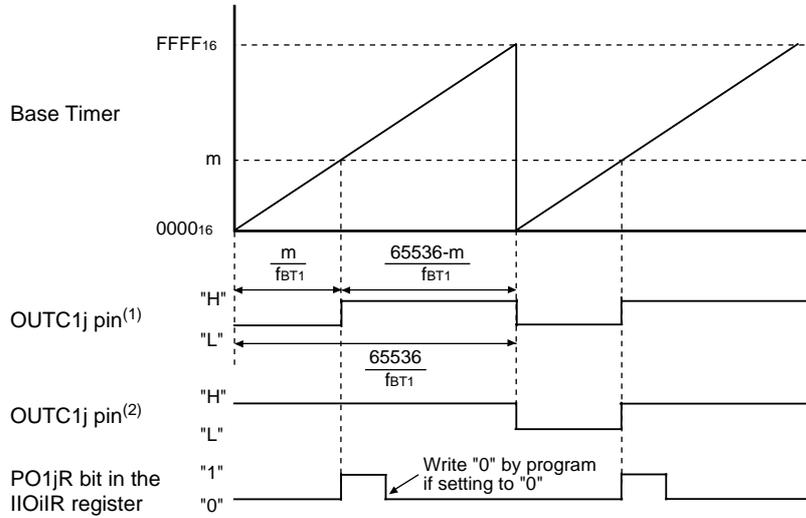
Table 22.9 Single-Phase Waveform Output Mode Specifications

Item	Specification
Output Waveform ⁽²⁾	<ul style="list-style-type: none"> Free-running operation (the RST2 and RST1 bits in the G1BCR1 register are set to "002") <p>Cycle : $\frac{65536}{f_{BT1}}$</p> <p>"L" width : $\frac{m}{f_{BT1}}$</p> <p>"H" width : $\frac{65536-m}{f_{BT1}}$</p> <p>m : setting value of the G1POj register (j=0 to 7), 0000₁₆ to FFFF₁₆</p> <ul style="list-style-type: none"> The base timer is cleared to "0000₁₆" by matching the base timer with the G1PO0 register (the RST1 bit is set to "1" and the RST2 bit is set to "0") <p>Cycle : $\frac{n+2}{f_{BT1}}$</p> <p>"L" width : $\frac{m}{f_{BT1}}$</p> <p>"H" width : $\frac{n+2-m}{f_{BT1}}$</p> <p>m : setting value of the G1POj register (j=1 to 7), 0000₁₆ to FFFF₁₆</p> <p>n : setting value of the G1PO0 register, 0001₁₆ to FFFD₁₆</p> <p>If $m \geq n+2$, the output level is fixed to "L"</p>
Waveform Output Start Condition ⁽¹⁾	The IFEj bit in the G1FE register is set to "1" (channel j function enabled)
Waveform Output Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Interrupt Request	The PO1jR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the G1POj register. (See Figure 11.14)
OUTC1j Pin	Pulse signal output pin
Selectable Function	<ul style="list-style-type: none"> Default value set function: Set starting waveform output level Inversed output function: Waveform output signal is inverted and provided from the OUTC1j pin

NOTES:

- Set the FSCj bit in the G1FS register to "0" (waveform generating function selected).
- When the INV bit in the G1POCRj register is set to "1" (output inverted), the "L" width and "H" width are inverted.

(1) Free-Running Operation
 (The RST2 to RST1 bits in the G1BCR1 register are set to "002")



$i=0$ to 4, 8 to 10; $j=0$ to 7
 m : Setting value of the G1POj register, 0000_{16} to $FFFF_{16}$

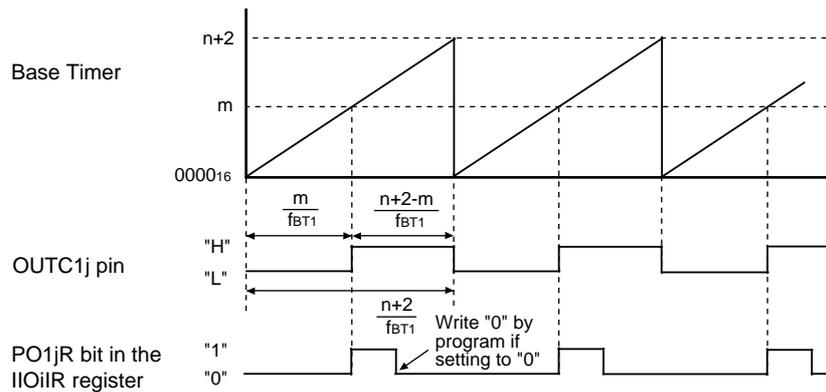
NOTES:

1. Waveform output when the INV bit in the G1POCRj register is set to "0" (not inverted) and the IVL bit is set to "0" (output "L" as default value).
2. Waveform output when the INV bit is set to "0" (not inverted) and the IVL bit is set to "1" ("H" output as default value).

The above applies under the following condition:

- The RST2 and RST1 bits in the G1BCR1 register are set to "002" (no base timer reset) and the UD1 and UD0 bits to "002" (counter increment mode)

(2) The Base Timer is Reset when the Base Timer Matches the G1PO0 Register
 (The RST1 bit is set to "1" and the RST2 bit is set to "0")



$i=0$ to 4, 8 to 10; $j=1$ to 7
 m : Setting value of the G1POj register, 0000_{16} to $FFFF_{16}$
 n : Setting value of the G1PO0 register, 0001_{16} to $FFFD_{16}$

The above diagram applies under the following conditions:

- The IVL bit in the G1POCRj register is set to "0" ("L" output as default value). The INV bit is set to "0" (not inverted).
- The UD1 and UD0 bits in the G1BCR1 register are set to "002" (counter increment mode)
- $m < n+2$

Figure 22.16 Single-Phase Waveform Output Mode

22.3.2 Phase-Delayed Waveform Output Mode

Output signal level of the OUTC1j pin is inverted every time the value of the base timer matches that of the G1POj register (j=0 to 7). Table 22.10 lists specifications of phase-delayed waveform output mode. Figure 22.17 lists an example of phase-delayed waveform output mode operation.

Table 22.10 Phase-Delayed Waveform Output Mode Specifications

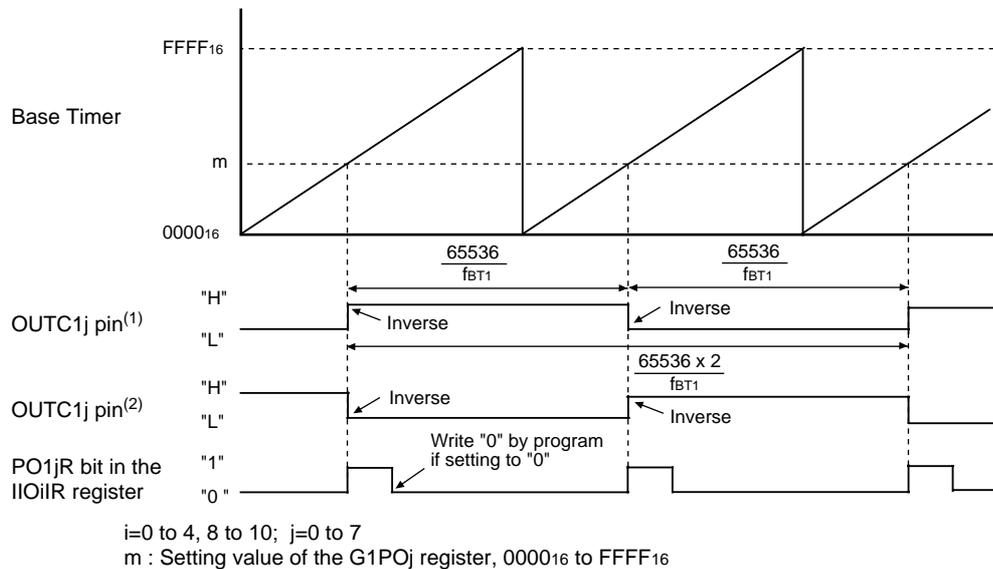
Item	Specification
Output Waveform	<ul style="list-style-type: none"> Free-running operation (the RST2 and RST1 bits in the G1BCR1 register are set to "002") <p>Cycle : $\frac{65536 \times 2}{f_{BT1}}$</p> <p>"H" and "L" widths : $\frac{65536}{f_{BT1}}$</p> <p>Setting value of the G1POj (j=0 to 7) register is 0000₁₆ to FFFF₁₆</p> <ul style="list-style-type: none"> The base timer is cleared to "0000₁₆" by matching the base timer with the G1PO0 register (the RST1 bit is set to "1" and the RST2 bit is set to "0") <p>Cycle : $\frac{2(n+2)}{f_{BT1}}$</p> <p>"H" and "L" widths : $\frac{n+2}{f_{BT1}}$</p> <p>n : setting value of the G1PO0 register, 0001₁₆ to FFFD₁₆</p> <p>Setting value of the G1POj (j=1 to 7) register is 0000₁₆ to FFFF₁₆</p> <p>If G1POj register $\geq n+2$, the output level is not inverted</p>
Waveform Output Start Condition ⁽¹⁾	The IFEj bit (j=0 to 7) in the G1FE register is set to "1" (channel j function enabled)
Waveform Output Stop Condition	The IFEj bit is set to "0" (channel j function disabled)
Interrupt Request	The PO1jR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the G1POj register. (See Figure 11.14)
OUTC1j Pin	Pulse signal output pin
Selectable Function	<ul style="list-style-type: none"> Default value set function: Set starting waveform output level Inversed output function <p>Waveform output level is inverted to output a waveform from the OUTC1j pin</p>

NOTES:

- Set the FSCj bit in the G1FS register to "0" (waveform generating function selected).

(1) Free-Running Operation

(The RST2 to RST1 bits in the G1BCR1 register are set to "002")



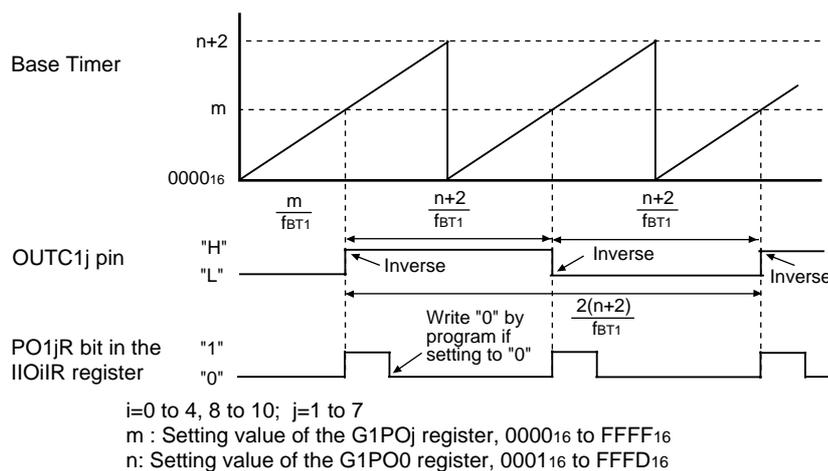
NOTES:

1. Waveform output when the INV bit in the G1POCRj register is set to "0" (not inverted) and the IVL bit is set to "0" ("L" output as default value).
2. Waveform output when the INV bit is set to "0" (not inverted) and the IVL bit is set to "1" ("H" output as default value).

The above diagram applies under the following condition:

- The RST2 and RST1 bits in the G1BCR1 register are set to "002" (no base timer reset) and the UD1 and UD0 bits to "002" (counter increment mode).

(2) The Base Timer is Reset when the Base Timer Matches the G1PO0 Register
(The RST1 bit is set to "1" and the RST2 bit is set to "0")



The above diagram applies to the following conditions:

- The IVL bit in the G1POCRj register is set to "0" ("L" output as default value). The INV bit is set to "0" (not inverted).
- The UD1 and UD0 bits in the G1BCR1 register are set to "002" (counter increment mode).
- $m < n+2$

Figure 22.17 Phase-delayed Waveform Output Mode

22.3.3 Set/Reset Waveform Output (SR Waveform Output) Mode

Output signal level of the OUTC1j pin becomes high ("H") when the value of the base timer matches that of the G1POj register (j=0, 2, 4, 6). The "H" signal switches to a low-level ("L") signal when the value of the base timer matches that of the G1POk register (k=j+1) or when the base timer is set to "000016". If the IVL bit in the G1POCRj register is set to "1" ("H" output as default value), an "H" signal output is provided when waveform output starts. If the INV bit is set to "1" (output inversed), the level of the output waveform is inversed. Table 22.11 lists specifications of SR waveform output mode. Figure 22.18 shows an example of a SR waveform output mode operation.

Table 22.11 SR Waveform Output Mode Specifications

Item	Specification
Output Waveform ⁽²⁾	<ul style="list-style-type: none"> • Free-running operation (the RST2 and RST1 bits in the G1BCR1 register are set to "002") (1) $m < n$ $\begin{aligned} \text{"H" width} &: \frac{n-m}{f_{BT1}} \\ \text{"L" width} &: \frac{m^{(3)}}{f_{BT1}} + \frac{65536 - n^{(4)}}{f_{BT1}} \end{aligned}$ (2) $m \geq n$ $\begin{aligned} \text{"H" width} &: \frac{65536 - m}{f_{BT1}} \\ \text{"L" width} &: \frac{m}{f_{BT1}} \end{aligned}$ <p style="margin-left: 40px;">m : setting value of the G1POj register (j=0, 2, 4, 6) n : setting value of the G1POk register (k=j+1)</p> • The base timer is cleared to "000016" by matching the base timer with the G1PO0 register⁽¹⁾ (the RST1 bit is set to "1" and the RST2 bit is set to "0") (1) $m < n < p+2$ $\begin{aligned} \text{"H" width} &: \frac{n-m}{f_{BT1}} \\ \text{"L" width} &: \frac{m^{(3)}}{f_{BT1}} + \frac{p+2 - n^{(4)}}{f_{BT1}} \end{aligned}$ (2) $m < p+2 \leq n$ $\begin{aligned} \text{"H" width} &: \frac{p+2 - m}{f_{BT1}} \\ \text{"L" width} &: \frac{m}{f_{BT1}} \end{aligned}$ (3) If $m \geq p+2$, the output level is fixed to "L" m : setting value of the G1POj register (j=2, 4, 6), 000016 to FFFF16 n : setting value of the G1POk register (k=j+1), 000016 to FFFF16 p : setting value of the G1PO0 register, 000116 to FFFD16

NOTES:

1. When the G1PO0 register resets the base timer, the channel 0 and 1 SR waveform generating functions are not available.
2. When the INV bit in the G1POCRj register is set to "1" (output inversed), the "L" width and "H" width are inversed.
3. Waveform from base timer reset until when output level becomes "H".
4. Waveform from when output level becomes "L" until base timer reset.

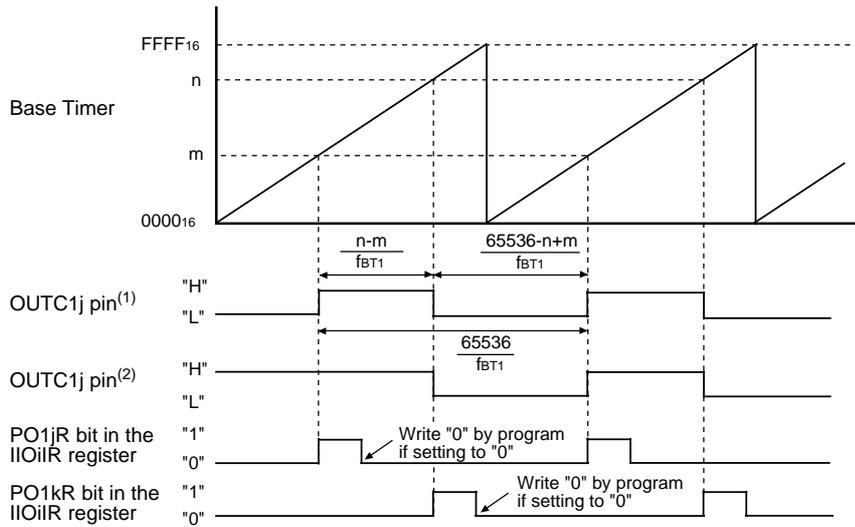
Table 22.11 SR Waveform Output Mode Specifications (Continued)

Item	Specification
Waveform Output Start Condition ⁽⁵⁾	The IFEq bit (q=0 to 7) in the G1FE register is set to "1" (channel q function enabled)
Waveform Output Stop Condition	The IFEq bit is set to "0" (channel q function disabled)
Interrupt Request	The PO1jR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the G1POj register. The PO1kR bit in the interrupt request register is set to "1" (interrupt requested) when the value of the base timer matches that of the G1POk register. (See Figure 11.14)
OUTC1j Pin	Pulse signal output pin
Selectable Function	<ul style="list-style-type: none"> • Default value set function: Set starting waveform output level • Inversed output function <p>Waveform output level is inversed to provide a waveform from the OUTC1j pin</p>

NOTES:

5. Set the FSCj bit in the G1FS register to "0" (waveform generating function selected).

(1) Free-Running Operation
 (The RST2 to RST0 bits in the G1BCR1 register are set to "002")



$i=0$ to 4, 8 to 10; $j=0, 2, 4, 6$; $k=j+1$
 m : Setting value of the G1POj register, 0000₁₆ to FFFF₁₆
 n : Setting value of the G1POk register, 0000₁₆ to FFFF₁₆

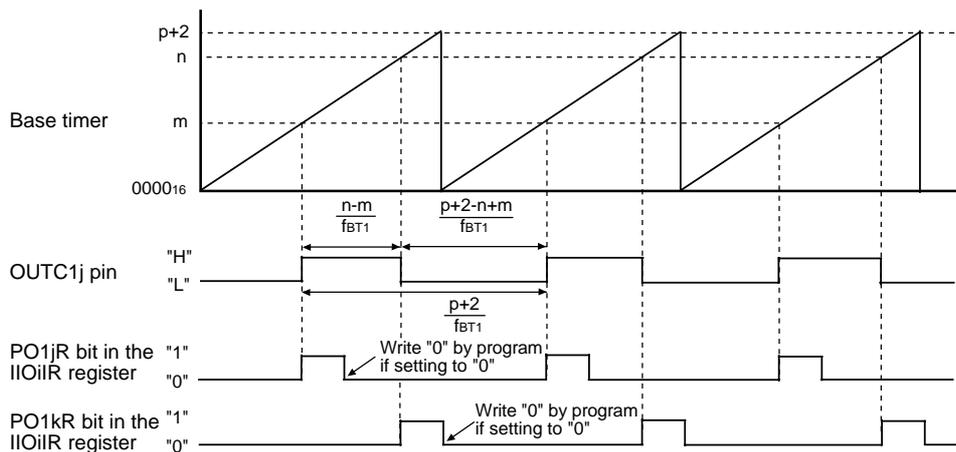
NOTES:

1. Waveform output when the INV bit in the G1POCRj register is set to "0" (not inverted) and the IVL bit is set to "0" (output "L" as default value).
2. Waveform output when the INV bit is set to "0" (not inverted) and the IVL bit is set to "1" ("H" output as default value).

The diagram above applies under the following condition:

- The RST2 and RST1 bits in the G1BCR1 register are set to "002" (no base timer reset) and the UD1 and UD0 bits to "002" (counter increment mode).
- $m < n$

(2) The Base Timer is Reset when the Base Timer Matches the G1PO0 Register
 (The RST1 bit is set to "1" and the RST2 bit is set to "0")



$i=0$ to 4, 8 to 10; $j=2, 4, 6$; $k=j+1$
 m : Setting value of the G1POj register, 0000₁₆ to FFFF₁₆
 n : Setting value of the G1POk register, 0000₁₆ to FFFF₁₆
 p : Setting value of the G1PO0 register, 0001₁₆ to FFFD₁₆

The diagram above applies to the following conditions:

- The IVL bit in the G1POCRj register is set to "0" ("L" output as default value). The INV bit is set to "0" (not inverted).
- The UD1 and UD0 bits in the G1BCR1 register are set to "002" (counter increment mode).
- $m < n < p+2$

Figure 22.18 SR Waveform Output Mode

22.4 Communication Unit 0 and 1 Communication Function

In the intelligent I/O communication unit 1, 8-bit clock synchronous serial I/O, 8-bit clock asynchronous serial I/O (UART) or HDLC data processing is available. In the communication unit 0, 8-bit clock synchronous serial I/O or HDLC data processing is available.

Figures 22.19 to 22.28 show registers associated with the communication function.

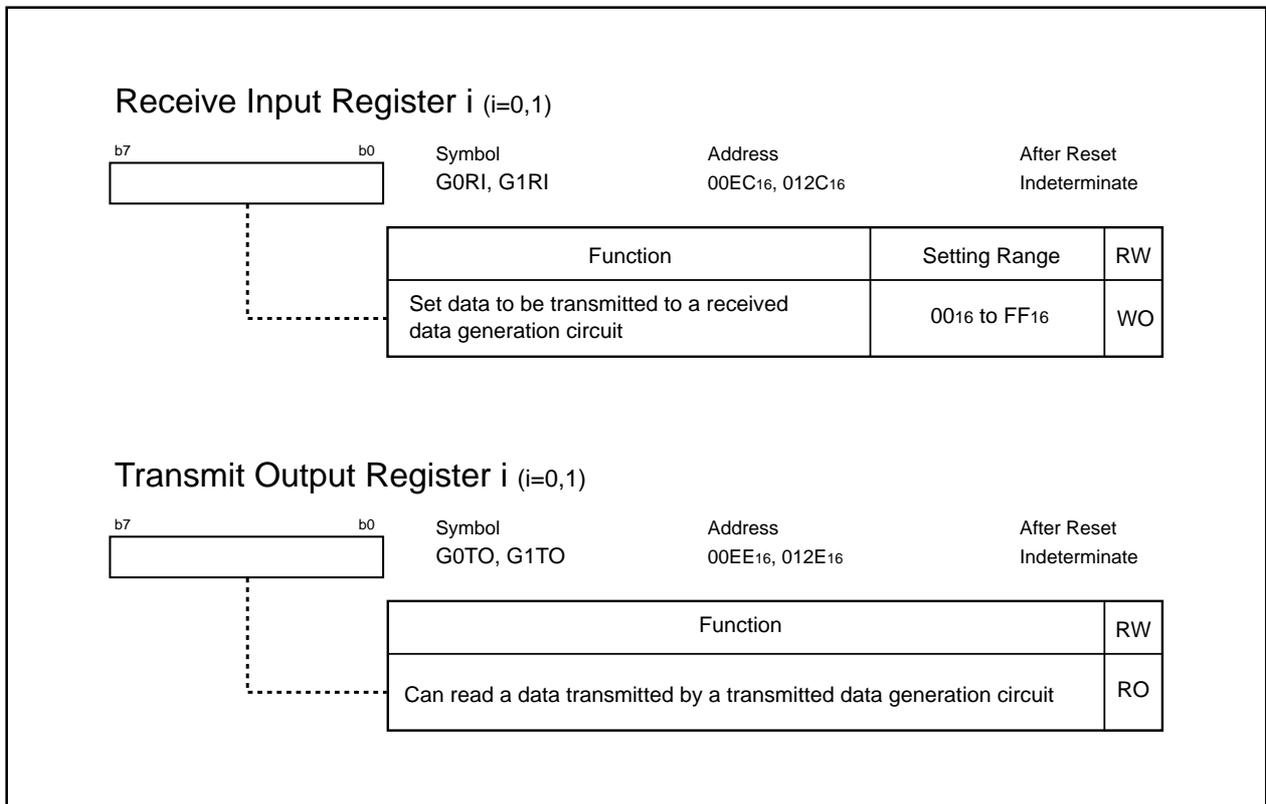


Figure 22.19 G0RI and G1RI Registers, G0TO and G1TO Registers

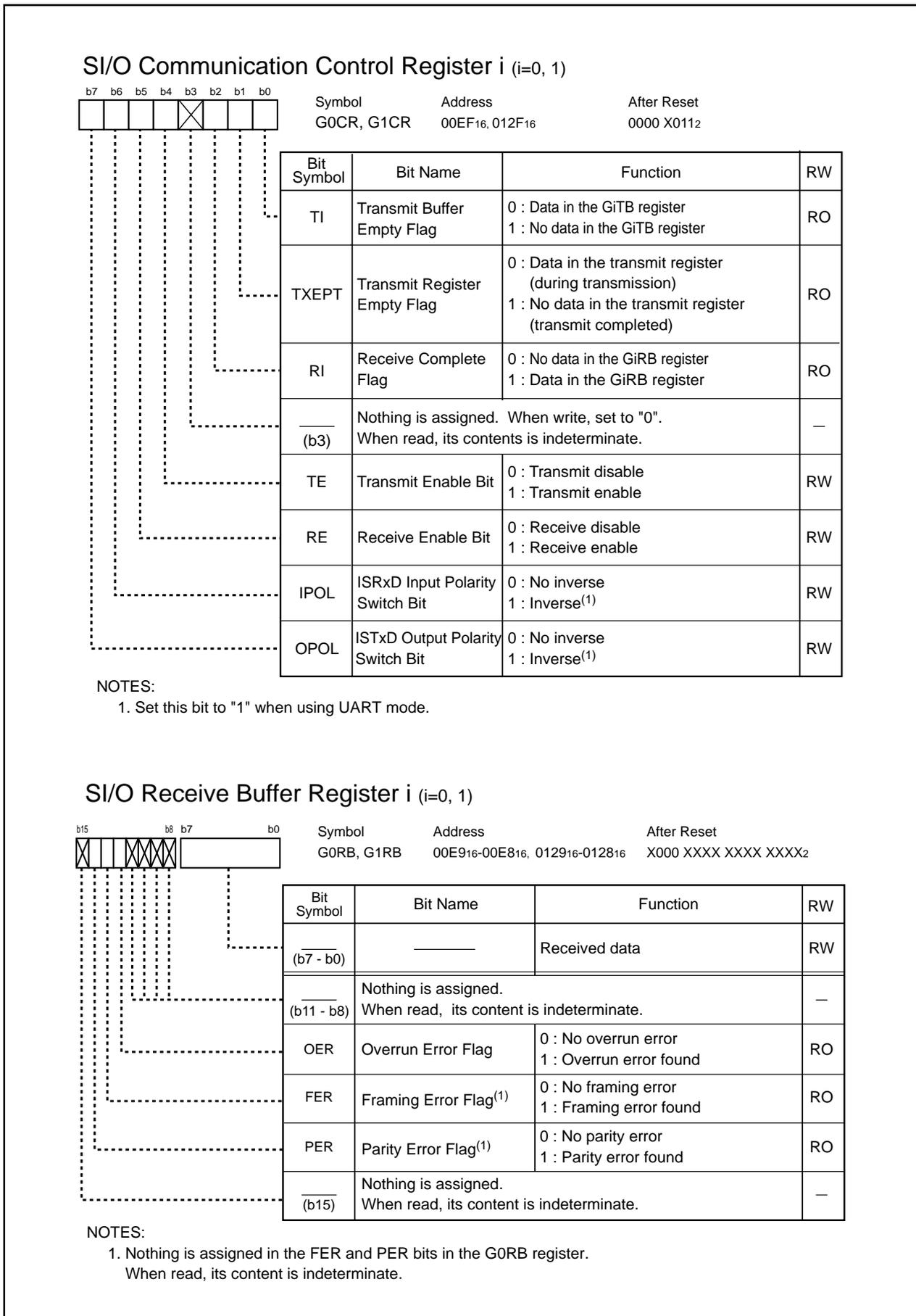


Figure 22.20 G0CR and G1CR Registers, G0RB and G1RB Registers

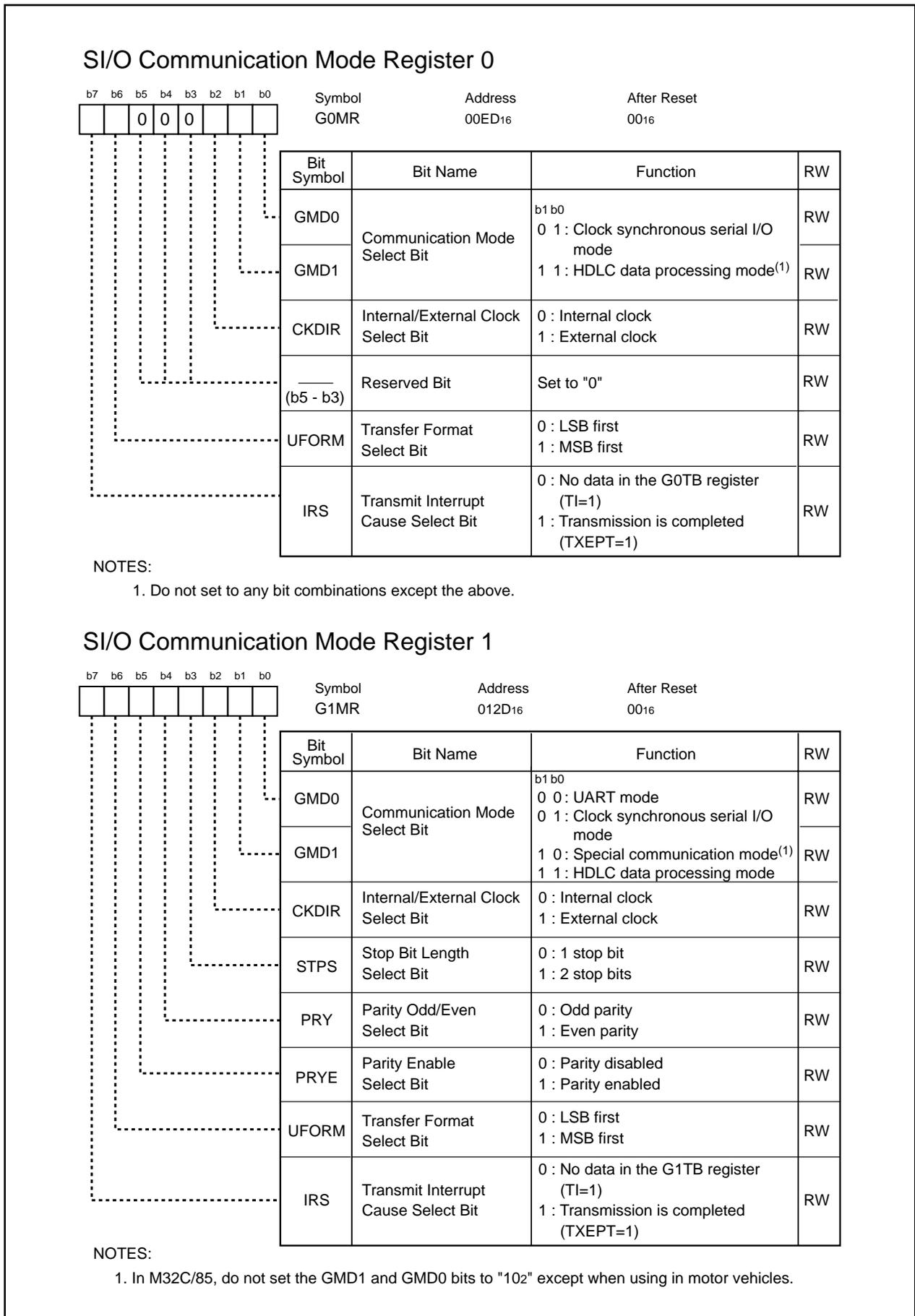


Figure 22.22 G0MR and G1MR Registers

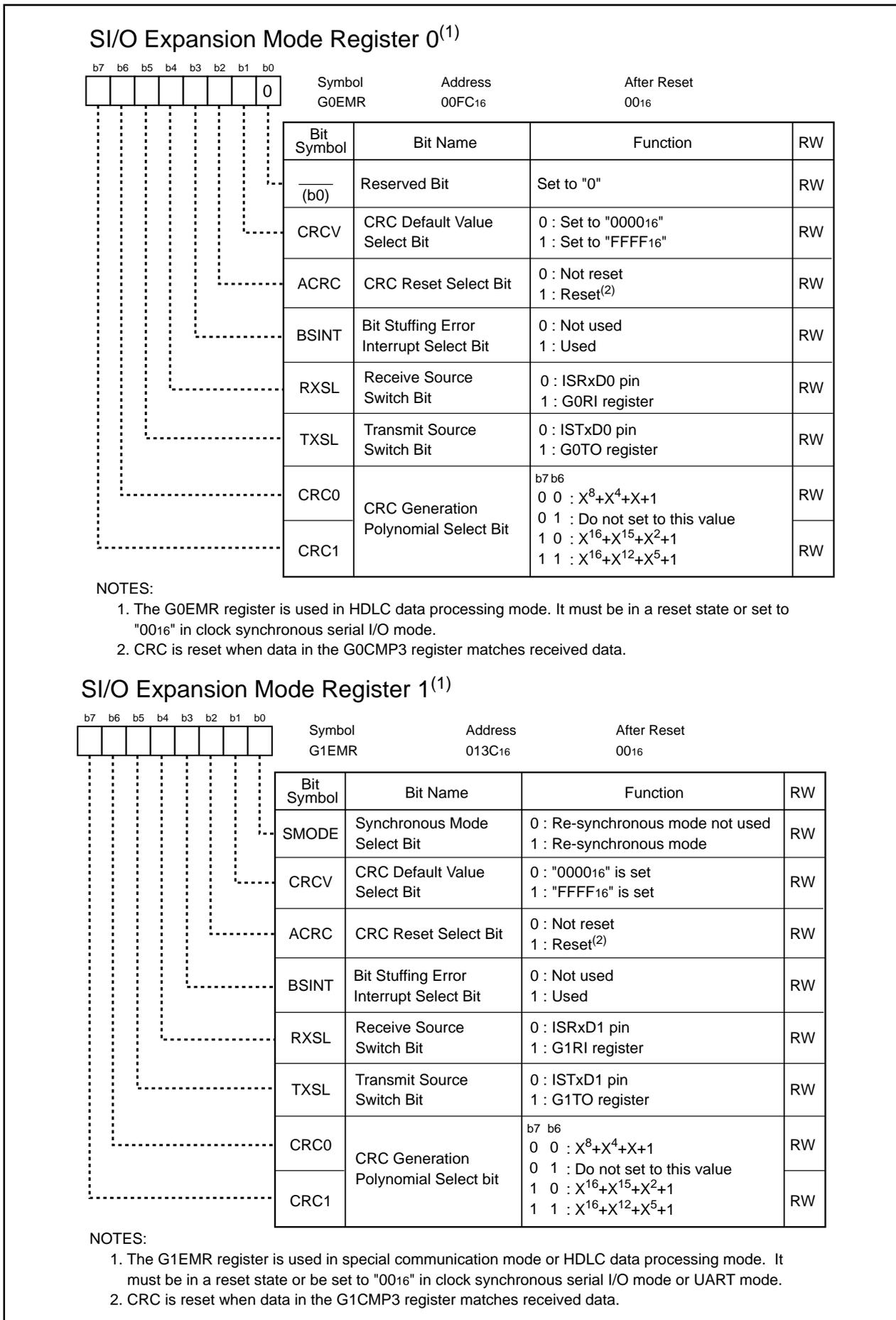


Figure 22.23 G0EMR and G1EMR Registers

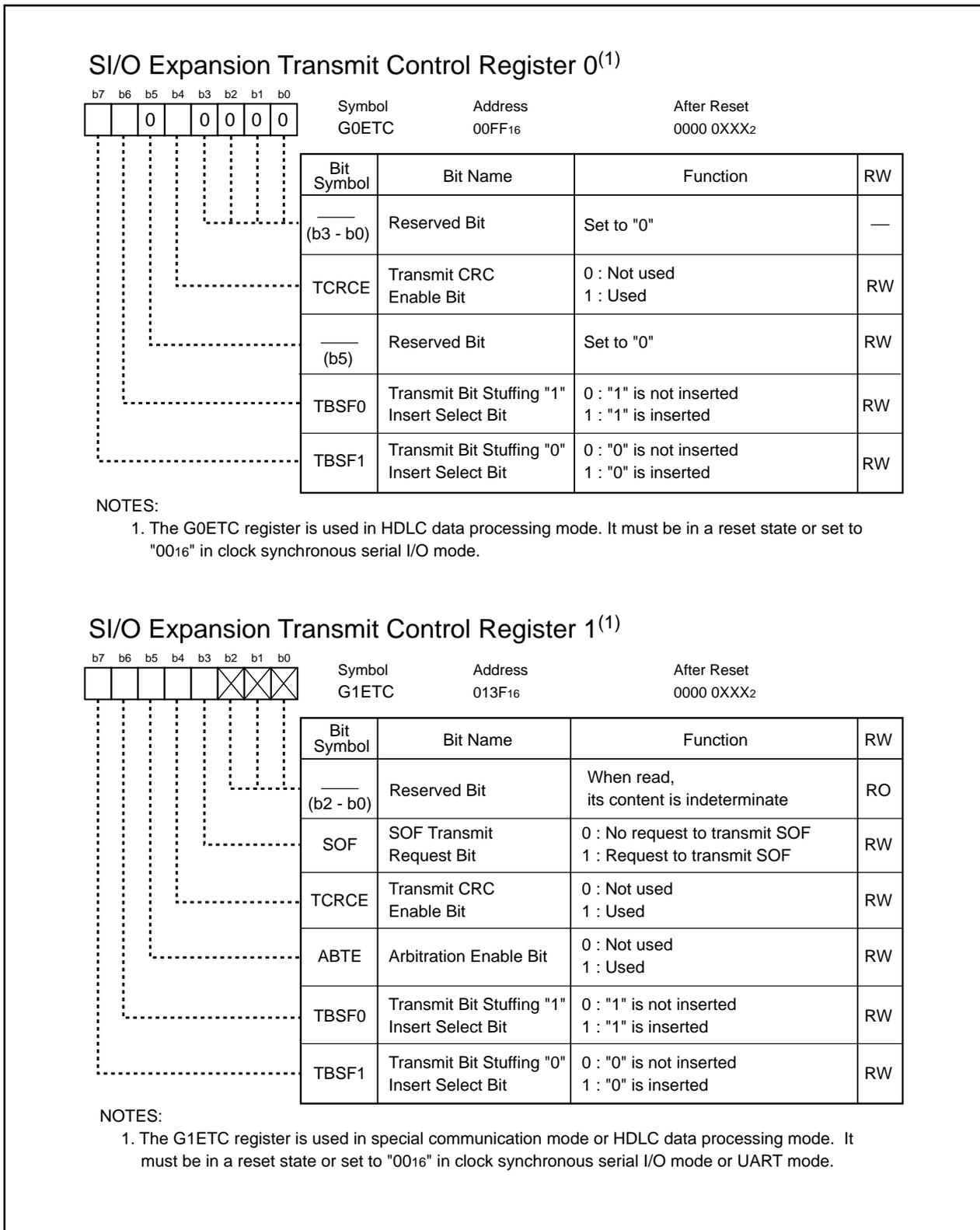


Figure 22.24 G0ETC and G1ETC Registers

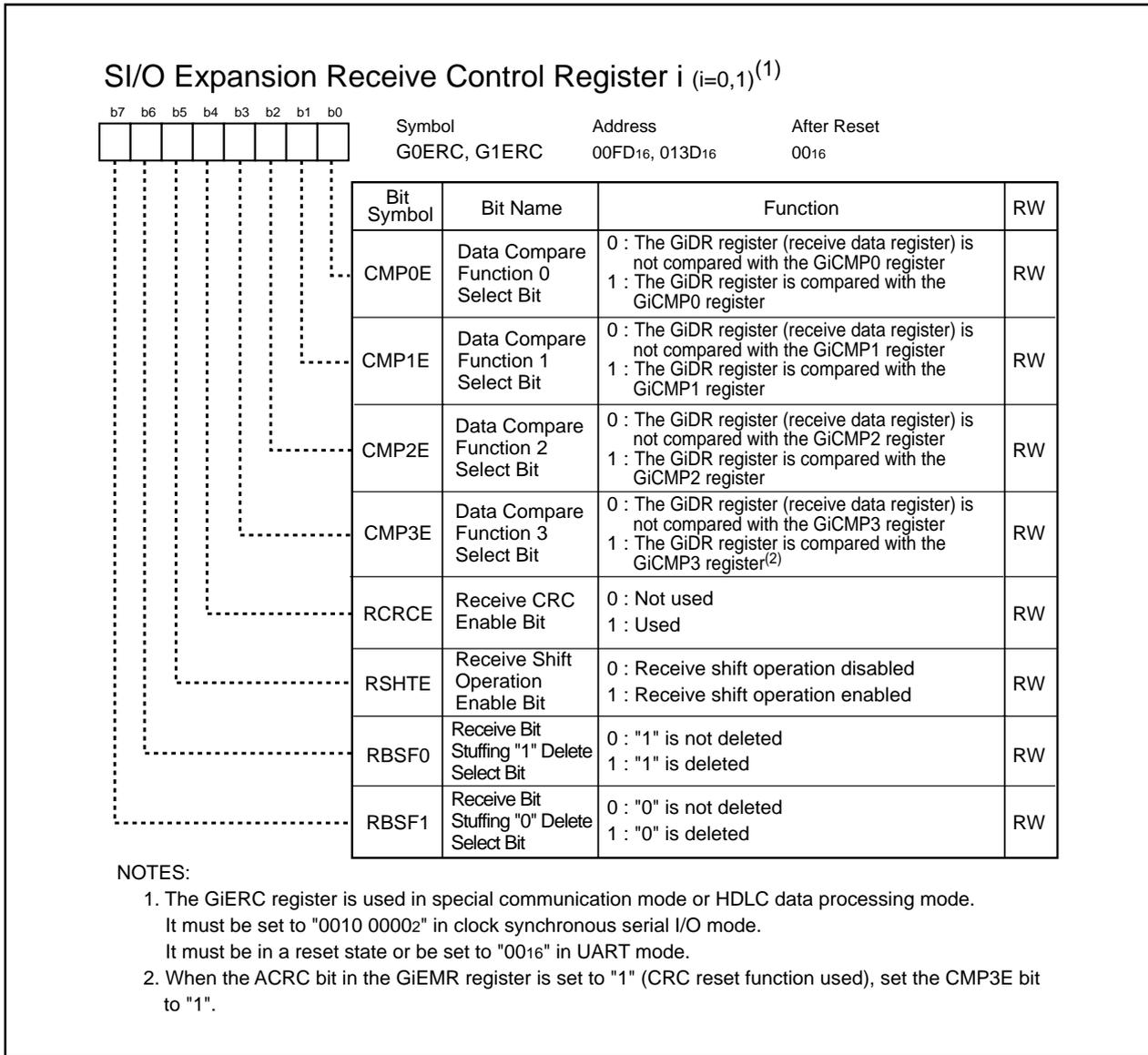


Figure 22.25 G0ERC and G1ERC Registers

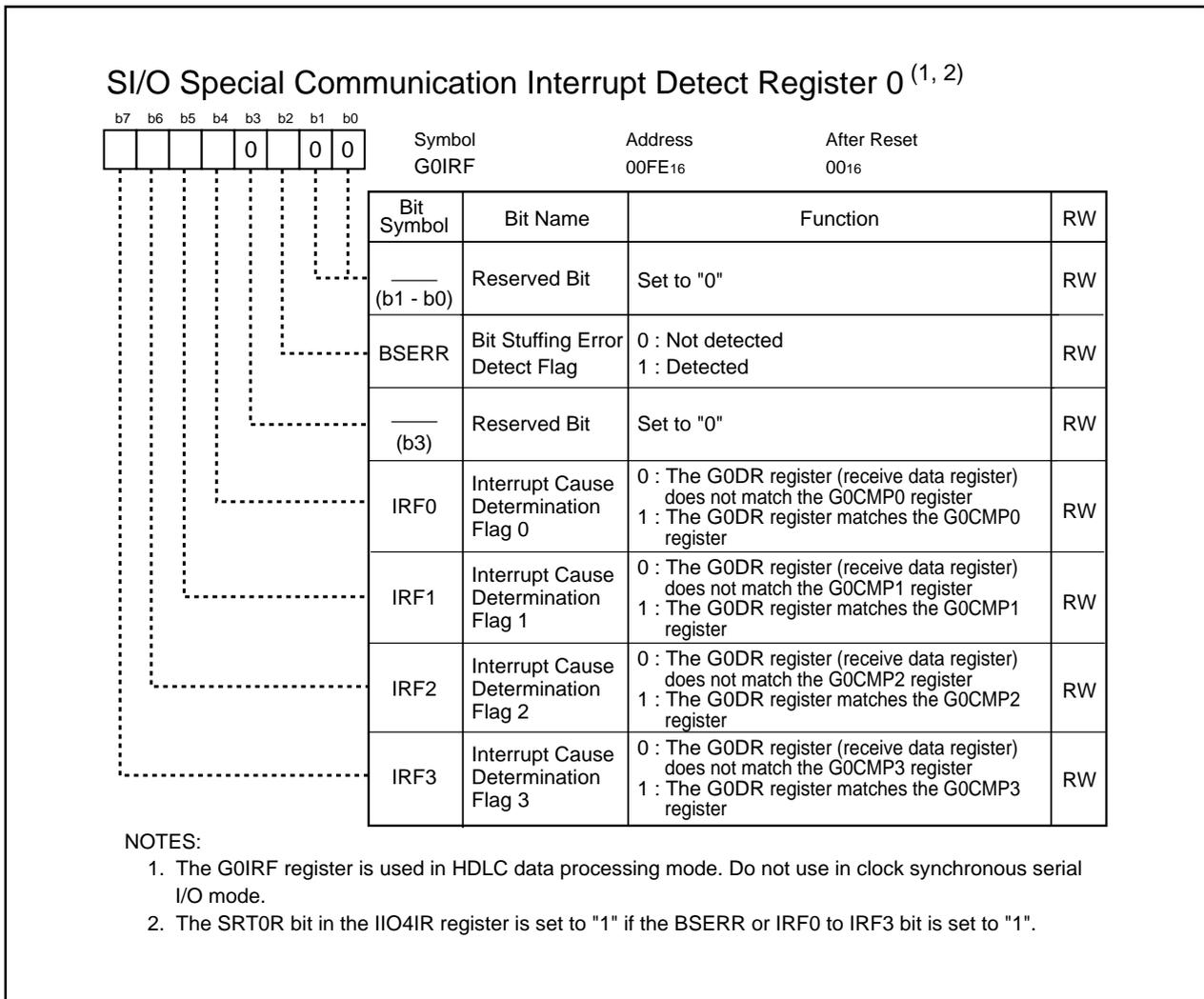


Figure 22.26 G0IRF Register

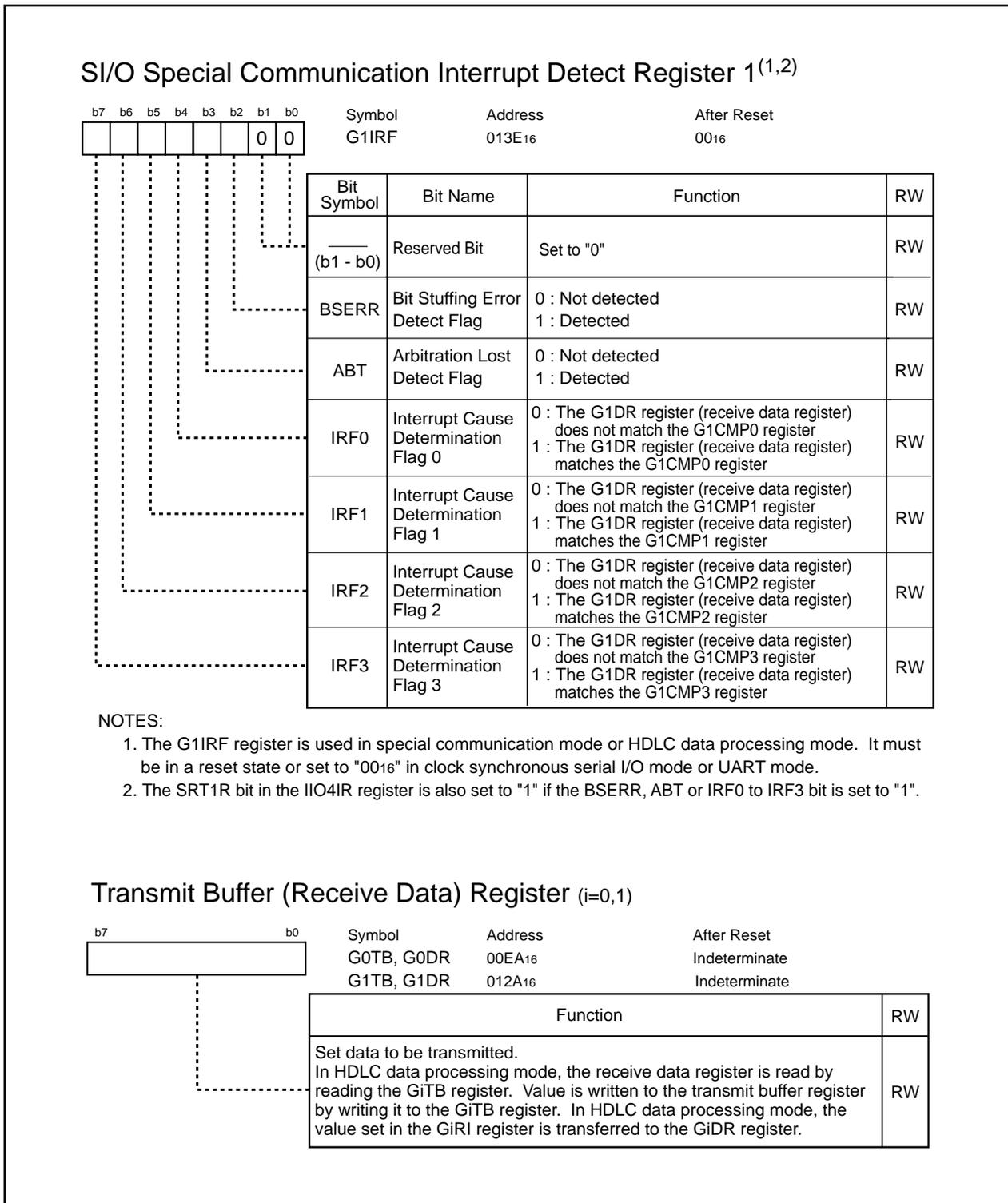
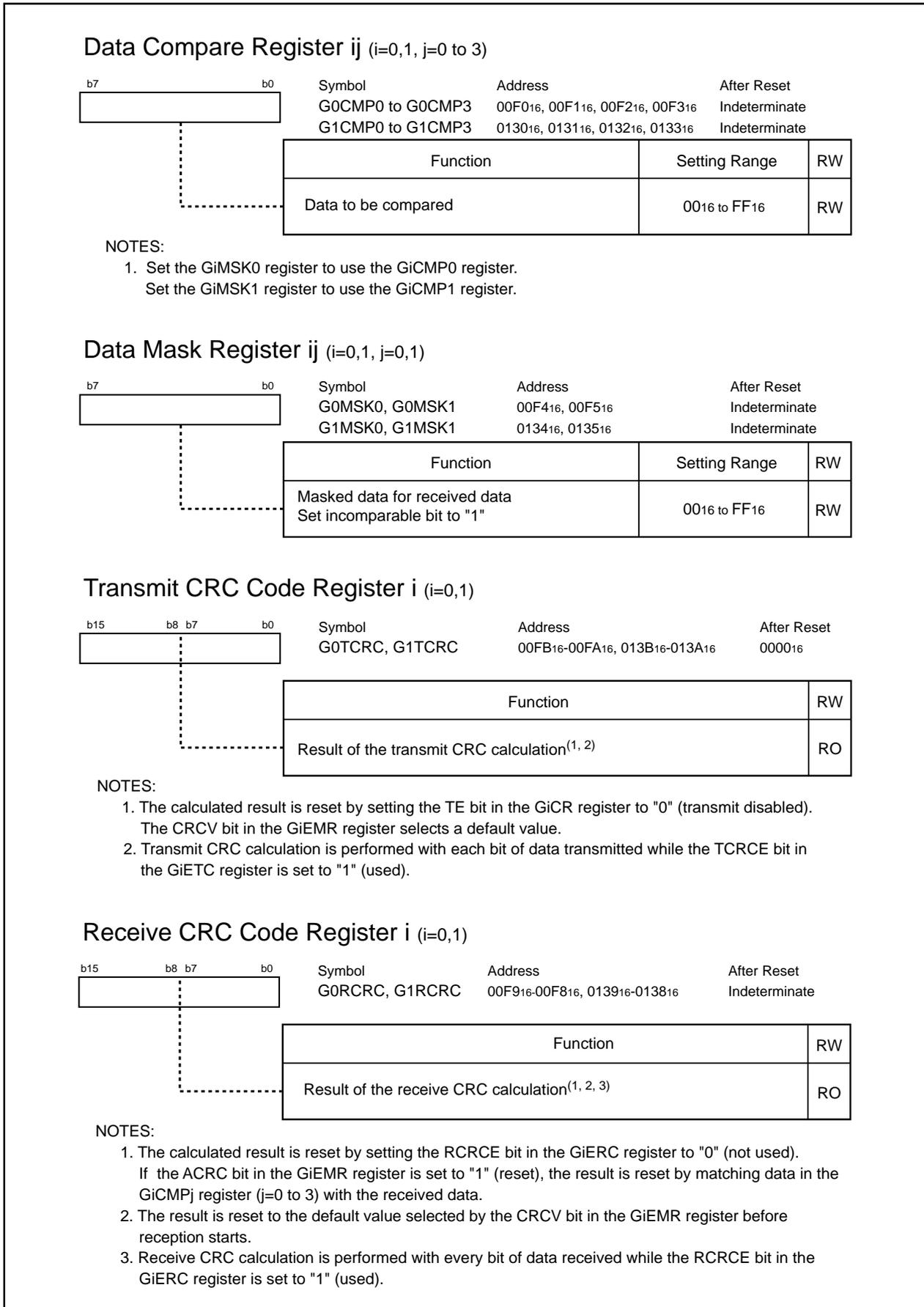


Figure 22.27 G1IRF Register, G0TB and G1TB / G0DR and G1DR Registers



**Figure 22.28 G0CMP0 to G0CMP3 Registers and G1CMP0 to G1CMP3 Registers
G0MSK0 and G0MSK1 Registers, G1MSK0 and G1MSK1 Registers
G0TCRC and G1TCRC Registers, G0RCRC and G1RCRC Registers**

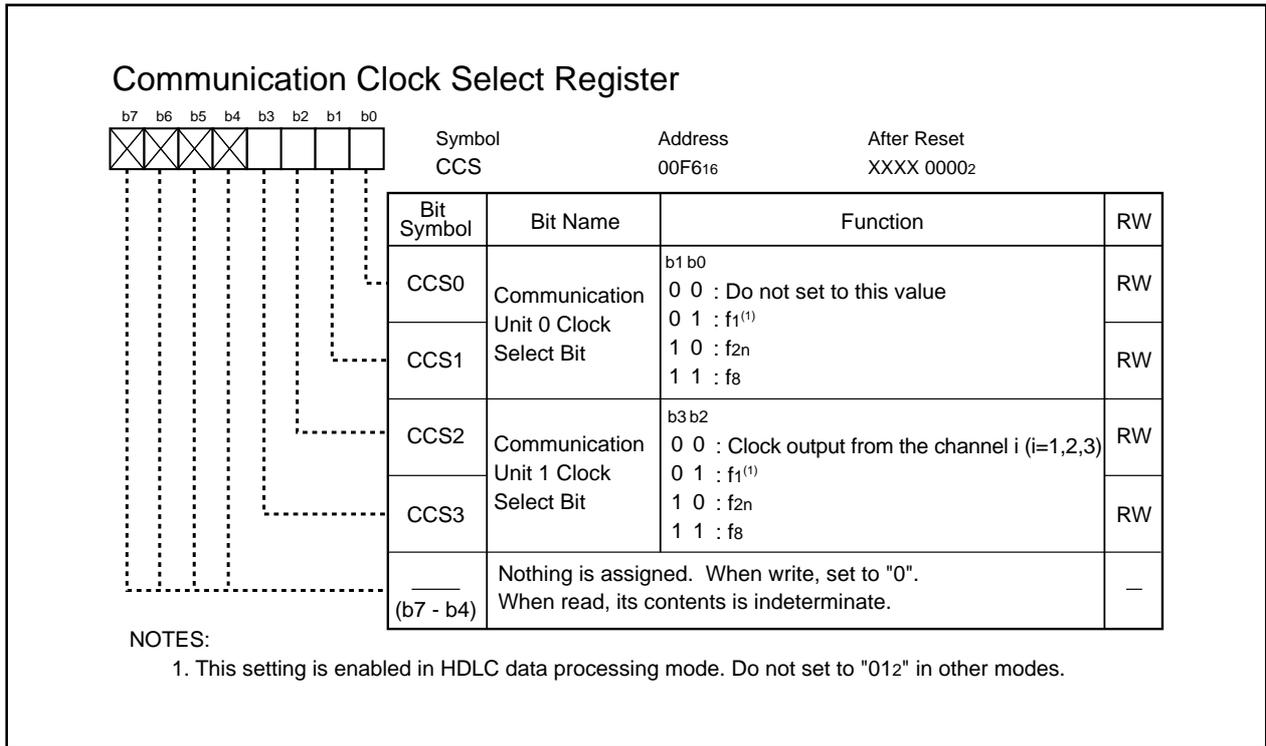


Figure 22.29 CCS Register

22.4.1 Clock Synchronous Serial I/O Mode (Communication Units 0 and 1)

In clock synchronous serial I/O mode, data is transmitted and received with the transfer clock. f_8 or f_{2n} can be selected as the communication unit 0 transfer clock. f_8 , f_{2n} or the clock generated by channels 0 and 3 can be selected as the communication unit 1 transfer clock.

Table 22.12 lists specifications of clock synchronous serial I/O mode for the communication units 0 and 1. Tables 22.13 and 22.14 list clock settings. Table 22.15 lists register settings. Tables 22.16 to 22.19 list pin settings. Figure 22.29 shows an example of transmit and receive operation.

Table 22.12 Clock Synchronous Serial I/O Mode Specifications (Communication Units 0 and 1)

Item	Specification
Transfer Data Format	Transfer data : 8 bits long
Transfer Clock ⁽¹⁾	See Tables 22.13 and 22.14
Transmit Start Condition	Set registers associated with the waveform generating function, the GiMR register and GiERC register. Then, set as is written below after waiting at least one transfer clock cycle. <ul style="list-style-type: none"> Set the TE bit in the GiCR register to "1" (transmit enable) Set the TI bit in the GiCR register to "0" (data in the GiTB register)
Receive Start Condition	Set registers associated with the waveform generating function, the GiMR register and GiERC register. Then, set as is written below after waiting at least one transfer clock cycle. <ul style="list-style-type: none"> Set the RE bit in the GiCR register to "1" (receive enable) Set the TE bit to "1" (transmit enable) Set the TI bit to "0" (data in the GiTB register)
Interrupt Request	<ul style="list-style-type: none"> While transmitting, one of the following conditions can be selected to set the SIOiTR bit to "1" (interrupt requested) (see Figure 11.14) : <ul style="list-style-type: none"> The IRS bit in the GiMR register is set to "0" (no data in the GiTB register) and data is transferred to the transmit register from the GiTB register The IRS bit is set to "1" (transmission completed) and data transfer from the transmit register is completed While receiving, the following condition can be selected to set SIOiRR bit is set to "1" (data reception is completed): <ul style="list-style-type: none"> Data is transferred from the receive register to the GiRB register
Error Detection	<p>Overrun error⁽²⁾</p> <p>This error occurs, when the next data reception is started and the 8th bit of the next data is received before reading the GiRB register</p>
Selectable Function	<ul style="list-style-type: none"> LSB first or MSB first <ul style="list-style-type: none"> Select either bit 0 or bit 7 to transmit or receive data ISTxDi and ISRxDi I/O polarity inverse <ul style="list-style-type: none"> ISTxDi pin output level and ISRxDi pin input level are inverted

NOTES:

- In clock synchronous serial I/O mode, set the RSHTTE bit in the GiERC register ($i=0, 1$) to "1" (receive shift operation enabled).
- When an overrun error occurs, the GiRB register is indeterminate.

When the OPOL bit in the GiCR register is set to "0" (ISTxD output polarity not inverted), the ISTxDi pin puts in a high-level ("H") signal output after selecting operating mode until transfer starts. When the OPOL bit is set to "1" (ISTxD output polarity inverted), the ISTxDi pin puts in a low-level ("L") signal output.

Table 22.13 Clock Settings (Communication Unit 0)

Transfer Clock	GOMR Register	CCS Register	
	CKDIR Bit	CCS0 Bit	CCS1 Bit
f_8	0	1	1
$f_{2n}^{(1)}$	0	0	1
Input from ISCLK0	1	-	-

NOTES:

- The CNT3 to CNT0 bits in the TCSPR register select no division ($n=0$) or divide-by- $2n$ ($n=1$ to 15).

Table 22.14 Clock Settings (Communication Unit 1)

Transfer Clock ⁽³⁾	G1MR Register	CCS Register	
	CKDIR Bit	CCS2 Bit	CCS3 Bit
$\frac{f_{BT1}}{2(n+2)}$ ⁽¹⁾	0	0	0
f_8	0	1	1
f_{2n} ⁽²⁾	0	0	1
Input from ISCLK1	1	-	-

n : Setting value of the G1PO0 register, 000116 to FFFD16

NOTES:

1. The transfer clock is generated in phase-delayed waveform output mode of the channel 3 waveform generating function.
2. The CNT3 to CNT0 bits in the TCSPR register select no division ($n=0$) or divide-by- $2n$ ($n=1$ to 15).
3. The transfer clock must be f_{BT1} divided by six or more.

Table 22.15 Register Settings in Clock Synchronous Serial I/O Mode (Communication Units 0 and 1)

Register	Bit	Function	
		Communication Unit 1	Communication Unit 0
CCS	CCS1, CCS0	Setting not required when using only communication unit 1	Select transfer clock
	CCS3, CSS2	Select transfer clock	Setting not required when using only communication unit 0
G1BCR0 ⁽²⁾	BCK1, BCK0	Set to "112" (f_1)	
	DIV4 to DIV0	Select divide ratio of count source	
	IT	Set to "0"	
G1BCR1 ⁽²⁾	7 to 0	Set to "0001 00102"	
G1POCR0 ⁽²⁾	7 to 0	Set to "0000 01112"	
G1POCR1 ⁽²⁾	7 to 0	Set to "0000 01112"	
G1POCR3 ⁽²⁾	MOD2 to MOD0	Set to "0102" ⁽¹⁾	
	IVL	Select default output value of ISCLKi ⁽¹⁾	
	RLD	Set to "0"	
	INV	Select whether ISCLKi puts in an inversed signal or not ⁽¹⁾	
G1PO0 ⁽²⁾	15 to 0	Set bit rate $\frac{f_{BT1}}{2 \times (\text{setting value} + 2)} = \text{transfer clock frequency}$	
G1PO3 ⁽²⁾	15 to 0	Set to a value smaller than the G1PO0 register ⁽¹⁾	
G1FS ⁽²⁾	FSC3, FSC1, FSC0	Set to "0" ⁽¹⁾	
G1FE ⁽²⁾	IFE3, IFE1, IFE0	Set to "1" ⁽¹⁾	
GiERC	7 to 0	Set to "0010 00002"	
GiMR	GMD1, GMD0	Set to "012"	
	CKDIR	Select the internal clock or external clock	
	STPS	Set to "0"	
	UFORM	Select either LSB first or MSB first	
	IRS	Select how the transmit interrupt is generated	
GiCR	TI	Transmit buffer empty flag	
	TXEPT	Transmit register empty flag	
	RI	Receive complete flag	
	TE	Set to "1" to enable transmission and reception	
	RE	Set to "1" to enable reception	
	IPOL	Select ISRxDi input polarity (usually set to "0")	
	OPOL	Select ISTxDi output polarity (usually set to "0")	
GiTB	–	Write data to be transmitted	
GiRB	–	Received data and error flag are stored	

$i = 0$ to 1

NOTES:

1. The CKDIR bit in the GiMR register is set to "0" (internal clock).
2. These registers must be set, when f_8 or f_{2n} is selected as transfer clock source notwithstanding.

Table 22.16 Pin Settings in Clock Synchronous Serial I/O Mode (Communication Units 0 and 1)(1)

Port Name	Function	Setting						Register ⁽¹⁾
		PS1 Register	PSL1 Register	PSC Register	PSD1 Register	PD7 Register	IPS Register	
P73	ISTxD1 Output	PS1_3=1	PSL1_3=0	PSC_3=1	-	-	-	G1POCR0
P74	ISCLK1 Input	PS1_4=0	-	-	-	PD7_4=0	IPS1=0	-
	ISCLK1 Output	PS1_4=1	PSL1_4=0	PSC_4=1	-	-	-	G1POCR1
P75	ISRxD1 Input	PS1_5=0	-	-	-	PD7_5=0	IPS1=0	-
p76	ISTxD0 Output	PS1_6=1	PSL1_6=0	PSC_6=0	PSD1_6=0	-	-	-
p77	ISCLK0 Input	PS1_7=0	-	-	-	PD7_7=0	IPS0=0	-
	ISCLK0 Output	PS1_7=1	PSL1_7=0	-	-	-	-	-

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function used).

Table 22.17 Pin Settings (2)

Port Name	Function	Setting		
		PS2 Register	PD8 Register	IPS Register
P80	ISRxD0 input	PS2_0 = 0	PD8_0 = 0	IPS0 = 0

Table 22.18 Pin Settings (3)

Port Name	Function	Setting			Register ⁽¹⁾
		PS5 Register	PD11 Register	IPS Register	
P110	ISTxD1 output	PS5_0 = 1	-	-	G1POCR0
P111	ISCLK1 input	PS5_1 = 0	PD11_1 = 0	IPS1 = 1	-
	ISCLK1 output	PS5_1 = 1	-	-	G1POCR1
P112	ISRxD1 input	PS5_2 = 0	PD11_2 = 0	IPS1 = 1	-

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "1112" (communication function output used).

Table 22.19 Pin Settings (4)

Port Name	Function	Setting		
		PS9 Register	PD15 Register	IPS Register
P150	ISTxD0 output	PS9_0 = 1	-	-
P151	ISCLK0 input	PS9_1 = 0	PD15_2 = 0	IPS0 = 1
	ISCLK0 output	PS9_1 = 1	-	-
P152	ISRxD0 input	-	PD15_2 = 0	IPS0 = 1

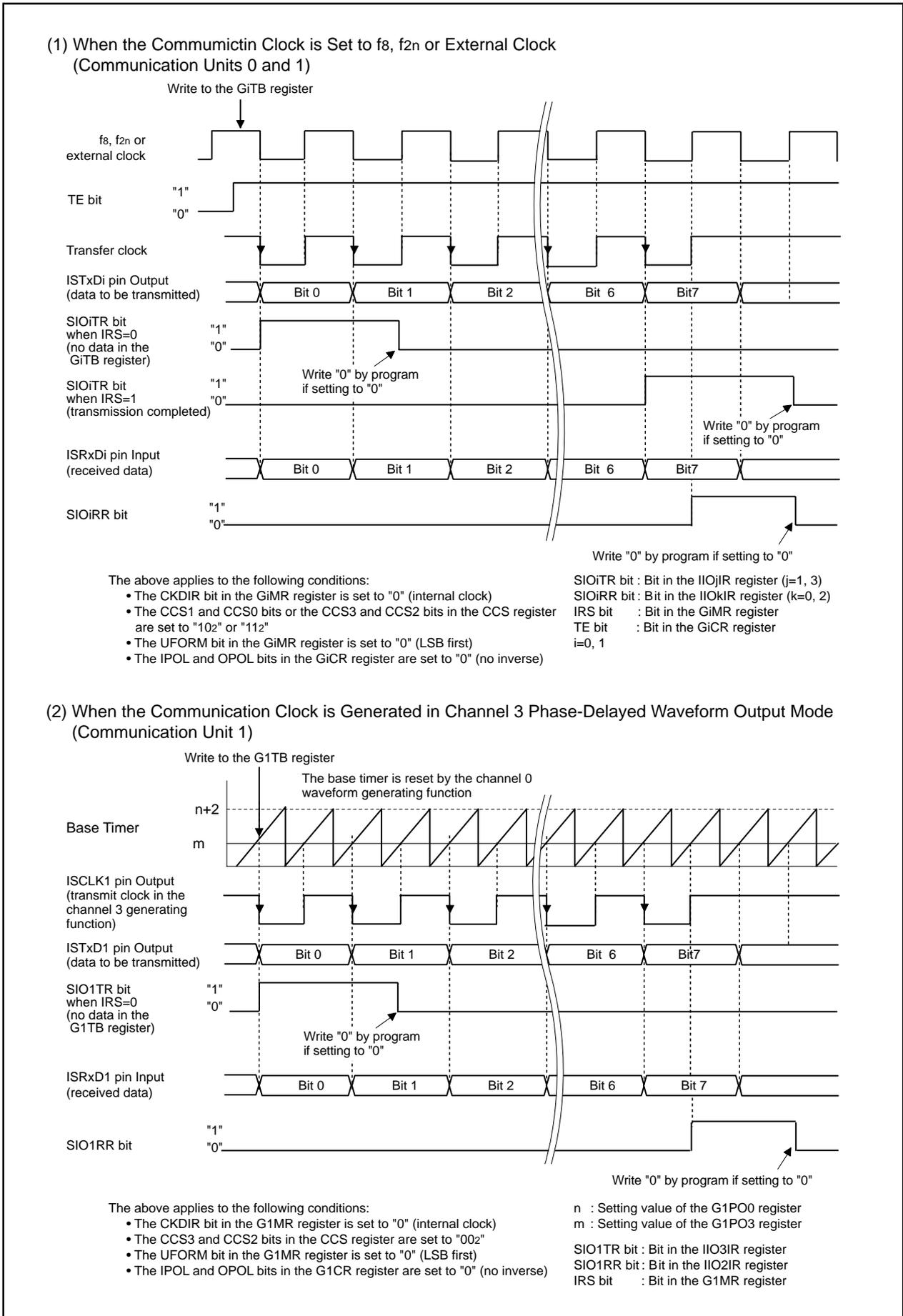


Figure 22.30 Transmit and Receive Operation

22.4.2 Clock Asynchronous Serial I/O (UART) Mode (Communication Unit 1)

In clock asynchronous serial I/O (UART) mode, data is transmitted at a desired bit rate and in a desired transfer data format. Table 22.20 lists specifications of UART mode in the communication unit 1. Table 22.21 lists clock settings. Table 22.22 lists register settings. Tables 22.23 and 22.24 list pin settings. Figure 22.30 shows an example of transmit operation. Figure 22.31 shows an example of receive operation.

Table 22.20 UART Mode Specifications (Communication Unit 1)

Item	Specification
Transfer Data Format	<ul style="list-style-type: none"> • Character Bit (transfer data) : 8 bits long • Start bit : 1 bit long • Parity bit: selected from odd, even, or none • Stop bit : selected length from 1 bit or 2 bits
Transfer Clock ⁽¹⁾	See Table 22.21
Transmit Start Condition	<p>Set registers associated with the waveform generating function, the G1MR register and G1ERC register. Then, set as written below after at least one transfer clock cycle.</p> <ul style="list-style-type: none"> • Set the TE bit in the G1CR register to "1" (transmit enable) • Set the TI bit in the G1CR register to "0" (data written to the G1TB register)
Receive Start Condition	<p>Set registers associated with the waveform generating function, the G1MR register and G1ERC register. Then, set as written below after at least one transfer clock cycle.</p> <ul style="list-style-type: none"> • Set the RE bit in the G1CR register to "1" (receive enable) • Detect the start bit
Interrupt Request	<ul style="list-style-type: none"> • While transmitting, one of the following conditions can be selected to set the SIO1TR bit to "1" (interrupt requested) (See Figure 11.14.) : <ul style="list-style-type: none"> – The IRS bit in the G1MR register is set to "0" (no data in the G1TB register) and data is transferred to the transmit register from the G1TB register. – The IRS bit is set to "1" (transmission completed) and data transfer from the transmit register is completed • While receiving, the following condition can be selected to set the SIO1RR bit is set to "1": <ul style="list-style-type: none"> Data is transferred from the receive register to the G1RB register (data reception is completed)
Error Detection	<ul style="list-style-type: none"> • Overrun error⁽²⁾ <p>This error occurs, when the next data reception is started and the final stop bit of the next data is received before reading the G1RB register</p> • Parity error <ul style="list-style-type: none"> While parity is enabled, this error occurs when the number of "1" in parity and character bits does not match the number of "1" set • Framing error <ul style="list-style-type: none"> This error occurs when the number of the stop bits set is not detected
Selectable Function	<ul style="list-style-type: none"> • Stop bit length <ul style="list-style-type: none"> The length of the stop bit is selected from 1 bit or 2 bits • LSB first or MSB first <ul style="list-style-type: none"> Select either bit 0 or bit 7 to transmit or receive data

NOTES:

1. The transfer clock must be fBT1 divided by six or more.
2. When an overrun error occurs, the G1RB register is indeterminate.

Table 22.21 Clock Settings (Communication Unit 1)

Transfer Clock ⁽³⁾	G1MR Register			CCS Register		
	CKDIR Bit			CCS2 Bit		CCS3 Bit
$\frac{f_{BT1}}{2(n+2)}$ ^(1, 2)	0			0		0

n: Value of the G1PO0 register 0001₁₆ to FFFD₁₆

NOTES:

1. Transmit clock is generated in phase-delayed waveform output mode of the channel 3 waveform generating function.
2. Received clock is generated when phase-delayed waveform mode of the channel 2 waveform generating function and the channel 2 time measurement function is simultaneously performed.
3. The transfer clock must be *f*_{BT1} divided by six or more.

Table 22.22 Register Settings in UART Mode (Communication Unit 1)

Register	Bit	Function
G1BCR0	BCK1, BCK0	Set to "112" (<i>f</i> ₁)
	DIV4 to DIV0	Select divide ratio of count source
	IT	Set to "0"
G1BCR1	7 to 0	Set to "0001 0010 ₂ "
G1POCR0	7 to 0	Set to "0000 0111 ₂ "
G1POCR2	7 to 0	Set to "0000 0110 ₂ "
G1POCR3	7 to 0	Set to "0000 0010 ₂ "
G1TMCR2	7 to 0	Set to "0000 0010 ₂ "
G1PO0	15 to 0	Set bit rate $\frac{f_{BT1}}{2 \times (\text{setting value} + 2)} = \text{transfer clock frequency}$
G1PO3	15 to 0	Set to a value smaller than the G1PO0 register
G1FS	FSC3 to FSC0	Set to "0100 ₂ "
G1FE	IFE3 to IFE0	Set to "1101 ₂ "
G1MR	GMD1, GMD0	Set to "00 ₂ "
	CKDIR	Set to "0"
	STPS	Select length of stop bit
	PRY, PRYE	Select either parity enabled or disabled and either odd parity or even parity
	UFORM	Select either the LSB first or MSB first
	IRS	Select how the receive interrupt is generated
G1CR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Set to "1" to enable transmission and reception
	RE	Set to "1" to enable reception
	IPOL	Set to "1"
OPOL	Set to "1"	
G1TB	7 to 0	Write data to be transmitted
G1RB	15 to 0	Received data and error flag are stored
CCS	CCS3, CCS2	Set to "00 ₂ "

Table 22.23 Pin Settings in UART Mode

Port Name	Function	Setting					Register ⁽¹⁾
		PS1 Register	PSL1 Register	PSC Register	PD7 Register	IPS Register	
P7 ₃	ISTxD1 output	PS1_3 = 1	PSL1_3 = 0	PSC_3 = 1	-	-	G1POCR0
P7 ₅	ISRxD1 input	PS1_5 = 0	-	-	PD7_5 = 0	IPS1 = 0	-

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "111₂" (communication function output used).

Table 22.24 Pin Settings (Continued)

Port Name	Function	Setting			Register ⁽¹⁾
		PS5 Register	PD11 Register	IPS Register	
P110	ISTxD1 output	PS5_0 = 1	-	-	G1POCR0
P112	ISRxD1 input	PS5_2 = 0	PD11_2 = 0	IPS1 = 1	-

NOTES:

1. Set the MOD2 to MOD0 bits in the corresponding register to "1112" (output of the communication function used).

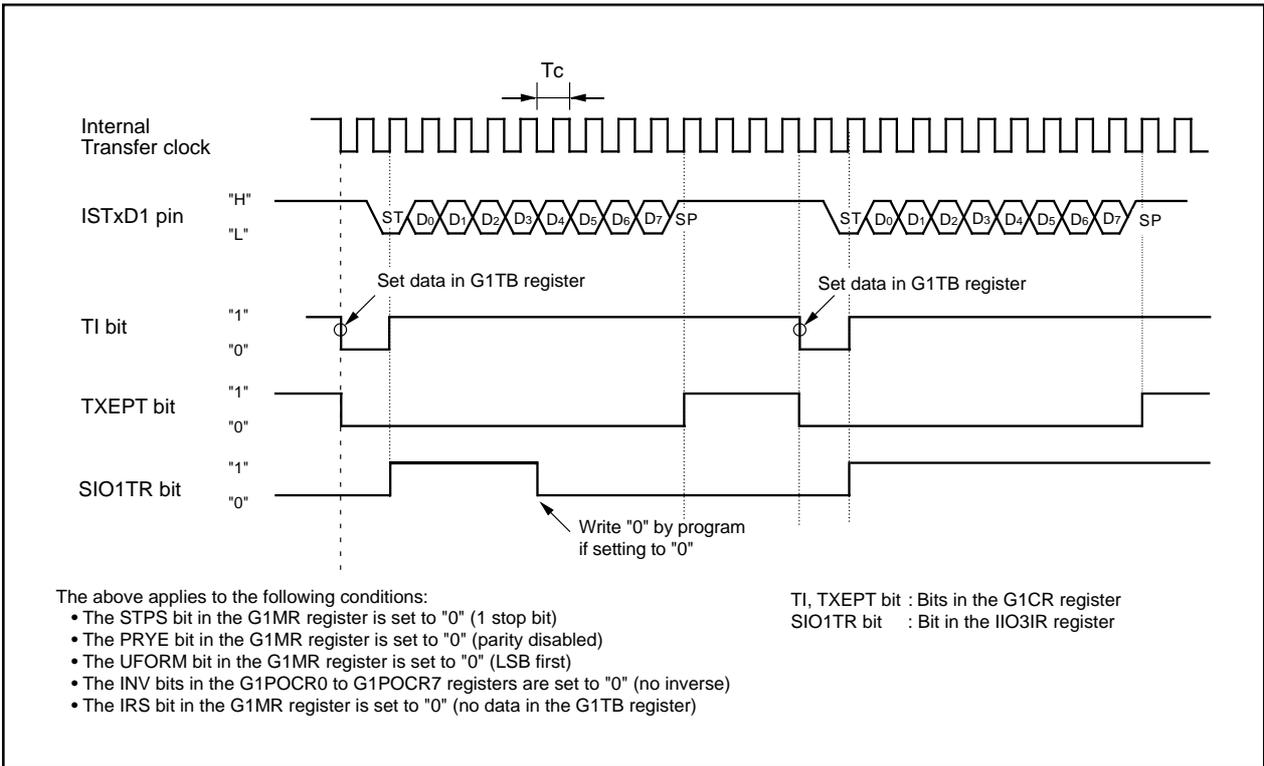


Figure 22.31 Transmit Operation

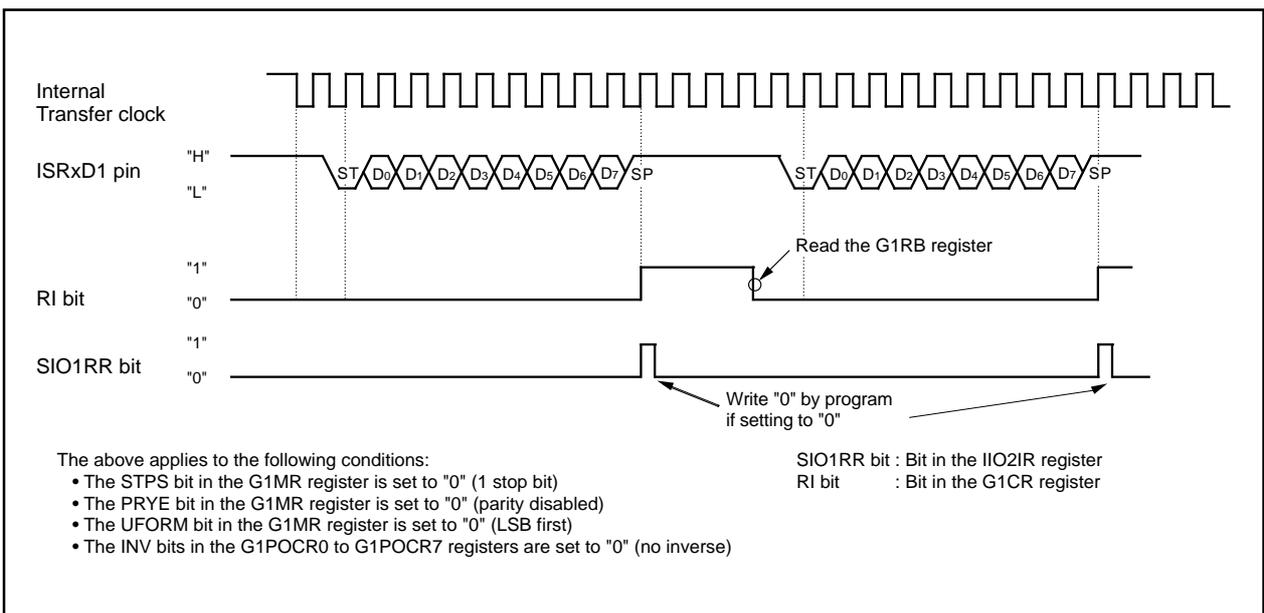


Figure 22.32 Receive Operation

22.4.3 HDLC Data Processing Mode (Communication Units 0 and 1)

In HDLC data processing mode, bit stuffing, flag detection, abort detection and CRC calculation are available for HDLC control. f_1 , f_8 or f_{2n} can become the communication unit 0 transfer clock. f_1 , f_8 , f_{2n} or clock, generated in the channel 0 or 1, can become the communication unit 1 transfer clock. No pins are used. To convert data, data to be transmitted is written to the GiTB register ($i=0,1$) and the data conversion result is restored after data conversion. If any data are in the GiTO register after data conversion, the conversion is terminated. If no data is in the GiTO register, bit stuffing processing is executed regardless of there being no data in the transmit output buffer. A CRC value is calculated every time one bit is converted. If no data is in the GiRI register, received data conversion is terminated.

Table 22.25 list specifications of the HDLC data processing mode. Tables 22.26 and 22.27 list clock settings. Table 22.28 lists register settings.

Table 22.25 HDLC Processing Mode Specifications (Communication Units 0 and 1)

Item	Specification
Input Data Format	8-bit data fixed, bit alignment is optional
Output Data Format	8-bit data fixed
Transfer Clock	See Tables 22.26 and 22.27
I/O Method	<ul style="list-style-type: none"> During transmit data processing, value set in the GiTB register is converted in HDLC data processing mode and transferred to the GiTO register. During received data processing, value set in the GiRI register is converted in HDLC data processing mode and transferred to the GiRB register. The value in the GiRI register is also transferred to the GiTB register (received data register).
Bit Stuffing	During transmit data processing, "0" following five continuous "1" is inserted. During received data processing, "0" following five continuous "1" is deleted.
Flag Detection	Write the flag data "7E16" to the GiCMPj register ($j=0$ to 3) to use the special communication interrupt (the SRTiR bit in the IIO4IR register)
Abort Detection	Write the masked data "0116" to the GiMSKj register
CRC	<p>The CRC1 and CRC0 bits are set to "112" ($X^{16}+X^{12}+X^5+1$). The CRCV bit is set to "1" (set to "FFFF16").</p> <ul style="list-style-type: none"> During transmit data processing, CRC calculation result is stored into the GiTCRC register. The TCRCE bit in the GiETC register is set to "1" (transmit CRC used). The CRC calculation result is reset when the TE bit in the GiCR register is set to "0" (transmit disabled). During received data processing, CRC calculation result is stored into the GiRCRC register. The RCRCE bit in the GiERC register is set to "1" (receive CRC used). The CRC calculation result is reset by comparing the flag data "7E16" and matching the result with the value in the GiCMP3 register. The ACRC bit in the GiEMR register is set to "1" (CRC reset).
Data Processing Start Condition	<p>The following conditions are required to start transmit data processing:</p> <ul style="list-style-type: none"> The TE bit in the GiCR register is set to "1" (transmit enable) Data is written to the GiTB register <p>The following conditions are required to start receive data processing:</p> <ul style="list-style-type: none"> The RE bit in the GiCR register is set to "1" (receive enable) Data is written to the GiRI register

Table 22.25 HDLC Processing Mode Specifications (Continued)

Item	Specification
Interrupt Request ⁽¹⁾	<p>During transmit data processing,</p> <ul style="list-style-type: none"> • One of the following conditions can be selected to set the GiTOR bit in the interrupt request register to "1" (interrupt request) (see Figure 11.14). <ul style="list-style-type: none"> – When the IRS bit in the GiMR register is set to "0" (no data in the GiTB register) and data is transferred from the GiTB register to the transmit register (transmit start). – When the IRS bit is set to "1" (transmission completed) and data transfer from the transmit register to the GiTO register is completed. • When data, which is already converted to HDLC data, is transferred from the receive register of the GiTO register to the transmit buffer, the GiTOR bit is set to "1" <p>During received data processing,</p> <ul style="list-style-type: none"> • When data is transferred from the GiRI register to the GiRB register (reception completed), the GiRIR bit is set to "1" (See Figure 11.14). • When received data is transferred from the receive buffer of the GiRI register to the receive register, the GiRIR bit is set to "1". • When the GiTB register is compared to the GiCMPj register (j=0 to 3), the SRTiR bit is set to "1".

NOTES:

1. See **Figure 11.14** for details on the GiTOR bit, GiRIR bit and SRTiR bit.

Table 22.26 Clock Settings (Communication Unit 0)

Transfer Clock ⁽¹⁾	CCS Register	
	CCS0 Bit	CCS1 Bit
f1	1	0
f8	1	1
f _{2n} ⁽²⁾	0	1

NOTES:

1. The transfer clock for reception is generated when the RSHTTE bit in the G0ERC register is set to "1" (receive shift operation enabled).
2. The CNT3 to CNT0 bits in the TCSPR register select no division ($n=0$) or divide-by- $2n$ ($n=1$ to 15).

Table 22.27 Clock Settings (Communication Unit 1)

Transfer Clock ⁽¹⁾	CCS Register	
	CCS2 Bit	CCS3 Bit
$\frac{f_{BT1}}{2 \times (n+2)}$ ⁽²⁾	0	0
f1	1	0
f8	1	1
f _{2n} ⁽³⁾	0	1

n : Setting value of the G1PO0 register, 0001₁₆ to FFFD₁₆

NOTES:

1. The transfer clock for reception is generated when the RSHTTE bit in the G1ERC register is set to "1" (receive shift operation enabled).
2. The transfer clock is generated in single-phase waveform output mode of the channel 1.
3. The CNT3 to CNT0 bits in the TCSPR register select no division ($n=0$) or divide-by- $2n$ ($n=1$ to 15).

Table 22.28 Register Settings in HDLC Processing Mode (Communication Units 0 and 1)

Register	Bit	Function
G1BCR0	BCK1, BCK0	Select count source
	DIV4 to DIV0	Select divide ratio of count source
	IT	Select the base timer interrupt
G1BCR1 ⁽¹⁾	7 to 0	Set to "0001 00102"
G1POCR0 ⁽¹⁾	7 to 0	Set to "0000 00002"
G1POCR1 ⁽¹⁾	7 to 0	Set to "0000 00002"
G1PO0 ⁽¹⁾	15 to 0	Set bit rate
G1PO1 ⁽¹⁾	15 to 0	Set the timing of the rising edge of the transfer clock. Timing of the falling edge ("H" width of the transfer clock) is fixed. Setting value of the G1PO1 register ≤ Setting value of the G1PO0 register
G1FS ⁽¹⁾	FSC1, FSC0	Set to "002"
G1FE ⁽¹⁾	IFE1, IFE0	Set to "112"
GiMR	GMD1, GMD0	Set to "112"
	CKDIR	Set to "0"
	UFORM	Set to "0"
	IRS	Select how the transmit interrupt is generated
GiEMR	7 to 0	Set to "1111 01102"
GiCR	TI	Transmit buffer empty flag
	TXEPT	Transmit register empty flag
	RI	Receive complete flag
	TE	Transmit enable bit
	RE	Receive enable bit
GiETC	SOF	Set to "0"
	TCRCE	Select whether transmit CRC is used or not
	ABTE	Set to "0"
	TBSF1, TBSF0	Transmit bit stuffing
GiERC	CMP2E to CMP0E	Select whether received data is compared or not
	CMP3E	Set to "1"
	RCRCE	Select whether receive CRC is used or not
	RSHTE	Set to "1" to use it in the receiver
	RBSF1, RBSF0	Receive bit stuffing
GiIRF	BSERR, ABT	Set to "0"
	IRF3 to IRF0	Select how an interrupt is generated
GiCMP0, GiCMP1	7 to 0	Write "FE16" to abort processing
GiCMP2	7 to 0	Data to be compared
GiCMP3	7 to 0	Write "7E16"
GiMSK0, GiMSK1	7 to 0	Write "0116" to abort processing
GiTCRC	15 to 0	Transmit CRC calculation result can be read
GiRCRC	15 to 0	Receive CRC calculation result can be read
GiTO	7 to 0	Data, which is output from a transmit data generation circuit, can be read
GiRI	7 to 0	Set data input to a receive data generation circuit
GiRB	7 to 0	Received data is stored
GiTB	7 to 0	For transmission: write data to be transmitted For reception : received data for comparison is stored
CCS	CCS1, CCS0	Select the HDLC processing clock
	CCS3, CCS2	Select the HDLC processing clock

i=0, 1

NOTES:

- These register settings are required when the CCS3 and CCS2 bit in the CCS register are set to "002" (clock output from channel j (j=1,2,3)).

23. CAN Module

The CAN (Controller Area Network) module included in the M32C/84 group (M32C/84, M32C/84T) is a Full CAN module, compatible with CAN Specification 2.0 Part B. One channel, CAN0, can be used. Table 23.1 lists specifications of the CAN module.

Table 23.1 CAN Module Specifications

Item	Specification
Protocol	CAN Specification 2.0 Part B
Message Slots	16 slots
Polarity	Dominant: "L" Recessive: "H"
Acceptance Filter	Global mask: 1 (for message slots 0 to 13) Local mask: 2 (for message slots 14 and 15 respectively)
Baud Rate	$\text{Baud rate} = \frac{1}{Tq \text{ clock cycle} \times Tq \text{ per bit}} \quad \text{--- Max. 1 Mbps}$ $Tq \text{ clock cycle} = \frac{BRP + 1}{\text{CAN clock}}$ $Tq \text{ per bit} = SS + PTS + PBS1 + PBS2$ <p>Tq: Time quantum BRP: Setting value of the COBRP register, 1-255 SS: Synchronization Segment; 1 Tq PTS: Propagation Time Segment; 1 to 8 Tq PBS1: Phase Buffer Segment 1; 2 to 8 Tq PBS2: Phase Buffer Segment 2; 2 to 8 Tq</p>
Remote Frame Automatic Answering Function	Message slot that receives the remote frame transmits the data frame automatically
Time Stamp Function	Time stamp function with a 16-bit counter. Count source can be selected from the CAN bus bit clock divided by 1, 2, 3 or 4 $\text{CAN bus bit clock} = \frac{1}{\text{CAN bit time}}$
BasicCAN Mode	BasicCAN function can be used with the CAN0 message slots 14 and 15
Transmit Abort Function	Transmit request is aborted
Loopback Function	Frame transmitted by the CAN module is received by the same CAN module
Forcible Error Active Transition Function	The CAN module is forced into an error active state by resetting an error counter
Single-Shot Transmit Function	The CAN module does not transmit data again even if arbitration lost or transmission error causes a transmission failure
Self-Test Function	The CAN module communicates internally and diagnoses its CAN module state

NOTES:

1. Use an oscillator with maximum 1.58% oscillator tolerance.

Figure 23.1 shows a block diagram of the CAN module. Figure 23.2 shows CAN0 message slot (the message slot) j ($j = 0$ to 15) and CAN0 message slot buffer. Table 23.2 lists pin settings of the CAN module. The message slot cannot be accessed directly from the CPU. Allocate the message slot j to be used to the message slot buffer 0 or 1. The message slot j is accessed via the message slot buffer address. The COSBS register selects the message slot j to be allocated. Figure 23.2 shows the 16-byte message slot buffer and message slot.

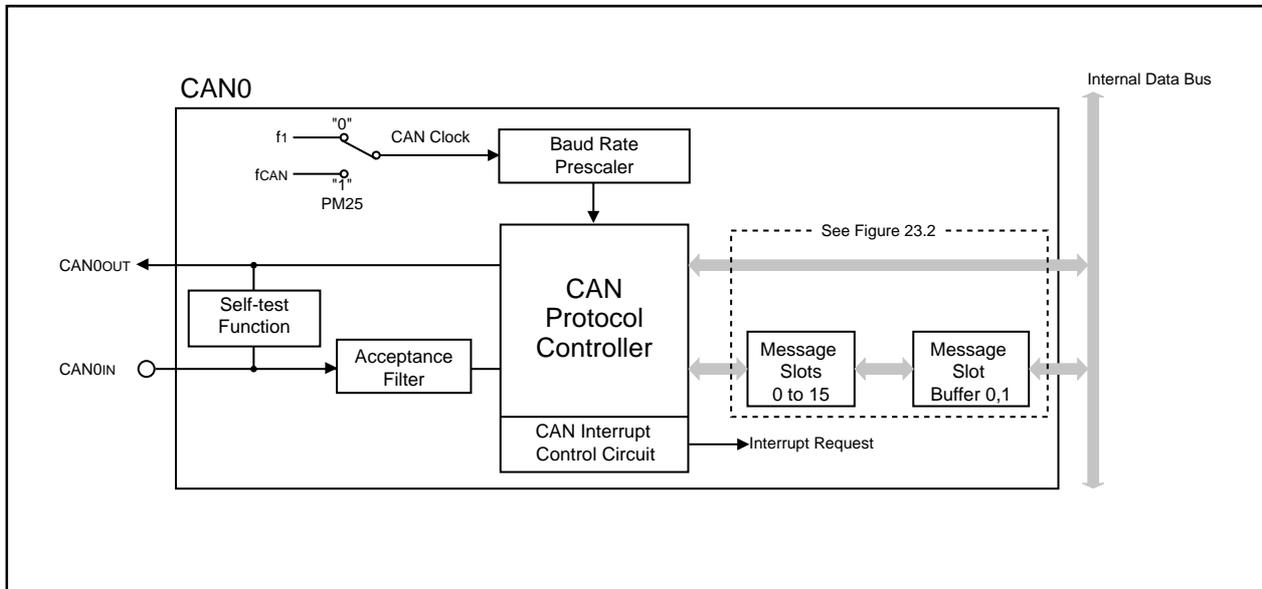


Figure 23.1 CAN Module Block Diagram

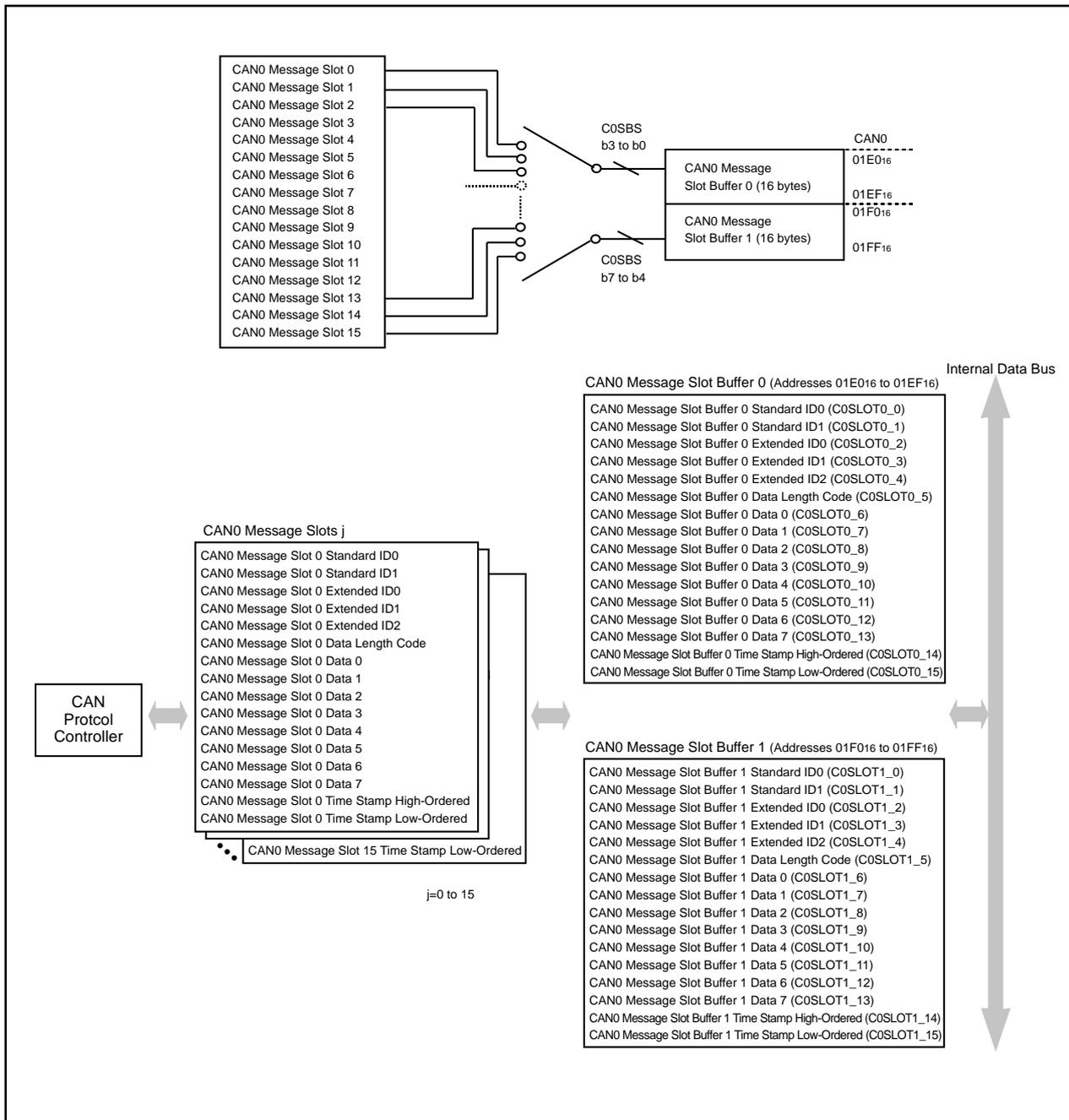


Figure 23.2 CAN0 Message Slot and CAN0 Message Slot Buffer

Table 23.2 Pin Settings

Port	Function	Bit and Setting				
		IPS Register	PS1, PS2 Registers	PSL1, PSL2, Registers	PSC, PSC2 Registers	PD7, PD8 Registers
P7 ₆	CAN0 _{OUT}	–	PS1_6=1	PSL1_6=0	PSC_6=1	–
P7 ₇	CAN0 _{IN}	IPS3=0	PS1_7=0	–	–	PD7_7=0
P8 ₂	CAN0 _{OUT}	–	PS2_2=1	PSL2_2=1	PSC2_2=0	–
P8 ₃	CAN0 _{IN}	IPS3=0	–	–	–	PD8_3=0

23.1 CAN-Associated Registers

Figures 23.3 to 23.18, and Figures 23.20 to 23.33 show registers associated with CAN. To access the CAN-associated registers, set the CM21 bit in the CM2 register to "0" (main clock or PLL clock as CPU clock) and the MCD4 to MCD0 bits in the MCD register to "100102" (no division mode). Or, set the PM24 bit in the PM2 register to "1" (main clock direct mode) and the PM25 bit in the PM2 register to "1" (CAN clock). Two wait states are added into the bus cycle.

Refer to **7. Processor Mode** and **9. Clock Generation Circuit**.

23.1.1 CAN0 Control Register 0 (C0CTRL0 Register)

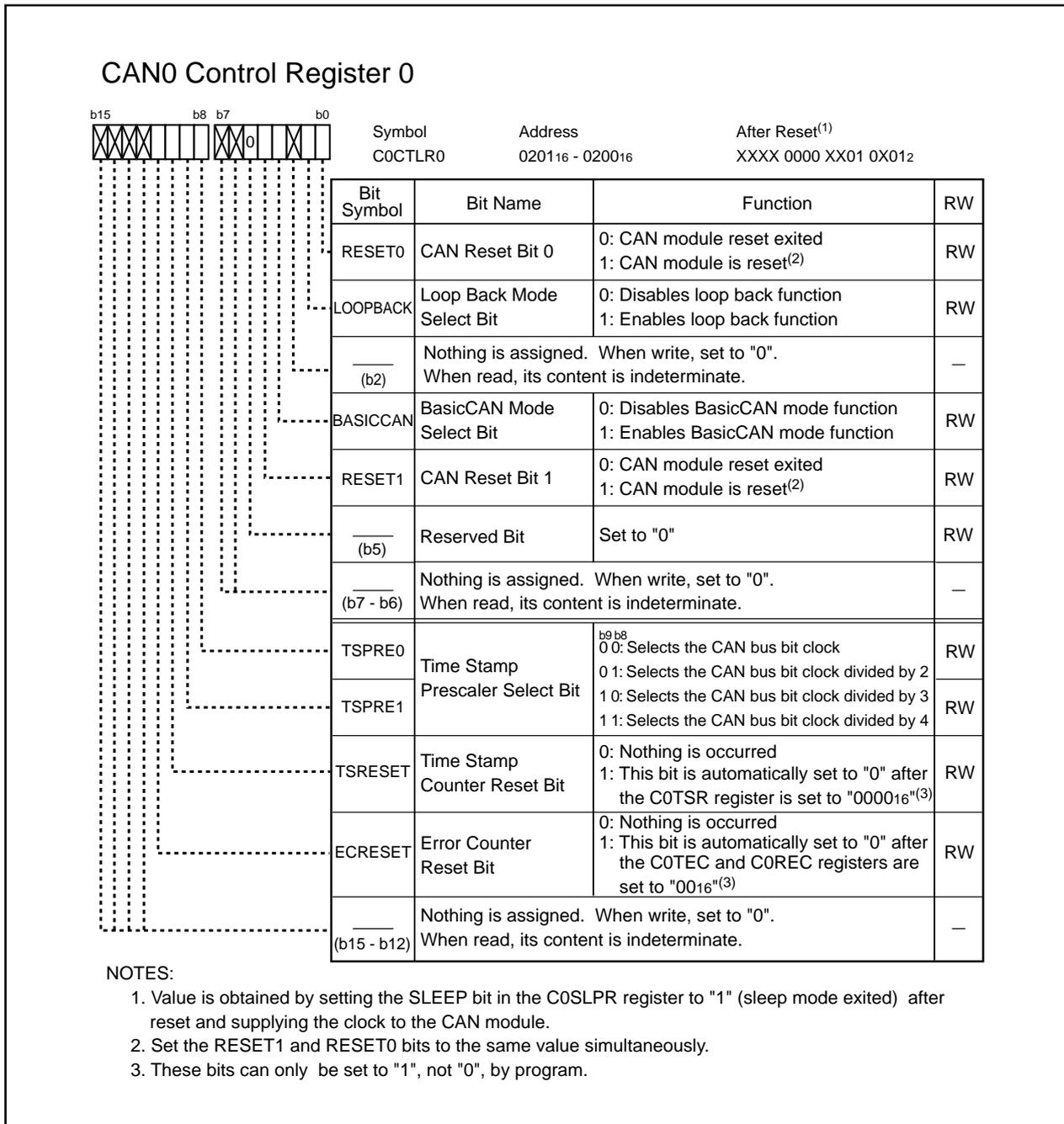


Figure 23.3 C0CTRL0 and C1CTRL0 Registers

23.1.1.1 RESET1 and RESET0 Bits

When both RESET1 and RESET0 bits are set to "1" (CAN module reset), the CAN module is immediately reset regardless of ongoing CAN communication.

After the RESET1 and RESET0 bits are set to "1" and the CAN module reset is completed, the C0TSR register is set to "0000₁₆". The C0TEC and C0REC registers are set to "00₁₆" and the STATE_ERRPAS and STATE_BUSOFF bits in the C0STR register are set to "0" as well.

When both RESET1 and RESET0 bit settings are changed "1" to "0", the C0TSR register starts counting. CAN communication is available after 11 continuous recessive bits are detected.

NOTES:

1. Set the same value in both RESET1 and RESET0 bits simultaneously.
2. Confirm that the STATE_RESET bit in the C0STR register is set to "1" (CAN module reset completed) after setting the RESET1 and RESET0 bits to "1".
3. The CANOUT pin puts out a high-level ("H") signal as soon as the RESET1 and RESET0 bits are set to "1". CAN bus error may occur when the RESET1 and RESET0 bits are set to "1" while the CAN frame is transmitting.
4. For CAN communication, set the PS1, PS2, PSL1, PSL2, PSC, PSC2, IPS, PD7 and PD8 registers when the STATE_RESET bit is set to "1" (CAN module reset completed).

23.1.1.2 LOOPBACK Bit

When the LOOPBACK bit is set to "1" (loopback function enabled) and the receive message slot has a matched ID and frame format with a transmitted frame, the transmitted frame is stored to the receive message slot.

NOTES:

1. No ACK for the transmitted frame is returned.
2. Change the LOOPBACK bit setting only when the STATE_RESET bit is set to "1" (CAN module reset completed).

23.1.1.3 BASICCAN Bit

When the BASICCAN bit is set to "1", the message slots 14 and 15 enter BasicCAN mode.

In BasicCAN mode, the message slots 14 and 15 are used as dual-structured buffers. The message slots 14 and 15 alternately store a received frame having matched ID detected by acceptance filtering. ID in the message slot 14 and the C0LMAR0 to C0LMAR4 registers are used for acceptance filtering when the message slot 14 is active (the next received frame is to be stored in the message slot 14). ID in the message slot 15 and the C0LMBR0 to C0LMBR4 registers are used when the message slot 15 is active. Both data frame and remote frame can be received.

Use the following procedure to enter BasicCAN mode.

- (1) Set the BASICCAN bit to "1".
- (2) Set the same value into IDs in the message slots 14 and 15.
- (3) Set the same value in the C0LMAR0 to C0LMAR4 registers and C0LMBR0 to C0LMBR4 registers.
- (4) Set the IDE14 and IDE15 bits in the C0IDR register to select a frame format (standard or extended) for the message slots 14 and 15. (Set to the same format.)
- (5) Set the C0MCTL14 and C0MCTL15 registers in the message slots 14 and 15 to receive data frame.

NOTES:

1. Change the BASICCAN bit setting only when the STATE_RESET bit is set to "1" (CAN module reset completed).
2. The message slot 14 is the first slot to become active after the RESET1 and RESET0 bits are set to "0".
3. The message slots 0 to 13 are not affected by entering BasicCAN mode.

23.1.1.4 TSPRE1 and TSPRE0 Bits

The TSPRE1 and TSPRE0 bits determine which count source is used for the time stamp counter.

NOTES:

1. Change the TSPRE1 and TSPRE0 bit settings only when the STATE_RESET bit is set to "1" (CAN module reset completed).

23.1.1.5 TSRESET Bit

When the TSRESET bit is set to "1", the C0TSR register is set to "0000₁₆". The TSRESET bit is automatically set to "0" after the C0TSR register is set to "0000₁₆".

23.1.1.6 ECRESET Bit

When the ECRESET bit is set to "1", the C0TEC and C0REC registers are set to "00₁₆". The CAN module forcibly goes into an error active state.

The ECRESET bit is automatically set to "0" after the CAN module enters an error active state.

NOTES:

1. In an error active state, the CAN module is ready to communicate when 11 continuous recessive bits are detected on the CAN bus.
2. The CAN0OUT pin provides an "H" signal output as soon as the ECRESET bit is set to "1". The CAN bus error may occur when setting the ECRESET bit to "1" during CAN frame transmission.

23.1.2 CAN0 Control Register 1 (C0CTLR1 Register)

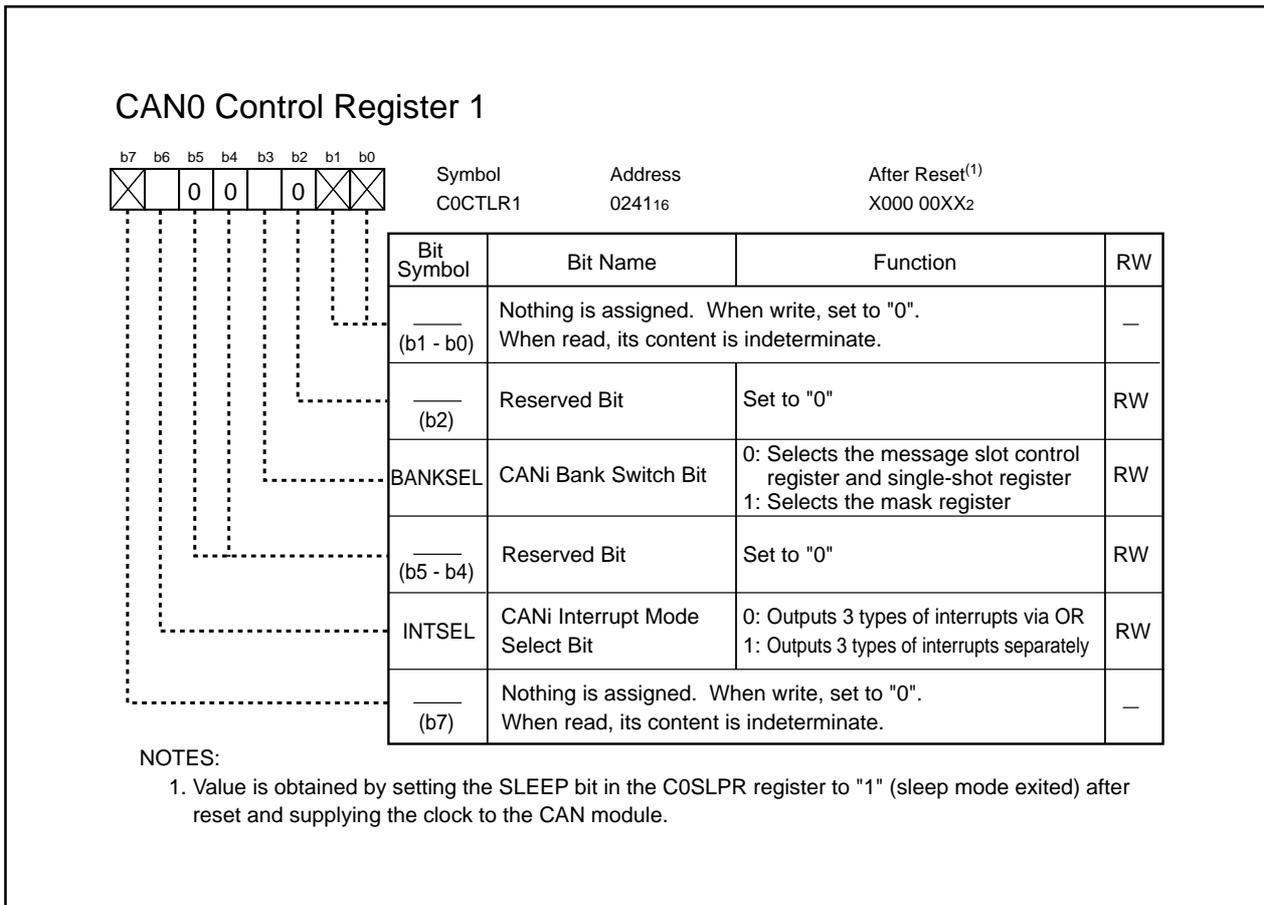


Figure 23.4 C0CTLR1 Register

23.1.2.1 BANKSEL Bit

The BANKSEL bit in the C0CTLR1 register selects the registers allocated to addresses 0220₁₆ to 023F₁₆.

The C0SSCTLR register, C0SSSTR register and the C0MCTL0 to C0MCTL15 registers can be accessed by setting the BANKSEL bit to "0". The C0GMR0 to C0GMR4 registers, C0LMAR0 to C0LMAR4 registers and C0LMBR0 to C0LMBR4 registers can be accessed by setting the BANKSEL bit to "1".

23.1.2.2 INTSEL Bit

The INTSEL bit determines whether the three types of interrupt outputs (CAN0 transmit interrupt, CAN0 receive interrupt and CAN0 error interrupt) are provided via OR or is done separately.

Refer to **23.4 CAN Interrupts** for details.

NOTES:

- Change the INTSEL bit setting when the STATE_RESET bit is set to "1" (CAN module reset completed).

23.1.3 CAN0 Sleep Control Register (C0SLPR Register)

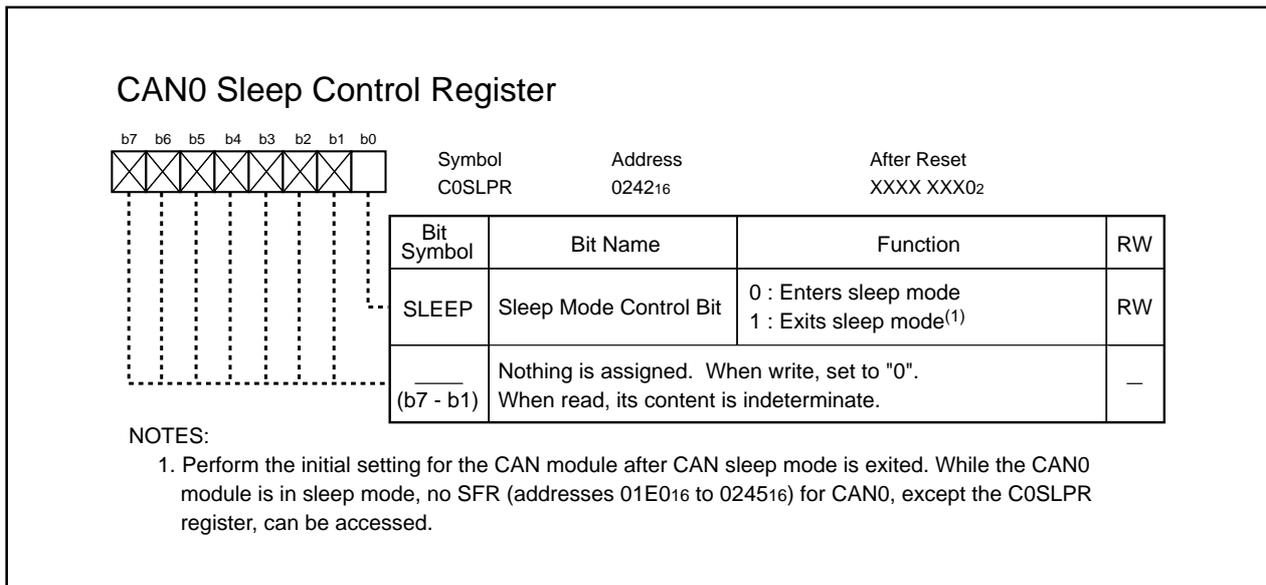


Figure 23.5 C0SLPR Register

23.1.3.1 SLEEP Bit

When the SLEEP bit is set to "0", the clock supplied to the CAN module stops running and the CAN module enters sleep mode.

When the SLEEP bit is set to "1", the clock supplied to the CAN module starts running and the CAN module exits sleep mode.

NOTES:

- Enter sleep mode after the STATE_RESET bit in the CiSTR register is set to "1" (CAN module reset completed).

23.1.4 CAN0 Status Register (C0STR Register)

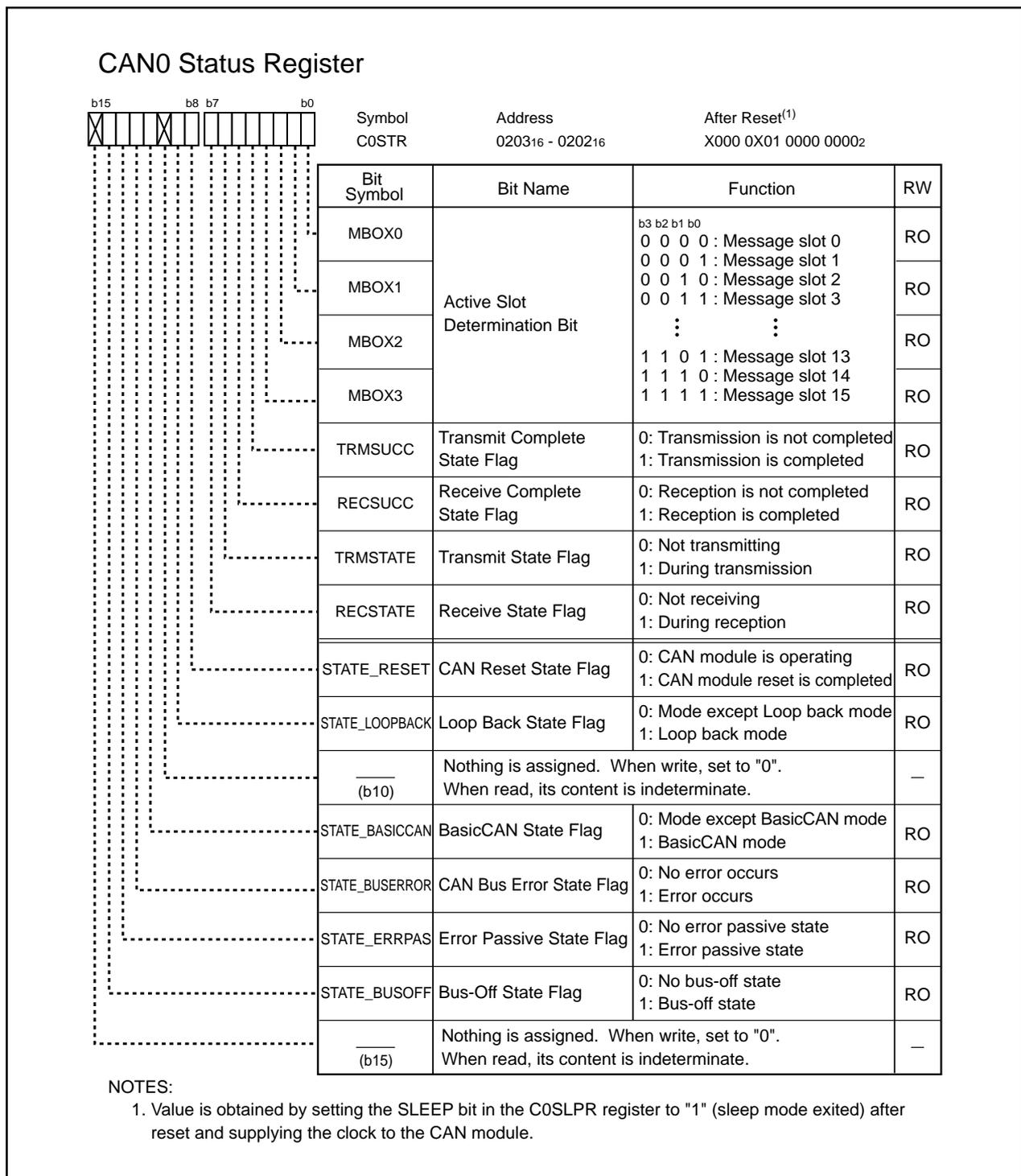


Figure 23.6 C0STR Register

23.1.4.1 MBOX3 to MBOX0 Bits

The MBOX3 to MBOX0 bits store relevant slot numbers when the CAN module has completed transmitting data or storing received data.

23.1.4.2 TRMSUCC Bit

The TRMSUCC bit is set to "1" when the CAN module has transmitted data successfully.
The TRMSUCC bit is set to "0" when the CAN module has received data successfully.

23.1.4.3 RECSUCC Bit

The RECSUCC bit is set to "1" when the CAN module has received data successfully. (Whether received message has been stored in the message slot or not is irrelevant.) If the received message is transmitted in loopback mode, the TRMSUCC bit is set to "1" and the RECSUCC bit is set to "0". The RECSUCC bit is set to "0" when the CAN module has transmitted data successfully.

23.1.4.4 TRMSTATE Bit

The TRMSTATE bit is set to "1" when the CAN module is performing as a transmit node. The TRMSTATE bit is set to "0" when the CAN module is in a bus-idle state or starts performing as a receive node.

23.1.4.5 RECSTATE Bit

The RECSTATE bit is set to "1" when the CAN module is performing as a receive node. The RECSTATE bit is set to "0" when the CAN module is in a bus-idle state or starts performing as a transmit node.

23.1.4.6 STATE_RESET Bit

After both RESET1 and RESET0 bits are set to "1" (CAN module reset), the STATE_RESET bit is set to "1" as soon as the CAN module is reset. The STATE_RESET bit is set to "0" when the RESET1 and RESET0 bits are set to "0".

23.1.4.7 STATE_LOOPBACK Bit

The STATE_LOOPBACK bit is set to "1" when the CAN module is in loopback mode. The STATE_LOOPBACK bit is set to "1" when the LOOPBACK bit in the C0CTRL0 register is set to "1" (loop back function enabled). The STATE_LOOPBACK bit is set to "0" when the LOOPBACK bit is set to "0" (loop back function disabled).

23.1.4.8 STATE_BASICCAN Bit

The STATE_BASICCAN bit is set to "1" when the CAN module is in BasicCAN mode. Refer to **23.1.1.3 BASICCAN bit** for BasicCAN mode. The STATE_BASICCAN bit is set to "0" when the BASICCAN bit is set to "0" (BasicCAN mode function disabled). The STATE_BASICCAN bit is set to "1" when the BASICCAN bit is set to "1" (BasicCAN mode function enabled), the REMACTIVE bits in the COMCTL14 and COMCTL15 registers in the message slots 14 and 15 are set to "0" (data frame received).

23.1.4.9 STATE_BUSERROR Bit

The STATE_BUSERROR bit is set to "1" when a CAN communication error is detected. The STATE_BUSERROR bit is set to "0" when the CAN module has transmitted or received data successfully. Whether a received message has been stored into the message slot or not is irrelevant.

NOTES:

1. When the STATE_BUSERROR bit is set to "1", the STATE_BUSERROR bit remains unchanged even if both RESET1 and RESET0 bits are set to "1" (CAN module reset).

23.1.4.10 STATE_ERRPAS Bit

The STATE_ERRPAS bit is set to "1" when the value of the C0TEC or C0REC register exceeds 127 and the CAN module is placed in an error-passive state.

The STATE_ERRPAS bit is set to "0" when the CAN module in an error-passive state is placed in another error state.

The STATE_ERRPAS bit is set to "0" when both RESET1 and RESET0 bits are set to "1" (CAN module is reset).

23.1.4.11 STATE_BUSOFF Bit

The STATE_BUSOFF bit is set to "1" when the value of the C0TEC register exceeds 255 and the CAN module is placed in a bus-off state.

The STATE_BUSOFF bit is set to "0" when the CAN module in a bus-off state is placed in an error-active state.

The STATE_BUSOFF bit is set to "0" when both RESET1 and RESET0 bits are set to "1" (CAN module reset).

23.1.5 CAN0 Extended ID Register (C0IDR Register)

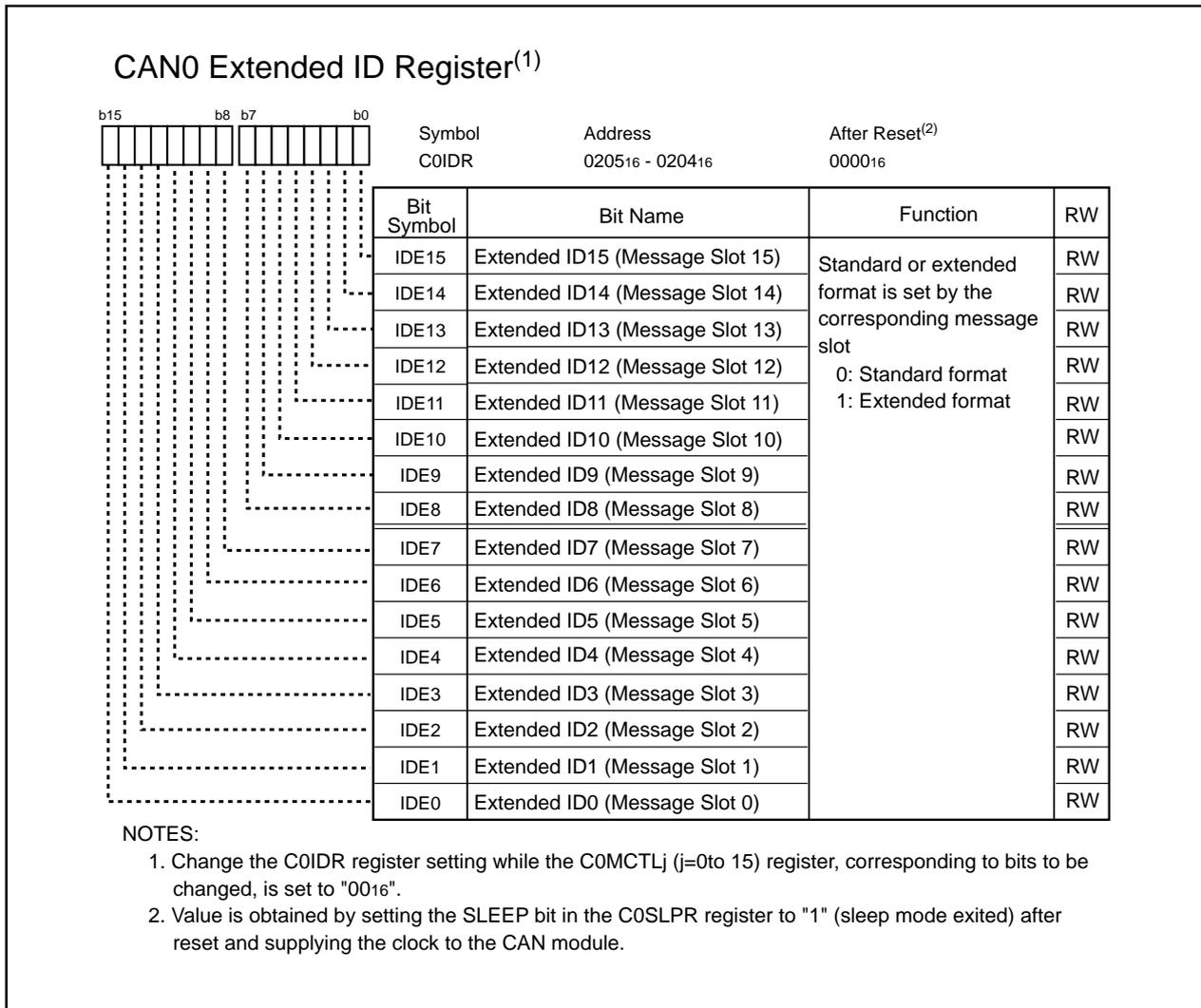


Figure 23.7 C0IDR Register

Bits in the C0IDR register determine the frame format in the message slot corresponding to each bit. The standard format is selected when the bit is set to "0". The extended format is selected when the bit is set to "1".

23.1.6 CAN0 Configuration Register (C0CONR Register)

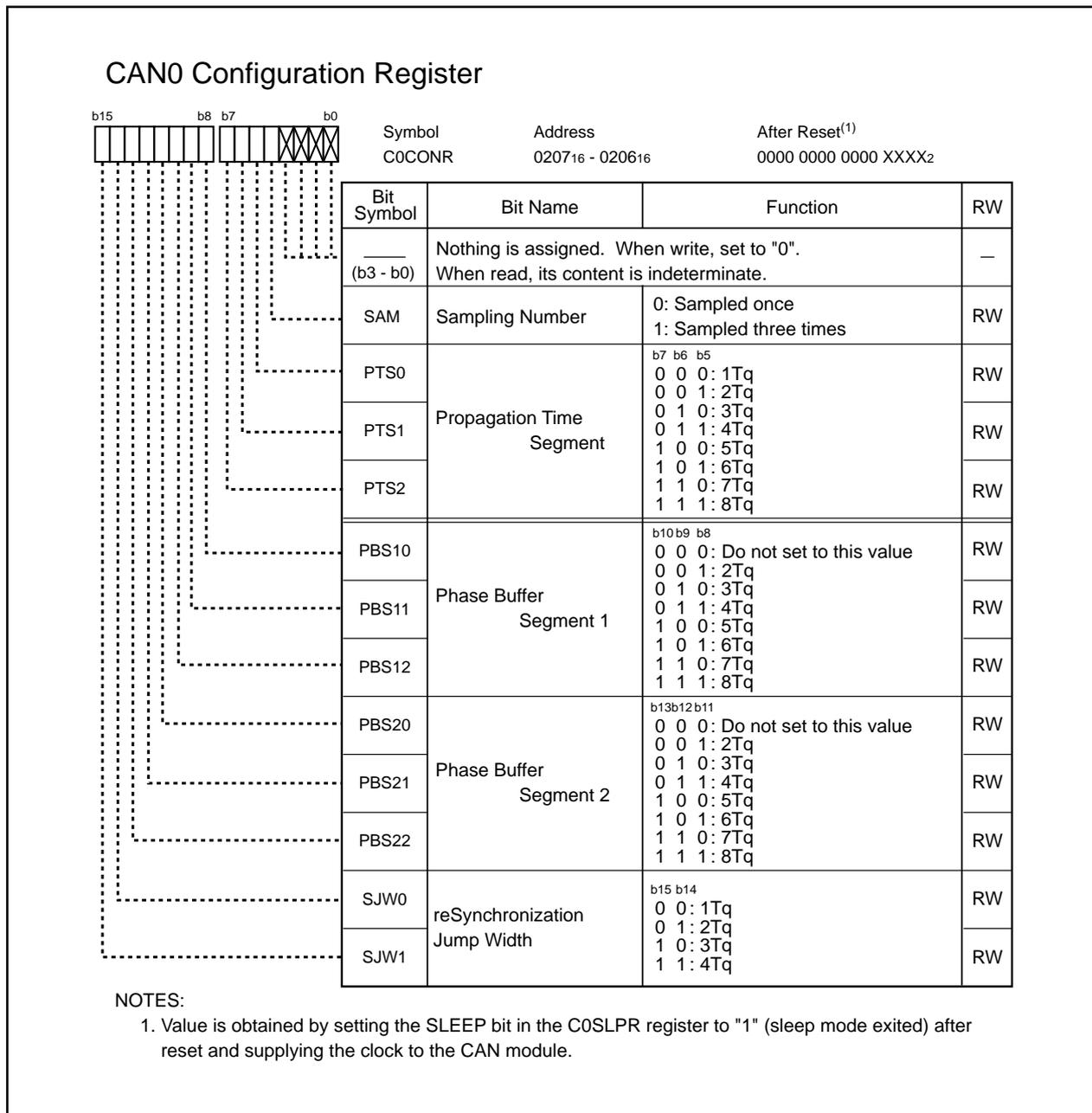


Figure 23.8 C0CONR Register

23.1.6.1 SAM Bit

The SAM bit determines the number of sample points to be taken per bit.

When the SAM bit is set to "0", only one sample is taken per bit at the end of the Phase Buffer Segment 1 (PBS1) to determine the value of the bit.

When the SAM bit is set to "1", three samples per bit are taken; one time quantum and two time quanta before the end of PBS1, and at the end of PBS1. The sample result value which is detected more than twice becomes the value of the bit sampled.

23.1.6.2 PTS2 to PTS0 Bits

The PTS2 to PTS0 bits determine PTS width.

23.1.6.3 PBS12 to PBS10 Bits

The PBS12 to PBS10 bits determine PBS1 width. Set the PBS12 to 10 bits to "0012" or more.

23.1.6.4 PBS22 to PBS20 Bits

The PBS22 to PBS20 bits determine PBS2 width. Set the PBS22 to PBS20 bits to "0012" or more.

23.1.6.5 SJW1 and SJW0 Bits

The SJW1 and SJW0 bits determine SJW width. Set the SJW1 and SJW0 bits to values less than or equal to the PBS22 to PBS20 bits and the PBS12 to PBS10 bits.

Table 23.3 Bit Timing when CPU Clock = 30 MHz

Baud Rate	BRP	Tq Clock Cycles (ns)	Tq Per Bit	PTS+PBS1	PBS2	Sample Point
1Mbps	1	66.7	15	12	2	87%
	1	66.7	15	11	3	80%
	1	66.7	15	10	4	73%
	2	100	10	7	2	80%
	2	100	10	6	3	70%
	2	100	10	5	4	60%
500Kbps	2	100	20	16	3	85%
	2	100	20	15	4	80%
	2	100	20	14	5	75%
	3	133.3	15	12	2	87%
	3	133.3	15	11	3	80%
	3	133.3	15	10	4	73%
	4	166.7	12	9	2	83%
	4	166.7	12	8	3	75%
	4	166.7	12	7	4	67%
	5	200	10	7	2	80%
	5	200	10	6	3	70%
	5	200	10	5	4	60%

23.1.7 CAN0 Baud Rate Prescaler (C0BRP Register)

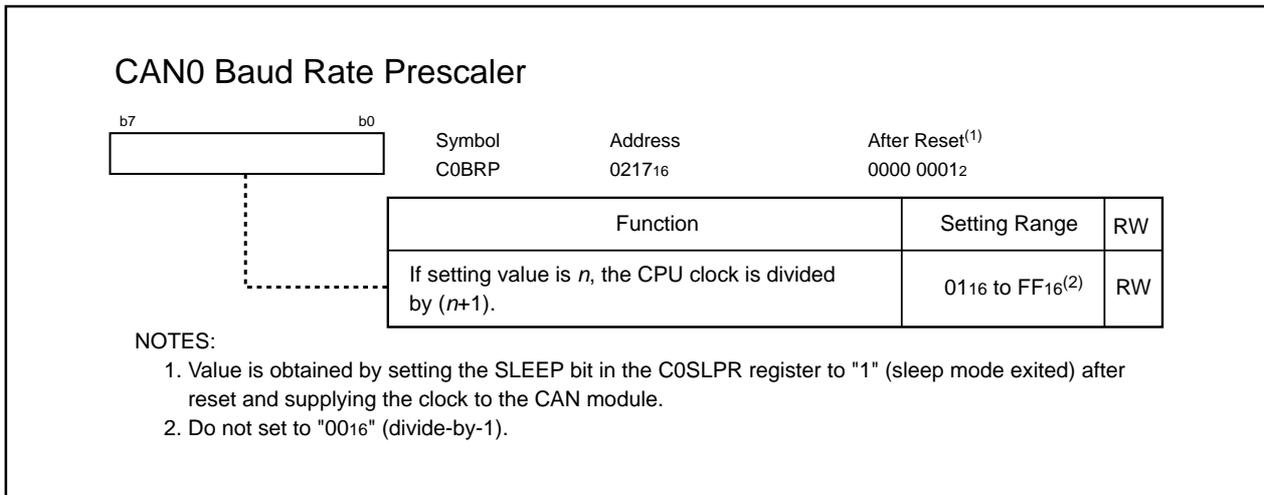


Figure 23.9 C0BRP Register

The C0BRP register determines the Tq clock cycle of the CAN bit time. The baud rate is obtained from Tq clock cycle x Tq per bit.

$$\text{Tq clock cycle} = (\text{BRP} + 1) / \text{CAN clock}$$

$$\text{Baud rate} = \frac{1}{\text{Tq clock cycle} \times \text{Tq per bit}}$$

$$\text{Tq per bit} = \text{SS} + \text{PTS} + \text{PBS1} + \text{PBS2}$$

Tq: Time quantum

SS: Synchronization Segment; 1 Tq

PBS1: Phase Buffer Segment 1; 2 to 8 Tq

BRP: Setting value of the C0BPR register; 1-255

PTS: Propagation Time Segment; 1 to 8 Tq

PBS2: Phase Buffer Segment 2; 2 to 8 Tq

23.1.8 CAN0 Time Stamp Register (C0TSR Register)

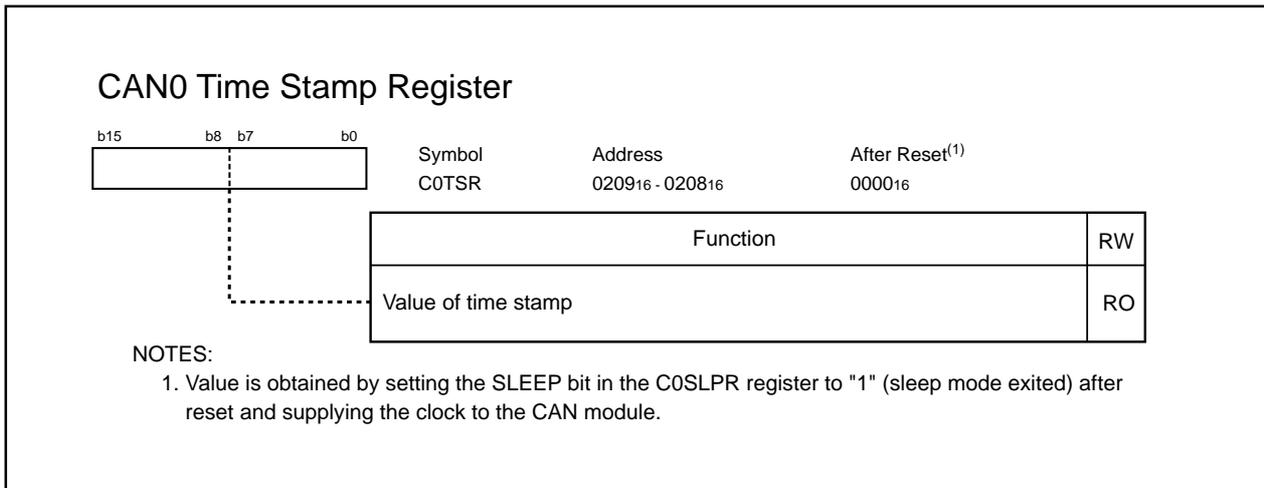


Figure 23.10 C0TSR Register

The C0TSR register is a 16-bit counter. The TSPRE1 and TSPRE0 bits in the C0CTRL0 register select the CAN bus bit clock divided by 1, 2, 3 or 4 as the count source for the C0TSR register. When data transmission or reception is completed, the value of the C0TSR register is automatically stored into the message slot.

In loopback mode, when either data frame receive message slot or remote frame receive message slot is available to store the message, the value of the C0TSR register is also stored into the message slot when data reception is completed. The value of the C0TSR register is not stored when data transmission is completed.

The C0TSR register starts a counter increment when the RESET1 and RESET0 bits in the C0CTRL0 register are set to "0".

The C0TSR register is set to "0000₁₆":

- at the next count timing after the C0TSR register is set to "FFFF₁₆";
- when the RESET1 and RESET0 bits are set to "1" (CAN module reset) by program; or
- when the TSRESET bit is set to "1" (C0TSR register reset) by program.

$$\text{CAN bus bit clock} = \frac{1}{\text{CAN bit time}}$$

23.1.9 CAN0 Transmit Error Count Register (C0TEC Register)

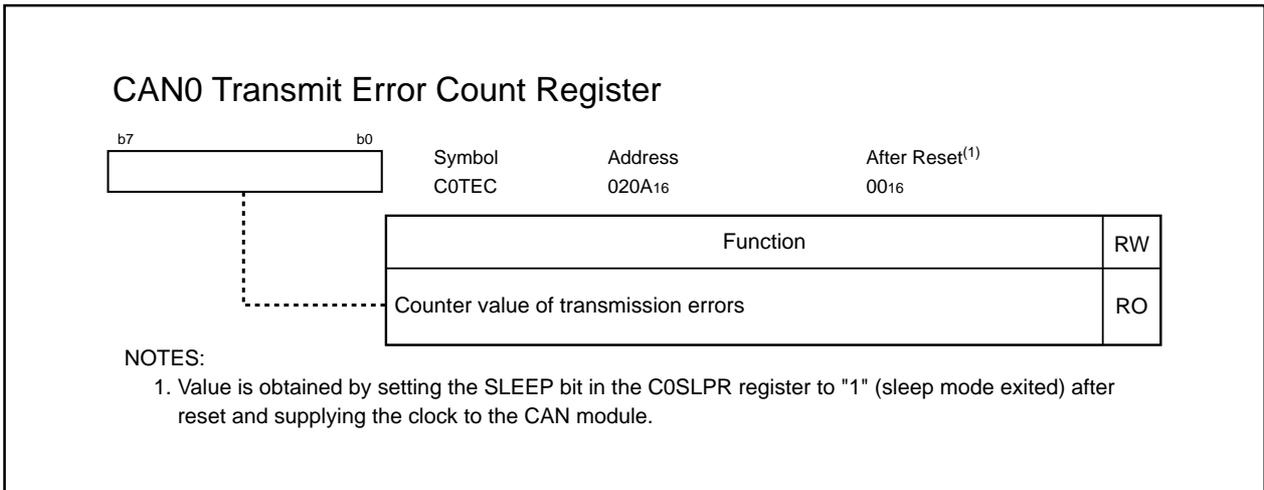


Figure 23.11 C0TEC Register

In an error active or an error passive state, the counting value of a transmission error is stored into the C0TEC register. The counter is decremented when the CAN module has transmitted data successfully or is incremented when an transmit error occurs.

In a bus-off state, an indeterminate value is stored into the C0TEC register. The C0TEC register is set to "00₁₆" when the CAN module is placed in an error active state again.

23.1.10 CAN0 Receive Error Count Register (C0REC Register)

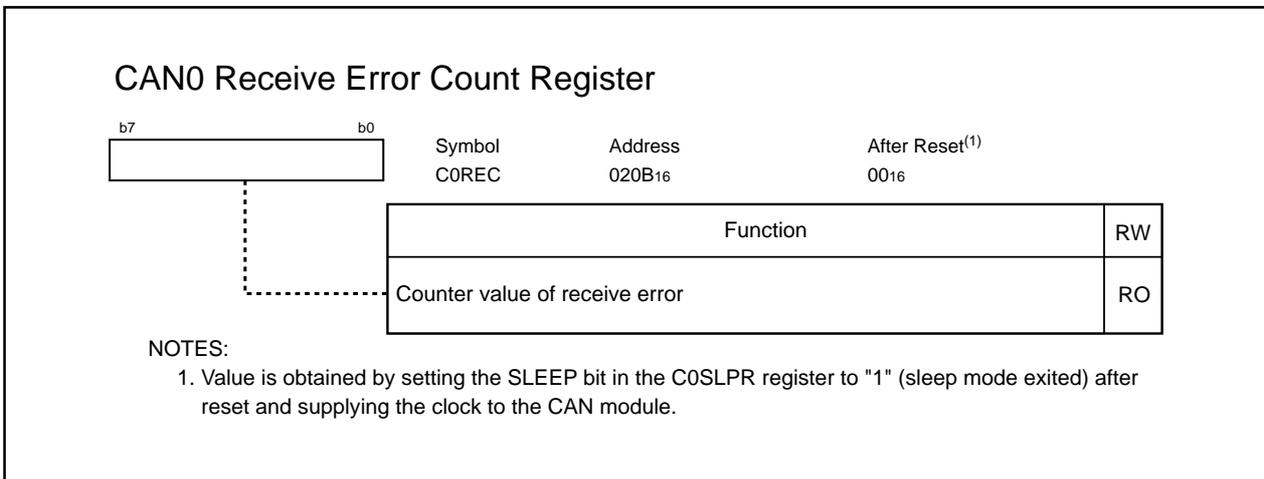


Figure 23.12 C0REC Register

In an error active or an error passive state, a counting value of the reception error is stored into the C0REC register. The counter is decremented when the CAN module has received data successfully or it is incremented when a receive error occurs.

The C0REC register is set to 127 when the C0REC register is 128 (error passive state) or more and the CAN module has received successfully.

In a bus-off state, an indeterminate value is stored into the C0REC register. The C0REC register is set to "00₁₆" when the CAN module is placed in an error active state again.

23.1.11 CAN0 Slot Interrupt Status Register (C0SISTR Register)

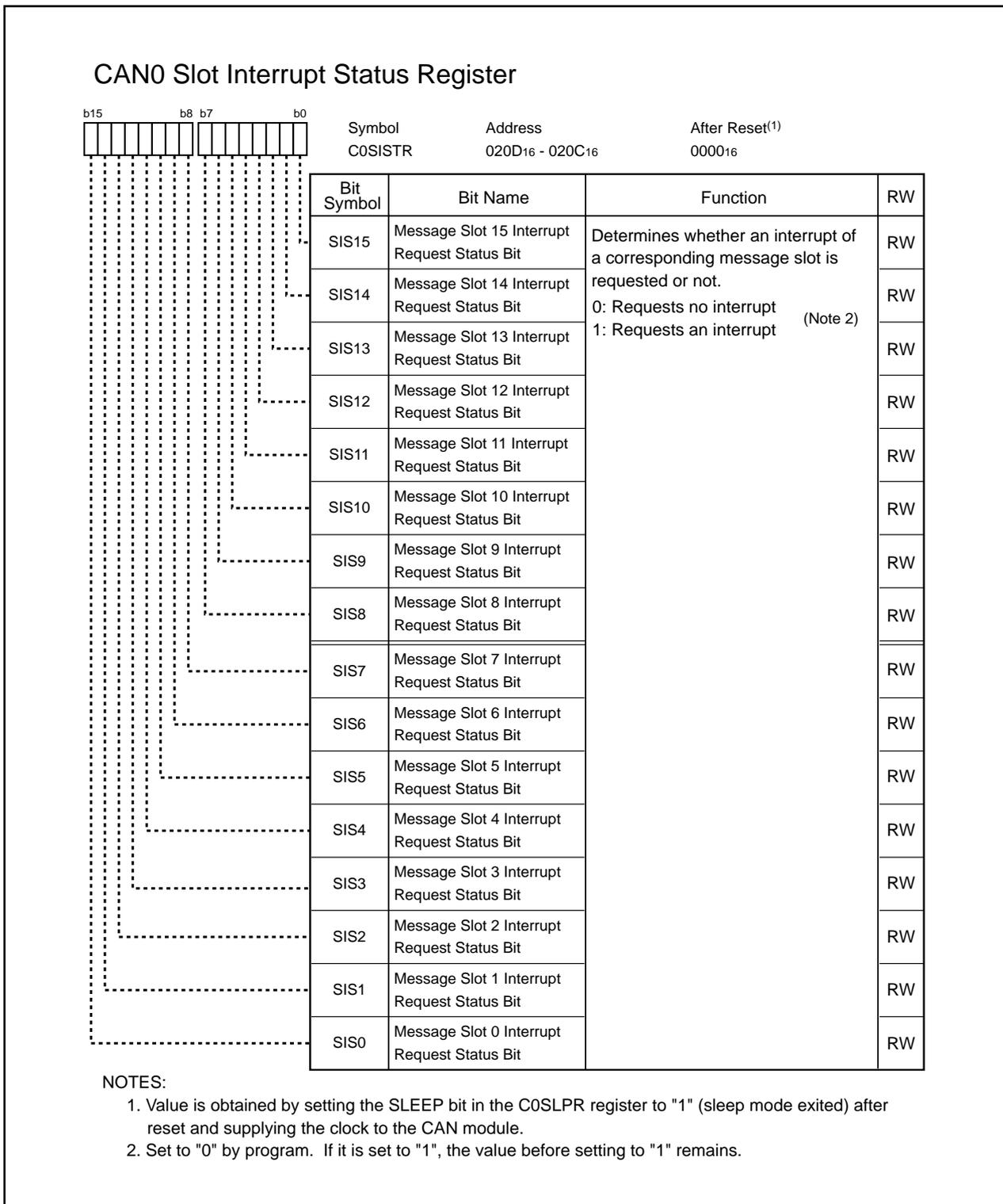


Figure 23.13 C0SISTR Register

When using the CAN interrupt, the C0SISTR register indicates which message slot is requesting an interrupt. The SISj bits (j=0 to 15) are not automatically set to "0" (no interrupt requested) when an interrupt is acknowledged. Set the SISj bits to "0" by program.

Use the MOV instruction, instead of the bit clear instruction, to set the SISj bits to "0". The SISj bits, which are not being changed to "0", must be set to "1".

For example: To set the SIS0 bit to "0"

Assembly language: `mov.w #07FFFh, C0SISTR`

C language: `c0sistr = 0x7FFF;`

Refer to **23.4 CAN Interrupt** for details.

23.1.11.1 Message Slot for Transmission

The SISj bit is set to "1" (interrupt requested) when the C0TSR register is stored into the message slot j after data transmission is completed.

23.1.11.2 Message Slot for Reception

The SISj bit is set to "1" (interrupt requested) when the received message is stored in the message slot j after data reception is completed.

NOTES:

- 1.If the automatic answering function is enabled in the remote frame receive message slot, the SISj bit is set to "1" after the remote frame is received and the data frame is transmitted.
- 2.In the remote frame transmit message slot, the SISj bit is set to "1" after the remote frame is transmitted and the data frame is received.
- 3.The SISj bit is set to "1" if the SISj bit is set to "1" by an interrupt request and "0" by program simultaneously.

23.1.12 CAN0 Slot Interrupt Mask Register (C0SIMKR Register)

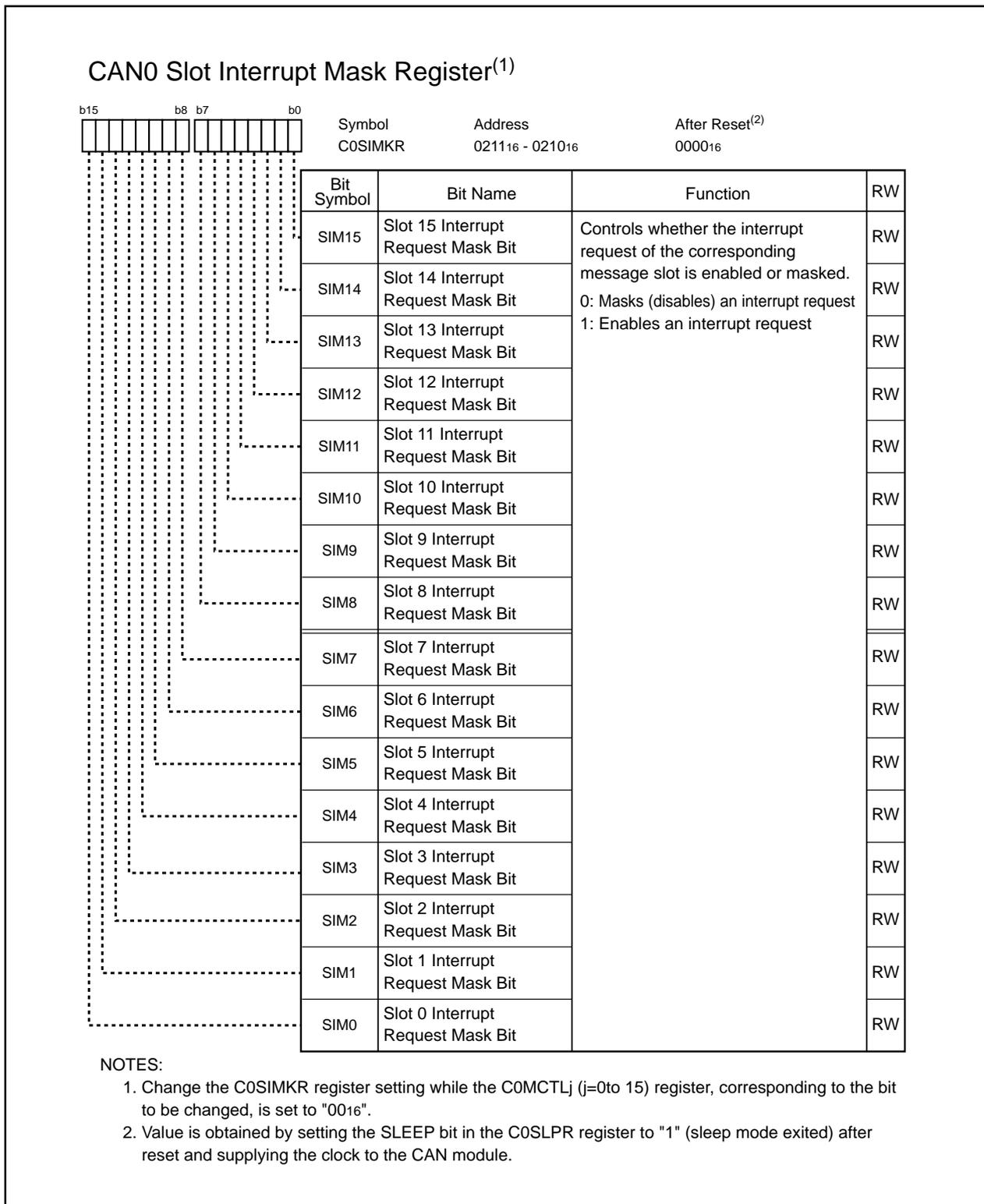


Figure 23.14 C0SIMKR Register

The C0SIMKR register determines whether an interrupt request, generated by a data transmission or reception in the corresponding message slot is enabled or disabled. When the SIM_j bit (j=0 to 15) is set to "1" (no interrupt requested), an interrupt request generated by a data transmission or reception in the corresponding message slot is enabled. Refer to **23.4 CAN Interrupt** for details.

23.1.13 CAN0 Error Interrupt Mask Register (C0EIMKR Register)

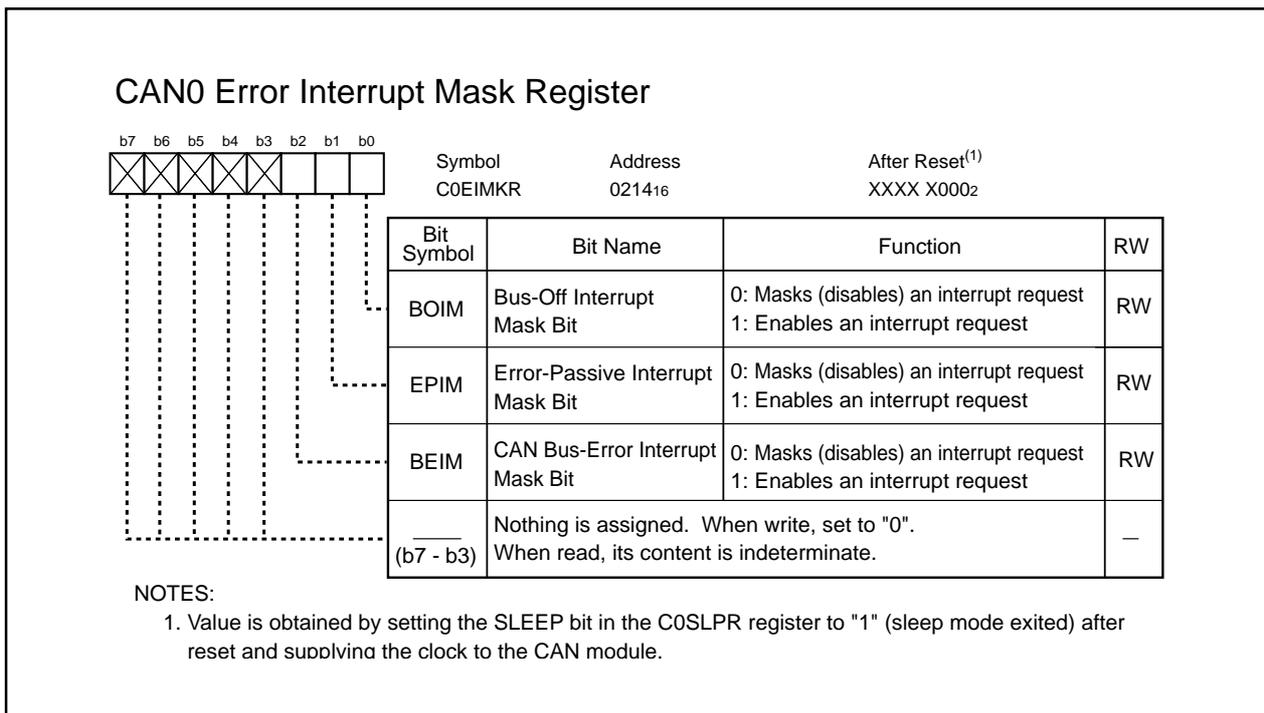


Figure 23.15 C0EIMKR Register

Refer to **23.4 CAN Interrupt** for details.

23.1.13.1 BOIM Bit

The BOIM bit determines whether an interrupt request is enabled or disabled when the CAN module is placed in a bus-off state. When the BOIM bit is set to "1", the bus-off interrupt request is enabled.

23.1.13.2 EPIM Bit

The EPIM bit determines whether an interrupt request is enabled or disabled when the CAN module is placed in an error passive state. When the EPIM bit is set to "1", the error passive interrupt request is enabled.

23.1.13.3 BEIM Bit

The BEIM bit determines whether an interrupt request is enabled or disabled when a CAN bus error occurs. When the BEIM bit is set to "1", the CAN bus error interrupt request is enabled.

23.1.14 CAN0 Error Interrupt Status Register (C0EISTR Register)

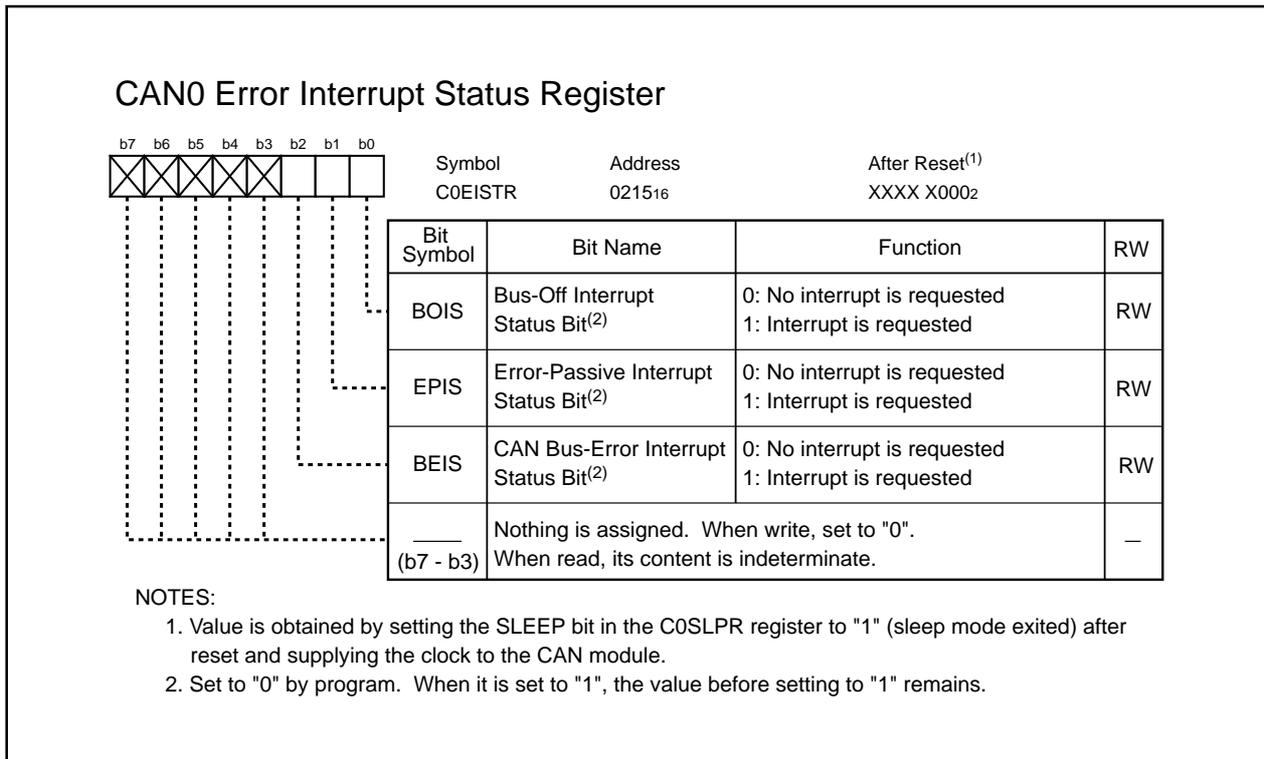


Figure 23.16 C0EISTR Register

When using the CAN interrupt, the C0EISTR register indicates the source of the generated error interrupt. The BOIS, EPIS and BEIS bits are not automatically set to "0" (no interrupt requested) even if an interrupt is acknowledged. Set these bits to "0" by program.

Use the MOV instruction, instead of the bit clear instruction, to set each bit in the C0EISTR register to "0". Bits not being changed to "0" must be set to "1".

For example: To set the BOIS bit to "0"

Assembly language: `mov.b#006h, C0EISTR`

C language: `c0eistr = 0x06;`

Refer to **23.4 CAN Interrupt** for details.

23.1.14.1 BOIS Bit

The BOIS bit is set to "1" when the CAN module is placed in a bus-off state.

23.1.14.2 EPIS Bit

The EPIS bit is set to "1" when the CAN module is placed in an error passive state.

23.1.14.3 BEIS Bit

The BEIS bit is set to "1" when a CAN bus error is detected.

23.1.15 CAN0 Error Factor Register (C0EFR Register)

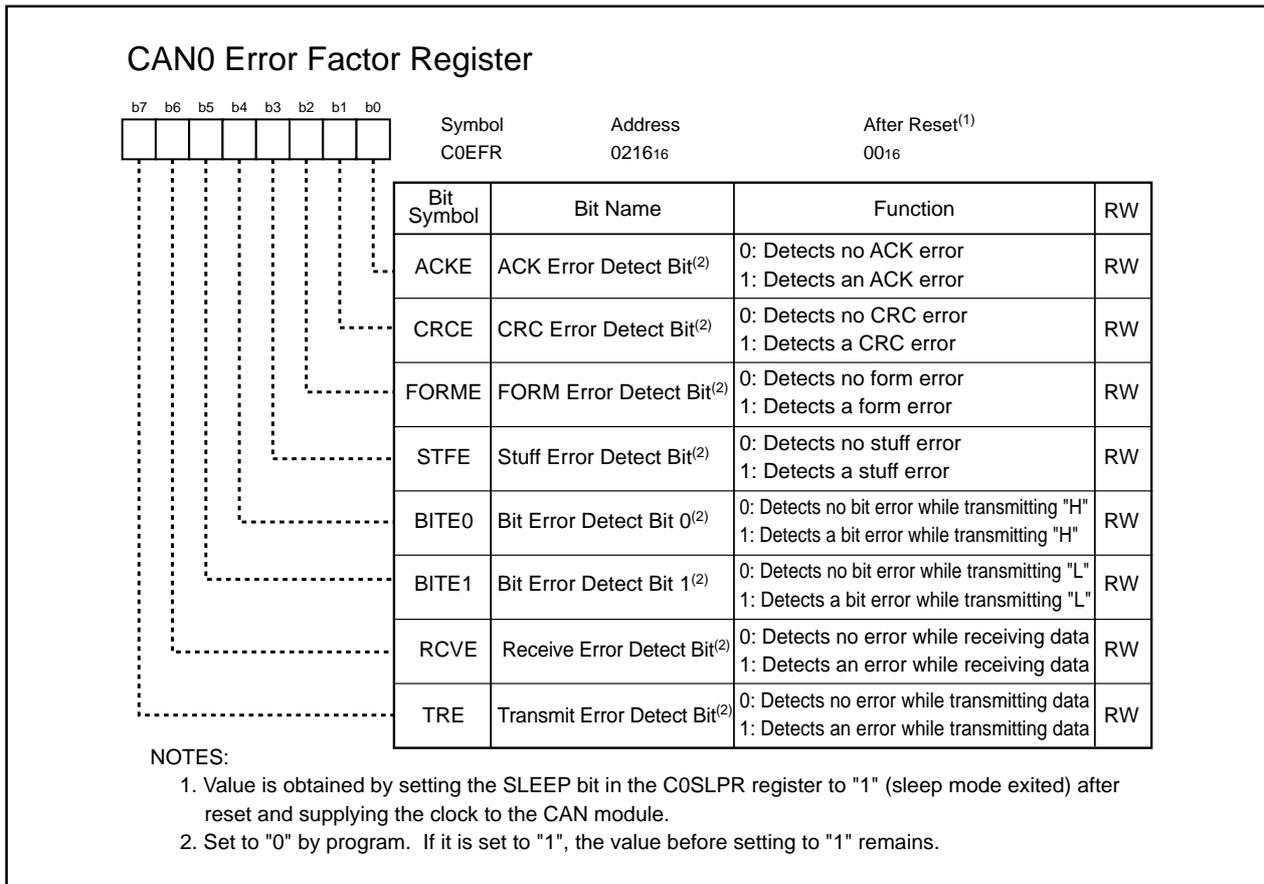


Figure 23.17 C0EFR Register

The C0EFR register indicates the cause of error when a communication error is detected. Set the following bits to "0" by program because they are not changed "1" to "0" automatically. Use the MOV instruction, instead of the bit clear instruction, to set each bit in the C0EFR register to "0". Bits not being changed to "0" must be set to "1".

For example: To set the ACKE bit to "0"

```
Assembly language:  mov.b#0FEh, C0EFR
C language:         c0efr = 0xFE;
```

23.1.15.1 ACKE Bit

The ACKE bit is set to "1" when an ACK error is detected.

23.1.15.2 CRCE Bit

The CRC bit is set to "1" when a CRC error is detected.

23.1.15.3 FORME Bit

The FORME bit is set to "1" when a form error is detected.

23.1.15.4 STFE Bit

The STFE bit is set to "1" when a stuff error is detected.

23.1.15.5 BITE0 Bit

The BITE0 bit is set to "1" when a bit error is detected while transmitting recessive "H".

23.1.15.6 BITE1 Bit

The BITE1 bit is set to "1" when a bit error is detected while transmitting dominant "L".

23.1.15.7 RCVE Bit

The RCVE bit is set to "1" when an error is detected while receiving data.

23.1.15.8 TRE Bit

The TRE bit is set to "1" when an error is detected while transmitting data.

23.1.16 CAN0 Mode Register (C0MDR Register)

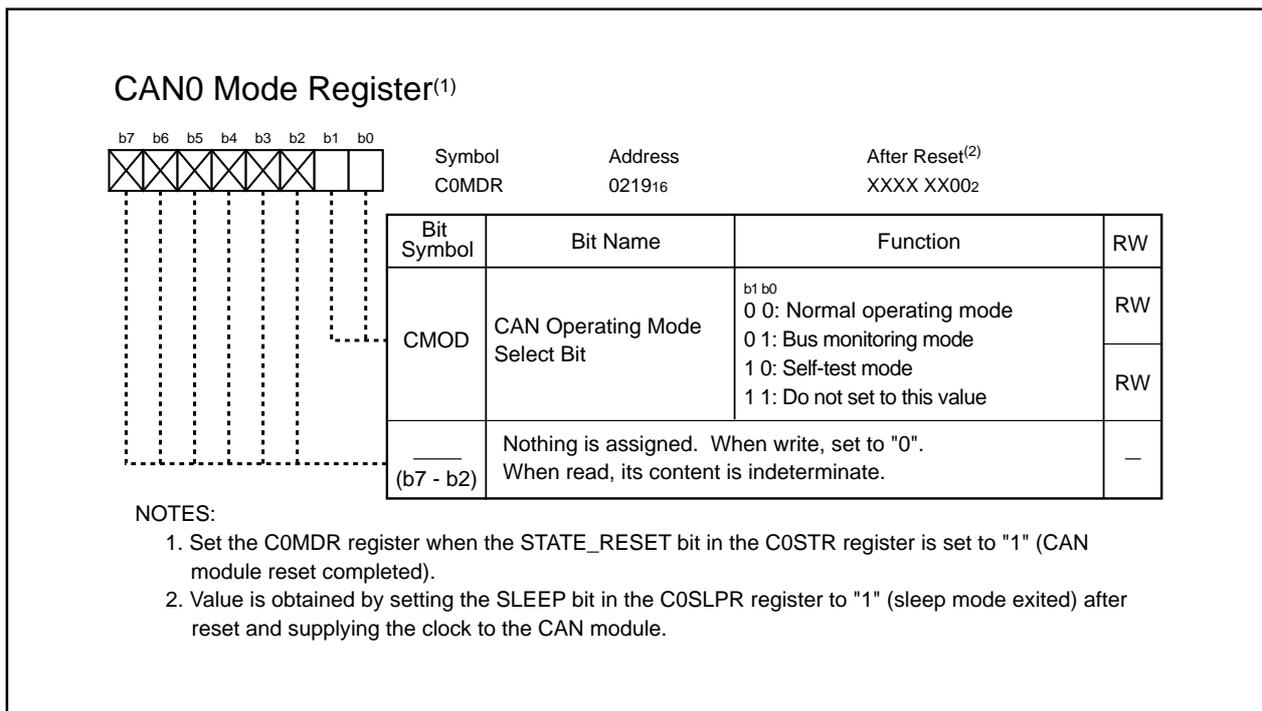


Figure 23.18 C0MDR Register

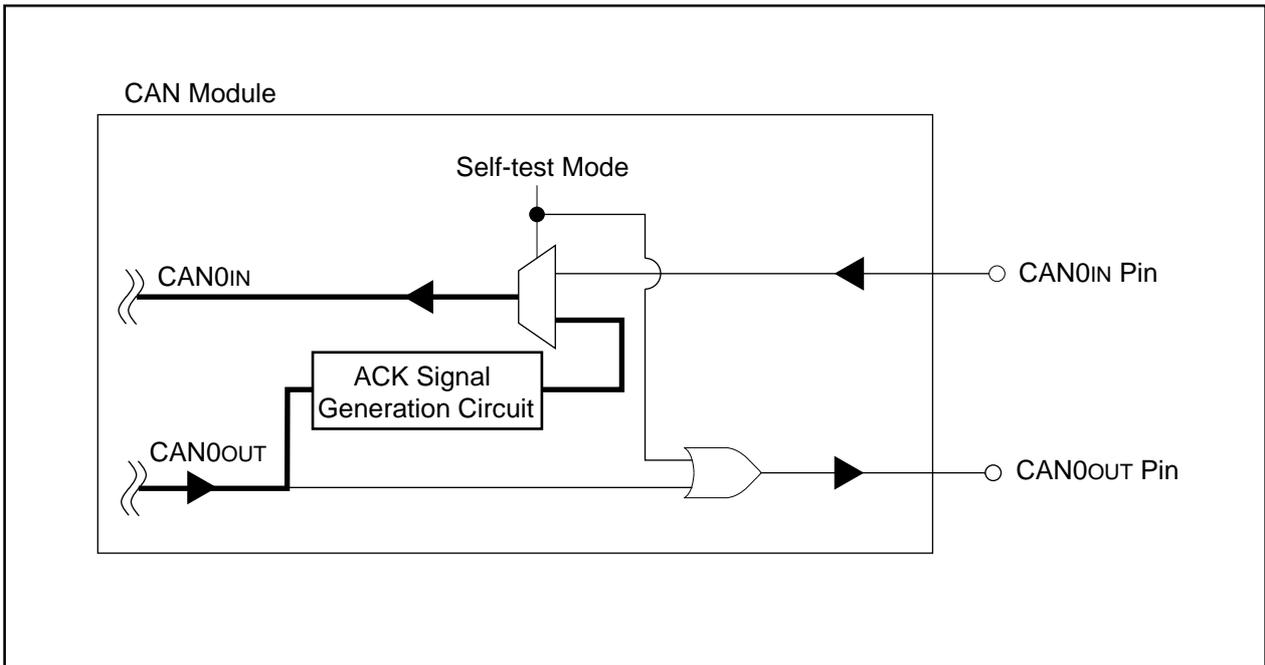
23.1.16.1 CMOD Bit

The CMOD bit selects a CAN operating mode.

- Normal operating mode: The CAN module transmits and receives data successfully.
- Bus monitoring mode⁽¹⁾: The CAN module receives data. Output signal from the CAN0OUT pin is fixed as a high-level ("H") signal in bus monitoring mode. The CAN module transmits neither ACK nor error frame.
- Self-test mode: The CAN module connects the CAN0OUT pin to the CAN0IN pin internally. The CAN module can communicate without additional device in loop back mode. Output signal from the CAN0OUT pin is fixed as an "H" signal in self-test mode while transmitting data. Figure 23.19 shows an image diagram in self-test mode.

NOTES:

- Do not generate a transmit request in bus monitoring mode.
The CAN module assumes the ACK bit is set to dominant "L" regardless of the ACK bit setting. Therefore, when the CRC delimiter is received successfully, the CAN module determines the data is received with no error regardless of the ACK bit setting.

**Figure 23.19 Self-Test Mode**

23.1.17 CAN0 Single-Shot Control Register (C0SSCTRL Register)

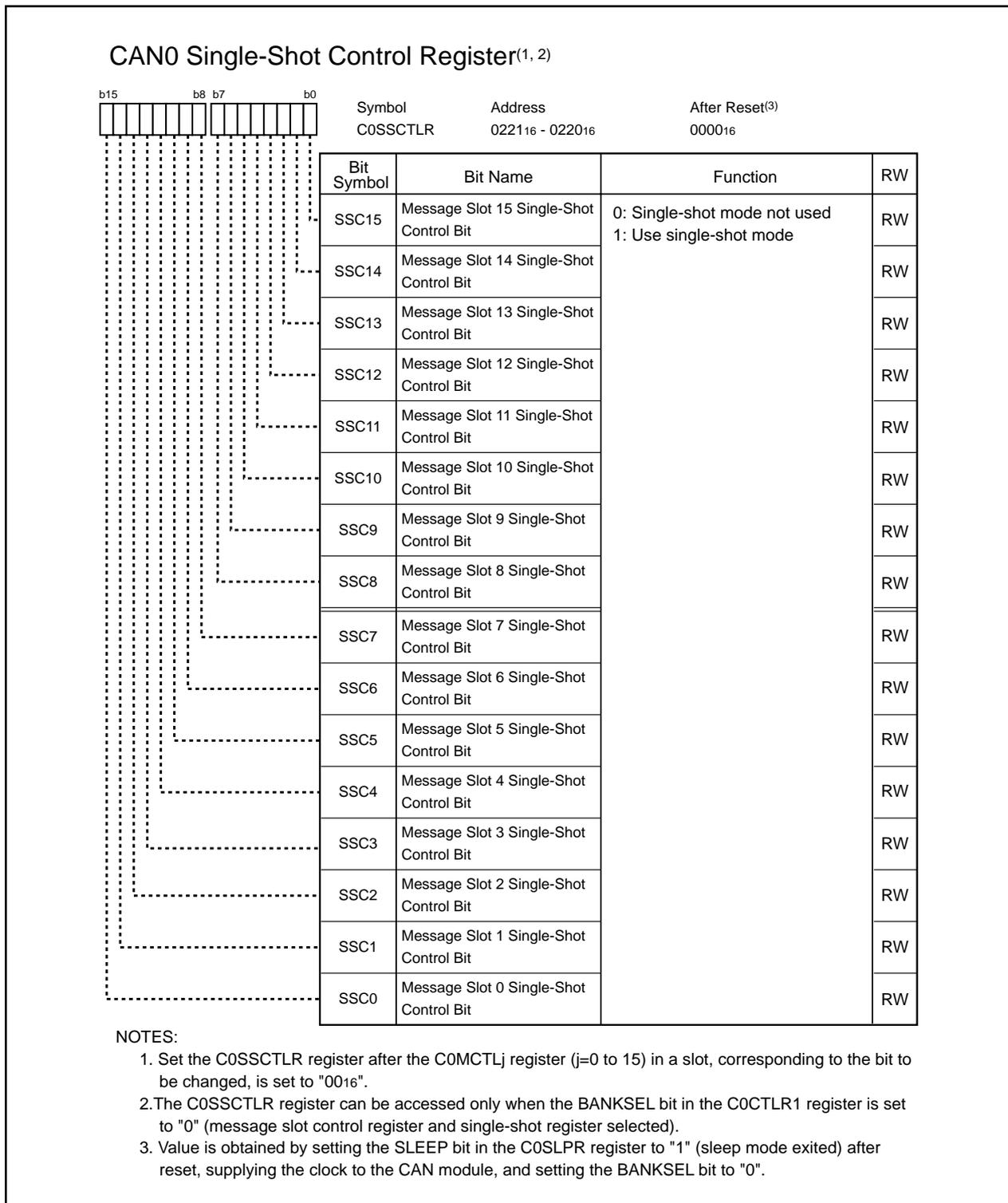


Figure 23.20 C0SSCTRL Register

According to the CAN Specification 2.0B0, if the arbitration lost or transmission error causes a transmit failure, the microcomputer continues transmitting data until the transmission is completed. The C0SSCTRL register determines whether or not, and from which slot, data is re-transmitted.

In single-shot mode, if the arbitration lost or transmission error causes a transmission failure, data is not transmitted again. When the SSCj bit (j=0 to 15) is set to "1", the corresponding message slot j is in single-shot mode.

23.1.18 CAN0 Single-Shot Status Register (C0SSSTR Register)

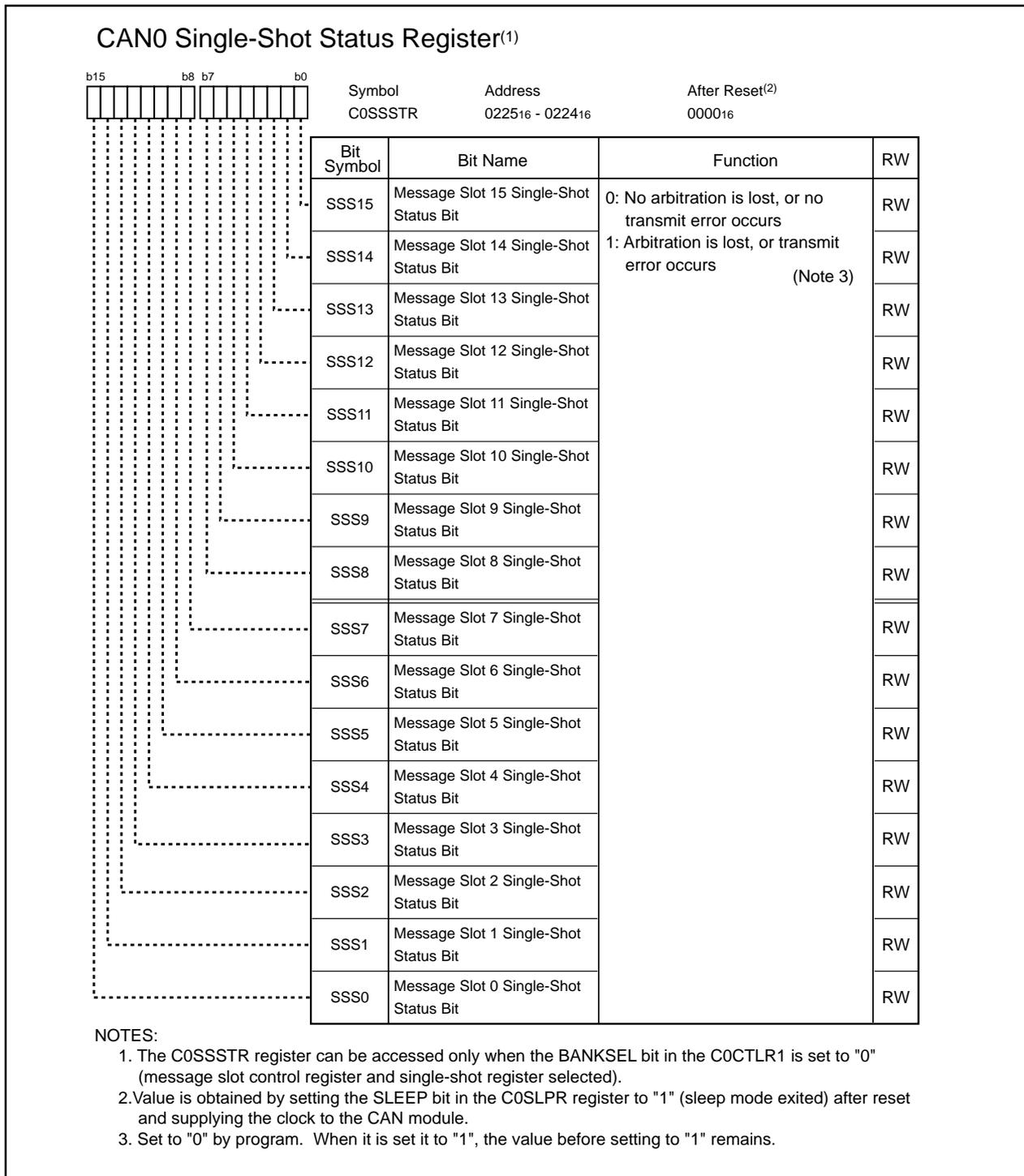


Figure 23.21 C0SSSTR Register

If the arbitration lost or transmission error causes a transmission failure, the bit corresponding to message slot j ($j=0$ to 15) is set to "1". The SSS j bit is set to "0" by program because it is not set to "0" automatically.

Use the MOV instruction, instead of the bit clear instruction, to set the SSS j bit to "0". Bits not being changed to "0" must be set to "1".

For example: To set the SSS0 bit to "0"

```
Assembly language:  mov.w #07FFFh, C0SSSTR
C language:         c0sstr = 0x7FFF;
```

23.1.19 CAN0 Global Mask Register, CAN0 Local Mask Register A and CAN0 Local Mask Register B (C0GMRk, C0LMARk and C0LMBRk Registers) (k=0 to 4)

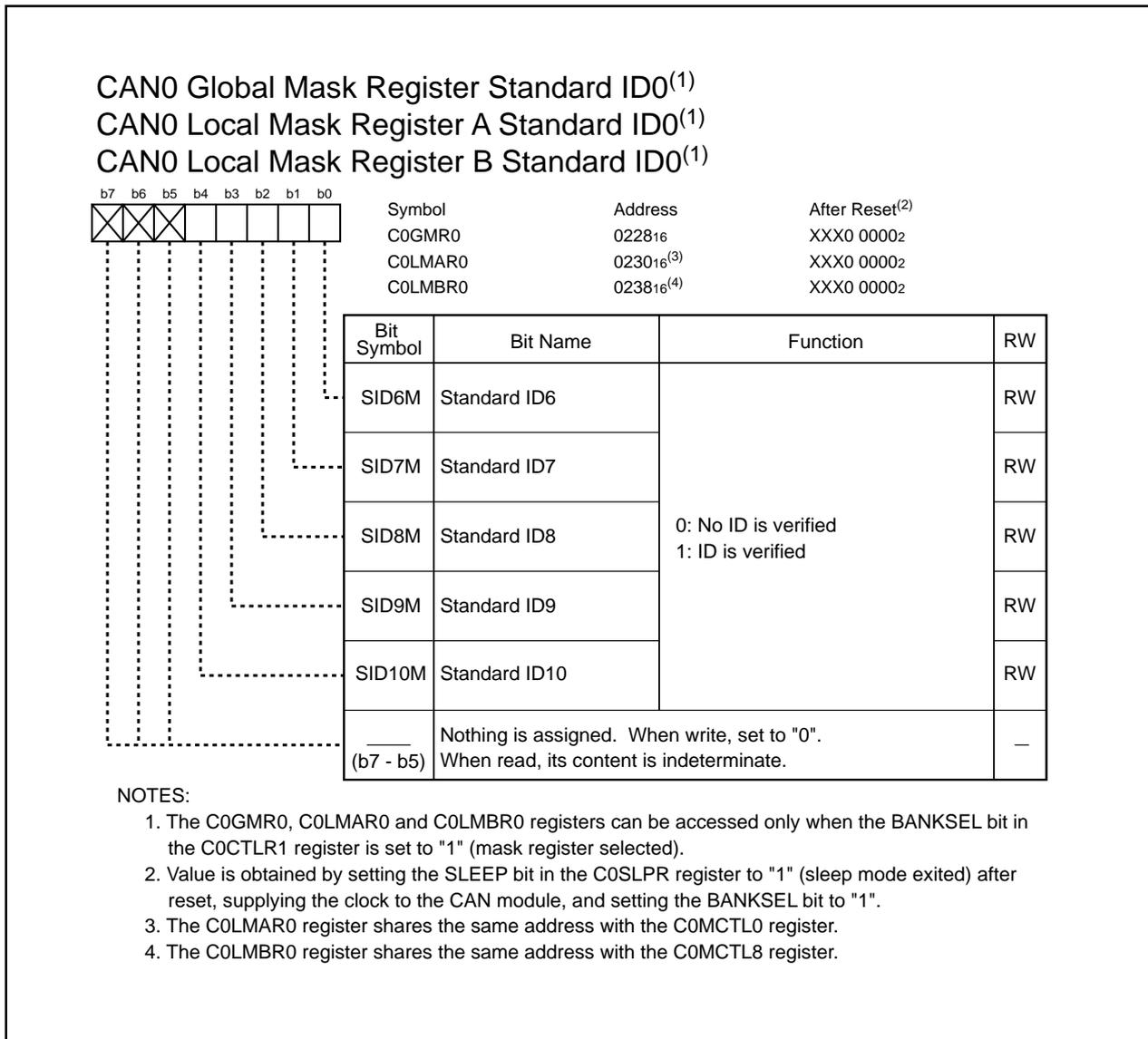


Figure 23.22 C0GMR0, C0LMAR0 and C0LMBR0 Registers

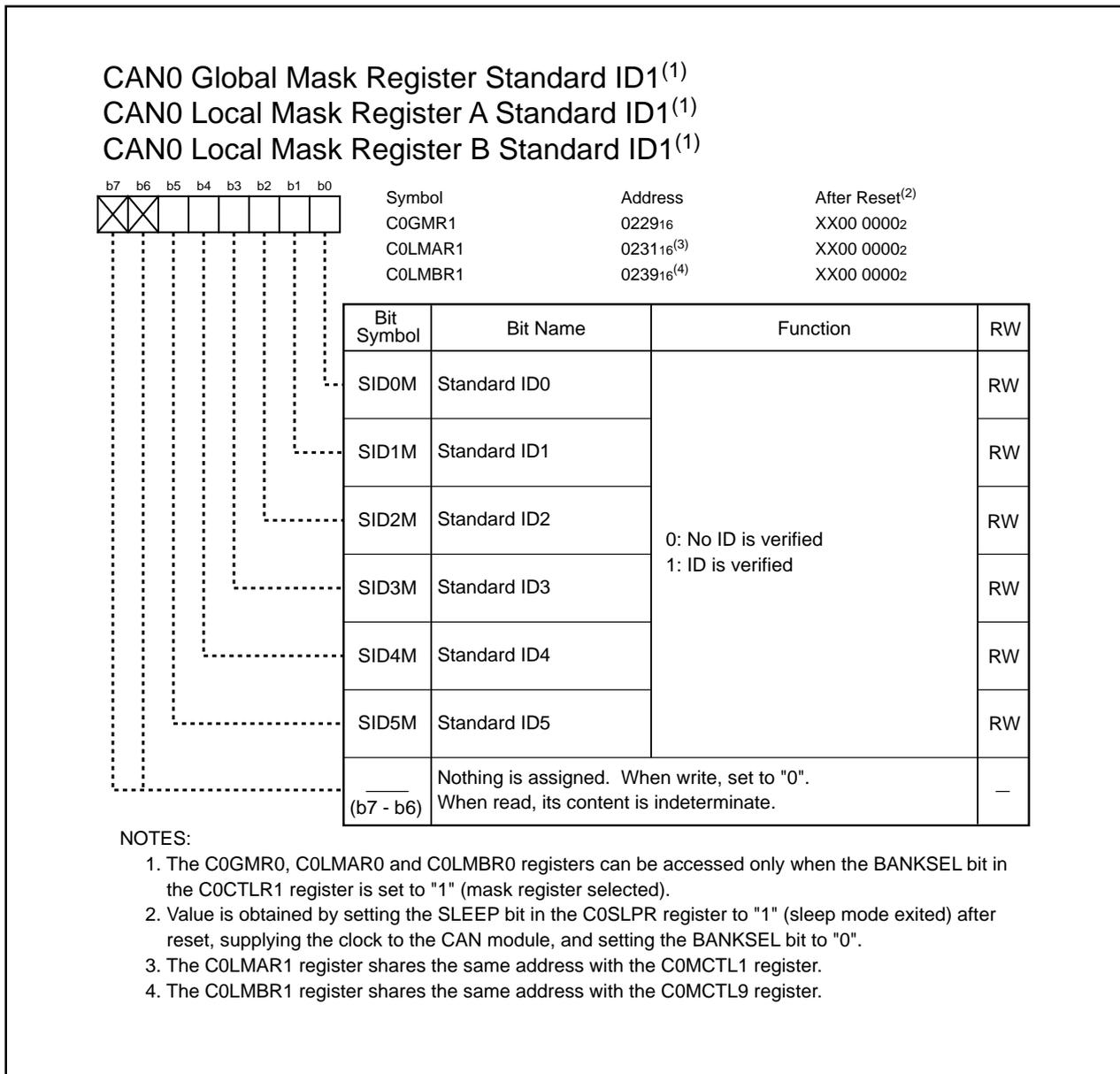


Figure 23.23 C0GMR1, C0LMAR1 and C0LMBR1 Registers

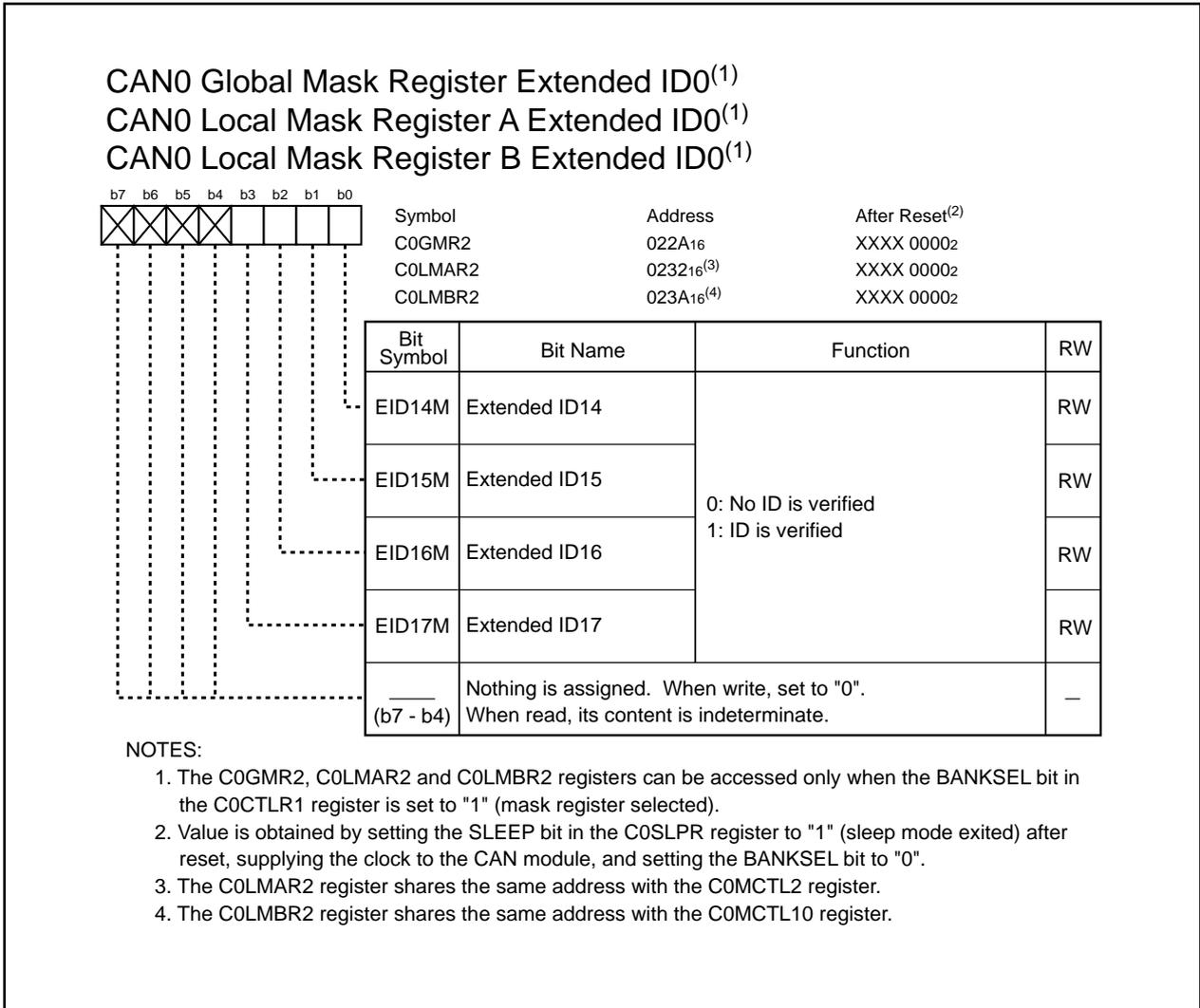


Figure 23.24 C0GMR2, C0LMAR2 and C0LMBR2 Registers

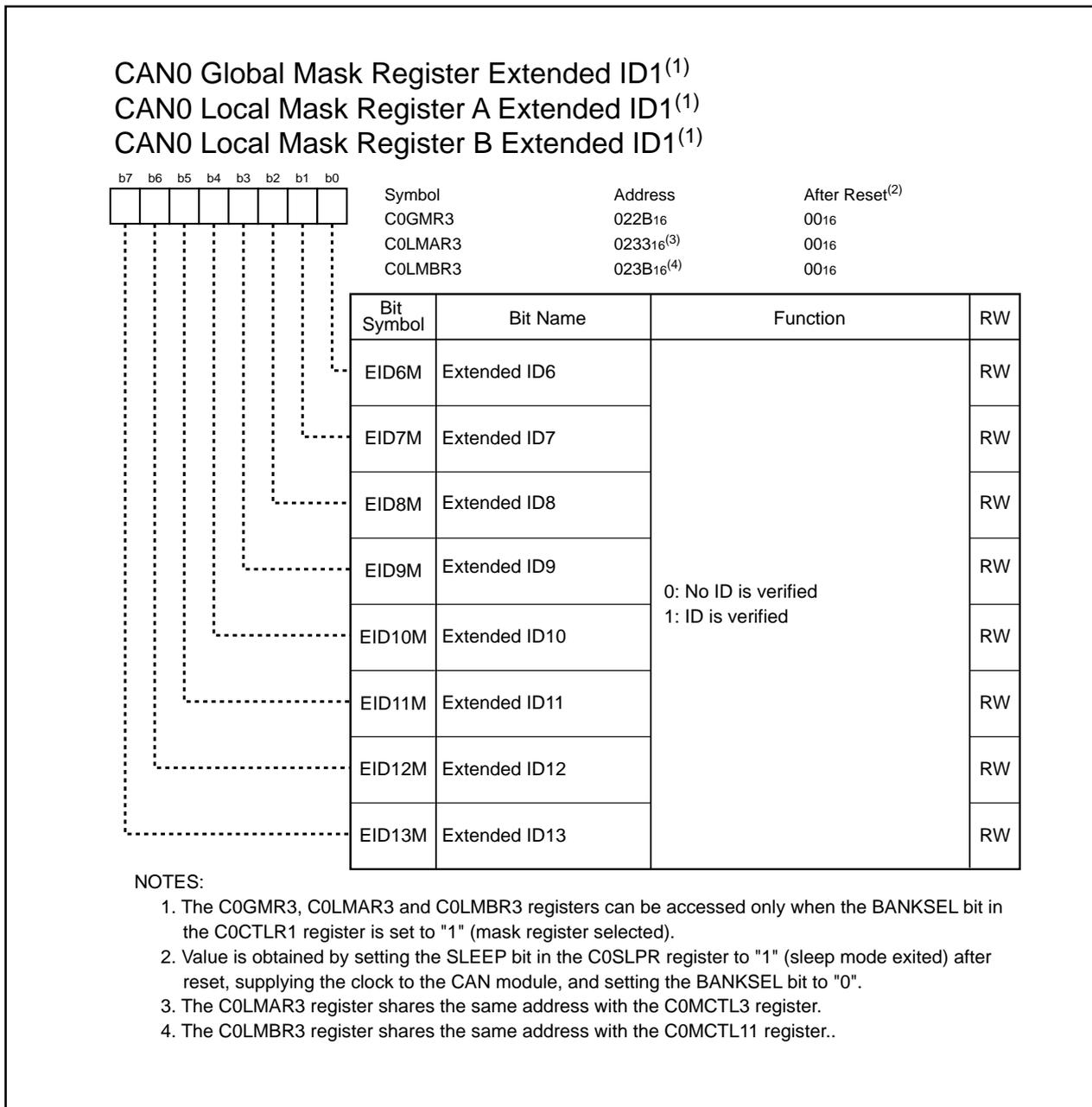


Figure 23.25 C0GMR3, C0LMAR3 and C0LMBR3 Registers

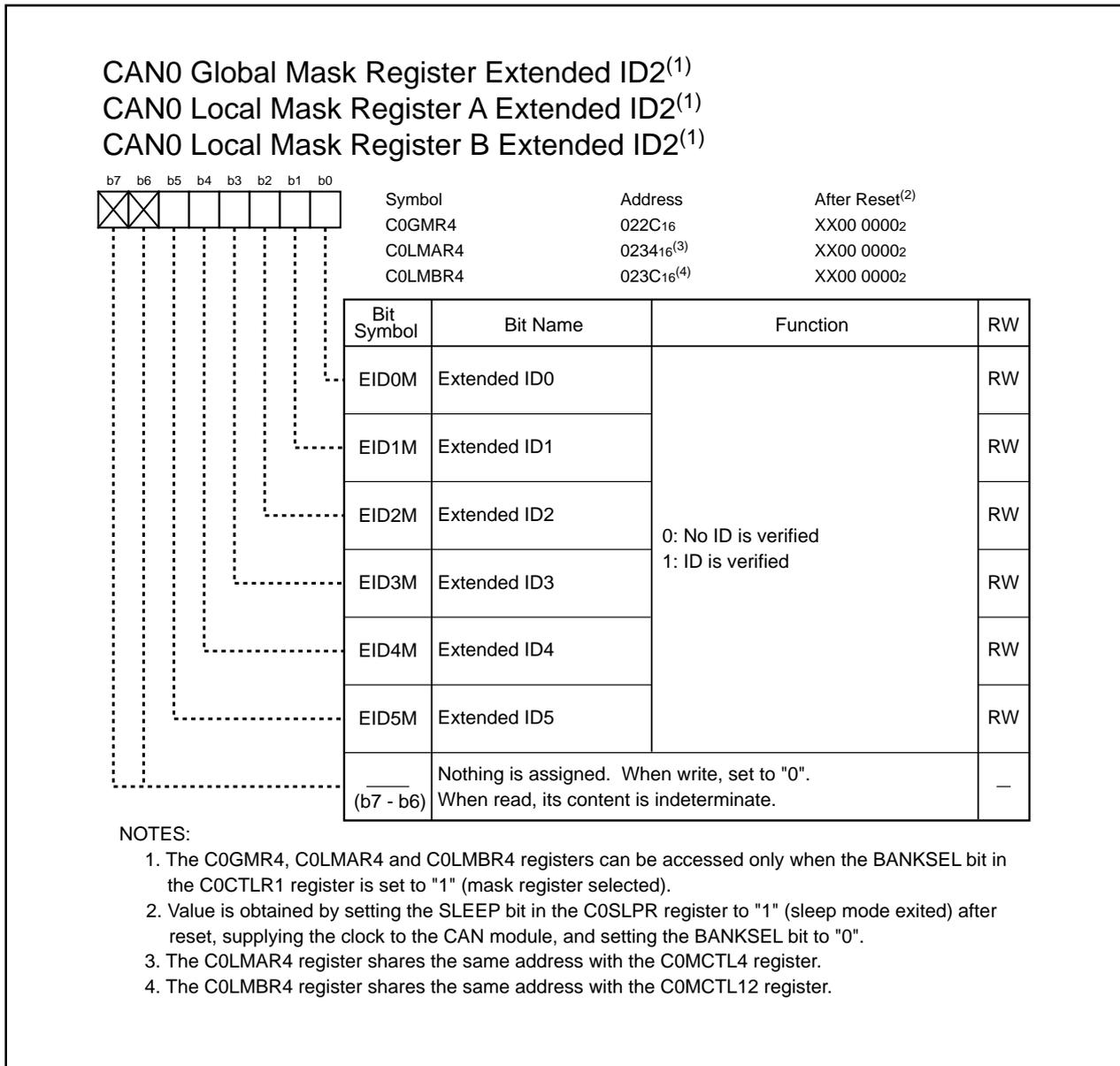


Figure 23.26 C0GMR4, C0LMAR4 and C0LMBR4 Registers

The C0GMRk, C0LMARk and C0LMBRk registers are used for acceptance filtering.

The users can select and receive user-desired messages.

The C0GMRk register determines whether IDs in the message slots 0 to 13 are verified. The C0LMARk register determines whether ID in the message slot 14 is verified. The C0LMBRk register determines whether ID in the message slot 15 is verified.

- When bits in these registers are set to "0", each standard ID0 and standard ID1 bits (ID bit) and extended ID0 to extended ID2 bits in the CAN0 message slots j ($j=0$ to 15) corresponding to the bits in the above registers, is masked while acceptance filtering. (The corresponding bits are assumed to have matching IDs.)
- When bits in these registers are set to "1", corresponding ID bits are compared with received IDs while acceptance filtering. If the received ID matches the ID in the message slot j , the received data having the matched ID is stored into that message slot.

NOTES:

1. Change the C0GMRk register setting only when the message slots 0 to 13 have no receive request.
2. Change the C0LMARk register setting only when the message slot 14 has no receive request.
3. Change the C0LMBRk register setting only when the message slot 15 has no receive request.
4. More than two message slots are able to store a receive message ID, the ID is stored into the message slot, having the smallest slot number.

Figure 23.27 shows each mask register and corresponding message slot. Figure 23.28 shows the acceptance filtering.

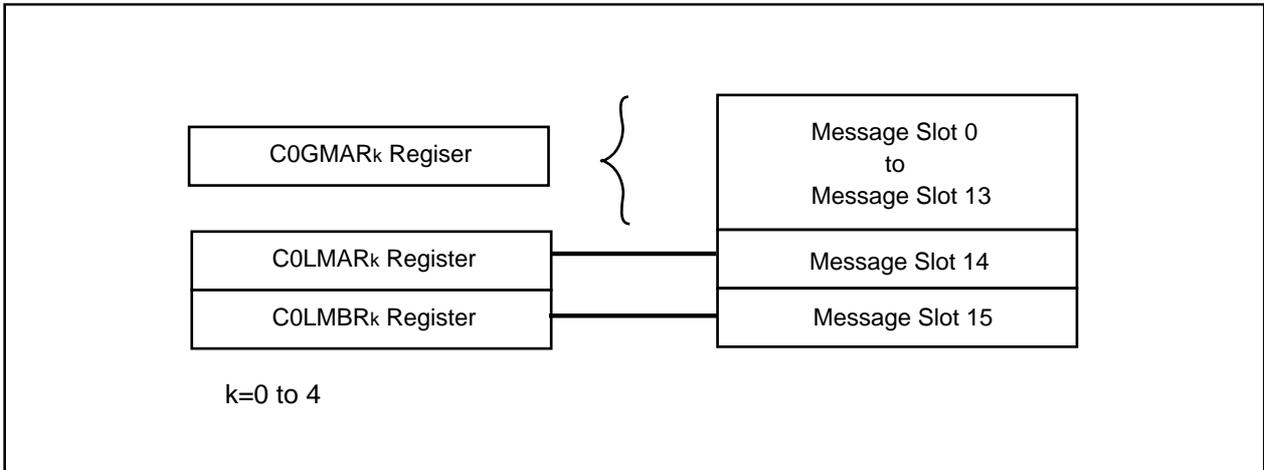


Figure 23.27 Mask Registers and Message Slots

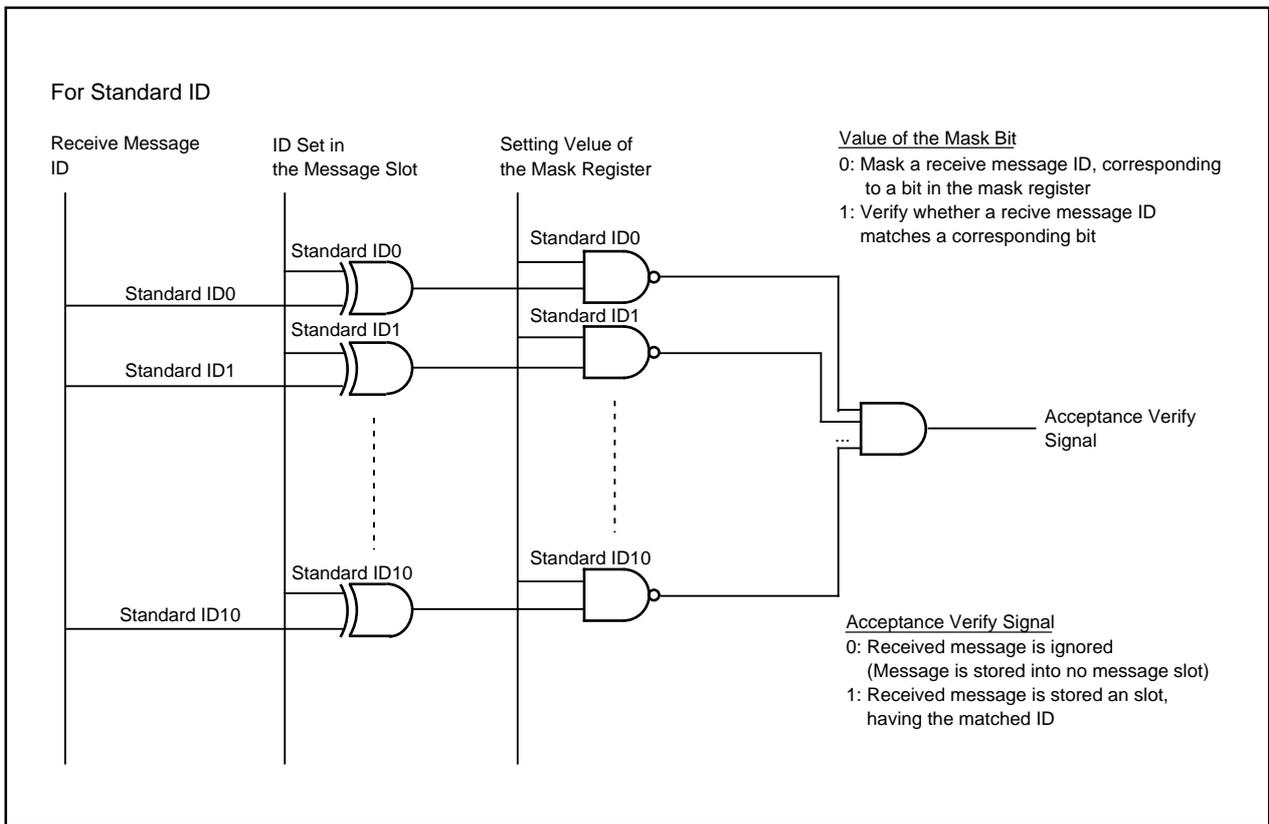


Figure 23.28 Acceptance Filtering

23.1.20 CAN0 Message Slot j Control Register (COMCTLj Register) (j=0 to 15)

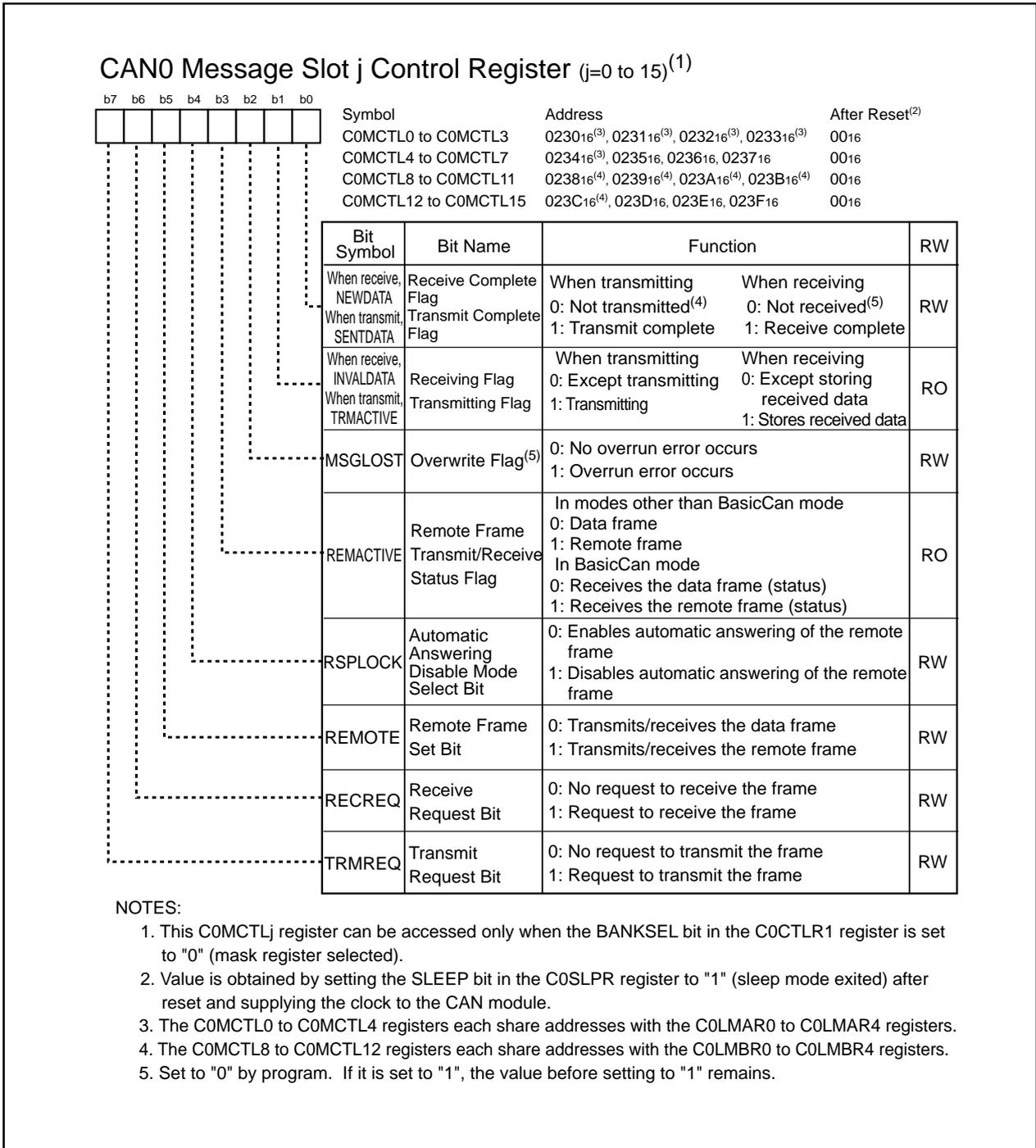


Figure 23.29 COMCTL0 to COMCTL15 Registers

Table 23.4 COMCTLj register(j= 0 to 15) Settings and Transmit/Receive Mode

Settings for the COMCTLj Register								Transmit/Receive Mode
TRMREQ	RECREQ	REMOTE	RSPLOCK	REMACTIVE	MSGLOST	TRMACTIVE INVALDATA	SENTDATA NEWDATA	
0	0	0	0	0	0	0	0	No frame is transmitted or received
0	1	0	0	0	0	0	0	Data frame is received
0	1	1	1 or 0	0	0	0	0	Remote frame is received (The data frame is transmitted after receiving the remote frame.)
1	0	0	0	0	0	0	0	Data frame is transmitted
1	0	1	0	0	0	0	0	Remote frame is transmitted (The data frame is received after transmitting the remote frame)

23.1.20.1 SENTDATA/NEWDATA Bit

The SENTDATA/NEWDATA bit indicates that the CAN module has transmitted or received the CAN message. Set the SENTDATA/NEWDATA bit to "0" (not transmitted or not received) by program before data transmission and reception is started. The SENTDATA/NEWDATA bit is not set to "0" automatically. When the TRMACTIVE/INVALDATA bit is set to "1" (during transmission or storing received data), the SENTDATA/NEWDATA bit cannot be set to "0".

SENTDATA : The SENTDATA bit is set to "1" (transmit complete) when data transmission is completed in the transmit message slot.

NEWDATA : The NEWDATA bit is set to "1" (receive complete) when the message to be stored into the message slot j (j=0 to 15) is received in the receive message slot successfully.

NOTES:

1. To read a received data from the message slot j, set the NEWDATA bit to "0" before reading. If the NEWDATA bit is set to "1" immediately after reading, this indicates that new received data has been stored into the message slot while reading and the read data contains an indeterminate value. In this case, discard the data with indeterminate value and then read the message slot again after the NEWDATA bit is set to "0".
2. When the remote frame is transmitted or received, the SENTDATA/NEWDATA bit remains unchanged after the remote frame transmission or reception is completed. The SENTDATA/NEWDATA bit is set to "1" when a subsequent data frame transmission or reception is completed.

23.1.20.2 TRMACTIVE/INVALDATA Bit

The TRMACTIVE/INVALDATA bit indicates that the CAN protocol controller is transmitting or receiving a message and accessing the message slot j. The TRMACTIVE/INVALDATA bit is set to "1" when the CAN module is accessing the message slot and to "0" when not accessing the message slot.

TRMACTIVE : The TRMACTIVE bit is set to "1" (except transmitting) when a data transmission is started in the message slot. If the CAN module loses in bus arbitration, the TRMACTIVE bit is set to "0" (stops transmitting) when a CAN bus error occurs or when a data transmission is completed.

INVALDATA : The INVALDATA bit is set to "1" (storing received data) when receiving a received message into the message slot j, after a message reception is completed. Then the INVALDATA bit is set to "0" after a message storage is completed. Data, if read from the message slot j while this bit is set to "1", is indeterminate.

23.1.20.3 MSGLOST Bit

The MSGLOST bit is valid only when the message slot is set for reception. The MSGLOST bit is set to "1" (overflow error occurred) when the message slot *j* is overwritten by a new received message while the NEWDATA bit is set to "1" (already received).

The MSGLOST bit is not automatically set to "0". Set to "0" (no overflow error occurred) by program.

23.1.20.4 REMACTIVE Bit

The COMCTL0 to COMCTL15 registers all have the same function when the STATE_BASICCAN bit is set to "0" (other than BasicCAN mode).

The REMACTIVE bit is set to "1" (remote frame) when the message slot *j* is set to transmit or receive the remote frame. The REMACTIVE bit is set to "0" (data frame) after the remote frame has been transmitted or received.

The functions of the COMCTL14 and COMCTL15 registers change when the STATE_BASICCAN bit is set to "1" (BasicCAN mode). When the REMACTIVE bit is set to "0", this indicates that a message stored into the message slot is the data frame. When the REMACTIVE bit is set to "1", this indicates a message stored into the message slot is the remote frame.

23.1.20.5 RSPLOCK Bit

The RSPLOCK bit is valid only when remote frame reception shown in Table 23.4 is selected. The RSPLOCK bit determines whether the received remote frame is processed or not.

When the RSPLOCK bit is set to "0" (automatic answering of the remote frame enabled), the slot automatically changes to a transmit slot after the remote frame is received and the message stored into the message slot is automatically transmitted as the data frame.

When the RSPLOCK bit is set to "1" (automatic answering of the remote frame disabled), message is not automatically transmitted upon receiving the remote frame.

Set the RSPLOCK bit to "0" to select any transmit/receive mode other than the remote frame reception.

23.1.20.6 REMOTE Bit

The REMOTE bit selects transmit/receive mode shown in Table 23.4. Set the REMOTE bit to "0" to transmit or receive data frame. Set to "1" to transmit or receive remote frame.

The followings occur during remote frame transmission or reception.

- Transmitting the remote frame

A message stored into the message slot *j* (*j*=0 to 15) is transmitted as the remote frame. After transmission, the slot automatically becomes ready to receive data frame.

If the data frame is received before the remote frame is transmitted, the data frame is stored into the message slot *j*. The remote frame is not transmitted.

- Receiving the remote frame

The message slot receives the remote frame. The RSPLOCK bit determines whether or not to process the received remote frame.

23.1.20.7 RECREQ Bit

The RECREQ bit selects transmit/receive mode shown in Table 23.4. Set the RECREQ bit to "1" (receive requested) when data frame or remote frame is received. Set the RECREQ bit to "0" (no receive requested) when data frame or remote frame is transmitted.

When a data frame is automatically transmitted after a remote frame is received, the RECREQ bit remains set to "1". Set the RECREQ bit to "0" to transmit a remote frame. After a remote frame is transmitted, a data frame is automatically received while the RECREQ bit remains set to "0".

When setting the TRMREQ bit to "1" (transmit requested), do not set the RECREQ bit to "1" (receive requested).

23.1.20.8 TRMREQ Bit

The TRMREQ bit selects transmit/receive mode shown in Table 23.4. Set the TRMREQ bit to "1" (transmit requested) when data frame or remote frame is transmitted.

Set the TRMREQ bit to "0" (no request to transmit the frame) when data frame or remote frame is received.

When the data frame is automatically received after the remote frame is transmitted, the TRMREQ bit remains set to "1". Set the TRMREQ bit to "0" to receive the remote frame. After the remote frame is received, data frame is automatically transmitted while the TRMREQ bit remains set to "0".

If the RECREQ bit is set to "1" (request to receive the frame), do not set the TRMREQ bit to "1" (request to transmit the frame).

NOTES:

1. If some message slots are requested to transmit the data frame or remote frame, the message slot, having the smallest slot number starts transmitting.
2. In single-shot mode, the COMCTLj register is set to "0016" when data transmission is failed, due to the arbitration lost or transmission error.

23.1.21 CAN0 Slot Buffer Select Register (C0SBS Register)

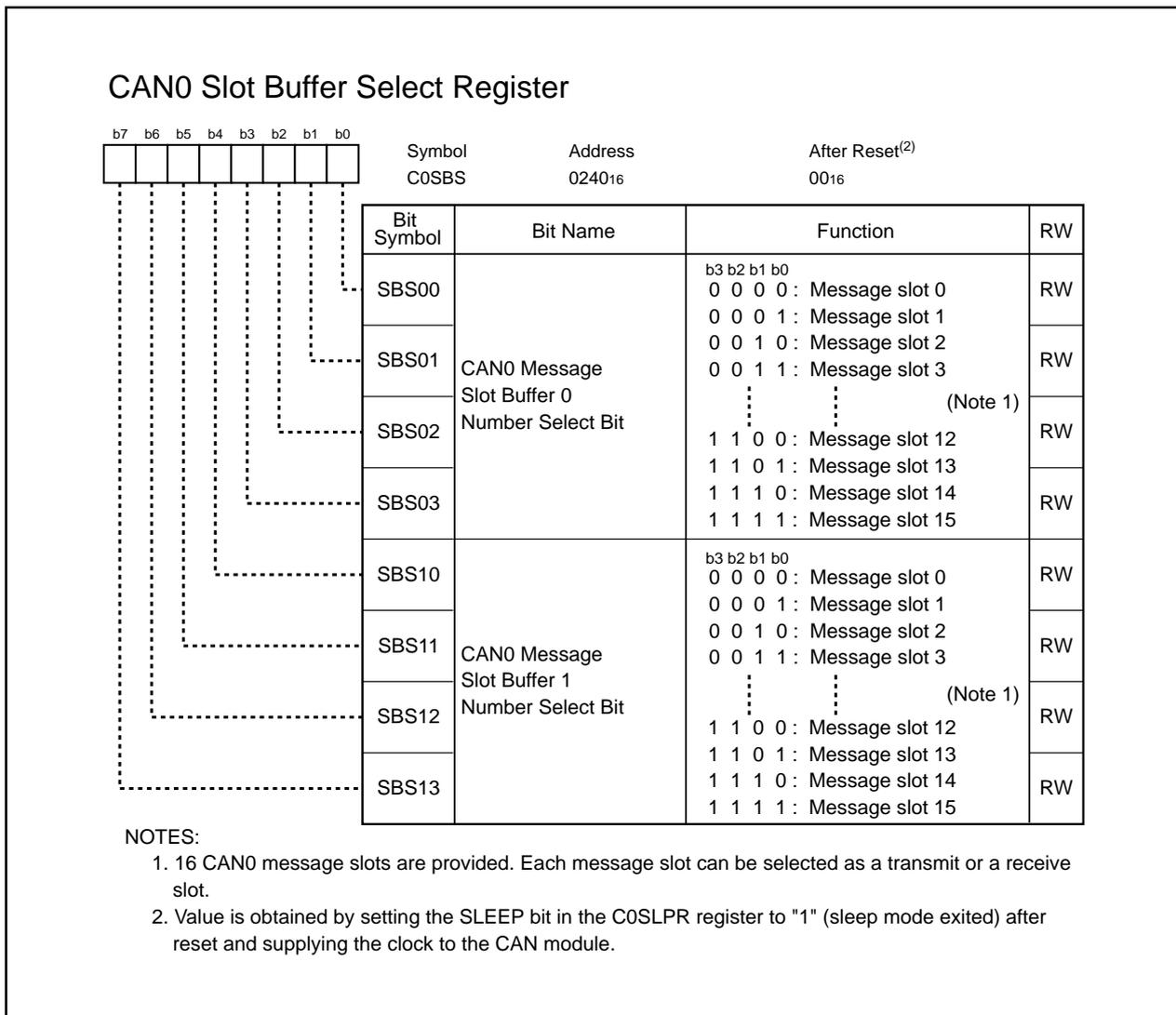


Figure 23.30 C0SBS Register

23.1.21.1 SBS03 to SBS00 Bits

If the SBS03 to SBS00 bits select a number j ($j=0$ to 15), the message slot j is allocated to the CAN0 message slot buffer 0. The message slot j can be accessed via addresses 01E0₁₆ to 01EF₁₆.

23.1.21.2 SBS13 to SBS10 Bits

If the SBS13 to SBS10 bits select a number j , the message slot j is allocated to the CAN0 message slot buffer 1. The message slot j can be accessed via addresses 01F0₁₆ to 01FF₁₆.

23.1.22 CAN0 Message Slot Buffer j (j=0,1)

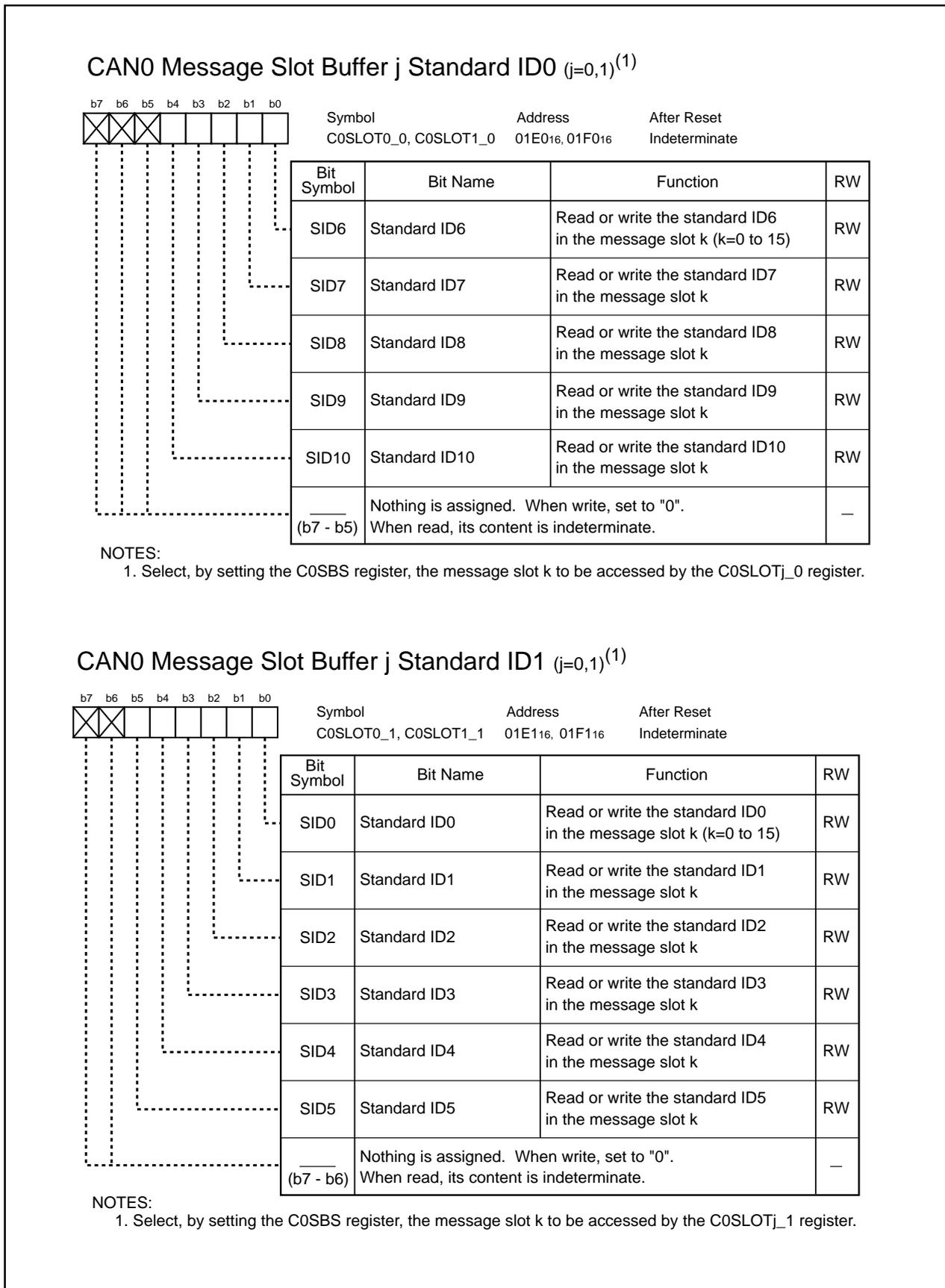


Figure 23.31 C0SLOT0_0, C0SLOT1_0, C0SLOT0_1 and C0SLOT1_1 Register

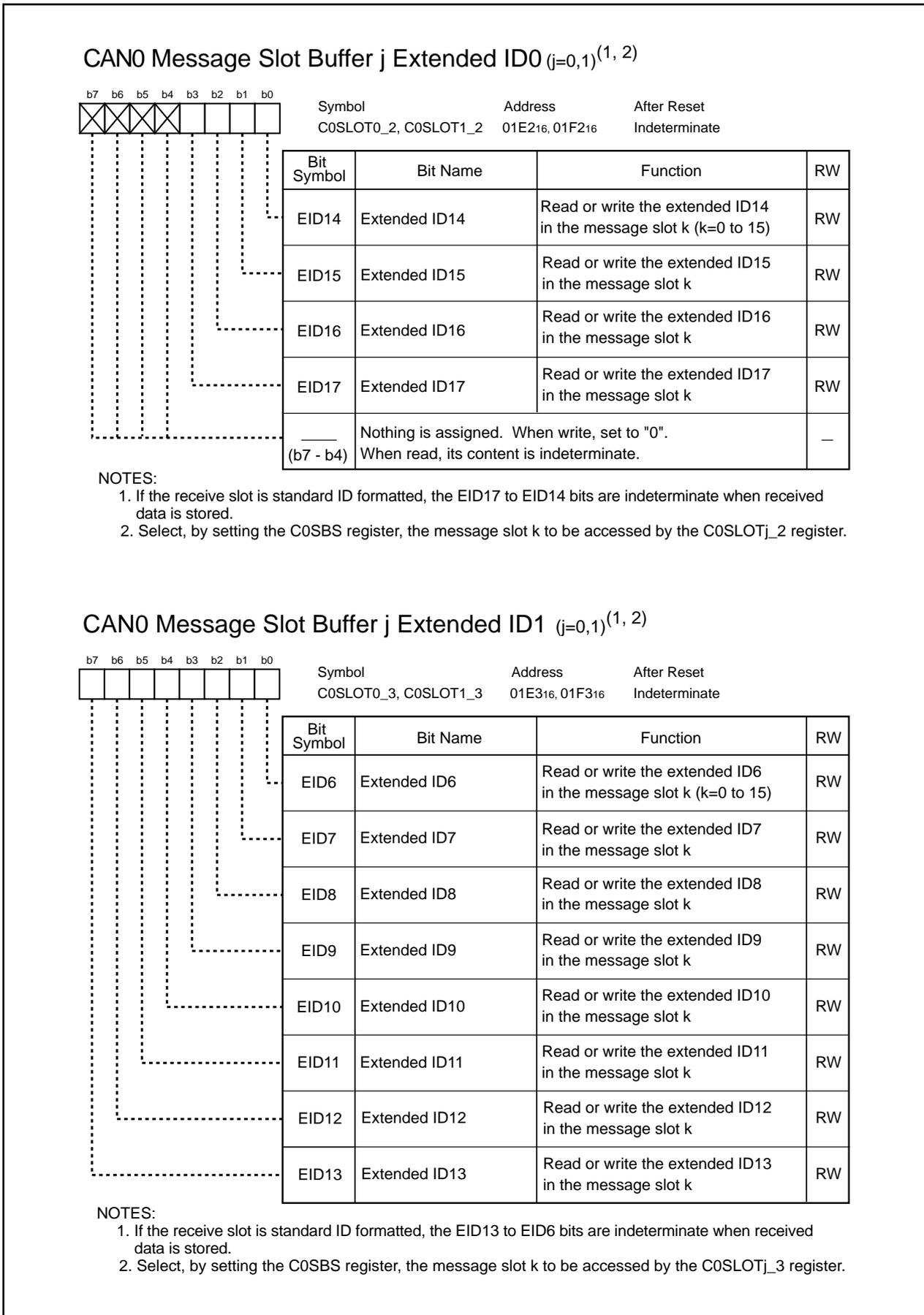


Figure 23.32 C0SLOT0_2, C0SLOT1_2, C0SLOT0_3 and C0SLOT1_3 Registers

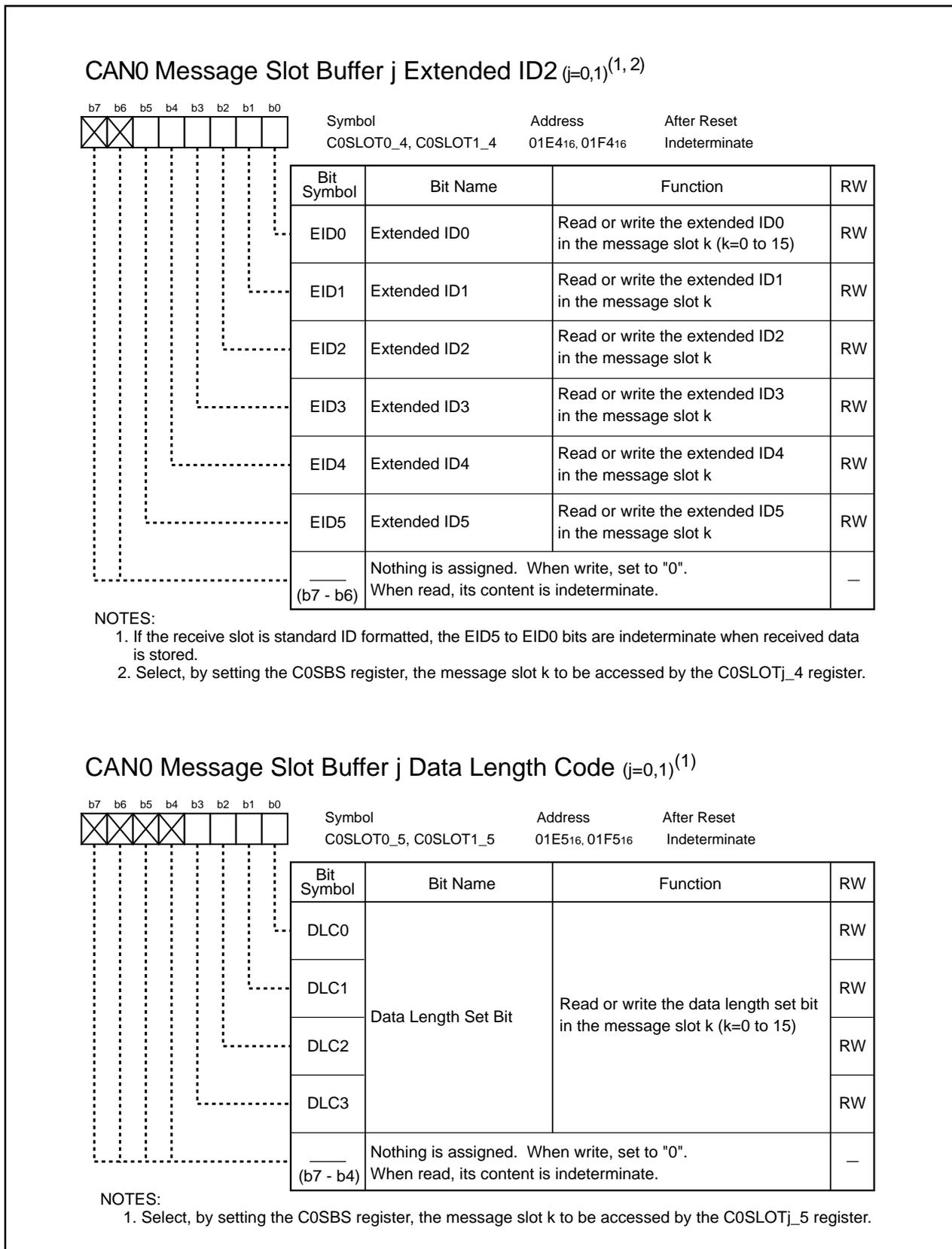


Figure 23.33 C0SLOT0_4, C0SLOT1_4, C0SLOT0_5 and C0SLOT1_5 Registers

CAN0 Message Slot Buffer j Data m (j=0,1, m=0 to 7)^(1, 2)

b7 ┌───────────┐ │ │ │ │ │ │ │ │ │ │ │ │ │ │ └───────────┘ b0	Symbol C0SLOT0_6 to C0SLOT0_13 C1SLOT0_6 to C1SLOT0_13	Address 01E6 ₁₆ - 01ED ₁₆ 01F6 ₁₆ - 01FD ₁₆	After Reset Indeterminate Indeterminate	
	Function		Setting Range	RW
	Read or write data m in the message slot k (k=0 to 15)		00 ₁₆ to FF ₁₆	RW

NOTES:

1. Select, by setting the C0SBS register, the data m in the message slot k to be accessed by the C0SLOTj_6 to C0SLOTj_13 registers.
2. When the data frame is received, data with less than the data length selected by the C0SLOTj_5 register is indeterminate.

CAN0 Message Slot Buffer j Time Stamp High-Ordered (j=0,1)⁽¹⁾

b7 ┌───────────┐ │ │ │ │ │ │ │ │ │ │ │ │ │ │ └───────────┘ b0	Symbol C0SLOT0_14, C0SLOT1_14	Address 01EE ₁₆ , 01FE ₁₆	After Reset Indeterminate	
	Function		Setting Range	RW
	Read or write the time stamp high-ordered in the message slot k (k=0 to 15)		00 ₁₆ to FF ₁₆	RW

NOTES:

1. Select, by setting the C0SBS register, the time stamp high-ordered in the message slot k to be accessed by the C0SLOTj_14 register.

CAN0 Message Slot Buffer j Time Stamp Low-Ordered (j=0,1)⁽¹⁾

b7 ┌───────────┐ │ │ │ │ │ │ │ │ │ │ │ │ │ │ └───────────┘ b0	Symbol C0SLOT0_15, C0SLOT1_15	Address 01EF ₁₆ , 01FF ₁₆	After Reset Indeterminate	
	Function		Setting Range	RW
	Read or write the time stamp low-ordered in the message slot k (k=0 to 15)		00 ₁₆ to FF ₁₆	RW

NOTES:

1. Select, by setting the C0SBS register, the time stamp low-ordered in the message slot k to be accessed by the C0SLOTj_15 register.

Figure 23.34 C0SLOT0_6 to C0SLOT0_13, C0SLOT1_6 to C0SLOT1_13, C0SLOT0_14, C0SLOT1_14, C0SLOT0_15 and C0SLOT1_15 Registers

The message slot, selected by setting the C0SBS register, is read by reading the message slot buffer. A message can be written in the message slot selected by the C0SBS register if the message is written to the message slot buffer.

Write to the message slot k (k=0 to 15) while the corresponding C0MCTLk register is set to "0016".

23.2 CAN Clock

The CAN clock is the operating clock for the CAN module. f_1 or f_{CAN} can be selected as the CAN clock. f_{CAN} has the same frequency as the main clock. The PM25 bit in the PM2 register determines the CAN clock. Refer to **9. Clock Generation Circuit** for details.

23.2.1 Main Clock Direct Mode

f_{CAN} becomes the CAN clock in main clock direct mode. The CAN module must enter main clock direct mode while the PM25 bit is set to "1" (main clock). Set the PM25 bit in CAN sleep mode.

Set the PM24 bit in the PM2 register to "1" (main clock) before accessing CAN-associated registers in main clock direct mode. Do not enter wait mode or stop mode when the PM24 bit is set to "1".

Table 23.5 lists CAN clock settings. Figure 23.36 shows a flow chart of accessing procedure for CAN-associated registers.

Table 23.5 CAN Clock Settings

CAN Clock	Clock Source	CM0 Register	CM1 Register	CM2 Register	PM2 Register		MCD Register
		CM07 Bit	CM17 Bit	CM21 Bit	PM24 Bit	PM25 Bit	MCD4 to MCD0 bits
f_{CAN}	Main Clock (Main Clock Direct Mode)	0	1	0	1	1	---
f_1	Main Clock	0	0	0	0	0	10010 ₂
	PLL Clock	0	1	0	0	0	10010 ₂

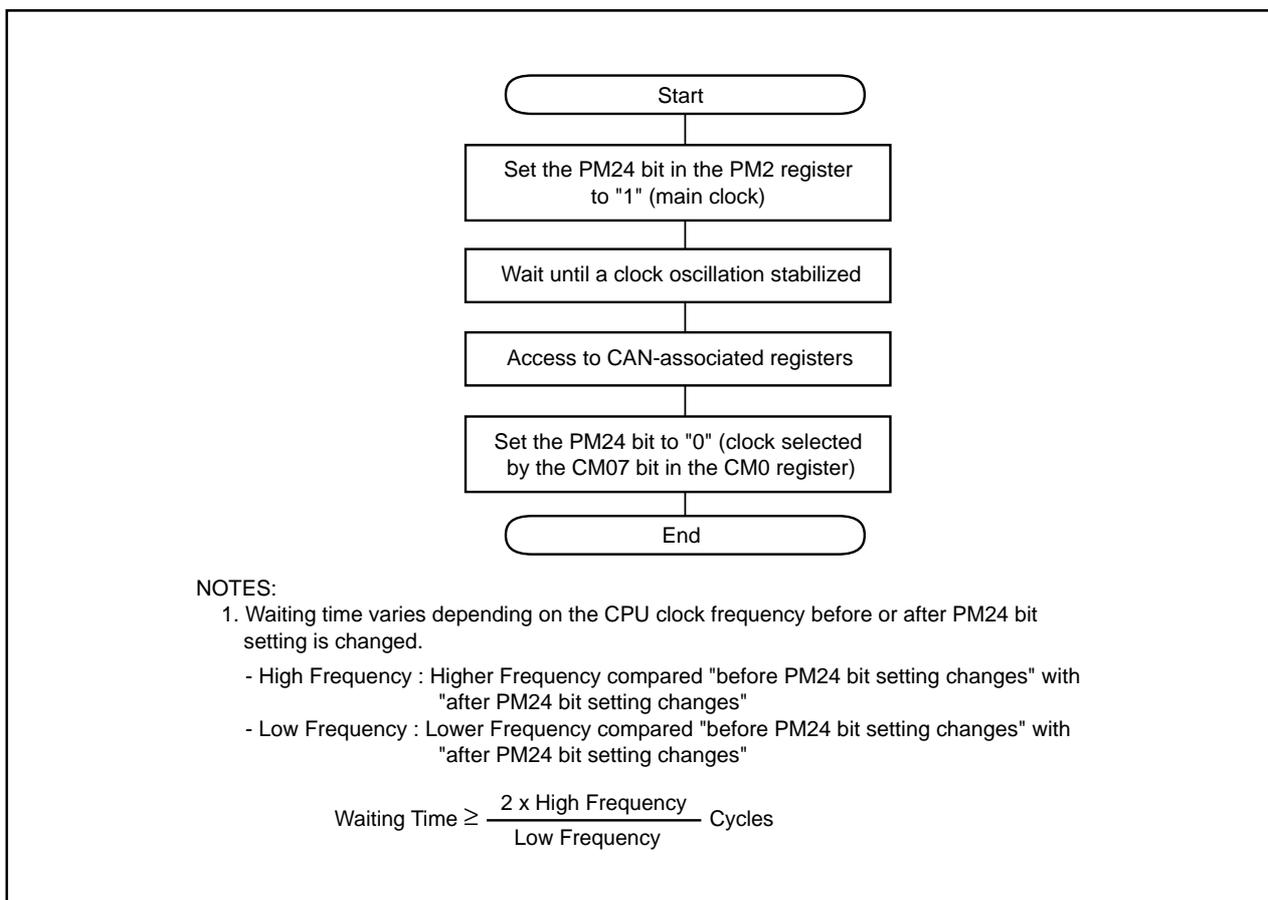


Figure 23.36 Accessing Procedure for CAN-Associated Registers

23.3 Timing with CAN-Associated Registers

23.3.1 CAN Module Reset Timing

Figure 23.37 shows an operation example of when the CAN module is reset.

- (1) The CAN module can be reset when the STATE_RESET bit in the C0STR register is set to "1" (CAN module reset completed) after the RESET1 and RESET0 bits in the C0CTRL0 register are set to "1" (CAN module reset).
- (2) Set necessary CAN-associated registers.
- (3) CAN communication can be established after the STATE_RESET bit is set to "0" (resetting) after the RESET1 and RESET0 bits are set to "0" (CAN module reset exited) .

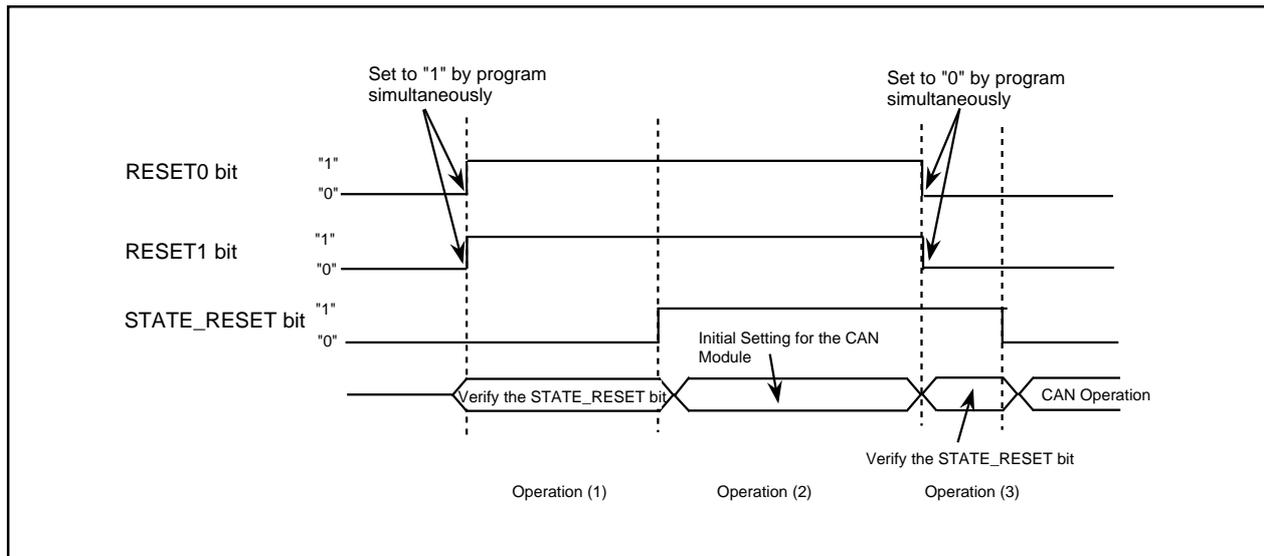


Figure 23.37 Example of CAN Module Reset Operation

23.3.2 CAN Transmit Timing

Figure 23.38 shows an operation example of when the CAN transmits a frame.

- (1) When the TRMREQ bit in the C0MCTLj register (j=0 to 15) is set to "1" (request to transmit the data frame) while the CAN bus is in an idle state, the TRMACTIVE bit in the C0MCTLj register is set to "1" (during transmission) and the TRMSTATE bit in the C0STR register is set to "1" (during transmission). The CAN starts transmitting the frame.
- (2) After a CAN frame transmission is completed, the SENTDATA bit in the C0MCTLj register is set to "1" (already transmitted), the TRMSUCC bit in the C0STR register to "1" (transmission completed) and the SISj bit in the C0SISTR register to "1" (interrupt requested). The MBOX3 to MBOX0 bits in the C0STR register store transmitted message slot numbers.

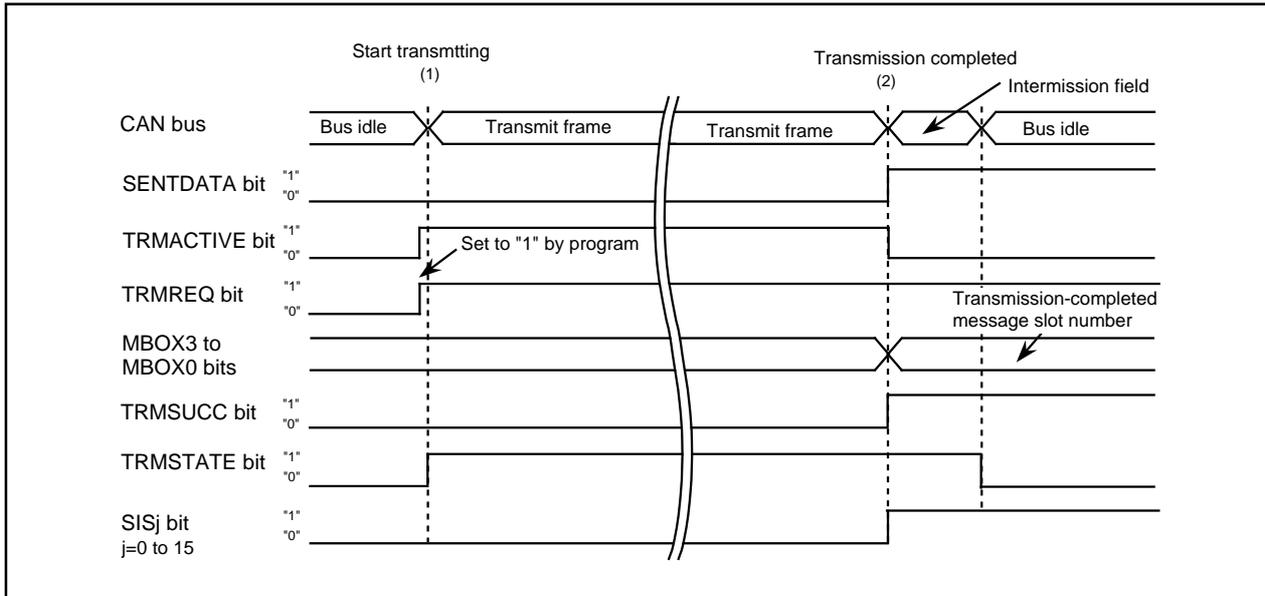


Figure 23.38 Example of CAN Data Frame Transmit Operation

23.3.3 CAN Receive Timing

Figure 23.39 shows an operation example of when the CAN receives a frame.

- (1) When the RECREQ bit in the COMCTLj register (j= 0 to 15) is set to "1" (receive requested), the CAN is ready to receive the frame at anytime.
- (2) When the CAN starts receiving the frame, the RECSTATE bit in the C0STR register is set to "1" (during reception).
- (3) After the CAN frame reception is completed, the INVALIDDATA bit in the COMCTLj register is set to "1" (storing received data), the NEWDATA bit in the COMCTLj register is set to "1" (receive complete) and the RECSUCC bit in the C0STR register is set to "1" (reception completed).
- (4) After data is written to the message slot, the INVALIDDATA bit is set to "0" (storing receiving data) and the SISj bit in the C0SISTR register is set to "1" (interrupt requested). The MBOX3 to MBOX0 bits in the C0STR register store received message slot numbers.

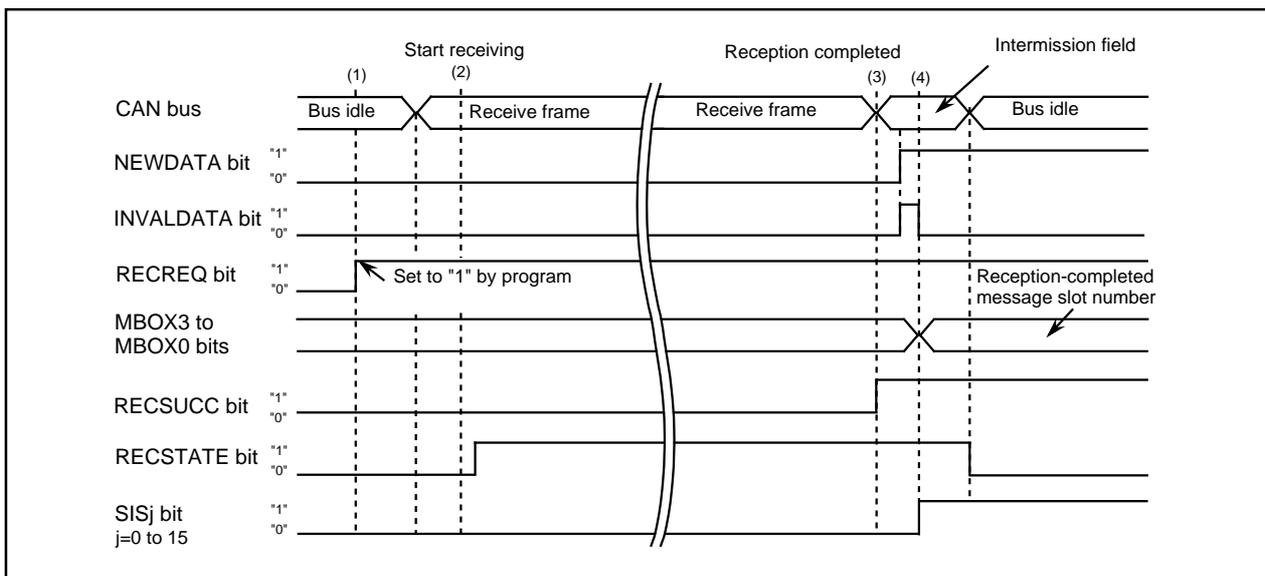


Figure 23.39 Example of CAN Data Frame Receive Operation

23.3.4 CAN Bus Error Timing

Figure 23.40 shows an operation example of when a CAN bus error occurs.

- (1) When a CAN bus error is detected, the STATE_BUSERROR bit in the C0STR register is set to "1", (error occurred) and the BEIS bit in the C0EISTR register is set to "1" (interrupt requested). The CAN starts transmitting the error frame.

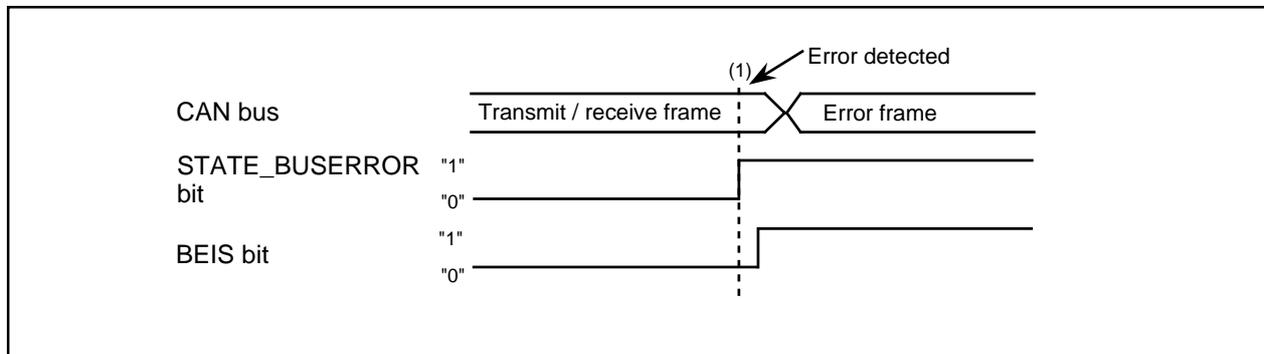


Figure 23.40 Operation Timing when CAN Bus Error Occurs

23.4 CAN Interrupts

The CAN0 wake-up interrupt and CAN0j interrupts (j=0 to 2) are provided as the CAN interrupt.

23.4.1 CAN0 Wake-Up Interrupt

If P77 (CAN0IN) is used as a CAN0 input port, the CAN0 wake-up interrupt is available by using event counter mode of the timer A3 (TA3IN) that shares a pin with CAN0IN.

If P83 (CAN0IN) is used as a CAN input port, the CAN0 wake-up interrupts are available by using $\overline{\text{INT1}}$ that shares a pin with CAN0IN.

23.4.2 CAN0j Interrupts

Figure 23.41 shows a block diagram of the CAN0j interrupts. The followings cause the CAN-associated interrupt request to be generated.

- The CAN0 slot k (k=0 to 15) completes a transmission
- The CAN0 slot k completes a reception
- The CAN0 module detects a bus error
- The CAN0 module moves into an error-passive state
- The CAN0 module moves into a bus-off state

The INTSEL bit in the C0CTRL1 register determines how an interrupt request is generated. When the INTSEL bit is set to "0", one of the above CAN0 interrupt request source causes the CAN0j interrupts to be generated by the OR circuit. When the INTSEL bit is set to "1", CAN0 transmission completed, CAN0 reception completed and CAN0 errors (CAN0 bus error detection, CAN0 module into error-passive state and CAN0 module into bus-off state) cause the CAN0j interrupt corresponding to each source to be generated.

23.4.2.1 When the INTSEL Bit is Set to "0"

If the CAN-associated interrupt is generated by one of the interrupt request source listed in **23.4.2 CAN0j Interrupts**, the corresponding bit in the C0SISTR register is set to "1" (interrupt requested) when the CAN0 slot k completes a transmission or a reception. The corresponding bit in the C0EISTR register is set to "1" (interrupt requested) when the CAN0 module detects a bus error, moves into an error-passive state, or moves into a bus-off state.

The CAN0 interrupt request signal is set to "1" when the corresponding bit in the C0SISTR or C0EISTR is set to "1" and the corresponding bit in the C0SIMKR or C0EIMKR is set to "1"

When the CAN0 interrupt request signal changes "0" to "1", all CAN0jR bits (j=0 to 2) in the IIO9IR to IIO11IR registers are set to "1" (interrupt requested).

If at least one of the CAN0jE bits in the IIO9IE to IIO11IE registers is set to "1" (interrupt enabled), the IR bits in the corresponding CAN0IC to CAN2IC registers are set to "1" (interrupt requested). The CAN0 interrupt request signal remains set to "1" if another interrupt request source causes a corresponding bit in the C0SISTR or C0EISTR to be set to "1" and the corresponding bit in the C0SIMKR or C0EIMKR to be set to "1" after the CAN0 interrupt request signal changes "0" to "1". The CAN0jR and IR bits also remain unchanged.

Bits in the C0SISTR or C0EISTR register and CAN0jR bits (j=0 to 2) in the IIO9IR to IIO11IR registers are not set to "0" automatically, interrupt acknowledgment notwithstanding. Set these bits to "0" by program.

The CAN0 interrupts are acknowledged when the CAN0jR bit in the IIO9IR to IIO11IR register and the corresponding bit in the C0SISTR or C0EISTR register are set to "0". If these bits remain set to "1", all CAN-associated interrupt request source become invalid.

23.4.2.2 When the INTSEL Bit is Set to "1"

If the CAN-associated interrupt is generated by one of the interrupt request source listed in **23.3.2 CAN0j Interrupts**, the corresponding bit in the C0SISTR register is set to "1" (interrupt requested) when the CAN0 slot k completes a transmission or a reception. The corresponding bit in the C0EISTR register is set to "1" (interrupt requested) when the CAN0 module detects a bus error, goes into an error-passive state, or goes into a bus-off state.

The CAN0 receive interrupt request signal is set to "1" if the corresponding bit in the C0SIMKR register is set to "1" (interrupt request enabled) and the corresponding bit in the C0SISTR register is set to "1" when the CAN0 module completes a reception.

The CAN0 transmit interrupt request signal is set to "1" if the corresponding bit in the C0SIMKR register is set to "1" and the corresponding bit in the C0SISTR register is set to "1" when the CAN0 module completes a transmission.

The CAN0 error interrupt request signal is set to "1" if corresponding bits in the C0EIMKR register are set to "1" and the corresponding bit in the C0EISTR register is set to "1" when the CAN0 module detects a bus error, goes into an error-passive state, or goes into a bus-off state.

When the CAN0 receive interrupt request signal changes "0" to "1", the CAN00R bit in the IIO9IR register is set to "1" (interrupt requested). If the CAN00E in the IIO9IE register is set to "1" (interrupt enabled), the IR bit in the CAN0IC register is set to "1" (interrupt requested).

When the CAN0 transmit interrupt request signal changes "0" to "1", the CAN01R bit in the IIO10IR register is set to "1" (interrupt requested). If the CAN01E in the IIO10IE register is set to "1" (interrupt enabled), the IR bit in the CAN1IC register is set to "1" (interrupt requested).

When the CAN0 error interrupt request signal changes "0" to "1", the CAN02R bit in the IIO11IR register is set to "1" (interrupt requested). If the CAN02E in the IIO11IE register is set to "1" (interrupt enabled), the IR bit in the CAN2IC register is set to "1" (interrupt requested).

The CAN0 error interrupt request signal remains set to "1" if another interrupt request causes the corresponding bit in the C0EIMKR register is set to "1" and the corresponding bit in the C0EISTR to be set to "1" after the CAN0 error interrupt request signal changes "0" to "1". The CAN02R and IR bits also remain unchanged.

Bits in the C0SISTR or C0EISTR register and CAN0jR bits (j=0 to 2) in the IIO9IR to IIO11IR registers are not set to "0" automatically, interrupt acknowledgment notwithstanding. Set these bits to "0" by program.

The CAN0 receive interrupt and CAN0 transmit interrupt are acknowledged when the CAN00R bit in the IIO9IR register and the CAN01R bit in the IIO10IR register are set to "0". Corresponding bits in the C0SISTR register can be set to either "0" or "1".

The CAN0 error interrupt is acknowledged when the CAN02R bit in the IIO11IR register and corresponding bits in the C0EISTR register are set to "0".

If these bits remain set to "1", all CAN-associated interrupt request source become invalid.

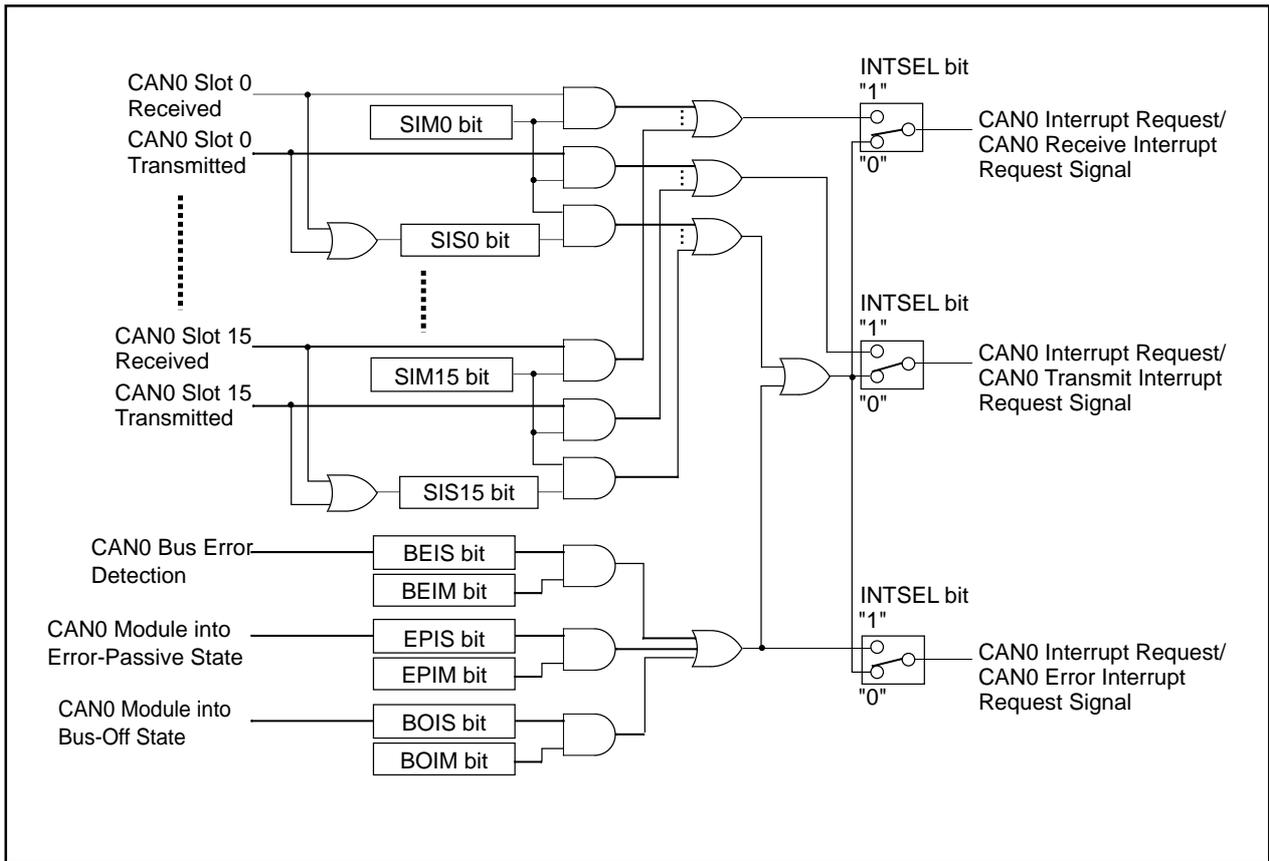


Figure 23.41 CAN Interrupts

24. Programmable I/O Ports

87 programmable I/O ports from P0 to P10 (excluding P85) are available in the 100-pin package and 123 programmable I/O ports from P0 to P15 (excluding P85) are in the 144-pin package. The direction registers determine each port status, input or output. The pull-up control registers determine whether the ports, divided into groups of four ports, are pulled up or not. P85 is an input port and no pull-up for this port is allowed. The P8_5 bit in the P8 register indicates an $\overline{\text{NMI}}$ input level since P85 shares pins with $\overline{\text{NMI}}$.

Figures 24.1 to 24.4 show programmable I/O port configurations.

Each pin functions as the programmable I/O port, an I/O pin for internal peripheral functions or the bus control pin.

To use the pins as input or output pins for internal peripheral functions, refer to the explanations for each function. Refer to **8. Bus** when used as the bus control pin.

The registers associated with the programmable I/O ports are as follows.

24.1 Port Pi Direction Register (PDi Register, i=0 to 15)

Figure 24.5 shows the PDi register.

The PDi register selects input or output status of a programmable I/O port. Each bit in the PDi register corresponds to a port.

In memory expansion and microprocessor mode, the PDi register cannot control pins being used as bus control pins (A0 to A22, $\overline{\text{A23}}$, D0 to D15, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{WRL/WR}}$, $\overline{\text{WRH/BHE}}$, $\overline{\text{RD}}$, BCLK/ALE/CLKOUT, $\overline{\text{HLDA/ALE}}$, $\overline{\text{HOLD}}$, ALE and $\overline{\text{RDY}}$). No bit controlling P85 is provided in the direction registers.

24.2 Port Pi Register (Pi Register, i=0 to 15)

Figure 24.6 shows the Pi register.

The Pi register writes and reads data to communicate with external devices. The Pi register consists of a port latch to hold output data and a circuit to read pin states. Each bit in the Pi register corresponds to a port. In memory expansion and microprocessor mode, the Pi register cannot control pins being used as bus control pins (A0 to A22, $\overline{\text{A23}}$, D0 to D15, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{WRL/WR}}$, $\overline{\text{WRH/BHE}}$, $\overline{\text{RD}}$, BCLK/ALE/CLKOUT, $\overline{\text{HLDA/ALE}}$, $\overline{\text{HOLD}}$, ALE and $\overline{\text{RDY}}$).

24.3 Function Select Register Aj (PSj Register) (j=0 to 3, 5, 8, 9)

Figures 24.7 to 24.10 show the PSj registers.

The PSj register selects either I/O port or peripheral function output if an I/O port shares pins with a peripheral function output (excluding DA0 and DA1.)

When multiple peripheral function outputs are assigned to a pin, set the PSL0 to PSL3, PSC, PSC2, PSC3 and PSD1 registers to select which function is used.

Tables 24.3 to 24.10 list peripheral function output control settings for each pin.

24.4 Function Select Register B0 to B3 (PSL0 to PSL3 Registers)

Figures 24.11 and 24.12 show the PSL0 to PSL3 registers.

When multiple peripheral function outputs are assigned to a pin, the PSL0 to PSL3 registers select which peripheral function output is used.

Refer to **24.10 Analog Input and Other Peripheral Function Input** for the PSL3_6 to PSL3_3 bits in the PSL3 register.

24.5 Function Select Register C (PSC, PSC2, PSC3 Registers)

Figures 24.13 and 24.14 show the PSC, PSC2 and PSC3 registers.

When multiple peripheral function outputs are assigned to a pin, the PSC register, the PSC2 register and the PSC3 register select which peripheral function output is used.

Refer to **24.10 Analog Input and Other Peripheral Function Input** for the PSC_7 bit in the PSC register.

24.6 Function Select Register D (PSD1 Register)

Figure 24.14 shows the PSD1 register.

When multiple peripheral function outputs are assigned to a pin, the PSD1 register selects which peripheral function output is used.

24.7 Pull-up Control Register 0 to 4 (PUR0 to PUR4 Registers)

Figures 24.15 and 24.16 show the PUR0 to PUR4 registers.

The PUR0 to PUR4 registers select whether the ports, divided into groups of four ports, are pulled up or not. Ports with bits in the PUR0 to PUR4 registers set to "1" (pull-up) and the direction registers set to "0" (input mode) are pulled up.

Set bits in the PUR0 and PUR1 registers in P0 to P5, running as bus, to "0" (no pull-up) in memory expansion mode and microprocessor mode. P0, P1 and P40 to P43 can be pulled up when they are used as input ports in memory expansion mode and microprocessor mode.

24.8 Port Control Register (PCR Register)

Figure 24.17 shows the PCR register.

The PCR register selects either CMOS output or N-channel open drain output as the P1 output format. If the PCR0 bit is set to "1", N-channel open drain output is selected because the P-channel in the CMOS port is turned off. This is, however, not a perfect open drain. Therefore, the absolute maximum rating of the input voltage is between $-0.3V$ and $V_{CC2} + 0.3V$.

If P1 is used as the data bus in memory expansion mode and microprocessor mode, set the PCR0 bit to "0".

If P1 is used as a port in memory expansion mode and microprocessor mode, the PCR0 bit determines the output format.

24.9 Input Function Select Register (IPS and IPSA Registers)

Figures 24.17 and 24.18 show the IPS and IPSA registers.

The IPS3, IPS1 and IPS0 bits in the IPS register and the IPSA_0 bit in the IPSA register select which pin is assigned for the intelligent I/O or CAN input functions.

Refer to **24.10 Analog Input and Other Peripheral Function Input** for the IPS2 bit.

24.10 Analog Input and Other Peripheral Function Input

The PSL3_6 to PSL3_3 bits in the PSL3 register, the PSC_7 bit in the PSC register and the IPS2 bit in the IPS register each separate analog I/O ports from other peripheral functions. Setting the corresponding bit to "1" (analog I/O) to use the analog I/O port (DA0, DA1, ANEX0, ANEX1, AN4 to AN7 or AN150 to AN157) prevents an intermediate potential from being impressed to other peripheral functions. The impressed intermediate potential may cause increase in power consumption.

Set the corresponding bit to "0" (except analog I/O) when analog I/O is not used. All peripheral function inputs except the analog I/O port are available when the corresponding bit is set to "0". These inputs are indeterminate when the bit is set to "1". When the PSC_7 bit is set to "1", key input interrupt request remains unchanged regardless of $\overline{KI0}$ to $\overline{KI3}$ pin input level change.

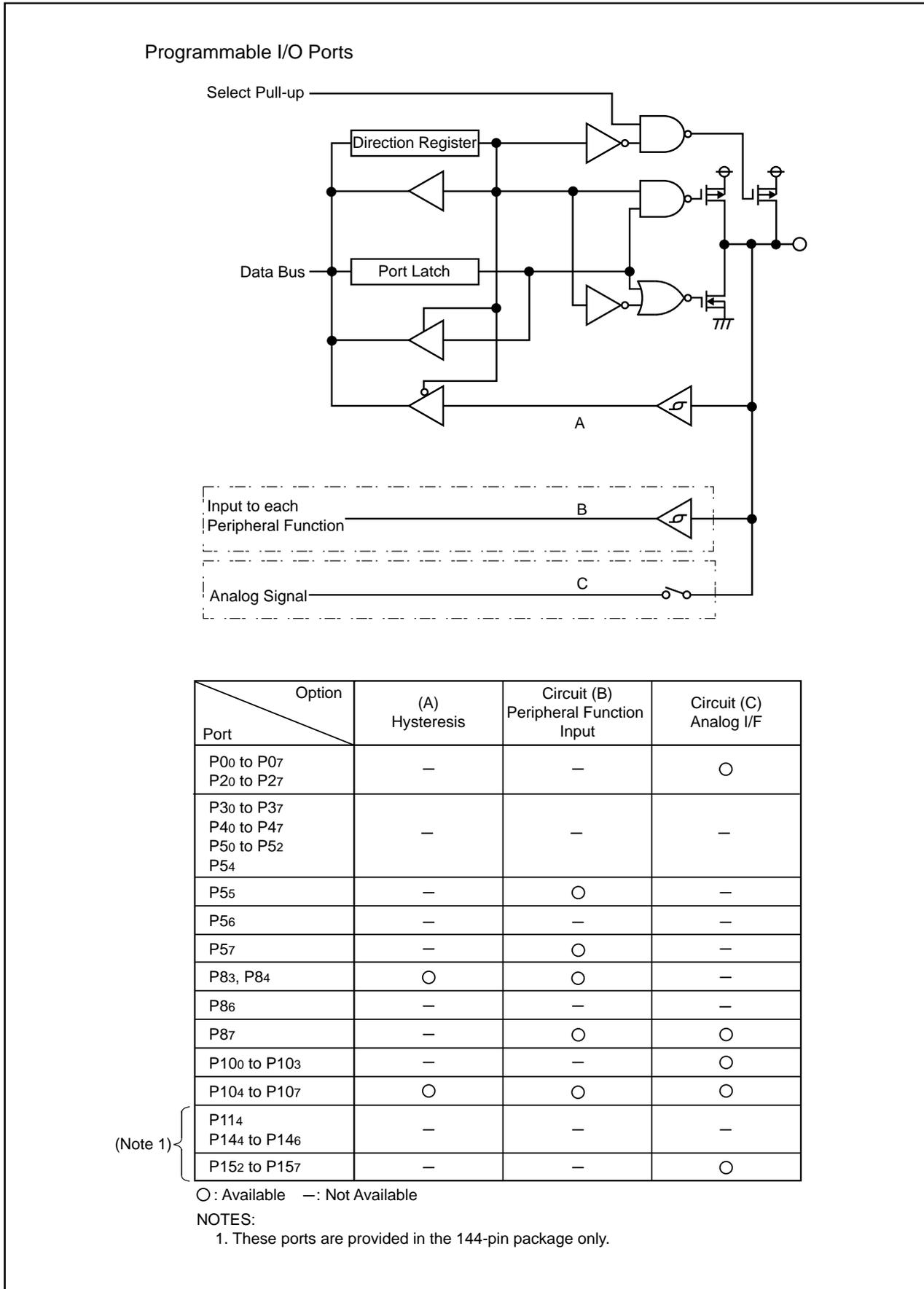


Figure 24.1 Programmable I/O Ports (1)

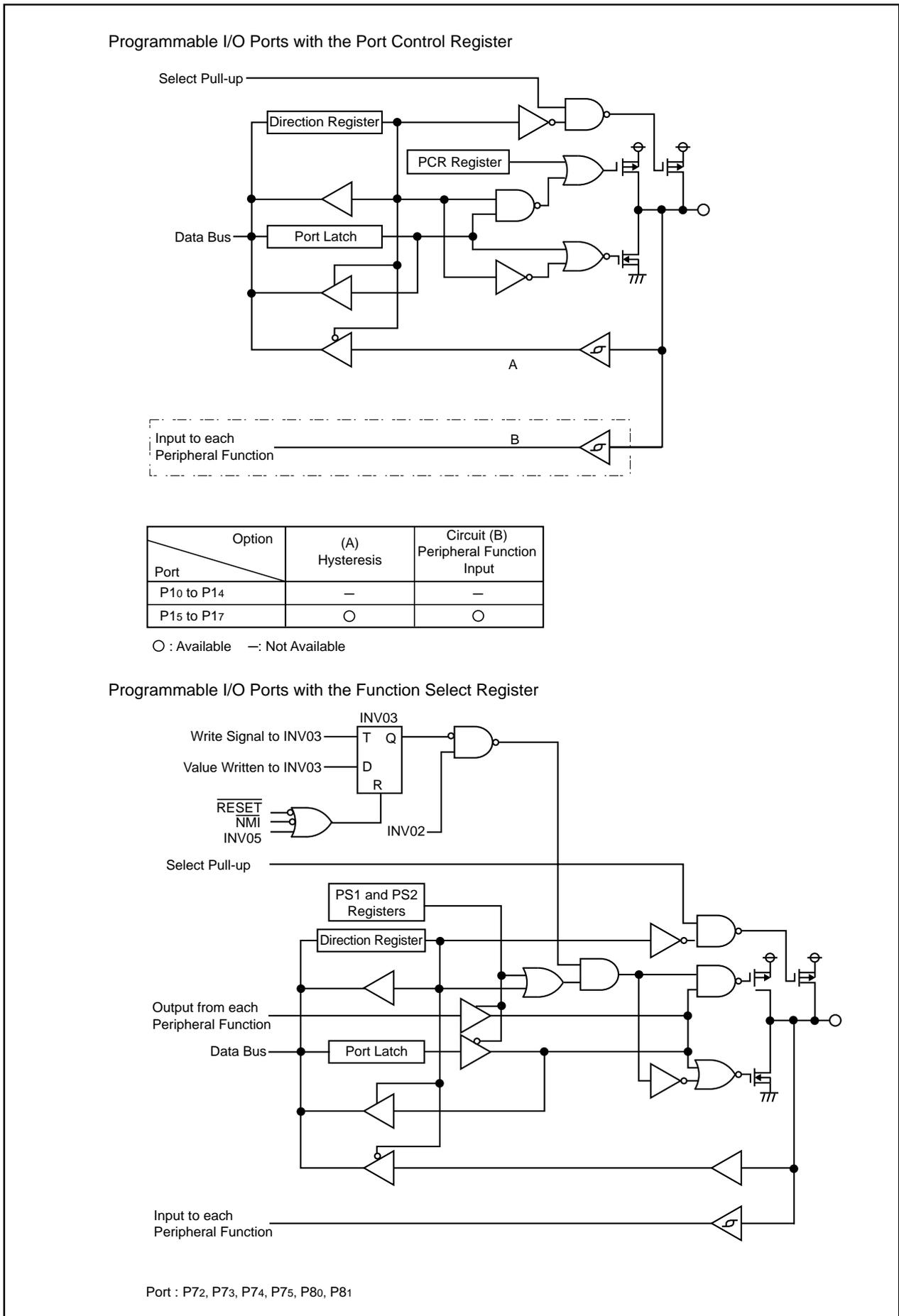


Figure 24.2 Programmable I/O Ports (2)

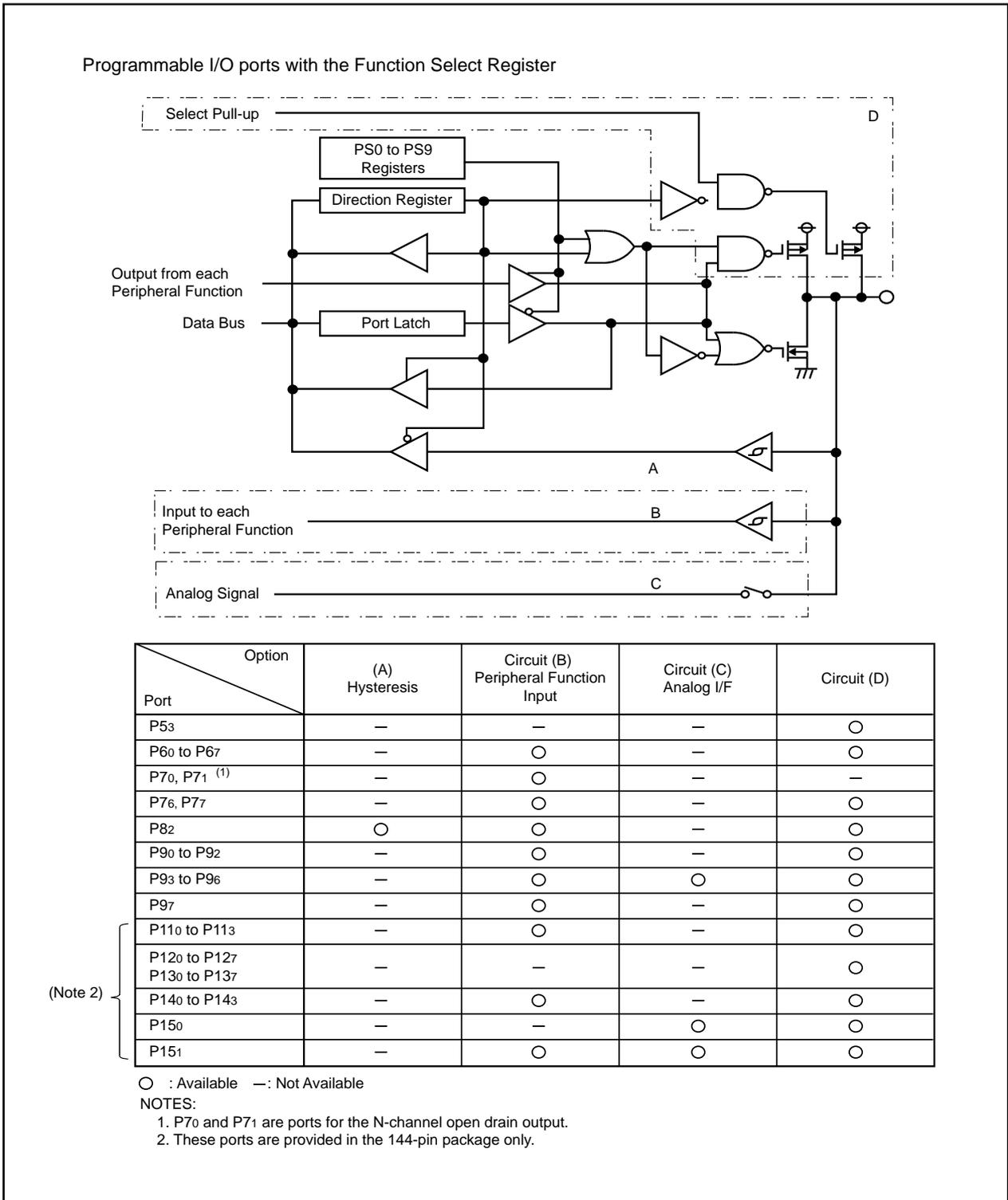


Figure 24.3 Programmable I/O Ports (3)

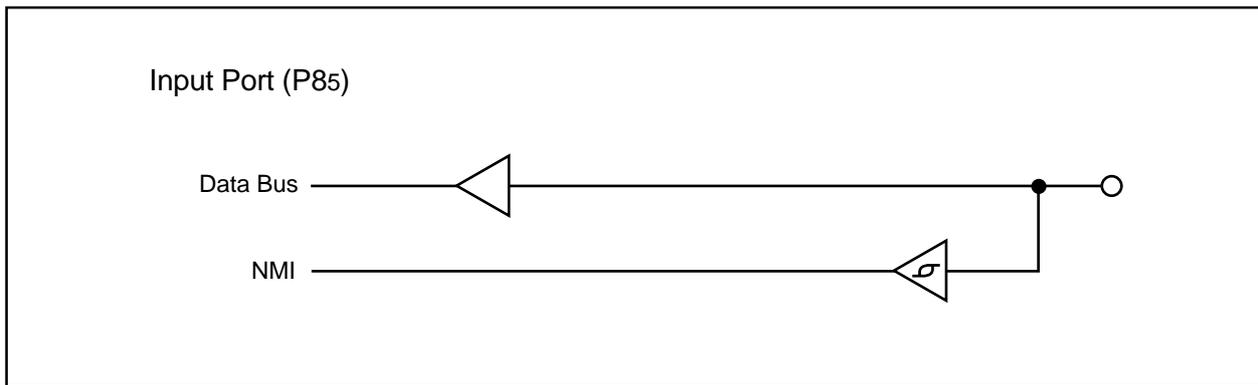


Figure 24.4 Programmable I/O Ports (4)

Port Pi Direction Register (i=0 to 15) (2)

Symbol	Address	After Reset
PD0 to PD3	03E2 ₁₆ , 03E3 ₁₆ , 03E6 ₁₆ , 03E7 ₁₆	00 ₁₆
PD4 to PD7	03EA ₁₆ , 03EB ₁₆ , 03C2 ₁₆ , 03C3 ₁₆	00 ₁₆
PD8	03C6 ₁₆ ⁽⁴⁾	00X0 0000 ₂
PD9 to PD10	03C7 ₁₆ ⁽¹⁾ , 03CA ₁₆	00 ₁₆
PD11	03CB ₁₆ ^(3, 4)	XXX0 0000 ₂
PD12 to PD13	03CE, 03CF ₁₆ ⁽³⁾	00 ₁₆
PD14	03D2 ₁₆ ^(3, 4)	X000 0000 ₂
PD15	03D3 ₁₆ ⁽³⁾	00 ₁₆

Bit Symbol	Bit Name	Function	RW
PD _i _0	Port Pi0 Direction Bit	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PD _i _1	Port Pi1 Direction Bit	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PD _i _2	Port Pi2 Direction Bit	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PD _i _3	Port Pi3 Direction Bit	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PD _i _4	Port Pi4 Direction Bit	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PD _i _5	Port Pi5 Direction Bit	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PD _i _6	Port Pi6 Direction Bit	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW
PD _i _7	Port Pi7 Direction Bit	0 : Input mode (Functions as input port) 1 : Output mode (Functions as output port)	RW

NOTES:

- Set the PD9 register immediately after the PRC2 bit in the PRCR register is set to "1" (write enable). Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the instruction to set the PD9 register.
- In memory expansion mode and microprocessor mode, the PD_i register cannot control pins being used as bus control pins (A₀ to A₂₂, A₂₃, D₀ to D₁₅, CS₀ to CS₃, WRL/WR, WRH/BHE, BCLK/ALE/CLK_{OUT}, RD, HLDA/ALE, HOLD, ALE and RDY). M32C/84T cannot be used in memory expansion mode and microprocessor mode.
- Set the PD11 to PD15 registers to "FF₁₆" in the 100-pin package.
- Nothing is assigned in the PD8_5 bit in the PD8 register, the PD11_7 to PD11_5 bits in the PD11 register (144-pin package only) and the PD14_7 bit in the PD14 register (144-pin package only). If write, set these bits to "0". When read, their contents are indeterminate.

Figure 24.5 PD0 to PD15 Registers

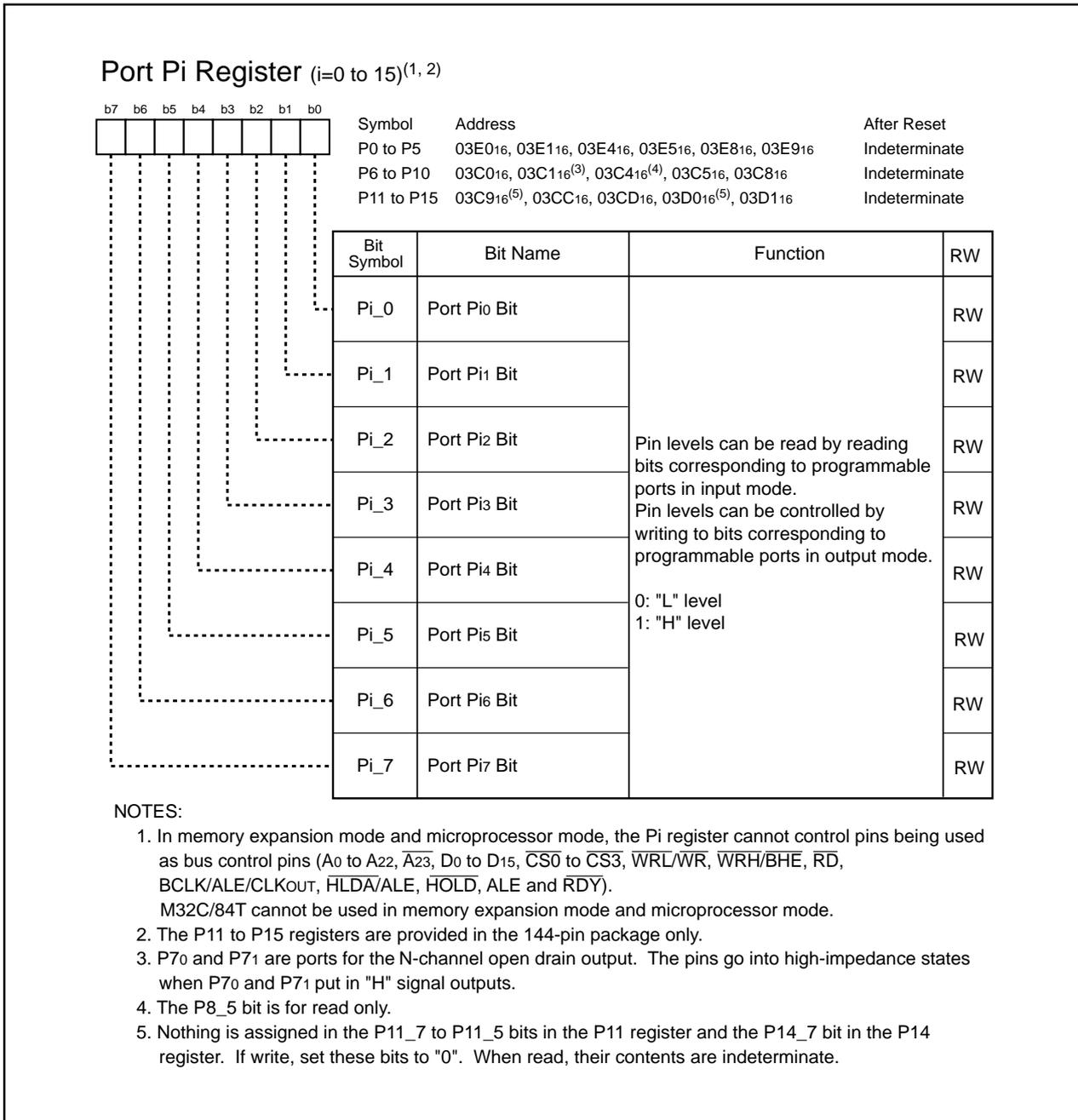


Figure 24.6 P0 to P15 Registers

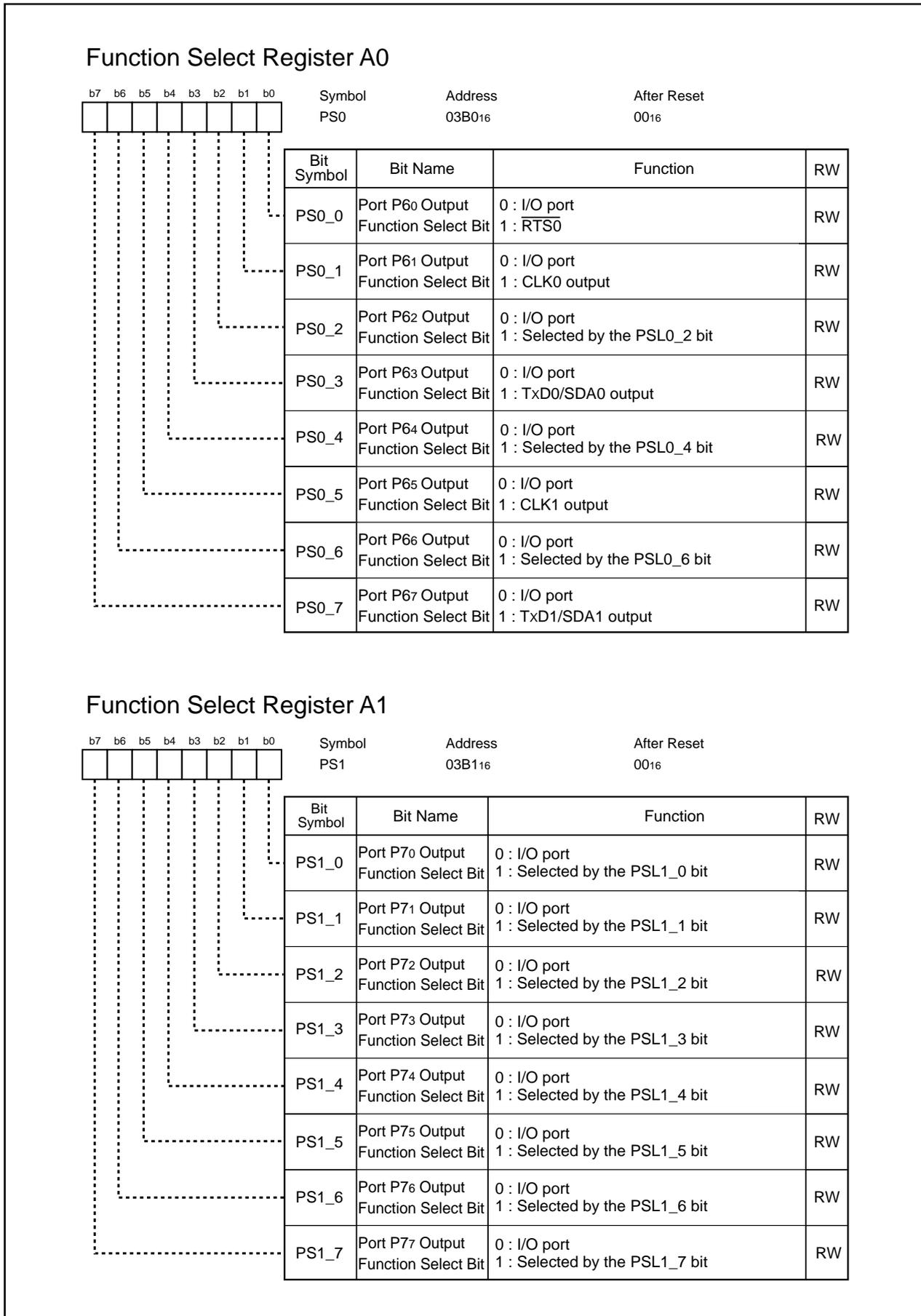


Figure 24.7 PS0 Register and PS1 Register

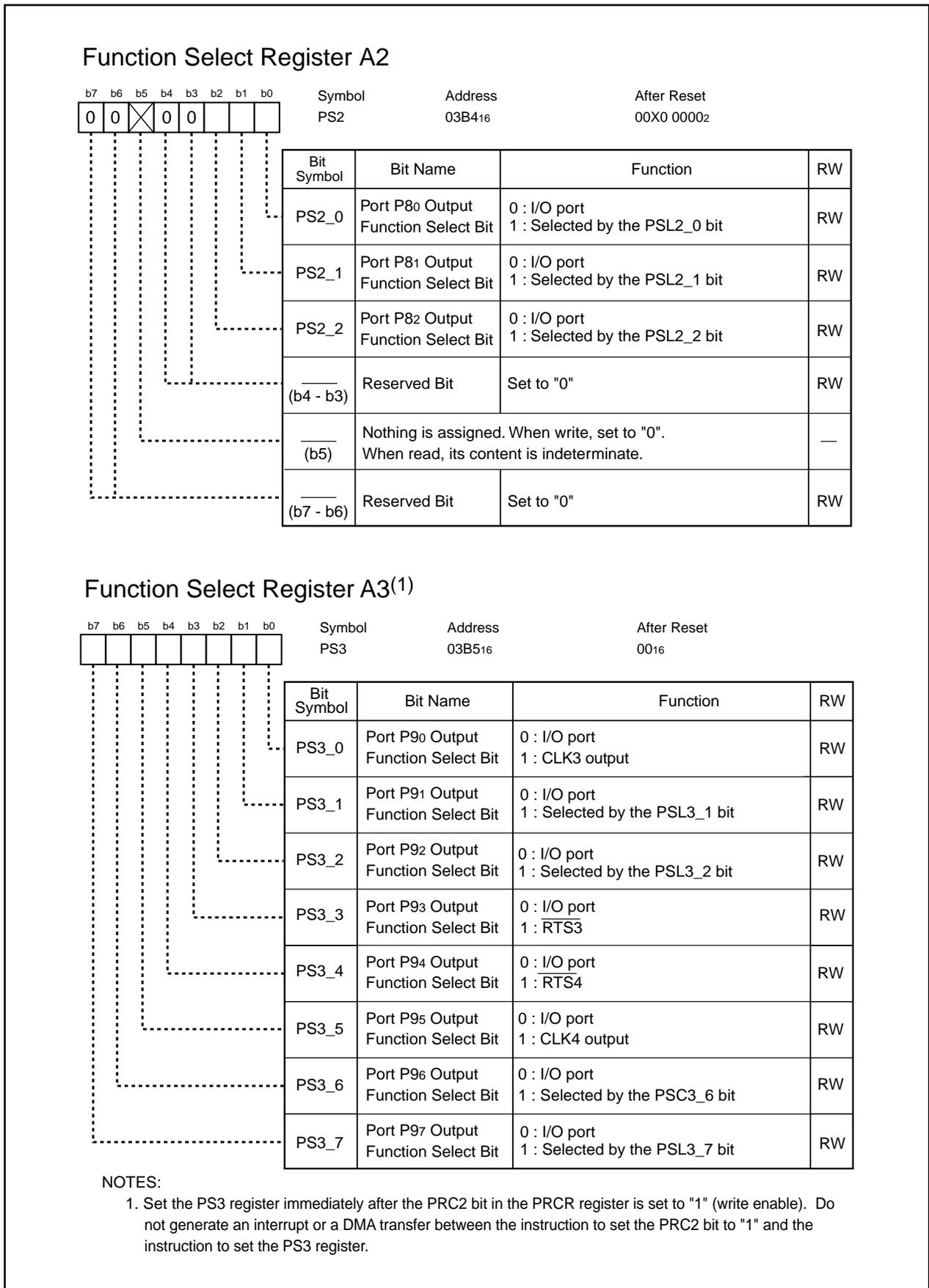


Figure 24.8 PS2 Register and PS3 Register

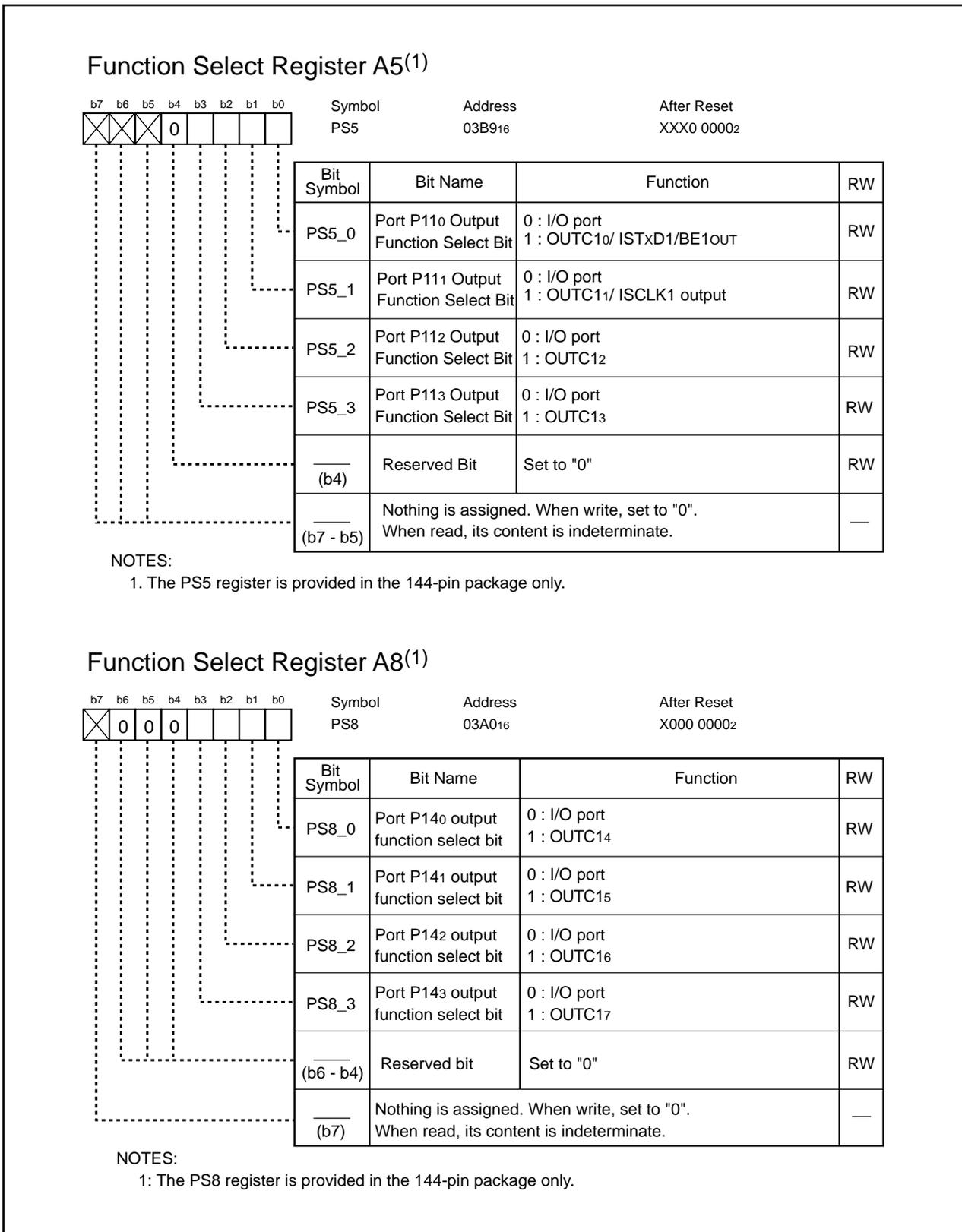
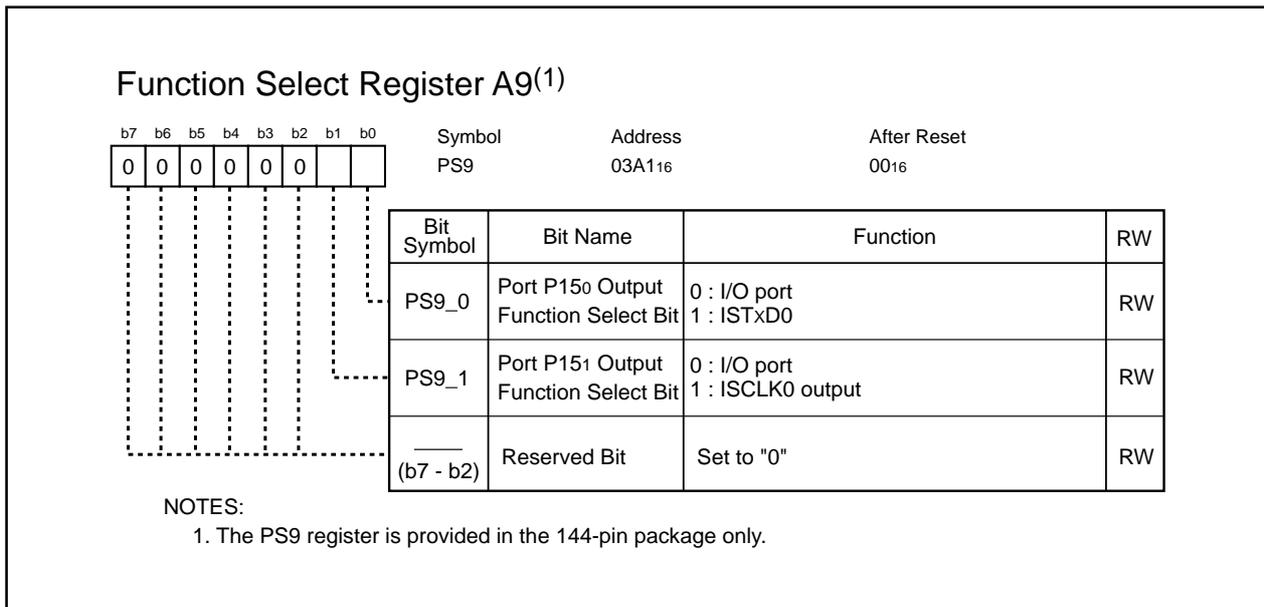


Figure 24.9 PS5 Register and PS8 Register

**Figure 24.10 PS9 Register**

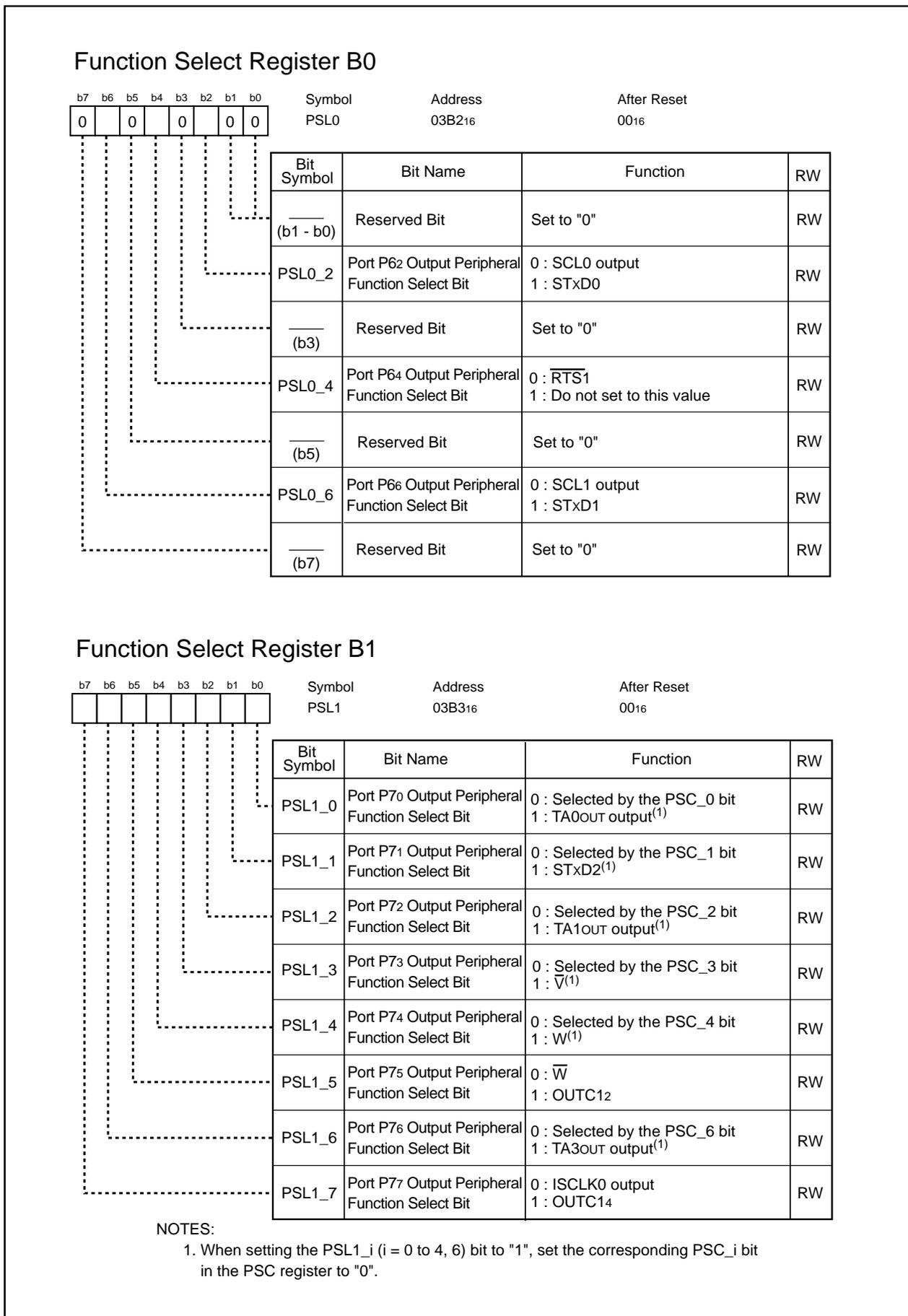


Figure 24.11 PSL0 Register and PSL1 Register

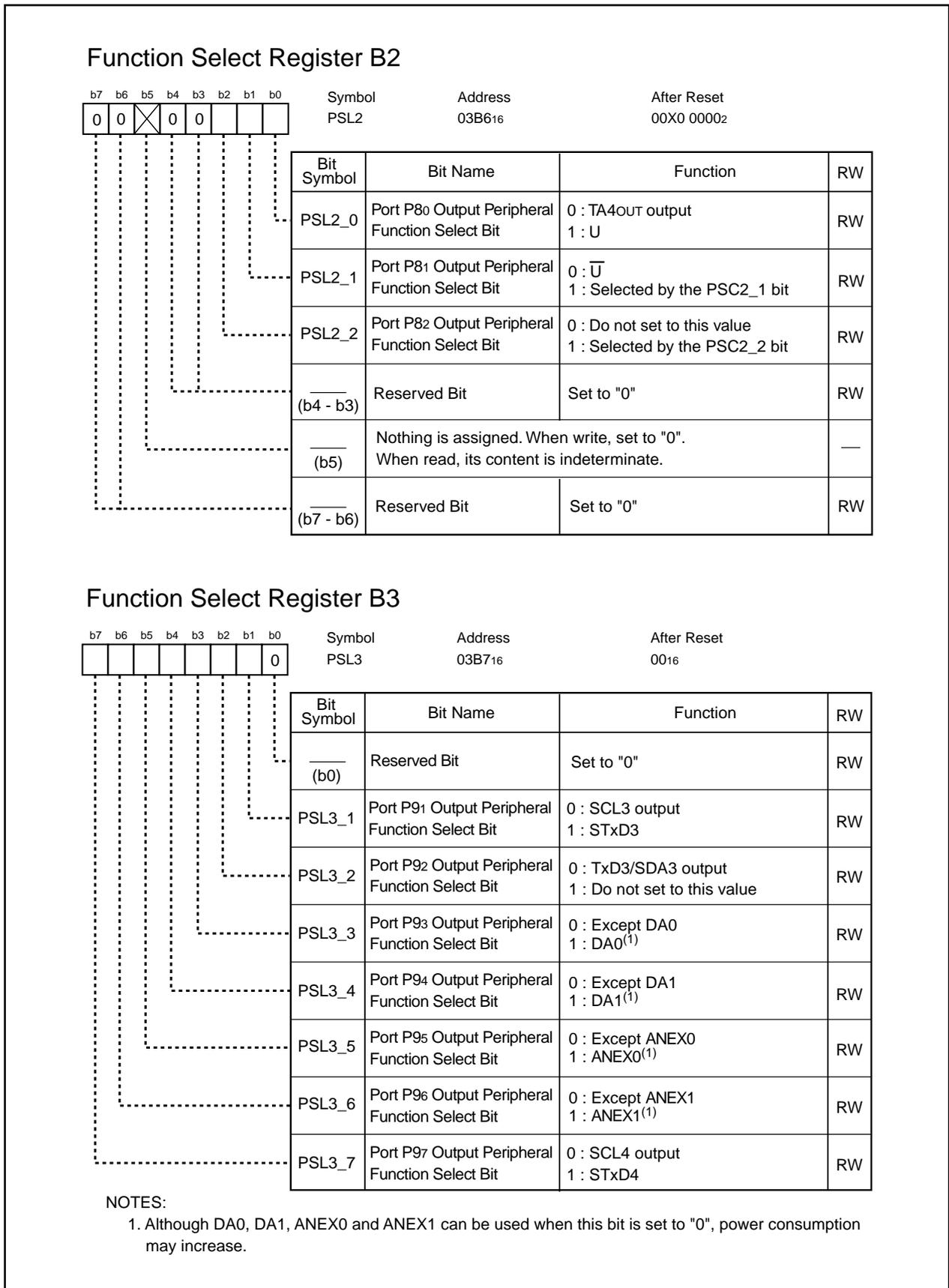


Figure 24.12 PSL2 Register and PSL3 Register

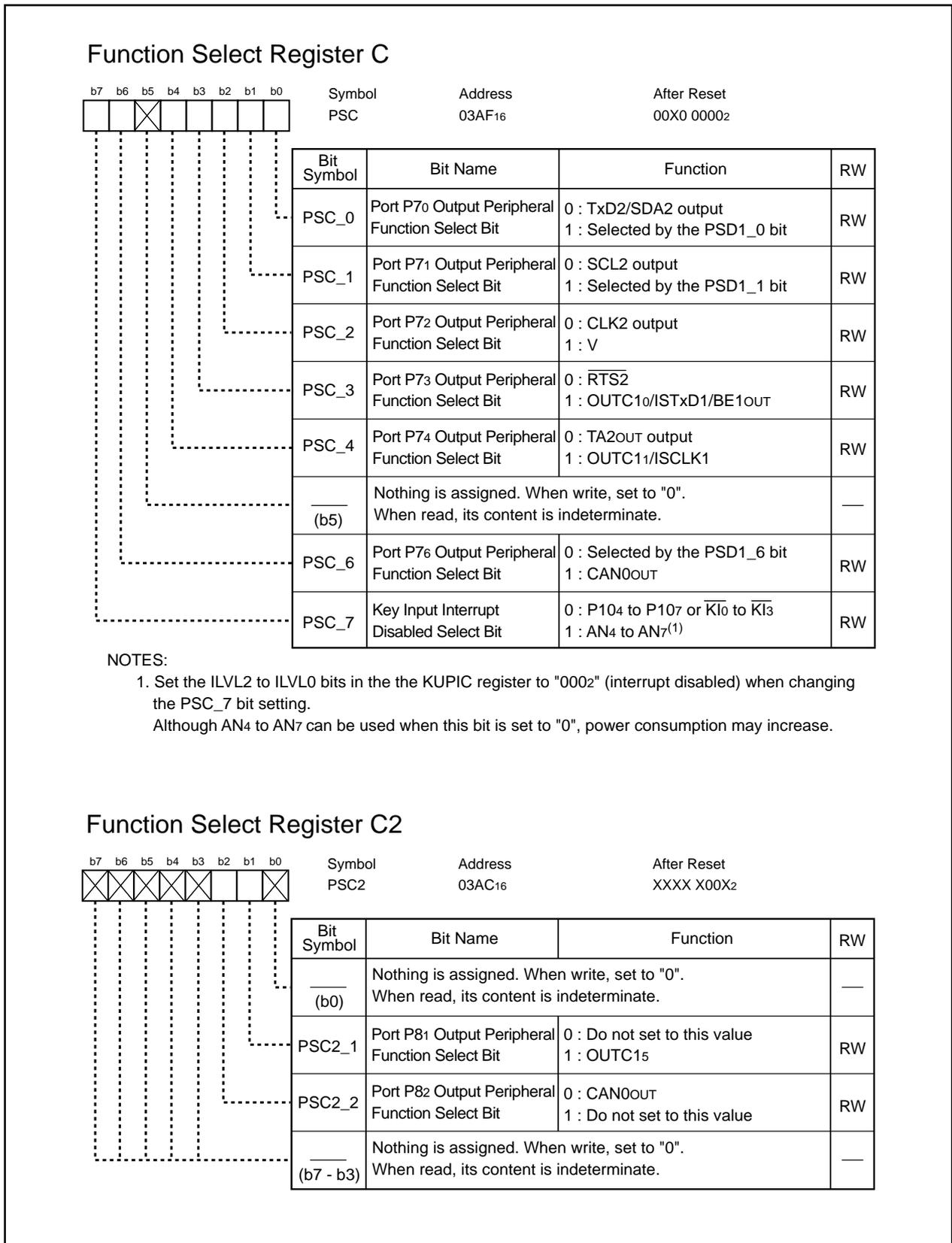


Figure 24.13 PSC Register and PSC2 Register

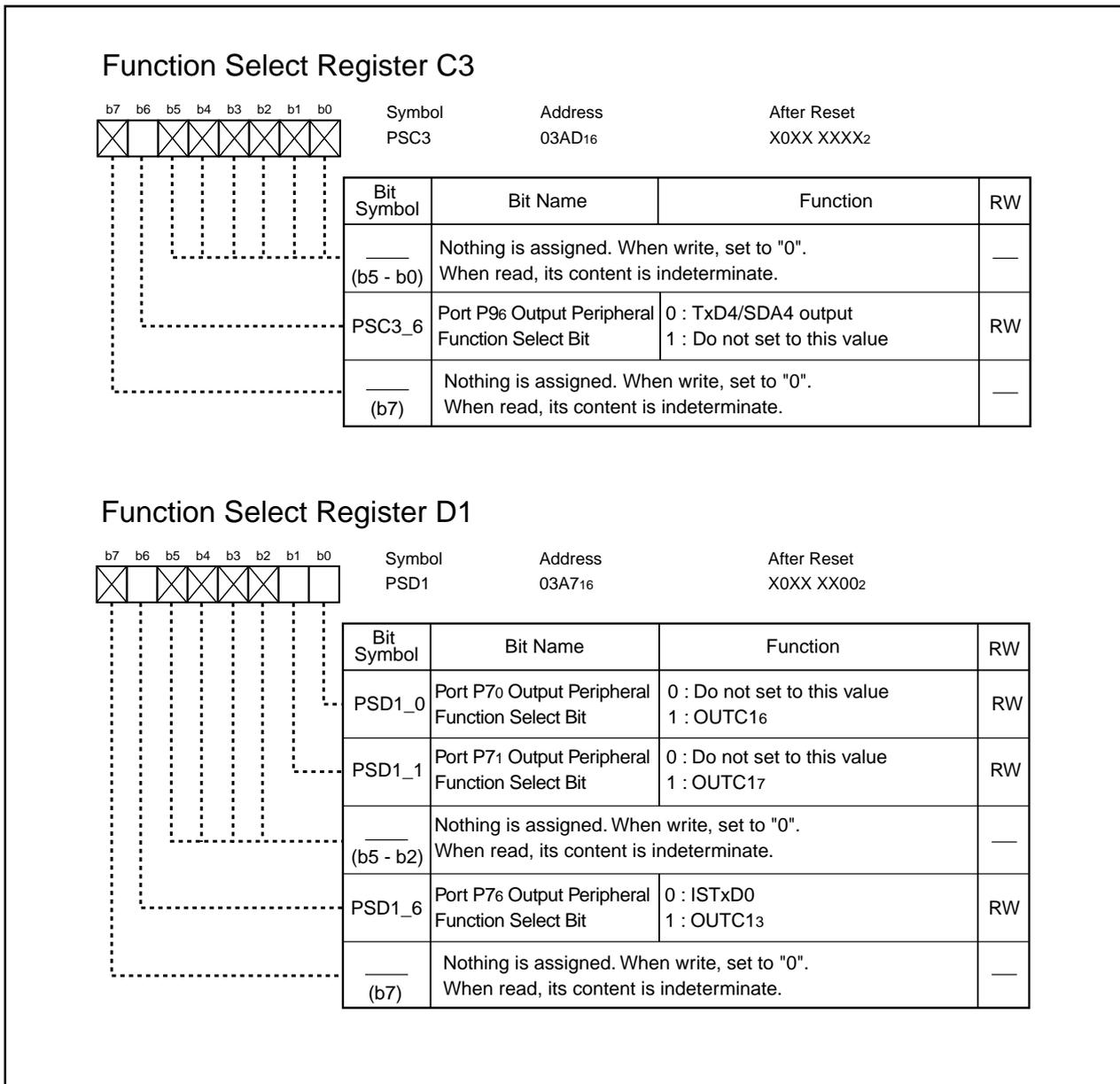


Figure 24.14 PSC3 Register and PSD1 Register

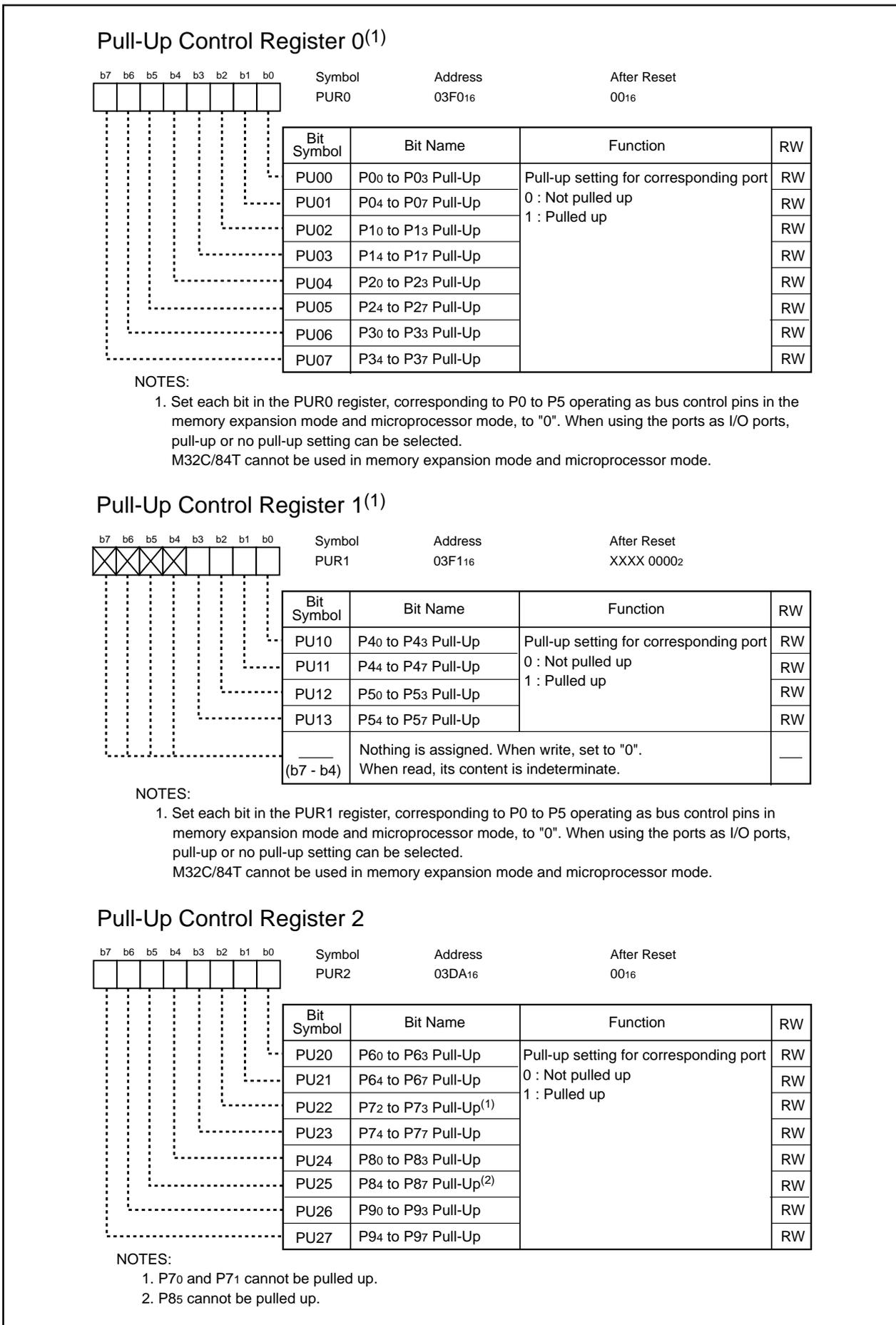


Figure 24.15 PUR0 Register, PUR1 Register and PUR2 Register

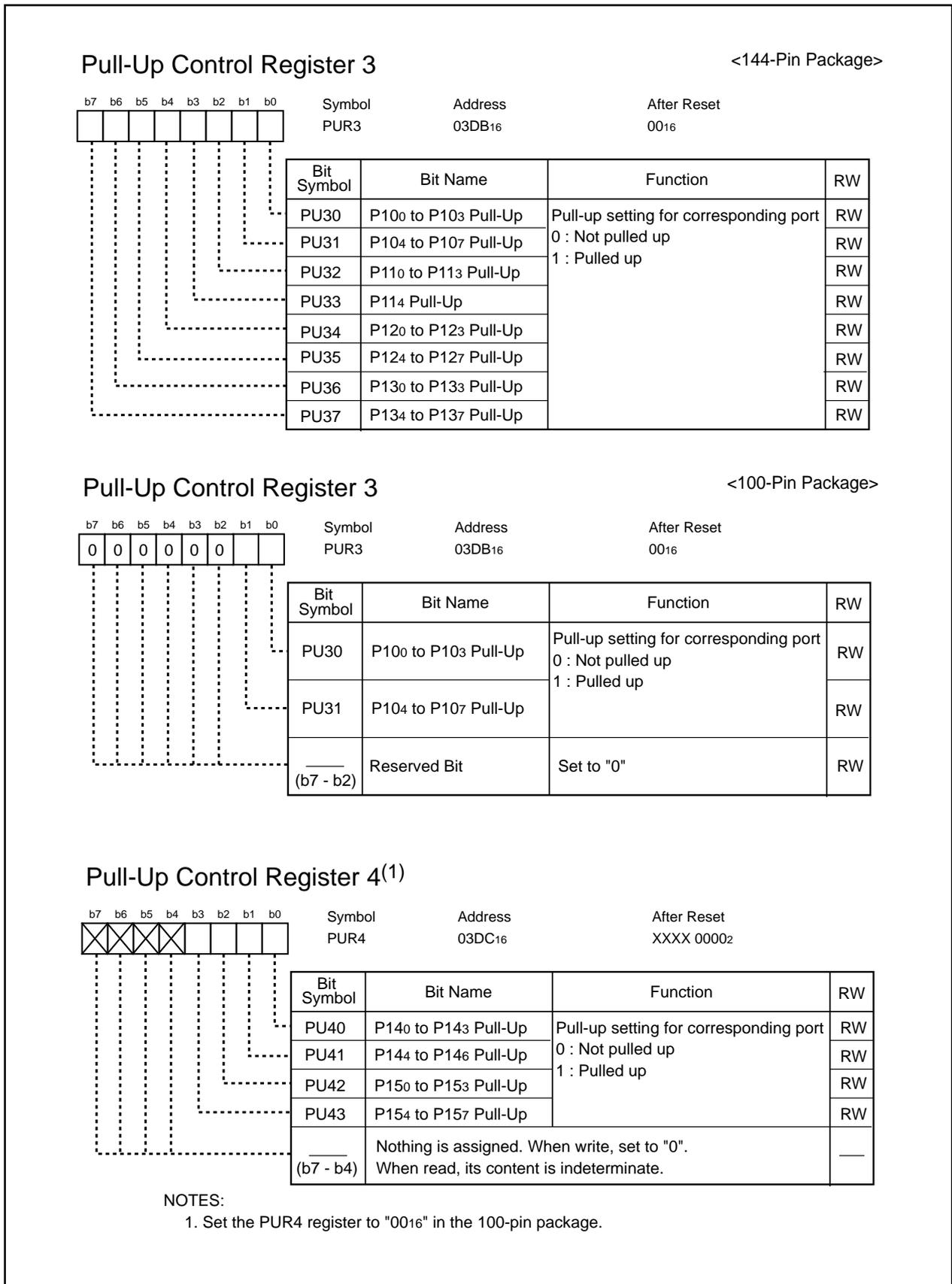


Figure 24.16 PUR3 Register and PUR4 Register

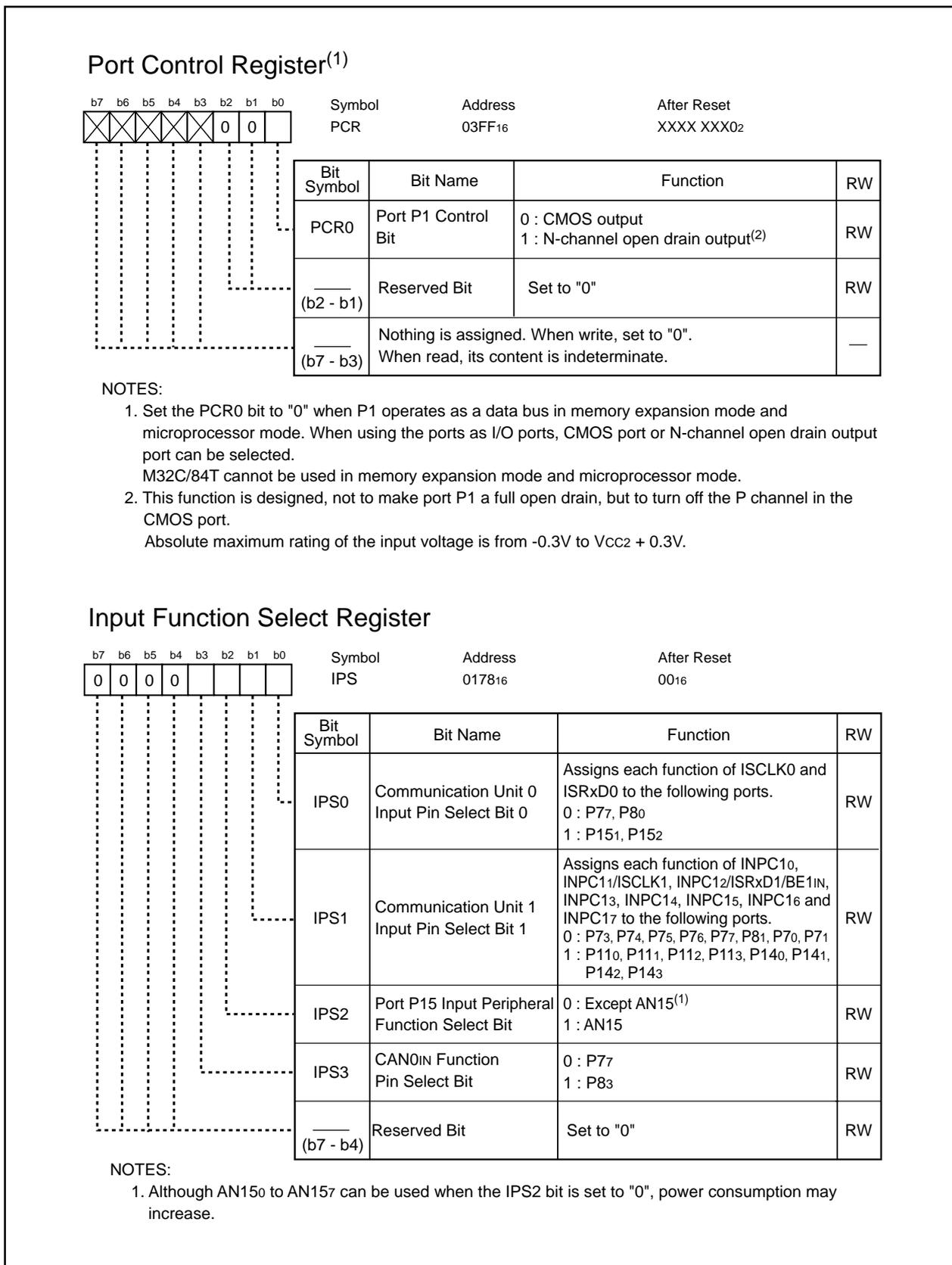


Figure 24.17 PCR Register and IPS Register

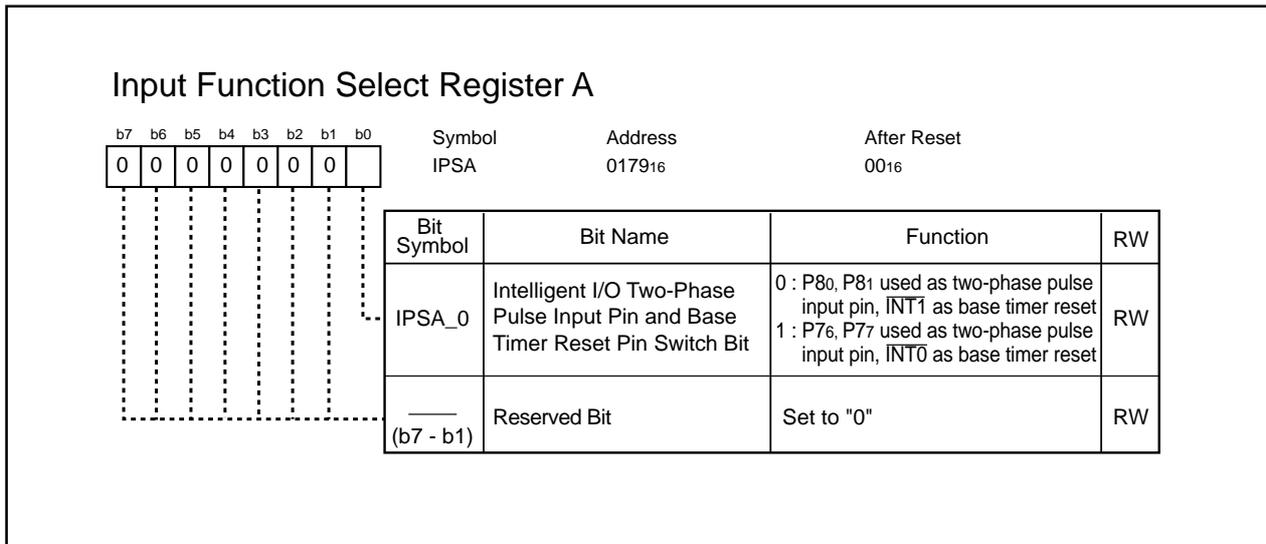


Figure 24.18 IPSA Register

Table 24.1 Unassigned Pin Settings in Single-Chip Mode

Pin Name	Setting
P0 to P15 (excluding P85) ^(1,2,3,4,6)	Enter input mode and connect each pin to VSS via a resistor (pull-down); or enter output mode and leave the pins open
XOUT ⁽⁵⁾	Leave pin open
NMI(P85)	Connect pin to VCC1 via a resistor (pull-up)
AVCC	Connect pin to VCC1
AVSS, VREF, BYTE	Connect pins to VSS

NOTES:

- P11 to P15 are provided in the 144-pin package only.
- If the port enters output mode and is left open, it is in input mode before output mode is entered by program after reset. While the port is in input mode, voltage level on the pins is indeterminate and power consumption may increase.
Direction register settings may be changed by noise or failure caused by noise. Configure direction register settings regularly to increase the reliability of the program.
- Use the shortest possible wiring to connect the microcomputer pins to unassigned pins (within 2 cm).
- P70 and P71 must put in low-level ("L") signal outputs if they are in output mode. They are N-channel open-drain outputs.
- When the external clock is applied to the XIN pin, set the pin as written above.
- In the 100-pin package, set "FF16" in the following addresses, in addition to the above settings:
Addresses 0003CB16, 0003CE16, 0003CF16, 0003D216, 0003D316

Table 24.2 Unassigned Pin Setting in Memory Expansion Mode and Microprocessor Mode

Pin Name	Setting
P6 to P15 (excluding P85) ^(1,2,3,4,6)	Enter input mode and connect each pin to VSS via a resistor (pull-down); or enter output mode and leave the pins open
BHE, ALE, HLDA, XOUT ⁽⁵⁾ , BCLK	Leave pin open
NMI(P85)	Connect pin to VCC1 via a resistor (pull-up)
RDY, HOLD	Connect pins to VCC2 via a resistor (pull-up)
AVCC	Connect pin to VCC1
AVSS, VREF	Connect pins to VSS

NOTES:

- P11 to P15 are provided in the 144-pin package only.
- If the port enters output mode and is left open, it is in input mode before output mode is entered by program after reset. While the port is in input mode, voltage level on the pins is indeterminate and power consumption may increase.
Direction register settings may be changed by noise or failure caused by noise. Configure direction register settings regularly to increase the reliability of the program.
- Use the shortest possible wiring to connect the microcomputer pins to unassigned pins (within 2 cm).
- P70 and P71 must put in low-level ("L") signal outputs if they are in output mode. They are N-channel open-drain outputs.
- When the external clock is applied to the XIN pin, set the pin as written above.
- In the 100-pin package, set "FF16" in the following addresses, in addition to the above settings:
Addresses 0003CB16, 0003CE16, 0003CF16, 0003D216, 0003D316

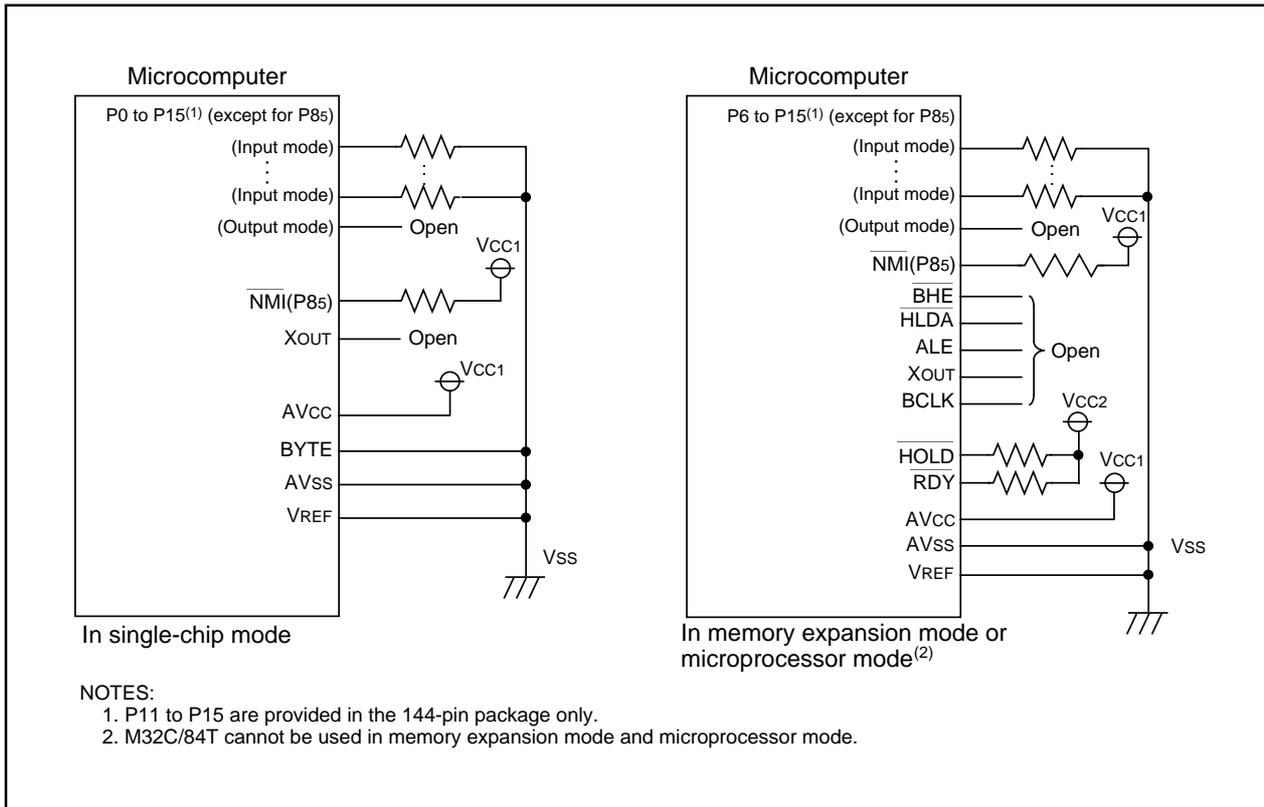


Figure 24.19 Unassigned Pin Handling

Table 24.3 Port P6 Peripheral Function Output Control

	PS0 Register	PSL0 Register
Bit 0	0: P60/CTS0/SS0 1: RTS0	Set to "0"
Bit 1	0: P61/CLK0(input) 1: CLK0(output)	Set to "0"
Bit 2	0: P62/RxD0/SCL0(input) 1: Selected by the PSL0 register	0: SCL0(output) 1: STxD0
Bit 3	0: P63/SRxD0/SDA0 (input) 1: TxD0/SDA0 (output)	Set to "0"
Bit 4	0: P64/CTS1/SS1 1: Selected by the PSL0 register	0: RTS1 1: Do not set this value
Bit 5	0: P65/CLK1(input) 1: CLK1(output)	Set to "0"
Bit 6	0: P66/RxD1/SCL1(input) 1: Selected by the PSL0 register	0: SCL1(output) 1: STxD1
Bit 7	0: P67/SRxD1/SDA1 (input) 1: TxD1/SDA1 (output)	Set to "0"

Table 24.4 Port P7 Peripheral Function Output Control

	PS1 Register	PSL1 Register	PSC Register ⁽¹⁾	PSD1 Register
Bit 0	0: P70/TA0OUT(input)/SRxD2 INPC16/SDA2 (input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: TA0OUT(output)	0: TxD2/SDA2(output) 1: Selected by the PSD1 register	0: Do not set to this value 1: OUTC16
Bit 1	0: P71/TB5IN/TA0IN/RxD2/ INPC17/SCL2 (input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: STxD2	0: SCL2(output) 1: Selected by the PSD1 register	0: Do not set to this value 1: OUTC17
Bit 2	0: P72/TA1OUT(input)/ CLK2(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: TA1OUT(output)	0: CLK2(output) 1: V	Set to "0"
Bit 3	0: P73/TA1IN/CTS2/SS2/ INPC10 1: Selected by the PSL1 register	0: Selected by the PSC register 1: \bar{V}	0: RTS2 1: OUTC10/ISTxD1/BE1OUT	Set to "0"
Bit 4	0: P74/INPC11/ISCLK1(input)/ TA2OUT(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: W	0: TA2OUT(output) 1: OUTC11/ISCLK1(output)	Set to "0"
Bit 5	0: P75/TA2IN/INPC12/ ISRxD1/BE1IN 1: Selected by the PSL1 register	0: \bar{W} 1: OUTC12	Set to "0"	Set to "0"
Bit 6	0: P76/INPC13/TA3OUT(input) 1: Selected by the PSL1 register	0: Selected by the PSC register 1: TA3OUT(output)	0: Selected by the PSD1 register 1: CAN0OUT	0: ISTxD0 1: OUTC13
Bit 7	0: P77/TA3IN/CAN0IN/ ISCLK0(input)/INPC14 1: Selected by the PSL1 register	0: ISCLK0(output) 1: OUTC14	0: P104 to P107 or K10 to K13 1: AN4 to AN7 (No relation to P77)	Set to "0"

NOTES:

1. When setting the PSL1_i bit (i=0 to 4, 6) to "1", set the corresponding PSC_i bit to "0".

Table 24.5 Port P8 Peripheral Function Output Control

	PS2 Register	PSL2 Register	PSC2 Register
Bit 0	0: P80/ISRxD0/TA4OUT(input) 1: Selected by the PSL2 register	0: TA4OUT(output) 1: U	Set to "0"
Bit 1	0: P81/TA4IN/INPC15 1: Selected by the PSL2 register	0: \bar{U} 1: Selected by the PSC2 register	0: Do not set to this value 1: OUTC15
Bit 2	0: P82/INT0 1: Selected by the PSL2 register	0: Do not set to this value 1: Selected by the PSC2 register	0: CAN0OUT 1: Do not set to this value
Bit 3 to 7	Set to "000002"		

Table 24.6 Port P9 Peripheral Function Output Control

	PS3 Register	PSL3 Register	PSC3 Register
Bit 0	0: P90/TB0IN/CLK3(input) 1: CLK3(output)	Set to "0"	Set to "0"
Bit 1	0: P91/TB1IN/RxD3/SCL3(input) 1: Selected by the PSL3 register	0: SCL3(output) 1: STxD3	Set to "0"
Bit 2	0: P92/TB2IN/SRxD3/SDA3(input) 1: Selected by the PSL3 register	0: TxD3/SDA3(output) 1: Do not set to this value	Set to "0"
Bit 3	0: P93/TB3IN/CTS3/SS3/DA0(output) 1: RTS3	0: Except DA0 1: DA0	Set to "0"
Bit 4	0: P94/TB4IN/CTS4/SS4/DA1(output) 1: RTS4	0: Except DA1 1: DA1	Set to "0"
Bit 5	0: P95/ANEX0/CLK4(input) 1: CLK4(output)	0: Except ANEX0 1: ANEX0	Set to "0"
Bit 6	0: P96/SRxD4/ANEX1/SDA4(input) 1: Selected by the PSC3 register	0: Except ANEX1 1: ANEX1	0: TxD4/SDA4 1: Do not set to this value
Bit 7	0: P97/RxD4/ \overline{ADTRG} /SCL4(input) 1: Selected by the PSL3 register	0: SCL4(output) 1: STxD4	Set to "0"

Table 24.7 Port P10 Peripheral Function Input Control

	PSC Register
Bit 7	0: P104 to P107 or $\overline{KI0}$ to $\overline{KI3}$ 1: AN4 to AN7

Table 24.8 Port P11 Peripheral Function Output Control

	PS5 Register
Bit 0	0: P110/INPC10 1: OUTC10/ISTxD1/BE1OUT
Bit 1	0: P111/INPC11/ISCLK1(input) 1: OUTC11/ISCLK1(output)
Bit 2	0: P112/INPC12/ISRxD1/BE1IN 1: OUTC12
Bit 3	0: P113/INPC13 1: OUTC13
Bit 4 to 7	Set to "00002"

Table 24.9 Port P14 Peripheral Function Output Control

	PS8 Register
Bit 0	0: P140/INPC14 1: OUTC14
Bit 1	0: P141/INPC15 1: OUTC15
Bit 2	0: P142/INPC16 1: OUTC16
Bit 3	0: P143/INPC17 1: OUTC17
Bit 4 to 7	Set to "00002"

Table 24.10 Port P15 Peripheral Function Output Control

	PS9 Register
Bit 0	0: P150/AN150 1: ISTxD0
Bit 1	0: P151/AN151/ISCLK0(input) 1: ISCLK0(output)
Bit 2 to 7	Set to "0000002"

25. Flash Memory Version

Aside from the built-in flash memory, the flash memory version microcomputer has the same functions as the masked ROM version.

In the flash memory version, rewrite operation to the flash memory can be performed in three modes: CPU rewrite mode, standard serial I/O mode and parallel I/O mode.

Table 25.1 lists specifications of the flash memory version. See **Tables 1.1 and 1.2** for the items not listed in Table 25.1.

Table 25.1 Flash Memory Version Specifications

Item		Specification
Flash Memory Operating Mode		3 modes (CPU rewrite, standard serial I/O, parallel I/O)
Erase Block	User ROM Area	See Figure 25.1
	Boot ROM Area	1 block (4 Kbytes) ⁽¹⁾
Program Method		Per word (16 bytes), per byte (8 bits) ⁽²⁾
Erase Method		All block erase, erase per block
Program and Erase Control Method		Software commands control programming and erasing on the flash memory
Protect Method		The lock bit protects each block in the flash memory
Number of Commands		8 commands
Program and Erase Endurance		100 times ⁽³⁾
Data Retention		10 years
ROM Code Protection		Standard serial I/O mode and parallel I/O mode supported

NOTES:

1. The rewrite control program for standard serial I/O mode is stored in the boot ROM area before shipment. This space can be rewritten in parallel I/O mode only.
2. Programming per byte is available in parallel I/O mode only.
3. Program and erase endurance refers to the number of times a block erase can be performed. Every block erase performed after writing data of one word or more counts as one program and erase operation.

Table 25.2 Flash Memory Rewrite Mode Overview

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	Software command execution by CPU rewrites the user ROM area. EW mode 0: Rewritable in areas other than flash memory EW mode 1: Rewritable in flash memory	A dedicated serial programmer rewrites the user ROM area. Standard serial I/O mode 1: Clock synchronous serial I/O Standard serial I/O mode 2: UART Standard serial I/O mode 3: CAN	A dedicated parallel programmer rewrites the boot ROM area and user ROM area.
Space which can be rewritten	User ROM area	User ROM area	User ROM area Boot ROM area
Operating mode	Single-chip mode Memory expansion mode (EW mode 0) Boot mode (EW mode 0)	Boot mode	Parallel I/O mode
Programmer	None	Serial programmer	Parallel programmer

25.1 Memory Map

The flash memory includes the user ROM area and the boot ROM area. The user ROM area has space to store the microcomputer operating programs in single-chip mode or memory expansion mode, and a separate 4-kbyte space as the block A. Figure 25.1 shows a block diagram of the flash memory.

The user ROM area is divided into several blocks, each of which can be protected (locked) from program or erase. The user ROM area can be rewritten in CPU rewrite mode, standard serial I/O mode and parallel I/O mode.

The boot ROM area is located at the same addresses as the user ROM area. It can only be rewritten in parallel I/O mode. A program in the boot ROM area is executed after a hardware reset occurs while a high-level ("H") signal is applied to the CNVss and P50 pins and a low-level ("L") signal is applied to the P5s pin. A program in the user ROM area is executed after a hardware reset occurs while an "L" signal is applied to the CNVss pin. Consequently, the boot ROM area cannot be read.

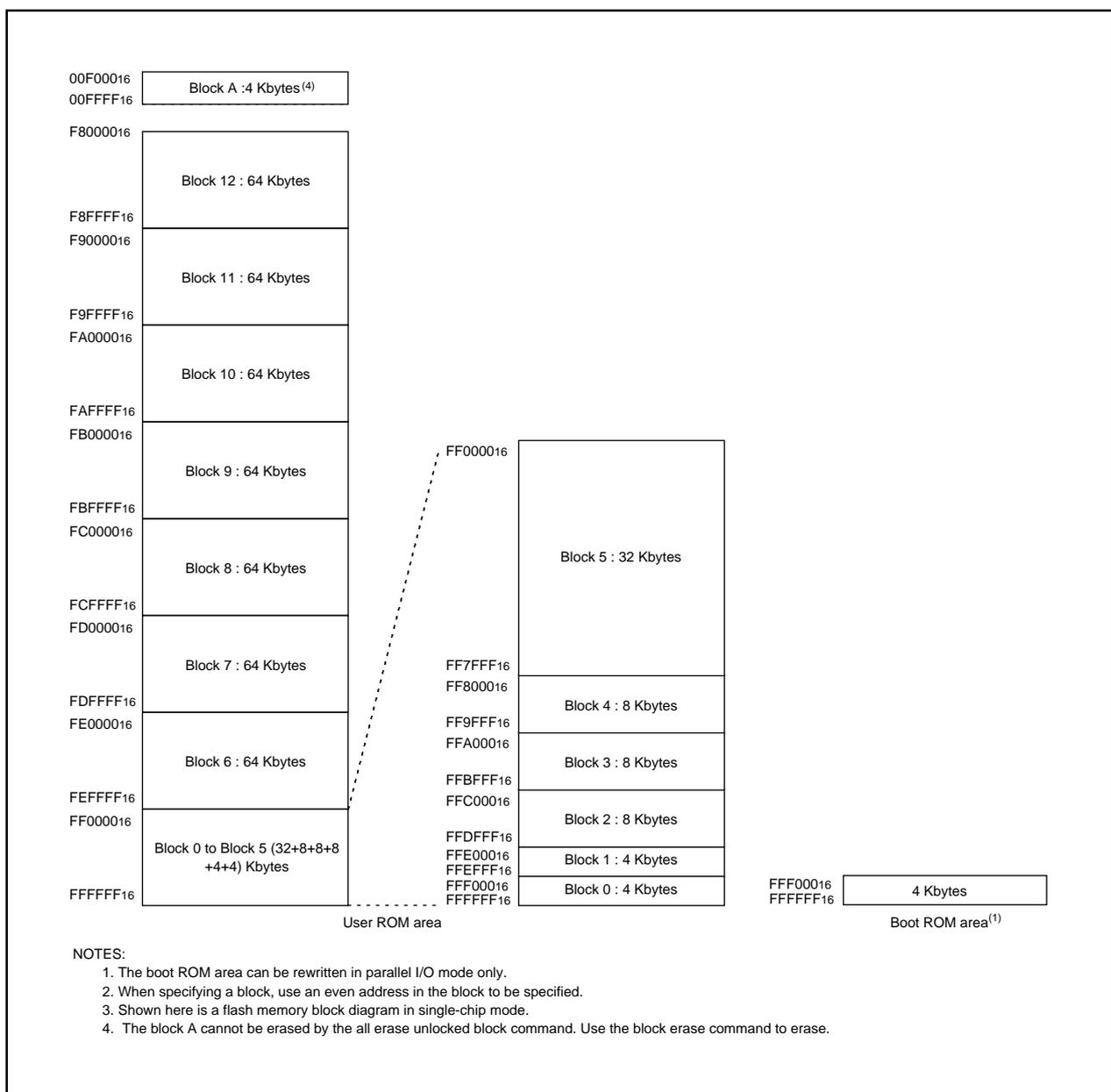


Figure 25.1 Flash Memory Block Diagram

25.1.1 Boot Mode

The microcomputer enters boot mode when a hardware reset is performed while a high-level ("H") signal is applied to the CNVss and P50 pins and a low-level ("L") signal is applied to the P55 pin. A program in the boot ROM area is executed.

In boot mode, the FMR05 bit in the FMR0 register selects access to either the boot ROM area or the user ROM area.

In the factory setting, the rewrite control program for standard serial I/O mode is stored into the boot ROM area.

The boot ROM area can be rewritten in parallel I/O mode only. If any rewrite control program using erase-write mode 0 (EW mode 0) is written in the boot ROM area, the flash memory can be rewritten according to the system implemented.

25.2 Functions to Prevent the Flash Memory from Rewriting

The flash memory has the ROM code protect function for parallel I/O mode and the ID code verify function for standard I/O mode to prevent the flash memory from reading or rewriting.

25.2.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from reading and rewriting in parallel I/O mode.

Figure 25.2 shows the ROMCP register. The ROMCP register is located in the user ROM area.

The ROM code protect function is enabled when the ROMCP1 bit is set to "002", "012" or "102".

25.2.2 ID Code Verify Function

Use the ID code verify function in standard serial I/O mode. The ID code sent from the serial programmer is compared with the ID code written in the flash memory for a match. If the ID codes do not match, commands sent from the serial programmer are not accepted. However, if the four bytes of the reset vector are "FFFFFFFF₁₆", ID codes are not compared, allowing all commands to be accepted.

The ID codes are 7-byte data stored consecutively, starting with the first byte, into addresses 0FFFFFFDF₁₆, 0FFFFFFE3₁₆, 0FFFFFFEB₁₆, 0FFFFFFEF₁₆, 0FFFFFFF3₁₆, 0FFFFFFF7₁₆ and 0FFFFFFFB₁₆. The flash memory must have a program with the ID codes set in these addresses.

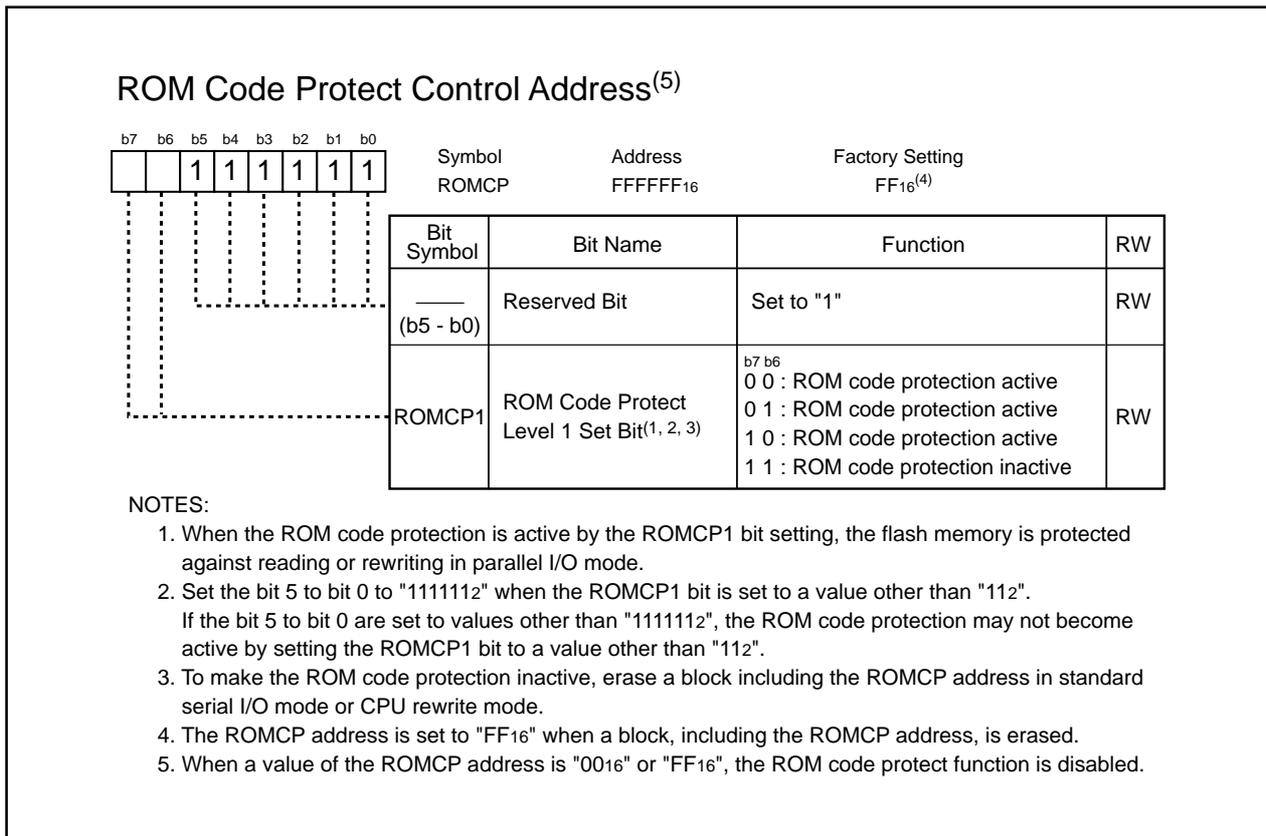


Figure 25.2 ROMCP Address

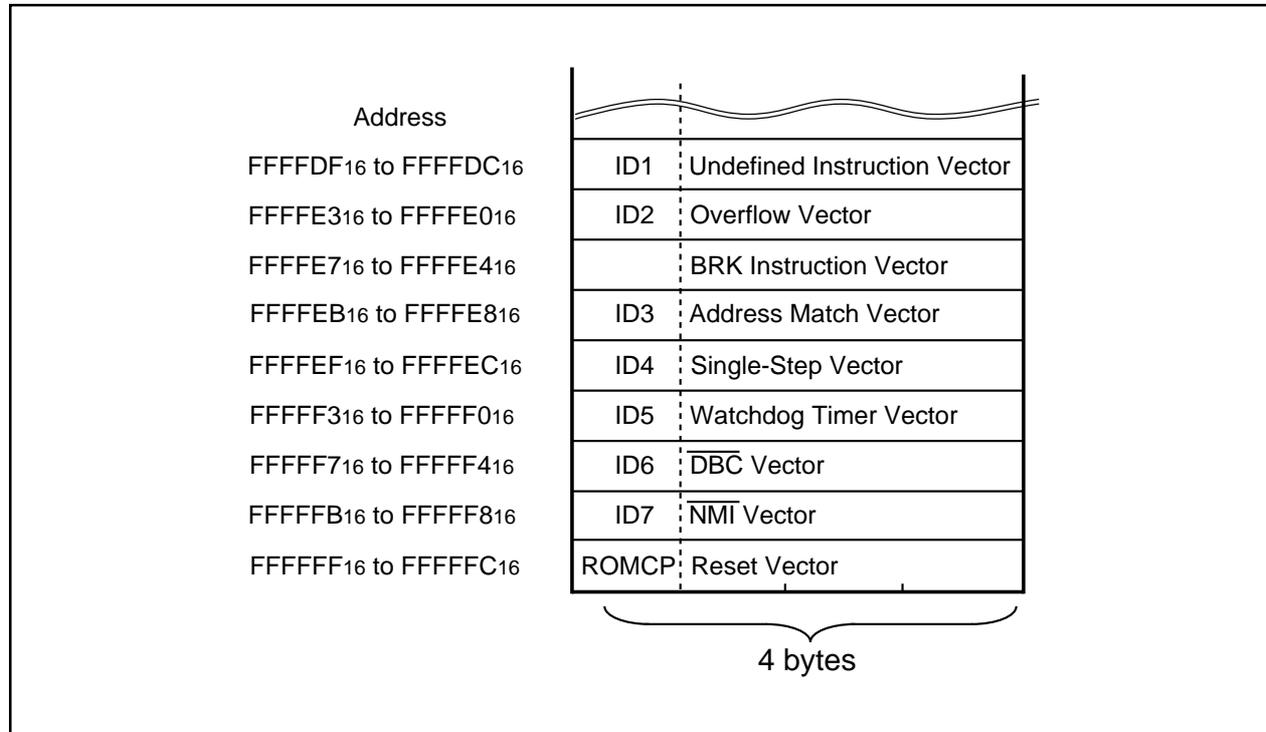


Figure 25.3 Address for ID Code Stored

25.3 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten when the CPU executes software commands. The user ROM area can be rewritten with the microcomputer mounted on a board without using a parallel or serial programmer.

In CPU rewrite mode, only the user ROM area shown in Figure 25.1 can be rewritten. The boot ROM area cannot be rewritten. The program and block erase commands are executed only for each block in the user ROM area.

Erase-write (EW) mode 0 and erase-write mode 1 are provided as CPU rewrite mode. Table 25.3 lists differences between EW mode 0 and EW mode 1.

Table 25.3 EW Mode 0 and EW Mode 1

Item	EW mode 0	EW mode 1
Operating Mode	<ul style="list-style-type: none"> Single-chip mode Memory expansion mode Boot mode 	Single-chip mode
Space where the rewrite control program can be placed	<ul style="list-style-type: none"> User ROM area Boot ROM area 	User ROM area
Space where the rewrite control program can be executed	The rewrite control program must be transferred to any space other than the flash memory (e.g.,RAM) before being executed	The rewrite control program can be executed in the user ROM area
Space which can be rewritten	User ROM area	User ROM area However, this excludes blocks with the rewrite control program
Software Command Restriction	None	<ul style="list-style-type: none"> Program and block erase commands cannot be executed in a block having the rewrite control program. Erase all unlocked block command cannot be executed when the lock bit in a block having the rewrite control program is set to "1"(unlocked) or when the FMR02 bit in the FMR0 register is set to "1"(lock bit disabled). Read status register command cannot be used.
Mode after Programming or Erasing	Read status register mode	Read array mode
CPU State during Auto Program and Erase Operation	Operating	In a hold state (I/O ports maintains the state before the command was executed) ⁽¹⁾
Flash Memory State Detection	<ul style="list-style-type: none"> Read the FMR00, FMR06 and FMR07 bits in the FMR0 register by program Execute the read status register command to read the SR7, SR5 and SR4 bits in the SRD register 	Read the FMR00, FMR06 and FMR07 bits in the FMR0 register by program

NOTES:

- Do not generate an interrupt (except $\overline{\text{NMI}}$ interrupt) or a DMA transfer.

25.3.1 EW Mode 0

The microcomputer enters CPU rewrite mode by setting the FMR01 bit in the FMR0 register to "1" (CPU rewrite mode enabled) and is ready to accept commands. EW mode 0 is selected by setting the FMR11 bit in the FMR1 register to "0". To set the FMR01 bit to "1", set to "1" after first writing "0".

The software commands control programming and erasing. The FMR0 register or the SRD register indicates whether a program or erase operation is completed as expected or not.

25.3.2 EW Mode 1

EW mode 1 is selected by setting the FMR11 bit to "1" after the FMR01 bit is set to "1". (Both bits must be set to "0" first before setting to "1".)

The FMR0 register indicates whether or not a program or erase operation has been completed as expected. The SRD register cannot be read in EW mode 1.

25.3.3 Flash Memory Control Register (FMR0 Register and FMR1 Register)

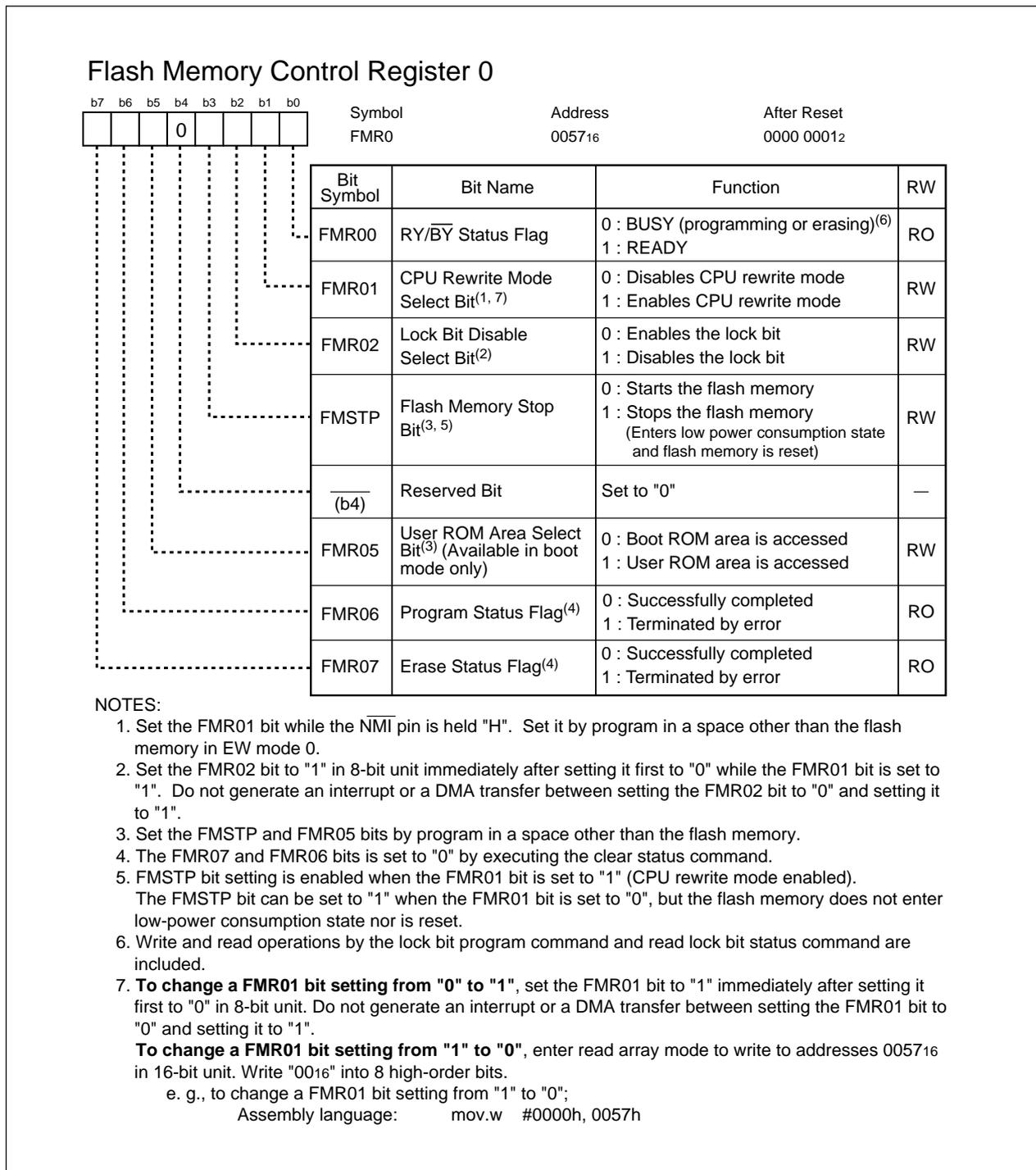


Figure 25.4 FMR0 Register

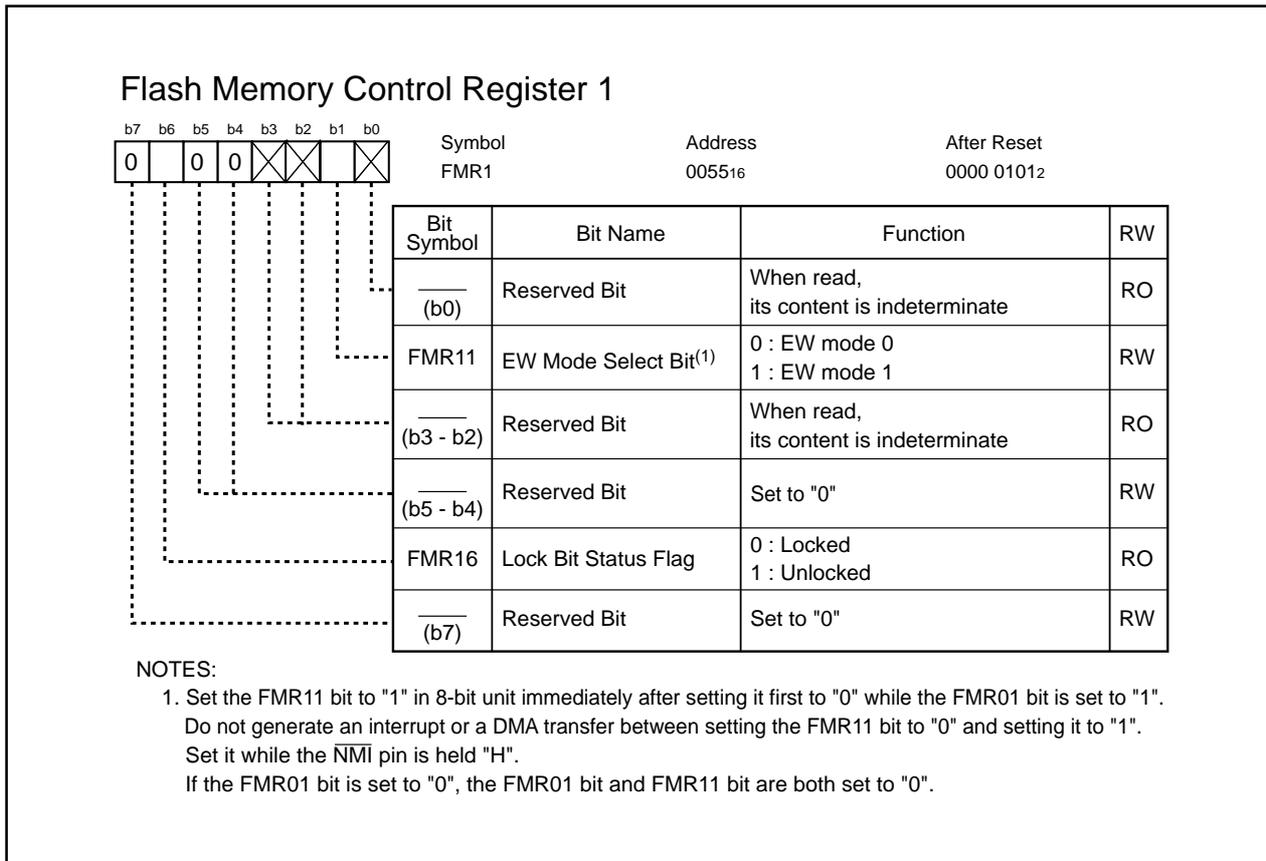


Figure 25.5 FMR1 Register

25.3.3.1 FMR00 Bit

The FMR00 bit indicates the flash memory operating state. It is set to "0" while the program, block erase, erase all unlocked block, lock bit program, or read lock bit status command is being executed; otherwise, it is set to "1".

25.3.3.2 FMR01 Bit

The microcomputer can accept commands when the FMR01 bit is set to "1" (CPU rewrite mode). Set the FMR05 bit to "1" (user ROM area access) as well if in boot mode.

25.3.3.3 FMR02 Bit

The lock bit is invalid by setting the FMR02 bit to "1" (lock bit disabled). (Refer to **25.3.6 Data Protect Function**.) The lock bit is valid by setting the FMR02 bit to "0" (lock bit enabled).

The FMR02 bit does not change the lock bit status but disables the lock bit function. If the block erase or erase all unlocked block command is executed when the FMR02 bit is set to "1", the lock bit status changes "0" (locked) to "1" (unlocked) after command execution is completed.

25.3.3.4 FMSTP Bit

The FMSTP bit resets the flash memory control circuits and minimizes power consumption in the flash memory. Access to the flash memory is disabled when the FMSTP bit is set to "1". Set the FMSTP bit by program in a space other than the flash memory.

Set the FMSTP bit to "1" if one of the followings occurs:

- A flash memory access error occurs while erasing or programming in EW mode 0 (FMR00 bit does not switch back to "1" (ready)).
- Low-power consumption mode or on-chip low-power consumption mode is entered.

Use the following the procedure to change the FMSTP bit setting.

- (1) Set the FMSTP bit to "1"
- (2) Set tps (the wait time to stabilize flash memory circuit)
- (3) Set the FMSTP bit to "0"
- (4) Set tps (the wait time to stabilize flash memory circuit)

Figure 25.8 shows a flow chart illustrating how to start and stop the flash memory before and after entering low power mode. Follow the procedure on this flow chart.

When entering stop or wait mode, the flash memory is automatically turned off. When exiting stop or wait mode, the flash memory is turned back on. The FMR0 register does not need to be set.

25.3.3.5 FMR05 Bit

The FMR05 bit selects the boot ROM or user ROM area in boot mode. Set to "0" to access (read) the boot ROM area or to "1" (user ROM access) to access (read, write or erase) the user ROM area.

25.3.3.6 FMR06 Bit

The FMR06 bit is a read-only bit indicating an auto program operation state. The FMR06 bit is set to "1" when a program error occurs; otherwise, it is set to "0". Refer to **25.3.8 Full Status Check**.

25.3.3.7 FMR07 Bit

The FMR07 bit is a read-only bit indicating the auto erase operation state. The FMR07 bit is set to "1" when an erase error occurs; otherwise, it is set to "0". For details, refer to **25.3.8 Full Status Check**.

Figure 25.6 shows how to enter and exit EW mode 0. Figure 25.7 shows how to enter and exit EW mode 1.

25.3.3.8 FMR11 Bit

EW mode 0 is entered by setting the FMR11 bit to "0" (EW mode 0).

EW mode 1 is entered by setting the FMR11 bit to "1" (EW mode 1).

25.3.3.9 FMR16 Bit

The FMR16 bit is a read-only bit indicating the execution result of the read lock bit status command. When the block, where the read lock bit status command is executed, is locked, the FMR16 bit is set to "0". When the block, where the read lock bit status command is executed, is unlocked, the FMR16 bit is set to "1".

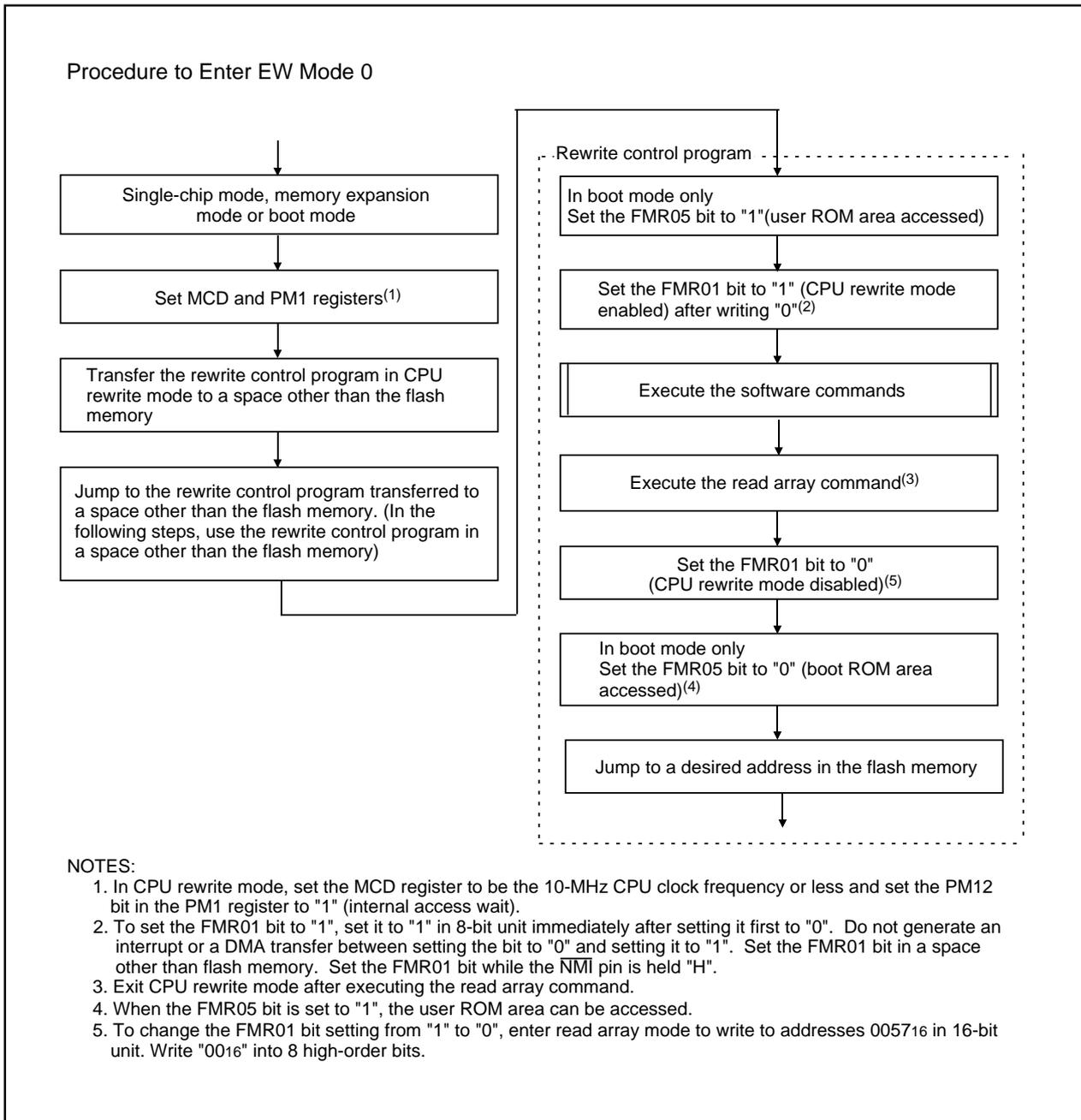


Figure 25.6 How to Enter and Exit EW Mode 0

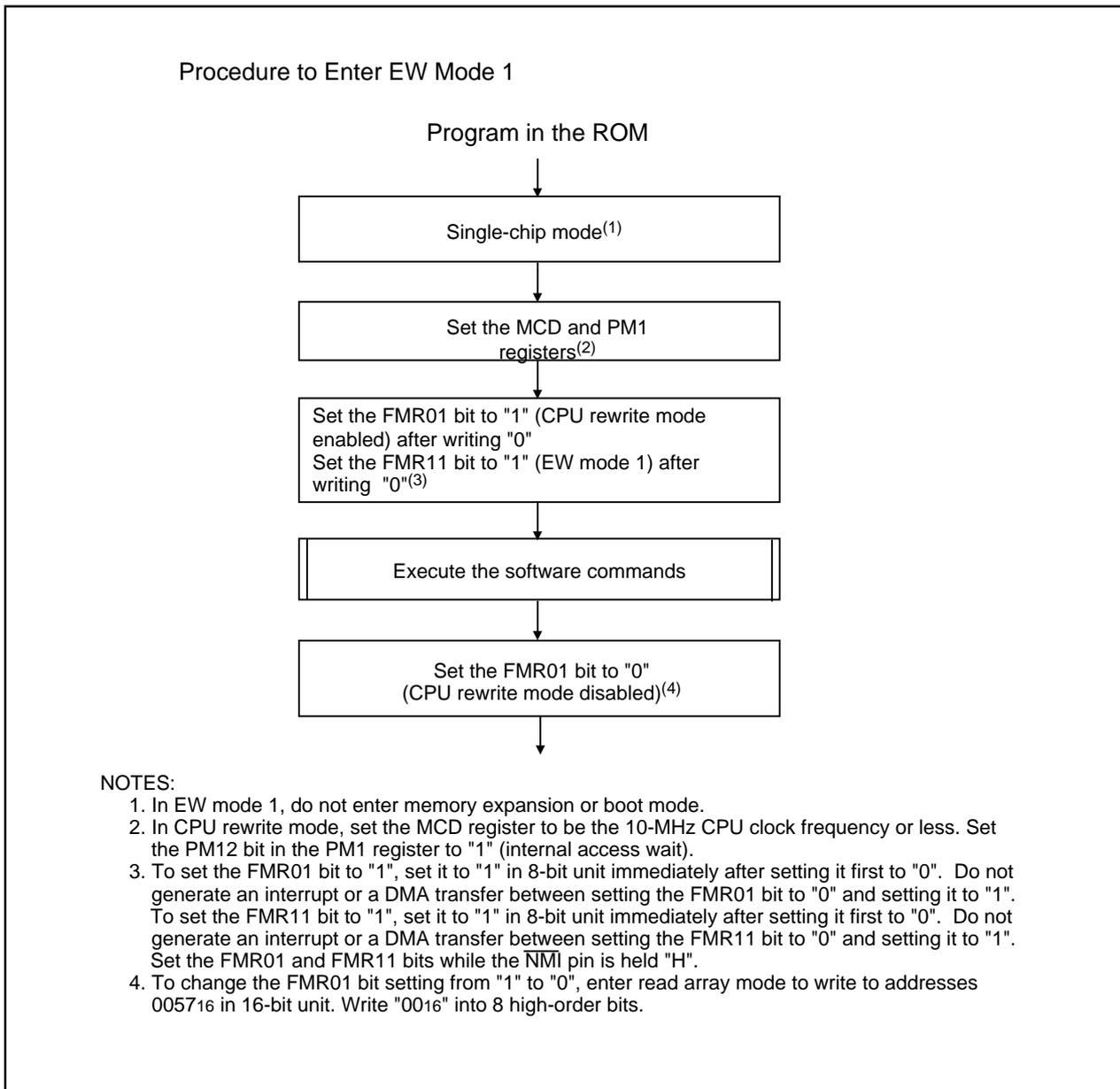


Figure 25.7 How to Enter and Exit EW Mode 1

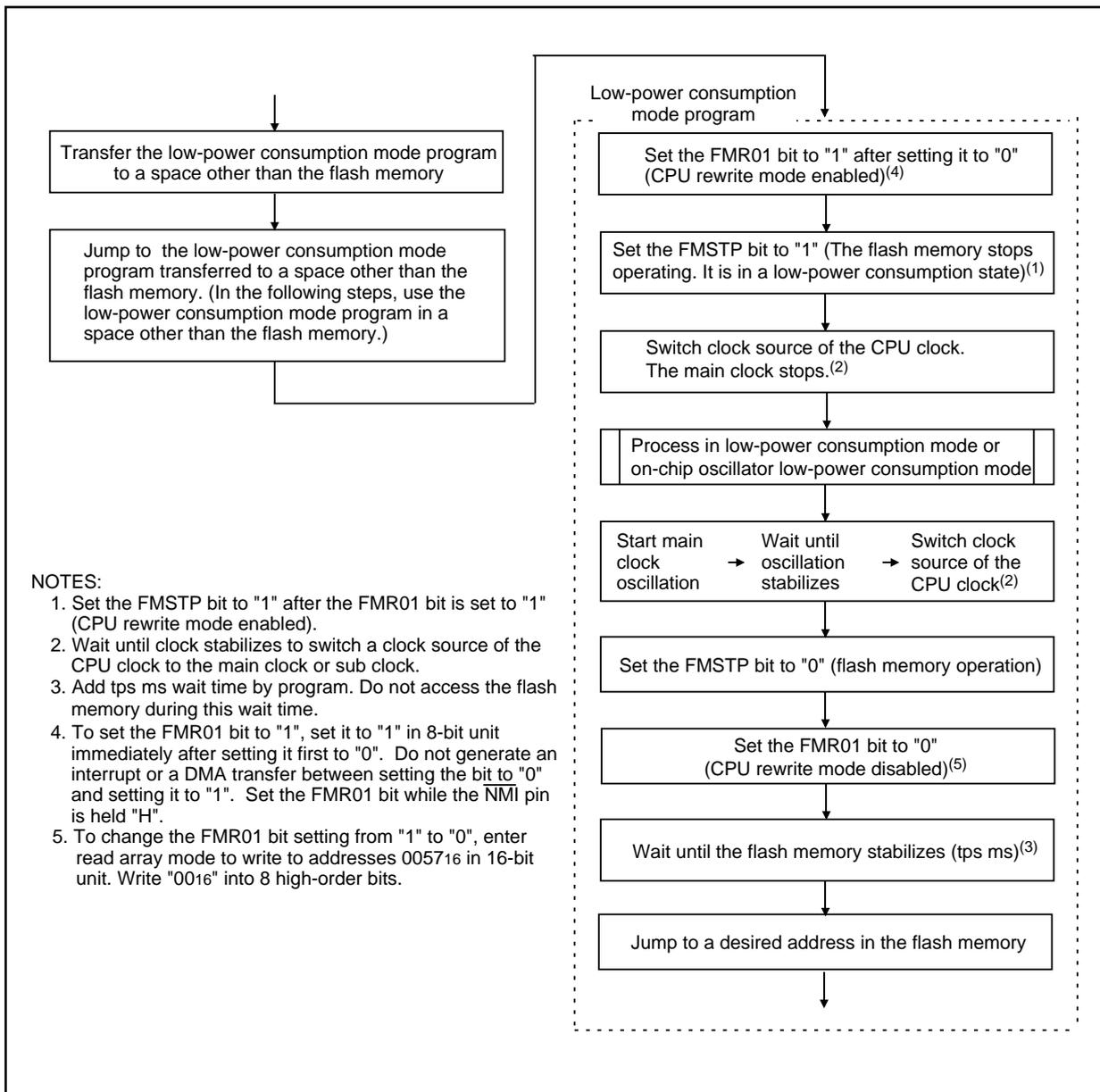


Figure 25.8 Handling Before and After Low Power Consumption Mode

25.3.4 Precautions in CPU Rewrite Mode

25.3.4.1 Operating Speed

Set the MCD4 to MCD0 bits in the MCD register to CPU clock frequency of 10 MHz or less before entering CPU rewrite mode (EW mode 0 or EW mode 1). Also, set the PM12 bit in the PM1 register to "1" (wait state).

25.3.4.2 Prohibited Instructions

The following instructions cannot be used in EW mode 0 because the CPU tries to read data in the flash memory: the UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

25.3.4.3 Interrupts (EW Mode 0)

- To use interrupts having vectors in a relocatable vector table, the vectors must be relocated to the RAM area.
- The $\overline{\text{NMI}}$ and watchdog timer interrupts are available since the FMR0 and FMR1 registers are forcibly reset when either interrupt occurs. Allocate the forward addresses for each interrupt routine to the fixed vector table. Flash memory rewrite operation is aborted when the $\overline{\text{NMI}}$ or watchdog timer interrupt occurs. Execute the rewrite program again after exiting the interrupt routine.
- The address match interrupt is not available since the CPU tries to read data in the flash memory.

25.3.4.4 Interrupts (EW Mode 1)

- Do not acknowledge any interrupts with vectors in the relocatable vector table or address match interrupt during the auto program or auto erase period.
- Do not use the watchdog timer interrupt.
- The $\overline{\text{NMI}}$ interrupt is available since the FMR0 and FMR1 registers are forcibly reset when either interrupt occurs. Allocate the forward address for the interrupt routine to the fixed vector table. Flash memory rewrite operation is aborted when the $\overline{\text{NMI}}$ interrupt occurs. Execute the rewrite program again after exiting the interrupt routine.

25.3.4.5 How to Access

To set the FMR01, FMR02 in the FMR0 register or FMR11 bit in the FMR1 register to "1", set to "1" in 8-bit units immediately after setting to "0". Do not generate an interrupt or a DMA transfer between the instruction to set the bit to "0" and the instruction to set the bit to "1". Set the bit while a high-level ("H") signal is applied to the $\overline{\text{NMI}}$ pin.

To change the FMR01 bit from "1" to "0", enter read array mode first, and write into address 005716 in 16-bit units. Eight high-order bits must be set to "0016".

25.3.4.6 Rewriting in the User ROM Area (EW Mode 0)

If the supply voltage drops while rewriting the block where the rewrite control program is stored, the flash memory cannot be rewritten because the rewrite control program is not rewritten as expected. If this error occurs, rewrite the user ROM area while in standard serial I/O mode or parallel I/O mode.

25.3.4.7 Rewriting in the User ROM Area (EW Mode 1)

Do not rewrite the block where the rewrite control program is stored.

25.3.4.8 DMA Transfer

In EW mode 1, do not generate a DMA transfer while the FMR00 bit in the FMR0 register is set to "0" (busy-programming or erasing).

25.2.4.9 Writing Command and Data

Write commands and data to even addresses in the user ROM area.

25.3.4.10 Wait Mode

When entering wait mode, set the FMR01 bit in the FMR0 register to "0" (CPU rewrite mode disabled) before executing the WAIT instruction.

25.3.4.11 Stop Mode

When entering stop mode, the following settings are required:

- Set the FMR01 bit to "0" (CPU rewrite mode disabled). Disable a DMA transfer before setting the CM10 bit to "1" (stop mode).
- Execute the instruction to set the CM10 bit to "1" (stop mode) and then the JMP.B instruction.

e.g., BSET 0, CM1 ; Stop mode

 JMP.B L1

 L1:

 Program after exiting stop mode

25.3.4.12 Low-Power Consumption Mode and On-Chip Oscillator Low-Power Consumption Mode

If the CM05 bit is set to "1" (main clock stopped), do not execute the following commands:

- Program
- Block erase
- Erase all unlocked blocks
- Lock bit program
- Read lock bit status

25.3.5 Software Commands

Read or write 16-bit commands and data from or to even addresses in the user ROM area, in 16-bit units. When writing a command code, 8 high-order bits (D15 to D8) are ignored.

Table 25.4 Software Commands

Command	First Bus Cycle			Second Bus Cycle		
	Mode	Address	Data (D15 to D0)	Mode	Address	Data (D15 to D0)
Read Array	Write	X	xxFF ₁₆			
Read Status Register	Write	X	xx70 ₁₆	Read	X	SRD
Clear Status Register	Write	X	xx50 ₁₆			
Program	Write	WA	xx40 ₁₆	Write	WA	WD
Block Erase	Write	X	xx20 ₁₆	Write	BA	xxD0 ₁₆
Erase All Unlocked Block ⁽¹⁾	Write	X	xxA7 ₁₆	Write	X	xxD0 ₁₆
Lock Bit Program	Write	BA	xx77 ₁₆	Write	BA	xxD0 ₁₆
Read Lock Bit Status	Write	X	xx71 ₁₆	Write	BA	xxD0 ₁₆

NOTES:

- Blocks 0 to 12 can be erased by the erase all unlocked block command. Block A cannot be erased. The block erase command must be used to erase the block A.

SRD: Data in the SRD register (D7 to D0)

WA: Address to be written (The address specified in the the first bus cycle is the same even address as the address specified in the second bus cycle.)

WD: 16-bit write data

BA: Highest-order block address (must be an even address)

X: Any even address in the user ROM space

xx: 8 high-order bits of command code (ignored)

25.3.5.1 Read Array Command

The read array command reads the flash memory.

Read array mode is entered by writing command code "xxFF₁₆" in the first bus cycle. Content of a specified address can be read in 16-bit units after the next bus cycle.

The microcomputer remains in read array mode until another command is written. Therefore, contents from multiple addresses can be read consecutively.

25.3.5.2 Read Status Register Command

The read status register command reads the SRD register (refer to **25.3.7 Status Register** for detail).

By writing command code "xx70₁₆" in the first bus cycle, the SRD register can be read in the second bus cycle. Read an even address in the user ROM area.

Do not execute this command in EW mode 1.

25.3.5.3 Clear Status Register Command

The clear status register command clears the SRD register. By writing "xx50₁₆" in the first bus cycle, the FMR07 and FMR06 bits in the FMR0 register are set to "002" and the SR5 and SR4 bits in the SRD register are set to "002".

25.3.5.4 Program Command

The program command writes 1-word, or 2-byte, data to the flash memory.

Auto program operation (data program and verify) will start by writing command code "xx4016" in the first bus cycle and data to the write address in the second bus cycle. The address value specified in the first bus cycle must be the same even address as the write address specified in the second bus cycle.

The FMR00 bit in the FMR0 register indicates whether or not an auto program operation has been completed. The FMR00 bit is set to "0" (busy) during auto program and to "1" (ready) when the auto program operation is completed.

After the completion of auto program operation, the FMR06 bit in the FMR0 register indicates whether or not the auto program operation has been completed as expected. (Refer to **25.3.8 Full Status Check**.)

An address that is already written cannot be altered or rewritten.

Figure 25.9 shows a flow chart of the program command programming.

The lock bit can protect each block from being programmed inadvertently. (Refer to **25.3.6 Data Protect Function**.)

In EW mode 1, do not execute this command on the block where the rewrite control program is allocated. In EW mode 0, the microcomputer enters read status register mode as soon as an auto program operation starts. The SRD register can be read. The SR7 bit in the SRD register is set to "0" at the same time an auto program operation starts. It is set to "1" when an auto program operation is completed. The microcomputer remains in read status register mode until the read array command is written. After completion of an auto program operation, the SRD register indicates whether or not the auto program operation has been completed as expected.

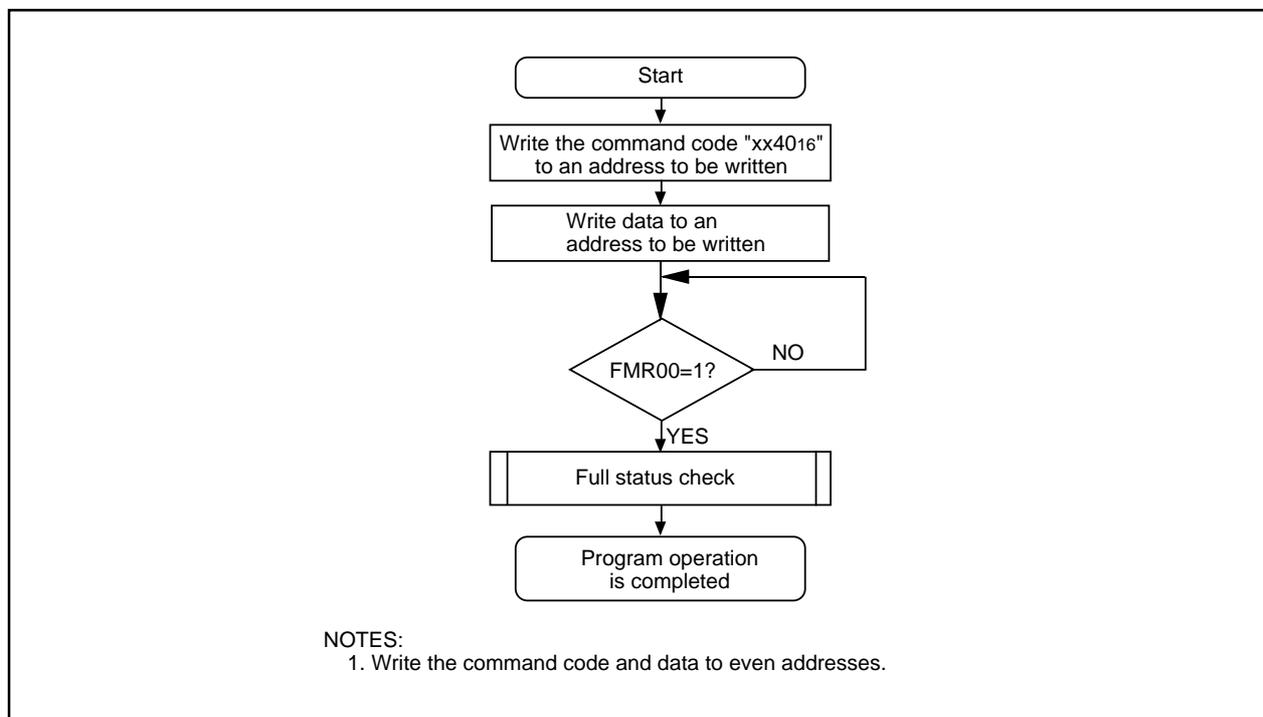


Figure 25.9 Program Command

25.3.5.5 Block Erase Command

The block erase command erases each block.

Auto erase operation (erase and verify) will start in the specified block by writing command code "xx20₁₆" in the first bus cycle and "xxD0₁₆" to the highest-order even address of a block in the second bus cycle.

The FMR00 bit in the FMR0 register indicates whether or not an auto erase operation has been completed. The FMR00 bit is set to "0" (busy) during auto erase and to "1" (ready) when the auto erase operation is completed.

After the completion of an auto erase operation, the FMR07 bit in the FMR0 register indicates whether or not the auto erase operation has been completed as expected. (Refer to **25.3.8 Full Status Check**.)

Figure 25.10 shows a flow chart of the block erase command programming.

The lock bit can protect each block from being programmed inadvertently. (Refer to **25.3.6 Data Protect Function**.)

In EW mode 1, do not execute this command on the block where the rewrite control program is allocated. In EW mode 0, the microcomputer enters read status register mode as soon as an auto erase operation starts. The SRD register can be read. The SR7 bit in the SRD register is set to "0" at the same time an auto erase operation starts. It is set to "1" when an auto erase operation is completed. The microcomputer remains in read status register mode until the read array command or read lock bit status command is written.

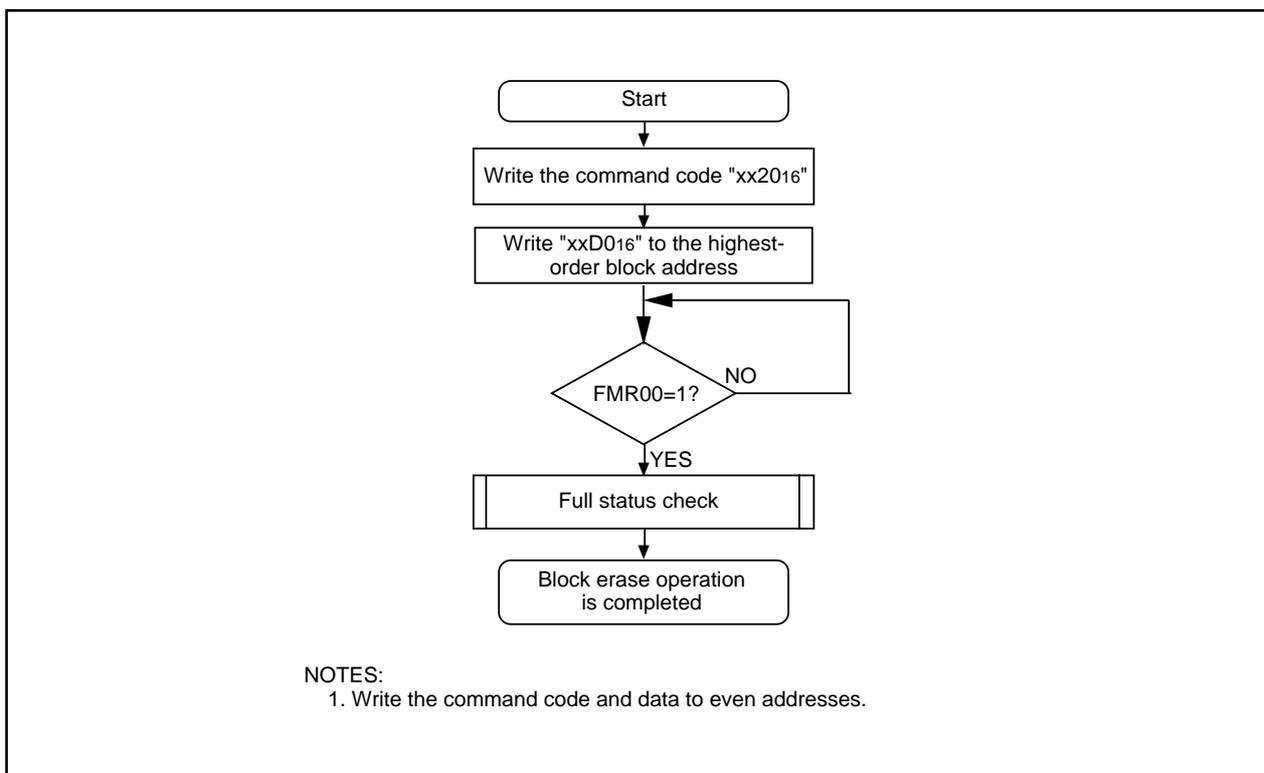


Figure 25.10 Block Erase Command

25.3.5.6 Erase All Unlocked Block Command

The erase all unlocked block command erases all blocks except the block A.

By writing command code "xxA716" in the first bus cycle and "xxD016" in the second bus cycle, auto erase (erase and verify) operation will run continuously in all blocks except the block A.

The FMR00 bit in the FMR0 register indicates whether or not an auto erase operation has been completed.

After the completion of an auto erase operation, the FMR07 bit in the FMR0 register indicates whether or not the auto erase operation has been completed as expected.

The lock bit can protect each block from being programmed inadvertently. (Refer to **25.3.6 Data Protect Function**.)

In EW mode 1, do not execute this command when the lock bit for any block storing the rewrite control program is set to "1" (unlocked) or when the FMR02 bit in the FMR0 register is set to "1" (lock bit disabled).

In EW mode 0, the microcomputer enters read status register mode as soon as an auto erase operation starts. The SRD register can be read. The SR7 bit in the SRD register is set to "0" (busy) at the same time an auto erase operation starts. It is set to "1" (ready) when an auto erase operation is completed. The microcomputer remains in read status register mode until the read array command or read lock bit status command is written.

Only blocks 0 to 12 can be erased by the erase all unlocked block command. The block A cannot be erased. Use the block erase command to erase the block A.

25.3.5.7 Lock Bit Program Command

The lock bit program command sets the lock bit for a specified block to "0" (locked).

By writing command code "xx7716" in the first bus cycle and "xxD016" to the highest-order even address of a block in the second bus cycle, the lock bit for the specified block is set to "0". The address value specified in the first bus cycle must be the same highest-order even address of a block specified in the second bus cycle.

Figure 25.11 shows a flow chart of the lock bit program command programming. Execute read lock bit status command to read lock bit state (lock bit data).

The FMR00 bit in the FMR0 register indicates whether a lock bit program operation is completed.

Refer to **25.3.6 Data Protect Function** for details on lock bit functions and how to set it to "1" (unlocked).

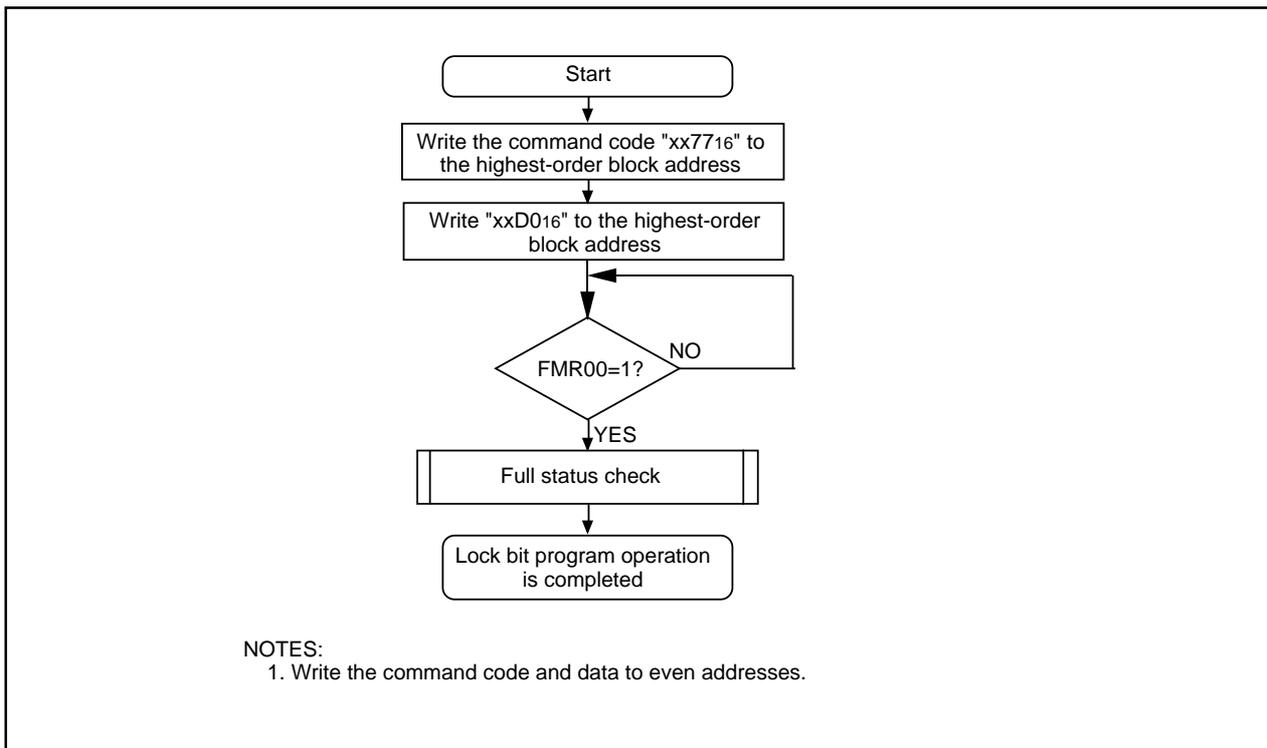


Figure 25.11 Lock Bit Program Command

25.3.5.8 Read Lock Bit Status Command

The read lock bit status command reads the lock bit state (the lock bit data) of a specified block. By writing command code "xx7116" in the first bus cycle and "xxD016" to the highest-order even address of a block in the second bus cycle, the FMR16 bit in the FMR1 register stores information on whether or not the lock bit of a specified block is locked. Read the FMR16 bit after the FMR00 bit in the FMR0 register is set to "1" (ready).

Figure 25.12 shows a flow chart of the read lock bit status command programming.

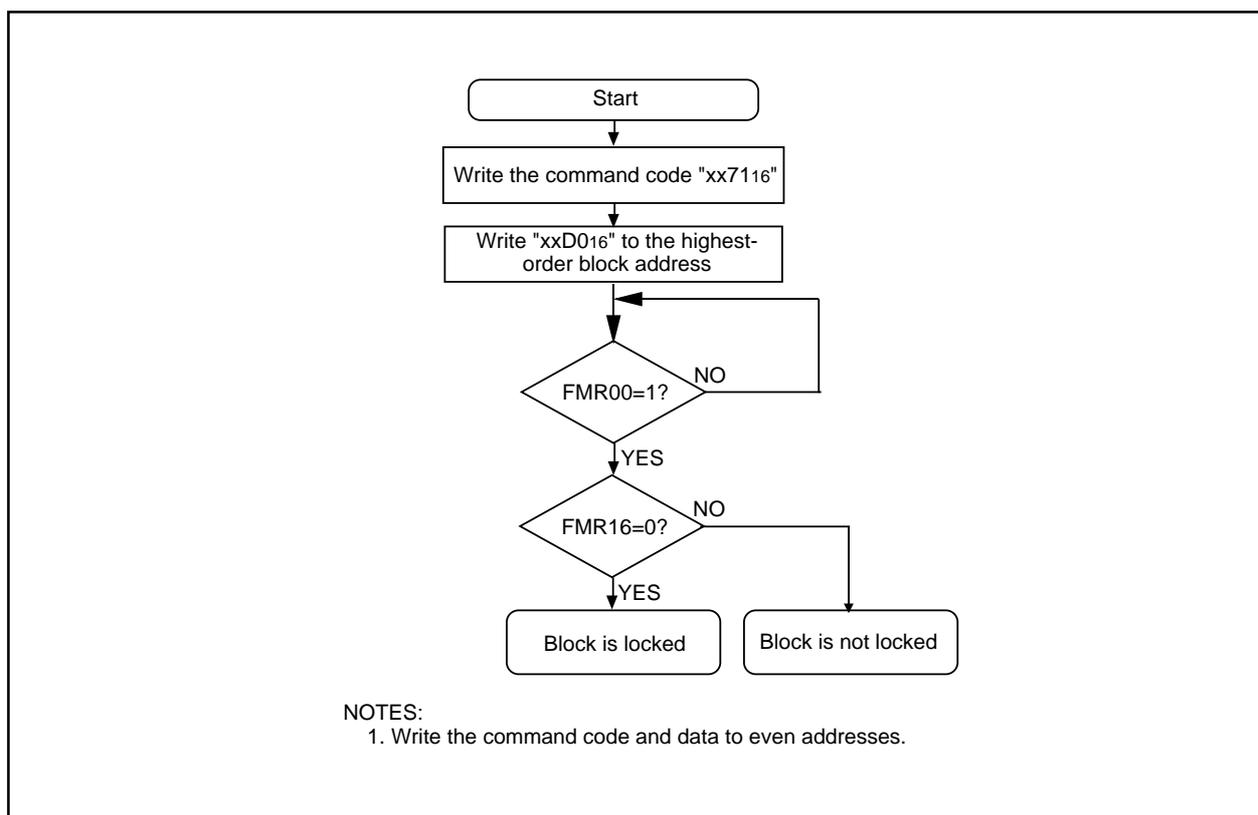


Figure 25.12 Read Lock Bit Status Command

25.3.6 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR02 bit to "0" (lock bit enabled). The lock bit individually protects (locks) each block against program and erase. This prevents data from being inadvertently written to or erased from the flash memory.

- When the lock bit status is set to "0", the block is locked (block is protected against program and erase).
- When the lock bit status is set to "1", the block is not locked (block can be programmed or erased).

The lock bit status is set to "0" (locked) by executing the lock bit program command and to "1" (unlocked) by erasing the block. The lock bit status cannot be set to "1" by any commands.

The lock bit status can be read by the read lock bit status command.

The lock bit function is disabled by setting the FMR02 bit to "1". All blocks are unlocked. However, individual lock bit status remains unchanged. The lock bit function is enabled by setting the FMR02 bit to "0". Lock bit status is retained.

If the block erase or erase all unlocked block command is executed while the FMR02 bit is set to "1", the target block or all blocks are erased regardless of lock bit status. The lock bit status of each block are set to "1" after an erase operation is completed.

Refer to **25.3.5 Software Commands** for details on each command.

25.3.7 Status Register (SRD Register)

The SRD register indicates the flash memory operating state and whether or not an erase or program operation is completed as expected. The FMR00, FMR06 and FMR07 bits in the FMR0 register indicate SRD register states.

Table 25.5 shows the SRD register.

In EW mode 0, the SRD register can be read when the followings occur.

- Any even address in the user ROM area is read after writing the read status register command
- Any even address in the user ROM area is read from when the program, block erase, erase all unlocked block, or lock bit program command is executed until when the read array command is executed.

25.3.7.1 Sequencer Status (SR7 and FMR00 Bits)

The sequencer status indicates the flash memory operating state. It is set to "0" while the program, block erase, erase all unlocked block, lock bit program, or read lock bit status command is being executed; otherwise, it is set to "1".

25.3.7.2 Erase Status (SR5 and FMR07 Bits)

Refer to **25.3.8 Full Status Check**.

25.3.7.3 Program Status (SR4 and FMR06 Bits)

Refer to **25.3.8 Full Status Check**.

Table 25.5 Status Register

Bits in SRD register	Bits in FMR0 Register	Status Name	Definition		Value after Reset
			"0"	"1"	
SR7 (D7)	FMR00	Sequencer status	BUSY	READY	1
SR6 (D6)	—	Reserved bit	-	-	-
SR5 (D5)	FMR07 ⁽¹⁾	Erase status	Successfully completed	Error	0
SR4 (D4)	FMR06 ⁽¹⁾	Program status	Successfully completed	Error	0
SR3 (D3)	—	Reserved bit	-	-	-
SR2 (D2)	—	Reserved bit	-	-	-
SR1 (D1)	—	Reserved bit	-	-	-
SR0 (D0)	—	Reserved bit	-	-	-

D0 to D7: These data buses are read when the read status register command is executed.

NOTES:

1. The FMR07 (SR5) and FMR06 (SR4) bits are set to "0" by executing the clear status register command. When the FMR07 (SR5) or FMR06 (SR4) bit is set to "1", the program, block erase, erase all unlocked block and lock bit program commands are not accepted.

25.3.8 Full Status Check

If an error occurs when a program or erase operation is completed, the FMR07 and FMR06 bits in the FMR0 register are set to "1", indicating a specific error. Therefore, execution results can be confirmed by verifying these bits (full status check).

Table 25.6 lists errors and FMR0 register state. Figure 25.13 shows a flow chart of the full status check and handling procedure for each error.

Table 25.6 Errors and FMR0 Register State

FMR0 Register (SRD Register) State		Error	Error Occurrence Conditions
FMR07 (SR5)	FMR06 (SR4)		
1	1	Command sequence error	<ul style="list-style-type: none"> • An incorrect command is written • A value other than "xxD016" or "xxFF16" is written in the second bus cycle of the lock bit program, block erase or erase all unlocked block command⁽¹⁾
1	0	Erase error	<ul style="list-style-type: none"> • The block erase command is executed on a locked block⁽²⁾ • The block erase or erase all unlocked block command is executed on an unlock block, but the erase operation is not completed as expected
0	1	Program error	<ul style="list-style-type: none"> • The program command is executed on locked blocks⁽²⁾ • The program command is executed on an unlocked block, but the program operation is not completed as expected • The lock bit program command is executed but the program operation is not completed as expected

NOTES:

1. The flash memory enters read array mode when command code "xxFF16" is written in the second bus cycle of these commands. The command code written in the first bus cycle becomes invalid.
2. When the FMR02 bit is set to "1" (lock bit disabled), no error occurs even under the conditions above.

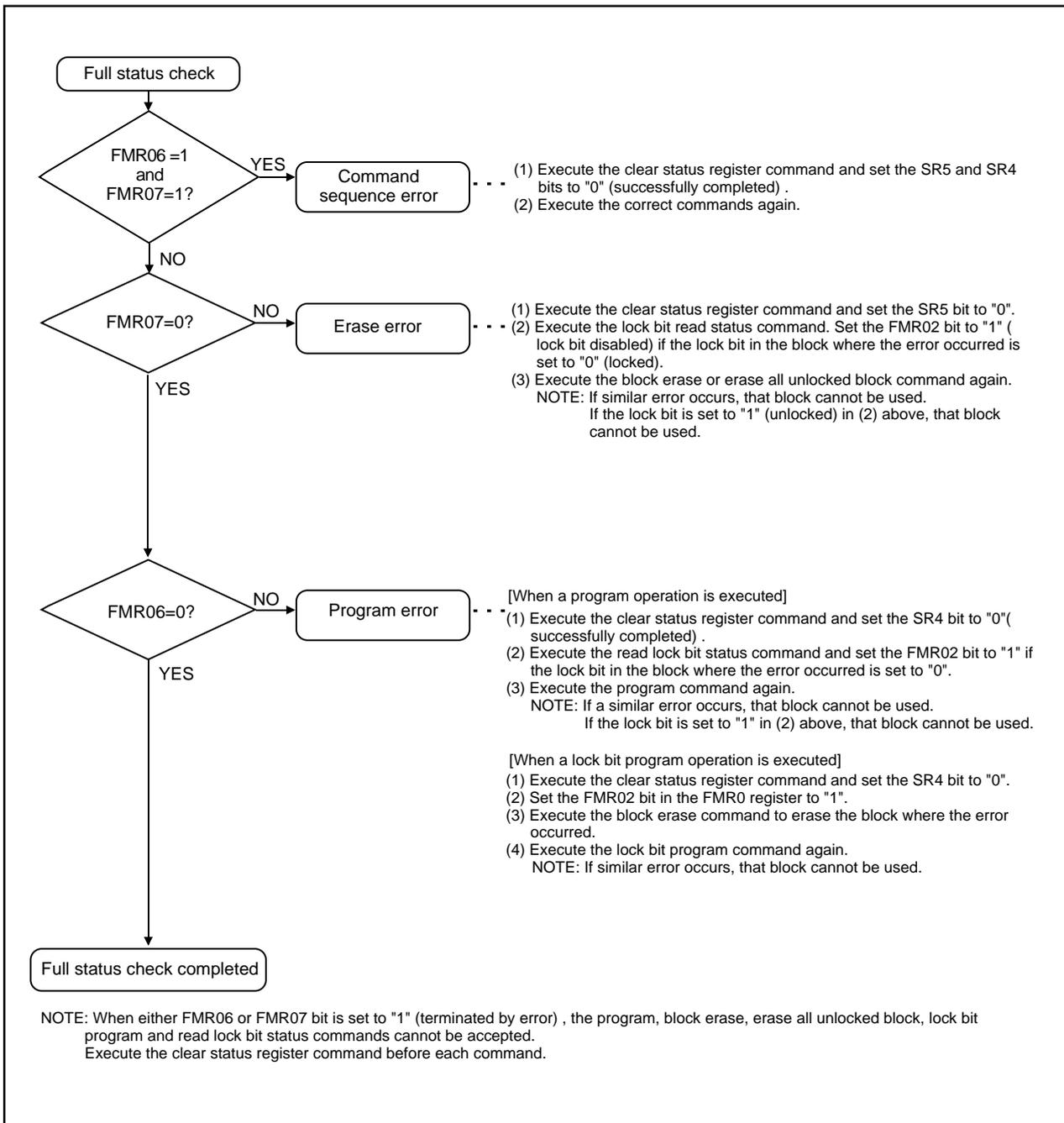


Figure 25.13 Full Status Check and Handling Procedure for Each Error

25.4 Standard Serial I/O Mode

In standard serial I/O mode, the serial programmer supporting the M32C/85 group (M32C/85, M32C/85T) can be used to rewrite the flash memory user ROM area, while the microcomputer is mounted on a board. For more information about the serial programmer, contact your serial programmer manufacturer. Refer to the user's manual included with your serial programmer for instructions.

Table 25.7 lists pin descriptions (flash memory standard serial I/O mode). Figures 25.14 to 25.16 show pin connections in serial I/O mode.

25.4.1 ID Code Verify Function

The ID code verify function determines whether or not the ID codes sent from the serial programmer matches those written in the flash memory. (Refer to **25.2 Functions to Prevent Flash Memory from Rewriting.**)

Table 25.7 Pin Description (Flash Memory Standard Serial I/O Mode)

Symbol	Function	I/O Type	Supply Voltage	Description
Vcc Vss	Power supply input	I	–	Apply the guaranteed program/erase supply voltage to the Vcc1 pin. Apply 0 V to the Vss pin
CNVss	CNVss	I	Vcc1	Connect this pin to Vcc1
RESET	Reset input	I	Vcc1	Reset input pin. Apply 20 or more clock cycles to the XIN pin while "L" is applied to the RESET pin
XIN	Clock input	I	Vcc1	Connect a ceramic resonator or crystal oscillator between XIN and XOUT
XOUT	Clock output	O	Vcc1	To use the external clock, input the clock from XIN and leave XOUT open
BYTE	BYTE input	I	Vcc1	Connect this pin to Vss or Vcc1
AVcc AVss	Analog power supply input	I	–	Connect AVcc to Vcc1 Connect AVss to Vss
VREF	Reference voltage input	I	–	Reference voltage input pin for the A/D converter
P00 to P07	Input port P0	I	Vcc2	Apply "H" or "L" to this pin, or leave open
P10 to P17	Input port P1	I	Vcc2	Apply "H" or "L" to this pin, or leave open
P20 to P27	Input port P2	I	Vcc2	Apply "H" or "L" to this pin, or leave open
P30 to P37	Input port P3	I	Vcc2	Apply "H" or "L" to this pin, or leave open
P40 to P47	Input port P4	I	Vcc2	Apply "H" or "L" to this pin, or leave open
P50	CE input	I	Vcc2	Apply "H" to this pin
P55	EPM input	I	Vcc2	Apply "L" to this pin
P51 to P54 P56, P57	Input port P5	I	Vcc2	Apply "H" or "L" to this pin, or leave open
P60 to P63 P64	Input port P6 BUSY output	I O	Vcc1 Vcc1	Apply "H" or "L" to this pin, or leave open Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Program running verify monitor Standard serial I/O mode 3: Leave open
P65	SCLK input	I	Vcc1	Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2, 3: Apply "L" to this pin
P66	RxD Data input	I	Vcc1	Standard serial I/O mode 1, 2: Serial data input pin Standard serial I/O mode 3: Apply "H" to this pin
P67	TxD Data output	O	Vcc1	Standard serial I/O mode 1, 2: Serial data output pin Standard serial I/O mode 3: Leave open
P70 to P75 P76	Input port P7 CAN output	I O	Vcc1 Vcc1	Apply "H" or "L" to this pin, or leave open Standard serial I/O mode 1, 2: Apply "H" or "L" to this pin, or leave open Standard serial I/O mode 3: CAN output pin
P77	CAN input	I	Vcc1	Standard serial I/O mode 1, 2: Apply "H" or "L" to this pin, or leave open Standard serial I/O mode 3: CAN input pin
P80 to P84 P86, P87 P85	Input port P8 NMI input	I I	Vcc1 Vcc1	Apply "H" or "L" to this pin, or leave open Connect this pin to Vcc1
P90 to P97	Input port P9	I	Vcc1	Apply "H" or "L" to this pin, or leave open
P100 to P107	Input port P10	I	Vcc1	Apply "H" or "L" to this pin, or leave open
P110 to P114	Input port P11	I	Vcc2	Apply "H" or "L" to this pin, or leave open ⁽¹⁾
P120 to P127	Input port P12	I	Vcc2	Apply "H" or "L" to this pin, or leave open ⁽¹⁾
P130 to P137	Input port P13	I	Vcc2	Apply "H" or "L" to this pin, or leave open ⁽¹⁾
P140 to P146	Input port P14	I	Vcc1	Apply "H" or "L" to this pin, or leave open ⁽¹⁾
P150 to P157	Input port P15	I	Vcc1	Apply "H" or "L" to this pin, or leave open ⁽¹⁾

NOTES:

1. These pins are provided in the 144-pin package only.

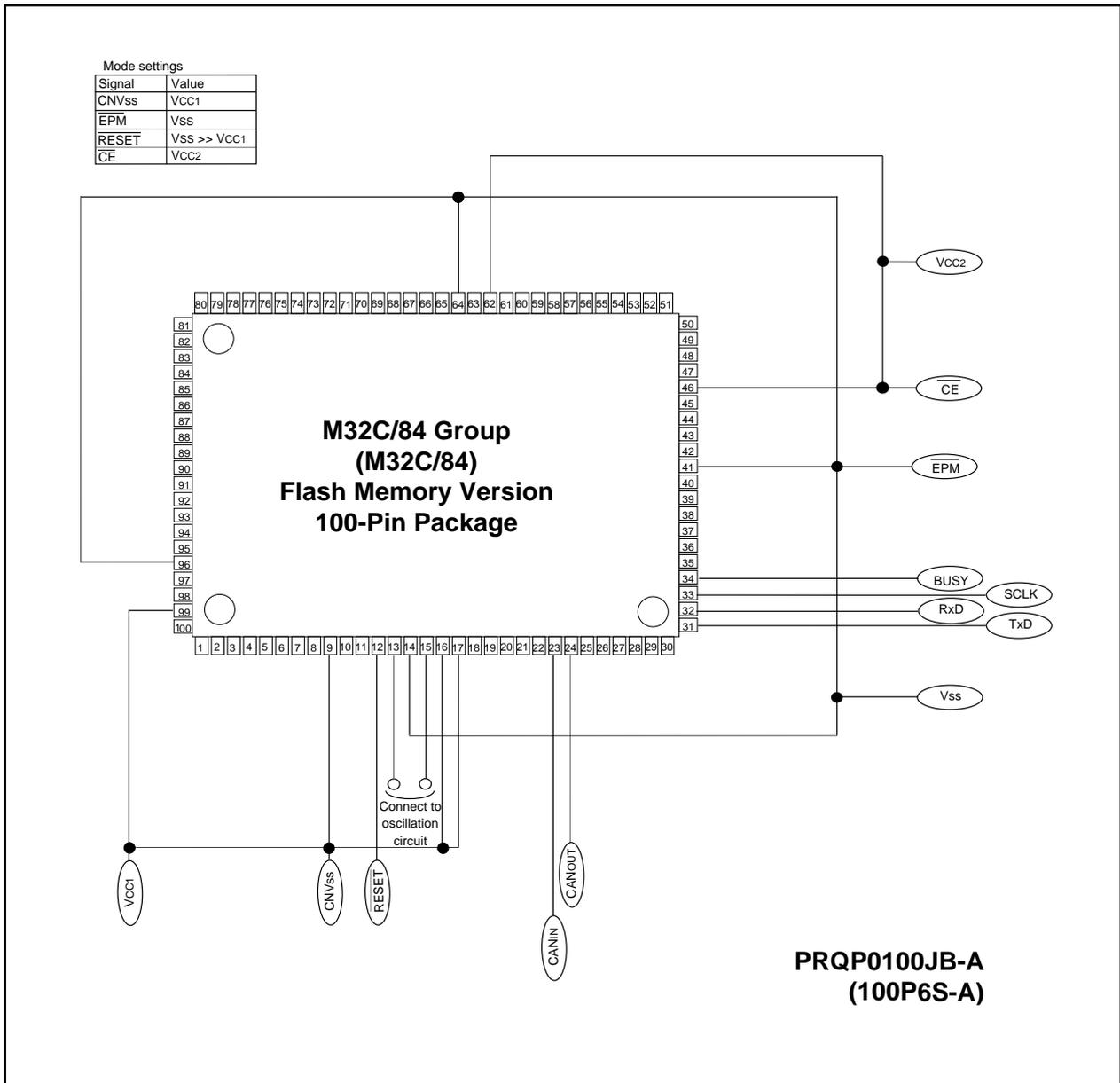


Figure 25.14 Pin Connections in Standard Serial I/O Mode (1)

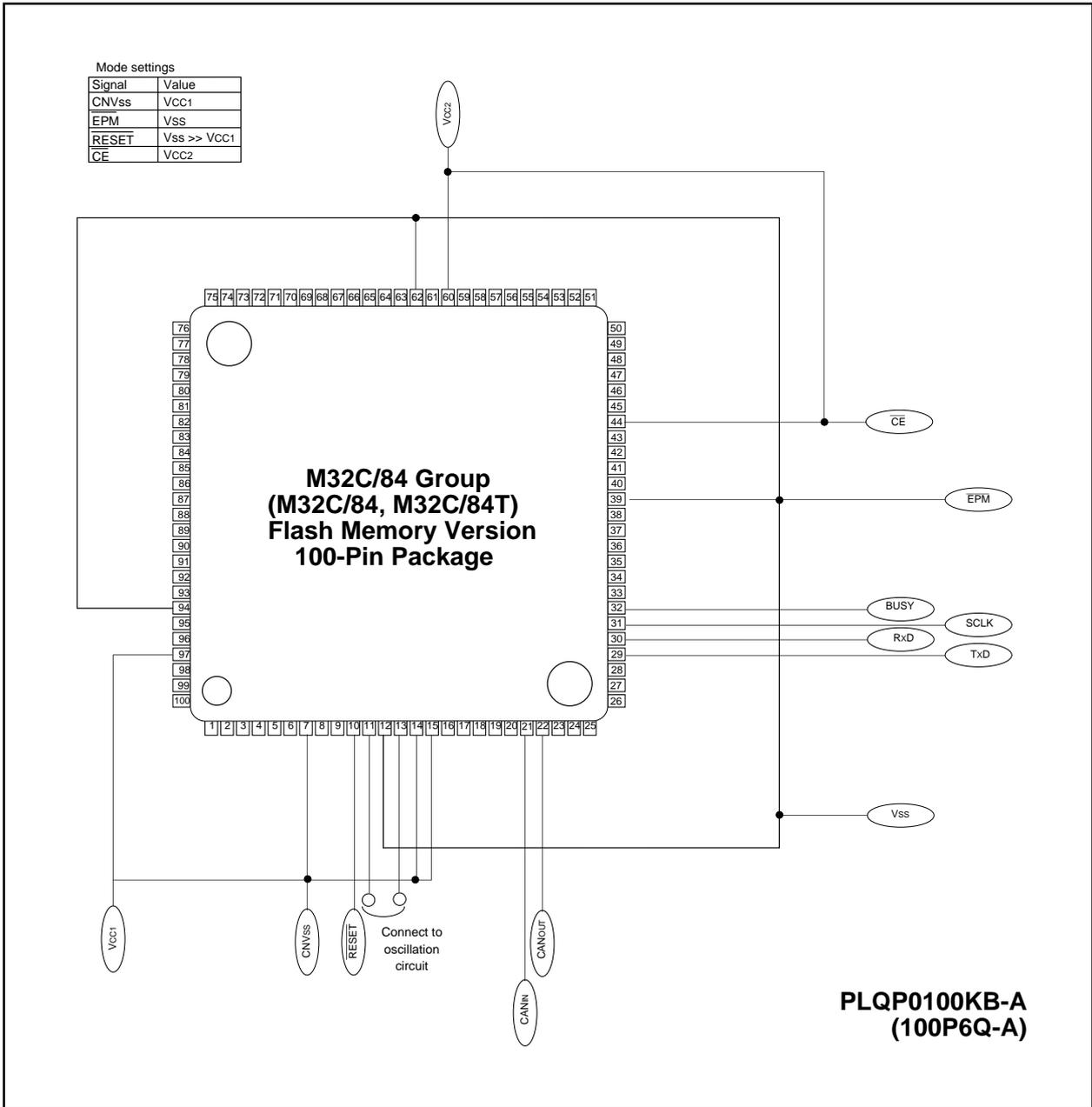


Figure 25.15 Pin Connections in Standard Serial I/O Mode (2)

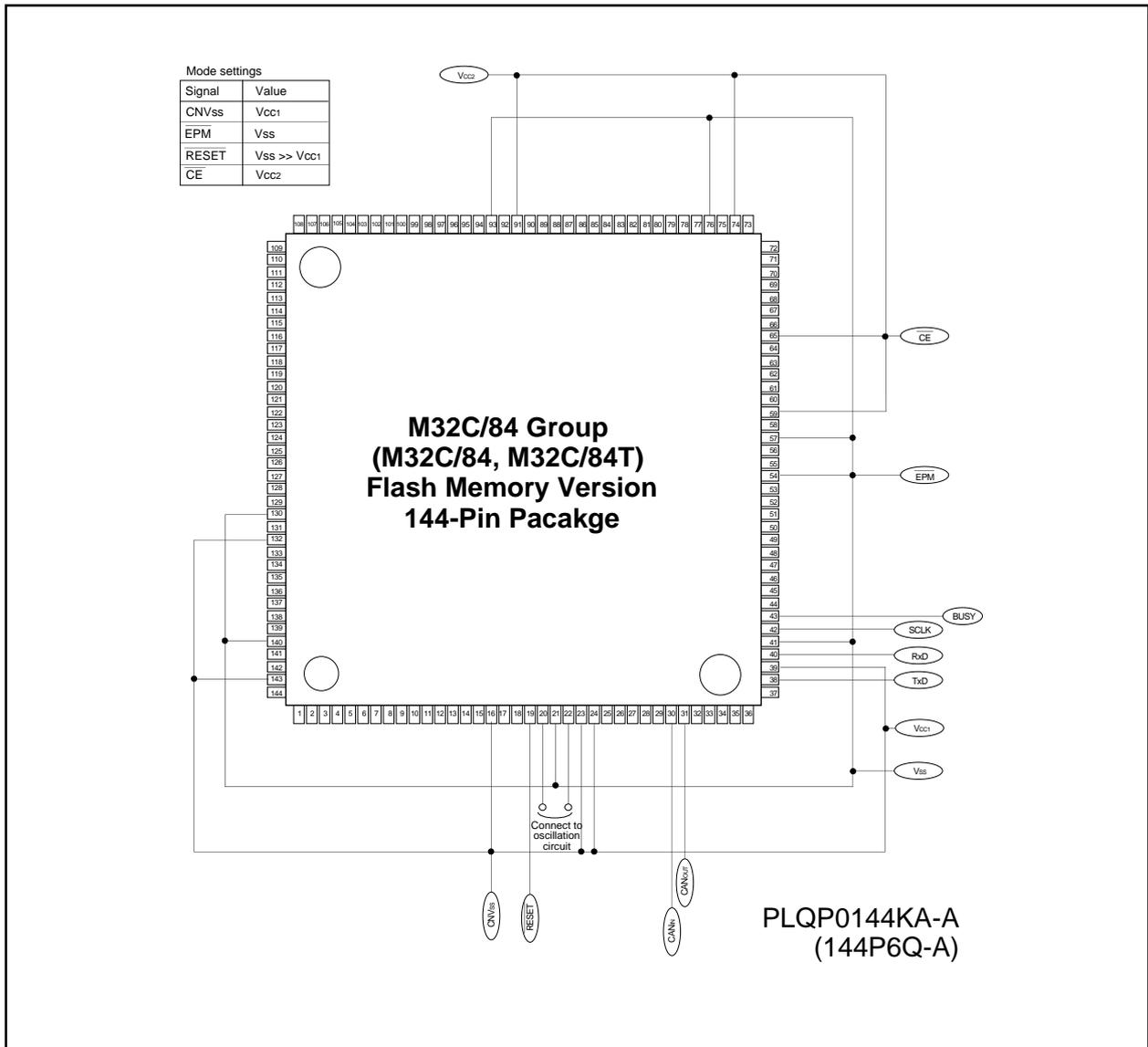


Figure 25.16 Pin Connections in Standard Serial I/O Mode (3)

25.4.2 Circuit Application in Standard Serial I/O Mode

Figure 25.17 shows an example of a circuit application in standard serial I/O mode 1. Figure 25.18 shows an example of a circuit application serial I/O mode 2. Figure 25.19 shows an example of a circuit application serial I/O mode 3. Refer to the user's manual of your serial programmer to handle pins controlled by the serial programmer.

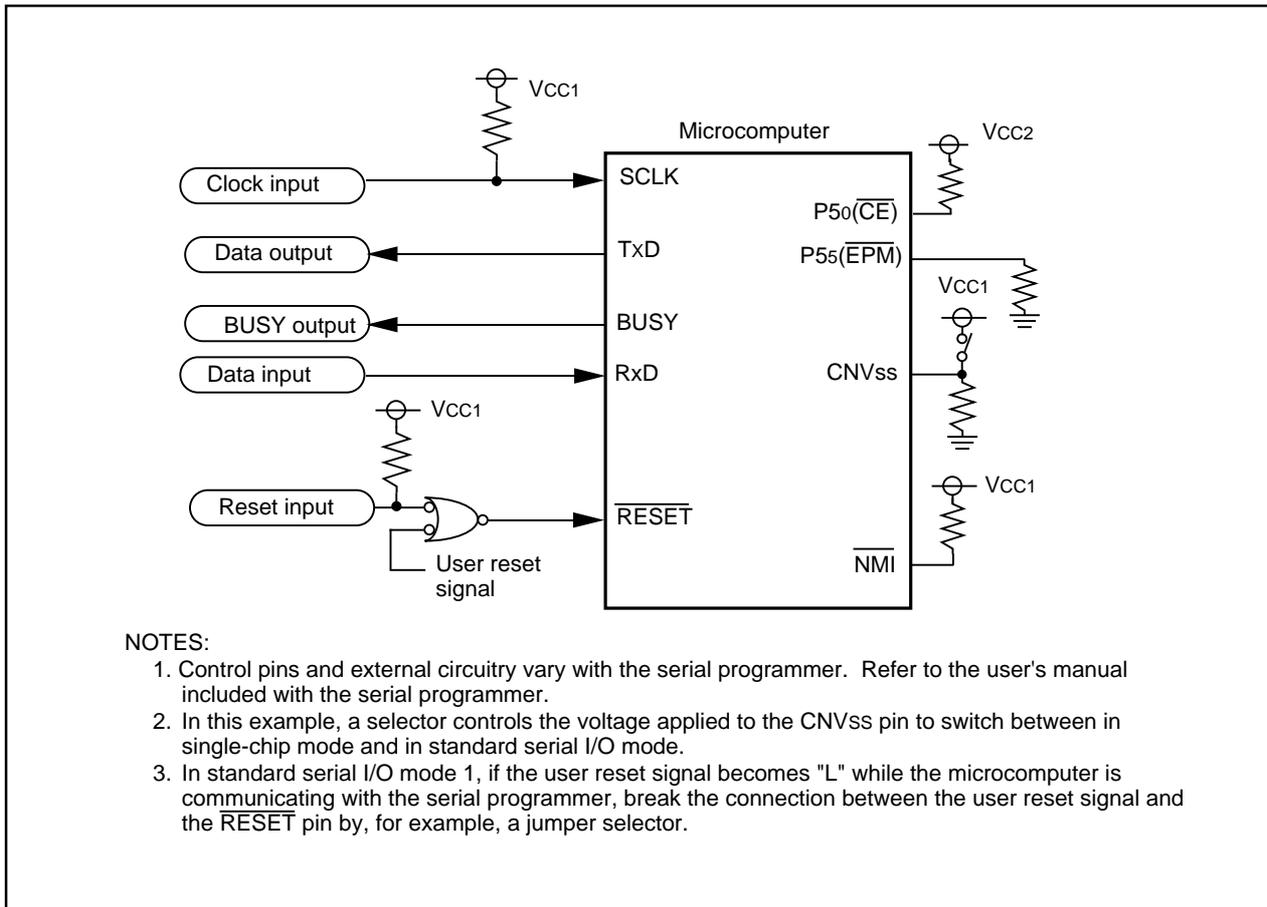


Figure 25.17 Circuit Application in Standard Serial I/O Mode 1

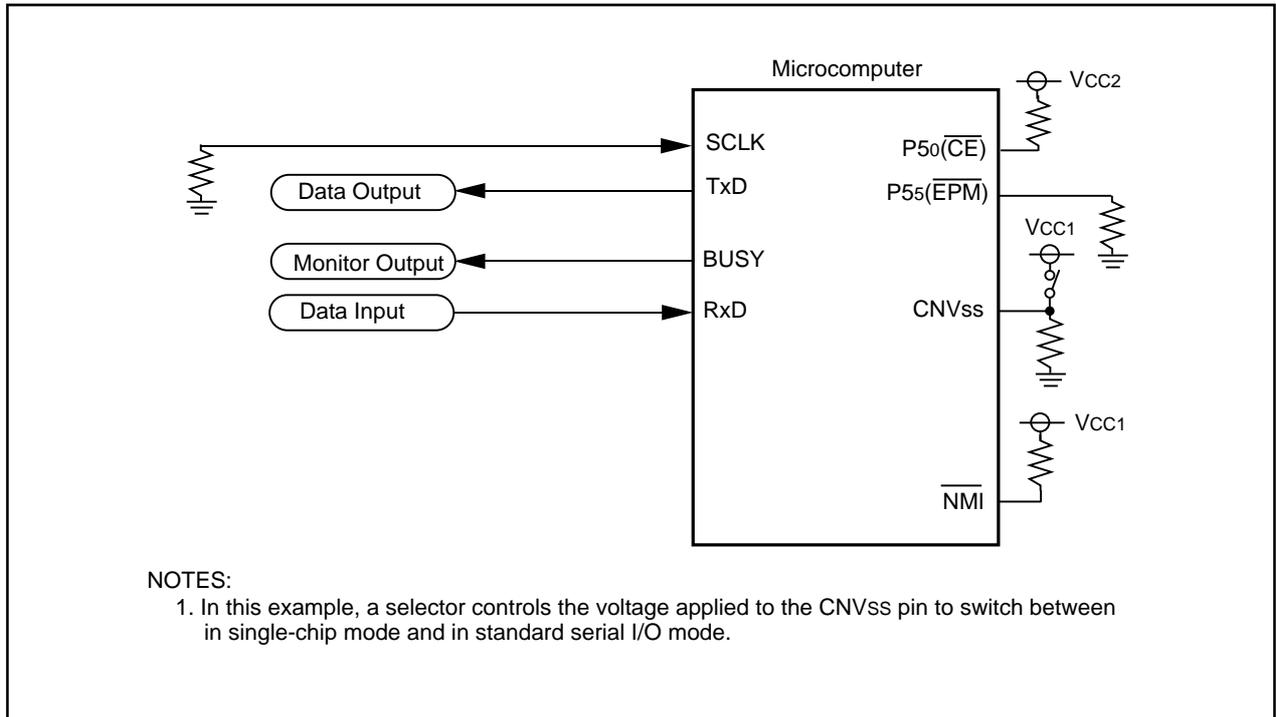


Figure 25.18 Circuit Application in Standard Serial I/O Mode 2

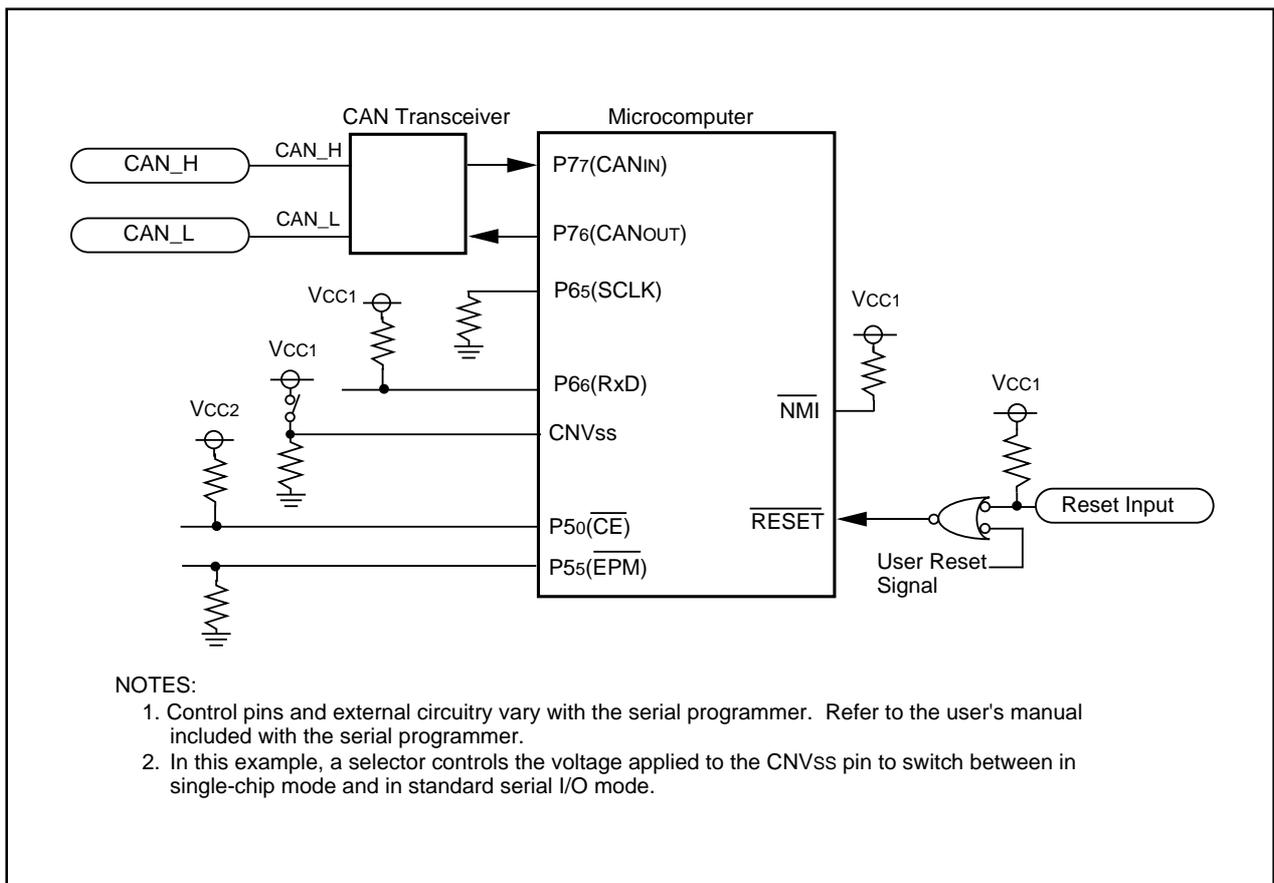


Figure 25.19 Circuit Application in Standard Serial I/O Mode 3

25.5 Parallel I/O Mode

In parallel I/O mode, the user ROM area and the boot ROM area can be rewritten by a parallel programmer supporting the M32C/85 Group (M32C/85, M32C/85T). Contact your parallel programmer manufacturer for more information on the parallel programmer. Refer to the user's manual included with your parallel programmer for instructions.

25.5.1 Boot ROM Area

An erase block operation in the boot ROM area is applied to only one 4-Kbyte block. The rewrite control program in standard serial I/O mode is written in the boot ROM area before shipment. Do not rewrite the boot ROM area if using the serial programmer.

In parallel I/O mode, the boot ROM area is located in addresses FFF000₁₆ to FFFFFFF₁₆. Rewrite this address range only if rewriting the boot ROM area. (Do not access addresses other than addresses FFF000₁₆ to FFFFFFF₁₆.)

25.5.2 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten in parallel I/O mode. (Refer to **25.2 Functions to Prevent Flash Memory from Rewriting.**)

26. Electrical Characteristics

26.1 Electrical Characteristics (M32C/84)

Table 26.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V _{CC1} , V _{CC2}	Supply Voltage		V _{CC1} =AV _{CC}	-0.3 to 6.0	V
V _{CC2}	Supply Voltage		-	-0.3 to V _{CC1}	V
AV _{CC}	Analog Supply Voltage		V _{CC1} =AV _{CC}	-0.3 to 6.0	V
V _i	Input Voltage	RESET, CNV _{SS} , BYTE, P60-P67, P72-P77, P80-P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾ , V _{REF} , X _{IN}		-0.3 to V _{CC1} +0.3	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽¹⁾		-0.3 to V _{CC2} +0.3	
		P70, P71		-0.3 to 6.0	
V _o	Output Voltage	P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾ , X _{OUT}		-0.3 to V _{CC1} +0.3	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽¹⁾		-0.3 to V _{CC2} +0.3	
		P70, P71		-0.3 to 6.0	
P _d	Power Dissipation		T _{opr} =25° C	500	mW
T _{opr}	Operating Ambient Temperature	during CPU operation		-20 to 85/ -40 to 85 ⁽²⁾	° C
		during flash memory program and erase operation		0 to 60	
T _{stg}	Storage Temperature			-65 to 150	° C

NOTES:

- P11 to P15 are provided in the 144-pin package only.
- Contact Renesas Technology Sales Co., Ltd, if temperature range of -40 to 85° C is required.

Table 26.2 Recommended Operating Conditions
(VCC1= VCC2=3.0V to 5.5V at Topr=– 20 to 85°C unless otherwise specified)

Symbol	Parameter	Standard			Unit	
		Min.	Typ.	Max.		
VCC1, VCC2	Supply Voltage (VCC1≥ VCC2)	3.0	5.0	5.5	V	
AVCC	Analog Supply Voltage		VCC1		V	
VSS	Supply Voltage		0		V	
AVSS	Analog Supply Voltage		0		V	
VIH	Input High ("H") Voltage	P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽⁴⁾	0.8VCC2		VCC2	V
		P60-P67, P72-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, P140-P146, P150-P157 ⁽⁴⁾ , XIN, RESET, CNVSS, BYTE	0.8VCC1		VCC1	
		P70, P71	0.8VCC1		6.0	
		P00-P07, P10-P17 (in single-chip mode)	0.8VCC2		VCC2	
		P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)	0.5VCC2		VCC2	
VIL	Input Low ("L") Voltage	P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽⁴⁾	0		0.2VCC2	V
		P60-P67, P70-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, P140-P146, P150-P157 ⁽⁴⁾ , XIN, RESET, CNVSS, BYTE	0		0.2VCC1	
		P00-P07, P10-P17 (in single-chip mode)	0		0.2VCC2	
		P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)	0		0.16VCC2	
IOH(peak)	Peak Output High ("H") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			-10.0	mA
IOH(avg)	Average Output High ("H") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			-5.0	mA
IOL(peak)	Peak Output Low ("L") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			10.0	mA
IOL(avg)	Average Output Low ("L") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			5.0	mA

NOTES:

- Typical values when average output current is 100ms.
- Total IOL(peak) for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be 80mA or less.
Total IOL(peak) for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be 80mA or less.
Total IOH(peak) for P0, P1, P2, and P11 must be -40mA or less.
Total IOH(peak) for P86, P87, P9, P10, P14 and P15 must be -40mA or less.
Total IOH(peak) for P3, P4, P5, P12 and P13 must be -40mA or less.
Total IOH(peak) for P6, P7, and P80 to P84 must be -40mA or less.
- VIH and VIL reference for P87 applies when P87 is used as a programmable input port.
It does not apply when P87 is used as XCIN.
- P11 to P15 are provided in the 144-pin package only.

Table 26.2 Recommended Operating Conditions (Continued)
(V_{CC1}=V_{CC2}=3.0V to 5.5V at Topr=-20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f(BCLK)	CPU Clock Frequency	V _{CC1} =4.2 to 5.5V	0		32	MHz
		V _{CC1} =3.0 to 5.5V	0		24	MHz
f(XIN)	Main Clock Input Frequency	V _{CC1} =4.2 to 5.5V	0		32	MHz
		V _{CC1} =3.0 to 5.5V	0		24	MHz
f(XCIN)	Sub Clock Frequency		32.768	50	kHz	
f(Ring)	On-chip Oscillator Frequency (V _{CC1} =V _{CC2} =5.0V, Topr=25° C)		0.5	1	2	MHz
f(PLL)	PLL Clock Frequency	V _{CC1} =4.2 to 5.5V	10		32	MHz
		V _{CC1} =3.0 to 5.5V	10		24	MHz
t _{SU(PLL)}	Wait Time to Stabilize PLL Frequency Synthesizer	V _{CC1} =5.0V			5	ms
		V _{CC1} =3.3V			10	ms

$V_{CC1}=V_{CC2}=5V$

Table 26.3 Electrical Characteristics**($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$, $f(BCLK)=32MHz$ unless otherwise specified)**

Symbol	Parameter	Condition	Standard			Unit		
			Min.	Typ.	Max.			
V _{OH}	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137	I _{OH} =-5mA	V _{CC2} -2.0		V _{CC2}	V	
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-5mA	V _{CC1} -2.0		V _{CC1}		
	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137	I _{OH} =-200μA	V _{CC2} -0.3		V _{CC2}	V		
			V _{CC1} -0.3		V _{CC1}			
	X _{OUT}	I _{OH} =-1mA	3.0		V _{CC1}	V		
	X _{COUT}	High Power	No load applied		2.5		V	
	Low Power	No load applied		1.6				
V _{OL}	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =5mA			2.0	V	
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =200μA			0.45	V	
	X _{OUT}	I _{OL} =1mA			2.0	V		
	X _{COUT}	High Power	No load applied		0		V	
		Low Power	No load applied		0			
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, K10-K13, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V	
		RESET		0.2		1.8	V	
I _{IH}	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =5V			5.0	μA	
I _{IL}	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-5.0	μA	
R _{PULLUP}	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I =0V	Flash Memory	30	50	167	kΩ
				Masked ROM	20	40	167	
R _{fXIN}	Feedback Resistance	X _{IN}				1.5	MΩ	
R _{fXCIN}	Feedback Resistance	X _{CIN}				10	MΩ	
V _{RAM}	RAM Standby Voltage	In stop mode				2.0	V	

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

Table 26.3 Electrical Characteristics (Continued)**($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(BCLK)=32MHz$ unless otherwise specified)**

Symbol	Parameter	Measurement Condition		Standard			Unit	
				Min.	Typ.	Max.		
I _{CC}	Power Supply Current	In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(BCLK)=32 MHz, Square wave, No division			28	45	mA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM	Flash Memory		430		μA
				Masked ROM		25		
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on RAM ⁽¹⁾			25		μA
			f(BCLK)=32 kHz, In wait mode, T _{opr} =25° C			10		μA
			While clock stops, T _{opr} =25° C			0.8	5	μA
While clock stops, T _{opr} =85° C				50	μA			

NOTES:

- Value is obtained when setting the FMSTP bit in the FMR0 register to "1" (flash memory stopped).

$V_{CC1}=V_{CC2}=5V$

Table 26.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}=4.2$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$, $f(BCLK) = 32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$	AN ₀ to AN ₇ , AN ₀₀ to AN ₀₇ , AN ₂₀ to AN ₂₇ , AN ₁₅₀ to AN ₁₅₇ , ANEX ₀ , ANEX ₁			±3	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
RLADDER	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	kΩ
t _{CONV}	10-bit Conversion Time ^(1, 2)			2.06			μs
t _{CONV}	8-bit Conversion Time ^(1, 2)			1.75			μs
t _{SAMP}	Sampling Time ⁽¹⁾			0.188			μs
V _{REF}	Reference Voltage			2		V _{CC1}	V
V _{IA}	Analog Input Voltage			0		V _{REF}	V

NOTES:

1. Divide $f(X_{IN})$, if exceeding 16 MHz, to keep ϕ_{AD} frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 26.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}=4.2$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$, $f(BCLK) = 32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution					8	Bits
-	Absolute Accuracy					1.0	%
t _{SU}	Setup Time					3	μs
R _O	Output Resistance			4	10	20	kΩ
I _{VREF}	Reference Power Supply Input Current	(Note 1)				1.5	mA

NOTES:

1. Measurement when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter, not being used, is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Table 26.6 Flash Memory Version Electrical Characteristics (V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at Topr=0 to 60°C unless otherwise specified)

Symbol	Parameter	Standard			Unit	
		Min.	Typ.	Max.		
-	Program and Erase Endurance ⁽²⁾	100			cycles	
-	Word Program Time (V _{CC1} =5.0V, Topr=25° C)		25	200	μs	
-	Lock Bit Program Time		25	200	μs	
-	Block Erase Time (V _{CC1} =5.0V, Topr=25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time ⁽¹⁾			4 x //	s	
t _{PS}	Wait Time to Stabilize Flash Memory Circuit			15	μs	
-	Data Hold Time (Topr=-40 to 85 ° C)	10			years	

NOTES:

1. //denotes the number of block to be erased.

2. Number of program-erase cycles per block.

If Program and Erase Endurance is //cycle (//≠100), each block can be erased and programmed //cycles. For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited).

$V_{CC1}=V_{CC2}=5V$

Table 26.7 Voltage Detection Circuit Electrical Characteristics ($V_{CC1}=V_{CC2}=3.0$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Low Voltage Detection Voltage ⁽¹⁾	$V_{CC1}=3.0$ to $5.5V$		3.8		V
Vdet3	Reset Space Detection Voltage ⁽¹⁾			3.0		V
Vdet3s	Low Voltage Reset Hold Voltage		2.0			V
Vdet3r	Low Voltage Reset Release Voltage ⁽²⁾			3.1		V

NOTES:

1. $V_{det4} > V_{det3}$
2. $V_{det3r} > V_{det3}$ is not guaranteed.

Table 26.8 Power Supply Timing

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	$V_{CC1}=3.0$ to $5.5V$			2	ms
td(S-R)	Wait Time to Release Brown-out. Detection Reset	$V_{CC1}=V_{det3r}$ to $5.5V$		6 ⁽¹⁾	20	ms
td(E-A)	Start-up Time for Low Voltage Detection Circuit Operation	$V_{CC1}=3.0$ to $5.5V$			20	μs

NOTES:

1. $V_{CC1}=5V$

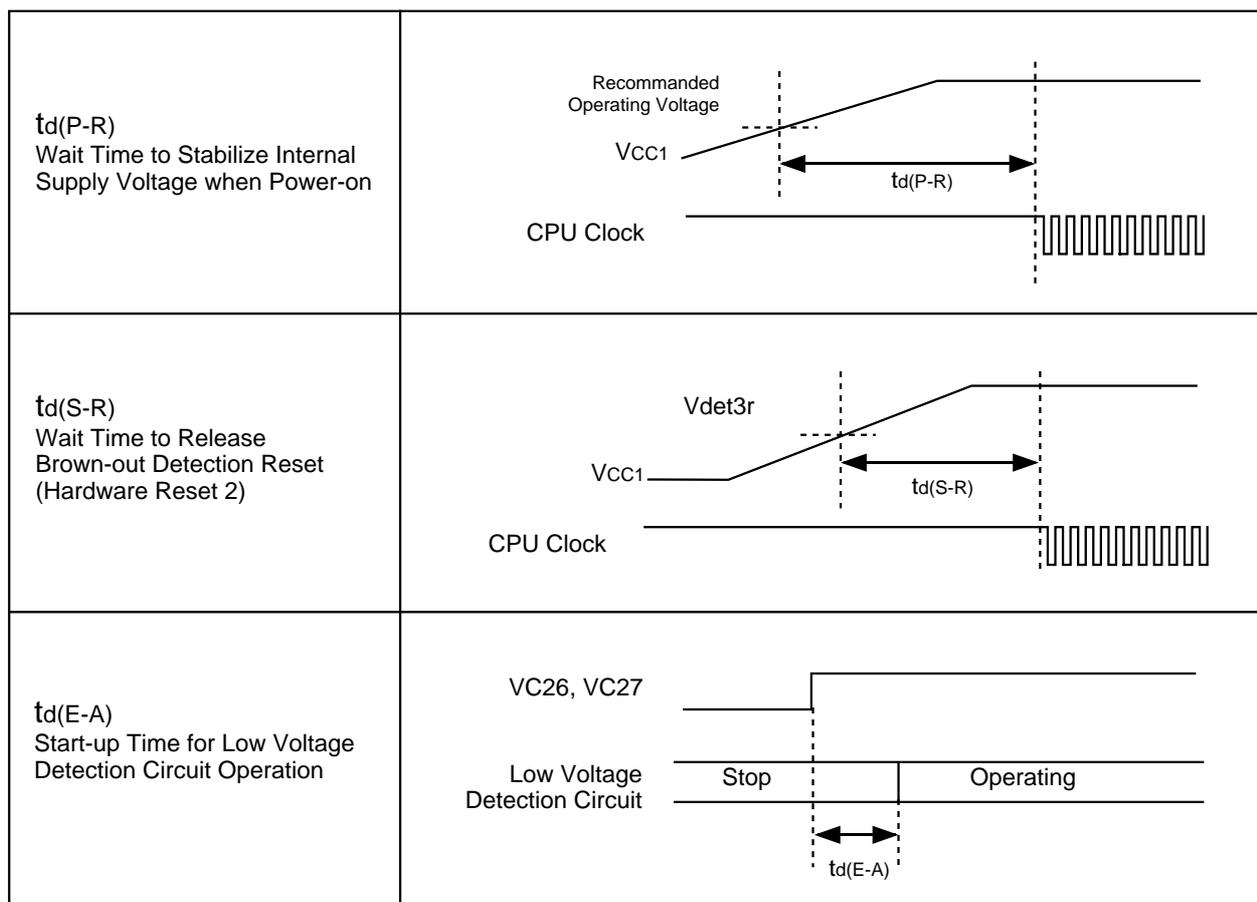


Figure 26.1 Power Supply Timing Diagram

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$ unless otherwise specified)

Table 26.9 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	31.25		ns
$t_{w(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	13.75		ns
t_r	External Clock Rise Time		5	ns
t_f	External Clock Fall Time		5	ns

Table 26.10 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexrd bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{su(RDY-BCLK)}$	\overline{RDY} Input Setup Time	26		ns
$t_{su(HOLD-BCLK)}$	\overline{HOLD} Input Setup Time	30		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	\overline{RDY} Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	\overline{HOLD} Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	\overline{HLDA} Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)+1)$$

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, n=a+b)$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)-1)$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, p=\{(a+b-1) \times 2\} + 1)$$

$V_{CC1}=V_{CC2}=5V$

Timing Requirements**($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{op}=-20$ to $85^{\circ}C$ unless otherwise specified)****Table 26.11 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 26.12 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 26.13 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 26.14 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 26.15 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements**($V_{CC1} = V_{CC2} = 4.2$ to $5.5V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)****Table 26.16 Timer B Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 26.17 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 26.18 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 26.19 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	\overline{ADTRG} Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	\overline{ADTRG} Input Low ("L") Width	125		ns

Table 26.20 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 26.21 External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} Input High ("H") Width	250		ns
$t_{w(INL)}$	\overline{INTi} Input Low ("L") Width	250		ns

$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 4.2$ to $5.5V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

**Table 26.22 Memory Expansion Mode and Microprocessor Mode
(when accessing external memory space)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See Figure 26.2		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		-3		ns
th(RD-AD)	Address Output Hold Time (RD standard) ⁽³⁾		0		ns
th(WR-AD)	Address Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
td(BCLK-CS)	Chip-Select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
th(RD-CS)	Chip-Select Signal Output Hold Time (RD standard) ⁽³⁾		0		ns
th(WR-CS)	Chip-Select Signal Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-5		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		-5		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 2)		ns
th(WR-DB)	Data Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
tW(WR)	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{W(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=(bx2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m= b)$$

3. t_c ns is added when recovery cycle is inserted.

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics**($V_{CC} = 4.2$ to $5.5V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)****Table 26.23 Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space with the multiplexed bus)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 26.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard) ⁽⁵⁾		(Note 1)		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard) ⁽⁵⁾		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard) ⁽⁵⁾		(Note 1)		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard) ⁽⁵⁾		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-5		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard) ⁽⁵⁾		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time (BCLK standard)		-2		ns
$t_{d(AD-ALE)}$	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
$t_{h(ALE-AD)}$	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
$t_{dz(RD-AD)}$	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [\text{ns}] \quad (\text{if external bus cycle is } a\phi + b\phi, m = (bx2)-1)$$

3. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$t_{d(AD-ALE)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 20 \quad [\text{ns}] \quad (\text{if external bus cycle is } a\phi + b\phi, n = a)$$

4. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$t_{h(ALE-AD)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}] \quad (\text{if external bus cycle is } a\phi + b\phi, n = a)$$

5. t_c ns is added when recovery cycle is inserted.

$$V_{CC1}=V_{CC2}=5V$$

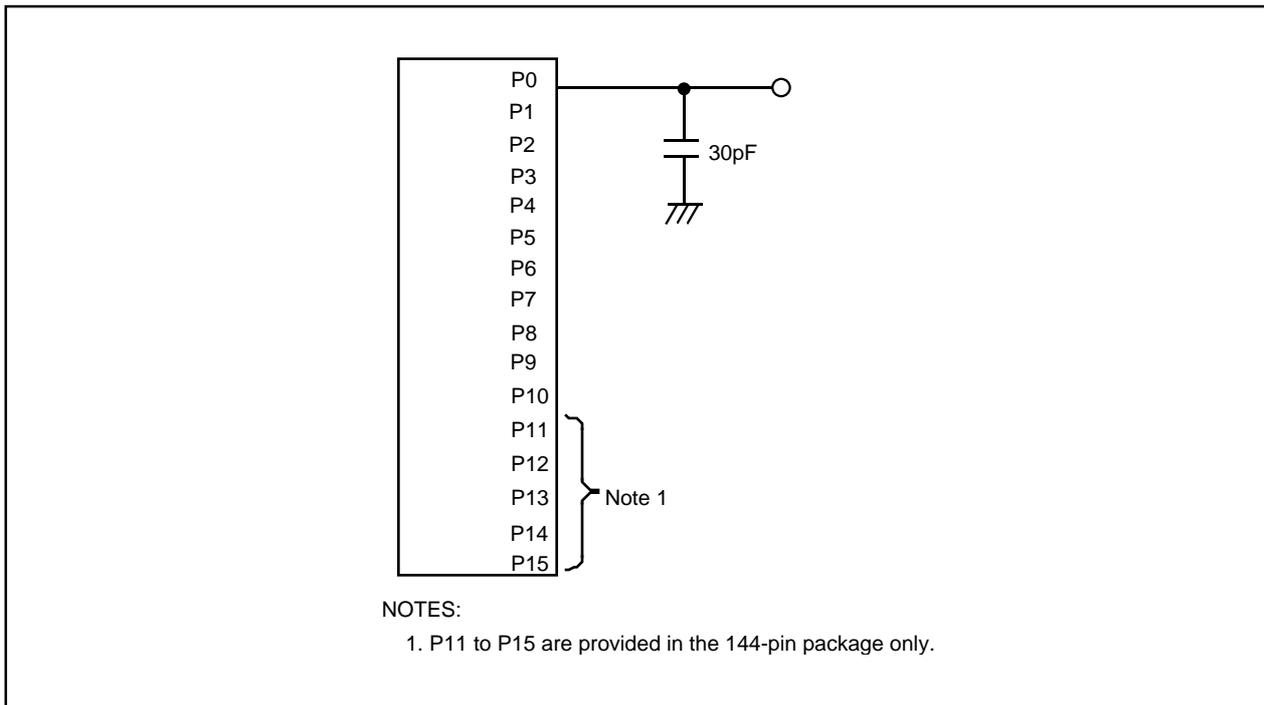


Figure 26.2 P0 to P15 Measurement Circuit

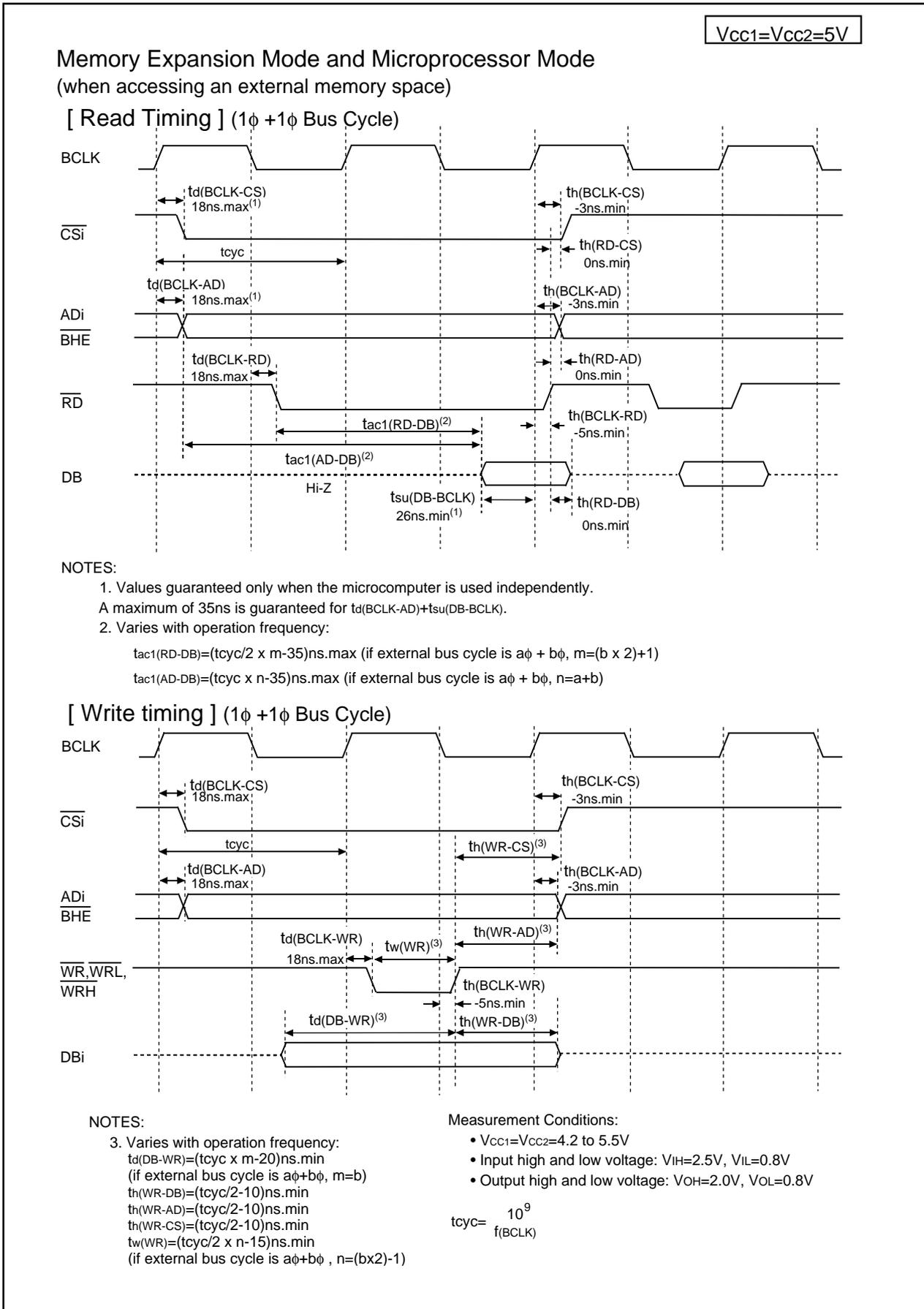


Figure 26.3 V_{CC1}=V_{CC2}=5V Timing Diagram (1)

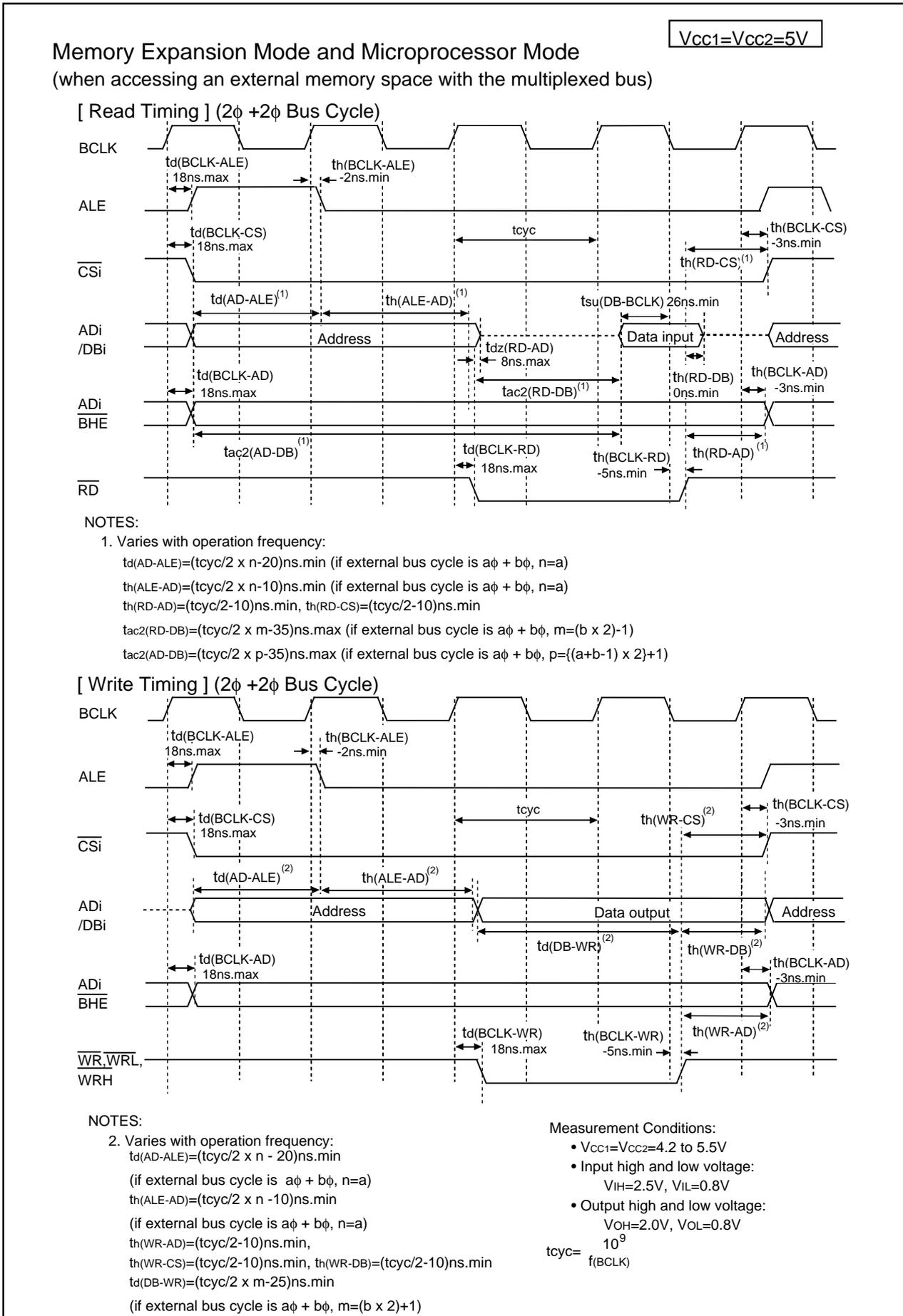


Figure 26.4 V_{CC1}=V_{CC2}=5V Timing Diagram (2)

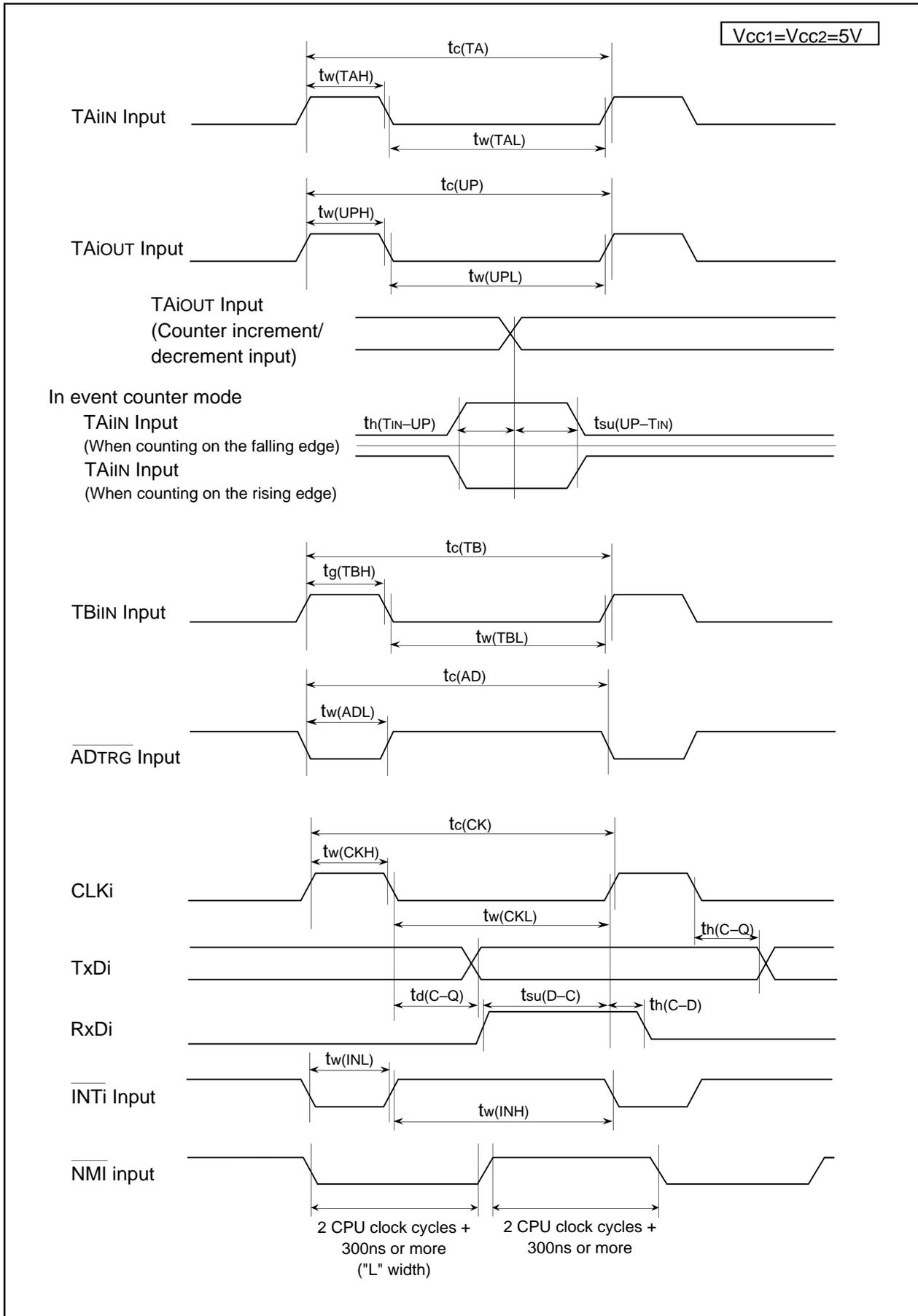


Figure 26.5 $V_{CC1}=V_{CC2}=5V$ Timing Diagram (3)

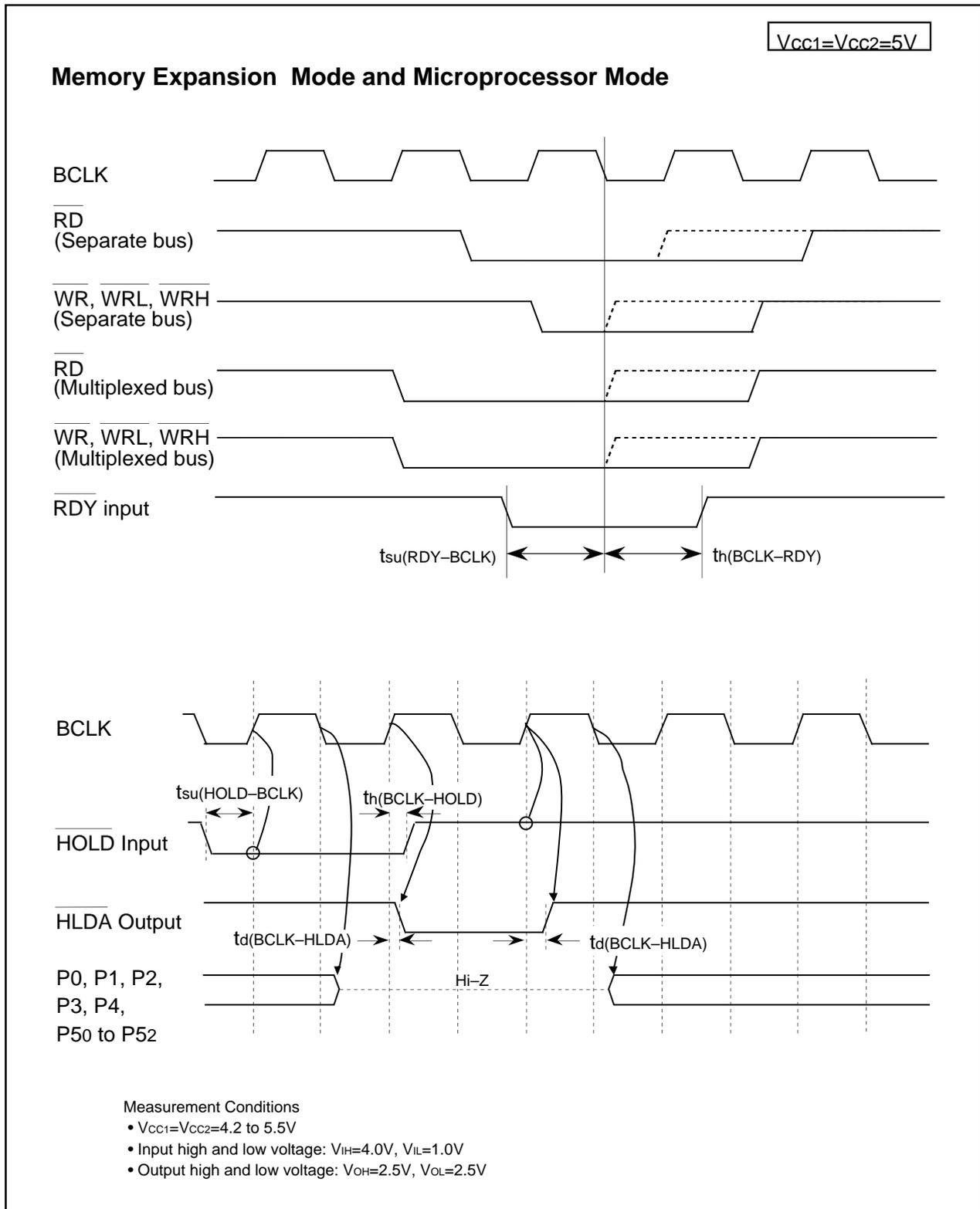


Figure 26.6 $V_{CC1}=V_{CC2}=5V$ Timing Diagram (4)

$V_{CC1}=V_{CC2}=3.3V$

Table 26.24 Electrical Characteristics ($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS}=0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(BCLK)=24MHz$ unless otherwise specified)

Symbol	Parameter	Condition	Standard			Unit			
			Min.	Typ.	Max.				
V _{OH}	Output High ("H") Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇	I _{OH} =-1mA	V _{CC2} -0.6		V _{CC2}	V		
		P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾		V _{CC1} -0.6		V _{CC1}	V		
	X _{OUT}	I _{OH} =-0.1mA	2.7		V _{CC1}	V			
	X _{COUT}	High Power	No load applied		2.5		V		
		Low Power	No load applied		1.6		V		
V _{OL}	Output Low ("L") Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾	I _{OL} =1mA			0.5	V		
		X _{OUT}	I _{OL} =0.1mA			0.5	V		
	X _{COUT}	High Power	No load applied		0		V		
		Low Power	No load applied		0		V		
	V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0 _{IN} -TA4 _{IN} , TB0 _{IN} -TB5 _{IN} , INT0-INT5, AD _{TRG} , CTS0-CTS4, CLK0-CLK4, TA0 _{OUT} -TA4 _{OUT} , NMI, K10-K13, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V	
RESET				0.2		1.8	V		
I _{IH}	Input High ("H") Current	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =3V			4.0	μA		
I _{IL}	Input Low ("L") Current	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₀ -P7 ₇ , P8 ₀ -P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-4.0	μA		
R _{PULLUP}	Pull-up Resistance	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾	V _I =0V	Flash Memory	66	120	500	kΩ	
				Masked ROM	40	70	500	kΩ	
R _{fXIN}	Feedback Resistance	X _{IN}				3.0	MΩ		
R _{fXCIN}	Feedback Resistance	X _{CIN}				20.0	MΩ		
V _{RAM}	RAM Standby Voltage	in stop mode			2.0		V		
I _{CC}	Power Supply Current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(BCLK)=24 MHz, Square wave, No division		22	35	mA		
				f(BCLK)=32 kHz, In wait mode, T _{opr} =25° C		10		μA	
					While clock stops, T _{opr} =25° C		0.8	5	μA
					While clock stops, T _{opr} =85° C			50	μA

NOTES:

- P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=3.3V$

Table 26.25 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}=3.0$ to $3.6V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(BCLK) = 24MHz$ unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
-	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	No S&H (8-bit)	$V_{CC1}=V_{CC2}=V_{REF}=3.3V$			± 2	LSB
DNL	Differential Nonlinearity Error	No S&H (8-bit)				± 1	LSB
-	Offset Error	No S&H (8-bit)				± 2	LSB
-	Gain Error	No S&H (8-bit)				± 2	LSB
RLADDER	Resistor Ladder		$V_{REF}=V_{CC1}$	8		40	k Ω
tCONV	8-bit Conversion Time ^(1, 2)			6.1			μs
VREF	Reference Voltage			3		V_{CC1}	V
VIA	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and Hold

NOTES:

1. Divide $f(X_{IN})$, if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.
2. S&H not available.

Table 26.26 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}=3.0$ to $3.6V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(BCLK) = 24MHz$ unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
-	Resolution					8	Bits
-	Absolute Accuracy					1.0	%
tsu	Setup Time					3	μs
Ro	Output Resistance			4	10	20	k Ω
I _{VREF}	Reference Power Supply Input Current		(Note 1)			1.0	mA

NOTES:

1. Measurement results when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter, not being used, is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$$V_{CC1}=V_{CC2}=3.3V$$

Timing Requirements

($V_{CC1}=V_{CC2}= 3.0$ to $3.6V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 26.27 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	41		ns
tw(H)	External Clock Input High ("H") Width	18		ns
tw(L)	External Clock Input Low ("L") Width	18		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 26.28 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tac1(RD-DB)	Data Input Access Time (RD standard)		(Note 1)	ns
tac1(AD-DB)	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
tac2(RD-DB)	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac2(AD-DB)	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tsu(DB-BCLK)	Data Input Setup Time	30		ns
tsu(RDY-BCLK)	\overline{RDY} Input Setup Time	40		ns
tsu(HOLD-BCLK)	HOLD Input Setup Time	60		ns
th(RD-DB)	Data Input Hold Time	0		ns
th(BCLK-RDY)	\overline{RDY} Input Hold Time	0		ns
th(BCLK-HOLD)	\overline{HOLD} Input Hold Time	0		ns
td(BCLK-HLDA)	\overline{HLDA} Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)+1)$$

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, n=a+b)$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)-1)$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, p=\{(a+b-1)x2\}+1)$$

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements**($V_{CC1}=V_{CC2}= 3.0$ to $3.6V$, $V_{SS}= 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)****Table 26.29 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 26.30 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 26.31 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 26.32 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 26.33 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{W(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{W(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{SU(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{H(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements**($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$ unless otherwise specified)****Table 26.34 Timer B Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TB _{iIN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TB _{iIN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TB _{iIN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TB _{iIN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TB _{iIN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TB _{iIN} Input Low ("L") Width (counted on both edges)	80		ns

Table 26.35 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TB _{iIN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TB _{iIN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TB _{iIN} Input Low ("L") Width	200		ns

Table 26.36 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TB _{iIN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TB _{iIN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TB _{iIN} Input Low ("L") Width	200		ns

Table 26.37 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	\overline{AD}_{TRG} Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	\overline{AD}_{TRG} Input Low ("L") Width	125		ns

Table 26.38 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK _i Input Cycle Time	200		ns
$t_{w(CKH)}$	CLK _i Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLK _i Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxD _i Output Delay Time		80	ns
$t_{h(C-Q)}$	TxD _i Hold Time	0		ns
$t_{su(D-C)}$	RxD _i Input Setup Time	30		ns
$t_{h(C-Q)}$	RxD _i Input Hold Time	90		ns

Table 26.39 External Interrupt \overline{INT}_i Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INT}_i Input High ("H") Width	250		ns
$t_{w(INL)}$	\overline{INT}_i Input Low ("L") Width	250		ns

$$V_{CC1}=V_{CC2}=3.3V$$

Switching Characteristics

($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

**Table 26.40 Memory Expansion Mode and Microprocessor Mode
(when accessing external memory space)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 26.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard) ⁽³⁾		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard) ⁽³⁾		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=(b \times 2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=b)$$

3. t_{cns} is added when recovery cycle is inserted.

$$V_{CC1}=V_{CC2}=3.3V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3.0$ to $3.6V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 26.41 Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space with the multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See Figure 26.2		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		0		ns
th(RD-AD)	Address Output Hold Time (RD standard) ⁽⁵⁾		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard) ⁽⁵⁾		(Note 1)		ns
td(BCLK-CS)	Chip-Select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
th(RD-CS)	Chip-Select Signal Output Hold Time (RD standard) ⁽⁵⁾		(Note 1)		ns
th(WR-CS)	Chip-Select Signal Output Hold Time (WR standard) ⁽⁵⁾		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-3		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(DB-WR)	Data Output delay Time (WR standard)		(Note 2)		ns
th(WR-DB)	Data Output Hold Time (WR standard) ⁽⁵⁾		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
tdz(RD-AD)	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained by the following equations, according to BCLK frequency.

$$th(RD - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

2. Values can be obtained by the following equations, according to BCLK frequency and external bus cycles.

$$td(DB - WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=(b+2)-1)$$

3. Values can be obtained by the following equations, according to BCLK frequency and external bus cycles.

$$td(AD - ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=a)$$

4. Values can be obtained by the following equations, according to BCLK frequency and external bus cycles.

$$th(ALE - AD) = \frac{10^9 \times n}{f(BCLK) \times 2} - 10 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=a)$$

5. t_c ns is added when recovery cycle is inserted.

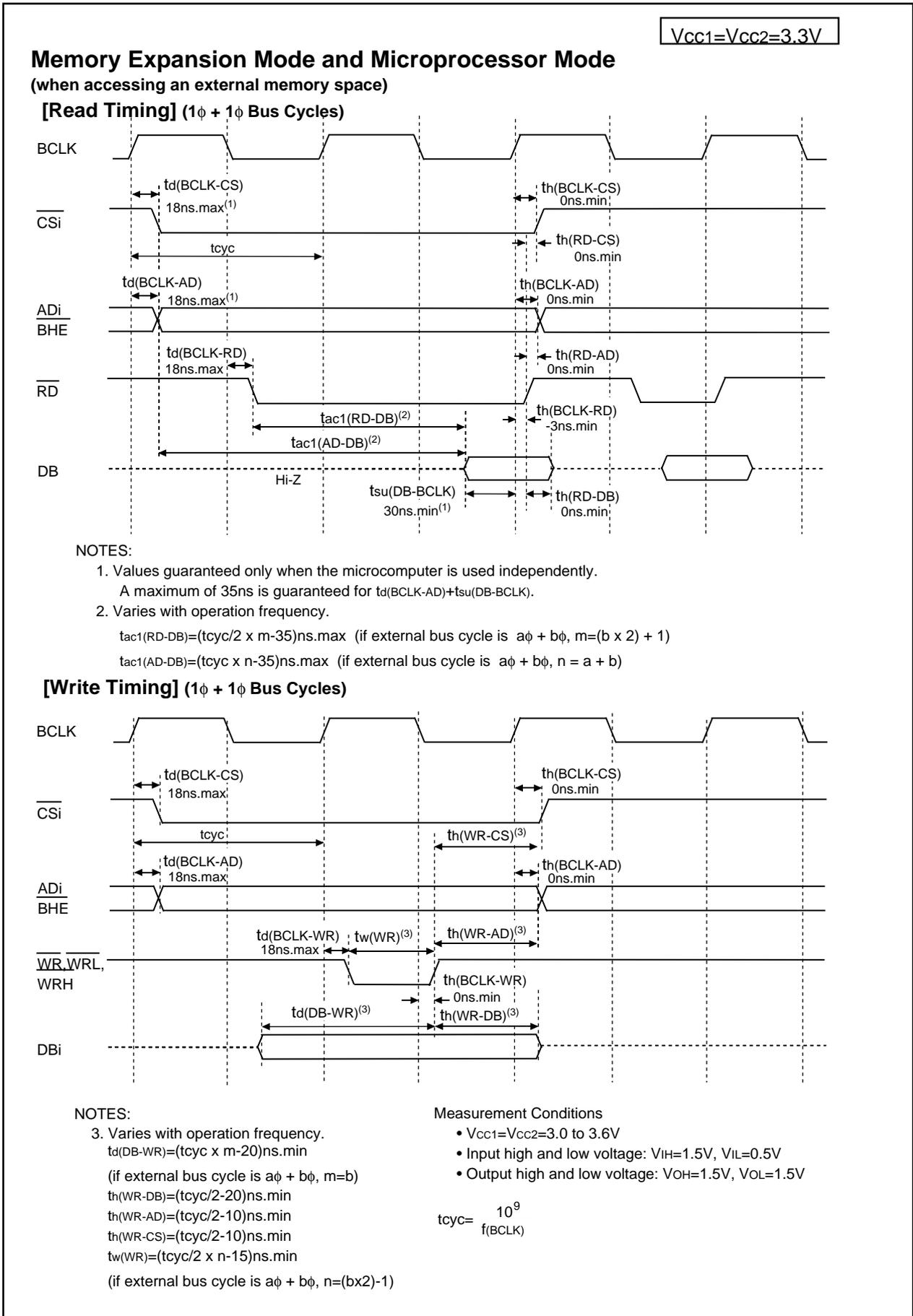


Figure 26.7 V_{CC1}=V_{CC2}=3.3V Timing Diagram (1)

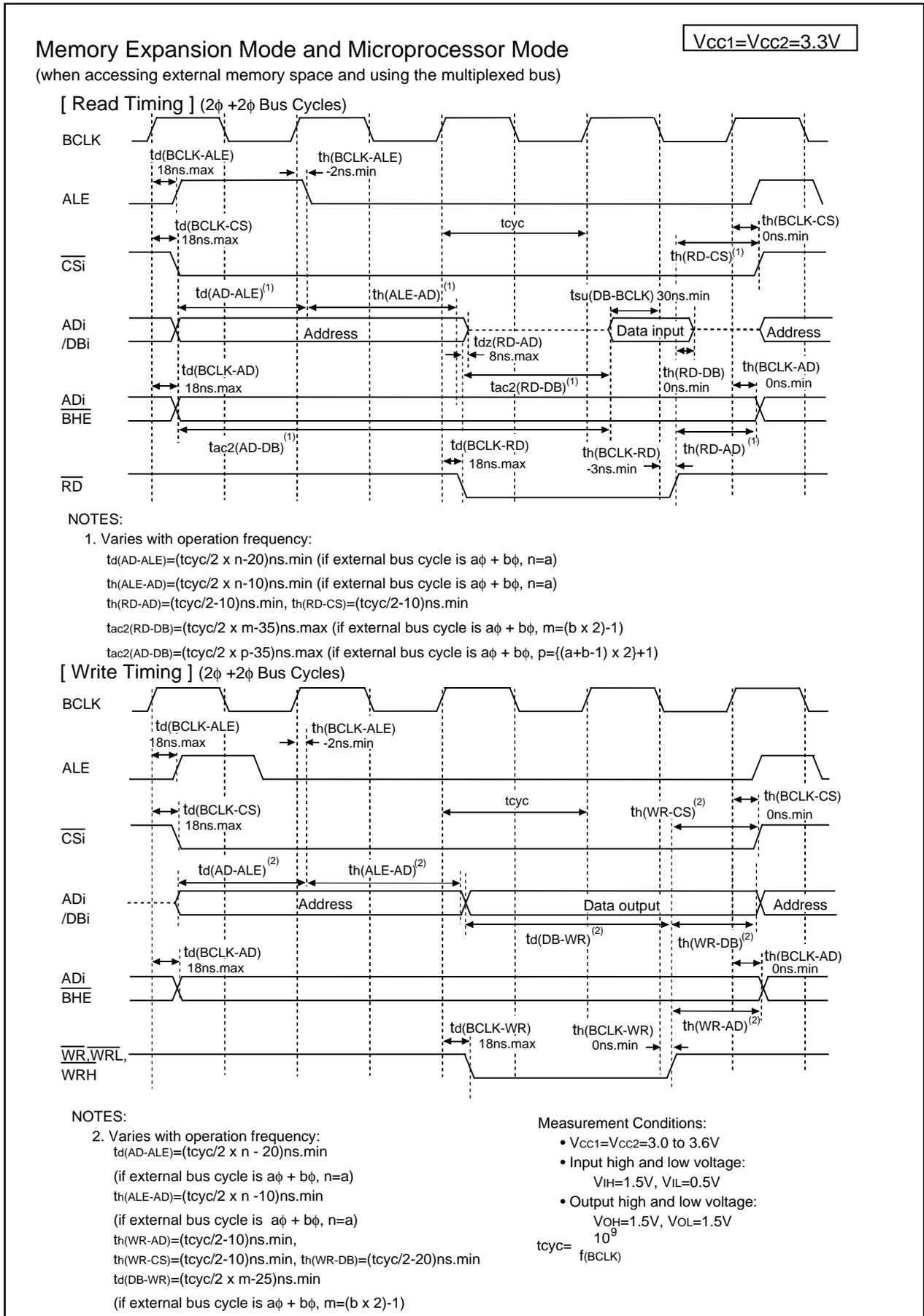


Figure 26.8 V_{CC1}=V_{CC2}=3.3V Timing Diagram (2)

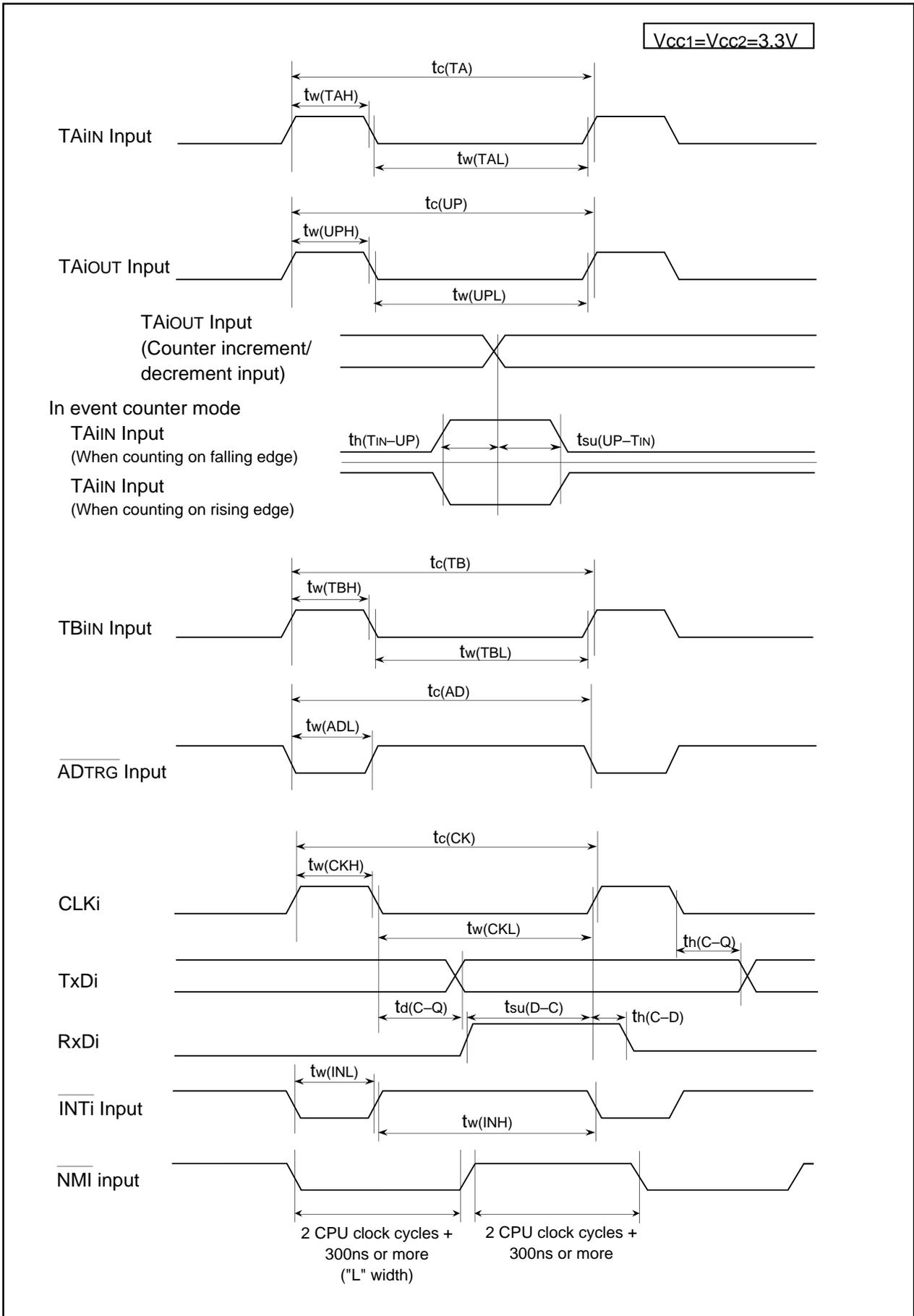


Figure 26.9 V_{CC1}=V_{CC2}=3.3V Timing Diagram (3)

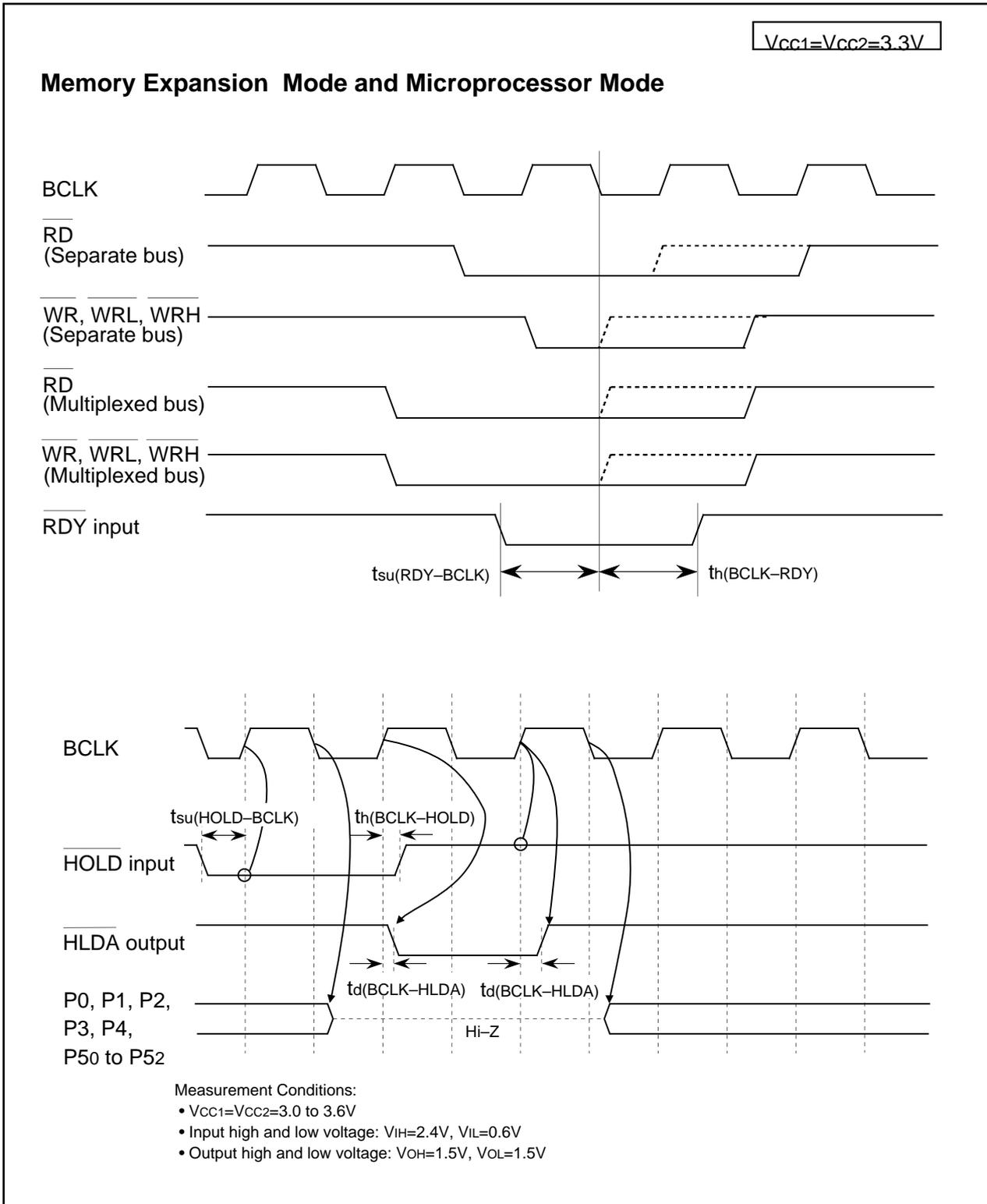


Figure 26.10 $V_{CC1}=V_{CC2}=3.3V$ Timing Diagram (4)

26.2 Electrical Characteristics (M32C/84T)

Table 26.42 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V _{CC1} , V _{CC2}	Supply Voltage		V _{CC1} =V _{CC2} =AV _{CC}	-0.3 to 6.0	V
AV _{CC}	Analog Supply Voltage		V _{CC1} =V _{CC2} =AV _{CC}	-0.3 to 6.0	V
V _I	Input Voltage	RESET, CNV _{SS} , BYTE, P60-P67, P72-P77, P80-P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾ , V _{REF} , X _{IN}		-0.3 to V _{CC1} +0.3	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽¹⁾		-0.3 to V _{CC2} +0.3	
		P70, P71		-0.3 to 6.0	
V _O	Output Voltage	P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾ , X _{OUT}		-0.3 to V _{CC1} +0.3	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽¹⁾		-0.3 to V _{CC2} +0.3	
		P70, P71		-0.3 to 6.0	
P _d	Power Dissipation		T _{opr} =25° C	500	mW
T _{opr}	Operating Ambient Temperature	during CPU operation	T version	-40 to 85	° C
		during flash memory program and erase operation		0 to 60	
T _{stg}	Storage Temperature			-65 to 150	° C

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

Table 26.43 Recommended Operating Conditions**(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)**

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V _{CC1} , V _{CC2}	Supply Voltage (V _{CC1} ≥ V _{CC2})		4.2	5.0	5.5	V
A _{VCC}	Analog Supply Voltage			V _{CC1}		V
V _{SS}	Supply Voltage			0		V
A _{VSS}	Analog Supply Voltage			0		V
V _{IH}	Input High ("H") Voltage	P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽⁴⁾	0.8V _{CC2}		V _{CC2}	V
		P60-P67, P72-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, P140-P146, P150-P157 ⁽⁴⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	0.8V _{CC1}		V _{CC1}	
		P70, P71	0.8V _{CC1}		6.0	
		P00-P07, P10-P17	0.8V _{CC2}		V _{CC2}	
V _{IL}	Input Low ("L") Voltage	P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽⁴⁾	0		0.2V _{CC2}	V
		P60-P67, P70-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, P140-P146, P150-P157 ⁽⁴⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	0		0.2V _{CC1}	
		P00-P07, P10-P17	0		0.2V _{CC2}	
I _{OH(peak)}	Peak Output High ("H") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			-10.0	mA
I _{OH(avg)}	Average Output High ("H") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			-5.0	mA
I _{OL(peak)}	Peak Output Low ("L") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			10.0	mA
I _{OL(avg)}	Average Output Low ("L") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			5.0	mA

NOTES:

- Typical values when average output current is 100ms.
- Total I_{OL(peak)} for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be 80mA or less.
Total I_{OL(peak)} for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be 80mA or less.
Total I_{OH(peak)} for P0, P1, P2, and P11 must be -40mA or less.
Total I_{OH(peak)} for P86, P87, P9, P10, P14 and P15 must be -40mA or less.
Total I_{OH(peak)} for P3, P4, P5, P12 and P13 must be -40mA or less.
Total I_{OH(peak)} for P6, P7, and P80 to P84 must be -40mA or less.
- V_{IH} and V_{IL} reference for P87 applies when P87 is used as a programmable input port.
It does not apply when P87 is used as X_{CIN}.
- P11 to P15 are provided in the 144-pin package only.

Table 26.43 Recommended Operating Conditions (Continued)**(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at T_{opr} = -40 to 85°C (T version) unless otherwise specified)**

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f(BCLK)	CPU Input Frequency	V _{CC1} =4.2 to 5.5V	0		32	MHz
f(XIN)	Main Clock Input Frequency	V _{CC1} =4.2 to 5.5V	0		32	MHz
f(XCIN)	Sub Clock Frequency			32.768	50	kHz
f(Ring)	On-chip Oscillator Frequency (V _{CC1} =V _{CC2} =5.0V, T _{opr} =25° C)		0.5	1	2	MHz
f(PLL)	PLL Clock Frequency	V _{CC1} =4.2 to 5.5V	10		32	MHz
t _{SU(PLL)}	Wait Time to Stabilize PLL Frequency Synthesizer	V _{CC1} =5.0V			5	ms

$V_{CC1}=V_{CC2}=5V$

Table 26.44 Electrical Characteristics

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr} = -40$ to $85^{\circ}C$ (T version),
 $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit	
				Min.	Typ.	Max.		
V _{OH}	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137	I _{OH} =-5mA	V _{CC2} -2.0		V _{CC2}	V	
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-5mA	V _{CC1} -2.0		V _{CC1}		
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137	I _{OH} =-200μA	V _{CC2} -0.3		V _{CC2}	V	
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-200μA	V _{CC1} -0.3		V _{CC1}		
		X _{OUT}	I _{OH} =-1mA	3.0			V	
		X _{COUT}	High Power	No load applied		2.5		V
		Low Power	No load applied		1.6			
V _{OL}	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =5mA			2.0	V	
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =200μA			0.45	V	
		X _{OUT}	I _{OL} =1mA			2.0	V	
		X _{COUT}	High Power	No load applied		0		V
		Low Power	No load applied		0			
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V	
		RESET		0.2		1.8	V	
I _{IH}	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =5V			5.0	μA	
I _{IL}	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-5.0	μA	
R _{PULLUP}	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I =0V	Flash Memory	30	50	167	kΩ
R _{fXIN}	Feedback Resistance	X _{IN}				1.5	MΩ	
R _{fXCIN}	Feedback Resistance	X _{CIN}				10	MΩ	
V _{RAM}	RAM Standby Voltage	In stop mode			2.0		V	

NOTES:

- P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

Table 26.44 Electrical Characteristics (Continued)
**($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr} = -40$ to $85^{\circ}C$ (T version),
 $f(BCLK)=32MHz$ unless otherwise specified)**

Symbol	Parameter	Measurement Condition	Standard			Unit	
			Min.	Typ.	Max.		
I _{cc}	Power Supply Current	In single-chip mode, output pins are left open and other pins are connected to V _{ss} .	f(BCLK)=32 MHz, Square wave, No division		28	50	mA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM		430		μA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on RAM ⁽¹⁾		25		μA
			f(BCLK)=32 kHz, In wait mode, T _{opr} =25° C		10		μA
			While clock stops, T _{opr} =25° C		0.8	5	μA
			While clock stops, T _{opr} =85° C			50	μA

NOTES:

- Value is obtained when setting the FMSTP bit in the FMR0 register to "1" (flash memory stopped).

$V_{CC1}=V_{CC2}=5V$

Table 26.45 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=-40$ to $85^{\circ}C$ (T version), $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$	AN ₀ to AN ₇ , AN ₀₀ to AN ₀₇ , AN ₂₀ to AN ₂₇ , AN ₁₅₀ to AN ₁₅₇ , ANEX ₀ , ANEX ₁			± 3	LSB
			External op-amp connection mode			± 7	LSB
DNL	Differential Nonlinearity Error					± 1	LSB
-	Offset Error					± 3	LSB
-	Gain Error					± 3	LSB
RLADDER	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	k Ω
t _{CONV}	10-bit Conversion Time ^(1, 2)			2.06			μs
t _{CONV}	8-bit Conversion Time ^(1, 2)			1.75			μs
t _{SAMP}	Sampling Time ⁽¹⁾			0.188			μs
V _{REF}	Reference Voltage			2		V _{CC1}	V
V _{IA}	Analog Input Voltage			0		V _{REF}	V

NOTES:

1. Divide $f(X_{IN})$, if exceeding 16 MHz, to keep ϕ_{AD} frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 26.46 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=-40$ to $85^{\circ}C$ (T version), $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution					8	Bits
-	Absolute Accuracy					1.0	%
t _{SU}	Setup Time					3	μs
R _O	Output Resistance			4	10	20	k Ω
I _{VREF}	Reference Power Supply Input Current	(Note 1)				1.5	mA

NOTES:

1. Measurement when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter, not being used, is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Table 26.47 Flash Memory Version Electrical Characteristics
($V_{CC1}=4.5$ to $5.5V$, 3.0 to $3.6V$ at $T_{opr}=0$ to $60^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Standard			Unit	
		Min.	Typ.	Max.		
-	Program and Erase Endurance ⁽²⁾	100			cycles	
-	Word Program Time ($V_{CC1}=5.0V$, $T_{opr}=25^{\circ}C$)		25	200	μs	
-	Lock Bit Program Time		25	200	μs	
-	Block Erase Time ($V_{CC1}=5.0V$, $T_{opr}=25^{\circ}C$)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time ⁽¹⁾			$4 \times n$	s	
tps	Wait Time to Stabilize Flash Memory Circuit			15	μs	
-	Data Hold Time ($T_{opr}=-40$ to $85^{\circ}C$)	10			years	

NOTES:

1. n denotes the number of block to be erased.

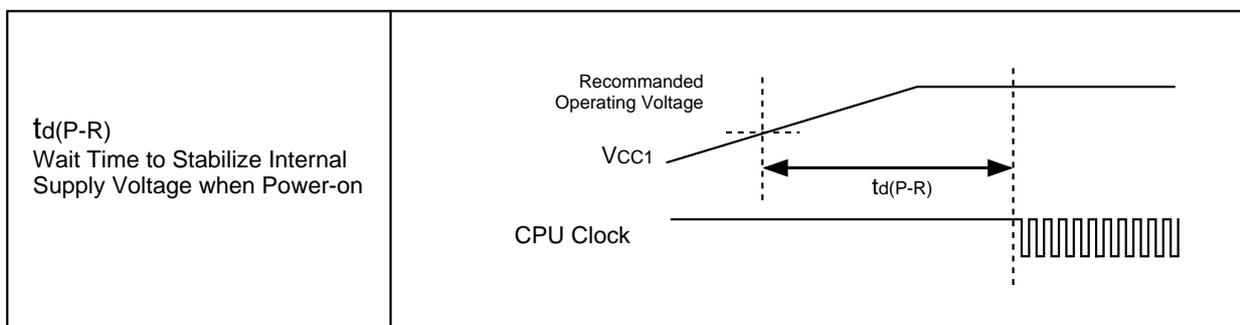
2. Number of program-erase cycles per block.

If Program and Erase Endurance is n cycle ($n \neq 100$), each block can be erased and programmed n cycles.

For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited).

Table 26.48 Power Supply Timing

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	$V_{CC1}=3.0$ to $5.5V$			2	ms

**Figure 26.11 Power Supply Timing Diagram**

$V_{CC1}=V_{CC2}=5V$

Timing Requirements**($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version) unless otherwise specified)****Table 26.49 External Clock Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
tw(H)	External Clock Input High ("H") Width	13.75		ns
tw(L)	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements**($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version) unless otherwise specified)****Table 26.50 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 26.51 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 26.52 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 26.53 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 26.54 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements**($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version) unless otherwise specified)****Table 26.55 Timer B Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 26.56 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 26.57 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 26.58 A/D Trigger Input

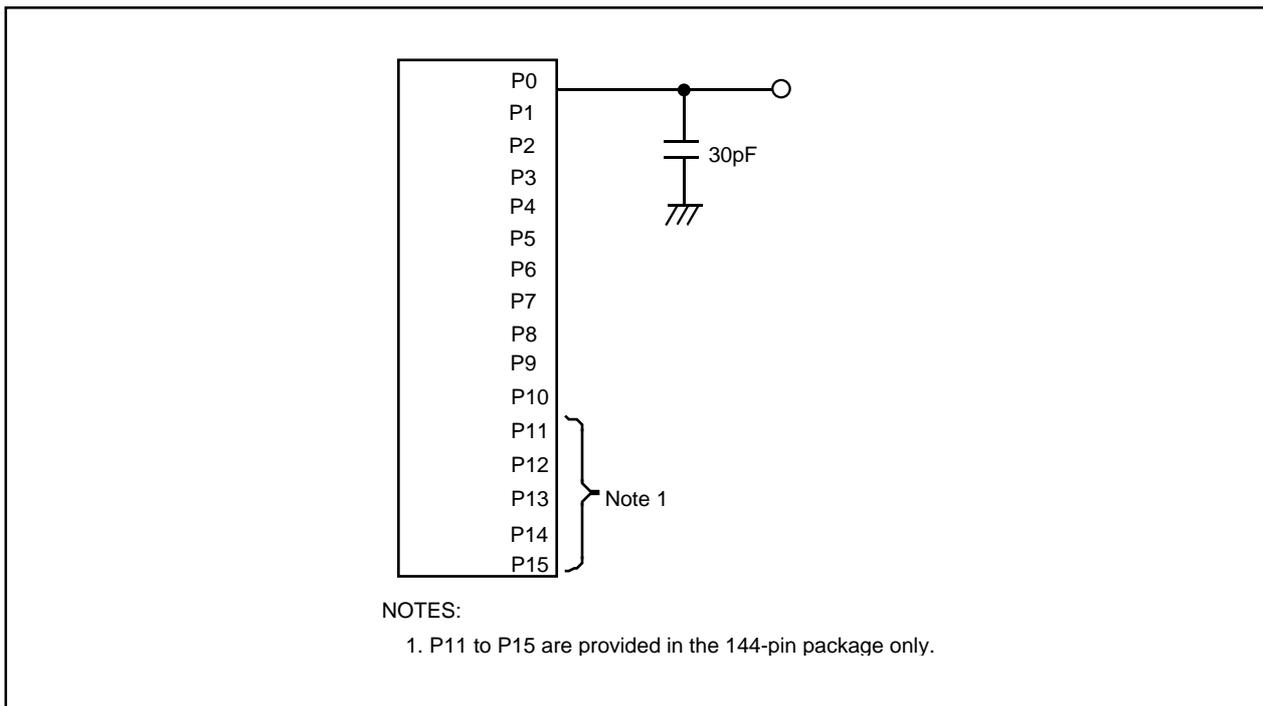
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	ADTRG Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	ADTRG Input Low ("L") Pulse Width	125		ns

Table 26.59 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 26.60 External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	INTi Input High ("H") Width	250		ns
$t_{w(INL)}$	INTi Input Low ("L") Width	250		ns

**Figure 26.12 P0 to P15 Measurement Circuit**

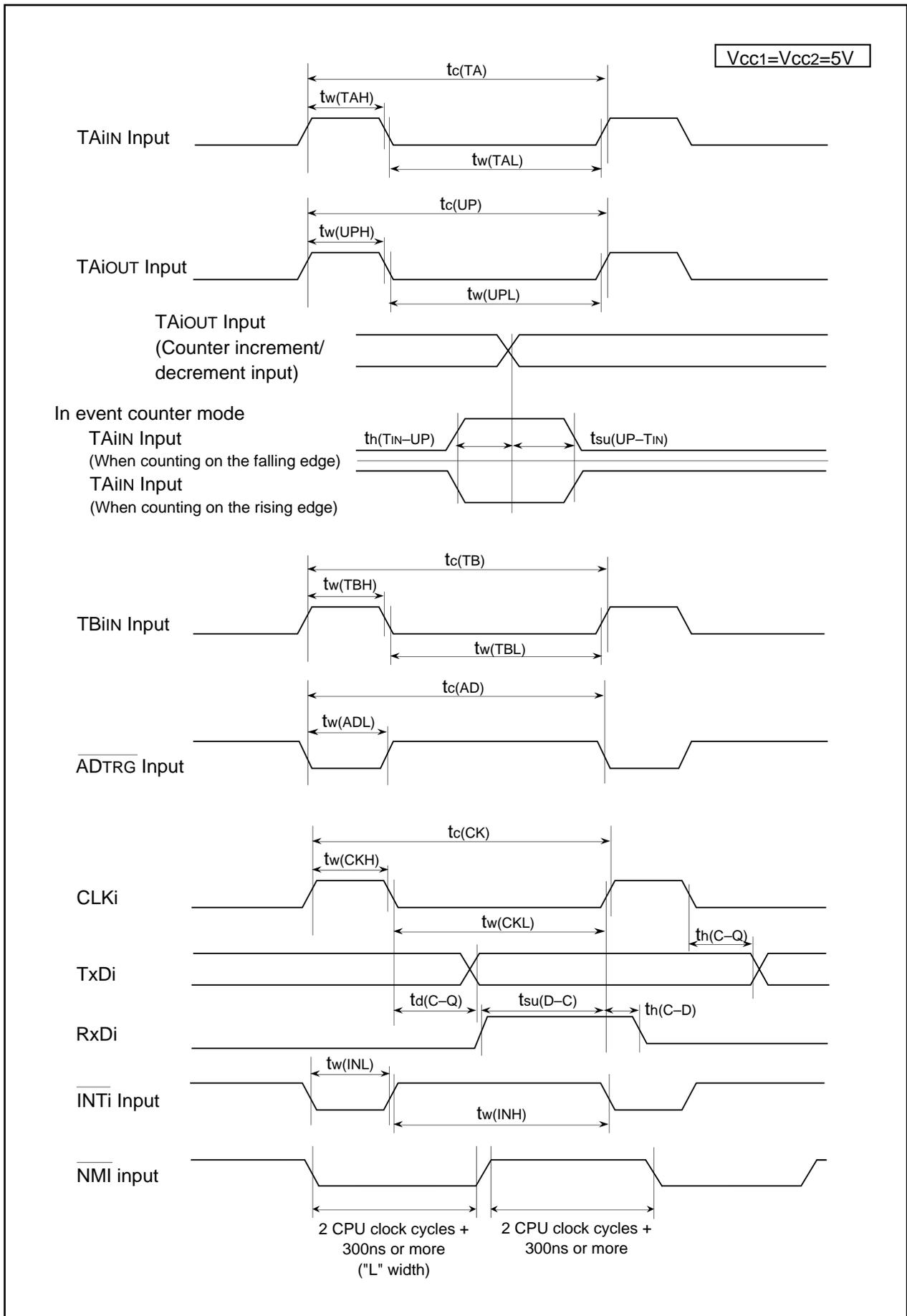


Figure 26.13 V_{CC1}=V_{CC2}=5V Timing Diagram

27. Precautions

27.1 Restrictions to Use M32C/84T (High-Reliability Version)

The M32C/84T microcomputer (high-reliability version) has the following usage restrictions:

- The supply voltage of M32C/84T must be $V_{CC1}=V_{CC2}$.
- M32C/84T must be used in single-chip mode only.
M32C/84T cannot be used in memory expansion mode and microprocessor mode.
- Bus control pins (A0 to A22, A23, D0 to D15, $\overline{CS0}$ to $\overline{CS3}$, $\overline{WRL/WR}$, $\overline{WRH/BHE}$, \overline{RD} , BCLK/ALE, $\overline{HLDA/ALE}$, \overline{HOLD} , ALE, \overline{RDY}) and BCLK pins in M32C/84T cannot be used.
- The voltage detection circuit in M32C/84T cannot be used. Low voltage detection interrupt and brown-out detection reset cannot also be used.
- The DS register, VCR1 register, VCR2 register, D4INT register and EWCR0 to EWCR3 registers in M32C/84T cannot be used.

27.2 Reset

Voltage applied to the VCC1 pin must meet the SVCC standard.

Table 27.1 Power Supply Increasing Slope

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
SVcc	Power Supply Increasing Slope (Vcc1)	0.05			V/ms

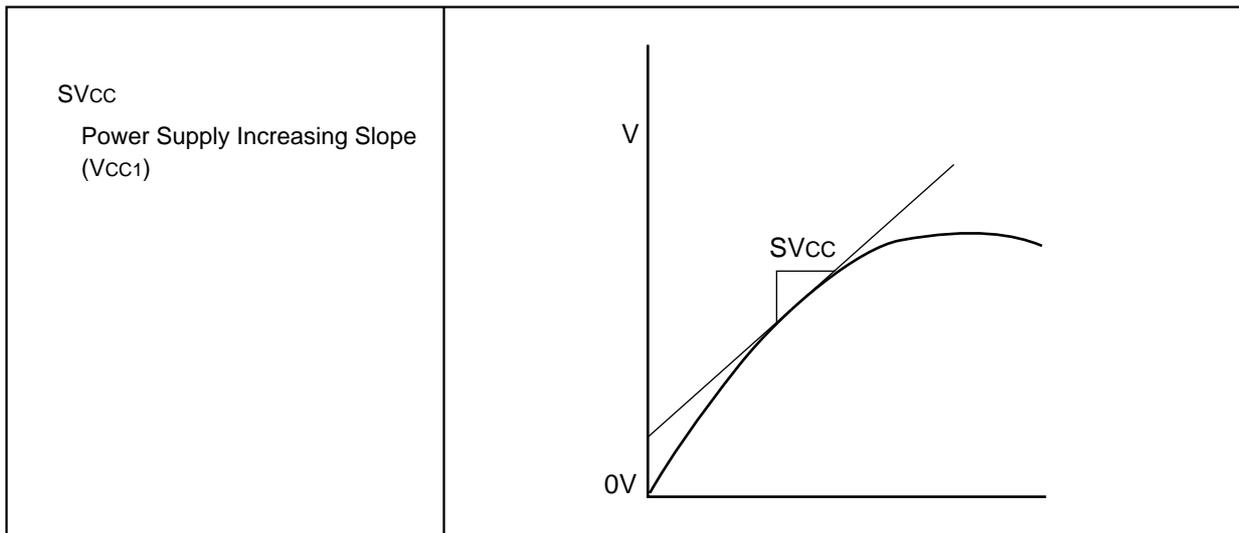


Figure 27.1 SVcc Timing

27.3 Bus

27.3.1 $\overline{\text{HOLD}}$ Signal

When entering microprocessor mode or memory expansion mode from single-chip mode and using $\overline{\text{HOLD}}$ input, set the PM01 and PM00 bits to "112" (microprocessor mode) or to "012" (memory expansion mode) after setting the PD4_7 to PD4_0 bits in the PD4 register and the PD5_2 to PD5_0 bits in the PD5 register to "0" (input mode).

P40 to P47 (A16 to A22, $\overline{\text{A23}}$, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, MA8 to MA12) and P50 to P52 ($\overline{\text{RD/WR/BHE}}$, $\overline{\text{RD/WRL/WRH}}$) are not placed in high-impedance states even when a low-level ("L") signal is applied to the $\overline{\text{HOLD}}$ pin, if the PM01 and PM00 bits are set to "112" (microprocessor mode) or to "012" (memory expansion mode) after setting the PD4_7 to PD4_0 bits in the PD4 register and the PD5_2 to PD5_0 bits in the PD5 register to "1" (output mode) in single-chip mode.

27.3.2 External Bus

The internal ROM cannot be read when a high-level ("H") signal is applied to the CNVss pin and the hardware reset (hardware reset 1 or brown-out detection reset) occurs.

27.4 SFR

27.4.1 100-Pin Package

Set address spaces 03CB₁₆, 03CE₁₆, 03CF₁₆, 03D2₁₆, 03D3₁₆ to "FF₁₆" after reset when using the 100-pin package. 03DC₁₆ must be set to "00₁₆" after reset.

27.4.2 Register Settings

Table 27.2 lists registers containing bits which can only be written to. Set these registers with immediate values. When establishing the next value by altering the present value, write the present value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.

Table 27.2 Registers with Write-only Bits

Register	Address	Register	Address
WDTS Register	000E ₁₆	U3BRG Register	0329 ₁₆
G0RI Register	00EC ₁₆	U3TB Register	032B ₁₆ , 032A ₁₆
G1RI Register	012C ₁₆	U2BRG Register	0339 ₁₆
U1BRG Register	02E9 ₁₆	U2TB Register	033B ₁₆ , 033A ₁₆
U1TB Register	02EB ₁₆ , 02EA ₁₆	UDF Register	0344 ₁₆
U4BRG Register	02F9 ₁₆	TA0 Register ⁽¹⁾	0347 ₁₆ , 0346 ₁₆
U4TB Register	02FB ₁₆ , 02FA ₁₆	TA1 Register ⁽¹⁾	0349 ₁₆ , 0348 ₁₆
TA11 Register	0303 ₁₆ , 0302 ₁₆	TA2 Register ⁽¹⁾	034B ₁₆ , 034A ₁₆
TA21 Register	0305 ₁₆ , 0304 ₁₆	TA3 Register ⁽¹⁾	034D ₁₆ , 034C ₁₆
TA41 Register	0307 ₁₆ , 0306 ₁₆	TA4 Register ⁽¹⁾	034F ₁₆ , 034E ₁₆
DTT Register	030C ₁₆	U0BRG Register	0369 ₁₆
ICTB2 Register	030D ₁₆	U0TB Register	036B ₁₆ , 36A ₁₆

NOTES :

1. In one-shot timer mode and pulse width modulation mode only.

27.5 Clock Generation Circuit

27.5.1 CPU Clock

- When the CPU operating frequency is 24 MHz or more, use the following procedure for better EMC (Electromagnetic Compatibility) performance.
 - 1) Oscillator connected between the XIN and XOUT pins, or external clock applied to the XIN pin, has less than 24 MHz frequency.
 - 2) Use the PLL frequency synthesizer to multiply the main clock.
- In M32C/84T, the main clock frequency must be 24 MHz or less.

27.5.2 Sub Clock

Set the CM03 bit to "0" (XCIN-XCOUT drive capacity "LOW") when selecting the sub clock (XCIN-XCOUT) as the CPU clock, or timer A or timer B count source (fc32).

27.5.2.1 Sub Clock Oscillation

When oscillating the sub clock, set the CM04 bit in the CM0 register to "1" (XCIN-XCOUT oscillation function) after setting the CM07 bit in the CM0 register to "0" (clock other than sub clock) and the CM03 bit to "1" (XCIN-XCOUT drive capacity "HIGH"). Set the CM03 bit to "0" after sub clock oscillation stabilizes.

Set the sub clock as the CPU clock, or timer A or timer B count source (fc32) after the above settings are completed.

27.5.2.2 Using Stop Mode

When the microcomputer enters stop mode, the CM03 bit is automatically set to "1" (XCIN-XCOUT drive capacity "HIGH"). Use the following procedure to select the main clock as the CPU clock when entering stop mode.

- 1) Set the CM17 bit in the CM1 register to "0" (main clock).
- 2) Set the CM21 bit in the CM2 register to "0" (clock selected by the CM17 bit).
- 3) Set the CM07 bit in the CM0 register to "0" (clock selected by the CM21 bit divided by the MCD register setting).

After exiting stop mode, wait for the sub clock oscillation to stabilize. Then set the CM03 bit to "0" and the CM07 bit to "1" (sub clock).

27.5.2.3 Oscillation Parameter Matching

If the sub clock oscillation parameters have only been evaluated with the drive capacity "HIGH", the parameters should be reevaluated for drive capacity "LOW".

Contact your oscillator manufacturer for details on matching parameters.

27.5.3 PLL Frequency Synthesizer

Stabilize supply voltage to meet the power supply standard when using the PLL frequency synthesizer.

Table 27.3 Power Supply Ripple

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
f_{ripple}	Power Supply Ripple Tolerable Frequency (V_{CC1})	$V_{CC1}=5V$		10	kHz
		$V_{CC1}=3.3V$		100	Hz
$V_{P-P(\text{ripple})}$	Power Supply Ripple Voltage Fluctuation Range	$V_{CC1}=5V$		0.5	V
		$V_{CC1}=3.3V$		0.2	V
$V_{CC1}(\Delta V/\Delta T)$	Power Supply Ripple Voltage Fluctuation Rate	$V_{CC1}=5V$		1	V/ms
		$V_{CC1}=3.3V$		0.1	V/ms

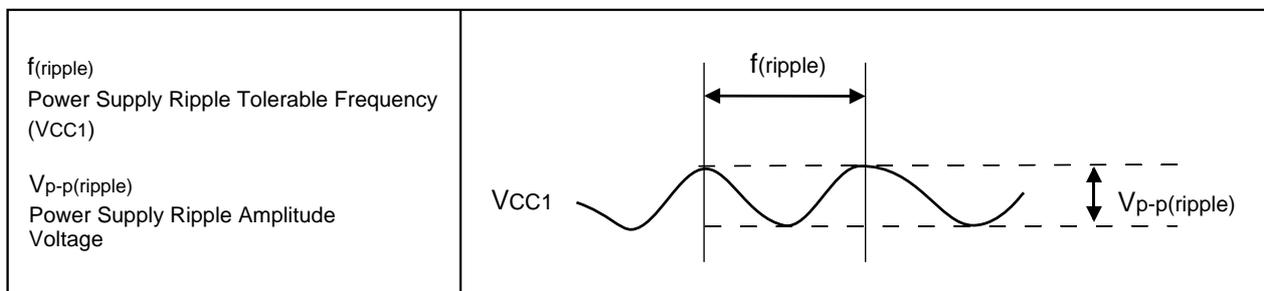


Figure 27.2 Power Supply Fluctuation Timing

27.5.4 External Clock

Do not stop an external clock running if the main clock is selected as the CPU clock while the external clock is applied to the XIN pin.

Do not set the CM05 bit in the CM0 register to "1" (main clock stopped) while the external clock input is used for the CPU clock.

27.5.5 Clock Divide Ratio

Set the PM12 bit in the PM1 register to "0" (no wait state) when changing the MCD4 to MCD0 bit settings in the MCD register.

27.5.6 Power Consumption Control

Stabilize the main clock, sub clock or PLL clock to switch the CPU clock source to each clock.

27.5.6.1 Wait Mode

When entering wait mode while the CM02 bit in the CM0 register is set to "1" (peripheral function stop in wait mode), set the MCD4 to MCD0 bits in the MCD register to maintain 10-MHz CPU clock frequency or less.

When entering wait mode, the instruction queue reads ahead to instructions following the WAIT instruction, and the program stops. Write at least 4 NOP instructions after the WAIT instruction.

27.5.6.2 Stop Mode

- Use the following procedure to select the main clock as the CPU clock when entering stop mode.
 - 1) Set the CM17 bit in the CM1 register to "0" (main clock).
 - 2) Set the CM21 bit in the CM2 register to "0" (clock selected by the CM17 bit).
 - 3) Set the CM07 bit in the CM0 register to "0" (clock selected by the CM21 bit divided by the MCD register setting).

If the PLL clock is selected as the CPU clock source, set the CM17 bit to "0" (main clock) and the PLC07 bit in the PLC0 register to "0" (PLL off) before entering stop mode.

- The microcomputer cannot enter stop mode if a low-level signal ("L") is applied to the $\overline{\text{NMI}}$ pin. Apply a high-level ("H") signal instead.
- If stop mode is exited by any reset, apply an "L" signal to the $\overline{\text{RESET}}$ pin until a main clock oscillation is stabilized enough.
- If using the $\overline{\text{NMI}}$ interrupt to exit stop mode, use the following procedure to set the CM10 bit in the CM1 register (all clocks stopped).
 - 1) Exit stop mode with using the $\overline{\text{NMI}}$ interrupt.
 - 2) Generate a dummy interrupt.
 - 3) Set the CM10 bit to "1".

```
e.g.,      int   #63                ; dummy interrupt
           bset  cm1                ; all clocks stopped
```

```
/* dummy interrupt handling */
```

```
dummy
  reit
```

- When entering stop mode, the instruction queue reads ahead to instructions following the instruction setting the CM10 bit in the CM1 register to "1" (all clocks stopped), and the program stops. When the microcomputer exits stop mode, the instruction lined in the instruction queue is executed before the interrupt routine for recovery is done.

Write the JMP.B instruction, as follows, after the instruction setting the CM10 bit in the CM1 register to "1" (all clocks stopped).

```
e.g.,      bset 0, prcr              ; protection removed
           bset 0, cm1              ; all clocks stopped
           jmp.b LABEL_001         ; JMP.B instruction executed (no instuction between JMP.B
                                   ; and LABEL.)
```

```
LABEL_001:
  nop                ; NOP (1)
  nop                ; NOP (2)
  nop                ; NOP (3)
  nop                ; NOP (4)
  mov.b #0, prcr    ; Protection set
  .
  .
  .
```

27.5.6.3 Suggestions for Reducing Power Consumption

The followings are suggestions for reducing power consumption when programming or designing systems.

Ports: I/O ports maintains the same state despite the microcomputer entering wait mode or stop mode. Current flows through active output ports. Feedthrough current flows through input ports in a high-impedance state. Set unassigned ports as input ports and stabilize electrical potential before entering wait mode or stop mode.

A/D Converter: If the A/D conversion is not performed, set the VCUT bit in the AD0CON1 register to "0" (no VREF connection). Set the VCUT bit to "1" (VREF connection) and wait at least 1 μ s before starting the A/D conversion.

D/A Converter: Set the DAi bit (i=0, 1) in the DACON register to "0" (output disabled) and set the DAi register to "00₁₆" when the D/A conversion is not performed.

Peripheral Function Stop: Set the CM02 bit in the CM0 register while in wait mode to stop unnecessary peripheral functions. However, this does not reduce power consumption because the peripheral function clock (fc32) generating from the sub clock does not stop. When in low-speed mode and low-power consumption mode, do not enter wait mode when the CM02 bit is set to "1" (peripheral clock stops in wait mode).

27.6 Protection

The PRC2 bit setting in the PRCR register is changed to "0" (write disable) when an instruction is written to any address after the PRC2 bit is set to "1" (write enable). Write instruction immediately after setting the PRC2 bit to "1" to change registers protected by the PRC2 bit. Do not generate an interrupt or a DMA transfer between the instruction to set the PRC2 bit to "1" and the following instruction.

27.7 Interrupts

27.7.1 ISP Setting

After reset, the ISP is set to "00000016". The program runs out of control if an interrupt is acknowledged before the ISP is set. Therefore, the ISP must be set before an interrupt request is generated. Set the ISP to an even address, which allows interrupt sequences to be executed at a higher speed.

To use $\overline{\text{NMI}}$ interrupt, set the ISP at the beginning of the program. The $\overline{\text{NMI}}$ interrupt can be acknowledged after the first instruction has been executed after reset.

27.7.2 $\overline{\text{NMI}}$ Interrupt

- $\overline{\text{NMI}}$ interrupt cannot be denied. Connect the $\overline{\text{NMI}}$ pin to Vcc via a resistor (pull-up) when not in use.
- The P8_5 bit in the P8 register indicates the $\overline{\text{NMI}}$ pin value. Read the P8_5 bit only to determine the pin level after a $\overline{\text{NMI}}$ interrupt occurs.
- "H" and "L" signals applied to the $\overline{\text{NMI}}$ pin must be over 2 CPU clock cycles + 300 ns wide.
- $\overline{\text{NMI}}$ interrupt request may not be acknowledged if this and other interrupt requests are generated simultaneously.

27.7.3 $\overline{\text{INT}}$ Interrupt

- Edge Sensitive
"H" and "L" signals applied to the $\overline{\text{INT}}0$ to $\overline{\text{INT}}5$ pins must be at least 250 ns wide, regardless of the CPU clock.
- Level Sensitive
"H" and "L" signals applied to the $\overline{\text{INT}}0$ to $\overline{\text{INT}}5$ pins must be at least 1 CPU clock cycle + 200 ns wide. For example, "H" and "L" must be at least 234ns wide if $X_{IN}=30\text{MHz}$ with no division.
- The IR bit may change to "1" (interrupt requested) when switching the polarity of the $\overline{\text{INT}}0$ to $\overline{\text{INT}}5$ pins. Set the IR bit to "0" (no interrupt requested) after selecting the polarity. Figure 27.3 shows an example of the switching procedure for the $\overline{\text{INT}}$ interrupt.

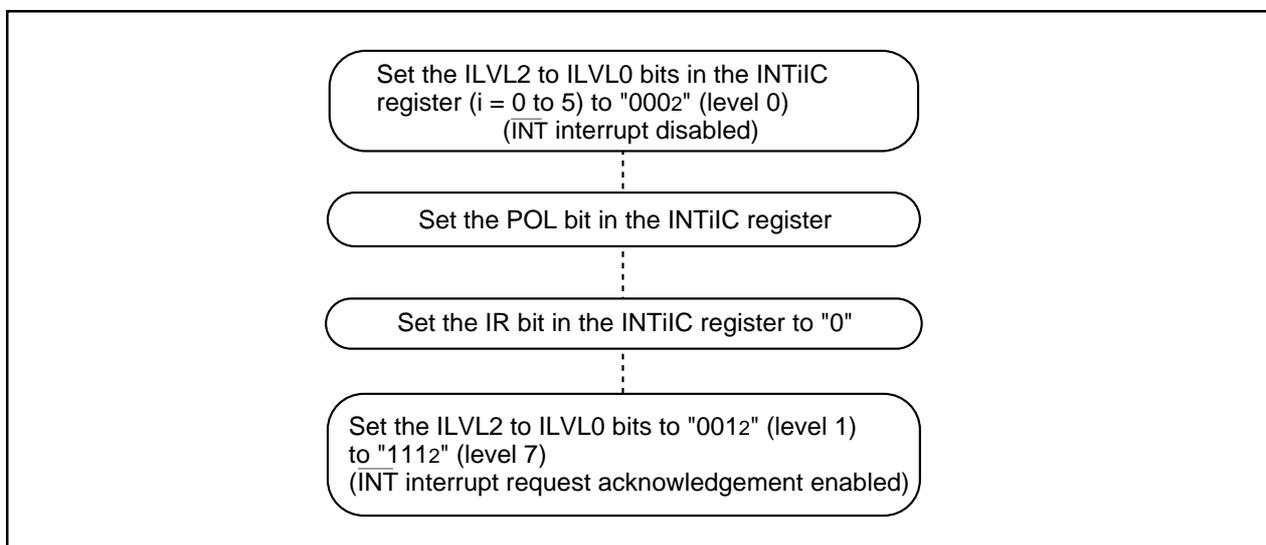


Figure 27.3 Switching Procedure for $\overline{\text{INT}}$ Interrupt

27.7.4 Watchdog Timer Interrupt

Reset the watchdog timer after a watchdog timer interrupt occurs.

27.7.5 Changing Interrupt Control Register

To change the interrupt control register while the interrupt request is denied, follow the instructions below.

Changing IR bit

The IR bit setting may not change to "0" (no interrupt requested) depending on the instructions written. If this is a problem, use the following instruction to change the register: MOV

Changing Bits Except IR Bit

When an interrupt request is generated while executing an instruction, the IR bit may not be set to "1" (interrupt requested) and the interrupt may be ignored. If this is a problem, use the following instructions to change the register: AND, OR, BCLR, BSET

27.7.6 Changing IIOiR Register (i = 0 to 4, 8 to 11)

Use the following instructions to set bits 1 to 7 in the IIOiR register to "0" (no interrupt requested): AND, BCLR

27.7.7 Changing RLVL Register

The DMAII bit is indeterminate after reset. When using the DMAII bit to generate an interrupt, set the interrupt control register after setting the DMAII bit to "0" (interrupt priority level 7 available for interrupts).

27.8 DMAC

- Set DMAC-associated registers while the MDi1 and MDi0 bits (i=0 to 3) in the channel to be used are set to "002" (DMA disabled). Set the MDi1 and MDi0 bits to "012" (single transfer) or "112" (repeat transfer) at the end of setup procedure to start DMA requests.
- Do not set the DRQ bit in the DMiSL register to "0" (no request).
If a DMA request is generated but the receiving channel is not ready to receive⁽¹⁾, the DMA transfer does not occur and the DRQ bit is set to "0".

NOTES:

1. The MDi1 and MDi0 bits are set to "002" or the DCTi register is set to "0000₁₆" (transferred 0 times).
- To start a DMA transfer by a software trigger, set the DSR bit and DRQ bit in the DMiSL register to "1" simultaneously.
e.g.,

```
OR.B #0A0h,DMiSL ; Set the DSR and DRQ bits to "1" simultaneously
```
 - Do not generate a channel i DMA request when setting the MDi1 and MDi0 bits in the DMDj register (j=0,1) corresponding to channel i to "012" (single transfer) or "112" (repeat transfer), if the DCTi register of channel i is set to "1".
 - Select the peripheral function which causes the DMA request after setting the DMA-associated registers. If none of the conditions above (setting $\overline{\text{INT}}$ interrupt as DMA request source) apply, do not write "1" to the DCTi register.
 - Enable DMA⁽²⁾ after setting the DMiSL register (i=0 to 3) and waiting six BCLK cycles or more by program.

NOTES:

2. DMA is enabled when the values set in the MDi1 to MDi0 bits in the DMDj register are changed from "002" (DMA disabled) to "012" (single transfer) or "112" (repeat transfer).

27.9 Timer

27.9.1 Timers A and B

The timers stop after reset. Set the TAI_S(i=0 to 4) bit or TB_jS(j=0 to 5) bit in the TABSR register or TBSR register to "1" (starts counting) after setting operating mode, count source and counter.

The following registers and bits must be set while the TAI_S bit or TB_jS bit is set to "0" (stops counting).

- TAI_{MR}, TB_jMR register
- TAI, TB_j register
- UDF register
- TAZIE, TA0TGL, TA0TGH bits in the ONSF register
- TRGSR register

27.9.2 Timer A

The TA1_{OUT}, TA2_{OUT} and TA4_{OUT} pins are placed in high-impedance states when a low-level ("L") signal is applied to the $\overline{\text{NMI}}$ pin while the INV03 and INV02 bits in the INVC0 register are set to "112" (forced cutoff of the three-phase output by an "L" signal applied to the $\overline{\text{NMI}}$ pin).

27.9.2.1 Timer A (Timer Mode)

- The TAI_S bit (i=0 to 4) in the TABSR register is set to "0" (stops counting) after reset. Set the TAI_S bit to "1" (starts counting) after selecting an operating mode and setting the TAI register.
- The TAI register indicates the counter value during counting at any given time. However, the counter is "FFFF₁₆" when reloading. The setting value can be read after setting the TAI register while the counter stops and before the counter starts counting.

27.9.2.2 Timer A (Event Counter Mode)

- The TAI_S (i=0 to 4) bit in the TABSR register is set to "0" (stops counting) after reset. Set the TAI_S bit to "1" (starts counting) after selecting an operating mode and setting the TAI register.
- The TAI register indicates the counter values during counting at any given time. However, the counter will be "FFFF₁₆" during underflow and "0000₁₆" during overflow, when reloading. The setting value can be read after setting the TAI register while the counter stops and before the counter starts counting.

27.9.2.3 Timer A (One-shot Timer Mode)

- The TAI_S (i=0 to 4) bit in the TABSR register is set to "0" (stops counting) after reset. Set the TAI_S bit to "1" (starts counting) after selecting an operating mode and setting the TAI register.
- The followings occur when the TABSR register is set to "0" (stops counting) while counting:
 - The counter stops counting and the microcomputer reloads contents of the reload register.
 - The TAI_{OUT} pin becomes low ("L").
 - The IR bit in the TAI_{IC} register is set to "1" (interrupt requested) after one CPU clock cycle.
- The output of the one-shot timer is synchronized with an internal count source. When set to an external trigger, there is a delay of one count source cycle maximum, from trigger input to the TAI_{IN} pin to the one-shot timer output.
- The IR bit is set to "1" when the following procedures are performed to set timer mode:
 - selecting one-shot timer mode after reset.
 - switching from timer mode to one-shot timer mode.
 - switching from event counter mode to one-shot timer mode.
 Therefore, set the IR bit to "0" to generate a timer A_i interrupt (IR bit) after performing these procedures.
- When a trigger is generated while counting, the reload register reloads and continues counting after the counter has decremented once following a re-trigger. To generate a trigger while counting, wait at least 1 count source cycle after the previous trigger has been generated and generate a re-trigger.
- If an external trigger input is selected to start counting in timer A one-shot timer mode, do not provide another external trigger input again for 300 ns before the timer A counter value reaches "0000₁₆". One-shot timer may stop counting.

27.9.2.4 Timer A (Pulse Width Modulation Mode)

- The TAI_S(i=0 to 4) bit in the TABSR register is set to "0" (stops counting) after reset. Set the TAI_S bit to "1" (starts counting) after selecting an operating mode and setting the TAI register.
- The IR bit is set to "1" when the following procedures are performed to set timer mode:
 - Selecting PWM mode after reset
 - Switching from timer mode to PWM mode
 - Switching from event counter mode to PWM mode
 Therefore, set the IR bit to "0" by program to generate a timer A_i interrupt (IR bit) after performing these procedures.
- The followings occur when the TAI_S bit is set to "0" (stops counting) while PWM pulse is output:
 - The counter stops counting
 - Output level changes to low ("L") and the IR bit changes to "1" when the TAI_{OUT} pin is held high ("H")
 - The IR bit and the output level remain unchanged when TAI_{OUT} pin is held "L"

27.9.3 Timer B

27.9.3.1 Timer B (Timer Mode, Event Counter Mode)

- The TBiS (i=0 to 5) bit is set to "0" (stops counting) after reset. Set the TBiS bit to "1" (starts counting) after selecting an operating mode and setting TBi register.
The TB2S to TB0S bits are bits 7 to 5 in the TABSR register. The TB5S to TB3S bits are bits 7 to 5 in the TBSR register.
- The TBi register indicates the counter value during counting at any given time. However, the counter is "FFFF16" when reloading. The setting value can be read after setting the TBi register while the counter stops and before the counter starts counting.

27.9.3.2 Timer B (Pulse Period/Pulse Width Measurement Mode)

- The IR bit in the TBiIC (i=0 to 5) register is set to "1" (interrupt requested) when the valid edge of a pulse to be measured is input and when the timer Bi counter overflows. The MR3 bit in the TBiMR register determines the interrupt source within an interrupt routine.
- Use another timer to count how often the timer counter overflows when an interrupt source cannot be determined by the MR3 bit, such as when a pulse to be measured is input at the same time the timer counter overflows.
- To set the MR3 bit in the TBiMR register to "0" (no overflow), set the TBiMR register after the MR3 bit is set to "1" (overflow) and one or more cycles of the count source are counted, while the TBiS bits in the TABSR and TBSR registers are set to "1" (starts counting).
- The IR bit in the TBiIC register is used to detect overflow only. Use the MR3 bit only to determine interrupt source within an interrupt routine.
- Indeterminate values are transferred to the reload register during the first valid edge input after counting is started. Timer Bi interrupt request is not generated at this time.
- The counter value is indeterminate when counting is started. Therefore, the MR3 bit setting may change to "1" (overflow) and causes timer Bi interrupt requests to be generated until a valid edge is input after counting is started.
- The IR bit may be set to "1" (interrupt requested) if the MR1 and MR0 bits in the TBiMR register are set to a different value after a count begins. If the MR1 and MR0 bits are rewritten, but to the same value as before, the IR bit remains unchanged.
- Pulse width measurement measures pulse width continuously. Use program to determine whether measurement results are high ("H") or low ("L").

27.10 Serial I/O

27.10.1 Clock Synchronous Serial I/O Mode

The $\overline{\text{RTS}}_2$ and CLK_2 pins are placed in high-impedance states when a low-level ("L") signal is applied to the $\overline{\text{NMI}}$ pin while the INV03 to INV02 bits in the INVC0 register are set to "112" (forced cutoff of the three-phase output by an "L" signal applied to the $\overline{\text{NMI}}$ pin).

27.10.1.1 Transmission /Reception

When the $\overline{\text{RTS}}$ function is used while an external clock is selected, the output level of the $\overline{\text{RTS}}_i$ pin is held "L" indicating that the microcomputer is ready for reception. The transmitting microcomputer is notified that reception is possible. The output level of the $\overline{\text{RTS}}_i$ pin becomes high ("H") when reception begins. Therefore, connecting the $\overline{\text{RTS}}_i$ pin to the $\overline{\text{CTS}}_i$ pin of the transmitting microcomputer synchronizes transmission and reception. The $\overline{\text{RTS}}$ function is disabled if an internal clock is selected.

27.10.1.2 Transmission

When an external clock is selected while the CKPOL bit in the UiC0 ($i=0$ to 4) register is set to "0" (data is transmitted on the falling edge of the transfer clock and received on the rising edge) and the external clock is held "H", or when the CKPOL bit is set to "1" (data is transmitted on the rising edge of the transfer clock and received on the falling edge) and the external clock is held "L", meet the following conditions:

- Set the TE bit in the UiC1 register to "1" (receive enabled)
- Set the TI bit in the UiC1 register to "0" (data in the UiTB register)
- Apply "L" signal to the $\overline{\text{CTS}}_i$ pin if the $\overline{\text{CTS}}$ function is selected

27.10.1.3 Reception

Activating the transmitter in clock synchronous serial I/O mode generates the shift clock. Therefore, set for transmission even if the microcomputer is used for reception only. Dummy data is output from the TxDi pin while receiving.

If an internal clock is selected, the shift clock is generated when the TE bit in the UiC1 registers is set to "1" (receive enabled) and dummy data is set in the UiTB register. If an external clock is selected, the shift clock is generated when the external clock is input into CLK_i pin while the TE bit is set to "1" (receive enabled) and dummy data is set in the UiTB register.

When receiving data consecutively while the RE bit in the UiC1 register is set to "1" (data in the UiRB register) and the next data is received by the UART_i reception register, an overrun error occurs and the OER bit in the UiRB register is set to "1" (overrun error). In this case, the UiRB register is indeterminate. When overrun error occurs, program both reception and transmission registers to retransmit earlier data. The IR bit in the SiRIC does not change when an overrun error occurs.

When receiving data consecutively, feed dummy data to the low-order byte in the UiTB register every time a reception is made.

When an external clock is selected while the CKPOL bit in the UiC0 register is set to "0" (data is transmitted on the falling edge of the transfer clock and received on the rising edge) and the external clock is held "H" or when the CKPOL bit is set to "1" (data is transmitted on the rising edge of the transfer clock and received on the falling edge) and the external clock is held "L", meet the following conditions:

- Set the RE bit in the UiC1 register to "1" (receive enabled)
- Set the TE bit in the UiC1 register to "1" (transmit enabled)
- Set the TI bit in the UiC1 register to "0" (data in the UiTB register)

27.10.2 UART Mode

Set the UiERE bit (i=0 to 4) in the UiC1 register after setting the UiMR register.

27.10.3 Special Mode 1 (I²C Mode)

To generate the start condition, stop condition or restart condition, set the STSPSEL bit in the UiSMR4 register to "0" first. Then, change each condition generating bit (the STAREQ bit, STPREQ bit or RSTAREQ bit) setting from "0" to "1" after going through a half cycle of the transfer clock.

27.11 A/D Converter

- Set the AD0CON0 (bit 6 excluded), AD0CON1, AD0CON2, AD0CON3, and AD0CON4 registers while the A/D conversion is stopped (before a register is generated).
- Wait a minimum of 1 μ s before starting the A/D conversion when changing the VCUT bit setting in the AD0CON1 register from "0" (VREF no connection) to "1" (VREF connection). Change the VCUT bit setting from "1" to "0" after the A/D conversion is completed.
- Insert capacitors between the AVCC pin, VREF pin, analog input pin AN_{ij} (i=none, 0, 2, 15; j=0 to 7) and AVSS pin to prevent latch-ups and malfunctions due to noise, and to minimize conversion errors. The same applies to the VCC and VSS pins. Figure 27.4 shows the use of capacitors to reduce noise.

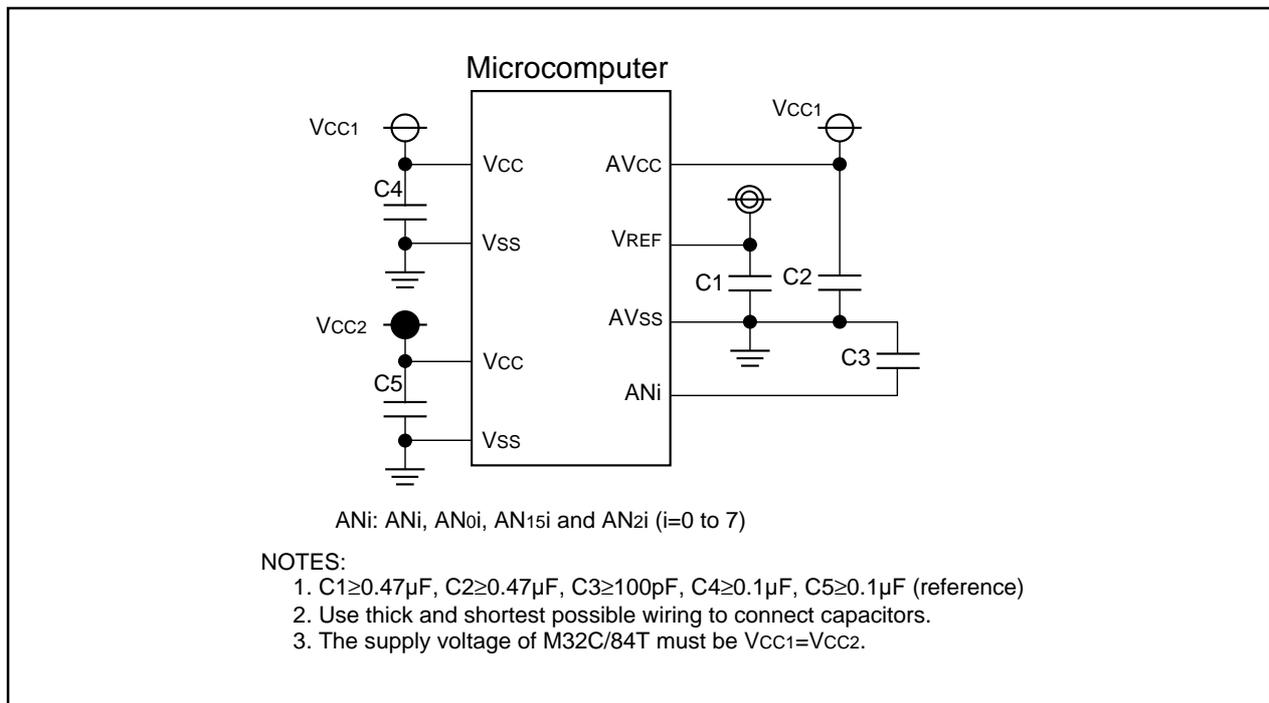


Figure 27.4 Use of Capacitors to Reduce Noise

- Set the bit in the port direction register, which corresponds to the pin being used as the analog input, to "0" (input mode). Set the bit in the port direction register, which corresponds to the $\overline{\text{ADTRG}}$ pin, to "0" (input mode) if the TRG bit in the AD0CON0 register is set to "1" (external trigger).
- When generating a key input interrupt, do not use the AN₄ to AN₇ pins as analog input pins (key input interrupt request is generated when the A/D input voltage becomes "L").
- The frequency of ϕ_{AD} must be 16MHz or less. When the sample and hold function is not activated, ϕ_{AD} frequency must be 250 kHz or more. If the sample and hold function is activated, ϕ_{AD} frequency must be 1MHz or more.
- Set the CH₂ to CH₀ bits in the AD0CON0 register or the SCAN₁ and SCAN₀ bits in the AD0CON1 register to re-select analog input pins when changing A/D conversion mode.

- $AVCC = VREF = VCC1 \geq VCC2$,
A/D input voltage (for AN0 to AN7, AN150 to AN157, ANEX0, and ANEX1) $\leq VCC1$,
A/D input voltage (for AN00 to AN07, and AN20 to AN27) $\leq VCC2$.
- Wrong values are stored in the AD0i register (i=0 to 7) if the CPU reads the AD0i register while the AD0i register stores results from a completed A/D conversion. This occurs when the CPU clock is set to a divided main clock or a sub clock.
In one-shot mode or single sweep mode, read the corresponding AD0i register after verifying that the A/D conversion has been completed. The IR bit in the AD0IC register determines the completion of the A/D conversion.
In repeat mode, repeat sweep mode 0, repeat sweep mode 1, multi-port single sweep mode, and multi-port repeat sweep mode 0, use an undivided main clock as the CPU clock.
- Conversion results of the A/D converter are indeterminate if the ADST bit in the AD0CON0 register is set to "0" (stop A/D conversion) and the conversion is forcibly terminated by program during the A/D conversion. The AD0i register not performing the A/D conversion may also be indeterminate.
If the ADST bit is changed to "0" by program, during the A/D conversion, do not use any values obtained from the AD0i registers.
- External triggers cannot be used in DMAC operating mode. Do not read the AD00 register by program.
- Do not perform the A/D conversion in wait mode.
- Set the MCD4 to MCD0 bits in the MCD register to "100102" (no division) if using the sample and hold function.
- Do not acknowledge any interrupt requests, even if generated, before setting the ADST bit, if the A/D conversion is terminated by setting the ADST bit in the AD0CON0 register to "0" (A/D conversion stopped) while the microcomputer is A/D converting in single sweep mode.

27.12 Intelligent I/O

27.12.1 Register Setting

Operations, controlled by the values written to the G1BT, G1BCR1, G1TMCR0 to G1TMCR7, G1TPR6, G1TPR7, G1TM0 to G1TM7, G1POCR0 to G1POCR7, G1PO0 to G1PO7, G1FS and G1FE registers, are affected by the count source (fBT1) set in the BCK1 and BCK0 bits in the G1BCR0 register.

Set the BCK1 and BCK0 bits before setting the G1BT, G1BCR1, G1TMCR0 to G1TMCR7, G1TPR6, G1TPR7, G1TM0 to G1TM7, G1POCR0 to G1POCR7, G1PO0 to G1PO7, G1FS and G1FE registers.

Operations, controlled by the values written to the G0RI and G1RI, G0TO and G1TO, G0CR and G1CR, G0RB and G1RB, G0MR and G1MR, G0EMR and G1EMR, G0ETC and G1ETC, G0ERC and G1ERC, G0IRF, G1IRF, G0TB and G1TB, G0CMP0 to G0CMP3, G1CMP0 to G1CMP3, G0MSK0 and G0MSK1, G1MSK0 and G1MSK1, G0TCRC and G1TCRC, G0RCRC and G1RCRC registers are affected by the transfer clock.

Set transfer clock before setting the G0RI and G1RI, G0TO and G1TO, G0CR and G1CR, G0RB and G1RB, G0MR and G1MR, G0EMR and G1EMR, G0ETC and G1ETC, G0ERC and G1ERC, G0IRF and G1IRF, G0TB and G1TB, G0CMP0 to G0CMP3, G1CMP0 to G1CMP3, G0MSK0 and G0MSK1, G1MSK0 and G1MSK1, G0TCRC and G1TCRC, G0RCRC and G1RCRC registers.

27.13 Programmable I/O Ports

- Because ports P72 to P75, P80, and P81 have three-phase PWM output forced cutoff function, they are affected by the three-phase motor control timer function and the $\overline{\text{NMI}}$ pin when these ports are set for output functions (port output, timer output, three-phase PWM output, serial I/O output, intelligent I/O output).

Table 27.4 shows the INVC0 register setting, the $\overline{\text{NMI}}$ pin input level and the state of output ports.

Table 27.4 INVC0 Register and the $\overline{\text{NMI}}$ Pin

Setting Value of INVC0 Register		Input Level to $\overline{\text{NMI}}$ Pin	States of P72 to P75, P80, and P81 Pins (when setting an output pin)
INV02 bit	INV03 bit		
0 (not using three-phase motor control function)	-	-	Output functions selected by the PS1, PSL1, PSC, PS2, and PSL2 registers
1 (using three-phase motor control timer function)	0 (three-phase PWM output disabled)	-	High-impedance state
	1 (three-phase PWM output enabled) ⁽¹⁾	H	Output functions selected by the PS1, PSL1, PSC, PS2, and PSL2 registers
		L (forcibly terminated)	High-impedance state

NOTES :

1. The INV03 bit is set to "0" after a low-level ("L") signal is applied to the $\overline{\text{NMI}}$ pin.

- The availability of pull-up resistors is indeterminate until internal power voltage stabilizes, if the RESET pin is held "L".
- The input threshold voltage varies between programmable I/O ports and peripheral functions. Therefore, if the level of the voltage applied to a pin shared by both programmable I/O ports and peripheral functions is not within the recommended operating condition, V_{IH} and V_{IL} (neither "H" nor "L"), the level may vary depending on the programmable ports and peripheral functions.

27.14 Flash Memory Version

27.14.1 Differences Between Flash Memory Version and Masked ROM Version

Due to differences in internal ROM and layout pattern, flash memory version and masked ROM version have varying electrical characteristics such as attributes, performance margins, noise endurance capacity, and noise radiation. When switching to masked ROM version, administer system evaluation tests equal to those held on the flash memory version.

27.14.2 Boot Mode

I/O pins may not be placed in high-impedance states until internal voltage stabilizes, when power is turned on in boot mode. Follow the procedure below to turn on power in boot mode.

- 1) Apply an "L" signal to the $\overline{\text{RESET}}$ and the CNVss pin
- 2) Wait a minimum of 2ms after VCC1 reaches 2.7V or above (until internal voltage stabilizes)
- 3) Apply an "H" signal to the CNVss pin
- 4) Apply an "H" signal to the $\overline{\text{RESET}}$ pin (reset exited)

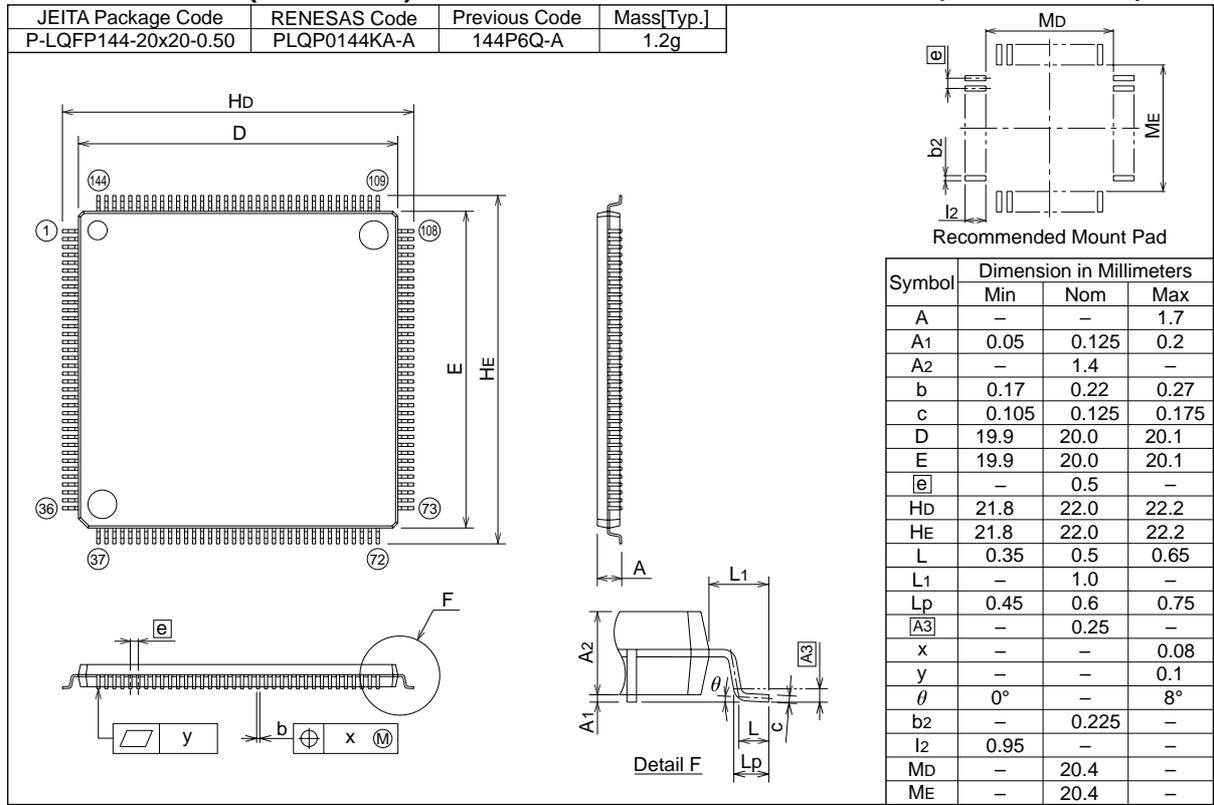
27.15 Noise

Connect a bypass capacitor (0.1 μ F or more) between VCC and VSS by shortest path, using thick wires.

Package Dimensions

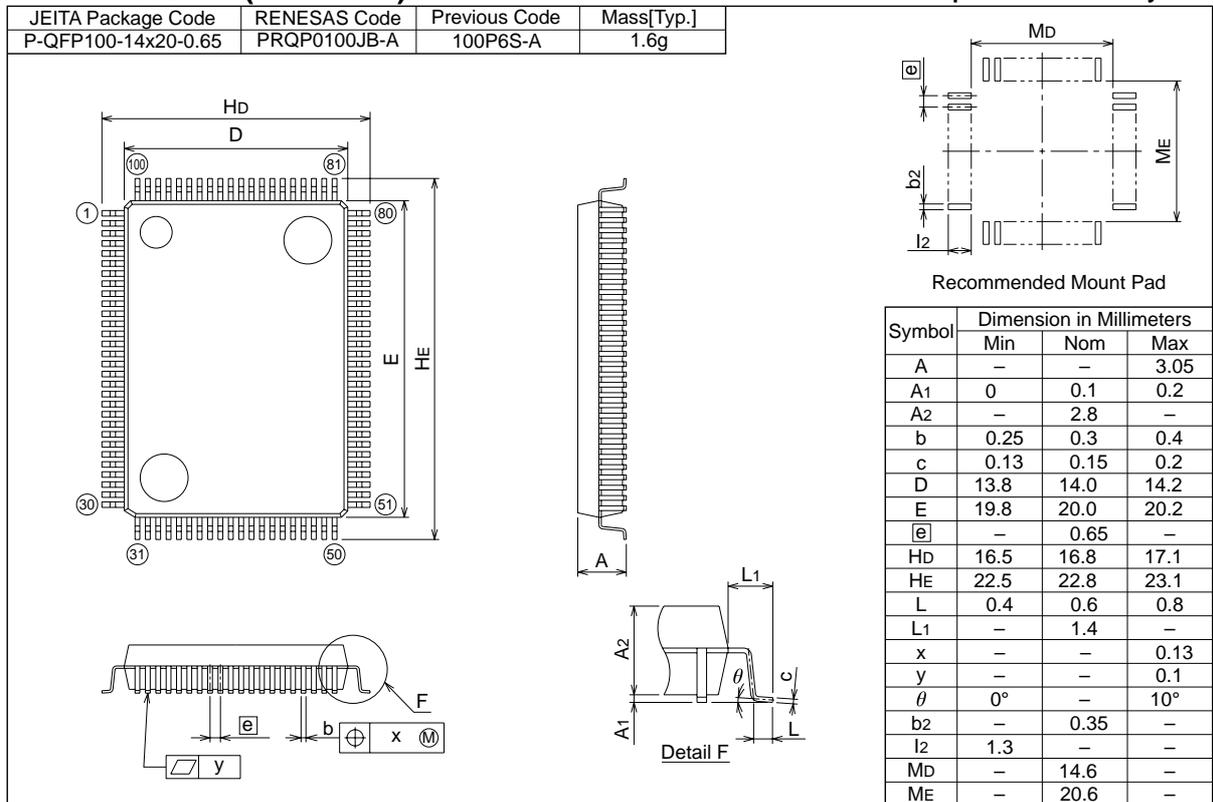
PLQP0144KA-A (144P6Q-A)

Plastic 144pin 20X20mm body LQFP



PRQP0100JB-A (100P6S-A)

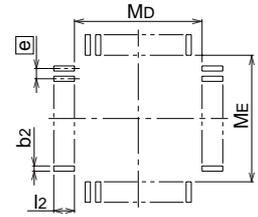
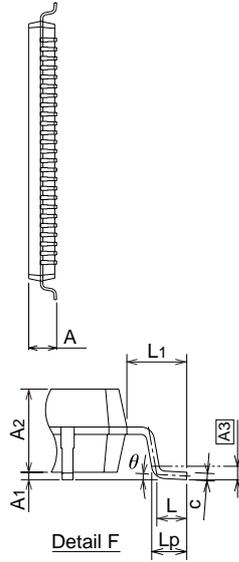
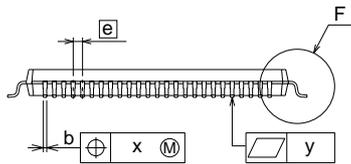
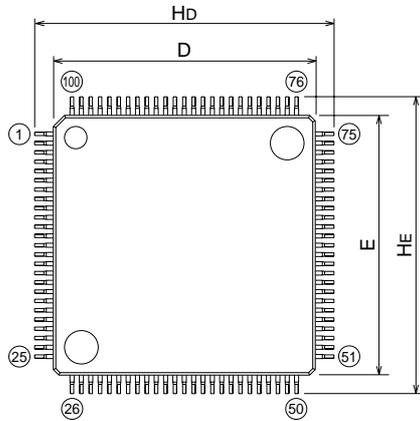
Plastic 100pin 14X20mm body QFP



PLQP0100KB-A (100P6Q-A)

Plastic 100pin 14X14mm body LQFP

JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A	0.6g



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	-	0.5	-
Hd	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
θ	0°	-	10°
b2	-	0.225	-
l2	0.9	-	-
MD	-	14.4	-
ME	-	14.4	-

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REVISION HISTORY

M32C/84 Group(M32C/84, M32C/84T) Hardware Manual

Rev.	Date	Description	
		Page	Summary
0.41	Mar., 03		New Document
0.50	Jun., 04	All pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
		128	Interrupts • Figure 10.15 IIO0IE to IIO5IE, IIO8IE to IIO11IE Registers Note 2 added
		129	Watchdog Timer • Figure 11.1 Watchdog Timer Block Diagram modified
		186	Three-Phase Motor Control Timer Functions • Figure 15.5 ICTB Register, TA1, TA2, TA4, TA11, TA21 and TA41 Registers and TB2SC Register Note 7 for TA1, TA2, TA4, TA11, TA21 and TA41 registers deleted
		387	Flash Memory Version • Figure 24.4 FMR0 Register Notes 1 and 7 revised
		388	• Figure 24.5 FMR1 Register Notes 1 revised
		390	• Figure 24.6 How to Enter and Exit EW0 Mode Note 2 revised; note 5 added
		391	• Figure 24.7 How to Enter and Exit EW1 Mode Note 3 revised; note 4 added
		392	• Figure 24.8 Handling Before and After Low Power Consumption Mode Notes 4 and 5 added
		393	• 24.3.4.5 How to Access Description modified
		413	Electrical Characteristics • Table 25.2 Recommended Operating Conditions $f_{(ripple)}$, $V_{p-p(ripple)}$, V_{CC} , SV_{CC} and note 1 deleted
		415	• Table 25.3 Electrical Characteristics R_{PULLUP} value for the masked ROM version added
		416	• Table 25.4 A/D Conversion Characteristics t_{SMP} value modified; note 1 added
418	• Table 25.7 Low Voltage Detect Circuit Electrical Characteristics added • Table 25.8 Power Supply Timing added • Figure 25.1 Power Supply Timing Diagram added		
425	• Figure 25.3 $V_{CC1}=V_{CC2}=5V$ Timing Diagram (1) $t_{ac1(AD-DB)}$ arithmetic expression modified		
429	• Table 25.24 Electrical Characteristics R_{PULLUP} value for the masked ROM version added		
430	• Table 25.25 A/D Conversion Characteristics t_{CONV} value modified		
436	• Figure 25.7 $V_{CC1}=V_{CC2}=5V$ Timing Diagram (1) $t_{ac1(AD-DB)}$ arithmetic expression modified		
-	-	Precautions • Section of Three-Phase Control Timer Functions deleted	
1.00	Apr., 05	-	M32C/84T (High-reliability version) added Description for the reserved bits on register diagrams modified
		1	Overview • 1.1 Applications Automobiles added

REVISION HISTORY

M32C/84 Group(M32C/84, M32C/84T) Hardware Manual

Rev.	Date	Description	
		Page	Summary
		2, 3	<ul style="list-style-type: none"> • Tables 1.1 and 1.2 M32C/84 Group (M32C/84, M32C/84T) Performance M32C/84T added; supply voltage on Power Consumption row modified; note 3 and 4 added
		4	<ul style="list-style-type: none"> • 1.3 Block Diagram Description deleted • Figure 1.1 M32C/84 Group (M32C/84, M32C/84T) Block Diagram; Note 3 added
		5	<ul style="list-style-type: none"> • 1.4 Product Information Description modified; ROM/RAM Capacity deleted • Table 1.3 M32C/84 Group (M32C/84, M32C/84T) Information updated; M32C/84T added
		6	<ul style="list-style-type: none"> • Figure 1.2 Product Numbering System Classification modified
		7, 12	<ul style="list-style-type: none"> • Figures 1.3 and 1.5 Pin Assignment for 144-Pin Package/ for 100-Pin Package Note 3/Note 5 added
		8-10,13,14	<ul style="list-style-type: none"> • Tables 1.4 and 1.5 Pin Characteristics for 144-Pin Package/ for 100-Pin Package Notes 2 and 3 added
		15	<ul style="list-style-type: none"> • Tables 1.6 Pin Characteristics for 100-Pin and 144-Pin Package Notes 2 and 3 added
		22	<p>Memory</p> <ul style="list-style-type: none"> • Figure 3.1 Memory Map Type number table modified; note 2 modified; notes 4 and 5 added
		23	<p>SFR</p> <ul style="list-style-type: none"> • The DS, VCR2, VCR1 and D4INT registers Note 2 added
		24	<ul style="list-style-type: none"> • The EWCR0 to EWCR3 registers Note 1 added
			<ul style="list-style-type: none"> • The RMR0 register Value after reset added
		26	<ul style="list-style-type: none"> • The RLVL register Value after reset modified
		29	<ul style="list-style-type: none"> • The G1RB register Value after reset modified
		35	<ul style="list-style-type: none"> • The IDB1 and IDB0 registers Value after reset modified
		37	<ul style="list-style-type: none"> • The DM3SL to DM0SL registers Value after reset modified
		38	<ul style="list-style-type: none"> • The A/D0 register Symbol name modified
		41	<ul style="list-style-type: none"> • The PSC register Value after reset modified
		-	<p>Reset</p> <ul style="list-style-type: none"> • Hardware Reset 2 changed to Voltage Down Detection Reset • Chapter structure modified
		43	<ul style="list-style-type: none"> • 5. Reset Hardware Reset 1 and Voltage Down Detection Reset added to description • 5.1 Hardware Reset Section deleted • Figure 5.1 Reset Circuit Note 1 modified
		44	<ul style="list-style-type: none"> • Figure 5.2 Reset Sequence Figure modified; Notes 1, 2, and 3 added
		45	<ul style="list-style-type: none"> • Table 5.1 Pin State while RESET Pin is Held "L" Note 3 added to P56 • 5.2 Voltage Down Detection Reset td(P-R) changed to td(S-R); Note 1 added

Rev.	Date	Description	
		Page	Summary
		-	Voltage Detection Circuit New Chapter
		48	• 6. Voltage Detection Circuit Note added; Description modified
		49	• Figure 6.1 Reset Circuit Block Diagram modified
		49	• Figure 6.2 WDC Register and VCR1 Register Note 3 added to the WDC register; note 1 deleted from and note 2 added to the VCR1 register
		50	• Figure 6.3 VCR2 Register Note 2 deleted; notes 5 and 6 added
		51	• Figure 6.4 D4INT Register Note 6 added
		52	• 6.1 Voltage Down Detection Interrupt Description modified
		52	• Table 6.1 Conditions to Generate the Voltage Down Detect interrupt Request D42 bit setting modified
		52	• Table 6.2 Sampling Periods Table modified
		53	• Figure 6.5 Voltage Down Detection interrupt Generating Circuit Component name modified
		54	• 6.2 Cold Start-up / Warm Start-up Determine Function Newly added
			Processor Mode
		55	• Chapter structuer modified
		57	• Figure 7.1 PM0 Register Notes 2 and 8 added
		58	• Figure 7.2 PM1 Register Note 3 added
		59	• Figure 7.3 Memory Map in Each Processor Mode Figure partially modified; Note 3 added
			Bus
		60	• 8. Bus Note added
		66	• Figure 8.1 DS Register Note 1 modified
		67	• Figure 8.3 EWCR0 to EWCR3 Registers Note 3 added
		67	• Table 8.5 Software Wait State and Bus Cycle Value of the EWCRi04 to EWCRi00 bits revised
		77-80	• 8.3 Page Mode Control Function Added
			Clock Generation Circuit
		82	• Figure 9.1 Clock Generation Circuit Block diagram modified; fCAN added
		84	• Figure 9.3 CM1 Register Note mark position changed
		86	• Figure 9.5 CM2 Register Note 2 added to TCSPR, COSRF and TCSPR registers
		87	• Figure 9.6 TCSPR and CPSRF Registers Note 2 added to the TCSPR register
		89	• Figure 9.8 PM2 Register The PM24 and PM25 bits newly available
		92	• Table 9.2 Bit Settings for On-Chip Oscillator Start Condition Newly added
		95	• Table 9.4 CPU Clock Source and Bit Settings Main clock (main clock direct mode), the PM24 bit in the PM2 register and note 1 added
		96	• 9.3.4 fCAN Newly added

REVISION HISTORY

M32C/84 Group(M32C/84, M32C/84T) Hardware Manual

Rev.	Date	Description	
		Page	Summary
		96	• Table 9.6 CLKOUT Pin in Memory Expansion Mode and Microprocessor Mode Note 4 added
		98	• 9.5.2 Wait Mode Chapter structure modified
		99	• Table 9.7 Pin States in Wait Mode Note 1 added
		101	• 9.5.3 Stop Mode Interrupt usable to exit stop mode added; note 1 added
		103	• Table 9.9 Pin Status in Stop Mode Note 1 added
		103	• Figure 9.13 Status Transition in Wait Mode and Stop Mode Figure partially modified; Note 2 deleted; Note numbers changed accordingly
		104	• Figure 9.14 Status Transition Note 5 modified
			Interrupts
		107	• Figure 11.1 Interrupts Note 3 added
		109	• Figure 11.1 Interrupts Note 3 added
		111	• 11.3.1.4 Low Voltage Detection Interrupt Note 1 added
		116	• Figure 11.4 Interrupt Control Register (2) Note mark position changed
		117	• Figure 11.5 RLVL Register Value after reset changed; note 4 deleted
		119	• 11.6.4 Interrupt Response Time Description modified
		120	• Figure 11.5 Interrupts without Interrupt Priority Levels and IPL Note1 added
		121	• 11.6.6 Saving a Register Description modified; note1 added
		122	• Figure 11.8 Interrupt Priority Note 1 added
		123	• Figure 11.9 Interrupt Priority Level Select Circuit Note 1 added
			Watchdog Timer
		131	• Figure 12.1 Watchdog Timer Block Diagram Block diagram modified
		132	• Figure 12.2 WDC Register and WDTS Register Note 3 added to the WDC register
			DMAC
		137	• Figure 13.2 DM0SL to DM3SL Registers Value after reset changed
		138	• Table 13.2 DMiSL Register (i=0 to 3) Function Note 3 modified
			DMACII
		147	• Figure 14.1 RLVL Register Value after reset changed; note 4 deleted
		153	• 14.8 Execution Time Description modified
			• Figure 14.5 Transfer Cycle The number of cycles changed
			Timer
		154	• Figure 15.1 Timer A Configuration Figure modified
		155	• Figure 15.2 Timer B Configuration Figure modified
		160	• Figure 15.7 TRGSR Register and TCSPR Register Added note 2 to the TCSPR register
		175	• Table 15.8 Settings for the TBiIn Pins (i=0 to 5) PS3 bit in the P94 register modified

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			Three-Phase Motor Control Timer Functions
		183	• Table 16.2 Pin Settings PSC register of P75 modified
		185	• Figure 16.2 INVC0 Register Function of INV07 bit modified
		187	• Figure 16.4 IDB0 and IDB1 Registers Value after reset modified
		191	• Figure 16.8 Triangular Wave Modulation Operation Figure
		192	• Figure 16.9 Sawtooth Wave Modulation Operation Figure partially modified
			Serial I/O
		194	• Figure 17.1 UARTi Block Diagram Figure partially modified
		195	• Figure 17.2 U0TB to U4TB Registers and U0RB to U4RB Registers Note 3 for the U0RB to U4RB registers modified
		197	• Figure 17.4 U0C0 to U4C0 Registers Note 3 added
			• Figure 17.5 U0C1 to U4C1 Registers and U0SMR to U4SMR Registers Note 2 for the U0C1 to U4C1 registers added
		199	• Figure 17.6 U0SMR2 to U4SMR2 Registers Reference table in Note 1 changed
		210	• Table 17.7 Registers to be Used and Settings in UART UiLCH bit function modified
		212	• Figure 17.14 Transmit Operation Figure modified
		213	• Figure 17.15 Receive Operation Figure modified
			• 17.2.1 Transfer Speed Added
		221	• Table 17.15 to 17.17 Pin Settings in I²C Mode Input settings added to tables
			• Table 17.17 Pin Settings in I²C Mode PSC register added
		232	• Table 17.24 GCI Mode Specifications Transmit/receive start condition modified
			A/D Converter
		247	• Table 18.1 A/D Converter Specifications Note 2 modified; note 3 added
		248	• Figure 18.1 A/D Converter Block Diagram Figure partially modified
		249	• Figure 18.2 AD0CON0 Register Note 5 modified; notes 8 and 9 added
		250	• Figure 18.3 AD0CON1 Register Notes 10 and 11 added
		254-257	• Tables 18.2 to 18.8 Each mode specification Note 1 added
		263	• 18.2.8 Output Impedance of Sensor Equivalent Circuit under A/D Conversion Added
		264	• Figure 18.8 Analog Input Pin and External Sensor Equivalent Circuit Value for the condenser changed
			Intelligent I/O
		277	• Figure 22.4 G1BCR1 Register RST2 bit function changed; Note 2 modified
		279	• Figure 22.6 G1TM0 to G1TM7 Registers and G1POCR0 to G1POCR7 Registers Notes 6 and 7 added to the G1POCR0 to G1POCR7 registers
		282	• Table 22.2 Base Timer Specifications Base timer reset condition changed
		283	• Figure 22.9 Base Timer Block Diagram Block diagram modified

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		287	• Table 22.4 Time Measurement Function Specifications Description for the gate function modified
		290	• Figure 22.14 Time Measurement Function (2) Figure modified
		291	• Figure 22.15 Prescaler Function and Gate Function Letters modified
		293	• Table 22.9 Single-Phase Waveform Output Mode Specifications Setting value of the G1PO0 register changed
		294	• Figure 22.16 Single-Phase Waveform Output Mode Setting value of registers added; condition added
		295	• Table 22.10 Phase-Delayed Waveform Output Mode Specifications Setting value of the G1PO0 register changed
		296	• Figure 22.17 Phase-Delayed Waveform Output Mode Setting value of registers added; condition added
		297	• Table 22.11 SR Waveform Output Mode Specifications Setting value of the G1PO0 register changed
		299	• Figure 22.18 SR Waveform Output Mode Setting value of registers added; condition added
		301	• Figure 22.20 G0CR to G1CR Registers, G0RB to G1RB Registers B14 in the G0RB to G1RB registers changed to PER bit
		311	• Table 22.14 Clock Settings (Communication Unit 1) G1PO0 register setting value changed
		311	• Table 22.15 Registers to be Used and Settings OPOL bit in the GiCR register modified
		312	• Table 22.16 Pin Settings in Clock Synchronous Serial I/O Mode (Communication Unit 0 and 1)(1) Registers to be used for P76 and P77 deleted
			• Table 22.17 Pin Settings (2) Register column deleted
			• Table 22.19 Pin Settings (3) Registers to be used for P150 and 151 deleted; Register column deleted
		315	• Table 22.20 UART Mode Specifications ISTxD1 and ISRxD1 Polarity Inverse function deleted
		316	• Table 22.21 Clock Settings Input from ISCLK1 deleted; note 4 deleted
			• Table 22.22 Registers to be Used and Settings UFORM bit function modified; CSS3 to CSS2 bit functions modified
		317	• Figure 22.31 Transmit Operation Figure modified
			• Figure 22.32 Receive Operation Figure modified
		318	• 22.4.3 HDLC Data Processing Mode Description modified
			• Table 22.25 HDLC Processing Mode Specifications Transmit Start Condition and Receive Start Condition brought together to Data Processing Start Condition
		320	• Table 22.28 Registers to be Used and Settings G1PO1 register function modified

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			CAN
		334	• 23.1.6.5 SJW1 and SJW0 Bits Explanation added
		365	• 23.2 CAN Clock Section added
			Programmable I/O Ports
		374	• Figure 24.1 Programmable I/O Ports (1) P150 to P157 deleted; P152 to P157 added
		375	• Figure 24.2 Programmable I/O Ports (2) Figure in Programmable I/O Ports with the Function Select Register modified
		376	• Figure 24.3 Programmable I/O Ports (3) P15 deleted; P150 added
		377	• Figure 24.5 PD0 to PD15 Registers Note 1 modified
		378	• Figure 24.6 P0 to P15 Registers Note 1 modified
		380	• Figure 24.8 PS2 Register and PS3 Register Description added to Note 1
		387	• Figure 24.15 PUR0 Register, PUR1 Register and PUR2 Register Note 1 each added to the PUR0 Register and PUR1 Register
		389	• Figure 24.17 PCR Register and IPS Register Note 1 added to the PCR register
		391	• Table 24.2 Unassigned Pin Setting in Memory Expansion Mode and Micro-processor Mode Table modified; note 3 added
			• Figure 24.19 Unassigned Pin Handling Figure modified
		393	• Table 24.3 Port P6 Peripheral Function Output Control Bits 3, 6 and 7 modified
			• Table 24.4 Port P7 Peripheral Function Output Control Bits 0 and 1 modified
		394	• Table 24.6 Port P9 Peripheral Function Output Control Bits 2 and 6 modified
			Flash Memory Version
		396	• Table 25.1 Flash Memory Version Specifications Description modified
		398	• 25.2.1 ROM Code Protect Function Sentence partially deleted
		399	• Figure 25.2 ROMCP Address Bits 4 and 5 deleted; Note 2 to 4 modified
		420	• Table 25.7 Pin Description (Flash Memory Standard Serial I/O Mode) Description of the P76 and P77 pins revised
		421-423	• Figures 25.14 to 25.16 Pin Connections in Standard Serial I/O Mode Figures modified
		424, 425	• Figure 25.17 to 25.19 Circuit Application in Standard Serial I/O Mode Figures modified
			Electrical Characteristics
		428	• Table 26.2 Recommended Operating Conditions $f_{(ripple)}$, $V_{p-p(ripple)}$, V_{CC} , SV_{CC} and note 1 added; standard max. and min. value of $f_{(RING)}$ added
		430-431	• Table 26.3 Electrical Characteristics Standard value in low power consumption mode added; min. value of V_{OH} changed; standard value (Masked ROM version) in low power consumption mode added
		433	• Table 26.6 Flash Memory Version Electrical Characteristics Notes modified

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		435	<ul style="list-style-type: none"> • Table 26.10 Memory Expansion Mode and Microprocessor Mode Values of $t_{su}(DB-BCLK)$, $t_{su}(RDY-BCLK)$, $t_{su}(HOLD-BCLK)$ modified
		438	<ul style="list-style-type: none"> • Table 26.22 Memory Expansion Mode and Microprocessor Mode Formula of $t_{th}(WR-DB)$ on note 1 modified; note 3 added
		439	<ul style="list-style-type: none"> • Table 26.23 Memory Expansion Mode and Microprocessor Mode Formula of $t_{th}(WR-DB)$ on note 1 modified; note 5 added
		441	<ul style="list-style-type: none"> • Figure 26.3 Vcc1=Vcc2=5V (1) Value of $t_{su}(DB-BCLK)$ modified; formula of $t_{th}(WR-DB)$ on note 3 modified
		442	<ul style="list-style-type: none"> • Figure 26.4 Vcc1=Vcc2=5V (2) Value of $t_{su}(DB-BCLK)$ modified
		443	<ul style="list-style-type: none"> • Figure 26.5 Vcc1=Vcc2=5V (3) \overline{NMI} input added
		445	<ul style="list-style-type: none"> • Table 26.24 Electrical Characteristics Min. value of V_{OH} modified
		450	<ul style="list-style-type: none"> • Table 26.40 Memory Expansion Mode and Microprocessor Mode Note 3 added
		451	<ul style="list-style-type: none"> • Table 26.41 Memory Expansion Mode and Microprocessor Mode Note 5 added
		452	<ul style="list-style-type: none"> • Figure 26.7 Vcc1=Vcc2=3.3V (1) Formula of $t_{th}(WR-DB)$ on note 3 modified
		454	<ul style="list-style-type: none"> • Figure 26.9 Vcc1=Vcc2=3.3V (3) \overline{NMI} input added
		456	<ul style="list-style-type: none"> • 26.2 Electrical Characteristics (M32C/84T) Newly added
		-	<p>Precautions</p> <ul style="list-style-type: none"> • Section of Processor Mode deleted
		468	<ul style="list-style-type: none"> • 27.1 Restrictions to Use M32C/84T (High-Reliability Version) Newly added
		469	<ul style="list-style-type: none"> • 27.2 Reset Added
		470	<ul style="list-style-type: none"> • 27.3.3 Page Mode Control Added
		472	<ul style="list-style-type: none"> • 27.5 Clock Generation Circuit Section structure modified; description modified
		473	<ul style="list-style-type: none"> • Table 27.3 Power Supply Ripple added • Figure 27.2 Power Supply Fluctuation Timing added
		477	<ul style="list-style-type: none"> • 27.7 DMAC Description modified
		480	<ul style="list-style-type: none"> • 27.9 Timer Ordering changed; description for Timer A modified
		483	<ul style="list-style-type: none"> • 27.10 Serial I/O Ordering changed
		485	<ul style="list-style-type: none"> • 27.11 A/D Converter Description modified • Figure 27.4 Use of Capacitors to Reduce Noise Note 3 added
1.01	Jul., 05	All pages	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		All pages	"Low Voltage Detection Reset" changed to "Brown-out Detection Reset"
		37	<p>Special Function Register (SFR)</p> <ul style="list-style-type: none"> • The TCSPR register Value after reset modified
		44	<p>Reset</p> <ul style="list-style-type: none"> • Figure 5.2 Reset Sequence Figure modified; BCLK cycle value for Mask ROM version added
		51	<p>Voltage Detection Circuit</p> <ul style="list-style-type: none"> • Figure 6.4 D4INT Register Note 6 added

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		58	Processor Mode • Figure 7.2 PM1 Register PM13 bit function changed
		62	Bus • Table 8.2 Processor Mode and Port Function Note 3 modified
		87 104 105	Clock Generation Circuit • Figure 9.6 TCSPR Register Value after reset modified • Figure 9.14 Status Transition Note 4 replaced to note 5 • 9.6 System Clock Protection Function Description modified
		113 124	Interrupt • Table 11.2 Relocatable Vector Table Fault Error deleted; Note 4 deleted • Figure 11.10 IFSR Register IFSR6 and IFSR7 bit functions changed
		131	Watchdog Timer • Chapter description modified
		162 164 165 170 171 176 177 178 180	Timer • Table 15.3 Timer Mode Specifications Write to Timer specification changed • Table 15.4 Event Counter Mode Specifications Write to Timer specification changed • Table 15.5 Event Counter Mode Specifications Write to Timer specification changed • Table 15.7 Pulse Width Modulation Mode Specifications Write to Timer specification changed • Figure 15.13 TA0MR to TA4MR Registers Value after reset modified • Table 15.9 Timer Mode Specifications Write to Timer specification changed • Table 15.10 Event Counter Mode Specifications Write to Timer specification changed • Figure 15.21 TB0MR to TB5MR Registers TCK1 bit name modified • Figure 15.22 TB0MR to TB5MR Registers Notes 1 and 2 modified
		194 196 197 198 202 213 225 226	Serial I/O • Figure 17.1 UARTi Block Diagram Diagram modified • Figure 17.3 U0MR to U4MR Registers Value after reset modified • Figure 17.4 U0C0 to U4C0 Registers Note 1 modified • Figure 17.5 U0C1 to U4C1 Registers Note 2 modified • Figure 17.9 IFSR Register IFSR6 and IFSR7 bit functions changed • Table 17.13 Register Settings in I²C Mode SWC and ALS bit functions modified • 17.3.6 SDA Input The IICM bit in the description modified to the IICM2 bit • Table 17.19 Special Mode 2 Specifications Transmit/Receive Control specification changed; Transmit Start Condition specification changed; Error Detection specification changed

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		227	• Table 17.20 Register Settings in Special Mode 2 The IFSR6 register and its function deleted
		229	• 17.4.1.2 When Setting the DINC Bit to "0" (Master Mode) Description Modified
		243	• Figure 17.29 SIM Interface Operation Diagram modified
			Intelligent I/O
		274	• Figure 22.1 Intelligent I/O Block Diagram BE1OUT added
		275	• Figure 22.2 Intelligent I/O Communication Block Diagram Diagram modified
		287	• Figure 22.13 Timer Measurement Function (1) The second condition modified
		292	• Table 22.8 Waveform Generating Function Associated Register Settings Note modified
		304	• Figure 22.24 G1ETC Register Bits 2 to 0 function changed
		307	• Figure 22.27 G1IRF Register Note 2 modified
			CAN Module
		324	• Figure 23.3 C0CTRL0 and C1CTRL0 Registers Note 3 added
		334	• 23.1.6.5 SJW1 and SJW0 Bits Description modified
		342	• 23.1.16.1 CMOD Bit Note 1 modified
		353	• Subsection description modified
		366	• Figure 23.40 Operation Timing when CAN Bus Error Occurs Diagram modified
			Flash Memory Version
		403	• 25.3.3.4 FMSTP Bit Description modified
		420	• Table 25.7 Pin Description P66 and P67 functions modified
			Electrical Characteristics
		427	• Table 26.2 Electrical Characteristics Parameter $f(\text{BCLK})$ and its values added
		435	• Table 26.10 Memory Expansion Mode and Microprocessor Mode $t_{\text{AC1}}(\text{RD-DB})$ expression on Note 1 modified; $t_{\text{AC2}}(\text{RD-DB})$ expression on Note 1 added
		441	• Figure 26.3 Vcc1=Vcc2=5V Timing Diagram (1) $t_{\text{W}}(\text{ER})$ expression on Note 3 modified; t_{CYC} expression added
		442	• Figure 26.4 Vcc1=Vcc2=5V Timing Diagram (2) $t_{\text{AC2}}(\text{AD-DB})$ expression on Note 1 modified; $t_{\text{H}}(\text{ALE-AD})$ expressions on Notes 1 and 2 modified; t_{CYC} expression added
		447	• Table 26.28 Memory Expansion Mode and Microprocessor Mode $t_{\text{AC1}}(\text{RD-DB})$ expression on Note 1 modified; $t_{\text{AC2}}(\text{RD-DB})$ expression on Note 1 added
		452	• Figure 26.7 Vcc1=Vcc2=3.3V Timing Diagram (1) $t_{\text{W}}(\text{ER})$ expression on Note 3 modified; t_{CYC} expression added
		453	• Figure 26.8 Vcc1=Vcc2=3.3V Timing Diagram (2) $t_{\text{AC2}}(\text{RD-DB})$ expression on Note 1 modified; $t_{\text{H}}(\text{ALE-AD})$ expressions on Notes 1 and 2 modified; $t_{\text{H}}(\text{WR-CS})$ expression on Note 2 modified; t_{CYC} expression added
		458	• Table 26.43 Electrical Characteristics Parameter $f(\text{BCLK})$ and its values added

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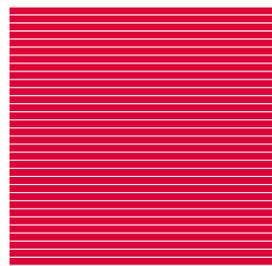
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		462	<ul style="list-style-type: none"> • Table 26.47 Flash Memory Version Electrical Characteristics Measurement condition changed
		482	<p>Precautions</p> <ul style="list-style-type: none"> • 27.9.3.2 Timer B (Pulse Period/Pulse Width Measurement Mode) Description modified

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