Ordering number : ENA0976

SANYO Semiconductors
DATA SHEET

LV25200M — Bi-CMOS IC
Single chip Tuner IC for Car Radio

Overview

LV25200M is a tuner IC for car radio, which incorporates the AM/FM Tuner, PLL, AM/FM Noise Canceller (NC), FM Stereodecoder (MPX) , Multipath-noise Rejection Circuit (MRC) .
This IC enables development of the low-cost analog tuner for OEM.

Functions

- AM+FM-FE+IF+NC+MPX+MRC+PLL

Features

- World-wide compatible tuners
  A single tuner module is enough to supply the world-wide compatible tuners.
  FM is compatible with US EURO, Japan bands while AM is compatible with LW, MW, SW, Weather-Band.
  With the image cancel mixer incorporated in FM MIX, the external RF AMP can be deleted.
  Compatible with RDS. PLL fast locking.
- Self-contained type IF band variable filter incorporated
  Detects any neighboring interfering station and varies the IF filter band, enabling superior selectivity characteristic.
- Auto alignment EEPROM necessary
  FM RF, VCO, Null-voltage, Mute-on, Mute-ATT, SNC, HCC, Station detector, Gain AGC sensitivity,
  CCB bus compatible
- Reduced parts quantity
  Parts quantity reduced from our conventional products
- Other functions
  AM noise canceller (genuine compatible)

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Specifications

Maximum Ratings at Ta = 25°C

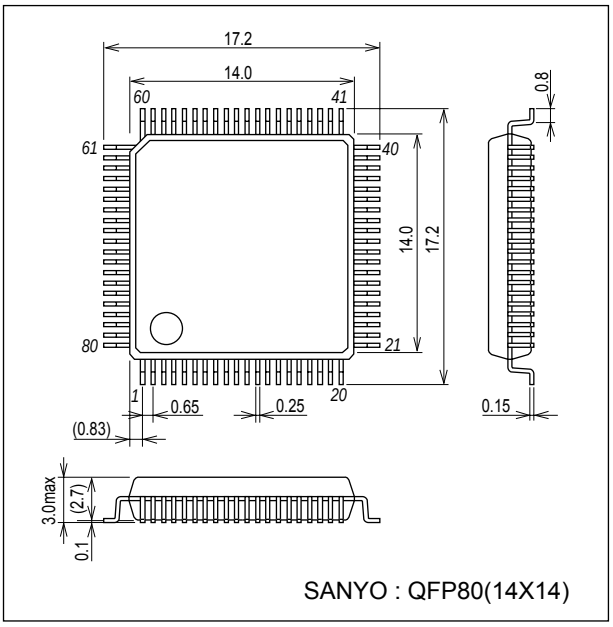
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}_H max	PIN 5, 77	8.7	V
	V_{CC}_L max	PIN 21, 27, 50	5.7	V
Maximum input current	V_{IN} max	PIN 17, 18, 19	-0.3 to +5.0	V
Maximum output current	V_O max	PIN 20	-0.3 to +6.5	V
Allowable power dissipation	Pd max	(Ta≤85°C)	950	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-40 to +150	°C

Recommended Operating Conditions at Ta = 25°C

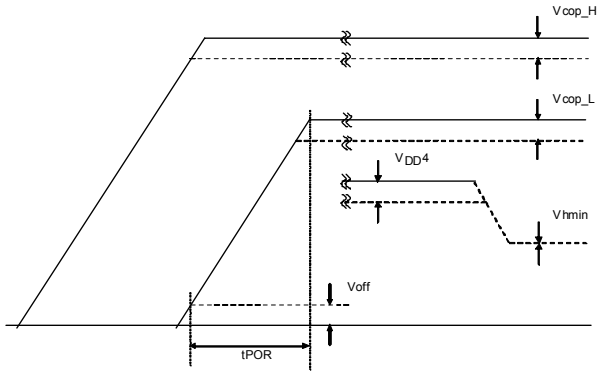
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}_H	PIN 5, 66, 75, 76, 77	8.0	V
	V_{CC}_L	PIN 21, 27, 50	5.0	V
Operating supply voltage range	VCcop_H	PIN 5, 66, 75, 76, 77	7.5 to 8.5	V
	VCcop_L	PIN 21, 27, 50	4.5 to 5.5	V
Input High level voltage	V_{IH}	PIN 17, 18, 19	2.5 to 4.0	V
Input Low level voltage	V_{IL}	PIN 17, 18, 19	0 to 0.8	V
Input amplitude voltage	V_{IN}	PIN 17, 18, 19	0 to 4.0	Vp-p
Input pulse width	tϕW	PIN 19	0.45 or more	µs
Setup time	Tsetup	PIN 17, 18, 19	0.45 or more	µs
Hold time	Thold	PIN 17, 18, 19	0.45 or more	µs

Package Dimensions

unit : mm (typ)
3255



Reset at Power ON



Recommended Operating Conditions at Ta=25°C, GND=0V

Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage	Vcop_H	PIN 5, 66, 75, 76, 77	7.5 to 8.5	V
	Vcop_L	PIN 21, 27, 50	4.5 to 5.5	V
Internal logic voltage	V_{DD}4	PIN 13	3.7 to 4.3	V
Internal register hold voltage	Vhmin	PIN 13, Design reference value	V_{DD}4 to 2.2	V
Internal register reset voltage	Voff	PIN 27, 50, Design reference value	0 to 0.2	V
Internal register reset power ON time	tPOR	PIN 27, 50, Design reference value	30 to 3000	µs

AC Characteristics

Operating Characteristics at Ta=25°C, V_{CC}=8.0V, V_{DD}=5.0V
with the designated measuring circuit outside standard.
Except that this measurement was made with the IC socket [Yamaichi Denki Kogyo Co., Ltd. IC51-0644-807].
Audio filter: IHF BPF used

[FM characteristics] FM FE MIX input (NO-Dummy)

	Parameter	Symbol	Conditions	CCB Command							min	typ	max	Unit
				IN1	IN2	IN3-1	IN3-2	IN3-3	IN3-4	IN3-5				
1-1	Current drain -8V	Icco-8V	No input FM mode I5+I66+I75+I76+I77	19	37	25	25	25	25	25	50	62	74	mA
1-2	Current drain -5V	Icco-5V	No input FM mode I21+I27+I50	19	37	25	25	25	25	25	44.5	51	58	mA
1-3	Demodulation output	Vo-FM	98.1MHz, 60dBμV, 1kHz, 100%mod, pin 25	19	37	25	25	25	25	25	220	277	350	mVrms
1-4	Pin 52 RDS demodulation output	Vo-52	98.1MHz, 60dBμV, 1kHz, 100%mod, pin 52	19	37	25	25	25	25	25	270	340	425	mVrms
1-5	Channel balance	CB	98.1MHz, 60dBμV, 1kHz, pins 25 and 26	19	37	25	25	25	25	25	-1	0	1	dB
1-6	Total harmonic distortion factor	THD-Fmmono (1)	98.1MHz, 60dBμV, 1kHz, 100%mod, pin 25	19	37	25	25	25	25	25		0.2	1	%
1-7	Total harmonic distortion	THD-Fmmono (2)	98.1MHz, 60dBμV, 1kHz, 150%mod, pin 25	19	37	25	25	25	25	25		0.3	2.5	%
1-8	Signal to noise ratio (MONO)	S/N-FM-MONO	98.1MHz, 60dBμV, 1kHz, 100%mod,	19	37	25	25	25	25	25	60	67		dB
1-9	Signal to noise ratio (ST)	S/N-FM-ST	98.1MHz, 60dBμV, 1kHz, 100%mod, pin 25, pilot=10%	19	37	25	25	25	25	25	54	58		dB
1-10	AM suppression ratio	AMR	98.1MHz, 60dBμV, 1kHz, 100%mod, 30% in AM mode, fm=1kHz, pin 25	19	37	25	25	25	25	25	54	61		dB
1-11	Muting attenuation (1)	Att-1	98.1MHz, 60dBμV, 1kHz, with V33=0→2V, pin 25 attenuation	19	37	25	25	14	25	25	-30	-25	-20	dB
1-12	Muting attenuation (2)	Att-2	98.1MHz, 60dBμV, 1kHz, with V33=0→2V, pin 25 attenuation	19	37	25	35	25	25	25	-20	-16	-11.2	dB
1-13	Muting attenuation (3)	Att-3	98.1MHz, 60dBμV, 1kHz, with V33=0→1V, pin 25 attenuation	19	37	25	35	25	25	25	-11	-6	-1	dB
1-14	Separation	Separation	98.1MHz, 60dBμV, mod=30%, pilot=10%, pin 25 output ratio [IN3-5 D0-5] Separation control adj	19	37	25	25	25	25	25	27	38		dB
1-15	Stereo ON level	ST-ON	Pilot demodulation at which V39<0.5V is established	19	37	25	25	25	25	25	1.9	4.1	6.3	%
1-16	Stereo OFF level	ST-OFF	Pilot demodulation at which V39>3.5V is established	19	37	25	25	25	25	25	1	3		%
1-17	Main distortion factor	THD-Main L	98.1MHz, 60dBμV, L+R=90%, pilot=10%, pin 25	19	37	25	25	25	25	25		0.3	1.2	%
1-18	SNC output attenuation	AttSNC	98.1MHz, 60dBμV, L-R=90%, pilot=10%, V28=3V→0.6V, pin 25; standard for single block	19	37	25	25	25	25	25	-10	-6	-2	dB
1-19	HCC output attenuation (1)	FM HCC	98.1MHz, 60dBμV, 10kHz, L+R=90%, pilot=10%, V29=3V→0.6V, pin 25; standard for single block	19	37	25	25	25	25	25	-6	-3	-0.5	dB
1-20	HCC output attenuation (2)	FM HCC	98.1MHz, 60dBμV, 10kHz, L+R=90%, pilot=10%, V29=3V→0.1V, pin 25; standard for single block	19	37	25	25	25	25	25	-14.5	-10.5	-6.5	dB
1-21	Input limiting voltage	Vi-lim	98.1MHz, 60dBμV, 30%mod, MIX input at which the input reference output is down by -3dB, V42=0V, V29=0V, with MUTE=OFF	19	37	25	25	25	25	25	-6	-1	1	dBμV
1-22	Muting sensitivity	Vi-mute	MIX input level at V42=1V, non-mod	19	37	25	25	25	25	25	0.1	5	9.9	dBμV

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	Parameter	Symbol	Conditions	CCB Command							min	typ	max	Unit
				IN1	IN2	IN3-1	IN3-2	IN3-3	IN3-4	IN3-5				
1-23	SD sensitivity	SD-senFM	MIX input level at which SD pin is ON, shifter-adj, non-mod	20	37	25	25	25	25	25	20	25	30	dBμV
	IF count sensitivity	IF-count-sens.FM	IF count sensitivity at MIX input, non-mod	20	37	25	19	25	25	25	16			dBμV
1-24	S-meter DC output	VSMFM-1	No input, pin 38 DC output non-mod	19	37	25	25	25	25	25			0.5	V
		VSMFM-2	10dBμV, pin 38 DC output non-mod	19	37	25	25	25	25	25		0.75		V
		VSMFM-3	30dBμV, pin 38 DC output non-mod [IN3-2 D0-4] S-meter shift-adj	19	37	25	A1	25	25	25	1.8	1.85	1.9	V
		VSMFM-4	50dBμV, pin 38 DC output non-mod	19	37	25	25	25	25	25		3.3		V
		VSMFM-5	80dBμV, pin 38 DC output non-mod	19	37	25	25	25	25	25			4.8	V
1-24	S-meter AC pin DC output	VSMFM-A1	No input, pin 40 DC output non-mod	19	37	25	25	25	25	25			0.45	V
		VSMFM-A2	10dBμV, pin 40 DC output non-mod	19	37	25	25	25	25	25		0.85		V
		VSMFM-A3	30dBμV, pin 40 DC output non-mod	19	37	25	25	25	25	25	1.51	1.78	2.1	V
		VSMFM-A4	50dBμV, pin 40 DC output non-mod	19	37	25	25	25	25	25		3.05		V
		VSMFM-A5	80dBμV, pin 40 DC output non-mod	19	37	25	25	25	25	25			4.8	V
1-25	S-meter inclination standard - 1	S-curve1	Holds [IN3-2 D0-4] data, which was obtained by deducting (VSMFM-2) from VSM (VSMFM-3)	19	37	25	25	25	25	25	0.85	1.1	1.4	V
1-26	S-meter inclination standard - 2	S-curve2	Holds [IN3-2 D0-4] data, which was obtained by deducting (VSMFM-3) from VSM (VSMFM-4)	19	37	25	25	25	25	25	1	1.45	1.9	V
1-27	Mute drive output	VMUTE-60	60dBμV, pin 42 output DC output non-mod	19	37	25	25	25	25	25		0.15	0.3	V
1-28	Noise convergence - 1	FM NOISE-20	60dBμV.98.1MHz, 30%mod, input reference, output level of the input -20dBμV, MUTE=OFF(42pin=GND)	19	37	25	25	25	25	25	-14	-9	-4	dB
1-29	N-AGC ON input	VNAGC	98.1MHz, non-mod, MIX input level at which pin 1 becomes 0.6V or more	19	37	25	25	33	25	25	66	75	84	dBμV
1-30	W-AGC ON input	VWAGC	98.1MHz, non-mod, pin 38 =1.0V applied (Keyed on), MIX input level at which pin 1 becomes 0.6V or more	19	37	25	25	35	25	25	82	90	98	dBμV
1-31	Image obstruction ratio-1		Removal amount of 108.1M +21.4MHz	21	37	25	25	25	25	25	15			dB
1-32	Image obstruction ratio-2		Removal amount of 90M -21.4MHz	28	37	25	25	25	25	25	15			dB
	SD bandwidth - 1	BW-mute1	98.1MHz, non-mod, 50dBμV, Bandwidth at which SD pin is turned ON	20	37	23	25	37	25	25	70	100	130	kHz
	SD bandwidth - 2	BW-mute2	98.1MHz, non-mod, 50dBμV, Bandwidth at which SD pin is turned ON	20	37	23	25	38	25	25	130	200	270	dB
1-33	Conversion gain	A.V.	98.1MHz, 60dBμV, non-mod, FECF output	28	37	25	25	25	25	25	85	130	200	mVrms

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[FM IF Filter characteristics] FM IF input

	Parameter	Symbol	Conditions	CCB Command							min	typ	max	Unit
				IN1	IN2	IN3-1	IN3-2	IN3-3	IN3-4	IN3-5				
2-1	IF variable filter gain-narrow band	FIL-G-N	70dBμV, pin 54 AC (450kHz) output non-mod, After CF adjustment, fit in through BW/G adjustment. Narrow-Fix MODE	19	37	21	25	25	25	25	79	84	89	
2-2	IF variable filter	FIL-BW-N	Pin 54 -AC output monitor. Confirm the 2dB or more level down at the ±25kHz point with reference to the center frequency of 450kHz. -3dB bandwidth. Narrow-Fix MODE	19	37	21	25	25	25	25	2			dB
2-3	IF variable filter	FIL-BW-W	Pin 54-AC output monitor. Confirm no level down exceeding 3 dB at the ±80kHz point with reference to the center frequency of 450kHz. -3dB bandwidth. Wide-Fix MODE	19	37	23	25	25	25	25			3	dB

[NC block] NC input (48pin), S-meter AC input (40pin)

	Parameter	Symbol	Conditions	CCB Command							min	typ	max	Unit
				IN1	IN2	IN3-1	IN3-2	IN3-3	IN3-4	IN3-5				
3-1	FM NC gate time	FM τGATE	NC input, pulse cycle=1kHz, 38pin=2V applied, pulse width=1μs, at 100mVp-o pulse input (after MVCO adjustment)	19	37	25	25	25	25	25	36	40	44	μs
3-2	FM NC noise sensitivity	SN-DETOUT	NC input (pin 48), 38pin=2V applied, measure the pulse input level at which the noise canceller starts operation, pulse cycle=1kHz, pulse width=1μs	19	37	25	25	25	25	25	17	30	43	mVp-o
3-3	FM NC noise sensitivity	SN-Vsm	S-meter (AC) input (pin 40), 38pin=0V applied, measure the pulse input level at which the noise canceller starts operation, pulse cycle=1kHz, pulse width=1μs	19	37	25	25	25	25	25		46		mVp-o
3-4	AM NC gate time	AM τGATE(1)	S-meter (AC) input (pin 40), pulse cycle=1kHz, pulse width=1μs, measurement at pin 33. 38pin=1.5	36	37	26	26	26	26	26	345	450	555	μs
3-5	AM NC noise sensitivity	SN	S-meter (AC) input (pin 40), measure the pulse input level at which the noise canceller starts operation, pulse cycle=1kHz, pulse width=1μs	36	37	26	26	26	26	26		24		mVp-o

[Multipath-noise rejection circuit] MRC input (pin 41)

	Parameter	Symbol	Conditions	CCB Command							min	typ	max	Unit
				IN1	IN2	IN3-1	IN3-2	IN3-3	IN3-4	IN3-5				
4-1	MRC output	VMRC	Pin 39 voltage when 3.5 V is applied to V38	19	37	25	25	25	25	25	2.76	2.96	3.16	V
4-2	MRC operation level	MRC-ON	SG (AG5) out level when pin 38 =5V and pin 39=2.6V, f=70kHz	19	37	25	25	25	25	25	50	71	100	mVrms

[AM characteristics] AM AMANT input

	Parameter	Symbol	Conditions	CCB Command							min	typ	max	Unit
				IN1	IN2	IN3-1	IN3-2	IN3-3	IN3-4	IN3-5				
5-1	Practical sensitivity	S/N-30	1MHz, 30dBμV, fm=1kHz, 30%mod, pin 25	36	37	26	26	26	26	26	20			dB
5-2	Detection output	Vo-AM	1MHz, 74dBμV, fm=1kHz, 30%mod, pin 25	36	37	26	26	26	26	26	84	105	131	mVrms
5-3	AGC-F.O.M	VAGC-FOM	1MHz, 74dBμV, output reference, input width at which the output decreases by 10dB, pin 25	36	37	26	26	26	26	26	50	54.5	59	dB
5-4	Signal-to-noise ratio	S/N-AM	1MHz, 74dBμV, fm=1kHz, 30%mod	36	37	26	26	26	26	26	51	60		dB
5-5	Total harmonic distortion ratio - 1	THD-AM-1	1MHz, 74dBμV, fm=1kHz, 80%mod	36	37	26	26	26	26	26		0.3	1	%
5-6	Total harmonic distortion ratio - 2	THD-AM-2	1MHz, 120dBμV, fm=1kHz, 80%mod	36	37	26	26	26	26	26		0.5	1.5	%
5-7	AM HCC output attenuation	AM HCC	1MHz, 74dBμV, fm=4kHz, 30%mod, V29=3V→0.6V, 25pin	36	37	26	26	26	26	26	5	9	13	dB
5-8	S-meter DC output	VSMAMDC-1	No input, 38pin DC output	36	37	26	26	26	26	26	0	0.1	0.5	V
		VSMAMDC-2	1MHz, 30dBμV, non-mod, 38pin DC output	36	37	26	26	26	26	26	1.2	1.5	1.9	V
		VSMAMDC-3	1MHz, 130dBμV, non-mod, 38pin DC output	36	37	26	26	26	26	26	2.85	3.6	4.9	V
5-9	S-meter AC output	VSMAMAC-1	No input, 40pin DC output	36	37	26	26	26	26	26		0	0.5	V
		VSMAMAC-2	1MHz, 74dBμV, non-mod, 40pin DC output	36	37	26	26	26	26	26		0.75		V
5-10	Wide band AGC sensitivity	W-AGCsen1	1.4MHz, input at V48=0.7V	36	37	26	26	26	26	26	82	92	102	dBμV
5-11	SD sensitivity	SD-senAM	1MHz, ANT input level at which the SD pin is turned ON	37	37	26	26	26	26	26	25	30	35	dBμV

Function

1. AM / FM front-end block

FM Image rejection Mixer		
AM Double balance Mixer		
Pin diode drive AGC output		
Keyed AGC adjustment	4 bit DAC	
Differential IF amplifier		
Wide AGC sensitivity setting	4 bit DAC	
Narrow AGC sensitivity setting	4 bit DAC	
Local oscillator	160MHz to 260MHz	
FM Local OSC divider	1/1 1/2 1/3	
AM Local OSC divider	1/10, 1/8, 1/6, 1/4	

2. FM IF block

IF Limiter Amplifier 6 stages		
S-meter shifter	5 bit DAC	
S-meter output (DC/AC)		
Multipath detector (dedicated FM S-meter)		
Quadrature detector	Vnull adj-5bit, QDP adj-4bit	450kHz
AF preamplifier (Audio mute)		
AFC output		
Variable bandwidth control	CF adj-5bit DAC BW/Gain adj-5bit DAC Gain adj-3bit DAC (for setting filter)	

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Soft mute setting	5 bit DAC	
Mute attenuation setting	6 bit DAC	-0.5dB to -25dB
IF counter buffer (FM circuits)	10.7MHz	
SD (IF counter buffer activation level) setting	5 bit DAC	
SD output (active-high) (also used by AM circuits)		
IF output Driver for DSP (AF out, non-muting)		
SD: Station Detector		
IF Gain	4 bit DAC	

3. AM Block (back end of AM tuner)

Double balance 2nd mixer		
IF amplifier	4 bit DAC	
AM detector		
RF Narrow AGC	4 bit DAC	
Wide AGC	4 bit DAC	
Pin diode drive AGC output		
S-meter output	2 bit DAC	
IF counter buffer		450kHz
SD (IF counter buffer activation level) setting	5 bit DAC	
SD output (active-high)		
Detector output frequency adjusting pin (Low-cut, De-emphasis)		

4. FM NC

High-Pass-Filter (1st-order)		
Delay circuit of Low-Pass-Filter (4th order)		
Noise-AGC (Sensitivity:2 Bit-control)	2 bit DAC	
Pilot signal compensation		
Noise sensitivity setting		
Modulation index		

5. AM NC

AM Noise canceller Gate-Time	6 bit DAC	
AM Noise canceller OFF Level	5 bit DAC	

6. MPX

VCO (Free-Run Frequency:6 Bit-control)	6 bit DAC	304kHz
Level following pilot canceller	2 bit (3 step adj.)	
Automatic stereo/mono switching		
VCO oscillator stop (AM mode)		
Forced monaural		
Stereo indicator (active-low)		
Anti-birdie filter (f=114kHz, 190kHz)		
SNC (stereo noise control)	5 bit DAC	
HCC (high-cut control)	5 bit DAC	
Separation setting	6 bit	64 steps

7. MRC (Multipath-noise Rejection Circuit)

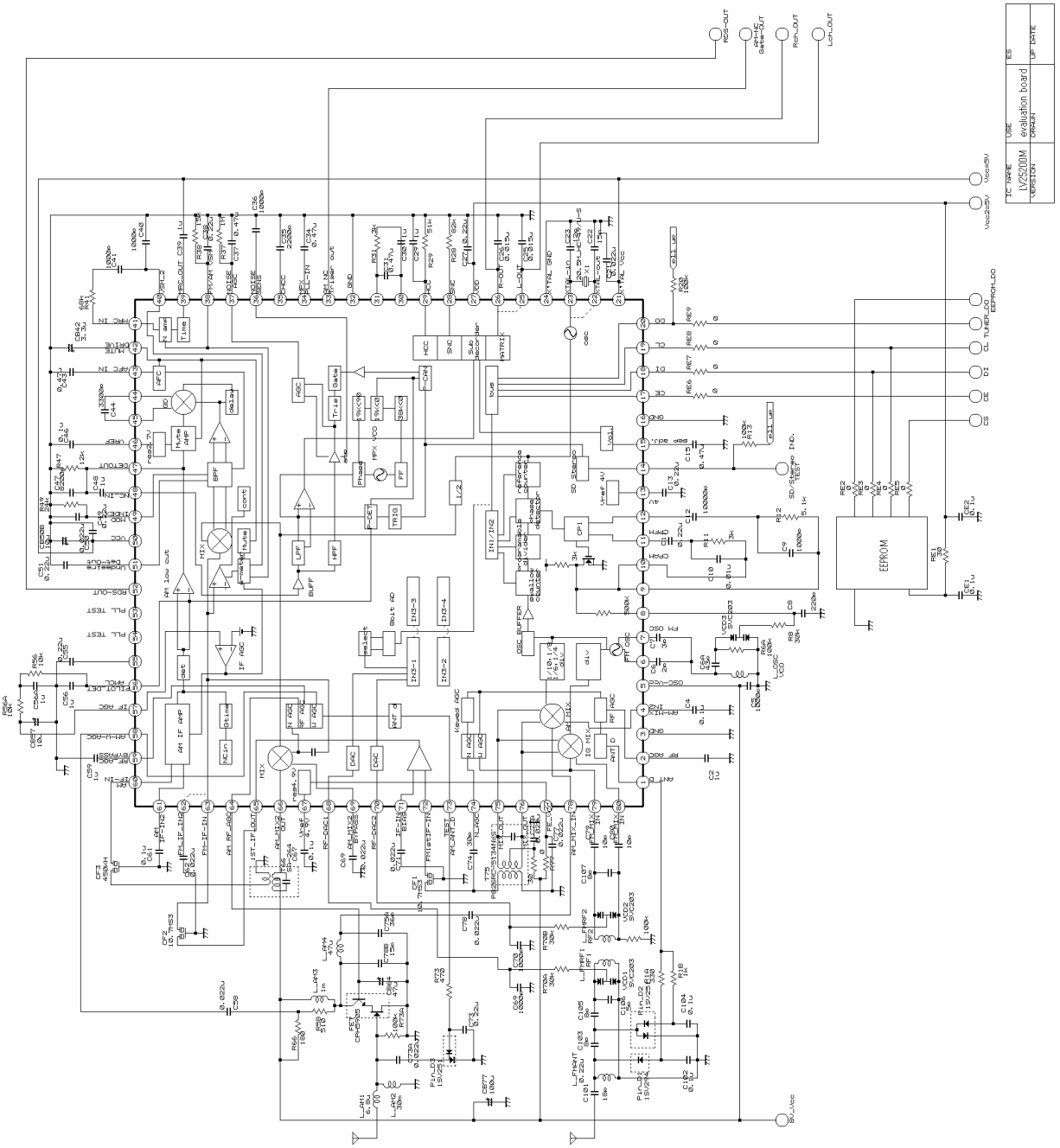
Noise Amplifier Gain (sensitivity setting)	2 bit	4 step
DC Level-Shifter		
SNC driving		
Time constant control circuit	2 bit	4 step

Pin Function

Pin No.	Function name	Block
1	FM-ANT-D	FE
2	FM-RF-AGC	FE
3	GND (FE)	---
4	AM-MIX-IN2	AM
5	OSC-V_{CC}	---
6	AM/FM-OSC (B)	FE
7	AM/FM-OSC (C)	FE
8	PLL-LPF	PLL
9	FM FET	PLL
10	AM FET	PLL
11	CPAM	PLL
12	CPFM	Common
13	PLL V_{DD}	MPX
14	ST/SD, VCO monitor and PLL-TEST	PLL
15	Sep.-ADJ.	MPX
16	GND (Analog)	---
17	CE	PLL
18	DI	PLL
19	CL	PLL
20	DO	PLL
21	V_{CC} (X'tal)	---
22	X'tal-OUT	X'tal
23	X'tal-IN	X'tal
24	GND (X'tal)	---
25	MPX-L-OUT	MPX
26	MPX-R-OUT	MPX
27	V_{CC} 5V (Digital)	---
28	SNC	MPX
29	HCC	MPX
30	MPX-PCO1	MPX
31	MPX-PCO2	MPX
32	GND (Digital)	---
33	NC-Gate- monitor	NC
34	MPX-PLL-IN	MPX
35	HCC capacity	MPX
36	Noise-Sens.	NC
37	Noise-AGC	NC
38	Vsm (Main)	IF
39	MRC-OUT	MRC
40	Vsm2 (Sub)	IF

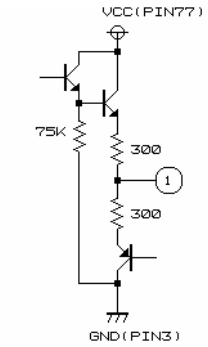
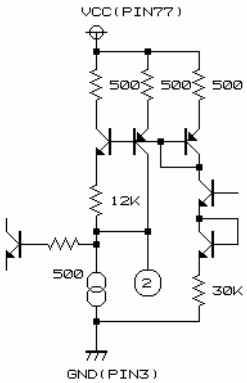
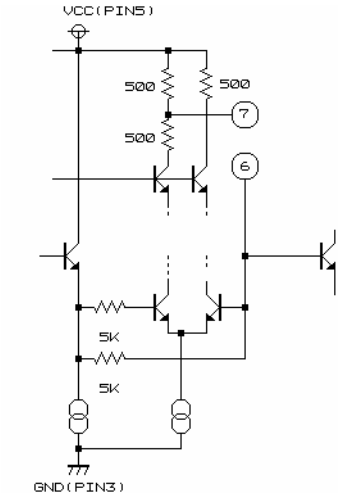
Pin-No.	Function name	Block
41	MRC-AC-IN	MRC
42	Mute-Drive	IF
43	AFC	IF
44	QD-Cap.	IF
45	QD-Cap.	IF
46	Vref 2.7V	Common
47	IF-Det-OUT	IF
48	NC-IN	NC
49	Mod.-Index	NC
50	V_{CC} 5V (Analog)	---
51	Interfering signal detected	FIL
52	RDS-OUT	IF
53	PLL-TEST	PLL
54	IF Filter OUT	FIL
55	AM-IFAGC (load for Vt setting)	AM
56	Pilot-Det/AM-LC	MPX/AM
57	IF-AGC	AM
58	AM-W-AGC	AM
59	AM-RF-AGC (BYPASS)	AM
60	AM-IF-IN	AM
61	AM-IN-IN2	AM
62	FM-IF-IN (BYPASS)	IF
63	FM-IF-IN AM-2nd-MIX-IN	IF AM
64	AM-RF-AGC	AM
65	1st-IF-OUT	FE
66	AM-MIX2-OUT	AM
67	Vref 4.9V	Common
68	RF-DAC1	FM
69	AM-2nd-MIX-IN (BYPASS)	AM
70	RF-DAC2	FM
71	IF-IN(BIAS)	FE
72	FM-1st-IF-IN	FE
73	AM-ANT-D and PLL-TEST	AM
74	N-AGC-IN	FE
75	MIX-OUT	FE
76	MIX-OUT	FE
77	V_{CC} (8V)	---
78	AM-MIX-IN	AM
79	FM-MIX-IN	FE
80	FM-MIX-IN	FE

Block Diagram



Pin Discription

Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
1	Antenna Damping Drive pin	Pin 2: Antenna damping current flows when the RF AGC voltage becomes V_{CC}-Vbe.	
2	RF AGC	RF AGC voltage. Voltage=Hi (around 8V) with AGC OFF. The voltage lowers when a level is inserted into the AGC circuit. AGC is applied at the voltage of V_{CC}-Vbe.	
3	FE.GND		FE GND(F.E.)
5	OSC V_{CC}	OSC dedicated V_{CC}	8V V_{CC} (VCO.)
6 7	FM/AM OSC IN FM/AM OSC OUT	OSC pin	

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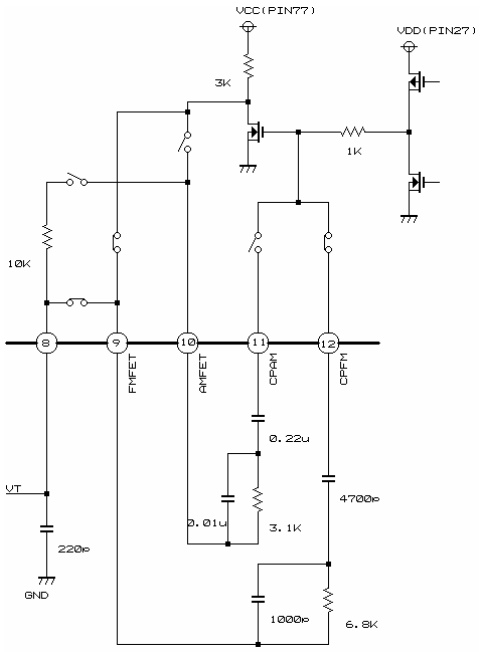
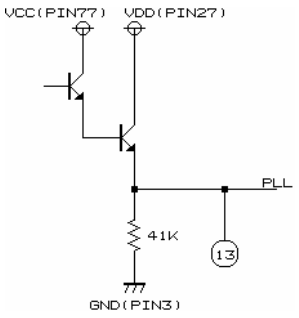
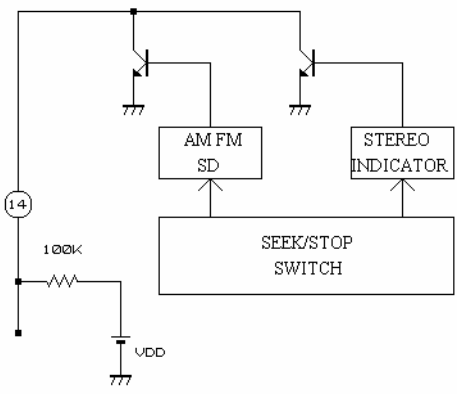
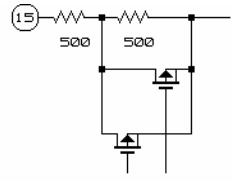
Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
8 9 10 11 12	Tuning voltage output LPF output FET for FM FET for AM Charge pump for FM Charge pump for AM	FM: PLL filter formed with pins 9 to 12 (Pins 10 and 11 to be left OPEN) AM: PLL filter formed with pins 10 and 11. In this case, the low pass filter is formed with the internal impedance (100kΩ) and external capacity. Simultaneous use of AM and FM filters (pins 9 to 12) is possible through mode changeover. In this case, internal impedance (100kΩ) is short-circuited.	
13	V_{DD} for PLL	PLL regulator output (4V)	
14	AM/FM SD pin STEREO indicator & VCO Monitor	STEREO indicator at reception: Low: STEREO High: MONO At SEEK: AM/FM SD ON=High OFF=Low Pin 14 output is output from DO (for SD information output). VCO monitor (at IN3-5 D6=H) Saw-tooth wave of MPX-VCO frequency is output, which is monitored for VCO adjustment (Adjust with IN3-5 D0-5.)	
15	Separation adjustment pin	The input level of sub-decoder is varied through BIT control. (The output level of MONO and MAIN remains unchanged.)	

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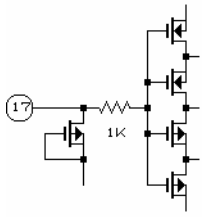
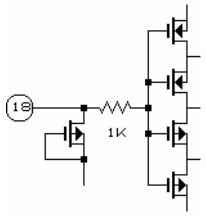
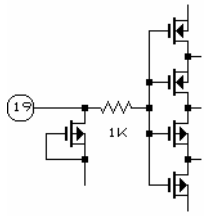
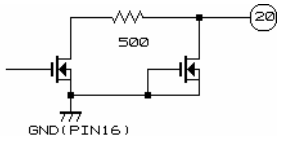
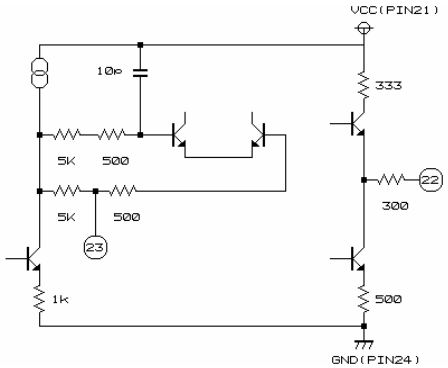
Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
16	N.C, MPX, MRC And PLL-GND		
17	CE	Pin to set the high level during serial data input (D1) to LV25200M or serial data output (DO).	
18	DI	Input pin for serial data for transfer from the controller to LV25200M	
19	CL	Clock for synchronization with the data during serial data input (DI) to LV25200M or serial data output (DO)	
20	DO	Output pin of serial data to be transferred from LV25200M to the controller	
21	V_{CC} 5V	X'tal-OSC dedicated V_{CC}	
22 23	X'tal-OSC-OUT X'tal-OSC-IN	Connect X'tal oscillator for 20.5MHz between pins 22 and 23. Connect capacitors, each 12pF, between pins 22 and 23 and GND.	
24	GND	X'tal-OSC dedicated GND	

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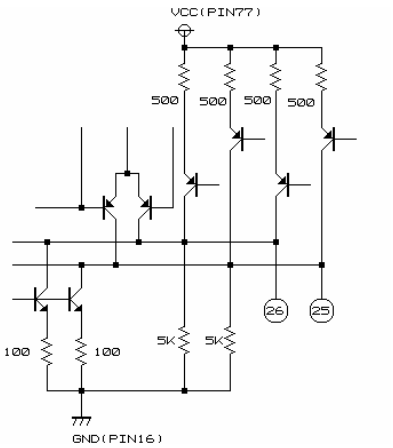
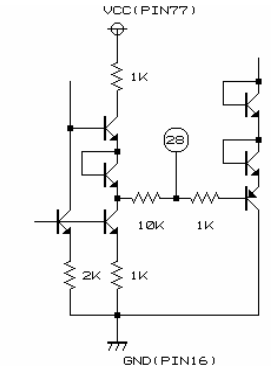
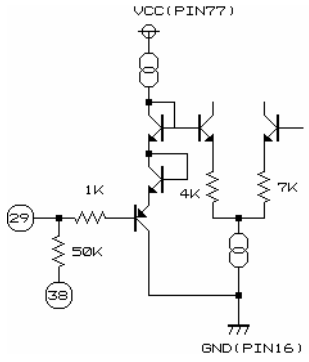
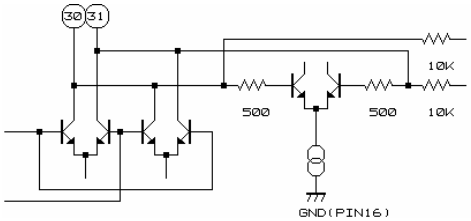
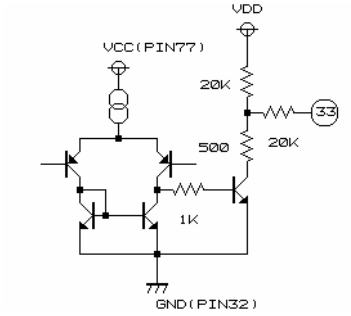
Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
25 26	MPX output (LEFT) MPX output (RIGHT)	MPX output Output impedance changed over with the de-Emphasis changeover Bit (IN3-4 D20) Low=3.3kΩ High=5kΩ (The figure in the right shows a case of 5kΩ.) (50/75μs changeover with the external capacity of 0.015μF)	
27	$V_{CC}2$ (5V)	V_{CC} for PLL and Digital system V_{CC}	
28	SNC control input pin	With the pin 28 input voltage, the attenuation of (L-R) Decode is controlled. ↓ Decrease Separation. ↓ The noise felt in the Stereo mode is reduced. (Threshold can be controlled with 5Bit.)	
29	HCC control input pin	With the pin 29 input voltage, attenuation of the high pass component is controlled. ↓ At weak input, high pass is cut to reduce the noise feeling. Same control for FM/AM HCC (f characteristics changed over automatically between AM and FM modes.) (Threshold can be controlled with 5Bit.)	
30 31	Phase-Comparator for MPX		
32	GND		
33	NC-Gate Trigger-OUT	Normal: High (V_{DD} potential) Gate: Low (0V) Note) Monitor output is not made unless the Bit setting of Pilot-Cancel is set to 11 (PICAN=OFF).	

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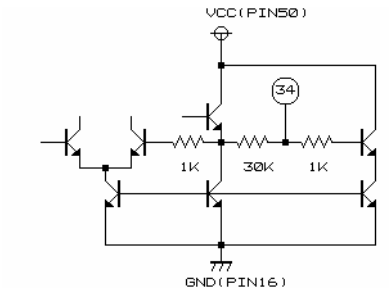
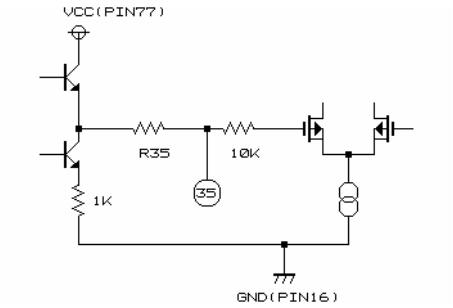
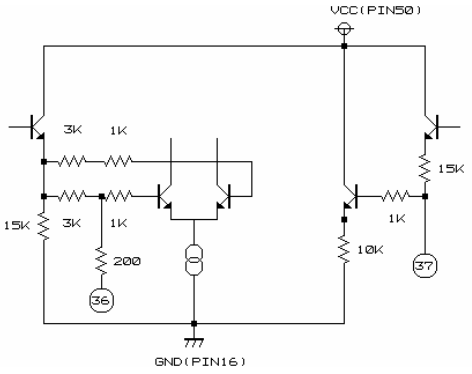
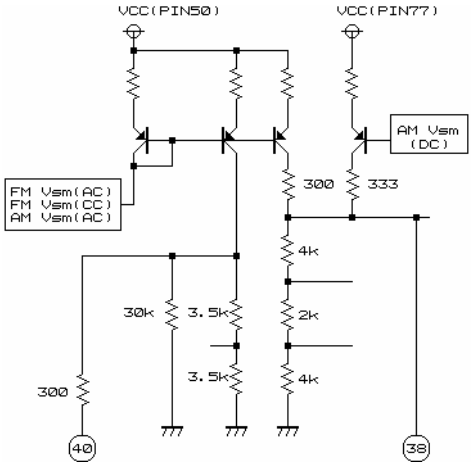
Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
34	MPX-PLL input	LPF formed with internal resistance 30kΩ and pin 34 eternal capacity ↓ HPF formed by subtracting the above LPS passage signal from the Composite signal. ↓ Supply to MPX-PLL circuit	
35	HCC capacitor pin	With pin 35 external capacity, High-Cut frequency characteristics are set. The value of internal resistance R35 is changed over in AM/FM mode: FM mode: R35=30kΩ AM mode: R35=100kΩ	
36 37	Noise detection sensitivity AGC adj pin	With the noise sensitivity setting pin of pin 36, set the medium electric field (about 50dBμ). Then, with the AGC-Adj pin of pin 37, carry out setting in the weak field (20 to 30dBμ).	
38 40	AM/FM S-meter (DC) AM/FM S-meter (AC)	Current drive type S-meter output Pin 38: Eliminate the AC component by external capacity Pin 40: Leaves the AC component (Pin for NC noise extraction and for multipath noise extraction)	

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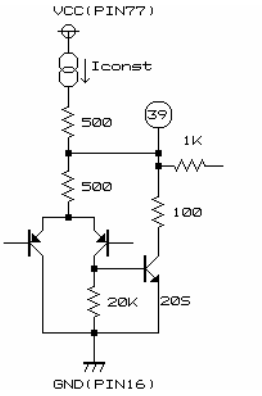
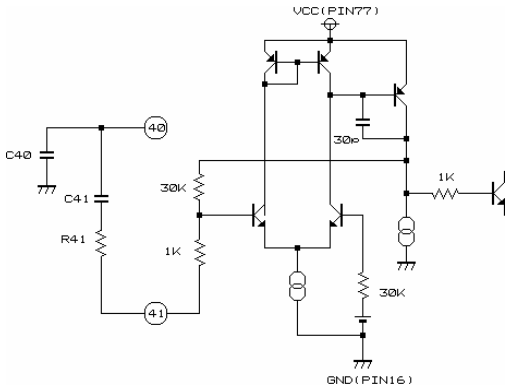
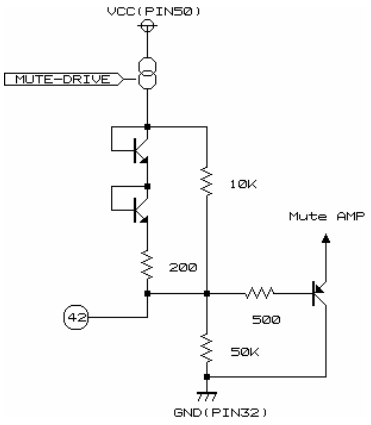
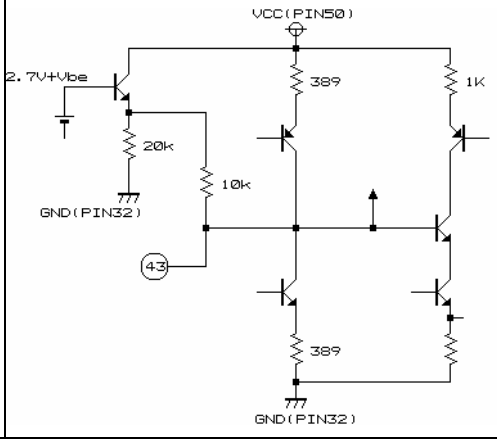
Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
39	MRC output (for SNC Control)	Time constant for Multipath-Noise Detector is determined with the following: 100Ω and C2 during discharge Iconst and C2 during charge Iconst can be changed over with 2Bit (MRC-Time-Constant)	
41	MRC AC input pin	From AC-S-meter (pin 40), enter the AC component. Amp-Gain, and frequency characteristics are determined with C41, (R41+1kΩ [internal resistance]) and 30kΩ (internal resistance). Amp-Gain can be controlled with 2Bit.	
42	Mute Drive	① The MUTE time constant is determined as follows by CR: • Attack time TA=10kΩ (R1) × C42 • Release time TR=50kΩ (R2) × C42 ② Noise convergence adjustment ③ MUTE OFF function MUTE is turned OFF when pin 42 is short-circuited with GND.	
43	AFC	Null voltage As compared with pin 46 2.7V	

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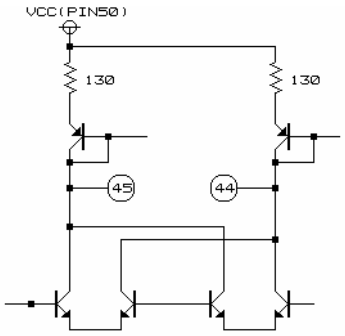
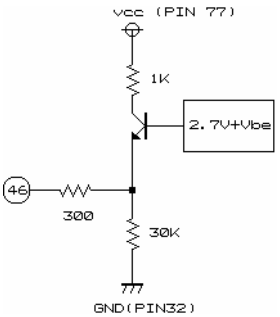
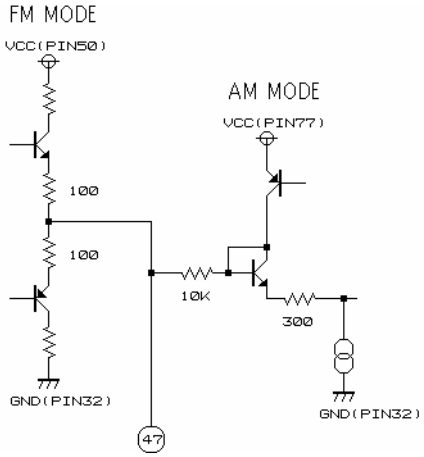
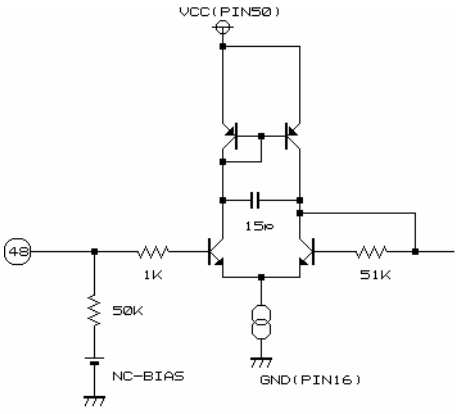
Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
44 45	FM DET capacity	FM quadrature detection capacity	
46	Vreg (2.7V)	2.7V regulator	
47	FM/AM DET OUT	AM/FM detection output Output impedance Low impedance in the FM mode 10kΩ in the AM mode	
48	Noise canceller input	Noise Canceller Input Input impedance 50kΩ	

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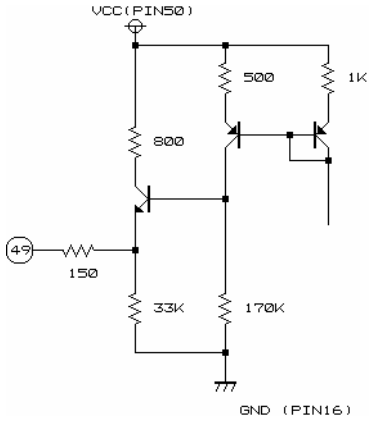
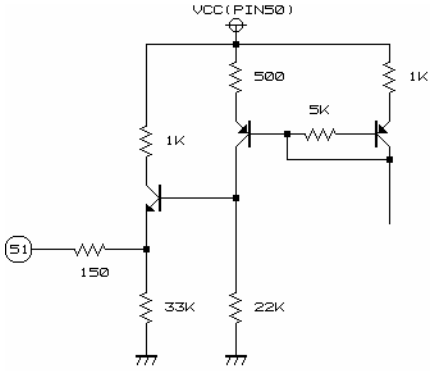
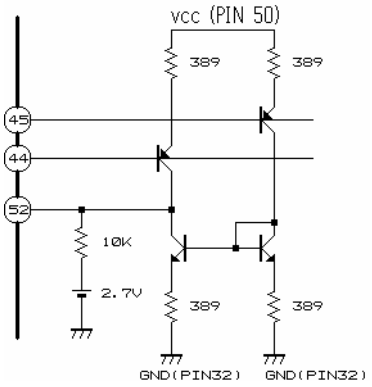
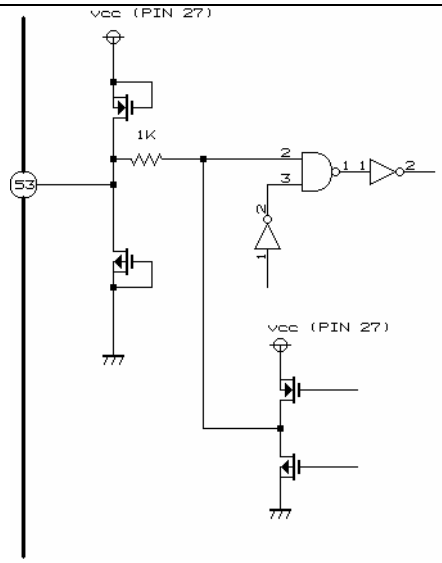
Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
49	MOD INDEX	Set the detection output level as DC output. C49 is the DC smoothing capacitor. (Used for control of the IF band variable filter)	
50	V_{CC} (5V) Analog system		
51	Undesire Det	Set the over-100kHz detection output noise level as DC output. C51 is the DC smoothing capacitor. (Used for control of the IF band variable filter)	
52	RDS OUT	FM detection output that is not passed through Mute AMP. * This output is not affected by the time constant due to muting.	
53	PLL TEST PIN	Test pin	

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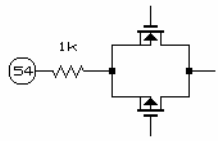
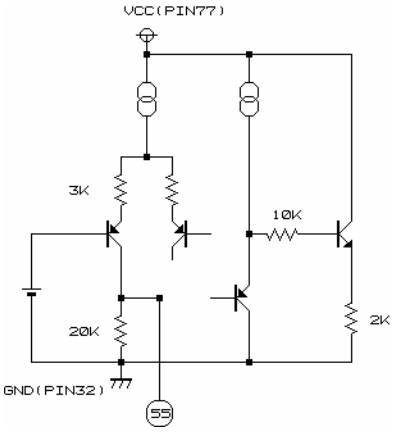
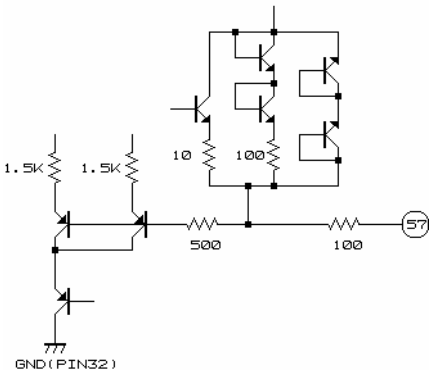
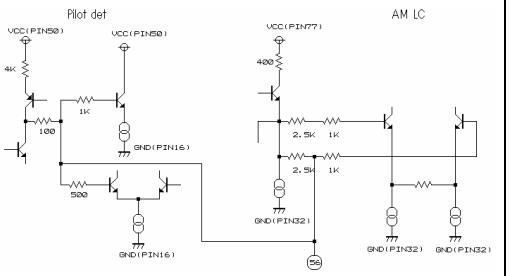
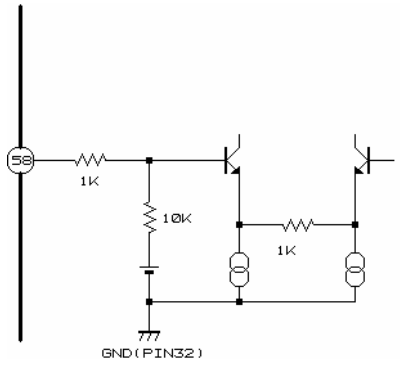
Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
54	PLL TEST PIN (IF band variable filter output)	IN3-1 Monitor • IF_FIL IF band variable filter output monitor (AC output)	
55	AM IFAGCBYPASS	IF AGC voltage DC smoothing capacitor pin	
57	AM IF AGC	TR1; Time constant changeover at Seek switch diode; 2.2μF Discharging diode ① At reception Time constant depends on the external LPF composition of pins 55 to 57. ② Seek Time constant is 57pin (C57) × 10Ω	
56	AM LC FM Pilot Det	AM LC; Frequency characteristics of unnecessary voice band of 100Hz or less is changed to produce the clear sound in the AM mode. AM LC f characteristic; Fc=1/(2π *2.5K*C56) Pilot Det; Insertion of 1MΩ between pin 56 and GND causes the forced MONO mode. For C56, 0.47μF or more is recommended.	
58	AM W-AGC	AMP for W-AGC pickup incorporated	

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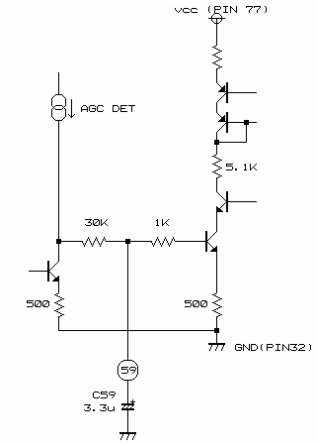
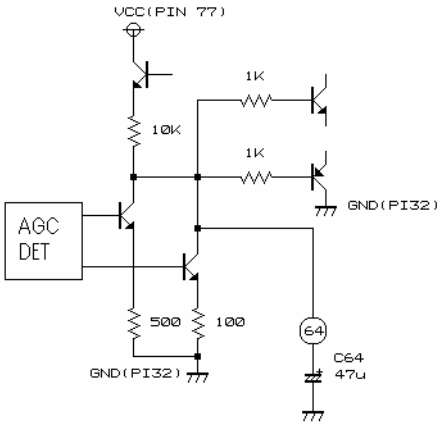
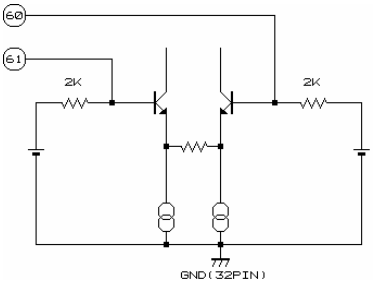
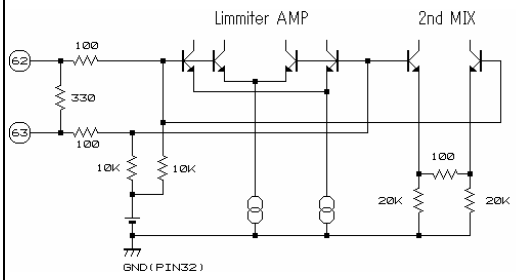
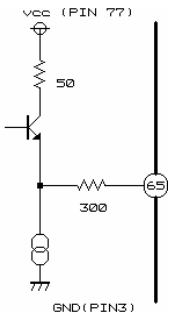
Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
59	AM RFAGC BYPASS	RF AGC rectifier capacitor Determination of the distortion ratio during low-frequency modulation Increase C59 and C64; Distortion → improved Response → slow Decrease C59 and C64; Distortion → worse Response → quick	
64	RF AGC	RF AGC rectifier capacitor Determination of distortion ratio during low-frequency modulation Increase C59 and C64; Distortion → improved Response → slow Decrease C59 and C64; Distortion → worse Response → quick	
60 61	AM IF AMP IN	AM 450kHz AMP input Input impedance=2kΩ	
62 63	FM 2nd MIX input FM AMP input	FM 2nd MIX 10.7MHz → 450kHz FM AMP (10.7MHz) AMP for S-meter voltage	
65	AM/FM 1st IF AMP OUTPUT	Output impedance=330Ω	

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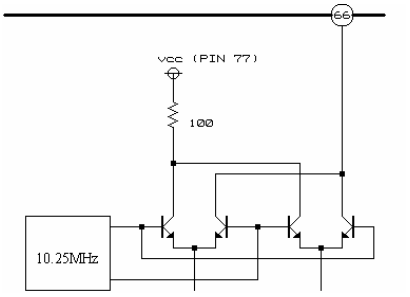
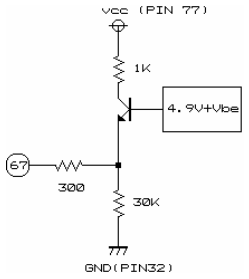
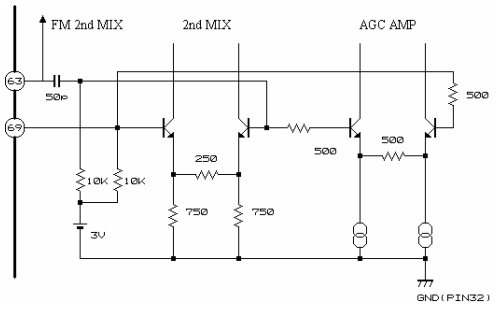
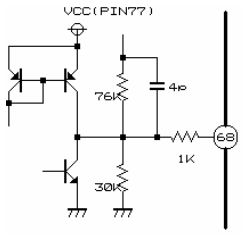
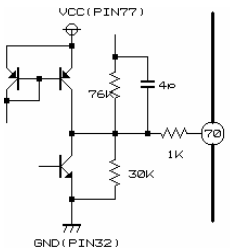
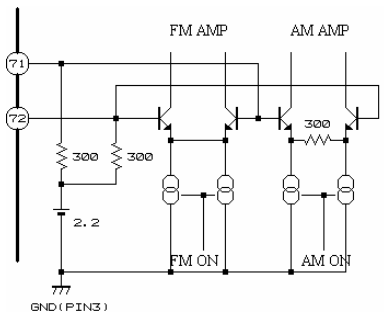
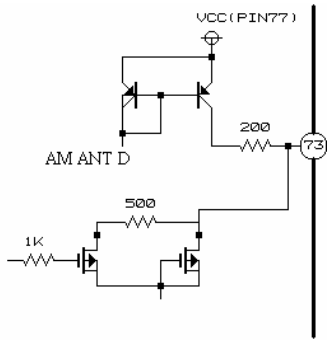
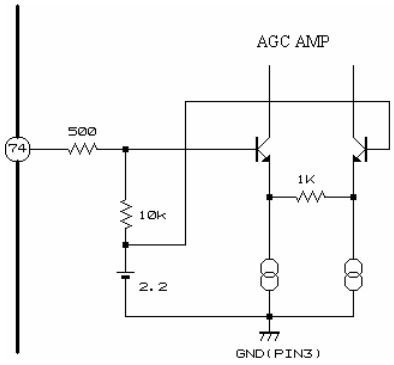
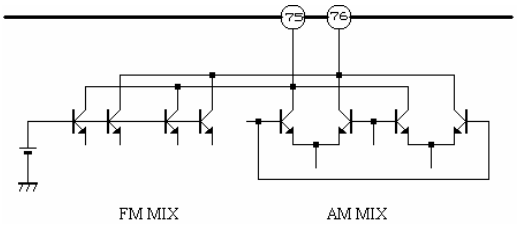
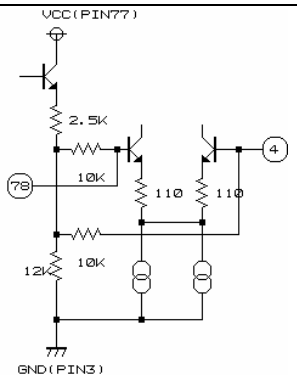
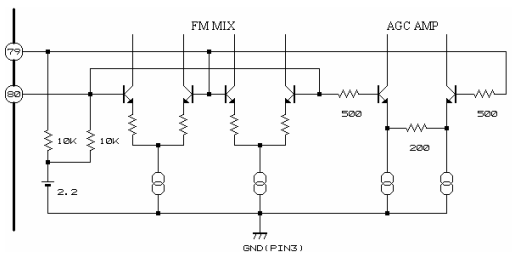
Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
66	AM 2nd MIX OUT	MIX coil connected to pin 66 MIX output must be connected to (V_{CC}).	
67	Vref 4.9V	4.9V regulator	
63 69	AM 2nd MIX input /AM AGC pick up	AM MIX input AMP for AM N-AGC pickup Input impedance 10kΩ	
68	RF DAC1	8bit DAC	
70	RF DAC2	8bit DAC	
71 72	FM/AM 1st IF AMP IN	10.7M AMP for FM/AM Input impedance=330Ω	

Continued on next page.

Continued from preceding page.

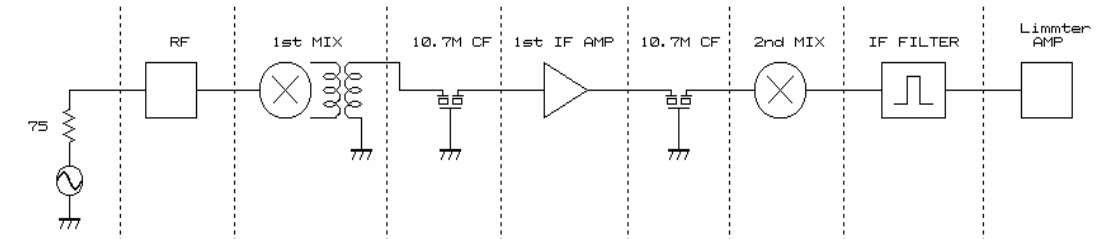
Unit (Resistance: Ω, Capacitance: F)

Pin	Function	Discription	Internal Equivalent Circuit
73	AM antenna damping output	For pin diode drive I73=6mA ANT damping current	
74	FM N-AGC IN	AMP for N-AGC pickup incorporated	
75 76	FM/AM 1st MIX OUT	FM/AM MIX OUT (common)	
77	V_{CC} (8V) FM FE, AM		
78	AM 1st MIX IN	AM MIX input Input impedance=10kΩ	
79 80	FM MIX IN FM W-AGC pick up	FM MIX input FM W-AGC pickup Input impedance=10kΩ	

FM/AM level Diagram

[FM]

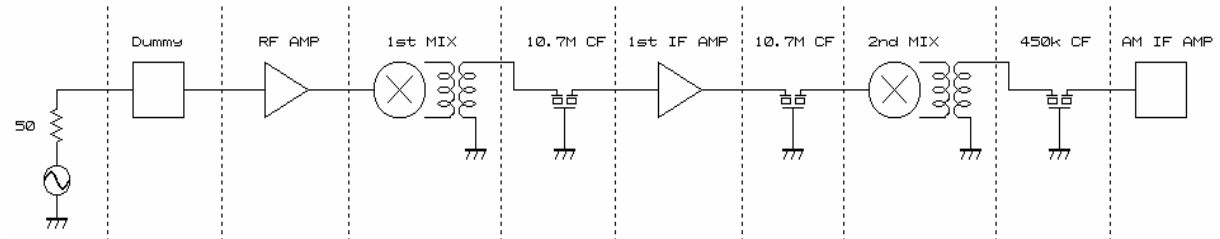
Input Condition : FM 98.1MHz, mod off, 30dBuV



	RF	1st MIX	10.7M CF	1st IF AMP	10.7M CF	2nd MIX	IF FILTER	
FM LEVEL	-2	28	-1.5	26.5	-3	14	0	dB

[AM]

Input Condition : AM 1MHz, mod off, 50dBuV

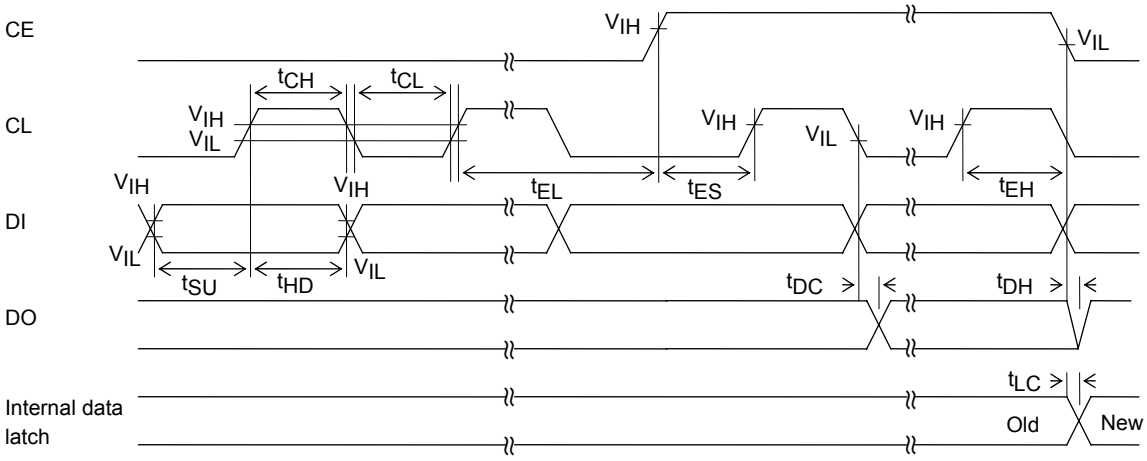


	JIS Dummy	RF AMP	1st MIX	10.7M CF	1st IF AMP	10.7M CF	2nd MIX	450k CF	
AM LEVEL	-18.1	26.8	5.7	-0.8	8	-3.9	10	-2.4	dB

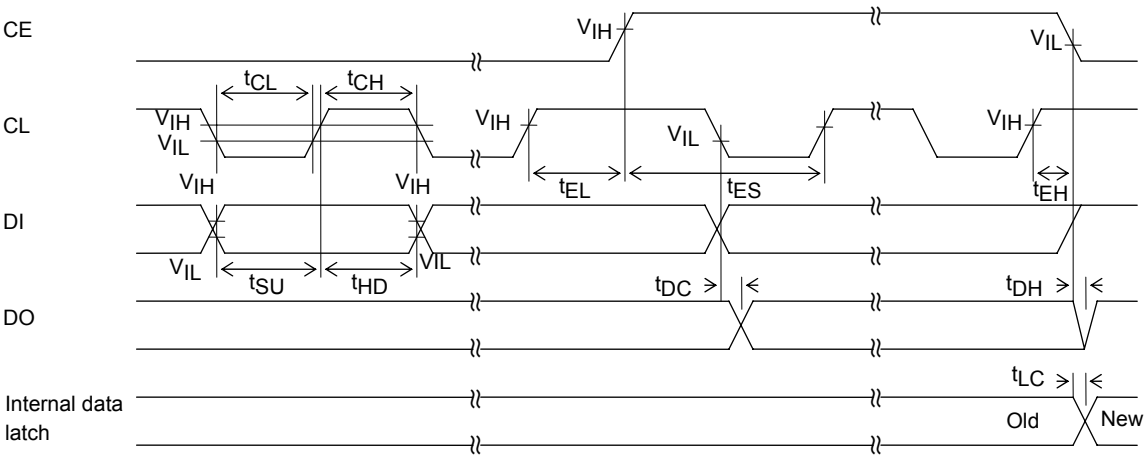
Serial Bus Data Timing

CE: Chip enable DI: Input data
CL: Clock DO: Output data

<<CL stopped at “L” level >>



<<CL stopped at “H” level >>

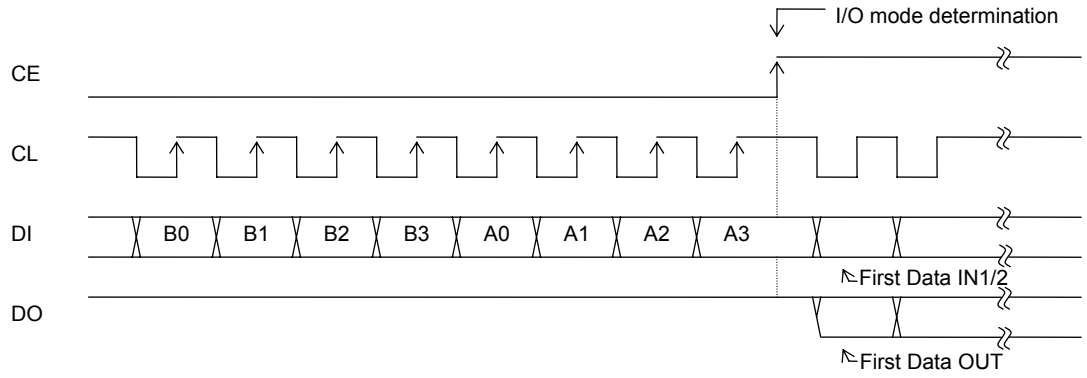


Parameter	Symbol	Pin	Conditions	min	typ	max	unit
Data setup time	t_{SU}	DI, CL		0.45			µs
Data hold time	t_{HD}	DI, CL		0.45			µs
Clock L level time	t_{CL}	CL		0.45			µs
Clock H level time	t_{CH}	CL		0.45			µs
CE wait time	t_{EL}	CE, CL		0.45			µs
CE setup time	t_{ES}	CE, CL		0.45			µs
CE hold time	t_{EH}	CE, CL		0.45			µs
Data latch change time	t_{LC}					0.45	µs
Data output time	t_{DC}	DO, CL	Varies depending on the pull-up resistance			0.2	µs
	t_{DH}	DO, CE					

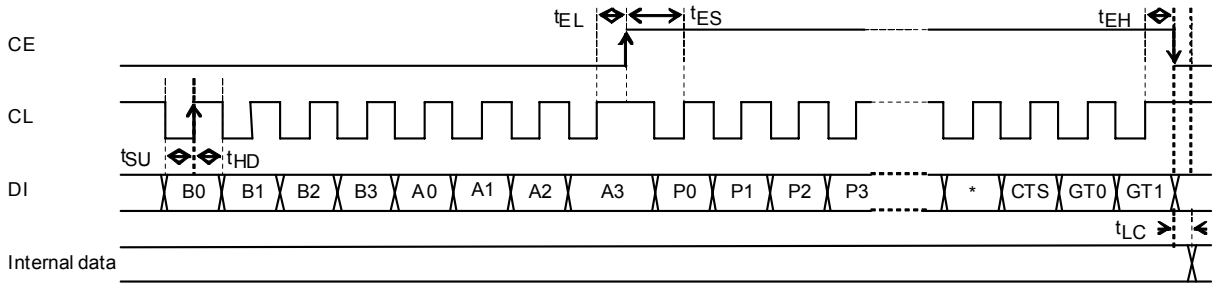
Serial Data I/O Method

This is the Sanyo Audio IC serial bus format. Data I/O is made with CCB (Computer Control Bus).
LV25200M is the 8-bit address type CCB.

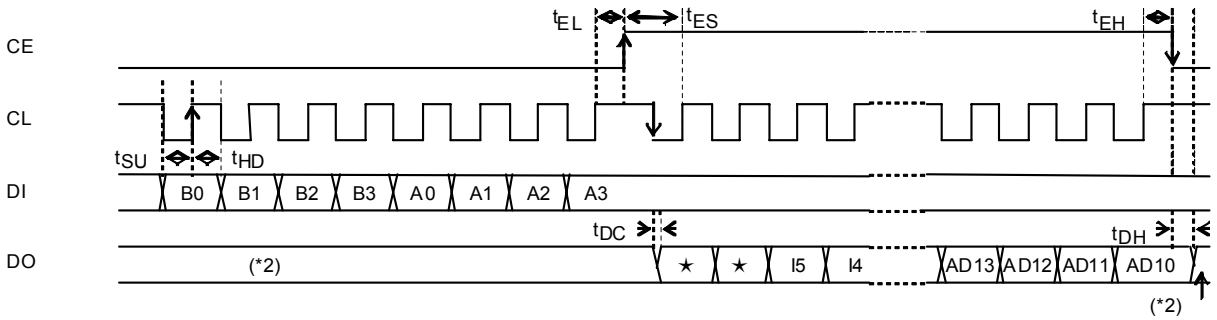
	I/O mode	Address								Description
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1	0	0	0	1	0	1	0	0	• Control data input (serial data input) mode. PLL setting • 32-bit data input
[2]	IN2	1	0	0	1	0	1	0	0	• Control data input (serial data input) mode. PLL setting • 32-bit data input
[3]	IN3	1	0	0	1	0	1	1	0	• Control data input (serial data input) mode, set by the tuner • 32-bit data input with sub-address
[4]	OUT	0	1	0	1	0	1	0	0	• Output data (serial data output) mode • Output of data corresponding to the clock amount. Max 48 bits



i) Serial data input (IN1/IN2/IN3) t_{SU}, t_{HD}, t_{ES}, t_{EL}, t_{EH}, > 0.45µs t_{LC} < 0.45µs



ii) Serial data output (OUT) t_{SU}, t_{HD}, t_{ES}, t_{EL}, > 0.45µs t_{DC}, t_{DH} < 0.2µs (*1)



(*1) As the DO pin is the Nch open drain pin, so that the data change time varies depending on the pull-up resistance and substrate capacity.
(*2) Normally, keep the DO pin in the OPEN state.

bit specification
IN1 setting

B0	B1	B2	B3	A0	A1	A2	A3

0	0	0	1	0	1	0	0

Address Code

OSC dividing ratio control for AM

OSD D1	OSC D2	Dividing ratio
0	0	10-division
0	1	8-division
1	0	6-division
1	1	4-division

CTE

0	IF count reset
1	IFcount start

DVS

0	Program-CTR stop
1	Program-CTR normal operation

	D1-0	D1-1	D1-2	D1-3	D1-4	D1-5	D1-6	D1-7	D1-8	D1-9	D1-10	D1-11	D1-12	D1-13	D1-14	D1-15	D1-16	D1-17	D1-18	D1-19	D1-20	D1-21	D1-22	D1-23	D1-24	D1-25	D1-26	D1-27	D1-28	D1-29	D1-30	D1-31
	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	OSC D1	OSC D2		CTE	R0	R1	R2	R3	DVS	AM/FM	SEEK1	SEEK2	MODE1	MODE2	WEATHER	DIV_SW3
Initial data at power ON	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H		L	L	L	L	L	L	H	L	L	L	L	L	L
	(1)																(2)			(3)	(4)				(5)	(6)	(7)		(8)		(9)	

Setting Program-CTR divisions (272 to 65535 divisions)

0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0	272-division
:	:
0 0 1 0 1 1 1 1 1 0 0 0 0 0 0 0	500-division
:	:
0 0 0 1 0 1 1 1 1 1 0 0 0 0 0 0	1000-division
:	:
0 0 0 0 1 0 1 1 1 1 1 0 0 0 0 0	2000-division
:	:
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0	21845-division
:	:
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	43690-division
:	:
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	65535-division

Reference frequency setting

0 0 0 0	Do not use
1 0 0 0	100kHz
0 1 0 0	50kHz
1 1 0 0	25kHz
0 0 1 0	12.5kHz
1 0 1 0	6.25kHz
0 1 1 0	3.125kHz
1 1 1 0	3.125kHz
0 0 0 1	10kHz
1 0 0 1	Do not use
0 1 0 1	5kHz
1 1 0 1	1kHz
0 0 1 1	Do not use
1 0 1 1	Do not use
0 1 1 1	Do not use
1 1 1 1	Do not use

AM/FM

0	FM
1	AM

PLL filter changeover

MODE1	MODE2	AM/FM	SEEK1	SEEK2	AM filter	FM filter
0	0	0	*	*	OFF	ON
0	0	1	*	*	ON	OFF
1	0	0	1	1	OFF	ON
1	0	0	0	1	OFF	ON
1	0	0	1	0	ON	OFF
1	0	1	*	*	ON	OFF
0	1	0	1	1	OFF	ON
0	1	0	0	1	OFF	ON
0	1	0	1	0	ON	ON
0	1	1	*	*	ON	ON

* Don't care

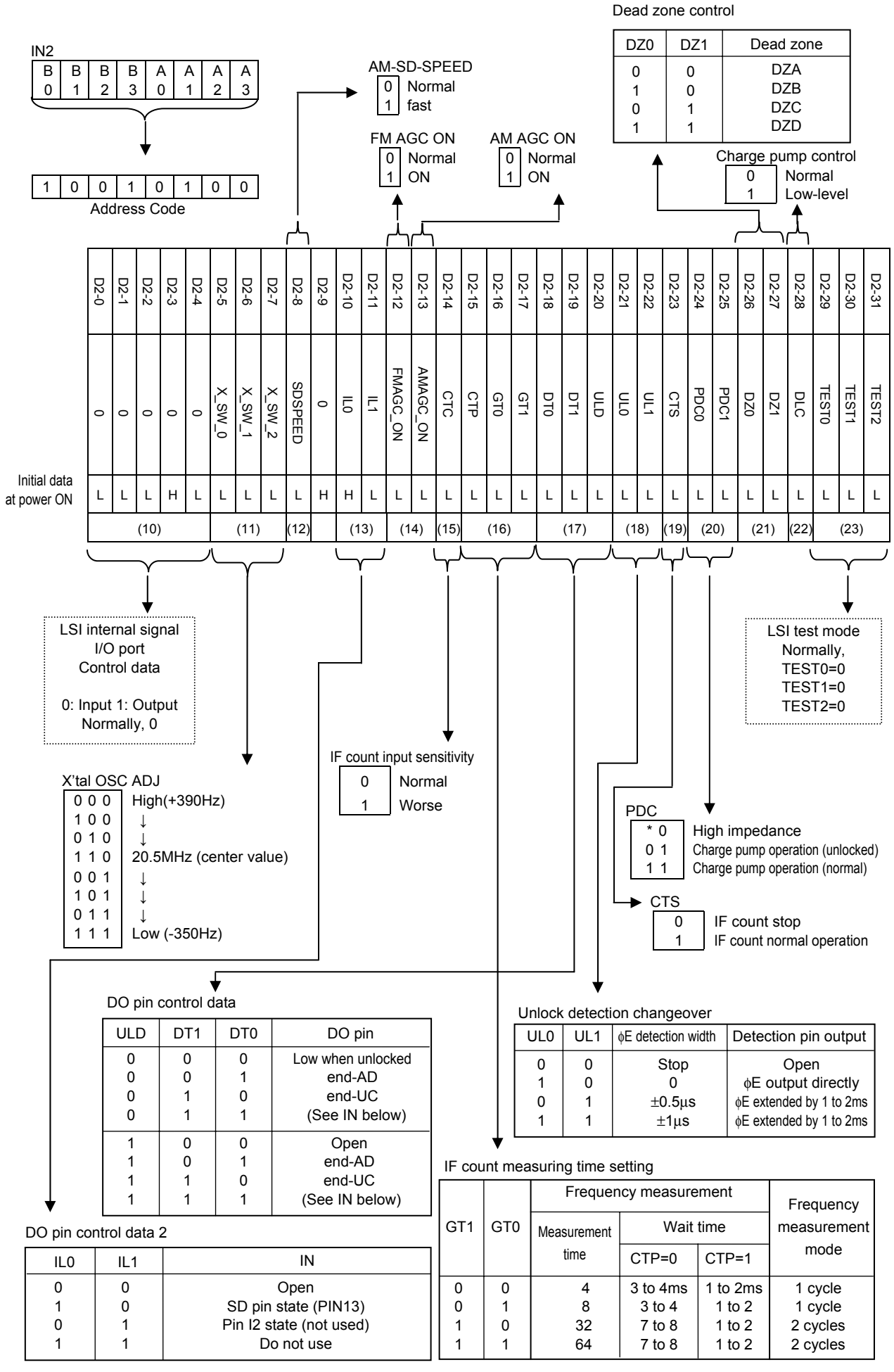
Tuner mode changeover

SEEK1	SEEK2	IFBC output
0	0	Do not use
1	0	STOP
0	1	RDS
1	1	SEEK

OSC ratio control for AM/FM/WB

WEATHER	DIV_SW3	Dividing ratio
0	0	2-division
0	1	3-division
1	0	1-division
1	1	1-division

* Select "1" for WB: Weather Band


IN2
B0 B1 B2 B3 A0 A1 A2 A3
1 0 0 1 0 1 0 0
Address Code
AM-SD-SPEED
0 Normal
1 fast
FM AGC ON
0 Normal
1 ON
AM AGC ON
0 Normal
1 ON
Dead zone control
DZ0 DZ1 Dead zone
0 0 DZA
1 0 DZB
0 1 DZC
1 1 DZD
Charge pump control
0 Normal
1 Low-level
D2-0 D2-1 D2-2 D2-3 D2-4 D2-5 D2-6 D2-7 D2-8 D2-9 D2-10 D2-11 D2-12 D2-13 D2-14 D2-15 D2-16 D2-17 D2-18 D2-19 D2-20 D2-21 D2-22 D2-23 D2-24 D2-25 D2-26 D2-27 D2-28 D2-29 D2-30 D2-31
0 0 0 0 0 X_SW_0 X_SW_1 X_SW_2 SDSPEED 0 IL0 IL1 FMAGC_ON AMAGC_ON CTC CTP GT0 GT1 DT0 DT1 ULD UL0 UL1 CTS PDC0 PDC1 DZ0 DZ1 DLC TEST0 TEST1 TEST2
Initial data at power ON
L L L H L L L L L H H L L L L L L L L L L L L L L L L L L L
(10) (11) (12) (13) (14) (15) (16) (17) (18) (19) (20) (21) (22) (23)
LSI internal signal I/O port Control data
0: Input 1: Output
Normally, 0
LSI test mode
Normally,
TEST0=0
TEST1=0
TEST2=0
X'tal OSC ADJ
0 0 0 High(+390Hz)
1 0 0 ↓
0 1 0 ↓
1 1 0 20.5MHz (center value)
0 0 1 ↓
1 0 1 ↓
0 1 1 ↓
1 1 1 Low (-350Hz)
IF count input sensitivity
0 Normal
1 Worse
PDC
* 0 High impedance
0 1 Charge pump operation (unlocked)
1 1 Charge pump operation (normal)
CTS
0 IF count stop
1 IF count normal operation
DO pin control data
ULD DT1 DT0 DO pin
0 0 0 Low when unlocked
0 0 1 end-AD
0 1 0 end-UC
0 1 1 (See IN below)
1 0 0 Open
1 0 1 end-AD
1 1 0 end-UC
1 1 1 (See IN below)
Unlock detection changeover
UL0 UL1 φE detection width Detection pin output
0 0 Stop Open
1 0 0 φE output directly
0 1 ±0.5μs φE extended by 1 to 2ms
1 1 ±1μs φE extended by 1 to 2ms
IF count measuring time setting
GT1 GT0 Frequency measurement Measurement time Wait time CTP=0 CTP=1 Frequency measurement mode
0 0 4 3 to 4ms 1 to 2ms 1 cycle
0 1 8 3 to 4 1 to 2 1 cycle
1 0 32 7 to 8 1 to 2 2 cycles
1 1 64 7 to 8 1 to 2 2 cycles
DO pin control data 2
IL0 IL1 IN
0 0 Open
1 0 SD pin state (PIN13)
0 1 Pin I2 state (not used)
1 1 Do not use

IN3-1 tuner setting 2
Address 69h, Subaddress[0 0]

B0	B1	B2	B3	A0	A1	A2	A3

1	0	0	1	0	1	1	0

Address Code

0	0	0

Sub Address Code

	D31-0	D31-1	D31-2	D31-3	D31-4	D31-5	D31-6	D31-7	D31-8	D31-9	D31-10	D31-11	D31-12	D31-13	D31-14	D31-15	D31-16	D31-17	D31-18	D31-19	D31-20	D31-21	D31-22	D31-23	D31-24	D31-25	D31-26	D31-27	D31-28	D31-29	D31-30	D31-31
Initial data at power ON	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	(24)									(25)	(26)									(27)	(28)						(29)		(30)	(65)			

Internal monitor changeover

0	IF-Filter
1	No use

MSLOP

0	Mute_D (steep inclination)
1	Mute_D (gentle inclination)

Filter-Fix_SW

D26	D27	Filter-Mode
0	0	Variable
1	0	Narrow-Fix
0	1	Wide-Fix
1	1	Dont Care

RF- DAC

0 0 0 0 0 0 0 0 0 0	0.3V
1 0 0 0 0 0 0 0 0 0	↓
0 1 0 0 0 0 0 0 0 0	↓
1 1 0 0 0 0 0 0 0 0	↓
0 0 1 0 0 0 0 0 0 0	↓
1 0 1 0 0 0 0 0 0 0	↓
0 1 1 0 0 0 0 0 0 0	↓
1 1 1 0 0 0 0 0 0 0	↓
0 0 0 1 0 0 0 0 0 0	↓
•	↓
•	↓
0 1 0 1 1 1 1 1 1 1	↓
1 1 0 1 1 1 1 1 1 1	↓
0 0 1 1 1 1 1 1 1 1	↓
1 0 1 1 1 1 1 1 1 1	↓
0 1 1 1 1 1 1 1 1 1	↓
1 1 1 1 1 1 1 1 1 1	7.1V

ANT- DAC

0 0 0 0 0 0 0 0 0 0	0.3V
1 0 0 0 0 0 0 0 0 0	↓
0 1 0 0 0 0 0 0 0 0	↓
1 1 0 0 0 0 0 0 0 0	↓
0 0 1 0 0 0 0 0 0 0	↓
1 0 1 0 0 0 0 0 0 0	↓
0 1 1 0 0 0 0 0 0 0	↓
1 1 1 0 0 0 0 0 0 0	↓
0 0 0 1 0 0 0 0 0 0	↓
•	↓
•	↓
0 1 0 1 1 1 1 1 1 1	↓
1 1 0 1 1 1 1 1 1 1	↓
0 0 1 1 1 1 1 1 1 1	↓
1 0 1 1 1 1 1 1 1 1	↓
0 1 1 1 1 1 1 1 1 1	↓
1 1 1 1 1 1 1 1 1 1	7.1V

TEST for DAC
0: Normal
1: Test-Mode

Test-PAD--1

D2	D1	D0	OUT
0	0	0	VSM_SHIFTER
0	0	1	FM-Mute-ON-Adj
0	1	0	NC_GT(DACOUT)
0	1	1	SNC_DAC / ARAG(H)
1	0	0	HCC_DAC
1	0	1	SD_ADJ
1	1	0	Mute_ATT(DACOUT2)
1	1	1	Mute-ANG

Test-PAD--2

D4	D3	OUT
0	0	W_AGC
0	1	N_AGC
1	0	A_IFGAIN
1	1	QDP_ADJ

Band variable filter
Narrow/wide Min (Max) value control

Narrow LMT Cont
D20 D21 D22

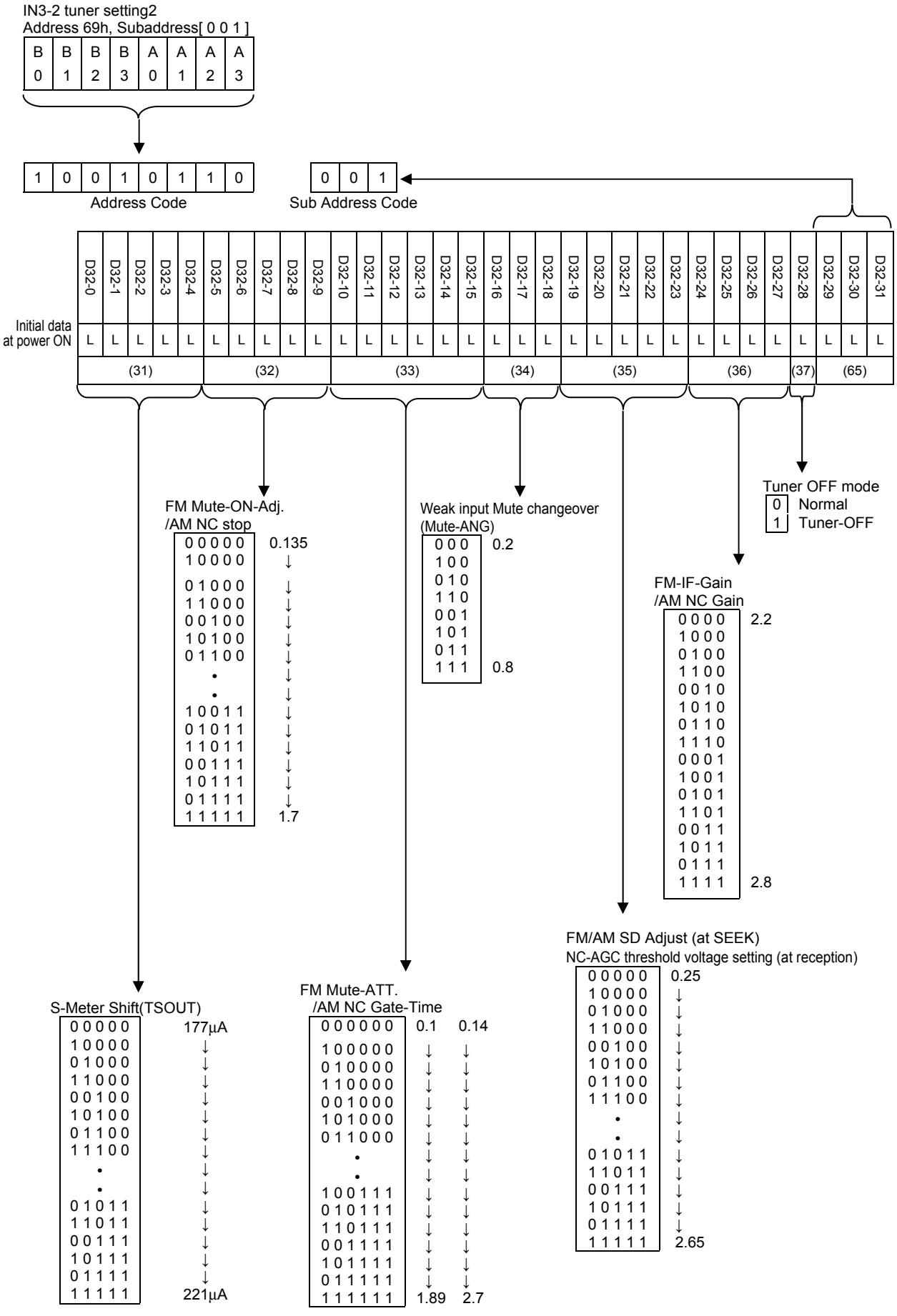
0 0 0	Min (40k)
1 0 0	
0 1 0	
•	
•	
1 0 1	
0 1 1	
1 1 1	Max (80k)

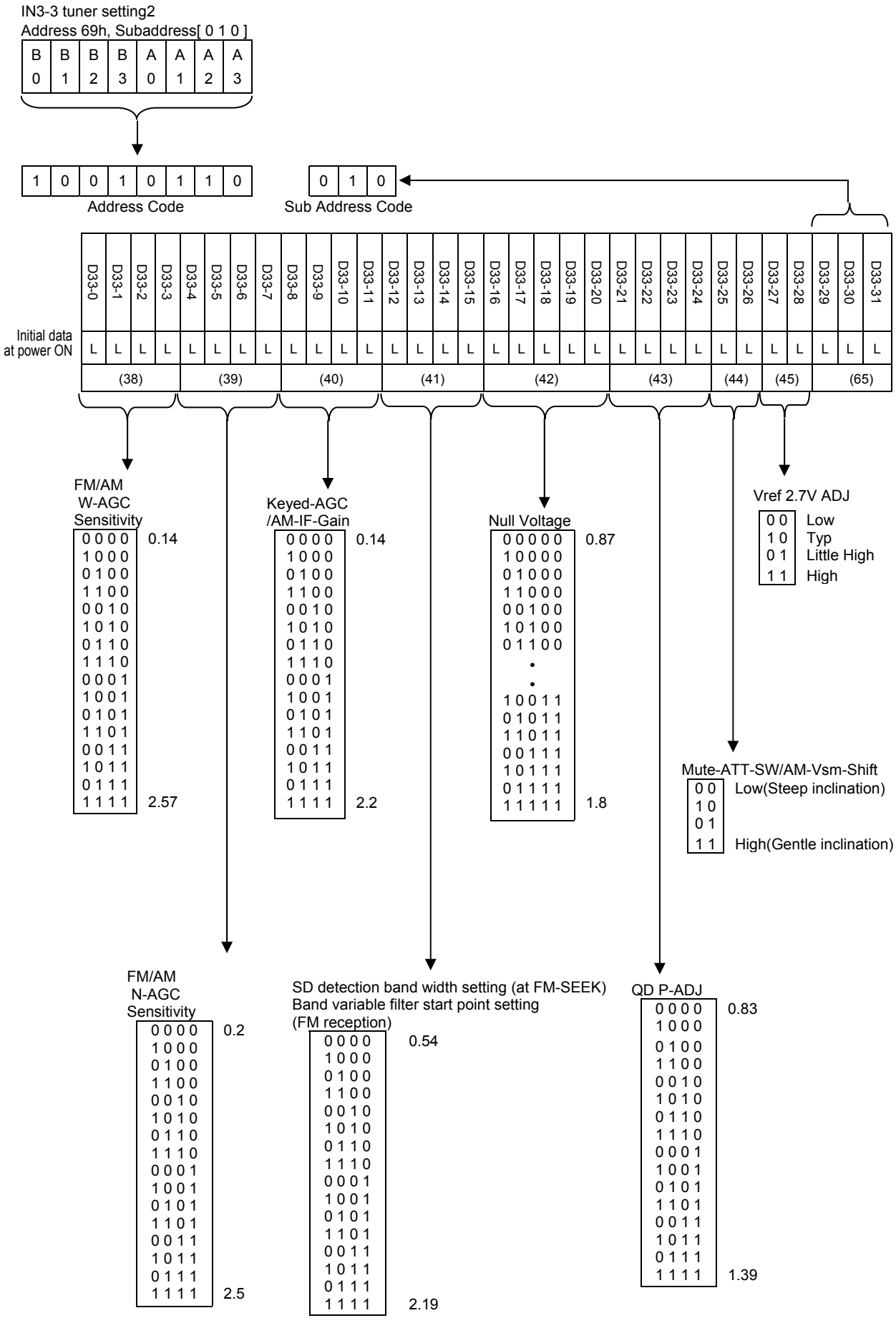
Wide LMT Cont
D23 D24 D25

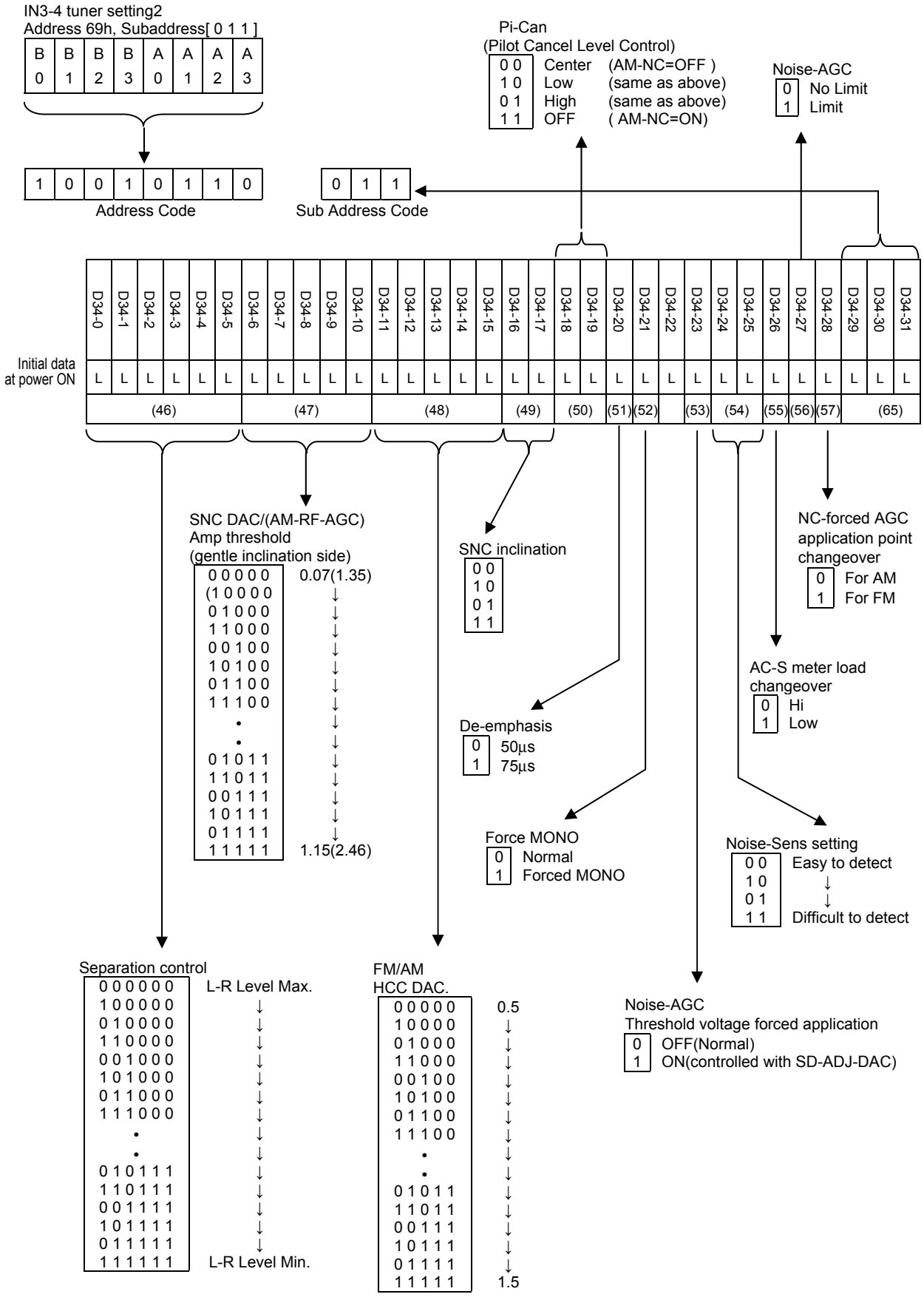
0 0 0	Max (220k)
1 0 0	
0 1 0	
•	
•	
1 0 1	
0 1 1	
1 1 1	Min (150k)

Test-PAD--3

D7	D6	D5	OUT
0	0	0	F_IFGAIN
0	0	1	NULL_VOL
0	1	0	AFC_BW(TSOUT=-2VBE)
0	1	1	AM_RFAGC(S)
1	0	0	KEYD_AGC


IN3-2 tuner setting2
Address 69h, Subaddress[0 0 1]
B0 B1 B2 B3 A0 A1 A2 A3
1 0 0 1 0 1 1 0
Address Code
0 0 1
Sub Address Code
D32-0 D32-1 D32-2 D32-3 D32-4 D32-5 D32-6 D32-7 D32-8 D32-9 D32-10 D32-11 D32-12 D32-13 D32-14 D32-15 D32-16 D32-17 D32-18 D32-19 D32-20 D32-21 D32-22 D32-23 D32-24 D32-25 D32-26 D32-27 D32-28 D32-29 D32-30 D32-31
Initial data at power ON
L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L
(31) (32) (33) (34) (35) (36) (37) (65)
FM Mute-ON-Adj. /AM NC stop
0 0 0 0 0 0.135
1 0 0 0 0
0 1 0 0 0
1 1 0 0 0
0 0 1 0 0
1 0 1 0 0
0 1 1 0 0
1 0 0 1 1
0 1 0 1 1
1 1 0 1 1
0 0 1 1 1
1 0 1 1 1
0 1 1 1 1
1 1 1 1 1 1.7
Weak input Mute changeover (Mute-ANG)
0 0 0 0.2
1 0 0
0 1 0
1 1 0
0 0 1
1 0 1
0 1 1
1 1 1 0.8
Tuner OFF mode
0 Normal
1 Tuner-OFF
FM-IF-Gain /AM NC Gain
0 0 0 0 2.2
1 0 0 0
0 1 0 0
1 1 0 0
0 0 1 0
1 0 1 0
0 1 1 0
1 1 1 0
0 0 0 1
1 0 0 1
0 1 0 1
1 1 0 1
0 0 1 1
1 0 1 1
0 1 1 1
1 1 1 1 2.8
FM/AM SD Adjust (at SEEK)
NC-AGC threshold voltage setting (at reception)
0 0 0 0 0 0.25
1 0 0 0 0
0 1 0 0 0
1 1 0 0 0
0 0 1 0 0
1 0 1 0 0
0 1 1 0 0
1 1 1 0 0
0 1 0 1 1
1 1 0 1 1
0 0 1 1 1
1 0 1 1 1
0 1 1 1 1
1 1 1 1 1 2.65
S-Meter Shift(TSOUT)
0 0 0 0 0 177µA
1 0 0 0 0
0 1 0 0 0
1 1 0 0 0
0 0 1 0 0
1 0 1 0 0
0 1 1 0 0
1 1 1 0 0
0 1 0 1 1
1 1 0 1 1
0 0 1 1 1
1 0 1 1 1
0 1 1 1 1
1 1 1 1 1 221µA
FM Mute-ATT. /AM NC Gate-Time
0 0 0 0 0 0 0.1 0.14
1 0 0 0 0 0
0 1 0 0 0 0
1 1 0 0 0 0
0 0 1 0 0 0
1 0 1 0 0 0
0 1 1 0 0 0
1 0 0 1 1 1
0 1 0 1 1 1
1 1 0 1 1 1
0 0 1 1 1 1
1 0 1 1 1 1
0 1 1 1 1 1
1 1 1 1 1 1 1.89 2.7


IN3-3 tuner setting2
Address 69h, Subaddress[0 1 0]
B0 B1 B2 B3 A0 A1 A2 A3
1 0 0 1 0 1 1 0
Address Code
0 1 0
Sub Address Code
D33-0 D33-1 D33-2 D33-3 D33-4 D33-5 D33-6 D33-7 D33-8 D33-9 D33-10 D33-11 D33-12 D33-13 D33-14 D33-15 D33-16 D33-17 D33-18 D33-19 D33-20 D33-21 D33-22 D33-23 D33-24 D33-25 D33-26 D33-27 D33-28 D33-29 D33-30 D33-31
Initial data at power ON
(38) (39) (40) (41) (42) (43) (44) (45) (65)
FM/AM W-AGC Sensitivity
0 0 0 0 0.14
1 0 0 0
0 1 0 0
1 1 0 0
0 0 1 0
1 0 1 0
0 1 1 0
1 1 1 0
0 0 0 1
1 0 0 1
0 1 0 1
1 1 0 1
0 0 1 1
1 0 1 1
0 1 1 1
1 1 1 1 2.57
Keyed-AGC /AM-IF-Gain
0 0 0 0 0.14
1 0 0 0
0 1 0 0
1 1 0 0
0 0 1 0
1 0 1 0
0 1 1 0
1 1 1 0
0 0 0 1
1 0 0 1
0 1 0 1
1 1 0 1
0 0 1 1
1 0 1 1
0 1 1 1
1 1 1 1 2.2
Null Voltage
0 0 0 0 0 0.87
1 0 0 0 0
0 1 0 0 0
1 1 0 0 0
0 0 1 0 0
1 0 1 0 0
0 1 1 0 0
1 0 0 1 1
0 1 0 1 1
1 1 0 1 1
0 0 1 1 1
1 0 1 1 1
0 1 1 1 1
1 1 1 1 1 1.8
Vref 2.7V ADJ
0 0 Low
1 0 Typ
0 1 Little High
1 1 High
Mute-ATT-SW/AM-Vsm-Shift
0 0 Low(Steep inclination)
1 0
0 1
1 1 High(Gentle inclination)
FM/AM N-AGC Sensitivity
0 0 0 0 0.2
1 0 0 0
0 1 0 0
1 1 0 0
0 0 1 0
1 0 1 0
0 1 1 0
1 1 1 0
0 0 0 1
1 0 0 1
0 1 0 1
1 1 0 1
0 0 1 1
1 0 1 1
0 1 1 1
1 1 1 1 2.5
SD detection band width setting (at FM-SEEK)
Band variable filter start point setting
(FM reception)
0 0 0 0 0.54
1 0 0 0
0 1 0 0
1 1 0 0
0 0 1 0
1 0 1 0
0 1 1 0
1 1 1 0
0 0 0 1
1 0 0 1
0 1 0 1
1 1 0 1
0 0 1 1
1 0 1 1
0 1 1 1
1 1 1 1 2.19
QD P-ADJ
0 0 0 0 0.83
1 0 0 0
0 1 0 0
1 1 0 0
0 0 1 0
1 0 1 0
0 1 1 0
1 1 1 0
0 0 0 1
1 0 0 1
0 1 0 1
1 1 0 1
0 0 1 1
1 0 1 1
0 1 1 1
1 1 1 1 1.39


IN3-4 tuner setting2
Address 69h, Subaddress[0 1 1]
B0 B1 B2 B3 A0 A1 A2 A3
1 0 0 1 0 1 1 0
Address Code
0 1 1
Sub Address Code
Pi-Can
(Pilot Cancel Level Control)
0 0 Center (AM-NC=OFF)
1 0 Low (same as above)
0 1 High (same as above)
1 1 OFF (AM-NC=ON)
Noise-AGC
0 No Limit
1 Limit
D34-0 D34-1 D34-2 D34-3 D34-4 D34-5 D34-6 D34-7 D34-8 D34-9 D34-10 D34-11 D34-12 D34-13 D34-14 D34-15 D34-16 D34-17 D34-18 D34-19 D34-20 D34-21 D34-22 D34-23 D34-24 D34-25 D34-26 D34-27 D34-28 D34-29 D34-30 D34-31
Initial data at power ON
L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L
(46) (47) (48) (49) (50) (51) (52) (53) (54) (55) (56) (57) (65)
SNC DAC/(AM-RF-AGC)
Amp threshold
(gentle inclination side)
0 0 0 0 0 0.07(1.35)
(1 0 0 0 0
0 1 0 0 0
1 1 0 0 0
0 0 1 0 0
1 0 1 0 0
0 1 1 0 0
1 1 1 0 0
0 1 0 1 1
1 1 0 1 1
0 0 1 1 1
1 0 1 1 1
0 1 1 1 1
1 1 1 1 1 1.15(2.46)
SNC inclination
0 0
1 0
0 1
1 1
De-emphasis
0 50µs
1 75µs
Force MONO
0 Normal
1 Forced MONO
NC-forced AGC
application point
changeover
0 For AM
1 For FM
AC-S meter load
changeover
0 Hi
1 Low
Noise-Sens setting
0 0 Easy to detect
1 0
0 1
1 1 Difficult to detect
Separation control
0 0 0 0 0 0 L-R Level Max.
1 0 0 0 0 0
0 1 0 0 0 0
1 1 0 0 0 0
0 0 1 0 0 0
1 0 1 0 0 0
0 1 1 0 0 0
1 1 1 0 0 0
0 1 0 1 1 1
1 1 0 1 1 1
0 0 1 1 1 1
1 0 1 1 1 1
0 1 1 1 1 1
1 1 1 1 1 1 L-R Level Min.
FM/AM
HCC DAC.
0 0 0 0 0 0.5
1 0 0 0 0
0 1 0 0 0
1 1 0 0 0
0 0 1 0 0
1 0 1 0 0
0 1 1 0 0
1 1 1 0 0
0 1 0 1 1
1 1 0 1 1
0 0 1 1 1
1 0 1 1 1
0 1 1 1 1
1 1 1 1 1 1.5
Noise-AGC
Threshold voltage forced application
0 OFF(Normal)
1 ON(controlled with SD-ADJ-DAC)

IN3-5 tuner setting2
Address 69h, Subaddress[1 0 0]

B0	B1	B2	B3	A0	A1	A2	A3

1	0	0	1	0	1	1	0

Address Code

1	0	0

Sub Address Code

	D35-0	D35-1	D35-2	D35-3	D35-4	D35-5	D35-6	D35-7	D35-8	D35-9	D35-10	D35-11	D35-12	D35-13	D35-14	D35-15	D35-16	D35-17	D35-18	D35-19	D35-20	D35-21	D35-22	D35-23	D35-24	D35-25	D35-26	D35-27	D35-28	D35-29	D35-30	D35-31
Initial data at power ON	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	(58)						(59)	(60)	(61)			(62)														(63)		(64)		(65)		

VCO ON
During
measurement: Hi

HCC SW
1 FM
0 AM

MRC
Sensitivity
0 0 Low
1 0 ↓
0 1 ↓
1 1 High

MRC Time constant
(Attack: Release Time)
0 0 Short
1 0
0 1
1 1 Long

MPX VCO
(Free-Run Freq. Control)
0 0 0 0 0 0 Freq=Low
1 0 0 0 0 0 ↓
0 1 0 0 0 0 ↓
1 1 0 0 0 0 ↓
0 0 1 0 0 0 ↓
1 0 1 0 0 0 ↓
0 1 1 0 0 0 ↓
1 1 1 0 0 0 ↓
• →
• →
0 1 0 1 1 1 ↓
1 1 0 1 1 1 ↓
0 0 1 1 1 1 ↓
1 0 1 1 1 1 ↓
0 1 1 1 1 1 ↓
1 1 1 1 1 Freq=High

"Filter-Wide fixed"
sensitivity/AM-RF-AGC
Amp threshold
(steep inclination side)
0 0 0 0 0.37
1 0 0 0
0 1 0 0
1 1 0 0
0 0 1 0
1 0 1 0
0 1 1 0
1 1 1 0
0 0 0 1
1 0 0 1
0 1 0 1
1 1 0 1
0 0 1 1
1 0 1 1
0 1 1 1
1 1 1 1 2.04

Filter-initial adjustment

D12-14	Gain	Gain adjustment
D15-19	CF	CF adjustment
D20-24	BW/G	BW/G adjustment

"Gain adjustment"
D12 13D D14
1 1 1 Gain Low
0 1 1
1 0 1
0 0 0 Typical
1 0 0
0 1 0
1 1 0 Gain High

"CF adjustment"
D15 • • • D19.
1 1 1 1 1 CF Left Shift
0 1 1 1 1
1 0 1 1 1
•
•
0 1 0 0 1
1 0 0 0 1
0 0 0 0 0 Typical
1 0 0 0 0
0 1 0 0 0
•
•
1 0 1 1 0
0 1 1 1 0
1 1 1 1 0 CF Right Shift

"BW/G adjustment"
D20 • • • D24.
1 1 1 1 1 BW(W)G↓
0 1 1 1 1
1 0 1 1 1
•
•
0 1 0 0 1
1 0 0 0 1
0 0 0 0 0 Typical
1 0 0 0 0
0 1 0 0 0
•
•
1 0 1 1 0
0 1 1 1 0
1 1 1 1 0 BW(N)G↑

BIT Control Standard: Reference Value

1. FM S-meter shifter

LSB				MSB	Function
D32-0	D32-1	D32-2	D32-3	D32-4	
0	0	0	0	0	Vsm(DC)=1.85V: +8dB
					↑
0	0	0	0	1	Vsm(DC)=1.85V: 0dB
					↓
1	1	1	1	1	Vsm(DC)=1.85V: -7dB

2-1. FM Mute-ON-adj

LSB				MSB	Function
D32-5	D32-6	D32-7	D32-8	D32-9	
0	0	0	0	0	-3dB Limitting sens: -6dB
					↑
1	1	1	1	0	-3dB Limitting sens: 0dB
					↓
1	1	1	1	1	-3dB Limitting sens: +10dB

2-2. AM NC stop

LSB				MSB	Function
D32-5	D32-6	D32-7	D32-8	D32-9	
0	0	0	0	0	Vsm (DC) for AM NC STOP=0.3V
					↑
0	0	0	0	1	Vsm (DC) for AM NC STOP=2.3V
					↓
1	1	1	1	1	Vsm (DC) for AM NC STOP=4.2V

3-1. FM Mute-ATT

LSB					MSB	Function
D32-10	D32-11	D32-12	D32-13	D32-14	D32-15	
0	0	0	0	0	0	MUTE attenuation: -0.5dB
						↑
0	0	0	0	0	1	MUTE attenuation: -13dB
						↓
1	1	1	1	1	1	MUTE attenuation: -25dB

3-2. AM NC Gate-Time

LSB					MSB	Function
D32-10	D32-11	D32-12	D32-13	D32-14	D32-15	
0	0	0	0	0	0	INPUT=60dBμV: 1000μs
						↑
0	0	0	0	0	1	INPUT=60dBμV: 350μs
						↓
1	1	1	1	1	1	INPUT=60dBμV: 200μs

4. FM weak input Mute changeover
(FM Mute-ON-adj:0000)

LSB		MSB	Function
D32-16	D32-17	D32-18	
0	0	0	INPUT=-20dBμV V42: 1.45V
			↑
1	1	0	INPUT=-20dBμV V42: 2.0V
			↓
1	1	1	INPUT=-20dBμV V42: 2.7V

5-1. FM SD Adjust

LSB				MSB	Function
D32-19	D32-20	D32-21	D32-22	D32-23	
0	0	0	0	0	SD on level: -19dB
					↑
0	0	0	0	1	SD on level: 0dB
					↓
1	1	1	1	1	SD on level: +20dB

5-2. AM SD Adjust

LSB				MSB	Function
D32-19	D32-20	D32-21	D32-22	D32-23	
0	0	0	0	0	SD on level: -13dB
					↑
0	0	0	0	1	SD on level: 0dB
					↓
1	1	1	1	1	SD on level: +25dB

6-1. FM IF-Gain

LSB			MSB	Function
D32-24	D32-25	D32-26	D32-27	
0	0	0	0	450kHz limit AMP: -6dB
				↑
0	0	0	1	450kHz limit AMP: 0dB
				↓
1	1	1	1	450kHz limit AMP: +6dB

7-1. FM W-AGC

LSB			MSB	Function
D33-0	D33-1	D33-2	D33-3	
0	0	0	0	W-AGC on level: -2dB
				↑
0	0	0	1	W-AGC on level: 0dB
				↓
1	1	1	1	W-AGC on level: +2dB

7-2. AM W-AGC

LSB			MSB	Function
D33-0	D33-1	D33-2	D33-3	
0	0	0	0	N-AGC on level: -9.5dB
				↑
0	0	0	1	N-AGC on level: 0dB
				↓
1	1	1	1	W-AGC on level: +6dB

8-1. FM N-AGC

LSB			MSB	Function
D33-4	D33-5	D33-6	D33-7	
0	0	0	0	N-AGC on level: -9dB
				↑
0	0	0	1	N-AGC on level: 0dB
				↓
1	1	1	1	N-AGC on level: +6dB

8-2. AM N-AGC

LSB			MSB	Function
D33-4	D33-5	D33-6	D33-7	
0	0	0	0	N-AGC on level: -10dB
				↑
0	0	0	1	N-AGC on level: 0dB
				↓
1	1	1	1	N-AGC on level: +6.5dB

9-1. FM Keyed-AGC

LSB			MSB	Function
D33-8	D33-9	D33-10	D33-11	
0	0	0	0	V38 for Keyed AGC ON: 0.12V
				↑
0	0	0	1	V38 for Keyed AGC ON: 1.2V
				↓
1	1	1	1	V38 for Keyed AGC ON: 2.1V

9-2. AM IF-Gain

LSB			MSB	Function
D33-8	D33-9	D33-10	D33-11	
0	0	0	0	AM 450kHz AMP Gain: -7.5dB
				↑
0	0	0	1	AM 450kHz AMP Gain: 0dB
				↓
1	1	1	1	AM 450kHz AMP Gain: -4.5dB

10-1. FM Mute-ATT-SW

LSB	MSB	Function
D33-25	D33-26	
0	0	MUTE attenuation at V42=1V: -6dB
1	0	MUTE attenuation at V42=1V: -8dB
0	1	MUTE attenuation at V42=1V: -13dB
1	1	MUTE attenuation at V42=1V: -19dB

10-2. AM Vsm-shifter

LSB	MSB	Function
D33-25	D33-26	
0	0	Vsm(DC)=1.5V ANT IN: 30dBμV
1	0	Vsm(DC)=1.5V ANT IN: 38dBμV
0	1	Vsm(DC)=1.5V ANT IN: 45dBμV
1	1	Vsm(DC)=1.5V ANT IN: 55dBμV

11-1. FM SNC DAC

LSB				MSB	Function
D34-6	D34-7	D34-8	D34-9	D34-10	
0	0	0	0	0	SEPARATION=15dB INPUT: -26dB
0	0	0	1	0	SEPARATION=15dB INPUT: -6dB
0	0	0	0	1	SEPARATION=15dB INPUT: 0dB
0	0	0	1	1	SEPARATION=15dB INPUT: +5dB
1	1	1	1	1	SEPARATION=15dB INPUT: +11dB

12-1. FM HCC DAC

LSB				MSB	Function
D34-11	D34-12	D34-13	D34-14	D34-15	
0	0	0	0	0	V29 at 10kHz mod, -6dB: 0.4V
					↑
0	0	0	0	1	V29 at 10kHz mod, -6dB: 0.85V
					↓
1	1	1	1	1	V29 at 10kHz mod, -6dB: 1.3V

12-2. AM HCC DAC

LSB				MSB	Function
D34-11	D34-12	D34-13	D34-14	D34-15	
0	0	0	0	0	V29 at 4kHz mod, -6dB: 0.04V
					↑
0	0	0	0	1	V29 at 4kHz mod, -6dB: 0.82V
					↓
1	1	1	1	1	V29 at 4kHz mod, -6dB: 1.3V

13-1. MRC Time constant

LSB	MSB	Function
D35-27	D35-28	
0	0	Pin 39 output current: 2.9μA
1	0	Pin 39 output current: 2.2μA
0	1	Pin 39 output current: 1.5μA
1	1	Pin 39 output current: 0.8μA

Description Of Control Data

<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data
P0 to P15</td><td>¤ Data to set the dividing ratio of the programmable divider.
Binary value with P0 as LSB and P15 as MSB</td><td>AM/FM
OSC D1,D2</td></tr>
<tr><td>(2)</td><td>AM OSC dividing ratio

OSC D1,OSC D2</td><td>¤ OSC dividing ratio determination for AM OSC D1 and OSC D2
<table>
<tr><th>OSC D1</th><th>OSC D2</th><th>Dividing ratio</th></tr>
<tr><td>0</td><td>0</td><td>10-division</td></tr>
<tr><td>0</td><td>1</td><td>8-division</td></tr>
<tr><td>1</td><td>0</td><td>6-division</td></tr>
<tr><td>1</td><td>1</td><td>4-division</td></tr>
</table></td><td>AM/FM
P0 to P15</td></tr>
<tr><td>(3)</td><td>General-purpose counter measurement start control

CTE</td><td>¤ General-purpose counter measurement start data

CTE =1: Count start
=0: Count reset</td><td>CTS
GT0,GT1
CTP
CTC</td></tr>
<tr><td>(4)</td><td>Reference divider data

R0 to R3</td><td>¤ Reference frequency (fref) selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency (kHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Do not use</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>100</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Do not use</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Do not use</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Do not use</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Do not use</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Do not use</td></tr>
</table></td><td></td></tr>
<tr><td>(5)</td><td>Stop of programmable divider

DVS</td><td>¤ DVS=0: PLL-IN pin in IC stopped (pulled-down)
1: PLL-IN pin in IC selected
Set number of divisions (N): 272 to 65536
Input frequency range: 120 to 270MHz
* For details, refer to “Programmable Divider Composition.”</td><td>CTS
GT0,GT1
CTP
CTC</td></tr>
<tr><td>(6)</td><td>Tuner mode changeover
AM/FM</td><td>¤ AM/FM mode changeover
1=AM 0=FM</td><td>P0 to P15
OSC D1,D2</td></tr>
<tr><td>(7)</td><td>Tuner mode changeover

SEEK1, SEEK2</td><td>¤ Data to determine the mode of tuner
<table>
<tr><th>SEEK1</th><th>SEEK2</th><th>IF buffer control output</th></tr>
<tr><td>0</td><td>0</td><td>Do not use</td></tr>
<tr><td>1</td><td>0</td><td>STOP</td></tr>
<tr><td>0</td><td>1</td><td>RDS</td></tr>
<tr><td>1</td><td>1</td><td>SEEK</td></tr>
</table></td><td>MODE1,
MODE2</td></tr>
</table>

Continued on next page.

Continued from preceding page.

<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(8)</td><td>PLL filter changeover

MODE1,MODE2</td><td>¤ Data to select/changeover the PLL filter * don't care
<table>
<tr><th>MODE1</th><th>MODE2</th><th>AM/FM</th><th>SEEK1</th><th>SEEK2</th><th>AM filter</th><th>FM filter</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>*</td><td>*</td><td>OFF</td><td>ON</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>*</td><td>*</td><td>ON</td><td>OFF</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>OFF</td><td>ON</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>OFF</td><td>ON</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>ON</td><td>OFF</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>*</td><td>*</td><td>ON</td><td>OFF</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>OFF</td><td>ON</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>OFF</td><td>ON</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>ON</td><td>ON</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>*</td><td>*</td><td>ON</td><td>ON</td></tr>
</table></td><td>AM/FM
SEEK1,
SEEK2</td></tr>
<tr><td>(9)</td><td>OSC dividing ratio control

WEATHER
DIV_SW3</td><td>¤ Data to set the OSC dividing ratio at reception of AM/FM/WB
<table>
<tr><th>WEATHER</th><th>DIV_SW3</th><th>Dividing ratio</th></tr>
<tr><td>0</td><td>0</td><td>2-division</td></tr>
<tr><td>0</td><td>1</td><td>3-division</td></tr>
<tr><td>1</td><td>0</td><td>1-division</td></tr>
<tr><td>1</td><td>1</td><td>1-division</td></tr>
</table></td><td>AM/FM
P0 to P15
OSC D1,
OSC D2</td></tr>
<tr><td>(10)</td><td>IC internal signal I/O port
Control data</td><td>Data to designate I/O of the I/O port
"Data" =0: input port Select "0" normally.
=1: output port Select "1" for IC test
* Select "0" for cases other than IC test.</td><td></td></tr>
<tr><td>(11)</td><td>X-TAL OSC
Fine adjustment data</td><td>Data to detune the reference frequency X'tal=20.5MHz when beat has occurred
Variable by about 100Hz per bit in eight steps of 0 to 7 bits
X'tal to be loaded with the external capacity at the 3-bit (110) setting
<table>
<tr><th>X'tal OSC ADJ</th><th></th></tr>
<tr><td>0 0 0</td><td>+390Hz</td></tr>
<tr><td>1 0 0</td><td>+250Hz</td></tr>
<tr><td>0 1 0</td><td>+110Hz</td></tr>
<tr><td>1 1 0</td><td>X'tal (center value)</td></tr>
<tr><td>0 0 1</td><td>-100Hz</td></tr>
<tr><td>1 0 1</td><td>-190Hz</td></tr>
<tr><td>0 1 1</td><td>-280Hz</td></tr>
<tr><td>1 1 1</td><td>-350Hz</td></tr>
</table></td><td></td></tr>
<tr><td>(12)</td><td>AMSD speedup

SDSPEED</td><td>Data to speed up the SD rise time in the AM mode
"SDSPEED"=0: NORMAL mode
=1: speedup mode</td><td></td></tr>
<tr><td>(13)</td><td>DO pin
Control data

IL0,IL1</td><td>¤ Data to control the DO pin output
<table>
<tr><th>IL1</th><th>Il0</th><th>IN</th></tr>
<tr><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>SD pin state (PIN13)</td></tr>
<tr><td>1</td><td>0</td><td>Pin I2 state (not used)</td></tr>
<tr><td>1</td><td>1</td><td>Do not use</td></tr>
</table>
Open when I/O-1 and I/O-2 pins are designated as output ports.
Note) Do not use with X'tal OSC STOP (DO does not change)</td><td></td></tr>
<tr><td>(14)</td><td>AM/FM-AGC ON
Control data

FMAGC_ON
AMAGC_ON</td><td>Data to make AGC of each of AM and FM effective
"FMAGC_ON"=0: NORMAL mode
=1: Forced ON mode } For FM
"AMAGC_ON"=0: NORMAL mode
=1: Forced ON mode } For AM</td><td></td></tr>
<tr><td>(15)</td><td>IF count sensitivity
deterioration control data
CTC</td><td>¤ Decrease the input sensitivity with CTC=1.
* Do not attempt change of bits during count (except for EVR).</td><td></td></tr>
</table>

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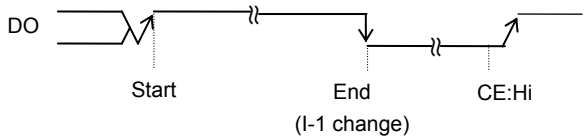
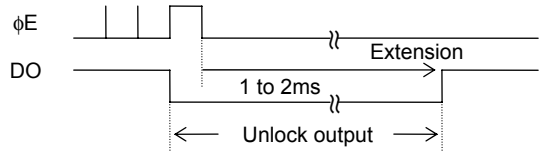
<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(16)</td><td>General-purpose counter Control data

GT0, GT1
CTP</td><td>¤ Data to determine the general-purpose counter measurement time (frequency mode) and number of cycles (cycle mode).
<table>
<tr><th rowspan="2">GT1</th><th rowspan="2">GT0</th><th colspan="3">Frequency measurement</th><th rowspan="2">Cycle measurement mode</th></tr>
<tr><th>Measurement time</th><th colspan="2">Wait time</th></tr>
<tr><th></th><th></th><th></th><th>CTP=0</th><th>CTP=1</th><th></th></tr>
<tr><td>0</td><td>0</td><td>4ms</td><td>3 to 4ms</td><td>1 to 2ms</td><td>1 cycle</td></tr>
<tr><td>0</td><td>1</td><td>8ms</td><td>3 to 4ms</td><td>1 to 2ms</td><td>1 cycle</td></tr>
<tr><td>1</td><td>0</td><td>32ms</td><td>7 to 8ms</td><td>1 to 2ms</td><td>2 cycles</td></tr>
<tr><td>1</td><td>1</td><td>64ms</td><td>7 to 8ms</td><td>1 to 2ms</td><td>2 cycles</td></tr>
</table>
¤ CTP=0: General-purpose counter input stopped at counter reset (CTE=0)
=1: General-purpose counter input not stopped and the wait time shortened at counter reset (CTE=0)
Except that Immediately after setting of CTP=1, it is necessary to wait for counter start till the general-purpose counter input pin is biased.</td><td></td></tr>
<tr><td>(17)</td><td>DO pin control data

ULD
DT0, DT1</td><td>¤ Data to determine the output of DO pin.
<table>
<tr><th>ULD</th><th>DT1</th><th>DT0</th><th>DO pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Low when unlocked</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Do not use</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>IN (*1)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Do not use</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>end-UC</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>IN (*1)</td></tr>
</table>
end-UC: Count over of the general-purpose counter

</td><td></td></tr>
<tr><td>(18)</td><td>Unlock detection data

UL0, UL1</td><td>¤ Data to select the phase error (ϕE) detection width in order to check PLL for locking. Phase error exceeding the ϕE detection width shown in the table below is determined to indicate unlock. At unlock, the detection pin (DO) becomes Low.
<table>
<tr><th>UL1</th><th>UL0</th><th>ϕE detection width</th><th>Detection pin output</th></tr>
<tr><td>0</td><td>0</td><td>Stop</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ϕE output directly</td></tr>
<tr><td>1</td><td>0</td><td>±0.5μs</td><td>ϕE extended by 1 to 2ms</td></tr>
<tr><td>1</td><td>1</td><td>±1μs</td><td>ϕE extended by 1 to 2ms</td></tr>
</table>

</td><td>ULD
DT0, DT1</td></tr>
<tr><td>(19)</td><td>IF count operation control data
CTS</td><td>¤ Data to select the general-purpose counter input pin (HCTR) in IC
CTS=1: HSTR pin in IC selected
0: HCTR pin in IC pulled down</td><td></td></tr>
<tr><td>(20)</td><td>Sub-charge pump control data

PDC0, PDC1</td><td>¤ Data to control the sub-charge pump
<table>
<tr><th>PDC1</th><th>PDC0</th><th>Sub-charge pump state</th></tr>
<tr><td>0</td><td>*</td><td>High impedance</td></tr>
<tr><td>1</td><td>0</td><td>Charge pump operating (unlocked)</td></tr>
<tr><td>1</td><td>1</td><td>Charge pump operating (normal)</td></tr>
</table>
(*: don't care)
* The sub-charge pump output is connected internally with the LPF FET gate. The sub-charge pump and the PD (main charge pump) pin are combined to form the fast lockup circuit.
* Except that this may not be effective depending on the filter multiplier (lighter filter).</td><td>UL0, UL1, DLC</td></tr>
</table>

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<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(21)</td><td>Phase comparator control data

DZ0, DZ1</td><td>¤ Data to control the dead band of phase comparator
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Deadban mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
* DZA at power ON and power reset</td><td></td></tr>
<tr><td>(22)</td><td>Charge pump control data

DLC</td><td>¤ Data to set the charge pump output to the low level (V_{SS} level) in a forced manner.
DLC=1: Low level
=0: Normal operation
* When the VCO control voltage (Vtune) is deadlocked because VCO stops oscillation at 0V, this data sets the charge pump output to the low level and Vtune to V_{CC}, enabling escape from the deadlock state. Normal operation mode at power ON and power reset</td><td></td></tr>
<tr><td>(23)</td><td>IC test data

TEST0
TEST1
TEST2</td><td>¤ IC test data
Set as follows:
TEST0=0
TEST1=0
TEST2=0
* All of test data is set to “0” at power ON and power reset.</td><td></td></tr>
<tr><td>(24)</td><td>RF-DAC control
D31-0 to D31-8</td><td>¤ Causes application of the control voltage to the RF tuning circuit (varactor).
9BIT</td><td></td></tr>
<tr><td>(25)</td><td>Internal monitor changeover data
D31-9</td><td>¤ Data to changeover the internal monitor.
1BIT</td><td></td></tr>
<tr><td>(26)</td><td>ANT-DAC control
D31-10 to D31-18</td><td>¤ Causes application of the control voltage to the ANT tuning circuit (varactor).
9BIT</td><td></td></tr>
<tr><td>(27)</td><td>MSLOP Control changeover data
D31-19</td><td>¤ Data to change over the FM MUTE curve inclination.
1BIT MSLOP
0 Mute_D (steep inclination)
1 Mute_D (gentle inclination)</td><td></td></tr>
<tr><td>(28)</td><td>Band variable filter control data
D31-20 to D31-25</td><td>¤ Narrow/wide band - (MIN/MAX) data to set the band variable filter
Each 3bits for narrow and wide bands
Band variable filter
Narrow/wide band MIN/MAC control value
Narrow LMT Cont
D20 D21 D22
0 0 0 Min (40k)
1 0 0
0 1 0
•
•
1 0 1
0 1 1
1 1 1 Max (80k)
Wide LMT Cont
D23 D24 D25
0 0 0 Max (220k)
1 0 0
0 1 0
•
•
1 0 1
0 1 1
1 1 1 Min (150k)</td><td></td></tr>
<tr><td>(29)</td><td>Band variable filter mode setting
D31-26 to D31-27</td><td>¤ Data to set the mode of band variable filter.
2BIT
Filter-Fix_SW
<table>
<tr><th>D26</th><th>D27</th><th>Filter-Mode</th></tr>
<tr><td>0</td><td>0</td><td>Variable</td></tr>
<tr><td>1</td><td>0</td><td>Narrow-Fix</td></tr>
<tr><td>0</td><td>1</td><td>Wide-Fix</td></tr>
<tr><td>1</td><td>1</td><td>Dont Care</td></tr>
</table></td><td></td></tr>
<tr><td>(30)</td><td>DAC TEST select data
D31-29</td><td>¤ Data to select the output circuit of internal DAC circuit</td><td></td></tr>
<tr><td>(31)</td><td>S-meter shifter control
D32-0 to D32-4</td><td>¤ Controls the output value of FM S-METER shifter circuit.
5BIT</td><td></td></tr>
<tr><td>(32)</td><td>FM MUTE-ON-adj/
AM NC stop control
D32-5 to D32-9</td><td>¤ FM: Controls FM MUTE-ON-adj characteristic.
AM: Controls the sensitivity of AM NC stop.
5BIT</td><td></td></tr>
<tr><td>(33)</td><td>FM MUTE-ATT/
AM NC Gate-Time control
D32-10 to D32-15</td><td>¤ FM: Controls FM MUTE-ATT characteristic.
AM: Controls the width of AM NC Gate-Time characteristic.
6BIT</td><td></td></tr>
</table>

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No.	Control block/data	Description	Related data
(34)	Weak input MUTE changeover D31-16 to D31-18	¤ Changes over weak input MUTE. 3BIT	
(35)	AM/FM SD-adj NC-AGC threshold voltage setting data D31-19 to D32-23	¤ Controls SD characteristic of AM/FM. Sets the threshold voltage of NC-AGC. 5BIT	
(36)	FM IF-Gain /AM NC Gain control data D32-24 to D32-27	¤ Controls Gain of FM IF limiter AMP. Controls also Gain of IF limiter AMP in the AM mode similarly to the FM mode. 4BIT	
(37)	TUNER OFF setting data D32-28	¤ Data to set the mode to turn OFF the tuner. 1BIT Tuner OFF mode 0 Normal operation 1 Tuner-OFF	
(38)	AM/FM WAGC setting data D33-0 to D33-3	¤ Data to set the AM/FM WAGC sensitivity. 4BIT	
(39)	AM/FM NAGC setting data D33-4 to D33-7	¤ Data to set the AM/FM NAGC sensitivity. 4BIT	
(40)	Keyed-AGC/ AM-IF-Gain setting data D33-8 to D33-11	¤ Controls FM Keyed-AGC sensitivity. Controls AM-IF-GAIN. 4BIT	
(41)	SD detection bandwidth setting/band variable filter start point setting data D33-12 to D33-15	¤ Used to set the SD detection bandwidth at FM-SEEK. Used to set the start point of band variable filter at FM reception. 4BIT	
(42)	Null Voltage setting data D33-16 to D33-20	¤ Controls the FM Null voltage. 5BIT	
(43)	QDP-ADJ setting data D33-21 to D33-24	¤ Controls the FM QDP voltage. 4BIT	
(44)	FM MUTE-ATT SW/AM S-meter shifter control D33-25 to D33-26	¤ FM: Controls FM MUTE-ATT-SW characteristic. AM: Controls S-meter shifter circuit output value. 2BIT Mute-ATT-SW/AM-Vsm-Shift 0 0 Low (steep inclination) 1 0 0 1 1 1 High (gengle inclination)	
(45)	VREF2.7V adj control D33-27 to D33-28	¤ Sets the Vref2.7V output voltage to the target value. 2BIT Vref2.7V ADJ 0 0 Low 1 0 Typ 0 1 Little High 1 1 High	
(46)	Separation control D34-0 to D34-5	¤ Controls separation of L/R output level in the FM stereo mode. 6BIT	
(47)	FM SNC/ AM-RF-AGC AMP Threshold value (gentle inclination side) setting data D34-6 to D34-10	¤ Sets FM SNC characteristic. Sets AM-RF-AGC AMP (gentle inclination side) threshold voltage. 5BIT	
(48)	FM/AM HCC setting data D34-11 to D34-15	¤ Sets HCC characteristic of FM and AM. 5BIT	
(49)	SNC inclination setting data D34-16 to D34-17	¤ Sets inclination of SNC voltage (sets the separation curve). 2BIT SNC inclination 0 0 1 0 ↓ 0 1 ↓ 1 1	

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<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(50)</td><td>Pilot cancel control
D34-18 to D34-19</td><td>¤ Data to control the pilot cancel degree.
2BIT Pi-Can (Pilot Cancel Level Control)
0 0 Center (AM-NC=OFF)
1 0 Low (same as above)
0 1 High (same as above)
1 1 OFF (AM-NC=ON)</td><td></td></tr>
<tr><td>(51)</td><td>De-emphasis select data
D34-20</td><td>¤ Data to select the De-Emphasis constant of L/R output.
1BIT De-emphasis
0 50μs
1 75μs</td><td></td></tr>
<tr><td>(52)</td><td>Force NOMO setting data
D34-21</td><td>¤ Data to force L/R output to the MONO mode.
1BIT
0 Normal
1 Forced MONO</td><td></td></tr>
<tr><td>(53)</td><td>Noise-AGC
Threshold voltage forced application data
D34-23</td><td>¤ Data to change the sensitivity by applying the Noise-AGC Threshold voltage in a forced manner.
1BIT Noise-AGC
Threshold voltage forced application
0 OFF (Normal)
1 ON(control with SD-ADJ-DAC)</td><td></td></tr>
<tr><td>(54)</td><td>Noise sensitivity setting data
D34-24 to D34-25</td><td>¤ Controls the noise detection sensitivity.
2BIT Noise-Sens setting
0 0 Easy to detect
1 0 ↓
0 1 ↓
1 1 Difficult to detect</td><td></td></tr>
<tr><td>(55)</td><td>AC S-meter
Load changeover data
D34-26</td><td>¤ S-meter output (Vsm2_sub):
Data to change over the output impedance (internal load resistance) of pin 40
1BIT AC-S meter load changeover
0 Hi (7kΩ)
1 Low (3.5kΩ)</td><td></td></tr>
<tr><td>(56)</td><td>Noise-AGC limit setting data
D34-27</td><td>¤ Data to changeover the AGC limiter of noise canceller.
1BIT Noise-AGC
0 No Limit (AGC easy to be effective)
1 Limit (AGC difficult to be effective)</td><td></td></tr>
<tr><td>(57)</td><td>D34-28</td><td>¤ No function
1BIT
0 0 : Normal setting
1</td><td></td></tr>
<tr><td>(58)</td><td>MPX VCO control data
D35-0 to D35-5</td><td>¤ Data for control to the MPX-VCO block free-run oscillation frequency of 304kHz
6BIT</td><td></td></tr>
<tr><td>(59)</td><td>VCO ON measurement bit
D35-6</td><td>¤ MPX-VCO block free-run oscillation frequency
During measurement: High
1BIT</td><td></td></tr>
<tr><td>(60)</td><td>HCC SW changeover bit
D35-6</td><td>¤ Data to change the HCC function AM/FM mode
1BIT HCC SW
1 FM
0 AM</td><td></td></tr>
<tr><td>(61)</td><td>Filter-Wide fixed sensitivity/ AM-RF-AGC AMP Threshold value (steep inclination side) setting data
D35-8 to D35-11</td><td>¤ Sets the Filter-Wide fixed sensitivity.
Sets the AM-RF-AGC AMP (steep inclination side) threshold voltage.
4BIT</td><td></td></tr>
<tr><td>(62)</td><td>Filter initial adjustment bit
D35-12 to D35-24</td><td>¤ Data for various initial settings of the filter
13BIT
D12-14 | Gain | Gain adjustment
D15-19 | CF | CF adjustment
D20-24 | BW/G | BW/G adjustment</td><td></td></tr>
</table>

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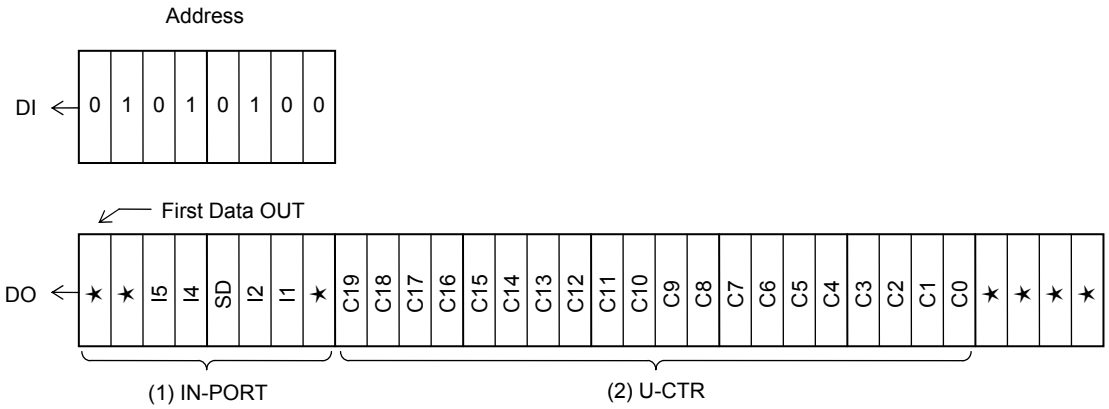
No.	Control block/data	Description	Related data
(63)	MRC Sensitivity Setting data D35-25 to D35-26	¤ Data for sensitivity setting of MRC 2BIT MRC sensitivity 0 0 Low 1 0 ↓ 0 1 ↓ 1 1 High	
(64)	MRC Time constant setting data D35-27 to D35-28	¤ MRC time constant (Attack/Release Time) setting data 2BIT MRC time constant (Attack: Release Time) 0 0 Short 1 0 0 1 1 1 Long	
(65)	D31-29 to D31-31 D32-29 to D32-31 D33-29 to D33-31 D34-29 to D34-31	¤ Sub-Code Address Each 3 bits	

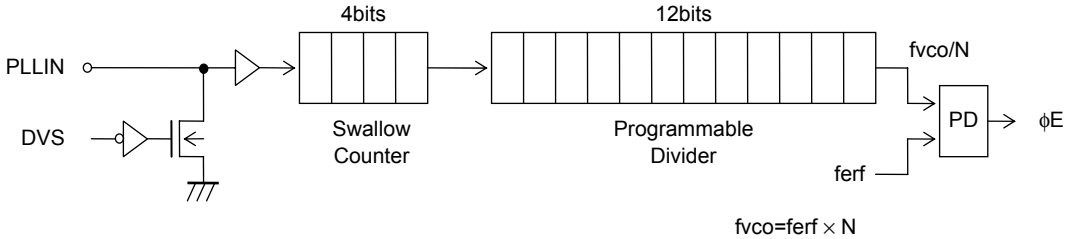
DO Output Data (Serial Data Output) Composition

[3] OUT



No.	Control block/data	Description	Related data
(1)	I/O port data I5 to I1	¤ I/O port; Data latching the state of pin 14 and other pins become I1 to I5. Latched when the data output mode becomes effective. Pin state=Hi: 1 =Low: 0 Currently, only pin 14 (SD state)	TEST-BIT (I/O-PORT)
(2)	General-purpose counter binary data C19 to C0	¤ Data latching the content of general-purpose counter (20-bit binary counter) becomes C19 to C0. C19 ← MSB of binary counter C0 ← LSB of binary counter	CTS0 CTS1 CTE

Programmable Divider Composition



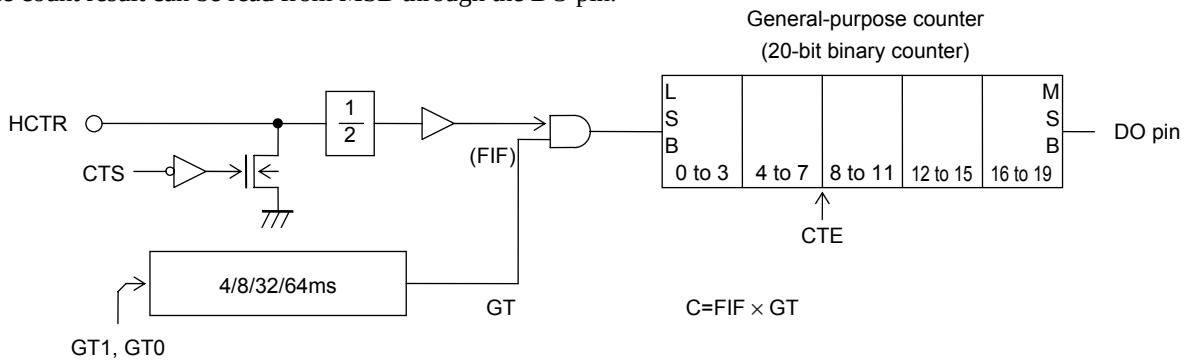
fvco=ferf × N

DVS	Set number of divisions (N)	Input frequency range (f [MHz])	PULL-IN pin in IC
1	272 to 65535	120 ≤ f ≤ 270	Selected
0	-	-	Stopped

* The input sensitivity is not shown here because the IC inside is closed.

Composition of The General-Purpose Counter

The general-purpose counter consists of 20-bit binary counters.
The count result can be read from MSB through the DO pin.



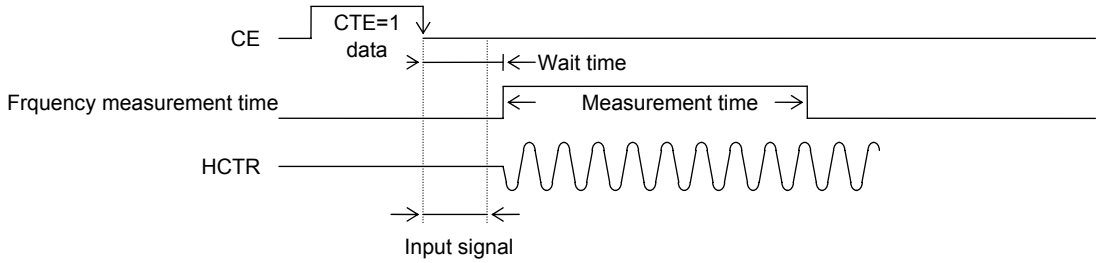
On the basis of GT0 and GT1 data, the measurement time for frequency measurement using the general-purpose counter can be selected from four types: 4,8,32,64 ms. By determining how many pulses are entered in the general-purpose counter within one of these periods, the frequency of signal entered in HCTR in IC can be determined.

CTP data: Data to determine the general-purpose counter input pin (HCTR) state at reset of this counter (CTE=0)
CTP = 0: General-purpose counter input pin turned OFF (pulled down)
= 1: General-purpose counter input pin not pulled down, but the wait time reduced to 1- 2 ms.
When setting CTP=1, it must be set first not later than 4 ms before count start (CTE=1).
When the counter is not to be used, set CTP=0.

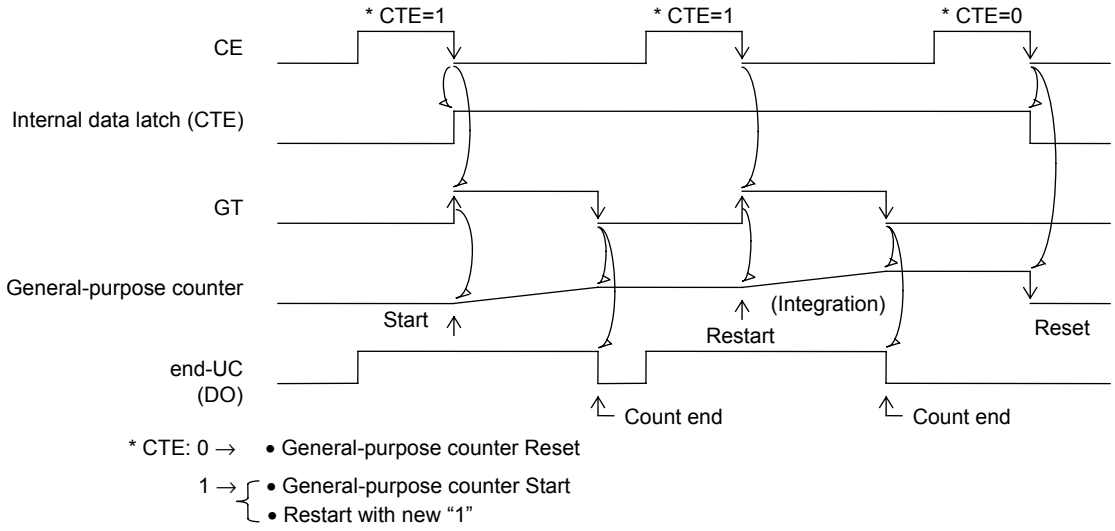
GT1	GT0	Frequency measurement mode		
		Measurement time	Wait time	
			CTP=0	CTP=1
0	0	4ms	3 to 4ms	1 to 2ms
0	1	8ms	7 to 8ms	
1	0	32ms		
1	1	64ms		

IF Counter Operation

Before count start with the general-purpose counter, set CTE=0 to reset the counter beforehand.
The general-purpose counter starts counting by setting the serial data to CTE=1.
Then, the count result of the counter must be read out while CTE=1.
(With CTE=0, the general-purpose counter is reset.)
The signal entered in the HCTR pin in IC is divided into one half internally, and transmitted to the general-purpose counter.
Accordingly, the count result of general-purpose counter is the one-half value of the actual frequency entered in the HCTR pin in IC.



For the integrating counter



During integrating counting, the counts are accumulated in the general-purpose counter.
Take care not to allow overflow of the counter.
Count value: O_H to $FFFFF_H$ (1,048,575)
When the serial data (IN1) is re-transmitted while keeping CTE=1, the general-purpose counter restarts measurement and the integrating count results are added.

Phase Comparator/Charge Pump

(1) Phase comparator/charge pump operation

In the PLL circuit block shown in Fig. 1, the phase comparator compares the phase difference of the reference frequency(fr) and comparative frequency (fp) and outputs the phase difference components from the charge pump.

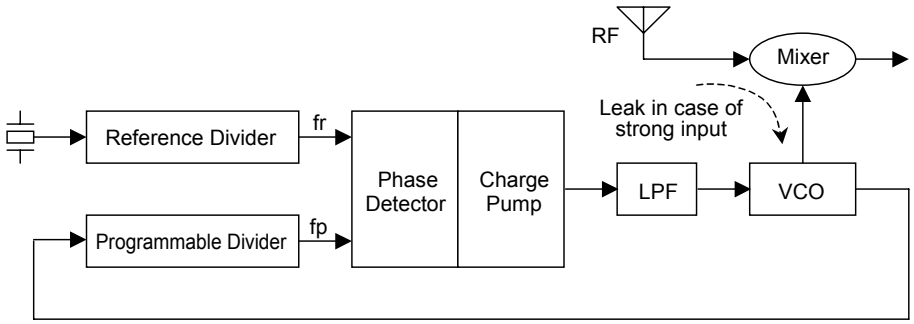
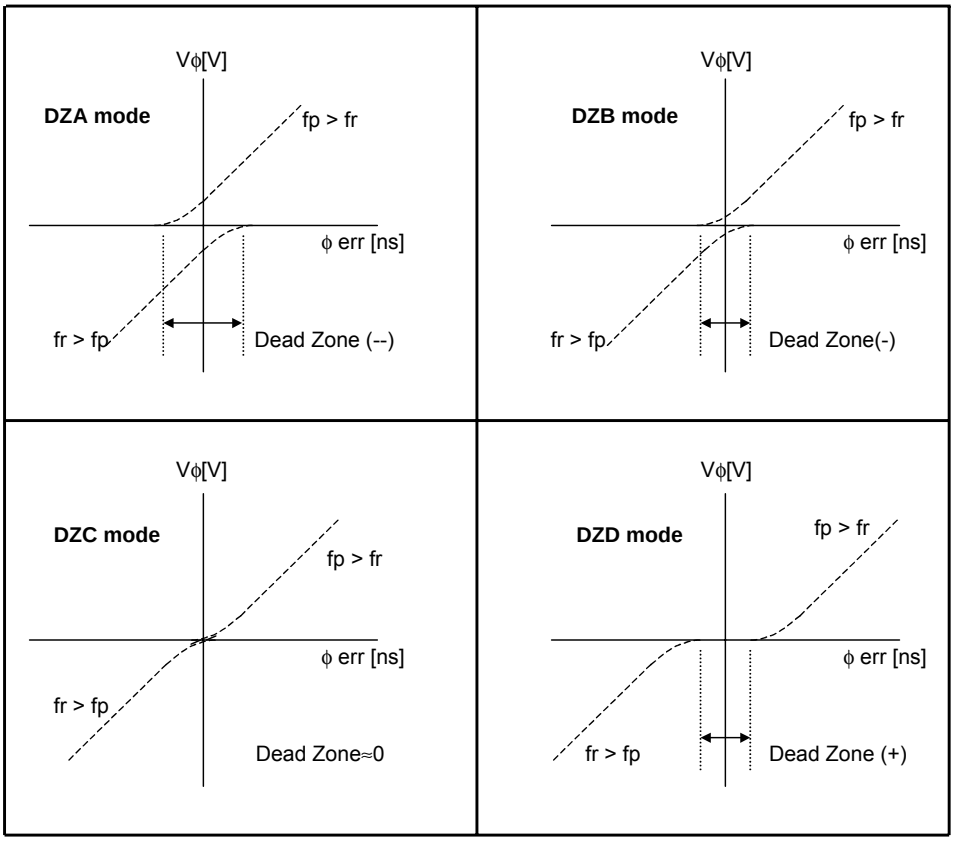


Fig. 1 PLL circuit block

Output characteristics of the phase comparator/charge pump are shown in Fig. 2.
The phase comparator outputs the output Vϕ that is proportional to the phase differenceϕ between fr and fp. By changing the setting of phase comparator dead zone mode, characteristics of phase comparator can be changed. Namely, the modes (DZA, DZB) to turn ON both P-CH and N-CH transistors of charge pump in case of extremely small phase difference and the mode (DZD) not to output the phase difference output in case of extremely small phase difference can be set.

Fig. 2 Phase comparator/charge pump characteristics



(2) Characteristics of the Dead Zone mode

The table below outlines characteristics in each dead zone mode.

Set data		Dead zone mode	Charge pump at phase difference 0 (Pch/Nch)	Dead zone width (Reference data)	Remarks
DZ1	DZ0				
0	0	DZA	ON/ON	-- (-15[ns])	
0	1	DZB	ON/ON	- (-8[ns])	
1	0	DZC	ON or OFF	≈0 (0[ns])	Do not use
1	1	DZD	OFF/OFF	+ (+8[ns])	

(3) Guideline and cautions for selecting the Dead Zone mode

Features of each Dead Zone mode and criteria for selection are described below:

1) DZA mode

In the DZA mode, the correction signal is output from the charge pump even when the phase difference agrees between the reference frequency (fr) and comparative frequency (fp), which is advantageous in obtaining the high S/N ratio with ease. On the other hand, the side band of reference frequency component may occur, readily causing beats in case of strong input. This is a phenomenon occurring because the PLL loop reacts sensitively due to leak components through the mixer, modulating VCO. Occurrence of side band of reference frequency component in the local oscillator also causes leakage of reference components to IF, which tends to worsen the interference characteristics.

2) DZB mode

The DZB mode is characterized by the reduced voltage of correction signal from the DZA mode though, similarly to the case of the DZA mode, the charge pump outputs the correction signal even when the phase difference agrees between the reference frequency (fr) and comparative frequency (fp). This mode features in easier achievement of high S/N ratio than DZC/DZD and improved beat and interference resistances.

3) DZC mode

In the DZC mode, the correction signal is output from the charge pump according to the phase difference between the reference frequency (fr) and comparative frequency (fp). Extremely small noise may occur when the phase difference is around 0 [ns]. Do not use this mode at low temperature (-30°C or less) because the S/N ratio may be deteriorated.

4) DZD mode

In the DZD mode, the correction signal is output from the charge pump according to the phase difference between the reference frequency (fr) and comparative frequency (fp). The correction signal is not output when the phase difference is ± several [ns]. Accordingly, the S/N ratio becomes lower than other dead-zone modes, but beat and interference resistances can be improved.