Ordering number : ENA0654

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA75520KVA — IF Signal Processing (VIF+SIF) IC that Supports the PAL Video Standard for TV Sets and VCRs

Overview

The LA75520KVA is a fully adjustment-free VIF + SIF signal processing IC for TV sets and VTRs that supports the PAL video standard. It supports 38.0MHz, 38.9MHz, and 39.5MHz as the IF frequencies, as well as PAL sound multi-system (M/N, B/G, I and D/K), and contains an on-chip sound carrier trap. The IC employs a 4MHz frequency (which can be switched to 4.43MHz) as the reference frequency of the adjustment free circuit, and controls the VCO, AFT, and sound filter using an external input signal.

Features

- Internal VCO adjustment free circuit eliminating the need for an external VCO coil.
- Internal sound carrier trap enables easy configuration of PAL sound multi-system at low cost.
- Considerably reduces the number of required peripheral parts.
- Use of digital AFT eliminates a problem of AFT tolerance.
- Package: SSOP24 (225mil)

Functions

- VIF amplifier
- Adjustment-free VCO and PLL detector circuit
- Digital AFT circuit
- RF AGC
- Buzz canceller
- EQAMP
- Internal sound carrier trap
- First SIF detector circuit
- PLL-FM detector circuit

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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}		6	V
Allowable power dissipation	Pd max	Ta ≤ 70°C, Mounted on a substrate.*	640	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a substrate : 76.1×114.3×1.6mm^3, glass epoxy board.

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5.0	V
Operating supply voltage	V_{CC} op		4.5 to 5.5	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5.0V, fp = 38.9MHz

Parameter	Symbol	Conditions	No.	Ratings			Unit
				min	typ	max	
VIF block							
Circuit current	I_4		V1	75	85	95	mA
Max RF AGC voltage	$V_{14}H$		V2	4.0	4.5	5.0	V
Min RF AGC voltage	$V_{14}L$		V3	0.0	0.5	1.0	V
Input sensitivity	V_i	Video out 2	V4	26	32	38	dBμV
AGC range	GR		V5	58	63		dB
Max allowable input	V_i max		V6	95	100		dBμV
Quiescent video output voltage	V_5		V7	2.2	2.5	2.8	V
Sync signal edge voltage	V_5 tip		V8	0.8	1.0	1.2	V
Video output level	V_O		V9	1.0	1.2	1.4	Vp-p
Black noise threshold voltage	V_{BTH}		V10	0.5	0.8	1.1	V
Black noise clamp voltage	V_{BCL}		V11	1.2	1.5	1.8	V
Video S/N	S/N	B/G	V12	46	50		dB
C-S best	IC-S	P/S = 10dB	V13	38	43		dB
Differential gain	DG	V_{IN} = 80dBμ	V14		3	6.5	%
Differential phase	DP		V15		3	5	deg
Quiescent AFT voltage	V_{12}	15pin to V_{CC}	V16	2.0	2.5	3.0	V
Max AFT voltage	$V_{12}H$	LOAD 22kΩ/22kΩ	V17	4	4.5	5	V
Min AFT voltage	$V_{12}L$	LOAD 22kΩ/22kΩ	V18	0	0.5	1	V
AFT sensitivity	SF	LOAD 22kΩ/22kΩ	V19	8.5	12.5	16.5	mV/kHz
APC pull-in range (U)	Fpu		V20	2.0	2.4		MHz
APC pull-in range (L)	Fpl		V21		-2.4	-2.0	MHz
VCO control sensitivity	β		V22	3	6	12	kHz/mV
VIF input resistance	R_i	38.9MHz	V23		1.0	1.5	kΩ
VIF input capacity	C_i	38.9MHz	V24		3	6	pF
N trap1 (4.5M)	NT1	wrt 1MHz	V25	-30	-35		dB
N trap2 (4.8M)	NT2	wrt 1MHz	V26	-19	-24		dB
BG trap1 (5.5M)	BT1	wrt 1MHz	V27	-27	-32		dB
BG trap2 (5.85M)	BT2	wrt 1MHz	V28	-20	-25		dB
I trap1 (6.0M)	IT1	wrt 1MHz	V29	-25	-30		dB
I trap2 (6.55M)	IT2	wrt 1MHz	V30	-15	-20		dB
DK trap1 (6.5M)	DT1	wrt 1MHz	V31	-25	-30		dB
Group delay 1 NTSC (3.0M)	NGD1	wrt 1MHz	V32	30	80	145	ns
Group delay 1-1 NTSC (3.5M)	NGD1-1	wrt 1MHz	V33	110	200	290	ns
Group delay 2 BG (4M)	BGD2	wrt 1MHz	V34	50	130	210	ns
Group delay 2-1 BG (4.4M)	BGD2-1	wrt 1MHz	V35	120	200	280	ns
Group delay 3 I (4M)	IGD3	wrt 1MHz	V36	0	80	130	ns

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Parameter	Symbol	Conditions	No.	Ratings			Unit
				min	typ	max	
Group delay 3-1 I (4.4M)	IGD3-1	wrt 1MHz	V37	80	120	160	ns
Group delay 4 DK (4M)	DGD4	wrt 1MHz	V38	10	30	50	ns
Group delay 4-1 DK (4.4M)	DGD4-1	wrt 1MHz	V39	30	60	90	ns
Video f characteristics MN1	VFMN1	M/N 1 to 2MHz	V40	-1.0	0.0	1.0	dB
Video f characteristics MN2	VFMN2	M/N 2 to 3MHz	V41	-1.0	0.0	1.0	dB
Video f characteristics MN3	VFMN3	M/N 3.58MHz	V42	-3.0	-1.5	0.0	dB
Video f characteristics BG1	VFBG1	B/G 1 to 3MHz	V43	-1.0	0.0	1.5	dB
Video f characteristics BG2	VFBG2	B/G 3 to 4MHz	V44	-1.5	0.0	1.5	dB
Video f characteristics BG3	VFBG3	B/G 4.43MHz	V45	-2.5	-1.0	0.5	dB
Video f characteristics I1	VFI1	I 1 to 3MHz	V46	-1.0	0.0	1.0	dB
Video f characteristics I2	VFI2	I 3 to 4MHz	V47	-1.0	0.0	1.5	dB
Video f characteristics I3	VFI3	I 4.43MHz	V48	-1.5	0.0	1.5	dB
Video f characteristics DK1	VFDK1	D/K 1 to 3MHz	V49	-1.0	0.0	1.0	dB
Video f characteristics DK2	VFDK2	D/K 3 to 4MHz	V50	-1.0	0.0	1.5	dB
Video f characteristics DK3	VFDK3	D/K 4.43MHz	V51	-1.5	0.0	1.5	dB
Group delay 2-2 BG shift (4M)	BGD2-2	wrt 1MHz	V52	50	100	150	ns
Group delay 2-3 BG shift (4.4M)	BGD2-3	wrt 1MHz	V53	110	180	250	ns
1st SIF Block							
SIF carrier output level 1	So1	V_i = 1mV	F1	21	43	86	mVrms
SIF carrier output level 2	So2	V_i = 10mV	F2	21	43	86	mVrms
1st SIF max input	Si max		F3	110	120		dBμV
1st SIF input resistance	Ris	33.4MHz	F4		2	2.4	kΩ
1st SIF input capacity	Cis	33.4MHz	F5		3	6	pF
SIF Block							
Limiting sensitivity (SPLIT)	V_i (lim) (SP)	P = 80dBμ CW	S1	20	25	30	dBμV
Limiting sensitivity (INTER)	V_i (lim) (IN)	P = 80dBμ P/S	S2	29	35	41	dB
FM detection output voltage	V_O (FM)	f = 5.5MHz, ΔF = ±30kHz	S3	390	560	730	mVrms
AM removal ratio	AMR		S4	50	60		dB
Distortion factor	THD		S5		0.3	0.8	%
FM detection output S/N	S/N (FM)	P = 80dBμ CW	S6	55	60		dB
PAL/NT audio voltage gain difference	GD		S7		6		dB
PAL De-emphasis	Pdeem		S8		-3		dB
NT De-emphasis	Ndeem		S9		-3		dB
Control Block							
SIF system SW threshold voltage A/B	V7_9th		C1	2.2	2.5	2.8	V
38MHz/38.9MHz threshold voltage	V10th1		C2	0.7	1.0	1.3	V
38.9MHz/39.5MHz threshold voltage	V10th2		C3	3.7	4.0	4.3	V
Inter-carrier system	V13th		C4			0.3	V
AFT mute level/SIF trap shift threshold voltage 1	V15th1		C5	0.7	1.0	1.3	V
AFT mute level/SIF trap shift threshold voltage 2	V15th2		C6	2.2	2.5	2.8	V
AFT mute level/SIF trap shift threshold voltage 3	V15th3		C7	3.7	4.0	4.3	V
Others							
Ref clock input level	Reflev	4.0MHz	O1	83	90	95	dBμV
Reference frequency SW threshold resistance	R11		O2	150	270		kΩ

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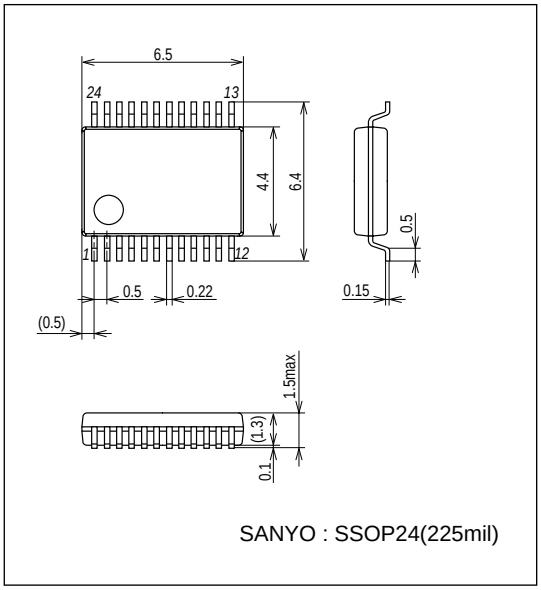
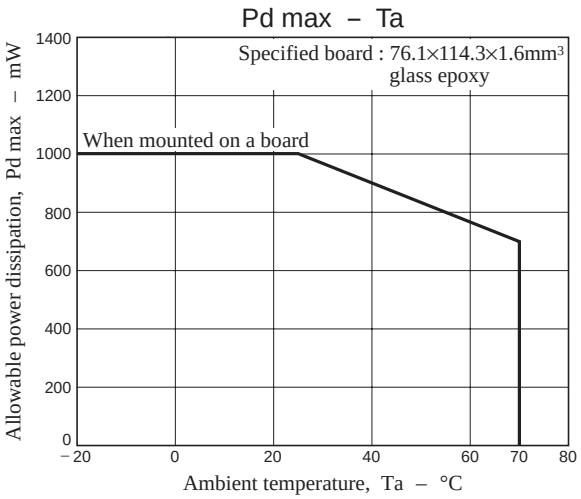
Package Dimensions

unit : mm (typ)

3287





System changeover

a. SIF system SW

The SIF system can be changed over by setting A (pin 7) and B (pin 9) to GND and OPEN respectively.

A	B	BG	I	DK	MN	FM DET LEVEL	De-emphasis
GND	GND				O	6dB	75μs
GND	OPEN			O		0dB	50μs
OPEN	GND		O			0dB	50μs
OPEN	OPEN	O				0dB	50μs

Note : Circles mean that the system indicated with a circle is selected

b. IF system SW

The IF frequency becomes 38.9MHz when pin 10 is open.
The IF frequency becomes 38.0MHz when pin 10 is set to GND.
The IF frequency becomes 39.5MHz when pin 10 is set to V_{CC}.

c. Split/inter carrier SW

Inter-carrier is selected by setting the 1st SIF input (pin 13) to GND.

d. Reference frequency changeover SW

The reference frequency becomes 4.43MHz when pin 11 is OPEN.
The reference frequency becomes 4.0MHz when 270kΩ is connected between pin 11 and GND.

e. AFT mute level, trap point shift SW

By changing the pin 15 voltage, the potential and TRAP point at which AFT is muted can be set to either just or shift (about +220kHz).

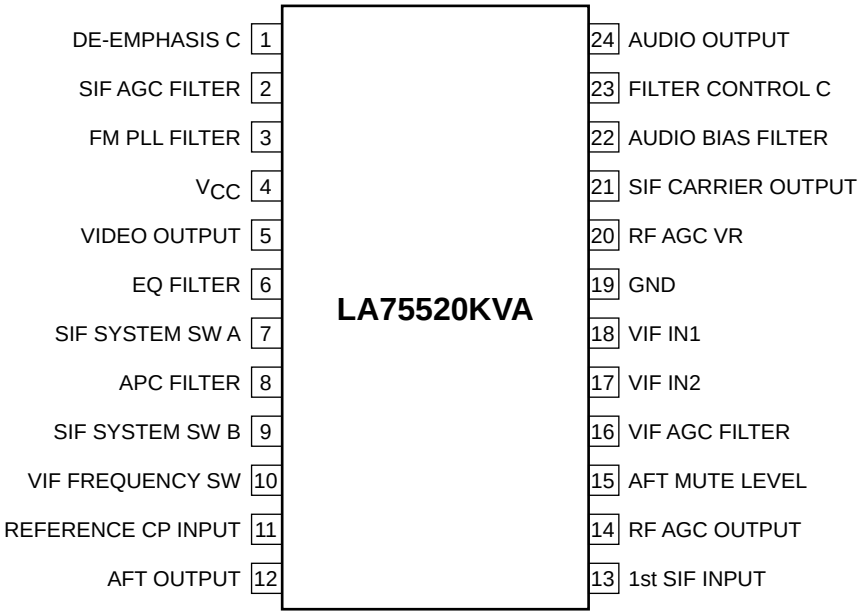
Pin 15 potential	AFT mute potential	TRAP point shift
V_{CC} to 4V	MIDDLE (V_{CC}/2)	Just
4V to 2.5V	MIDDLE (V_{CC}/2)	Shift
2.5V to 1V	HI (V_{CC})	Just
1V to GND	HI (V_{CC})	Shift

* V_{CC}=5V

f. FM detector function not used

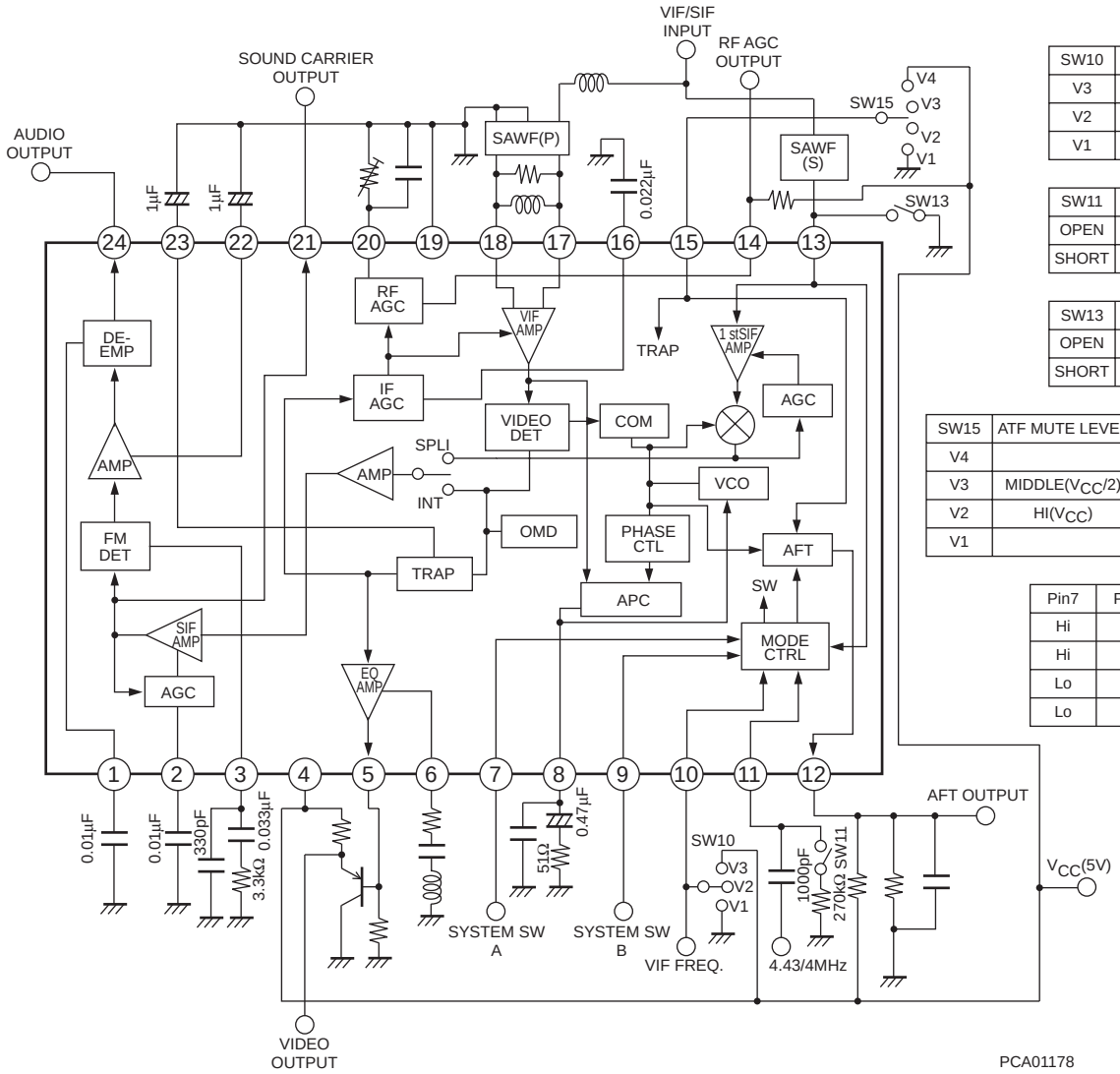
To stop FM detection VCO without using the SIF circuit, short-circuit pin 1 – GND with resistance of 1kΩ or less.

Pin Assignment



Top View

Block Diagram and Sample Application



SW10	VIF FREQUENCY
V3	39.5MHz
V2	38.9MHz
V1	38.0MHz

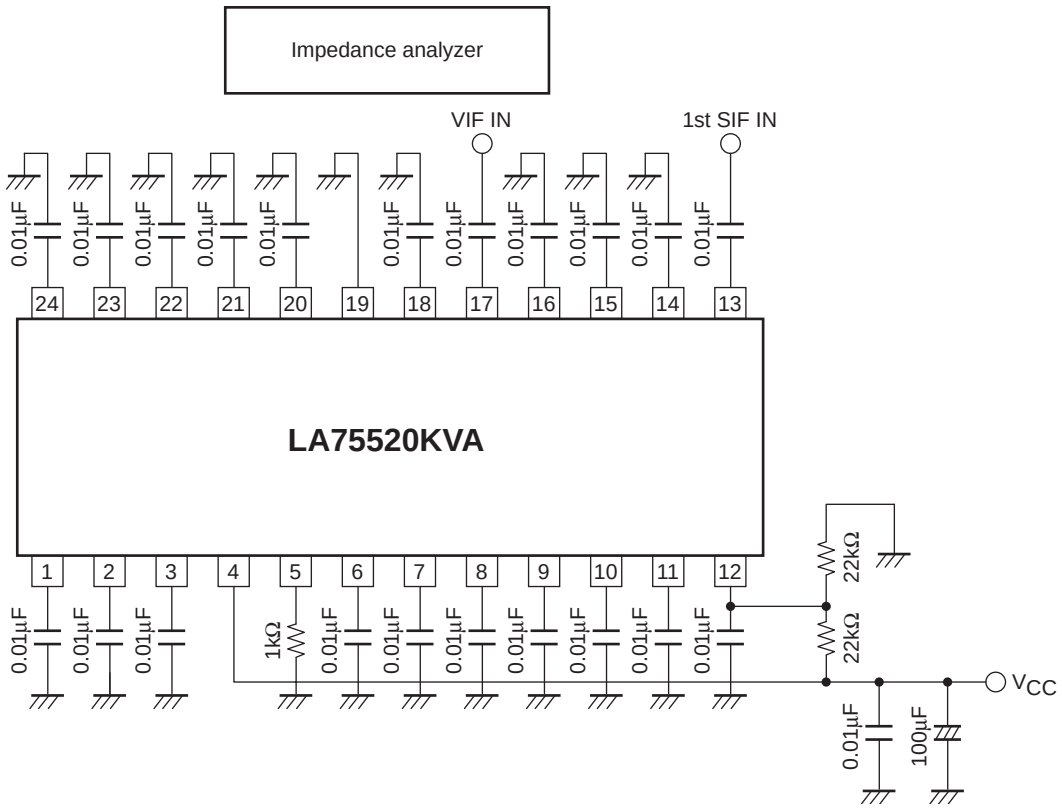
SW11	REFERENCE
OPEN	4.43MHz
SHORT	4.0MHz

SW13	SYSTEM
OPEN	SPLIT
SHORT	INTER

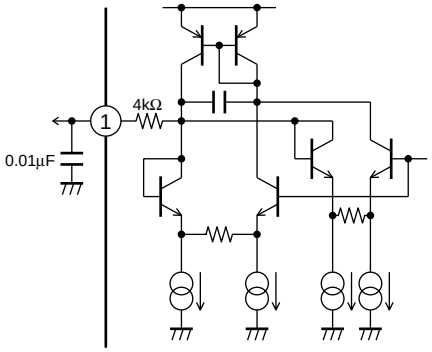
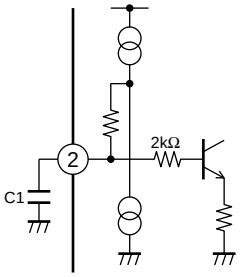
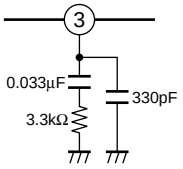
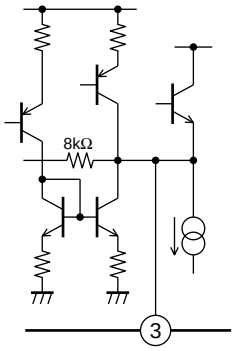
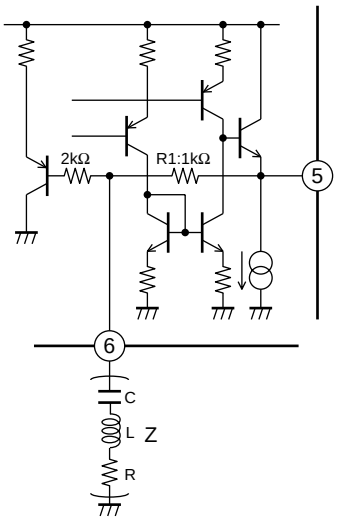
SW15	ATF MUTE LEVEL	B/G TRAP SHIFT
V4		0
V3	MIDDLE(V_{CC}/2)	+250kHz
V2	HI(V_{CC})	0
V1		+250kHz

Pin7	Pin9	SIF SYSTEM
Hi	Hi	B/G
Hi	Lo	I
Lo	Hi	D/K
Lo	Lo	M

Input Impedance Test Circuit (VIF and first SIF input impedance)



Pin Functions

Pin No.	Pin name	Function	Equivalent Circuit
1	DE-EMPHASIS C	De-emphasis capacitor connection pin This is used to switch the equivalent resistance (5kΩ or 7.5kΩ) internally in the IC to select the time constant. This switching is linked to the SIF input switch. To disable de-emphasis, disconnect the capacitor. Connection of an external capacitance of 0.01μF enables switching between 50 and 75μs. When the FM detector circuit is not to be used, the FM VCO can be stopped by connecting it to ground with a resistor of 1kΩ or less.	
2	SIF AGC FILTER	AGC filter pin for SIF carrier 0.01μF is recommended for C1.	
3	FM PLL FILTER	PLL filter pin of FM detector This is used to configure an external lag lead filter. Example: Connect 330pF in parallel with the filter on the left (0.033μF + 3.3kΩ). 	
4	V_{CC}	Power supply	
5 6	EQ OUT EQ FILTER	Equalizer circuit. This circuit is used to correct the video signal frequency characteristics. Notes on equalizer amplifier design • The equalizer amplifier is designed as a voltage follower amplifier with a gain of about 0 dB. When used for frequency characteristics correction, a capacitor, inductor, and resistor must be connected in series between pin 6 and ground. Equalizer amplifier gain $AV = \frac{R1}{Z} + 1$ R1 is the IC internal resistance, and is 1kΩ. In the application design, simply select Z to correspond to the desired characteristics. However, since the EQ amplifier gain will be maximum at the resonant point defined by Z, care is required to assure that distortion does not occur.	

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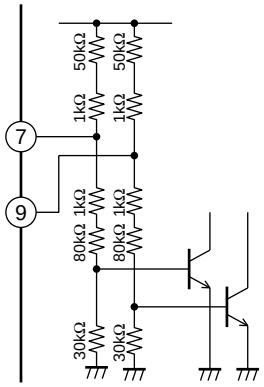
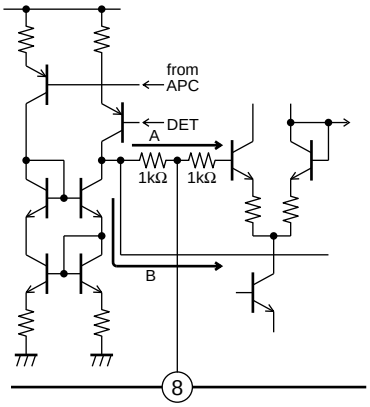
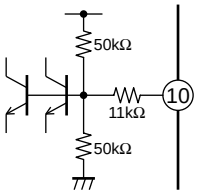
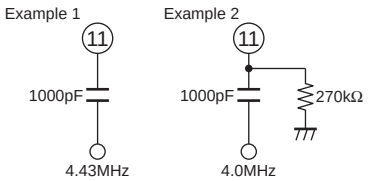
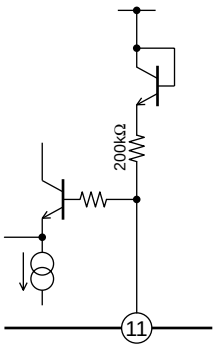
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Function</th><th>Equivalent Circuit</th></tr>
<tr><td>7
9</td><td>SIF SYSTEM SW A</td><td>SIF system selection switch pins. Combining the settings of these two pins supports four systems.
In M/N mode, the audio output level is increased by 6dB.
The internal trap is also linked to these switches.
The truth-values are as follows.
<table>
<tr><th>Pin7</th><th>Pin9</th><th>MODE</th></tr>
<tr><td>H</td><td>H</td><td>B/G</td></tr>
<tr><td>H</td><td>L</td><td>I</td></tr>
<tr><td>L</td><td>H</td><td>D/K</td></tr>
<tr><td>L</td><td>L</td><td>M/N</td></tr>
</table></td><td> 
</td></tr>
<tr><td>8</td><td>APC FILTER</td><td>PLL APC filter connection pin. The APC count is switched internally in the IC.
The VCO is normally controlled by route A.
When unlocked and during weak field reception, the VCO is controlled by route B and the loop gain is increased.
For this APC filter we recommend a resistor of 51Ω and capacitor of 0.47μF.
The buzz characteristics can be improved by connecting a capacitor of 100pF or so between pins 5 and 8.</td><td> 
</td></tr>
<tr><td>10</td><td>VIF FREQUENCY SW</td><td>Switch pin for selecting the IF frequency
When this pin is open, 1/2V_{CC} exists.

V_{CC} : 39.5MHz
Open : 38.9MHz
GND : 38.0MHz</td><td> 
</td></tr>
<tr><td>11</td><td>REFERENCE CP INPUT</td><td>Reference signal input pin necessary for adjusting the internal sound carrier trap, AFT, etc.
Either 4.0 or 4.43 MHz can be selected. Use the configuration shown in example 1 when using 4.43MHz and configuration shown in example 2 when using 4.0MHz.
Since no oscillator can be configured simply by connecting the X'tal resonator to pin 11, input the reference signal from an external source without fail.
 
</td><td> 
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</table>

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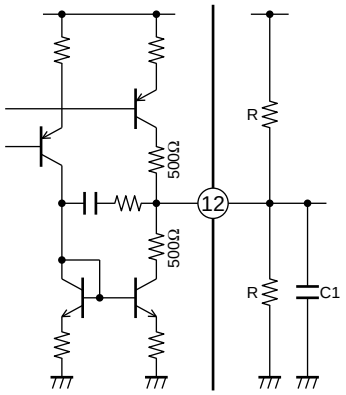
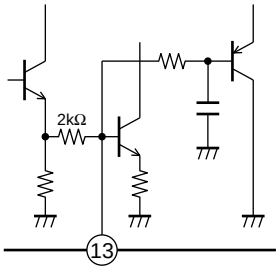
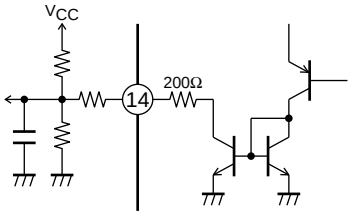
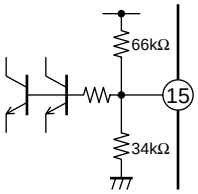
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Function</th><th>Equivalent Circuit</th></tr>
<tr><td>12</td><td>AFT OUTPUT</td><td>AFT output pin. The AFT center voltage is generated by an external bleeder resistor. The AFT gain is increased by increasing the resistance of this external bleeder resistor.
For the resistor we recommend a resistance equal to or greater than 22kΩ.
For the filter C1 we recommend a capacitance of 0.1μF.</td><td> 
</td></tr>
<tr><td>13</td><td>1st SIF INPUT</td><td>First SIF input pin. A DC cut capacitor must be used in the input circuit.
(a) If a SAW filter is used :
The first SIF sensitivity can be increased by inserting an inductor between the SAW filter and the IC to neutralize the SAW filter output capacitance and the IC input capacitance.

(b) When used in an intercarrier system :
Connect this pin to ground.</td><td> 
</td></tr>
<tr><td>14</td><td>RF AGC OUTPUT</td><td>RF AGC output pin. This output controls the tuner RF AGC.
This is the open collector output and a protective 200Ω resistor is inserted. Determine the external bleeder resistor value in accordance with the specifications of the tuner.</td><td> 
</td></tr>
<tr><td>15</td><td>AFT MUTE LEVEL</td><td>A switch pin for selecting the mute potential when muting is applied to the AFT due to PLL unlock, etc. At the same time, it is used to control the trap point shift of the audio trap (in the B/G mode). When the frequency characteristics of the video band are to be made as flat as possible with the split input, the trap can be shifted to the high range although the attenuation of the sound carrier will drop. Therefore, when used in combination with the SAW filter, verify that the level is high enough before use.
<table>
<tr><th>Voltage</th><th>ATF MUTE Voltage</th><th>TRAP SHIFT</th></tr>
<tr><td>V_{CC} to 4V</td><td>V_{CC}/2</td><td>0</td></tr>
<tr><td>4V to 2.5V</td><td>V_{CC}/2</td><td>+250kHz</td></tr>
<tr><td>2.5V to 1V</td><td>V_{CC}</td><td>0</td></tr>
<tr><td>1V to GND</td><td>V_{CC}</td><td>+250kHz</td></tr>
</table>
* When V_{CC} = 5 V</td><td> 
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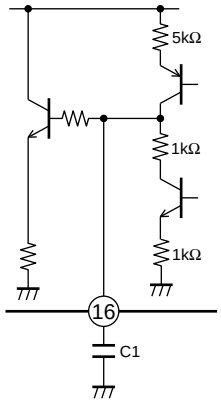
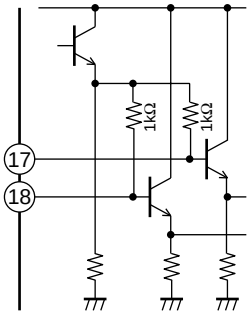
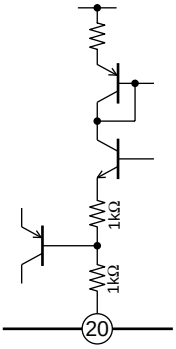
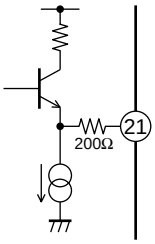
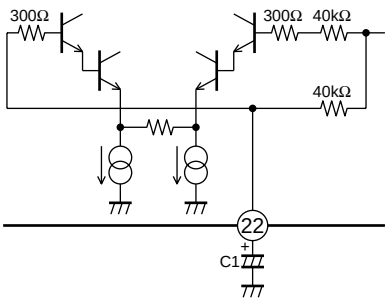
Pin No.	Pin name	Function	Equivalent Circuit
16	IF AGC	IF AGC filter connection pin. The signal peak-detected by the built-in AGC detector is converted to the AGC voltage at pin 16. Additionally, a second AGC filter (a lag-lead filter) used to create the dual time constants is provided internally in the IC. Use a 0.022µF capacitor as the external capacitor (C1), and adjust the value according to the sag, AGC speed, and other characteristics.	
17 18	VIF IN2 VIF IN1	VIF amplifier input pin The input circuit is a balanced circuit, and the input impedance is as follows: R ≈ 1.0kΩ	
19	GND		
20	RF AGC VR	RF AGC volume connection pin This pin sets the tuner RF AGC operating point. Also, the FM output and the video output can both be muted at the same time by connecting this pin to ground.	
21	SIF CARRIER OUT	First SIF output pin This is an emitter-follower output with a 200Ω resistor attached in series.	
22	AUDIO BIAS FILTER	Connection pin for a filter used to hold the FM detector output DC voltage fixed. Normally, a 1µF electrolytic capacitor should be used. The capacitance (CI) should be increased if the low band (around 50Hz) frequency characteristics need to be improved.	

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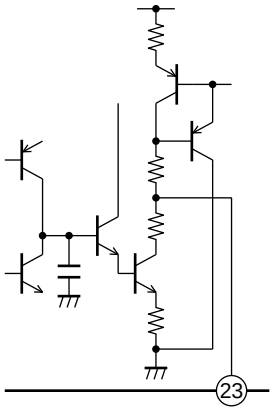
Pin No.	Pin name	Function	Equivalent Circuit
23	FILTER CONTROL C	Internal filter (trap) control pin Connect a capacitor with a capacitance between 0.47 to 1μF, depending on the video S/N as well as the levels of the AM and PM noise.	
24	AUDIO OUTPUT	Sound output pin Emitter follower output