

Single 4 x 1 and Dual 2 x 1 Multiplexers

DESCRIPTION

The DG9414, a single 4 to 1 multiplexer, and the DG9415, a dual 2 x 1 multiplexer, are monolithic CMOS analog devices designed for high performance low voltage operation. Combining low power, high speed, low on-resistance and small physical size, the DG9414 and DG9415 are ideal for portable and battery powered applications requiring high performance and efficient use of board space.

Both the DG9414 and DG9415 are built on Vishay Siliconix's low voltage BCD-15 process. Minimum ESD protection, per Method 3015.7, is 2000 volts. An epitaxial layer prevents latchup. Break-before-make is guaranteed for DG9415.

FEATURES

- Low Voltage Operation (+ 2.7 to + 12 V)
- Low On-Resistance - $r_{DS(on)}$: 14 Ω
- Low Power Consumption
- TTL Compatible
- ESD Protection > 2000 V (Method 3015.7)
- Available in TSSOP-10 (aka MSOP-10)


RoHS
COMPLIANT

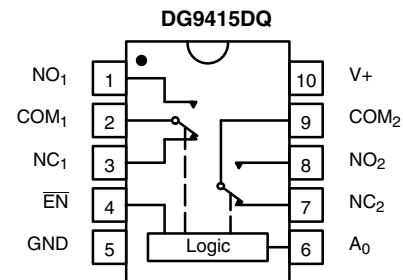
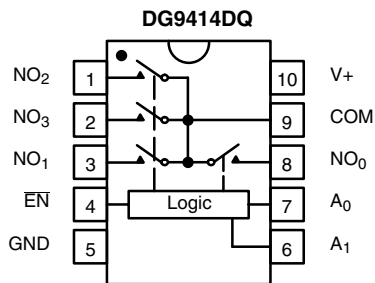
BENEFITS

- High Accuracy
- Simple Logic Interface
- Reduce Board Space

APPLICATIONS

- Battery Operated Systems
- Portable Test Equipment
- Sample and Hold Circuits
- Cellular Phones
- Communication Systems
- Networking Equipment

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



\overline{EN}	A ₁	A ₀	On Switch
1	X	X	None
0	0	0	NO ₀
0	0	1	NO ₁
0	1	0	NO ₂
0	1	1	NO ₃

X = Do not Care

\overline{EN}	A ₀	On Switch
1	X	None
0	0	NC ₁ NC ₂
0	1	NO ₁ NO ₂

X = Do not Care

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 °C	MSOP-10	DG9414DQ-T1-E3
		DG9415DQ-T1-E3



ABSOLUTE MAXIMUM RATINGS		
Parameter	Limit	Unit
Reference V+ to GND	- 0.3 to + 13	V
IN, COM, NC, NO ^a	- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)	± 20	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)	± 40	
ESD (Method 3015.7)	> 2000	V
Storage Temperature (D Suffix)	- 65 to 150	°C

Notes:

- a. Signals on S_x, D_x or IN_x exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads soldered or welded to PC board.

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V _{IN} = 0.4 V or 2.4 V ^e	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^c	Typ ^b	Max ^c	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 2.7 V, V _{COM} = 1.0 V/1.5 V/2.0 V I _{NO} or I _{NC} = 5 mA	Room		63	97	Ω
r _{ON} Match ^d	Δr _{ON}		Full			101	
r _{ON} Flatness ^{d,f}	r _{ON} Flatness		Room		3	11	
NO or NC Off Leakage Current ^g	I _{NO/NC(off)}	V+ = 3.3, V _{NO} or V _{NC} = 0.3 V/3 V V _{COM} = 3 V/0.3 V	Room	- 1		1	nA
COM Off Leakage Current ^g	I _{COM(off)}		Full	- 10		10	
Channel-On Leakage Current ^g	I _{COM(on)}	V+ = 3.3 V V _{COM} = V _{NO} or V _{NC} = 0.3 V/3 V	Room	- 1		1	
			Full	- 10		10	
Digital Control							
Input Current ^g	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	- 1.0		1.0	μA
Input High Voltage ^d	V _{INH}		Full	1.6			V
Input Low Voltage ^d	V _{INL}		Full			0.4	
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 1.5 V	Room		102	125	ns
Turn-Off Time	t _{OFF}		Full		45	68	
Break-Before-Make Time	t _D		Room	7	78	75	
Transition Time	t _{trans}	V _{NO} = 1.5 V/0 V, V _{NC} = 0 V/1.5 V	Room		81	128	pC
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{gen} = 0 V, R _{gen} = 0 Ω	Full			144	
Off-Isolation	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		- 58		dB
Channel-to-Channel Crosstalk (DG9415)	X _{TALK}	R _L = 50 Ω, f = 1 MHz	Room		- 64		
NO, NC Off Capacitance	C _{NO(off)} , C _{NC(off)}	f = 1 MHz	DG9414	Room	11		pF
			DG9415	Room	10		
COM Off Capacitance	C _{COM(off)}		DG9414	Room	26		
			DG9415	Room	13		
COM On Capacitance	C _{COM(on)}		DG9414	Room	43		
			DG9415	Room	25		
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current ^h	I+	V+ = 3.3 V, V _{IN} = 0 or 3.3 V	Full			1.0	μA



SPECIFICATIONS (V ₊ = 5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V ₊ = 5 V, ± 10 %, V _{IN} = 0.8 V or 2.4 V ^e	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^c	Typ ^b	Max ^c	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	0		V ₊	V
On-Resistance	r _{ON}	V ₊ = 4.5 V, V _{COM} = 1.5 V/2.5 V/3.5 V I _{NO} or I _{NC} = 10 mA	Room		33	56	Ω
r _{ON} Match	Δr _{ON}		Room		2	10	
r _{ON} Flatness ^f	r _{ON} Flatness		Room		10	20	
NO or NC Off Leakage Current ^g	I _{NO/NC(off)}	V ₊ = 5.5 V, V _{NO} or V _{NC} = 1 V/4.5 V V _{COM} = 4.5 V/1 V	Room	- 1		1	nA
COM Off Leakage Current ^g	I _{COM(off)}		Room	- 1		1	
Channel-On Leakage Current ^g	I _{COM(on)}	V ₊ = 5.5 V V _{COM} = V _{NO} or V _{NC} = 1 V/4.5 V	Room	- 1		1	
Digital Control							
Input Current ^h	I _{INL} or I _{INH}	V _{IN} = 0 or V ₊	Full	- 1.0		1.0	μA
Input High Voltage ^d	V _{INH}		Full	1.8			V
Input Low Voltage ^d	V _{INL}		Full			0.6	
Dynamic Characteristics							
Turn-On Time ^h	t _{ON}	V _{NO} or V _{NC} = 3.0 V	Room		56	77	ns
Turn-Off Time ^h	t _{OFF}		Room		25	46	
Break-Before-Make Timet ^h	t _D		Room	7	34		
Transition Time	t _{trans}	V _{NO} = 3 V/ 0 V, V _{NC} = 0 V/3 V	Room		47	77	dB
Off-Isolation	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		- 58		
Channel-to-Channel Crosstalk (DG9415)	X _{TALK}	R _L = 50 Ω, f = 1 MHz	Room		- 64		
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{gen} = 0 V, R _{gen} = 0 Ω	Room		6		pC
NO, NC Off Capacitance	C _{NO(off)} , C _{NC(off)}	f = 1 MHz	DG9414	Room		11	pF
			DG9415	Room		10	
COM Off Capacitance	C _{COM(off)}		DG9414	Room		25	
			DG9415	Room		13	
COM On Capacitance	C _{COM(on)}		DG9414	Room		42	
			DG9415	Room		24	
Power Supply							
Power Supply Range	V ₊			4.5		5.5	V
Power Supply Current ^h	I ₊	V ₊ = 5.5 V, V _{IN} = 0 or 5.5 V	Full			1.0	μA

Notes:

- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. Typical values are for design aid only, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Difference of min and max values.
- g. Guaranteed by 12 V leakage testing, not production tested.
- h. Guaranteed by worst case test conditions and not subject to test.

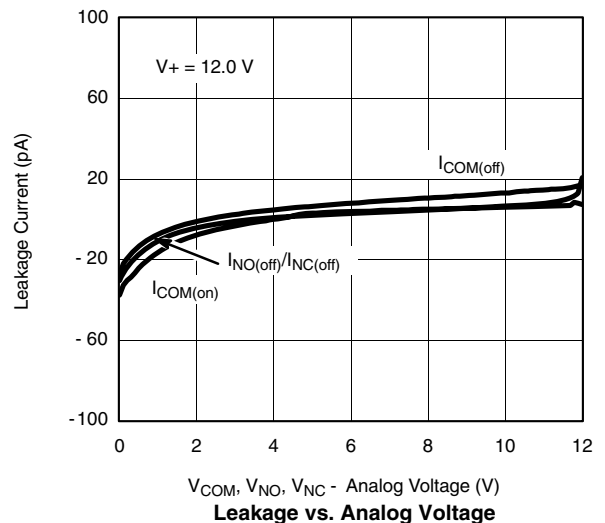
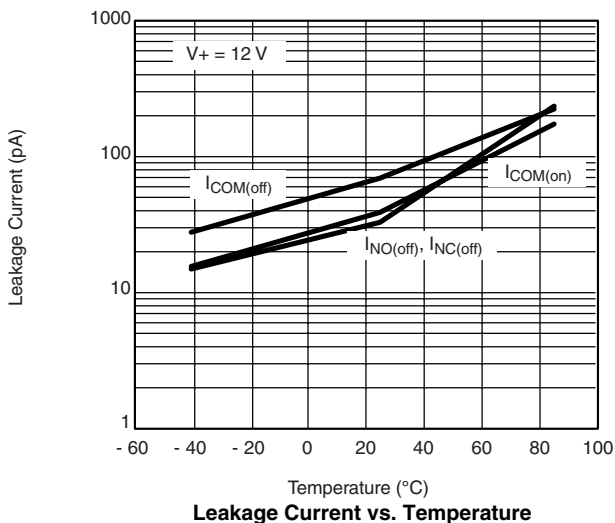
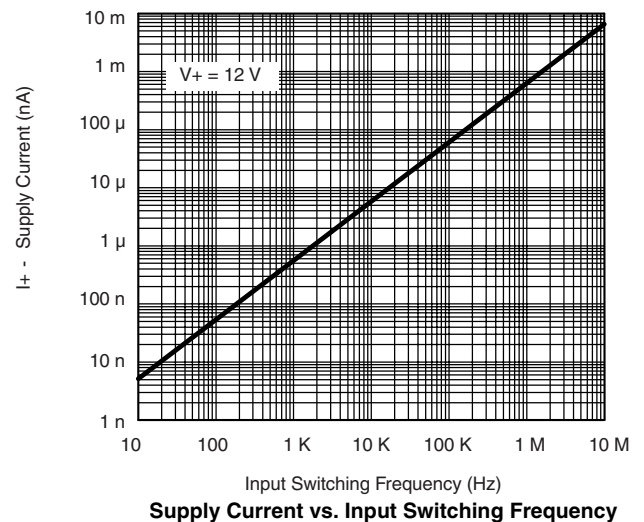
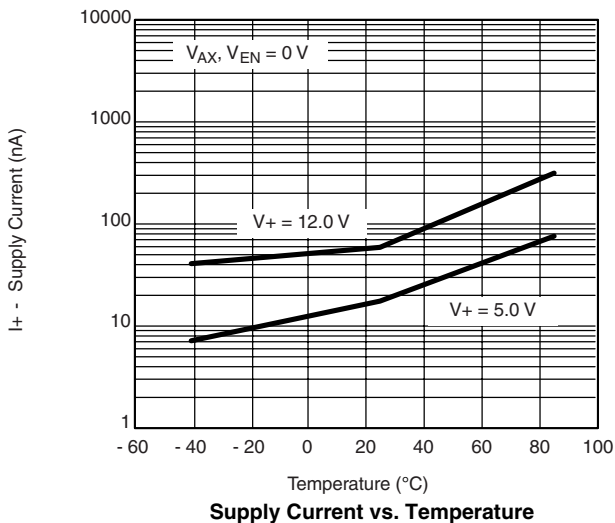
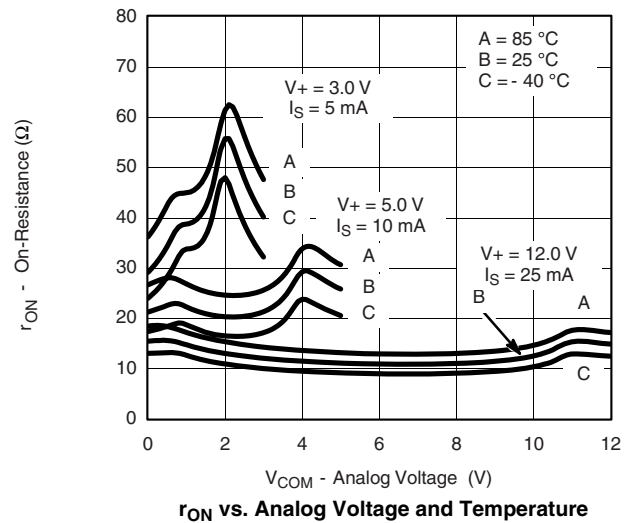
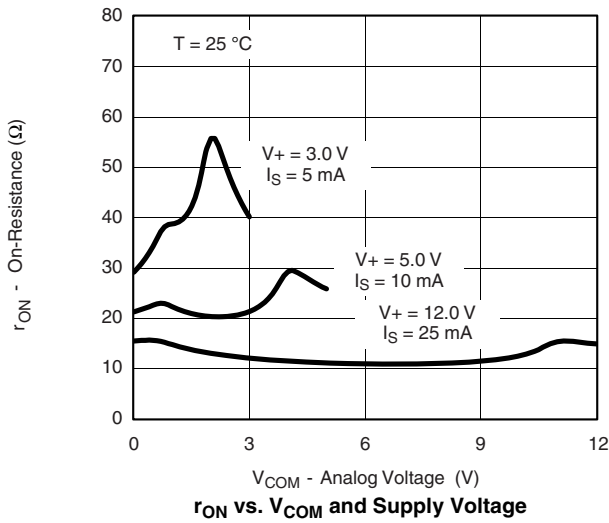


SPECIFICATIONS (V+ = 12 V)							
Parameter	Symbol	Test Conditions Unless Specified V+ = 12 V, VIN = 0.8 V or 2.4 V ^e	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^c	Typ ^b	Max ^c	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	0		12	V
r _{ON} Match	Δr _{ON}		Room		1	9	Ω
r _{ON} Flatness ^{d,f}	r _{ON} Flatness		Room		1	10	
On-Resistance	r _{ON}	V+ = 10.8 V, I _{NO} , I _{NC} = 25 mA V _{COM} = 2/9 V	Room Full		14	17 19	
Switch Off Leakage Current	I _{NO(off)} I _{NC(off)}	V _{COM} = 1/11 V V _{NO} , V _{NC} = 11/1 V	Room Full	- 1 - 10		1 10	nA
	I _{COM(off)}		Room Full	- 1 - 10		1 10	
Channel On Leakage Current	I _{COM(on)}	V _{NO} , V _{NC} = V _{COM} = 11/1 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	- 1		1	μA
Input High Voltage ^d	V _{INH}		Full	2.4			V
Input Low Voltage ^d	V _{INL}		Full			0.8	
Dynamic Characteristics							
Turn-On Time ^h	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _{NO} , V _{NC} = 5 V See Figure 2	Room Full		33	55 59	ns
Turn-Off Time ^h	t _{OFF}		Room Full		17	40 41	
Break-Before-Make Time Delay ^h	t _D	DG419L Only, V _{NC} , V _{NO} = 5 V R _L = 300 Ω, C _L = 35 pF	Room	2	24		
Transition Time	t _{trans}	V _{NO} = 5 V/ 0 V, V _{NC} = 0 V/ 5 V	Room Full		29	56 59	
Charge Injection ^d	Q _{INJ}	V _g = 0 V, R _g = 0 Ω, C _L = 1 nF	Room		13		pC
Off Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF f = 1 MHz	Room		- 58		dB
Channel-to-Channel Crosstalk ^d	X _{TALK}		Room		- 64		
NO, NC Off Capacitance ^d	C _{NO(off)} , C _{NC(off)}	V _{IN} = 0 or V+, f = 1 MHz	DG9414	Room		10	pF
			DG9415	Room		10	
COM Off Capacitance	C _{COM(off)}		DG9414	Room		24	
			DG9415	Room		13	
COM On Capacitance ^d	C _{COM(on)}		DG9414	Room		40	
			DG9415	Room		23	
Power Supplies							
Positive Supply Current	I+	V _{IN} = 0 or 12 V	Full			1	μA

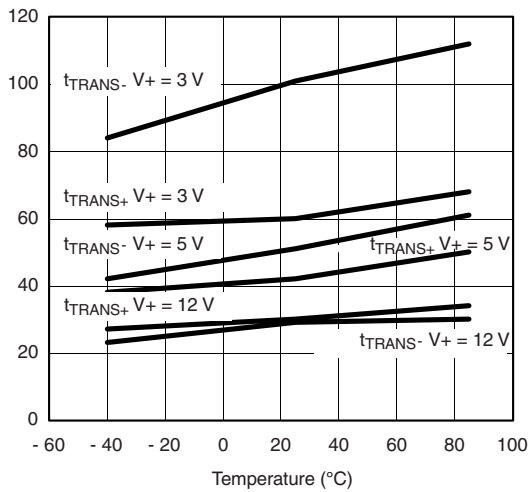
Notes:

- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. Typical values are for design aid only, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Difference of min and max values.
- g. Guaranteed by 12 V leakage testing, not production tested.
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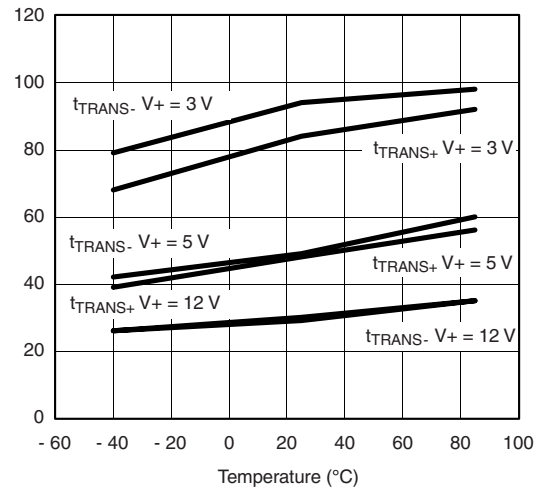
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


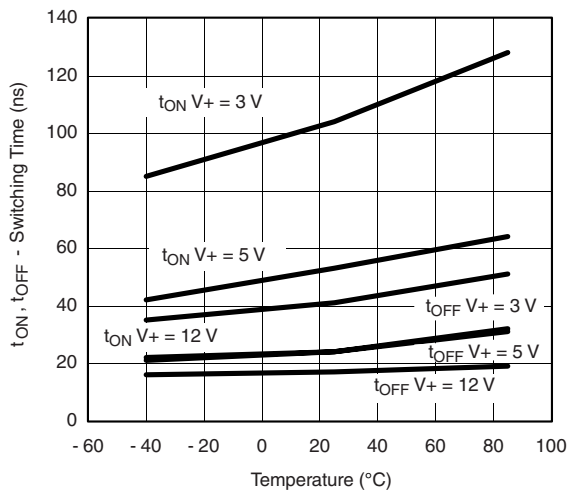
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



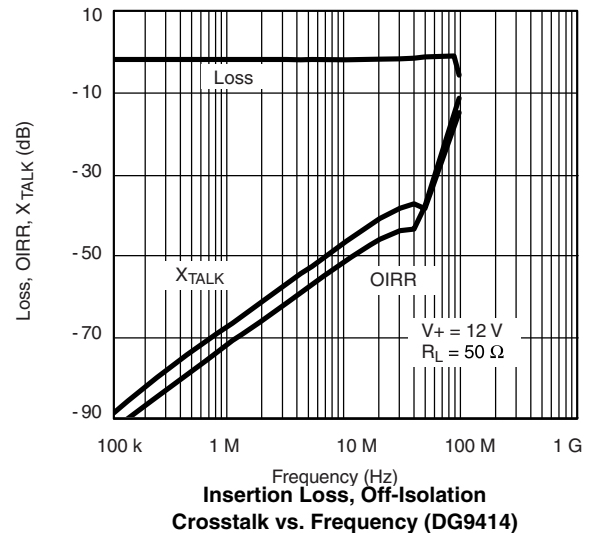
Transition Time vs. Temperature (DG9414)



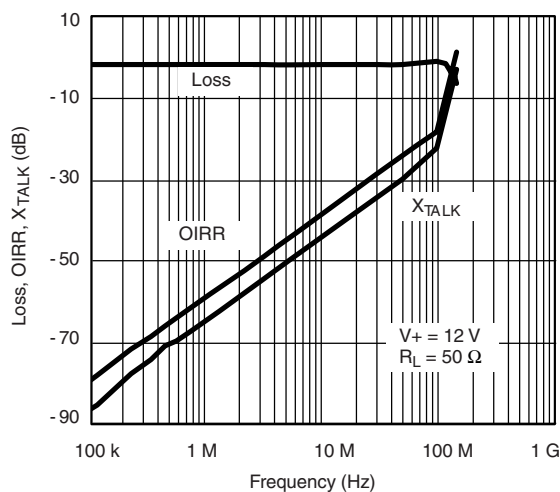
Transition Time vs. Temperature (DG9415)



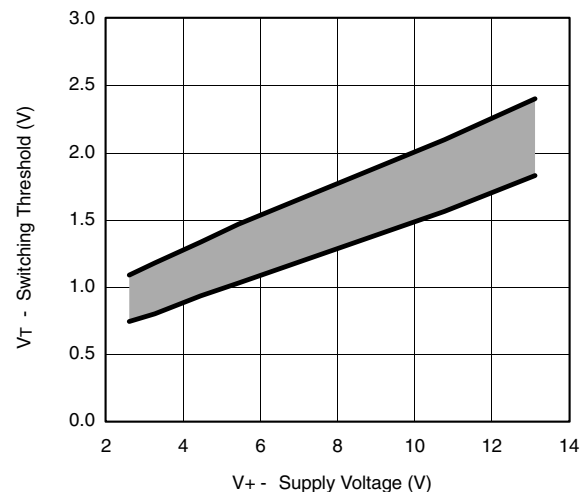
Switching Time vs. Temperature



Insertion Loss, Off-Isolation Crosstalk vs. Frequency (DG9414)

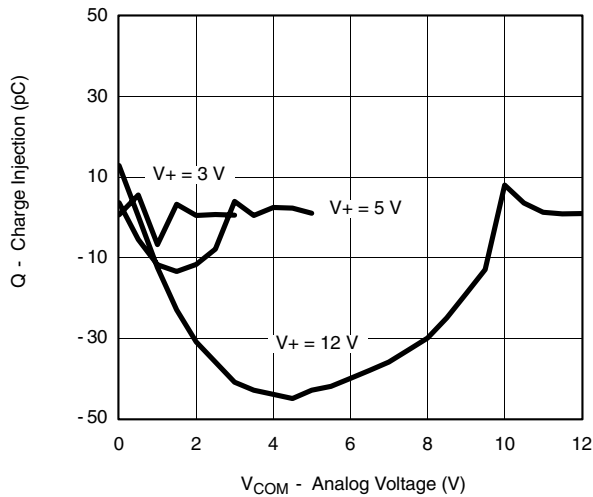


Insertion Loss, Off-Isolation Crosstalk vs. Frequency (DG9415)

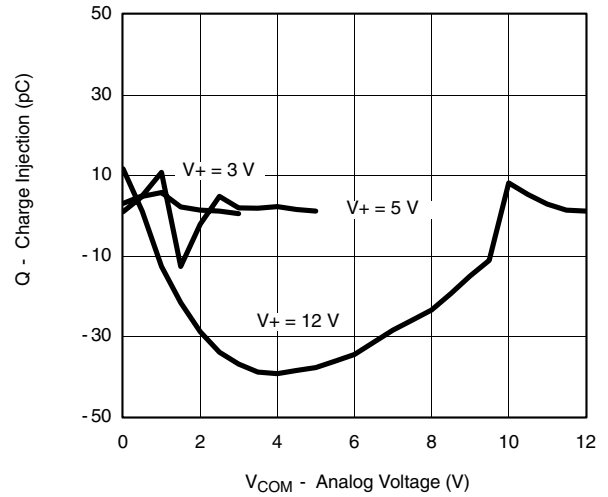


Switching Threshold vs. Supply Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Charge Injection vs. Analog Voltage (DG9414)



Charge Injection vs. Analog Voltage (DG9415)

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

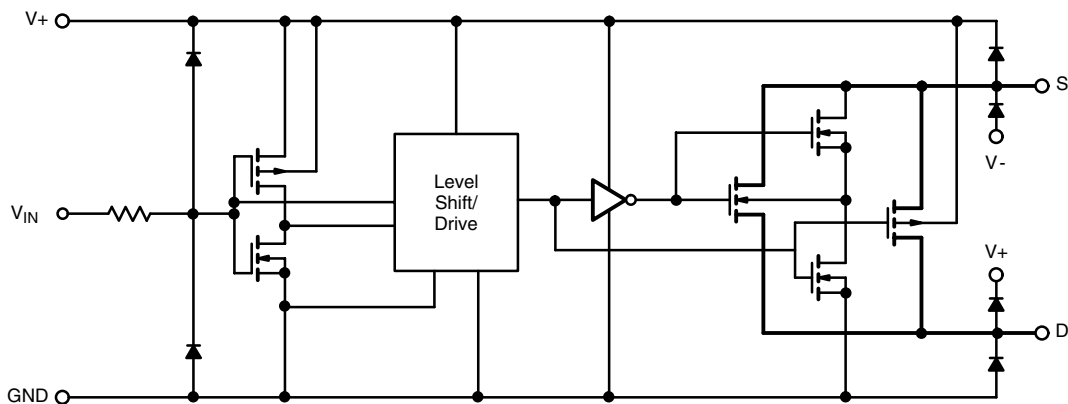
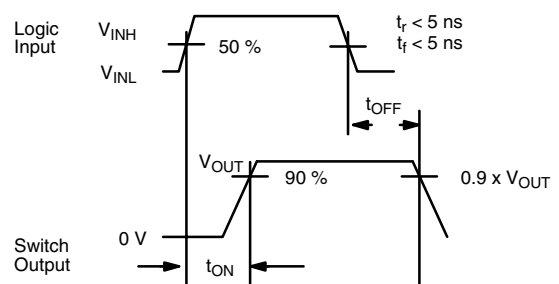
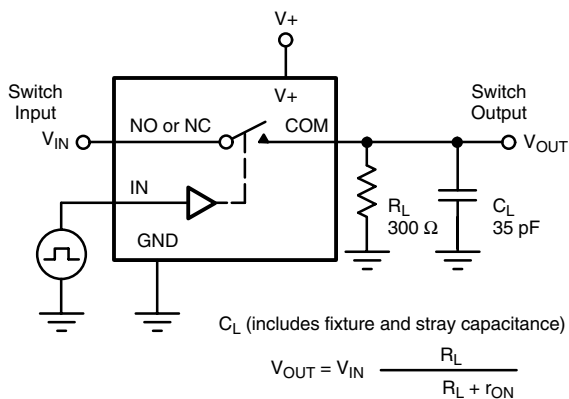


Figure 1.

TEST CIRCUITS



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time

TEST CIRCUITS

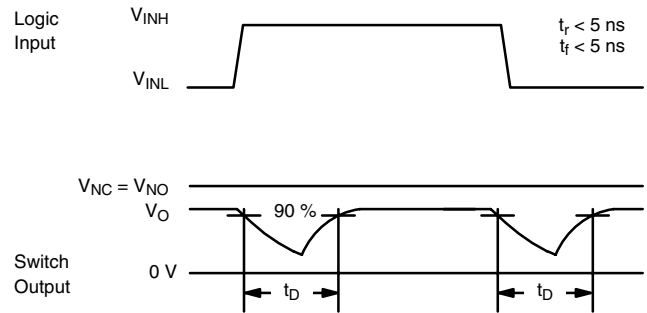
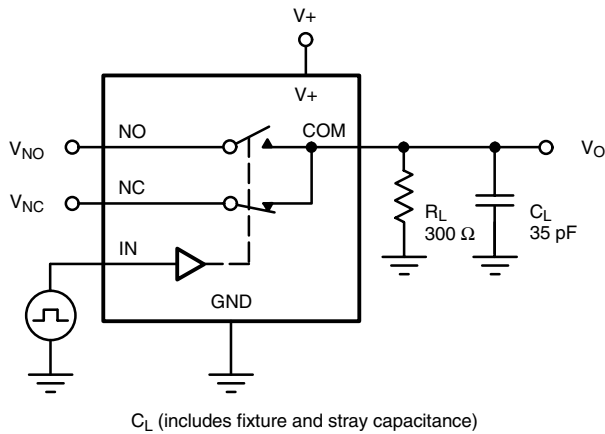


Figure 3. Break-Before-Make

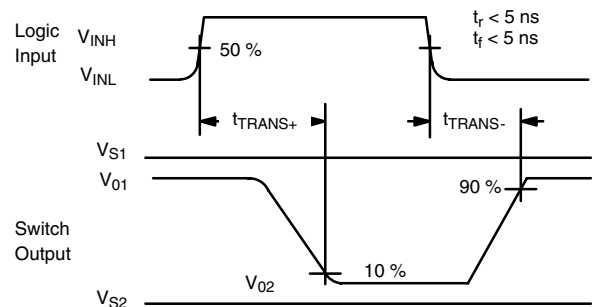
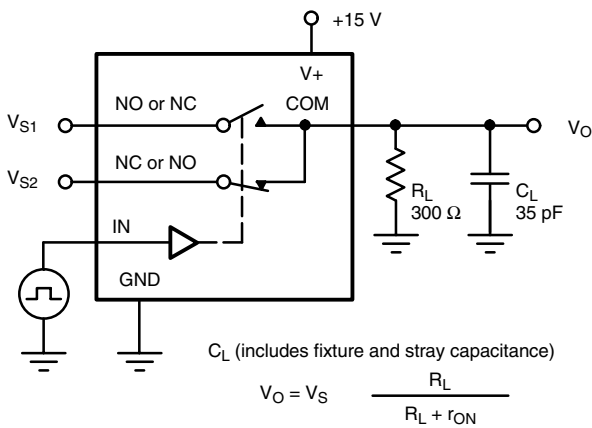
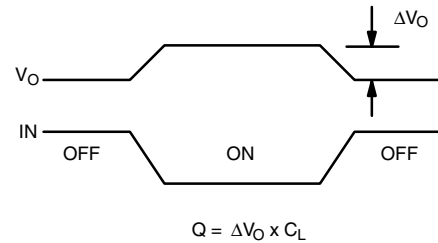
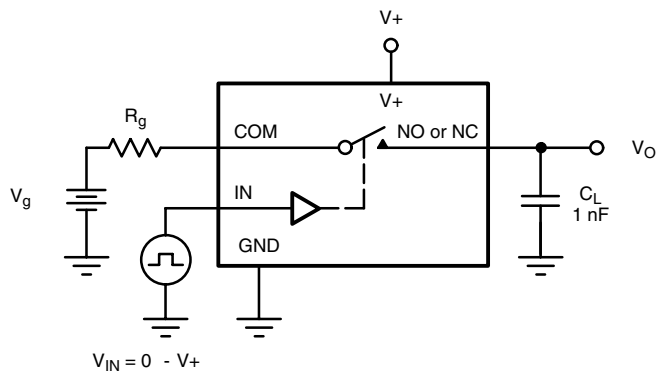


Figure 4. Transition Time



IN dependent on switch configuration Input polarity determined by sense of switch.

Figure 5. Charge Injection

TEST CIRCUITS

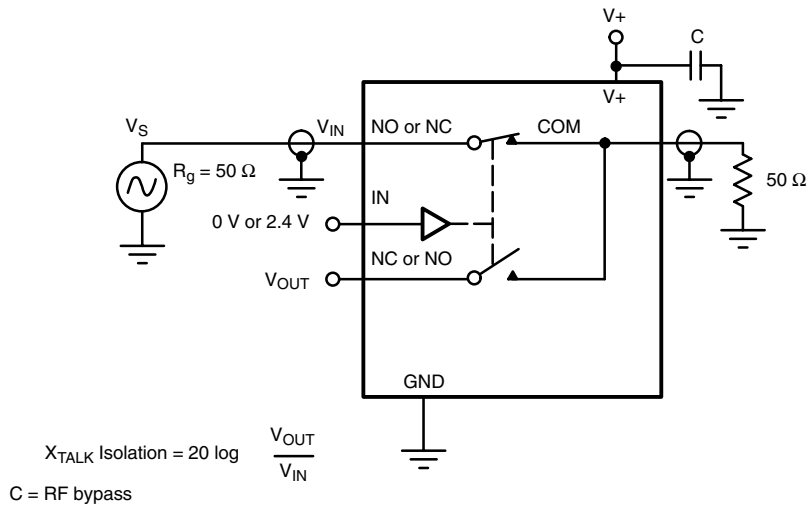


Figure 6. Crosstalk

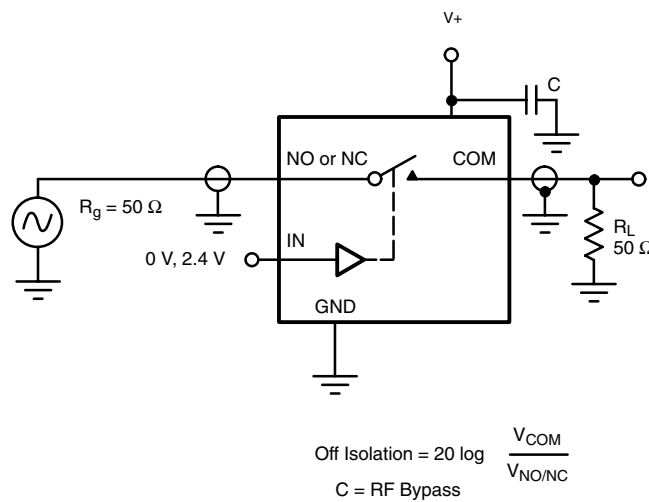


Figure 7. Off Isolation

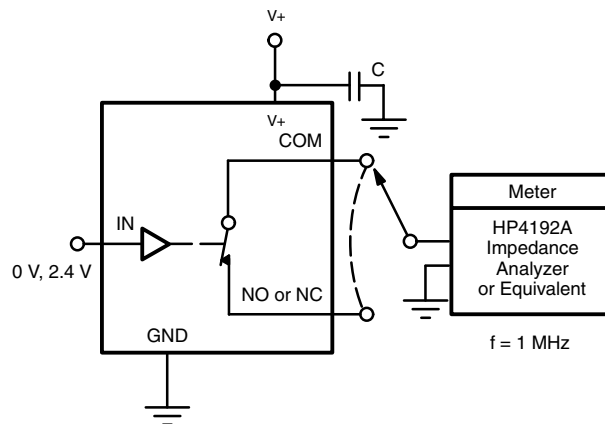


Figure 8. Source/Drain Capacitances

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