PRELIMINARY

CY14B104KA, CY14B104MA

4 Mbit (512K x 8/256K x 16) nvSRAM with Real-Time-Clock

Features

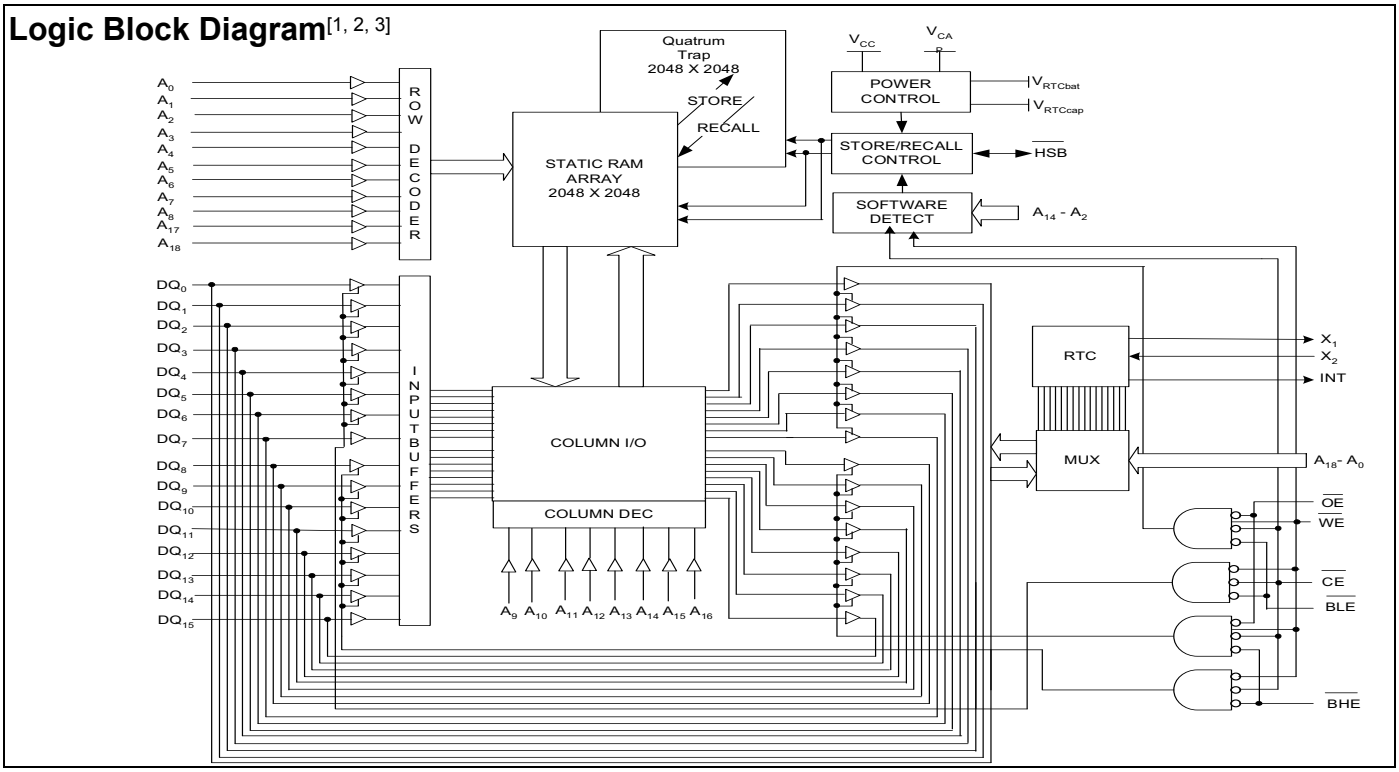
- 20 ns, 25 ns, and 45 ns access times
- Internally organized as 512K x 8 (CY14B104KA) or 256K x 16 (CY14B104MA)
- Hands off automatic STORE on power down with only a small capacitor
- STORE to QuantumTrap® nonvolatile elements is initiated by software, device pin, or AutoStore® on power down
- RECALL to SRAM initiated by software or power up
- High reliability
- Infinite read, write, and recall cycles
- 200,000 STORE cycles to QuantumTrap
- 20 year data retention
- Single 3V +20%, –10% operation
- Data integrity of Cypress nvSRAM combined with full featured Real-Time-Clock
- Watchdog timer
- Clock alarm with programmable interrupts
- Capacitor or battery backup for RTC
- Commercial and industrial temperatures
- 44 and 54-pin TSOP II package
- Pb-free and RoHS compliance

Functional Description

The Cypress CY14B104KA/CY14B104MA combines a 4-Mbit nonvolatile static RAM with a full featured real-time-clock in a monolithic integrated circuit. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM is read and written infinite number of times, while independent nonvolatile data resides in the nonvolatile elements.

The real-time-clock function provides an accurate clock with leap year tracking and a programmable, high accuracy oscillator. The alarm function is programmable for one time alarms or periodic seconds, minutes, hours, or days. There is also a programmable watchdog timer for process control.

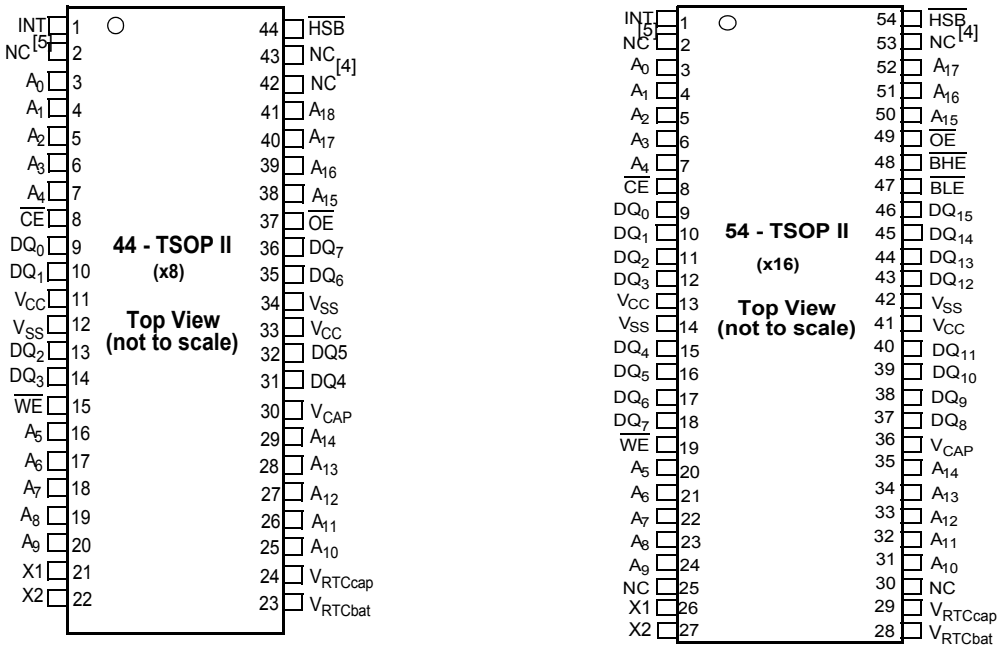
Logic Block Diagram[1, 2, 3]



Notes
1. Address A_0 - A_{18} for x8 configuration and Address A_0 - A_{17} for x16 configuration.
2. Data DQ_0 - DQ_7 for x8 configuration and Data DQ_0 - DQ_{15} for x16 configuration.
3. $\overline{BHE}$ and $\overline{BLE}$ are applicable for x16 configuration only.

Pinouts

Figure 1. Pin Diagram - 44/54-Pin TSOP II



Pin Definitions

Pin Name	IO Type	Description
$A_0 – A_{18}$	Input	**Address Inputs Used to Select one of the 524,288 bytes of the nvSRAM for x8 Configuration**.
$A_0 – A_{17}$		**Address Inputs Used to Select one of the 262,144 words of the nvSRAM for x16 Configuration**.
$DQ_0 – DQ_7$	Input/Output	**Bidirectional Data IO Lines for x8 Configuration**. Used as input or output lines depending on operation.
$DQ_0 – DQ_{15}$		**Bidirectional Data IO Lines for x16 Configuration**. Used as input or output lines depending on operation.
NC	No Connect	**No Connects.** This pin is not connected to the die.
$\overline{WE}$	Input	**Write Enable Input, Active LOW**. When selected LOW, data on the IO pins is written to the specific address location.
$\overline{CE}$	Input	**Chip Enable Input, Active LOW.** When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	**Output Enable, Active LOW.** The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the IO pins to tri-state.
$\overline{BHE}$	Input	**Byte High Enable, Active LOW**. Controls DQ_{15} - DQ_8.
$\overline{BLE}$	Input	**Byte Low Enable, Active LOW**. Controls DQ_7 - DQ_0.
X_1	Output	**Crystal Connection**. Drives crystal on start up.
X_2	Input	**Crystal Connection.** For 32.768 KHz crystal.
V_{RTCcap}	Power Supply	**Capacitor Supplied Backup RTC Supply Voltage**. Left unconnected if V_{RTCbat} is used.
V_{RTCbat}	Power Supply	**Battery Supplied Backup RTC Supply Voltage**. Left unconnected if V_{RTCcap} is used.

Notes
4. Address expansion for 8 Mbit. NC pin not connected to die.
5. Address expansion for 16 Mbit. NC pin not connected to die.

Pin Definitions (continued)

Pin Name	IO Type	Description
INT	Output	**Interrupt Output**. Programmable to respond to the clock alarm, the watchdog timer, and the power monitor. Also programmable to either active HIGH (push or pull) or LOW (open drain).
V_{SS}	Ground	**Ground for the Device**. Must be connected to ground of the system.
V_{CC}	Power Supply	**Power Supply Inputs to the Device**. 3.0V +20%, –10%
$\overline{HSB}$	Input/Output	**Hardware Store Busy (HSB)**. When LOW this output indicates that a hardware store is in progress. When pulled LOW external to the chip it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin HIGH if not connected (connection optional). After each store operation HSB is driven HIGH for short time with standard output high current.
V_{CAP}	Power Supply	**AutoStore Capacitor**. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.

Device Operation

The CY14B104KA/CY14B104MA nvSRAM is made up of two functional components paired in the same physical cell. These are a SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations SRAM read and write operations are inhibited. The CY14B104KA/CY14B104MA supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 200K STORE operations. See the "Truth Table For SRAM Operations" on page 23 for a complete description of read and write modes.

SRAM Read

The CY14B104KA/CY14B104MA performs a read cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW, and $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins A_{0-18} or A_{0-17} determines which of the 524,288 data bytes or 262,144 words of 16 bits each are accessed. Byte enables ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are enabled to the output, in the case of 16-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common IO pins DO_{0-15} are written into the memory if it is valid t_{SD} before the end of a $\overline{WE}$ controlled write or before the end of a $\overline{CE}$ controlled write. The Byte Enable inputs ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are written, in the case of 16-bit words. Keep $\overline{OE}$ HIGH during the entire write cycle to avoid data bus contention on common IO lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

The CY14B104KA/CY14B104MA stores data to the nvSRAM using one of three storage operations. These three operations are: hardware store, activated by the $\overline{HSB}$; software store, activated by an address sequence; AutoStore, on device power down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B104KA/CY14B104MA.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 2. AutoStore Mode

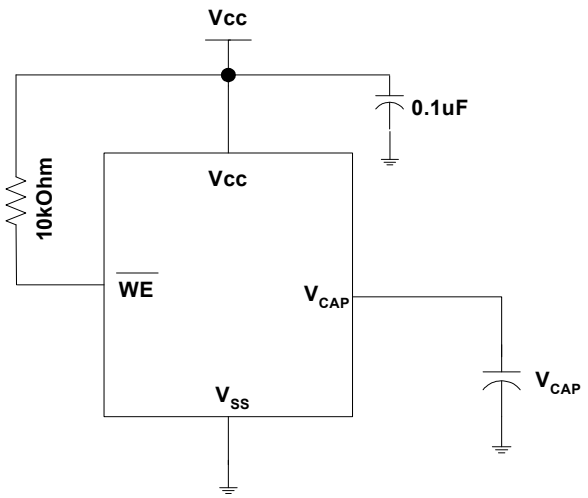


Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to DC Electrical Characteristics on page 14 for the size of the V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{CC} by a regulator on the chip. A pull up should be placed on $\overline{WE}$ to hold it inactive during power up. This pull up is only effective if the $\overline{WE}$ signal is tri-state during

power up. Many MPUs tri-state their controls on power up. Verify this when using the pull up. When the nvSRAM comes out of power-on-recall, the MPU must be active or the WE held inactive until the MPU comes out of reset.

To reduce unnecessary nonvolatile stores, AutoStore and hardware store operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place. The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.

Hardware STORE (HSB) Operation

The CY14B104KA/CY14B104MA provides the HSB pin to control and acknowledge the STORE operations. The HSB pin is used to request a hardware STORE cycle. When the HSB pin is driven LOW, the CY14B104KA/CY14B104MA conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle begins only if a write to the SRAM has taken place since the last STORE or RECALL cycle. The HSB pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

SRAM read and write operations, that are in progress when HSB is driven LOW by any means, are given time to complete before the STORE operation is initiated. After HSB goes LOW, the CY14B104KA/CY14B104MA continues SRAM operations for t_{DELAY}. If a write is in progress when HSB is pulled LOW it is allowed a time, t_{DELAY} to complete. However, any SRAM write cycles requested after HSB goes LOW are inhibited until HSB returns HIGH. In case the write latch is not set, HSB is not driven LOW by the CY14B104KA/CY14B104MA but any SRAM read and write cycles are inhibited until HSB is returned HIGH by MPU or another external source.

During any STORE operation, regardless of how it is initiated, the CY14B104KA/CY14B104MA continues to drive the HSB pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the CY14B104KA/CY14B104MA remains disabled until the HSB pin returns HIGH. Leave the HSB unconnected if it is not used.

Hardware RECALL (Power Up)

During power up or after any low power condition (V_{CC}< V_{SWITCH}), an internal RECALL request is latched. When V_{CC} again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time HSB is driven LOW by the HSB driver.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14B104KA/CY14B104MA software STORE cycle is initiated by executing sequential CE controlled read cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following read sequence must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with CE controlled reads or OE controlled reads. After the sixth address in the sequence is entered, the STORE cycle starts and the chip is disabled. It is important to use read cycles and not write cycles in the sequence, although it is not necessary that OE be LOW for a valid sequence. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for read and write operations.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, perform the following sequence of CE controlled read operations:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4C63 Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

Table 1. Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$[3]	A_{15} - A_0[6]	Mode	IO	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	L	X	Read SRAM	Output Data	Active
L	L	X	X	Write SRAM	Input Data	Active
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[7, 8]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[7, 8]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC2}[7, 8]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active[7, 8]

Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

The AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (hardware or software) is issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

Notes

6. While there are 19 address lines on the CY14B104KA (18 address lines on the CY14B104MA), only the 13 address lines (A_{14} - A_2) are used to control software modes. Rest of the address lines are don't care.
7. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile cycle.
8. IO state depends on the state of $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$. The IO table shown assumes $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$ LOW.

Data Protection

The CY14B104KA/CY14B104MA protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH}. If the CY14B104KA/CY14B104MA is in a write mode (both CE and WE are LOW) at power up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after t_{LZHSB} (HSB to output active). This protects against inadvertent writes during power up or brown out conditions.

Noise Considerations

Refer to CY application note AN1064.

Real-Time-Clock Operation

nvTIME Operation

The CY14B104KA/CY14B104MA offers internal registers that contain clock, alarm, watchdog, interrupt, and control functions. RTC registers use the last 16 address locations of the SRAM. Internal double buffering of the clock and the clock or timer information registers prevents accessing transitional internal clock data during a read or write operation. Double buffering also circumvents disrupting normal timing counts or the clock accuracy of the internal clock when accessing clock data. Clock and alarm registers store data in BCD format.

RTC functionality is described with respect to CY14B104KA in the following sections. The same description applies to CY14B104MA, except for the RTC register addresses. The RTC register addresses for CY14B104KA range from 0x7FFF0 to 0x7FFFF, while those for CY14B104MA range from 0x3FFF0 to 0x3FFFF. Refer to Table 3 on page 10 and Table 4 on page 11 for a detailed Register Map description.

Clock Operations

The clock registers maintain time up to 9,999 years in one second increments. The time can be set to any calendar time and the clock automatically keeps track of days of the week and month, leap years, and century transitions. There are eight registers dedicated to the clock functions, which are used to set time with a write cycle and to read time during a read cycle. These registers contain the time of day in BCD format. Bits defined as ‘0’ are currently not used and are reserved for future use by Cypress.

Reading the Clock

The double buffered RTC register structure reduces the chance of reading incorrect data from the clock. The user must stop internal updates to the CY14B104KA time, keeping registers before reading clock data, to prevent reading of data in transition. Stopping the internal register updates does not affect clock accuracy. The updating process is stopped by writing a ‘1’ to the read bit ‘R’ (in the flags register at 0x7FFF0), and does not restart until a ‘0’ is written to the read bit. The RTC registers are then read while the internal clock continues to run. After a ‘0’ is written to the read bit (‘R’), all CY14B104KA registers are simultaneously updated within 20 ms.

Setting the Clock

Setting the write bit ‘W’ (in the flags register at 0x7FFF0) to a ‘1’ stops updates to the time keeping registers and enables the time to be set. The correct day, date, and time is then written into the registers in 24 hour BCD format. The time written is referred to as the “Base Time”. This value is stored in nonvolatile registers and used in the calculation of the current time. Resetting the write bit to ‘0’ transfers the register values to the actual clock counters, after which the clock resumes normal operation.

Backup Power

The RTC in the CY14B104KA is intended for permanently powered operation. The V_{RTCcap} or V_{RTCbat} pin is connected depending on whether a capacitor or battery is chosen for the application. When the primary power, V_{CC}, fails and drops below V_{SWITCH} the device switches to the backup power supply.

The clock oscillator uses very little current, which maximizes the backup time available from the backup source. Regardless of the clock operation with the primary source removed, the data stored in the nvSRAM is secure, having been stored in the nonvolatile elements when power was lost.

During backup operation, the CY14B104KA consumes a maximum of 300 nanoamps at 2 volts. The user must choose capacitor or battery values according to the application. Backup time values based on maximum current specifications are shown in the following table. Nominal backup times are approximately three times longer.

Table 2. RTC Backup Time

Capacitor Value	Backup Time
0.1F	72 hours
0.47F	14 days
1.0F	30 days

Using a capacitor has the advantage of recharging the backup source each time the system is powered up. If a battery is used, a 3V lithium is recommended and the CY14B104KA sources current only from the battery when the primary power is removed. The battery is not, however, recharged at any time by the CY14B104KA. The battery capacity must be chosen for total anticipated cumulative down time required over the life of the system.

Stopping and Starting the Oscillator

The OSCEN bit in the calibration register at 0x7FFF8 controls the enable and disable of the oscillator. This bit is nonvolatile and is shipped to customers in the “enabled” (set to 0) state. To preserve the battery life when the system is in storage, OSCEN must be set to ‘1’. This turns off the oscillator circuit, extending the battery life. If the OSCEN bit goes from disabled to enabled, it takes approximately one second (two seconds maximum) for the oscillator to start.

While system power is off, if the voltage on the backup supply (V_{RTCcap} or V_{RTCbat}) falls below their respective minimum level, the oscillator may fail.The CY14B104KA has the ability to detect oscillator failure when system power is restored. This is recorded in the OSCF (Oscillator Failed bit) of the flags register at the address 0x7FFF0. When the device is powered ON (V_{CC} goes

above V_{SWITCH}) the OSCEN bit is checked for “enabled” status. If the OSCEN bit is enabled and the oscillator is not active within the first 5 ms, the OSCF bit is set to “1”. Check for this condition and then write ‘0’ to clear the flag. Note that in addition to setting the OSCF flag bit, the time registers are reset to the “Base Time” (see Setting the Clock on page 6), which is the value last written to the timekeeping registers. The control or calibration registers and the OSCEN bit are not affected by the ‘oscillator failed’ condition.

The value of OSCF must be reset to ‘0’ when the time registers are written for the first time. This initializes the state of this bit which may have become set when the system was first powered on.

To reset OSCF, set the write bit “W” (in the flags register at 0x7FFF0) to a “1” to enable writes to the Flag register. Write a “0” to the OSCF bit and then reset the write bit to “0” to disable writes.

Calibrating the Clock

The RTC is driven by a quartz controlled oscillator with a nominal frequency of 32.768 KHz. Clock accuracy depends on the quality of the crystal, usually specified to 35 ppm limits at 25°C. This error could equate to +1.53 minutes per month. The CY14B104KA employs a calibration circuit that improves the accuracy to +1 or –2 ppm at 25°C. The calibration circuit adds or subtracts counts from the oscillator divider circuit.

The number of times pulses are suppressed (subtracted, negative calibration) or split (added, positive calibration) depends on the value loaded into the five calibration bits found in the calibration register at 0x7FFF8. Adding counts speeds the clock up; subtracting counts slows the clock down. The calibration bits occupy the five lower order bits in the control register 8. These bits are set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit, where ‘1’ indicates positive calibration and ‘0’ indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles.

If a binary ‘1’ is loaded into the register, only the first 2 minutes of the 64 minute cycle are modified; if a binary ‘6’ is loaded, the first 12 are affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles; that is, 4.068 or –2.034 ppm of adjustment for every calibration step in the calibration register.

To determine how to set the calibration, the CAL bit in the flags register at 0x7FFF0 is set to ‘1’, which causes the INT pin to toggle at a nominal 512 Hz. Any deviation measured from the 512 Hz indicates the degree and direction of the required correction. For example, a reading of 512.01024 Hz indicates a +20 ppm error, which requires the loading of a –10 (001010) into the calibration register. Note that setting or changing the calibration register does not affect the frequency test output frequency.

To set or clear CAL, set the write bit “W” (in the flags register at 0x7FFF0) to “1” to enable writes to the Flag register. Write a value to CAL, and then reset the write bit to “0” to disable writes.

Alarm

The alarm function compares user programmed values of alarm time/date (stored in the registers 0x7FFF1-5) with the corresponding time of day/date values. When a match occurs, the alarm internal flag (AF) is set and an interrupt is generated on INT pin if Alarm Interrupt Enable (AIE) bit is set. If the interrupt is triggered at the time when the user is reading the RTC Flags register, it is not reflected on INT pin until the user completes the read operation.

There are four alarm match fields: date, hours, minutes, and seconds. Each of these fields has a match bit that is used to determine if the field is used in the alarm match logic. Setting the match bit to ‘0’ indicates that the corresponding field is used in the match process. Depending on the match bits, the alarm occurs as specifically as once a month or as frequently as once every minute. Selecting none of the match bits (all 1s) indicates that no match is required. In this condition, alarm is disabled. Selecting all match values (all 0s) causes an exact time and date match.

There are two ways to detect an alarm event: by reading the AF flag or monitoring the INT pin. The AF flag in the flags register at 0x7FFF0 indicates that a date or time match has occurred. The AF bit is set to “1” when a match occurs. Reading the flags or control register clears the alarm flag bit (and all others). A hardware interrupt pin may also be used to detect an alarm event.

Note CY14B104KA/CY14B104MA require the alarm match bit for seconds (0x7FFF2 - D7) to be set to ‘0’ for the proper operation of Alarm Flag and Interrupt.

Alarm registers are not nonvolatile and therefore, they need to be reinitialized by software on power up. To set, clear, or enable an alarm, set the ‘W’ bit (in Flags Register - 0x7FFFF) to “1” to enable writes to Alarm Registers. After writing the alarm value, clear the ‘W’ bit back to “0” for the changes to take effect.

Watchdog Timer

The watchdog timer is a free running down counter that uses the 32 Hz clock (31.25 ms) derived from the crystal oscillator. The oscillator must be running for the watchdog to function. It begins counting down from the value loaded in the watchdog timer register.

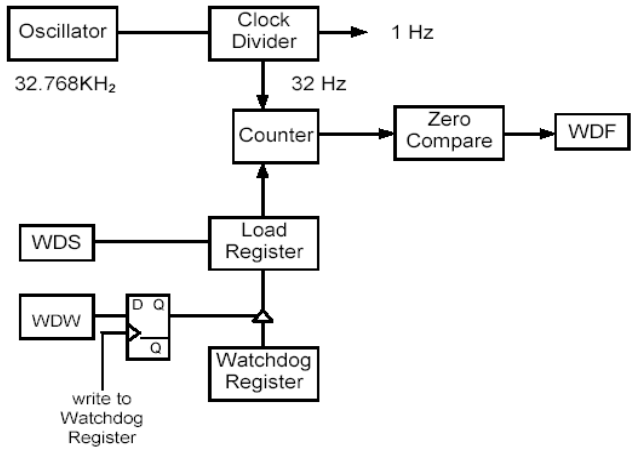
The counter consists of a loadable register and a free running counter. On power up, the watchdog timeout value in register 0x7FFF7 is loaded into the counter load register. Counting begins on power up and restarts from the loadable value any time the Watchdog Strobe (WDS) bit is set to ‘1’. The counter is compared to the terminal value of 0. If the counter reaches this value, it causes an internal flag and an optional interrupt output. The timeout interrupt is prevented by setting WDS bit to ‘1’ before the counter reaches ‘0’. This causes the counter to reload with the watchdog timeout value and get restarted. As long as the WDS bit is set before the counter reaches the terminal value, the interrupt and flag never occurs.

New timeout values are written by setting the watchdog write (WDW) bit to ‘0’. When the WDW is ‘0’ (from the previous operation), new writes to the watchdog timeout value bits D5–D0 enable the modification of timeout values. When WDW is ‘1’, then writes to bits D5–D0 are ignored. The WDW function enables setting the WDS bit without concern that the watchdog timer value is modified. A logical diagram of the watchdog timer

is shown in Figure 3 on page 8. Note that setting the watchdog timeout value to '0' is otherwise meaningless and as a result, disables the watchdog function.

The output of the watchdog timer is a flag bit WDF that is set if the watchdog is allowed to timeout. The flag is set on a watchdog timeout and cleared when the flags or control register is read by the user. The user can also enable an optional interrupt source to drive the INT pin if the watchdog timeout occurs.

Figure 3. Wachdog Timer Block Diagram



Power Monitor

The CY14B104KA provides a power management scheme with power fail interrupt capability. It also controls the internal switch to backup power for the clock and protects the memory from low V_{CC} access. The power monitor is based on an internal bandgap reference circuit that compares the V_{CC} voltage to various thresholds.

As described in the section AutoStore Operation on page 3, when V_{SWITCH} is reached as V_{CC} decays from power loss, a data store operation is initiated from SRAM to the nonvolatile elements, securing the last SRAM data state. Power is also switched from V_{CC} to the backup supply (battery or capacitor) to operate the RTC oscillator.

When operating from the backup source, no data is read or written and the clock functions are not available to the user. The clock continues to operate in the background. The updated clock data is available to the user after $t_{HRECALL}$ delay (see AutoStore/Power Up RECALL on page 20) after V_{CC} is restored to the device.

Interrupts

The CY14B104KA provides three potential interrupt sources. They include the watchdog timer, the power monitor, and the clock or calendar alarm. Each are individually enabled and assigned to drive the INT pin. In addition, each has an associated flag bit that the host processor uses to determine the cause of the interrupt. Some sources have additional control bits that determine functional behavior. In addition, the pin driver has three bits that specify its behavior when an interrupt occurs.

The three interrupts each have a source and an enable. Both the source and the enable must be active (true HIGH) to generate an interrupt output. Only one source is necessary to drive the pin. The user can identify the source by reading the flags or control register, which contains the flags associated with each source.

All flags are cleared to '0' when the register is read. The cycle must be a complete read cycle (WE HIGH); otherwise, the flags are not cleared. The power monitor has two programmable settings explained in the section Power Monitor.

After an interrupt source is active, the pin driver determines the behavior of the output. It has two programmable settings. Pin driver control bits are located in the interrupt register.

According to the programming selections, the pin is driven in the backup mode for an alarm interrupt. In addition, the pin is an active LOW (open drain) or an active HIGH (push pull) driver. If programmed for operation during backup mode, it is active LOW. Lastly, the pin can provide a one shot function so that the active condition is a pulse or a level condition. In one-shot mode, the pulse width is internally fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In the level mode, the pin goes to its active polarity until the flags or control register is read by the user. This mode is used as an interrupt to a host microcontroller. The control bits are summarized as follows.

Watchdog Interrupt Enable - WIE. When set to '1', the watchdog timer drives the INT pin and an internal flag when a watchdog timeout occurs. When WIE is set to '0', the watchdog timer affects only the internal flag.

Alarm Interrupt Enable - AIE. When set to '1', the alarm match drives the INT pin and an internal flag. When set to '0', the alarm match only affects the internal flag.

Power Fail Interrupt Enable - PFE. When set to '1', the power fail monitor drives the pin and an internal flag. When set to '0', the power fail monitor affects only the internal flag.

High/Low - H/L. When set to a '1', the INT pin is active HIGH and the driver mode is push pull. The INT pin can drive HIGH only when $V_{CC} > V_{SWITCH}$. When set to '0', the INT pin is active LOW and the drive mode is open drain. Active LOW (open drain) is operational even in battery backup mode.

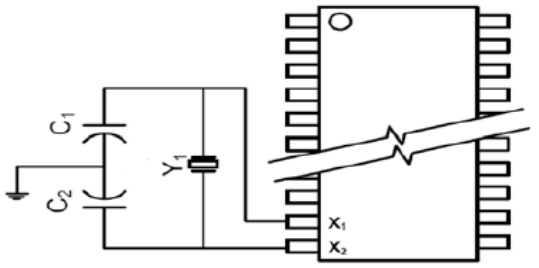
Pulse/Level - P/L. When set to '1' and an interrupt occurs, the INT pin is driven for approximately 200 ms. When P/L is set to '0', the INT pin is driven HIGH or LOW (determined by H/L) until the flags or control register is read.

When an enabled interrupt source activates the INT pin, an external host can read the flags or control register to determine the cause. All flags are cleared when the register is read. If the INT pin is programmed for level mode, then the condition clears and the INT pin returns to its inactive state. If the pin is programmed for pulse mode, then reading the flag also clears the flag and the pin. The pulse does not complete its specified duration if the flags or control register is read. If the INT pin is used as a host reset, then the flags or control register must not be read during a reset. During a power on reset with no battery, the interrupt register is automatically loaded with the value 24h. This enables the power fail interrupt with an active LOW pulse.

Flags Register

The Flag regizster has three flag bits: WDF, AF, and PF, which can generate an interrupt. These flags are set by the watchdog timeout, alarm match, or power fail monitor respectively.The processor can either poll this register or enable interrupts to be informed when a flag is set. These flags are automatically reset once the register is read. The flags register is automatically loaded with the value 00h on power up except for the OSCF bit. (See "Stopping and Starting the Oscillator" on page 6.)

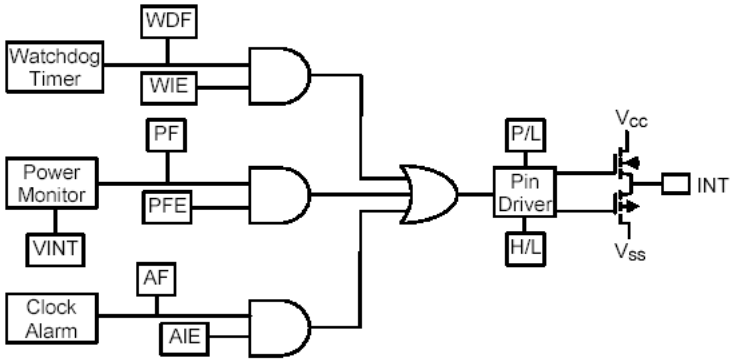
Figure 4. RTC Recommended Component Configuration



Recommended Values

Y1 = 32.768KHz
C_1 = 0
C_2 = 12 pF

Figure 5. Interrupt Block Diagram



Legend

WDF - Watchdog Timer Flag
WIE - Watchdog Interrupt Enable
PF - Power Fail Flag
PFE - Power Fail Enable
AF - Alarm Flag
AIE - Alarm Interrupt Enable
P/L - Pulse/Level
H/L - High/Low

Table 3. RTC Register Map[9, 10]

Register		BCD Format Data								Function/Range
CY14B104KA	CY14B104MA	D7	D6	D5	D4	D3	D2	D1	D0	
0x7FFFF	0x3FFFF	10s Years				Years				Years: 00–99
0x7FFFE	0x3FFFE	0	0	0	10s Months	Months				Months: 01–12
0x7FFFD	0x3FFFD	0	0	10s Day of Month		Day Of Month				Day of Month: 01–31
0x7FFFC	0x3FFFC	0	0	0	0	0	Day of week			Day of week: 01–07
0x7FFFB	0x3FFFB	0	0	10s Hours		Hours				Hours: 00–23
0x7FFFA	0x3FFFA	0	10s Minutes			Minutes				Minutes: 00–59
0x7FFF9	0x3FFF9	0	10s Seconds			Seconds				Seconds: 00–59
0x7FFF8	0x3FFF8	OSCEN	0	Cal Sign	Calibration					Calibration Values [11]
0x7FFF7	0x3FFF7	WDS	WDW	WDT						Watchdog [11]
0x7FFF6	0x3FFF6	WIE	AIE	PFE	0	H/L	P/L	0	0	Interrupts [11]
0x7FFF5	0x3FFF5	M	0	10s Alarm Date		Alarm Date				Alarm, Day of Month: 01–31
0x7FFF4	0x3FFF4	M	0	10s Alarm Hours		Alarm Hours				Alarm, Hours: 00–23
0x7FFF3	0x3FFF3	M	10s Alarm Minutes			Alarm Minutes				Alarm, Minutes: 00–59
0x7FFF2	0x3FFF2	M	10s Alarm Seconds			Alarm Seconds				Alarm, Seconds: 00–59
0x7FFF1	0x3FFF1	10s Centuries				Centuries				Centuries: 00–99
0x7FFF0	0x3FFF0	WDF	AF	PF	OSCF	0	CAL	W	R	Flags[11]

Note
9. 0 - Not implemented, reserved for future use.
10. Upper Byte D_{15}-D_8 (CY14B104MA) of RTC registers are reserved for future use
11. This is a binary value, not a BCD value.

Table 4. Register Map Detail

Register		Description							
CY14B104KA	CY14B104MA								
0x7FFFF	0x3FFFF	**Time Keeping - Years**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		10s Years				Years			
		Contains the lower two BCD digits of the year. Lower nibble (four bits) contains the value for years; upper nibble (four bits) contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0–99.							
0x7FFFE	0x3FFFE	**Time Keeping - Months**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	0	0	10s Month	Months			
		Contains the BCD digits of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1–12.							
0x7FFFD	0x3FFFD	**Time Keeping - Date**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	0	10s Day of Month		Day of Month			
		Contains the BCD digits for the date of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the 10s digit and operates from 0 to 3. The range for the register is 1–31. Leap years are automatically adjusted for.							
0x7FFFC	0x3FFFC	**Time Keeping - Day**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	0	0	0	0	Day of Week		
		Lower nibble (three bits) contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, because the day is not integrated with the date.							
0x7FFFB	0x3FFFB	**Time Keeping - Hours**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	0	10s Hours		Hours			
		Contains the BCD value of hours in 24 hour format. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0–23.							
0x7FFFA	0x3FFFA	**Time Keeping - Minutes**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	10s Minutes			Minutes			
		Contains the BCD value of minutes. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper minutes digit and operates from 0 to 5. The range for the register is 0–59.							
0x7FFF9	0x3FFF9	**Time Keeping - Seconds**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	10s Seconds			Seconds			
		Contains the BCD value of seconds. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper digit and operates from 0 to 5. The range for the register is 0–59.							

Table 4. Register Map Detail (continued)

Register		Description							
CY14B104KA	**CY14B104MA**								
0x7FFF8	**0x3FFF8**	**Calibration/Control**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		OSCEN	0	Calibration Sign	Calibration				
OSCEN		Oscillator Enable. When set to 1, the oscillator is stopped. When set to 0, the oscillator runs. Disabling the oscillator saves battery or capacitor power during storage.							
Calibration Sign		Determines if the calibration adjustment is applied as an addition (1) to or as a subtraction (0) from the time-base.							
Calibration		These five bits control the calibration of the clock.							
0x7FFF7	**0x3FFF7**	**WatchDog Timer**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		WDS	WDW	WDT					
WDS		Watchdog Strobe. Setting this bit to 1 reloads and restarts the watchdog timer. Setting the bit to 0 has no effect. The bit is cleared automatically after the watchdog timer is reset. The WDS bit is write only. Reading it always returns a 0.							
WDW		Watchdog Write Enable. Setting this bit to 1 disables any WRITE to the watchdog timeout value (D5–D0). This allows the user to set the watchdog strobe bit without disturbing the timeout value. Setting this bit to 0 allows bits D5–D0 to be written to the watchdog register when the next write cycle is complete. This function is explained in more detail in Watchdog Timer on page 7.							
WDT		Watchdog timeout selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32 Hz count (31.25 ms). The range of timeout value is 31.25 ms (a setting of 1) to 2 seconds (setting of 3 Fh). Setting the watchdog timer register to 0 disables the timer. These bits can be written only if the WDW bit was set to 0 on a previous cycle.							
0x7FFF6	**0x3FFF6**	**Interrupt Status/Control**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		WIE	AIE	PFE	0	H/L	P/L	0	0
WIE		Watchdog Interrupt Enable. When set to 1 and a watchdog timeout occurs, the watchdog timer drives the INT pin and the WDF flag. When set to 0, the watchdog timeout affects only the WDF flag.							
AIE		Alarm Interrupt Enable. When set to 1, the alarm match drives the INT pin and the AF flag. When set to 0, the alarm match only affects the AF flag.							
PFE		Power Fail Enable. When set to 1, the alarm match drives the INT pin and the PF flag. When set to 0, the power fail monitor affects only the PF flag.							
0		Reserved for future use							
H/L		High/Low. When set to 1, the INT pin is driven active HIGH. When set to 0, the INT pin is open drain, active LOW.							
P/L		Pulse/Level. When set to 1, the INT pin is driven active (determined by H/L) by an interrupt source for approximately 200 ms. When set to 0, the INT pin is driven to an active level (as set by H/L) until the flags register is read.							
0x7FFF5	**0x3FFF5**	**Alarm - Day**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	0	10s Alarm Date		Alarm Date			
		Contains the alarm value for the date of the month and the mask bit to select or deselect the date value.							
M		Match. When this bit is set to 0, the date value is used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the date value.							

Table 4. Register Map Detail (continued)

Register		Description							
CY14B104KA	CY14B104MA								
0x7FFF4	0x3FFF4	**Alarm - Hours**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	10s Alarm Hours			Alarm Hours			
		Contains the alarm value for the hours and the mask bit to select or deselect the hours value.							
M		Match. When this bit is set to 0, the hours value is used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the hours value.							
0x7FFF3	0x3FFF3	**Alarm - Minutes**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	10s Alarm Minutes			Alarm Minutes			
		Contains the alarm value for the minutes and the mask bit to select or deselect the minutes value.							
M		Match. When this bit is set to 0, the minutes value is used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the minutes value.							
0x7FFF2	0x3FFF2	**Alarm - Seconds**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	10s Alarm Seconds			Alarm Seconds			
		Contains the alarm value for the seconds and the mask bit to select or deselect the seconds' value.							
M		Match. When this bit is set to 0, the seconds value is used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the seconds value.							
0x7FFF1	0x3FFF1	**Time Keeping - Centuries**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		10s Centuries				Centuries			
		Contains the BCD value of centuries. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 9. The range for the register is 0-99 centuries.							
0x7FFF0	0x3FFF0	**Flags**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		WDF	AF	PF	OSCF	0	CAL	W	R
WDF		Watchdog Timer Flag. This read only bit is set to 1 when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to 0 when the Flags register is read or on power-up.							
AF		Alarm Flag. This read only bit is set to 1 when the time and date match the values stored in the alarm registers with the match bits = 0. It is cleared when the Flags register is read or on power-up.							
PF		Power Fail Flag. This read only bit is set to 1 when power falls below the power fail threshold V_{SWITCH}. It is cleared to 0 when the Flags register is read or on power-up.							
OSCF		Oscillator Fail Flag. Set to 1 on power up if the oscillator is enabled and not running in the first 5 ms of operation. This indicates that RTC backup power failed and clock value is no longer valid. The user must reset this bit to 0 to clear this condition (Flag). The chip does not clear this flag. This bit survives power cycles.							
CAL		Calibration Mode. When set to 1, a 512 Hz square wave is output on the INT pin. When set to 0, the INT pin resumes normal operation. This bit defaults to 0 (disabled) on power up.							
W		Write Enable: Setting the W bit to 1 freezes updates to the RTC registers and enables writes to RTC registers, Alarm registers, Calibration register, Interrupt register and OSCF bit of Flags register. Setting the W bit to 0 causes the contents of the RTC registers to be transferred to the clock counters if the time has been changed (a new base time is loaded). This bit defaults to 0 on power up.							
R		Read Enable: Setting R bit to 1, stops clock updates to user RTC registers so that clock updates are not seen during the reading process. Set R bit to 0 to resume clock updates to the holding register. This bit defaults to 0 on power up.							

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Maximum Accumulated Storage Time

.....At 150°C Ambient Temperature.....1000h

.....At 85°C Ambient Temperature..... 20 Years

Ambient Temperature with Power Applied ..... –55°C to +150°C

Supply Voltage on V_{CC} Relative to GND .....–0.5V to 4.1V

Voltage Applied to Outputs in High-Z State.....–0.5V to V_{CC} + 0.5V

Input Voltage.....–0.5V to Vcc + 0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential .....–2.0V to V_{CC} + 2.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Surface Mount Pb Soldering Temperature (3 Seconds)..... +260°C

DC Output Current (1 output at a time, 1s duration).....15 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	–40°C to +85°C	2.7V to 3.6V

DC Electrical Characteristics

Over the Operating Range (V_{CC} = 2.7V to 3.6V)

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{cc} Current	t_{RC} = 20 ns t_{RC} = 25 ns t_{RC} = 45 ns Values obtained without output loads (I_{OUT} = 0 mA)	Commercial		65 65 50	mA mA
			Industrial		70 70 52	mA mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Don't Care, V_{CC} = Max. Average current for duration t_{STORE}			10	mA
I_{CC3}[12]	Average V_{CC} Current at t_{RC} = 200 ns, 3V, 25°C typical	All I/P cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA).			35	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Don't Care, V_{CC} = Max. Average current for duration t_{STORE}			5	mA
I_{SB}	V_{CC} Standby Current	CE ≥ (V_{CC} – 0.2). All others V_{IN} ≤ 0.2V or ≥ (V_{CC} – 0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.			5	mA
I_{IX}[13]	Input Leakage Current (except HSB)	V_{CC} = Max, V_{SS} ≤ V_{IN} ≤ V_{CC}		–1	+1	µA
	Input Leakage Current (for HSB)	V_{CC} = Max, V_{SS} ≤ V_{IN} ≤ V_{CC}		–100	+1	µA
I_{OZ}	Off State Output Leakage Current	V_{CC} = Max, V_{SS} ≤ V_{OUT} ≤ V_{CC}, CE or OE ≥ V_{IH} or BHE/BLE ≥ V_{IH} or $\overline{WE}$ ≤ V_{IL}		–1	+1	µA
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –2 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 4 mA			0.4	V
V_{CAP}[14]	Storage Capacitor	Between V_{CAP} pin and V_{SS}, 5V Rated		61	180	µF

Notes

12. Typical conditions for the active current shown on the DC Electrical characteristics are average values at 25°C (room temperature), and V_{CC} = 3V. Not 100% tested.
13. The $\overline{HSB}$ pin has I_{OUT} = -2 uA for V_{OH} of 2.4V when both active HIGH and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.
14. V_{CAP} (Storage capacitor) nominal value is 68uF.

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data Retention	20	Years
NV_C	Nonvolatile STORE Operations	200	K

Capacitance

In the following table, the capacitance parameters are listed. [15]

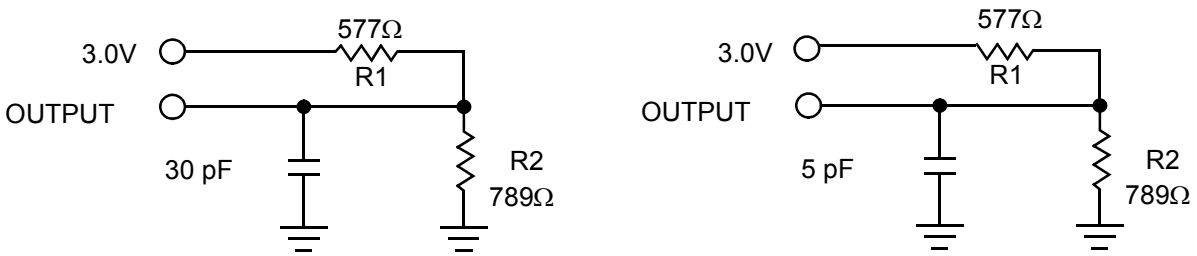
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0V	7	pF
C_{OUT}	Output Capacitance		7	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed.[15]

Parameter	Description	Test Conditions	44 TSOP II	54 TSOP II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	31.11	30.73	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		5.56	6.08	°C/W

Figure 6. AC Test Loads



AC Test Conditions

Input Pulse Levels .....0V to 3V
Input Rise and Fall Times (10% - 90%)..... ≤3 ns
Input and Output Timing Reference Levels 1.5V

Note
15. These parameters are guaranteed but not tested.

Table 5. RTC Characteristics

Parameters	Description	Test Conditions		Min	Max	Units
I_{BAK}[16]	RTC Backup Current		Commercial		300	nA
			Industrial		350	nA
V_{RTCbat}[17]	RTC Battery Pin Voltage			1.8	3.3	V
V_{RTCcap}[18]	RTC Capacitor Pin Voltage			1.5	3.6	V
tOCS	RTC Oscillator Time to Start	At Minimum Temperature from Power up or Enable			2	sec
		At 25°C Temperature from Power up or Enable			1	sec

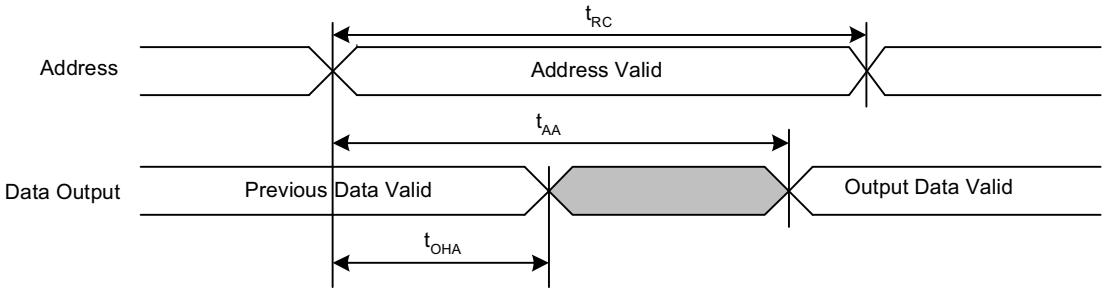
Notes
16. From either V_{RTCcap} or V_{RTCbat}.
17. Typical = 3.0V during normal operation.
18. Typical = 2.4V during normal operation.

AC Switching Characteristics

Parameters		Description	20 ns		25 ns		45 ns		Unit
Cypress Parameters	Alt Parameters		Min	Max	Min	Max	Min	Max	
SRAM Read Cycle									
t_{ACE}	t_{ACS}	Chip Enable Access Time		20		25		45	ns
t_{RC} [19]	t_{RC}	Read Cycle Time	20		25		45		ns
t_{AA} [20]	t_{AA}	Address Access Time		20		25		45	ns
t_{DOE}	t_{OE}	Output Enable to Data Valid		10		12		20	ns
t_{OHA} [20]	t_{OH}	Output Hold After Address Change	3		3		3		ns
t_{LZCE} [21]	t_{LZ}	Chip Enable to Output Active	3		3		3		ns
t_{HZCE} [21]	t_{HZ}	Chip Disable to Output Inactive		8		10		15	ns
t_{LZOE} [21]	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
t_{HZOE} [21]	t_{OHZ}	Output Disable to Output Inactive		8		10		15	ns
t_{PU} [15]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
t_{PD} [15]	t_{PS}	Chip Disable to Power Standby		20		25		45	ns
t_{DBE}	-	Byte Enable to Data Valid		10		12		20	ns
t_{LZBE}	-	Byte Enable to Output Active	0		0		0		ns
t_{HZBE}	-	Byte Disable to Output Inactive		8		10		15	ns
SRAM Write Cycle									
t_{WC}	t_{WC}	Write Cycle Time	20		25		45		ns
t_{PWE}	t_{WP}	Write Pulse Width	15		20		30		ns
t_{SCE}	t_{CW}	Chip Enable To End of Write	15		20		30		ns
t_{SD}	t_{DW}	Data Setup to End of Write	8		10		15		ns
t_{HD}	t_{DH}	Data Hold After End of Write	0		0		0		ns
t_{AW}	t_{AW}	Address Setup to End of Write	15		20		30		ns
t_{SA}	t_{AS}	Address Setup to Start of Write	0		0		0		ns
t_{HA}	t_{WR}	Address Hold After End of Write	0		0		0		ns
t_{HZWE} [21,22]	t_{WZ}	Write Enable to Output Disable		8		10		15	ns
t_{LZWE} [21]	t_{OW}	Output Active after End of Write	3		3		3		ns
t_{BW}	-	Byte Enable to End of Write	15		20		30		ns

Switching Waveforms

Figure 7. SRAM Read Cycle 1: Address Controlled[19, 20, 23]



Notes
19. WE must be HIGH during SRAM read cycles.
20. Device is continuously selected with CE, OE and BHE / BLE LOW.
21. Measured ±200 mV from steady state output voltage.
22. If WE is LOW when CE goes LOW, the outputs remain in the high impedance state.
23. HSB must remain HIGH during READ and WRITE cycles.

Switching Waveforms

Figure 8. SRAM Read Cycle 2: $\overline{CE}$ Controlled[3, 19, 23]

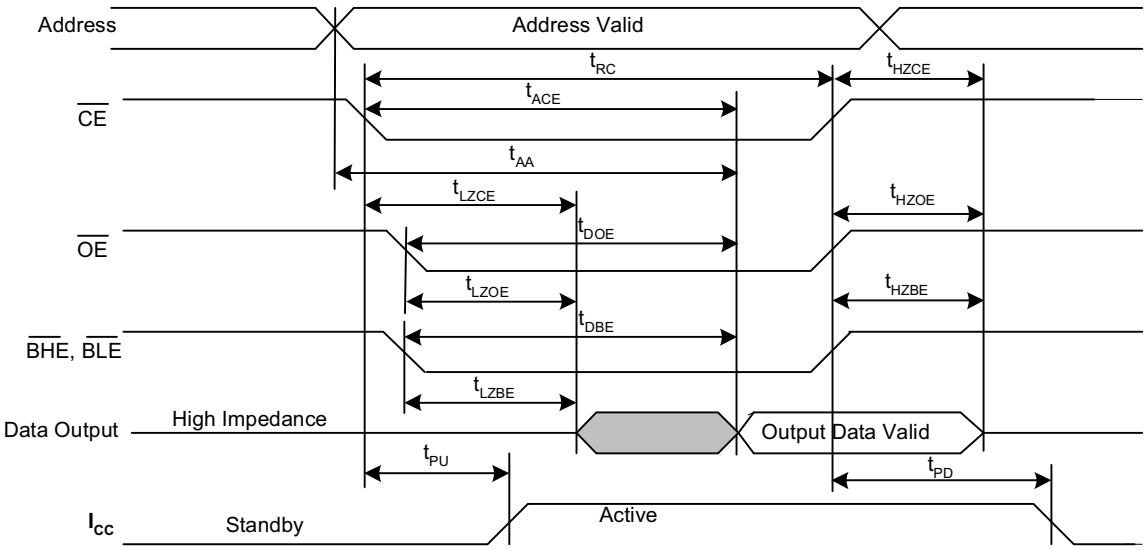
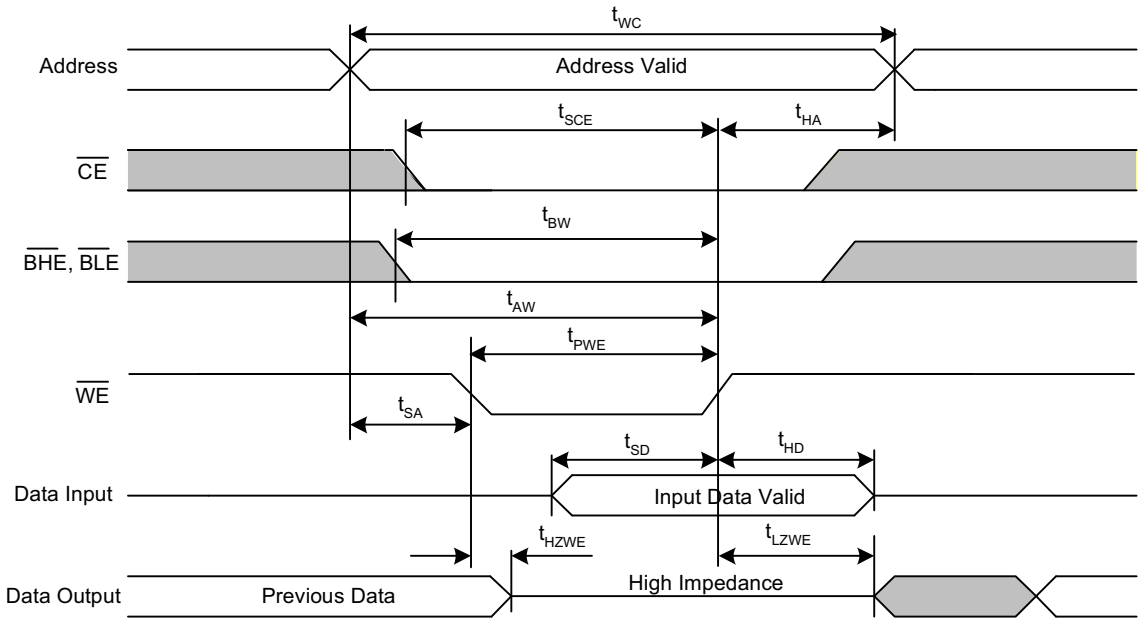


Figure 9. SRAM Write Cycle 1: $\overline{WE}$ Controlled[3, 22, 23, 24]



Notes
24. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

Switching Waveforms

Figure 10. SRAM Write Cycle 2: $\overline{CE}$ Controlled[3, 22, 23, 24]

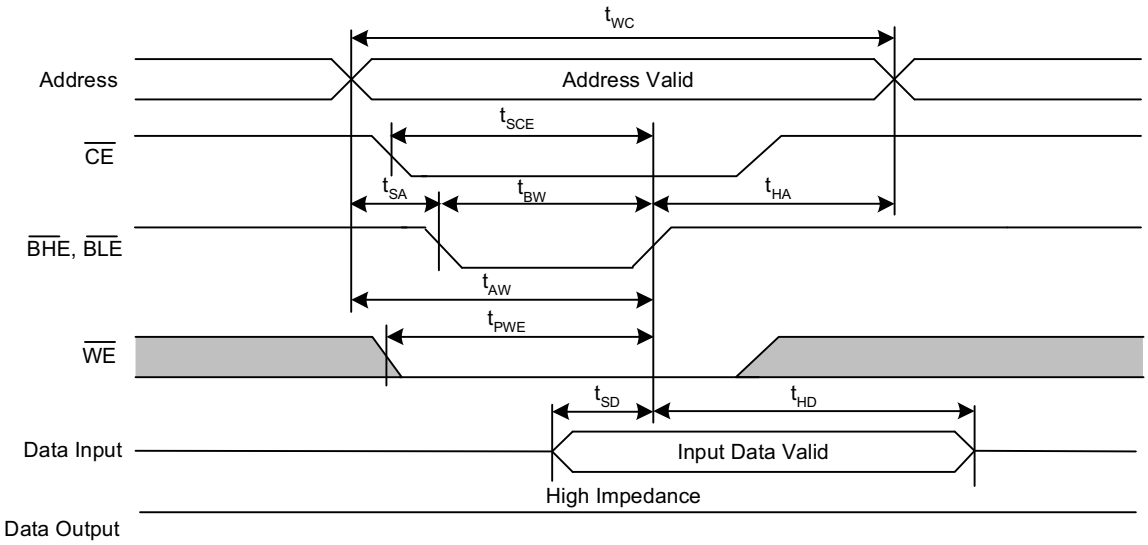
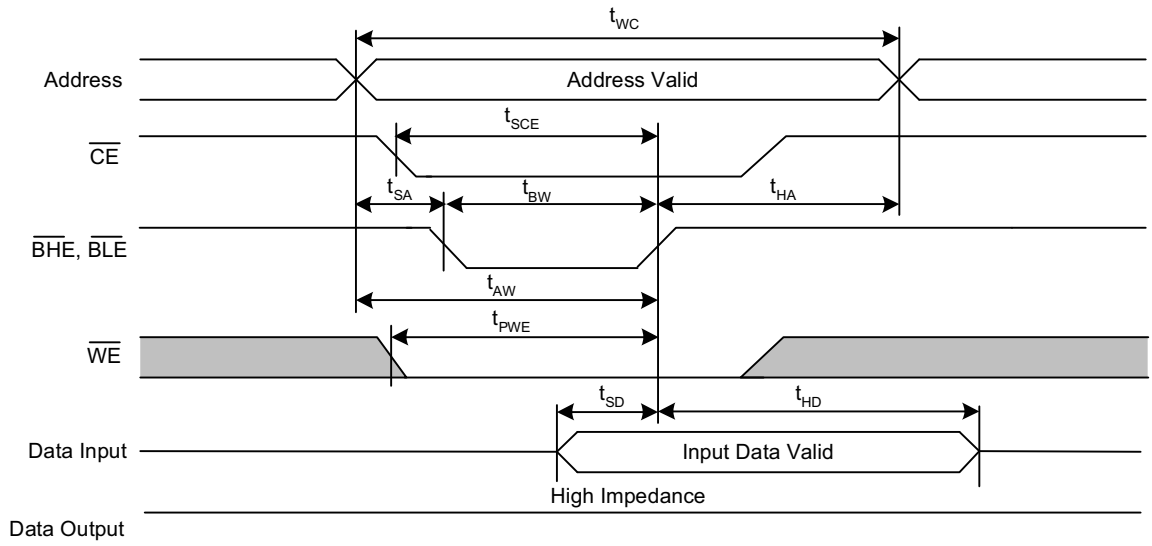


Figure 11. SRAM Write Cycle 3: $\overline{BHE}$ and $\overline{BLE}$ Controlled[6, 22, 23, 24]

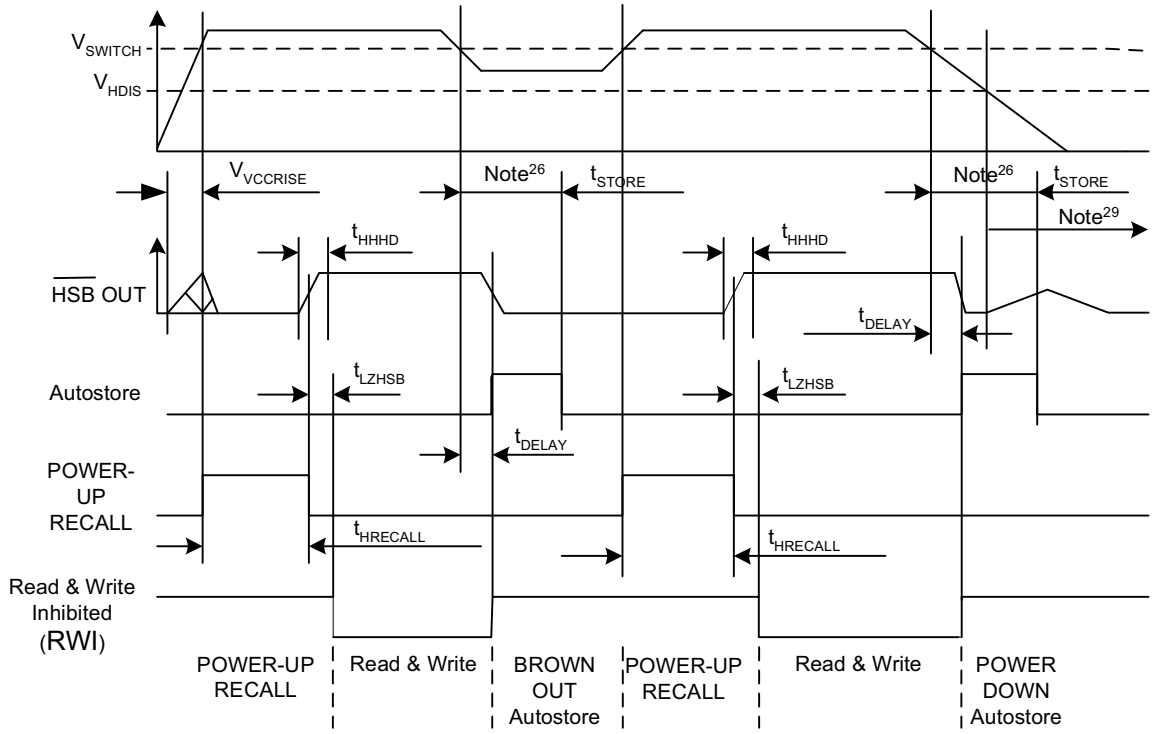


AutoStore/Power Up RECALL

Parameters	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
$t_{HRECALL}$ [25]	Power Up RECALL Duration		20		20		20	ms
t_{STORE} [26]	STORE Cycle Duration		8		8		8	ms
t_{DELAY} [27]	Time Allowed to Complete SRAM Cycle		20		25		25	ns
V_{SWITCH}	Low Voltage Trigger Level		2.65		2.65		2.65	V
$t_{VCCRISE}$	VCC Rise Time	150		150		150		µs
V_{HDIS} [15]	$\overline{HSB}$ Output Driver Disable Voltage		1.9		1.9		1.9	V
t_{LZHSB}	$\overline{HSB}$ To Output Active Time		5		5		5	µs
t_{HHHD}	$\overline{HSB}$ High Active Time		500		500		500	ns

Switching Waveforms

Figure 12. AutoStore or Power Up RECALL [28]



Notes

25. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
26. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware Store takes place.
27. On a Hardware STORE, Software Store / Recall, AutoStore Enable / Disable and AutoStore initiation, SRAM operation continues to be enabled for time t_{DELAY}.
28. Read and Write cycles are ignored during STORE, RECALL, and while VCC is below V_{SWITCH}.
29. HSB pin is driven HIGH to VCC only by internal 100kOhm resistor, HSB driver is disabled.

Software Controlled STORE and RECALL Cycle

In the following table, the software controlled STORE and RECALL cycle parameters are listed. [30, 31]

Parameters	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	STORE/RECALL Initiation Cycle Time	20		25		45		ns
t_{SA}	Address Setup Time	0		0		0		ns
t_{CW}	Clock Pulse Width	15		20		30		ns
t_{HA}	Address Hold Time	0		0		0		ns
t_{RECALL}	RECALL Duration		200		200		200	µs

Switching Waveforms

Figure 13. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE and RECALL Cycle[31]

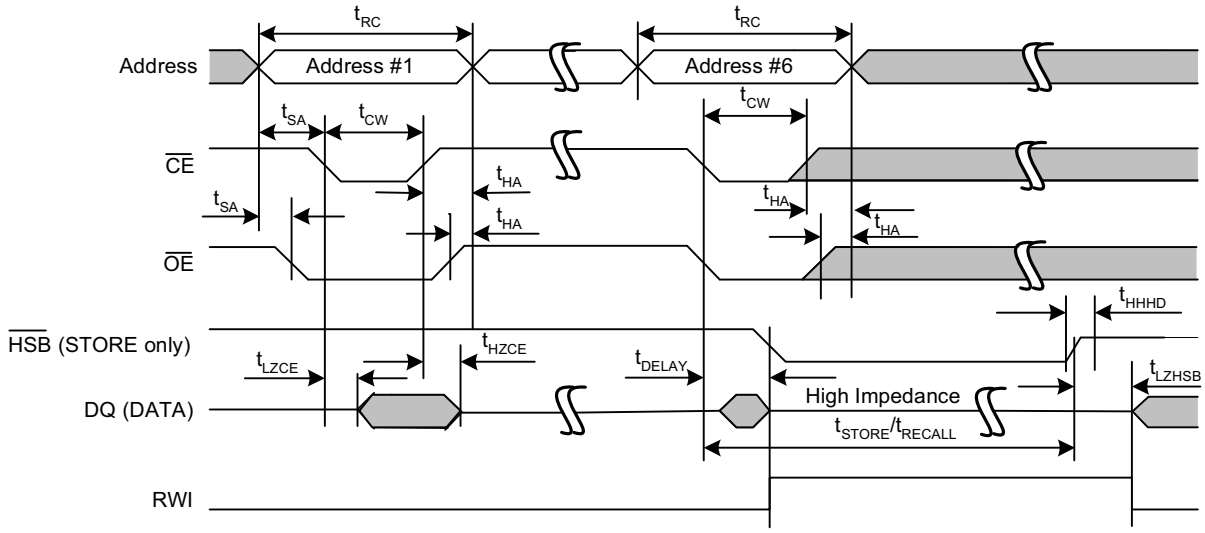
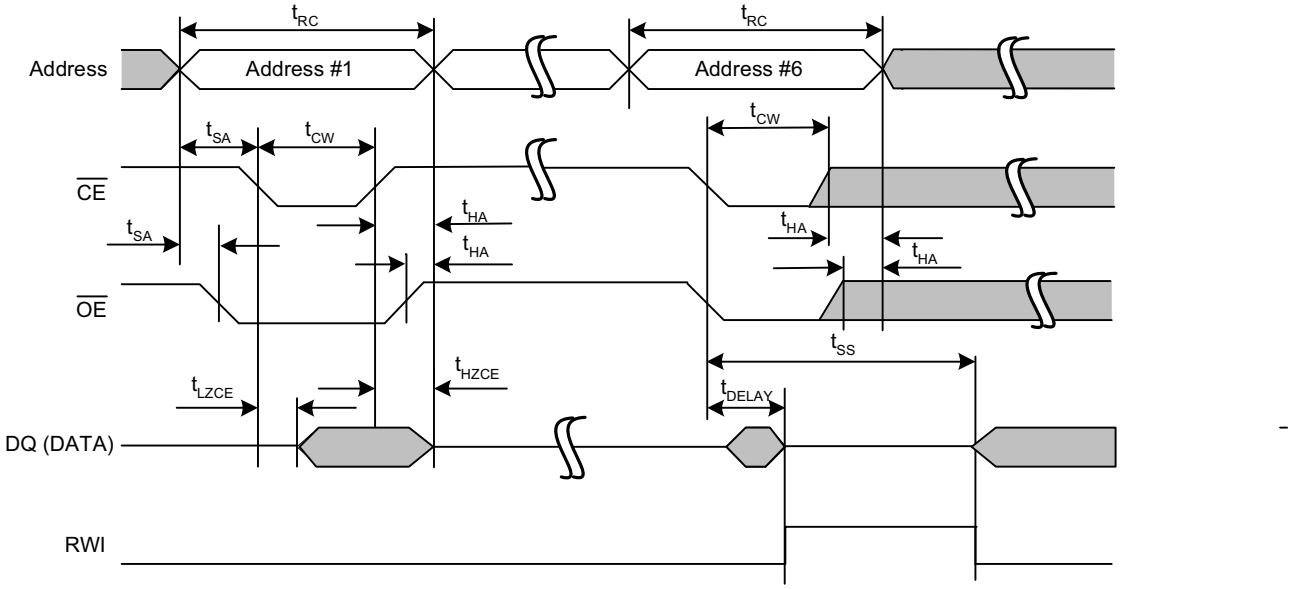


Figure 14. Autostore Enable and Disable Cycle



Notes

30. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
31. The six consecutive addresses must be read in the order listed in Table 1. $\overline{WE}$ must be HIGH during all six consecutive cycles.

Hardware STORE Cycle

Parameters	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{DHSB}	$\overline{HSB}$ To Output Active Time when write latch not set		20		25		25	ns
t_{PHSB}	Hardware STORE Pulse Width	15		15		15		ns
t_{SS} [32, 33]	Soft Sequence Processing Time		100		100		100	µs

Switching Waveforms

Figure 15. Hardware STORE Cycle[26]

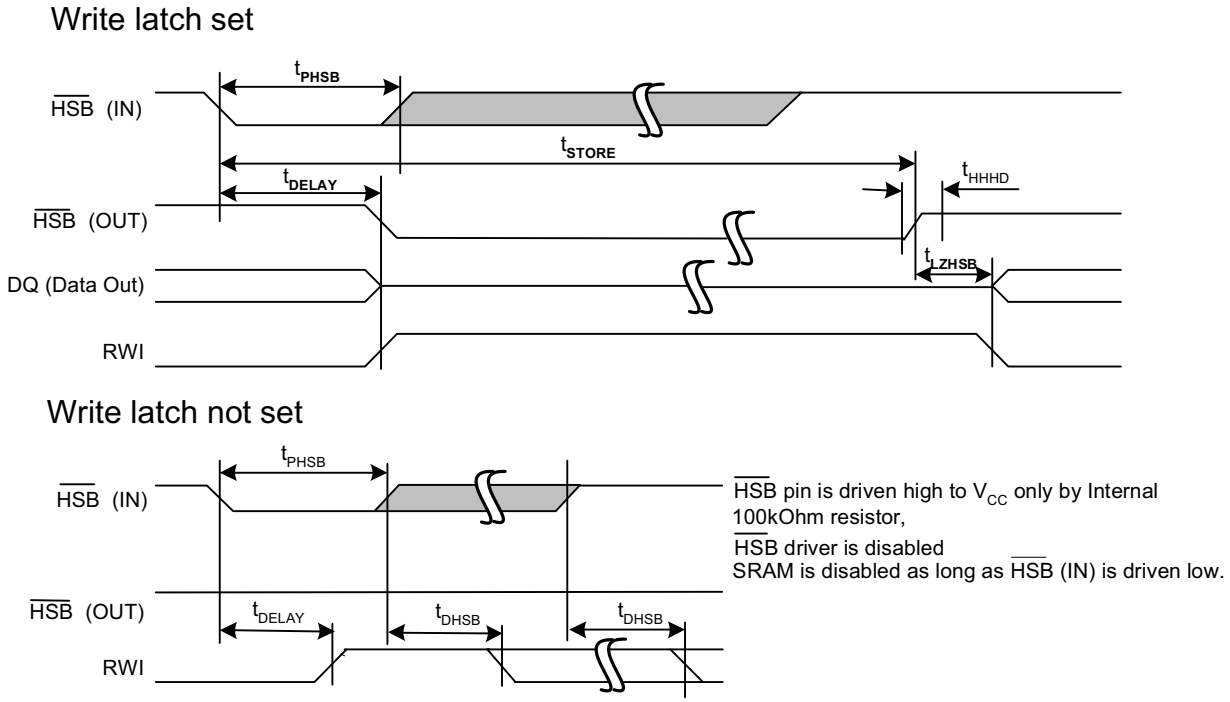
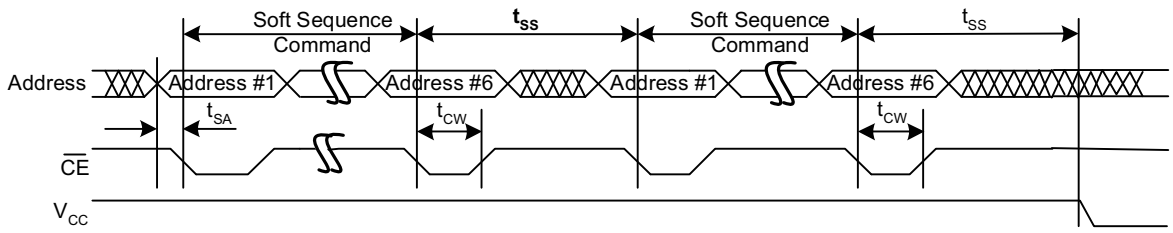


Figure 16. Soft Sequence Processing[32, 33]



Notes
32. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
33. Commands such as STORE and RECALL lock out IO until operation is complete which further increases this time. See the specific command.

Truth Table For SRAM Operations

$\overline{HSB}$ should remain HIGH for SRAM Operations.

For x8 Configuration

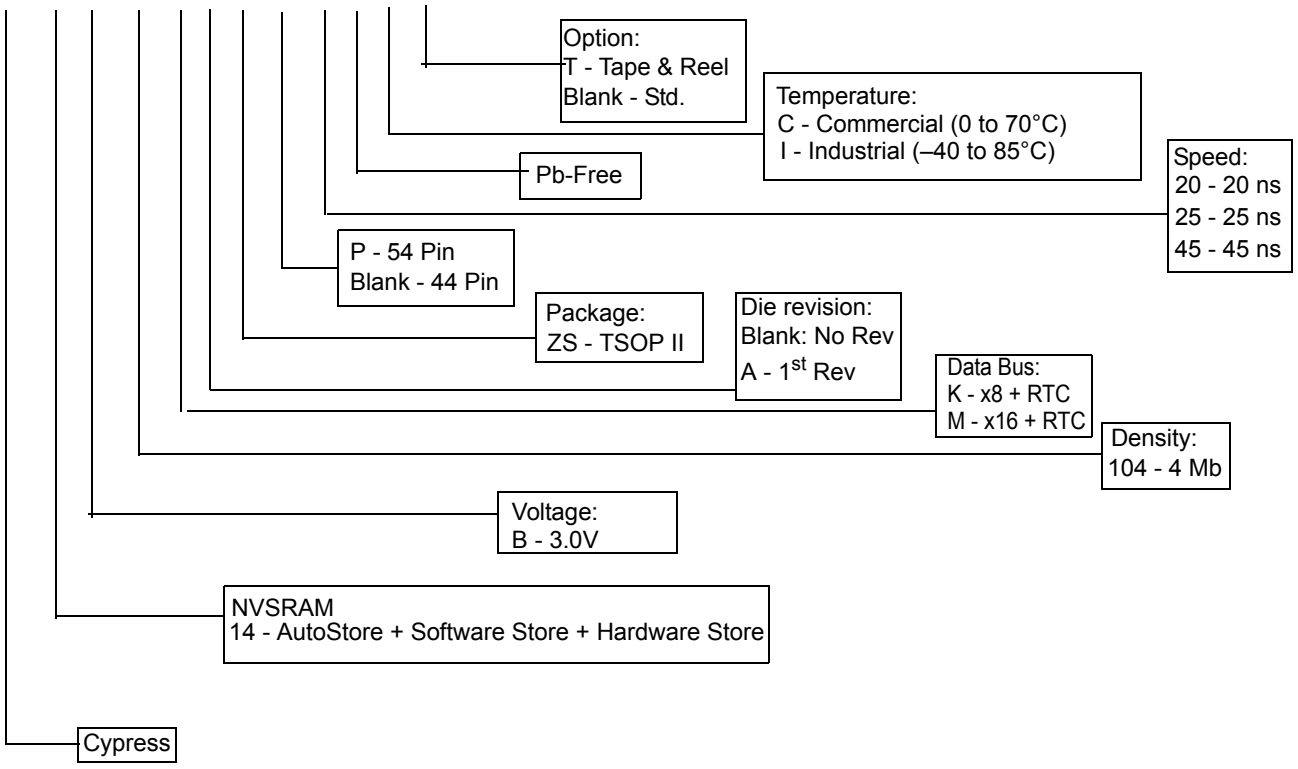
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs and Outputs[2]	Mode	Power
H	X	X	High Z	Deselect/Power down	Standby
L	H	L	Data Out (DQ_0–DQ_7);	Read	Active
L	H	H	High Z	Output Disabled	Active
L	L	X	Data in (DQ_0–DQ_7);	Write	Active

For x16 Configuration

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs and Outputs[2]	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power down	Standby
L	X	X	H	H	High-Z	Output Disabled	Active
L	H	L	L	L	Data Out (DQ_0–DQ_{15})	Read	Active
L	H	L	H	L	Data Out (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Read	Active
L	H	L	L	H	Data Out (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Read	Active
L	H	H	L	L	High-Z	Output Disabled	Active
L	H	H	H	L	High-Z	Output Disabled	Active
L	H	H	L	H	High-Z	Output Disabled	Active
L	L	X	L	L	Data In (DQ_0–DQ_{15})	Write	Active
L	L	X	H	L	Data In (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Write	Active
L	L	X	L	H	Data In (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Write	Active

Part Numbering Nomenclature

CY14 B 104 K A ZS P 20 X C T



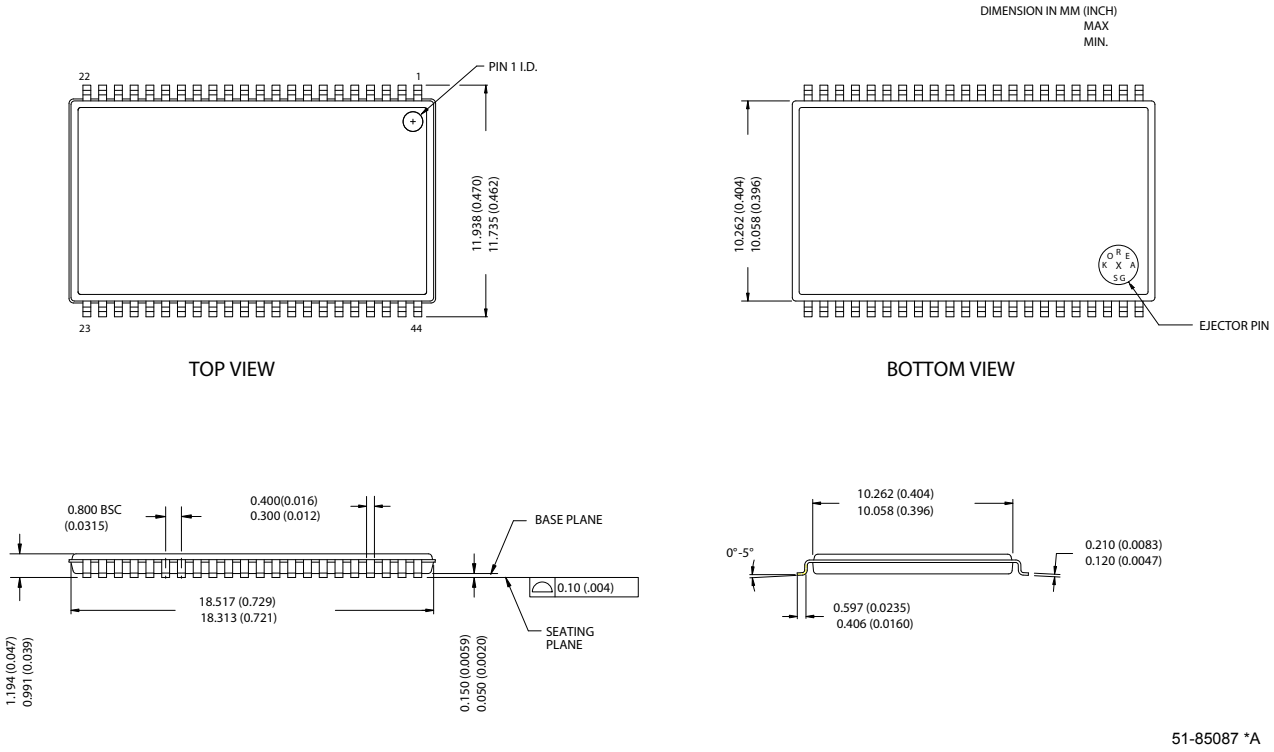
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
20	CY14B104KA-ZS20XCT	51-85087	44-pin TSOPII	Commercial
	CY14B104KA-ZS20XIT	51-85087	44-pin TSOPII	Industrial
	CY14B104KA-ZS20XI	51-85087	44-pin TSOPII	
	CY14B104MA-ZS20XCT	51-85087	44-pin TSOPII	Commercial
	CY14B104MA-ZS20XIT	51-85087	44-pin TSOPII	Industrial
	CY14B104MA-ZS20XI	51-85087	44-pin TSOPII	
	CY14B104KA-ZSP20XCT	51-85160	54-pin TSOPII	Commercial
	CY14B104KA-ZSP20XIT	51-85160	54-pin TSOPII	Industrial
	CY14B104KA-ZSP20XI	51-85160	54-pin TSOPII	
	CY14B104MA-ZSP20XCT	51-85160	54-pin TSOPII	Commercial
	CY14B104MA-ZSP20XIT	51-85160	54-pin TSOPII	Industrial
	CY14B104MA-ZSP20XI	51-85160	54-pin TSOPII	
25	CY14B104KA-ZS25XCT	51-85087	44-pin TSOPII	Commercial
	CY14B104KA-ZS25XIT	51-85087	44-pin TSOPII	Industrial
	CY14B104KA-ZS25XI	51-85187	44-pin TSOPII	
	CY14B104MA-ZS25XCT	51-85087	44-pin TSOPII	Commercial
	CY14B104MA-ZS25XIT	51-85087	44-pin TSOPII	Industrial
	CY14B104MA-ZS25XI	51-85087	44-pin TSOPII	
	CY14B104KA-ZSP25XCT	51-85160	54-pin TSOPII	Commercial
	CY14B104KA-ZSP25XIT	51-85160	54-pin TSOPII	Industrial
	CY14B104KA-ZSP25XI	51-85160	54-pin TSOPII	
	CY14B104MA-ZSP25XCT	51-85160	54-pin TSOPII	Commercial
	CY14B104MA-ZSP25XIT	51-85160	54-pin TSOPII	Industrial
	CY14B104MA-ZSP25XI	51-85160	54-pin TSOPII	
45	CY14B104KA-ZS45XCT	51-85087	44-pin TSOPII	Commercial
	CY14B104KA-ZS45XIT	51-85087	44-pin TSOPII	Industrial
	CY14B104KA-ZS45XI	51-85187	44-pin TSOPII	
	CY14B104MA-ZS45XCT	51-85087	44-pin TSOPII	Commercial
	CY14B104MA-ZS45XIT	51-85087	44-pin TSOPII	Industrial
	CY14B104MA-ZS45XI	51-85087	44-pin TSOPII	
	CY14B104KA-ZSP45XCT	51-85160	54-pin TSOPII	Commercial
	CY14B104KA-ZSP45XIT	51-85160	54-pin TSOPII	Industrial
	CY14B104KA-ZSP45XI	51-85160	54-pin TSOPII	
	CY14B104MA-ZSP45XCT	51-85160	54-pin TSOPII	Commercial
	CY14B104MA-ZSP45XIT	51-85160	54-pin TSOPII	Industrial
	CY14B104MA-ZSP45XI	51-85160	54-pin TSOPII	

All parts are Pb-free. The above table contains Preliminary information. Please contact your local Cypress sales representative for availability of these parts.

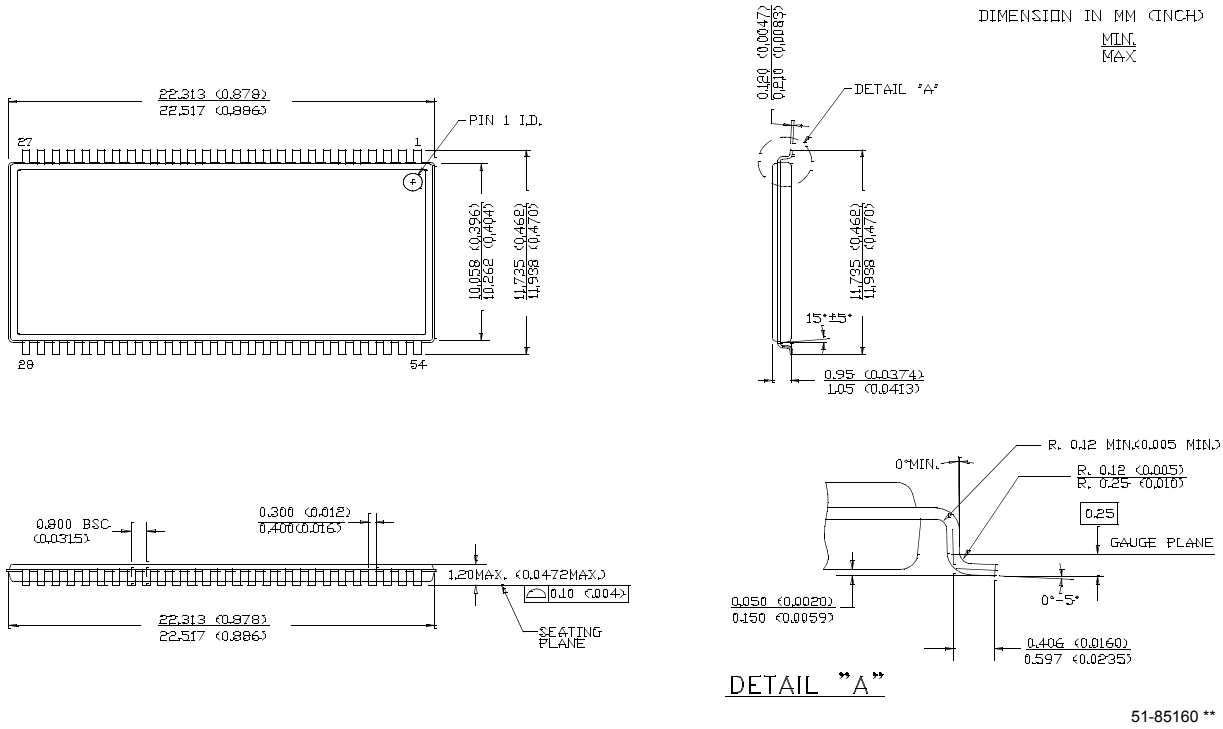
Package Diagrams

Figure 17. 44-Pin TSOP II (51-85087)



Package Diagrams (continued)

Figure 18. 54-Pin TSOP II (51-85160)



Document History Page

Document Title: CY14B104KA/CY14B104MA 4 Mbit (512K x 8/256K x 16) nvSRAM with Real-Time-Clock Document Number: 001-07103				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	431039	See ECN	TUP	New Data Sheet
*A	489096	See ECN	TUP	Removed 48 SSOP Package Added 44 TSOPII and 54 TSOPII Packages Updated Part Numbering Nomenclature and Ordering Information Added Soft Sequence Processing Time Waveform Added RTC Characteristics Table Added RTC Recommended Component Configuration
*B	499597	See ECN	PCI	Removed 35ns speed bin Added 55ns speed bin. Updated AC table for the same Changed “Unlimited” read/write to “infinite” read/write Features section: Changed typical I_{CC} at 200-ns cycle time to 8 mA Changed STORE cycles from 500K to 200K cycles. Shaded Commercial grade in operating range table. Modified Icc/Isb specs. Changed V_{CAP} value in DC table Added 44 TSOP II in Thermal Resistance table Modified part nomenclature table. Changes reflected in the ordering information table.
*C	517793	See ECN	TUP	Removed 55ns speed bin Changed pinout for 44TSOPII and 54TSOPII packages Changed I_{SB} to 1mA Changed I_{CC4} to 3mA Changed V_{CAP} min to 35µF Changed V_{IH} max to Vcc + 0.5V Changed t_{STORE} to 15ns Changed t_{PWE} to 10ns Changed t_{SCE} to 15ns Changed t_{SD} to 5ns Changed t_{AW} to 10ns Removed t_{HLBL} Added Timing Parameters for $\overline{BHE}$ and $\overline{BLE}$ - t_{DBE}, t_{LZBE}, t_{HZBE}, t_{BW} Removed min. specification for Vswitch Changed t_{GLAX} to 1ns Added t_{DELAY} max. of 70us Changed t_{SS} specification from 70us min. to 70us max.
*D	825240	See ECN	UHA	Changed the data sheet from Advance information to Preliminary Changed t_{DBE} to 10ns in 15ns part Changed t_{HZBE} in 15ns part to 7ns and in 25ns part to10ns Changed t_{BW} in 15ns part to 15ns and in 25ns part to 20ns Changed t_{GLAX} to t_{GHAX} Changed the value of I_{CC3} to 25mA Changed the value of t_{AW} in 15ns part to 15ns
*E	914280	See ECN	UHA	Changed the figure-14 title from 54-Pb to 54 Pin Included all the information for 45ns part in this data sheet

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Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*F	1890926	See ECN	vsutmp8/AE-SA	Added Footnote 1, 2 and 3. Updated Logic Block diagram Updated Pin definition Table Changed 8Mb Address expansion Pin from Pin 43 to Pin 42 for 44-TSOP II (x8) package. Corrected typo in V_{IL} min spec Changed the value of I_{CC3} from 25mA to 13mA Changed I_{SB} value from 1mA to 2mA Updated ordering information table Rearranging of Footnotes. Changed Package diagrams title. The pins X1 and X2 interchanged in 44TSOP II(x8) and 54TSOP II(x16) pinout diagram.
*G	2267286	See ECN	GVCH/PYRS	Rearranging of “Features” Added $\overline{BHE}$ and $\overline{BLE}$ Information in Pin Definitions Table Updated Figure 2 (Autostore mode) Updated footnote 6 RTC Register Map:Register 0x1FFF6:Changed D4 from ABE to 0 Register Map Detail:0x1FFF6:Changed D4 from ABE to 0 and removed ABE information Changed I_{CC2} & I_{CC4} from 3mA to 6mA Changed I_{CC3} from 13mA to 15mA Changed I_{SB} from 2mA to 3mA Added input leakage current (I_{IX}) for $\overline{HSB}$ in DC Electrical Characteristics table Changed Vcap from 35uF min and 57uF max value to 54uF min and 82uF max value Corrected typo in t_{DBE} value from 22ns to 20ns for 45ns part Corrected typo in t_{HZBE} value from 22ns to 15ns for 45ns part Corrected typo in t_{AW} value from 15ns to 10ns for 15ns part Changed Vrtccap max from 2.7V to 3.6V Changed tRECALL from 100 to 200us Added footnote 10, 29 Reframed footnote 18, 25 Added footnote 18 to figure 8 (SRAM WRITE Cycle #1) Added footnote 18, 26 and 27 to figure 9 (SRAM WRITE Cycle #2)
*H	2483627	See ECN	GVCH/PYRS	Removed 8 mA typical I_{CC} at 200 ns cycle time in Feature section Referenced footnote 9 to I_{CC3} in DC Characteristics table Changed I_{CC3} from 15 mA to 35 mA Changed Vcap minimum value from 54 uF to 61 uF Changed t_{AVAV} to t_{RC} Changed V_{RTCcap} minimum value from 1.2V to 1.5V Figure 12:Changed t_{SA} to t_{AS} and $t_{SCE\ to}$ t_{CW}

Document Title: CY14B104KA/CY14B104MA 4 Mbit (512K x 8/256K x 16) nvSRAM with Real-Time-Clock Document Number: 001-07103				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*I	2519319	06/20/08	GVCH/PYRS	Added 20 ns access speed in “Features” Added I_{CC1} for tRC=20 ns for both industrial and Commercial temperature Grade Updated Thermal resistance values for 44-TSOP II and 54-TSOP II packages Added AC Switching Characteristics specs for 20 ns access speed Added Software controlled STORE/RECALL cycle specs for 20 ns access speed Updated ordering information and Part numbering nomenclature
*J	2600941	11/04/08	GVCH/PYRS	Removed 15 ns access speed from “Features” Changed part number from CY14B104K/CY14B104M to CY14B104KA/CY14B104MA Updated Logic block diagram Updated footnote 1 Added footnote 2 Pin definition: Updated $\overline{WE}$, $\overline{HSB}$ and NC pin description Page 4: Updated SRAM READ, SRAM WRITE, Autostore operation description Page 4: Updated Hardware store operation and Hardware RECALL (Power-up) description Footnote 1 and 8 referenced for Mode selection Table Updated footnote 6 Page 6: updated Data protection description Page 6: Updated Starting and stopping the oscillator description Page 7: Updated Calibrating the clock description Page 7: Updated Alarm description Page 8: Added Flags register Added footnote 10 and 11 Updated Figure 4: Removed RF register and Changed C_2 value from 56pF to 12pF Updated Register Map Table 3 Updated Register map detail Table 4 Maximum Ratings: Added Max. Accumulated storage time Changed Output short circuit current parameter name to DC output current Changed I_{CC2} from 6mA to 10mA Changed I_{CC4} from 6mA to 5mA Changed I_{SB} from 3mA to 5mA Updated I_{CC1}, I_{CC3}, I_{SB} and I_{OZ} Test conditions Changed V_{CAP} voltage max value from 82uF to 180uF Updated footnote 12 and 13 Added footnote 14 Added Data retention and Endurance Table Updated Input Rise and Fall time in AC test Conditions Changed tOCS value for minimum teperature from 10 to 2 sec updated tOCS value for room temperature from 5 to 1sec Referenced footnote 20 to t_{OHA} parameter Updated All switching waveforms Updated footnote 20 Added Figure 11 (SRAM WRITE CYCLE:$\overline{BHE}$ and $\overline{BLE}$ controlled) Updated t_{DELAY} value Added V_{HDIS}, t_{HHHD} and t_{LZHSB} parameters Updated footnote 27 Added footnote 29 Software controlled STORE/RECALL Table: Changed t_{AS} to t_{SA} Changed t_{GHAX} to t_{HA} Changed t_{HA} value from 1ns to 1ns Added t_{DHSB} parameter Changed t_{HLHX} to t_{PHSB} Updated t_{SS} from 70us to 100us Added truth table for SRAM operations Updated ordering information and part numbering nomenclature

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