

# AM42-0041

GaAs MMIC VSAT Power Amplifier, 0.5 W  
14.0 - 14.5 GHz

Rev. V4

## Features

- High Linear Gain: 28 dB Typ.
- High Saturated Output Power: +28 dBm Typ.
- High Power Added Efficiency: 22% Typ.
- 50  $\Omega$  Input/Output Broadband Matched
- Lead-Free Ceramic Bolt Down Package
- RoHS\* Compliant and 260°C Reflow Compatible

## Description

M/A-COM's AM42-0041 is a four-stage MMIC linear power amplifier in a lead-free, ceramic bolt down style hermetic package. The AM42-0041 employs a fully matched chip with internally decoupled Gate and Drain bias networks. The AM42-0041 is designed to be operated from a constant current Drain supply. By varying the Gate bias voltage, the saturated output power performance of this device can be tailored for various applications.

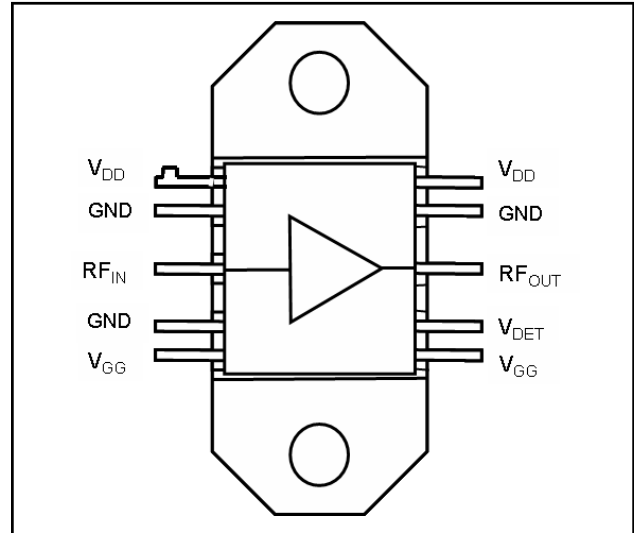
The AM42-0041 is ideally suited for use as an output stage or driver, in applications for VSAT systems. This design is fully monolithic and requires a minimum of external components.

M/A-COM's AM42-0041 is fabricated using a mature 0.5 micron GaAs MESFET process. The process features full passivation for increased performance and reliability. This product is 100% RF tested to ensure compliance to performance specifications.

## Ordering Information

Part Number	Package
AM42-0041	Ceramic Bolt Down Package

## Functional Schematic



## Pin Configuration

Pin No.	Pin Name	Description
1	V <sub>DD</sub>	Drain Supply
2	GND	DC and RF Ground
3	RF In	RF Input
4	GND	DC and RF Ground
5	V <sub>GG</sub>	Gate Supply
6	V <sub>GG</sub>	Gate Supply
7	V <sub>DET</sub>	Detector
8	RF Out	RF Output
9	GND	DC and RF Ground
10	V <sub>DD</sub>	Drain Supply

\* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

## GaAs MMIC VSAT Power Amplifier, 0.5 W 14.0 - 14.5 GHz

Rev. V4

**Electrical Specifications:  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = +8\text{ V}$ ,  $V_{GG}$  adjusted for  $I_{DS} = 500\text{ mA}$ ,  $Z_0 = 50\ \Omega$**

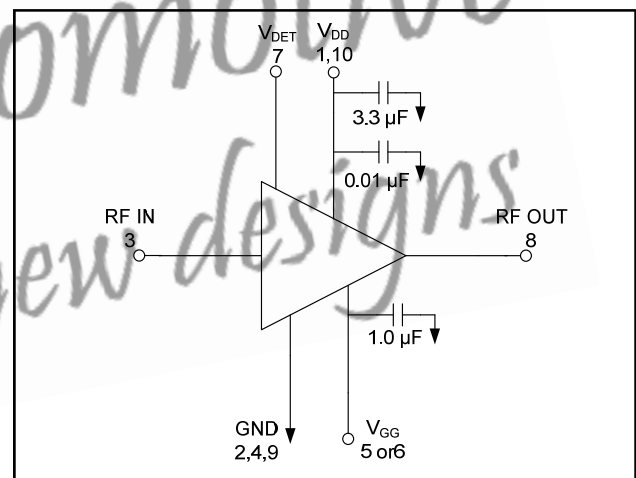
Parameter	Test Conditions	Units	Min.	Typ.	Max.
Linear Gain	$P_{IN} \leq -10\text{ dBm}$	dB	27	28	—
Input VSWR	$P_{IN} \leq -10\text{ dBm}$	Ratio	—	2.5:1	2.7:1
Output VSWR	$P_{IN} \leq -10\text{ dBm}$	Ratio	—	2.5:1	—
Saturated Output Power	$P_{IN} = +3\text{ dBm}$ , $I_{DD} = 500\text{ mA Typ.}$	dBm	27	28	29
Output Power Flatness vs. Frequency	$P_{IN} = +3\text{ dBm}$ , $I_{DD} = 500\text{ mA Typ.}$	dB	—	1.0	1.5
Output Power vs. Temperature (with respect to $T_A = +25^\circ\text{C}$ )	$P_{IN} = +3\text{ dBm}$ , $I_{DD} = 500\text{ mA Typ.}$ $T_A = -40^\circ\text{C to } +70^\circ\text{C}$	dB	—	$\pm 0.4$	—
Noise Figure	$P_{IN} \leq -10\text{ dBm}$ , $I_{DD} = 500\text{ mA Typ.}$	dB	—	7	—
Drain Bias Current	$P_{IN} = +3\text{ dBm}$	mA	400	500	600
Gate Bias Voltage	$P_{IN} = +3\text{ dBm}$ , $I_{DS} = 500\text{ mA Typ.}$	V	-2.4	-1.0	-0.4
Gate Bias Current	$P_{IN} = +3\text{ dBm}$ , $I_{DS} = 500\text{ mA Typ.}$	mA	—	5	15
Thermal Resistance	$25^\circ\text{C Heat Sink}$	$^\circ\text{C/W}$	—	9.5	—
Power Added Efficiency	$P_{IN} = +3\text{ dBm}$ , $I_{DS} = 500\text{ mA Typ.}$	%	—	22	—
$V_{DET}$	$P_{IN} = +3\text{ dBm}$ , $I_{DS} = 500\text{ mA}$	V	1	—	—

### Absolute Maximum Ratings <sup>1,2,3</sup>

Parameter	Absolute Maximum
Input Power	+23 dBm
$V_{DD}$	+12 Volts
$V_{GG}$	-3 Volts
$V_{DD} - V_{GG}$	12 Volts
$I_{ds}$	1000 mA
Channel Temperature	$-40^\circ\text{C to } +85^\circ\text{C}$
Storage Temperature	$-65^\circ\text{C to } 150^\circ\text{C}$

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Case Temperature (TC) =  $+85^\circ\text{C}$

### Application Schematic <sup>4,5,6,7,8</sup>



- Nominal bias is obtained by first connecting -2.4 volts to pin 5 or pin 6 (VGG), followed by connecting +8 volts to pin 1 or pin 10 (VDD). Note sequence. Adjust VGG for a drain current of 500 mA typical.
- RF ground and thermal interface is the flange (case bottom). Adequate heat sinking is required.
- No DC bias voltage appears at the RF ports.
- No DC resistance at the input and output ports is a short circuit. No voltage is allowed on these ports.
- For optimum IP3 performance, the VDD bypass capacitors should be placed within 0.5 inches of the  $V_{DD}$  leads.

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**ADVANCED:** Data Sheets contain information regarding a product M/A-COM Technology Solutions is considering for development. Performance is based on target specifications, simulated results, and/or prototype measurements. Commitment to develop is not guaranteed.

**PRELIMINARY:** Data Sheets contain information regarding a product M/A-COM Technology Solutions has under development. Performance is based on engineering tests. Specifications are typical. Mechanical outline has been fixed. Engineering samples and/or test data may be available. Commitment to produce in volume is not guaranteed.

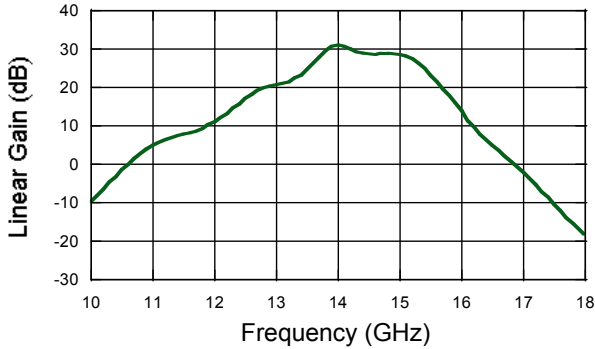
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Visit [www.macomtech.com](http://www.macomtech.com) for additional data sheets and product information.

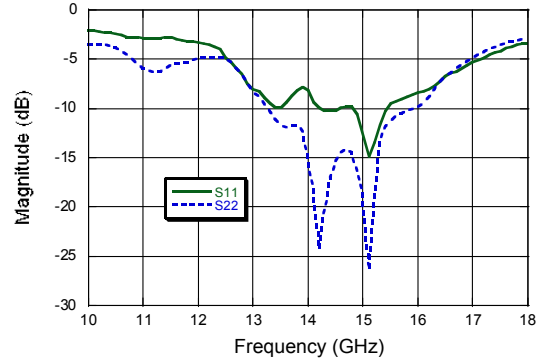
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## Typical Performance Curves @ +25°C

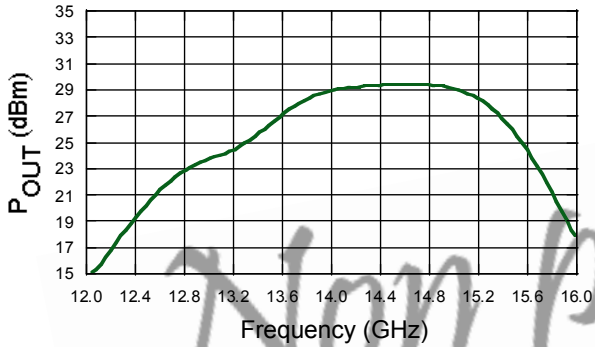
Linear Gain vs. Frequency



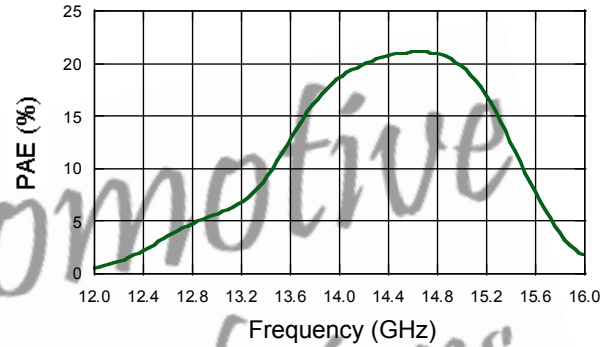
Input and Output Return Loss vs. Frequency



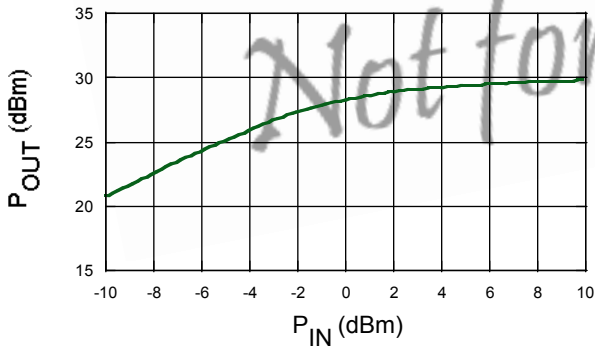
Output Power vs. Frequency @  $P_{IN} = +3$  dBm



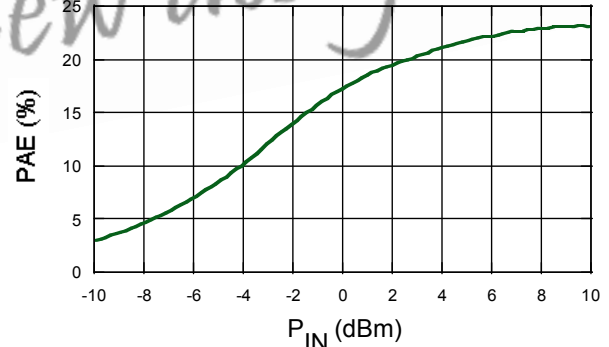
PAE vs. Frequency @  $P_{IN} = +3$  dBm



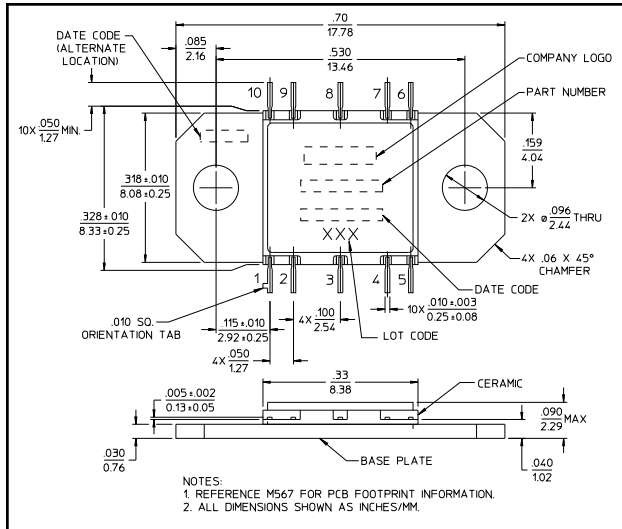
Output Power vs. Input Power @ 14.25 GHz



PAE vs. Input Power @ 14.25 GHz



## Lead-Free CR-15†



† Reference Application Note M538 for lead-free solder reflow recommendations.

Meets JEDEC moisture sensitivity level 1 requirements.

## Handling Procedures

Please observe the following precautions to avoid damage:

## Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

*Non promotive  
Not for new designs*