SONY

High-speed Buffer Amplifier for CCD Image Sensor

CXA3741AUR

Description

The CXA3741UR is a high-speed buffer amplifier IC with built-in switches.
(Applications: CCD image sensor output buffers, digital still cameras, camcorders, other general buffers)

Features

- Power consumption: 26 mW (typ.)
  (IDRV = 50μA (220kΩ when V_{CC} = 15V), ISF current = 0, during no signal)
- Push-pull output
- High-speed response: 500 V/μs (IDRV = 50μA (220kΩ when V_{CC} = 15V), C_L = 20pF)
- Internal sink current mode for CCD source follower output. Settable by external resistance R_{ISF}
- Sink current and drive current with each built-in switch. Each current value can be set by an external resistance.

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

(Ta = 25°C)

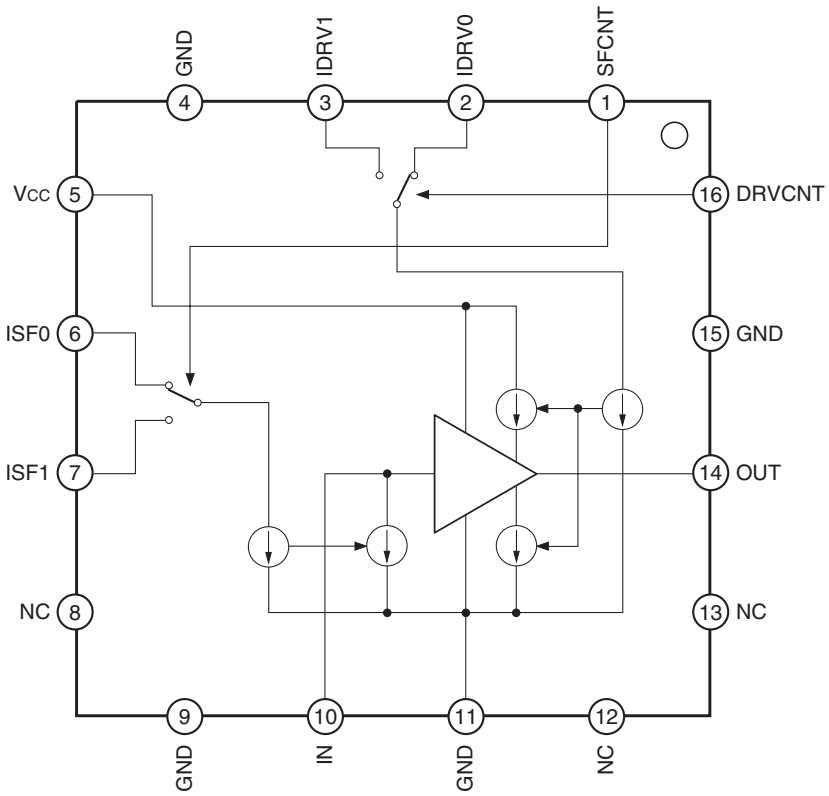
• Supply voltage	V_{CC}	16	V
• Input voltage	IN	GND – 0.3 to V_{CC} + 0.3	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	0.73	W
		(when mounted on a two-layer board; 30mm × 30mm, t = 0.8mm)	

Recommended Operating Conditions

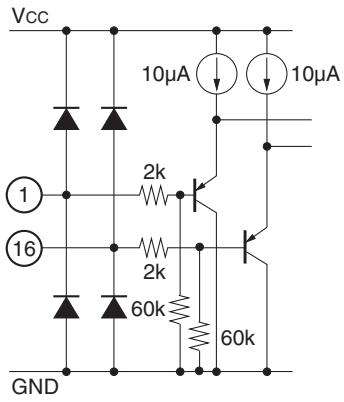
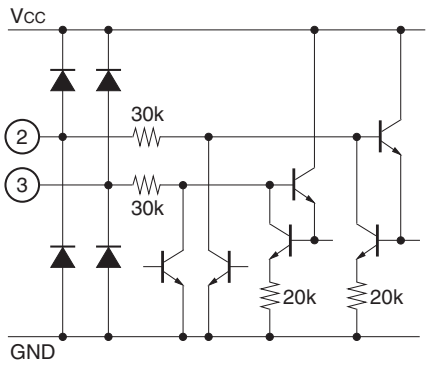
• Supply voltage	V_{CC}	9 to 15.5	V
• Operating temperature	Ta	–20 to +75	°C

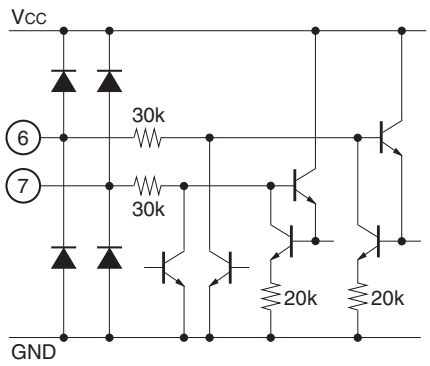
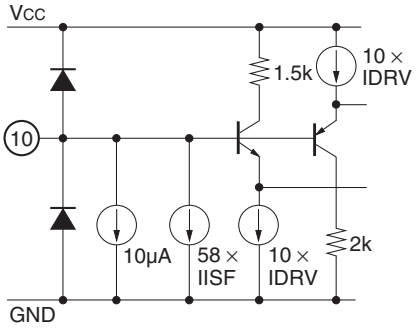
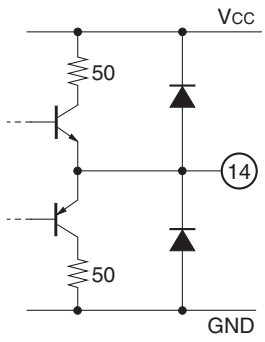
E07711

Block Diagram and Pin Description



Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
4	GND	—	0V	—	GND
5	Vcc	—	15V	—	Power supply
9	GND	—	0V	—	GND
11	GND	—	0V	—	GND
15	GND	—	0V	—	GND
1	SFCNT	I	CMOS		Switches the sink current setting for CCD with open source output. When the SFCNT pin (Pin 16) input logic is low, the sink current is set according to the current set by the ISF0 pin (Pin 6). When high, the sink current is set according to the current set by the ISF1 pin (Pin 7).
16	DRVCNT	I	CMOS		Switches the drive current setting. When the DRVCNT pin (Pin 16) input logic is low, the drive current is set according to the current set by the IDRV0 pin (Pin 2). When high, the drive current is set according to the current set by the IDRV1 pin (Pin 3).
2	IDRV0	I	—		External resistor connection for setting the drive current. Connect external resistors between these pins and Vcc (Pin 5). When not using this function, connect these pins to GND. *The minimum value for external resistors should be 100kΩ (when Vcc is 15V).
3	IDRV1	I	—		

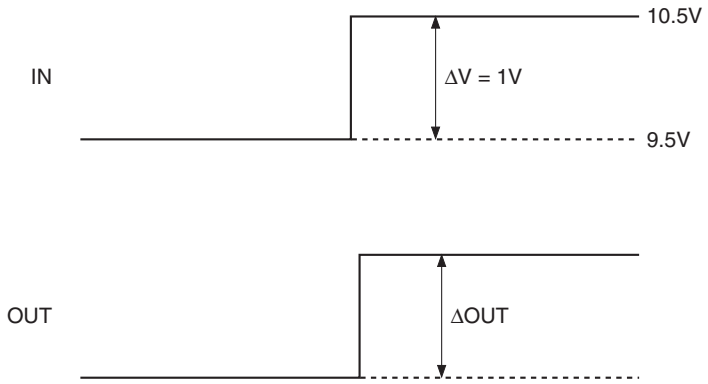
Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
6	ISF0	I	—		External resistor connection for setting the CCD with open source output sink current. Connect external resistors between these pins and Vcc (Pin 5). When not using this function, connect these pins to GND. *The minimum value for external resistors should be 100kΩ (when Vcc is 15V).
7	ISF1	I	—		
10	IN	I	CCD output voltage		Input
14	OUT	O	≈IN		Output

Electrical Characteristics

(Ta = 25°C, V_{CC} = 15V, R_{IDRV0} = 220kΩ, R_{IDRV1} = 470kΩ, ISF0 and ISF1 pins: connected to GND)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Supply current	I_{CC}	IN = 10V, R_{DRV0} = 220kΩ, R_{DRV1} = 470kΩ DRVCNT = 0V	1.5	1.7	1.9	mA
Voltage gain	V_{GAIN}	*1 IN: F10Vdc ΔV = 1V GAIN = ΔOUT/ΔV	—	0.999	—	V/V
I/O offset voltage	V_{OFFSET}	IN = 10V V_{OFFSET} = OUT-IN	–100	—	100	mV
I/O voltage range	V_{RANGE}	R_{IDRV} = 100kΩ R_{IDRV} = 150kΩ R_{IDRV} = 220kΩ R_{IDRV} = 330kΩ	3.3 2.9 2.5 2.1	— — — —	V_{CC} – 2.0 V_{CC} – 1.85 V_{CC} – 1.8 V_{CC} – 1.7	V
Input bias current	I_{BIAS}	IN = 10V, ISF0, 1 = 0V, IDRV0, 1 = 220kΩ	–6.0	3.0	20	μA
		IN = 10V, ISF0, 1, IDRV0, 1 = 0V	3.0	9.0	15	μA
Sink current	I_{SINK}	IN = 10V, R_{ISF0} = 220kΩ, R_{ISF1} = 470kΩ SFCNT = 0V	2.6	2.9	3.2	mA
Switch control voltage "High"	VcontH	V_{DD} = 3.0 ± 0.3V	2.025	—	—	V
Switch control voltage "Low"	VcontL		—	—	0.825	V

*1 Voltage gain

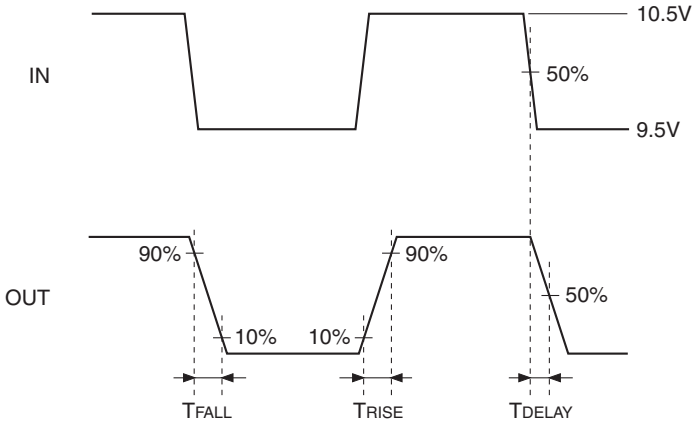


AC Characteristics

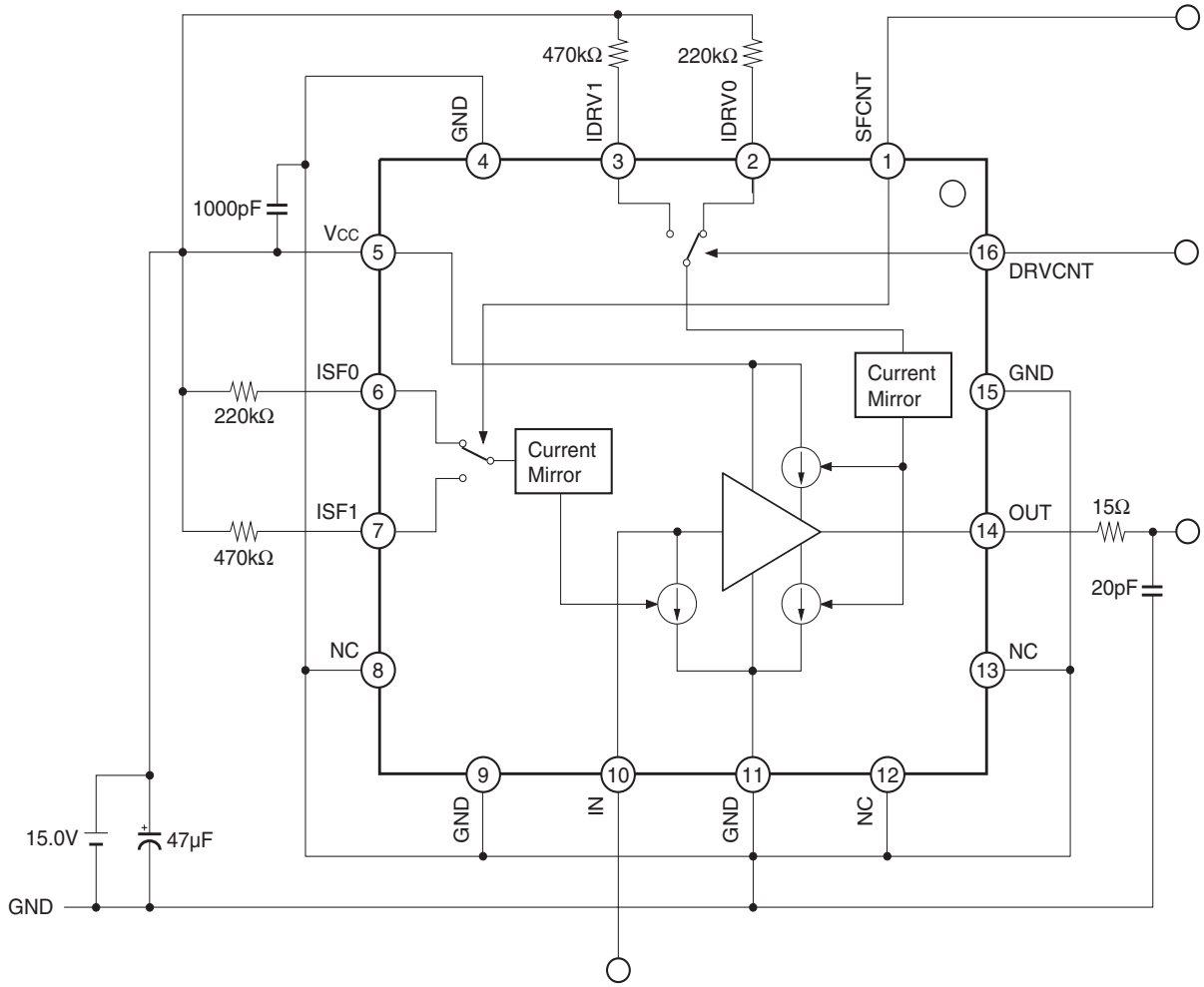
(Ta = 25℃, IDRV = 50μA (220kΩ when V_{CC} = 15V), ISF0 and ISF1 pins: connected to GND, R_L = 15Ω, C_L = 20pF)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Bandwidth	GBW	IN = 50mVp-p	—	220	—	MHz
Rise time	T_{RISE}	*1 IN = 9.5 to 10.5V 10 to 90%	—	2.5	3.5	ns
Fall time	T_{FALL}	*1 IN = 10.5 to 9.5V 10 to 90%	—	3.0	4.0	ns
I/O delay time	T_{DELAY}	*1 IN = 9.5 to 10.5V @50%	0.9	1.0	2.0	ns

*1 Rise time, fall time and I/O delay time



Evaluation Circuit



Description of Operation

Current Settings

1. Output Drive Current

The small signal output impedance of the OUT pin (Pin 14) can be set by connecting the IDRV0 pin (Pin 2) or the IDRV1 pin (Pin 3) to V_{CC} through a resistor.
The inflow current to the IDRV pin is multiplied by 10 times inside the IC, and flows as the output stage idling current.
The IDRV pins have internal 50kΩ resistors.
When the drive current setting switching pin DRVCNT (Pin 16) input logic is low, the inflow current to the IDRV pin is set according to the current set by the IDRV0 pin (Pin 2).
When high, the inflow current to the IDRV pin is set according to the current set by the IDRV1 pin (Pin 3).
The above-mentioned inflow current to the IDRV pin can be calculated as follows.

$$IIDRV = (V_{CC} - VBE \times 2)/(R_{IDRV} + 50k\Omega)$$
$$= (15 - 1.46)/270k\Omega$$
$$= 50.1\mu A$$

Here, V_{CC} = 15V, VBE = 0.73V (typ.), and R_{IDRV} = 220kΩ.
The small signal output impedance at this time can be calculated as follows.

$$ROUT = (26mV/(10 \times IIDRV))/2$$
$$= (26mV/501\mu A)/2$$
$$= 26\Omega$$

2. Sink Current for CCD with Open Source Output

The sink current of the IN pin (Pin 10) can be set by connecting the ISF0 pin (Pin 6) or the ISF1 pin (Pin 7) to V_{CC} through a resistor.
This sink current can be used as the CCD output stage source follower drive current.
The inflow current to the ISF pin is multiplied by 58 times inside the IC, and flows as the sink current.
The ISF pins have internal 50kΩ resistors.
When the CCD source follower output sink current setting switching pin SFCNT (Pin 1) input logic is low, the inflow current to the ISF pin is set according to the current set by the ISF0 pin (Pin 6).
When high, the inflow current to the ISF pin is set according to the current set by the ISF1 pin (Pin 7).
The above-mentioned inflow current to the ISF pin can be calculated as follows.

$$IISF = (V_{CC} - VBE \times 2)/(R_{ISF} + 50k\Omega)$$
$$= (15 - 1.46)/270k\Omega$$
$$= 50.1\mu A$$

Here, V_{CC} = 15V, VBE = 0.73V (typ.), and R_{ISF} = 220kΩ.
The sink current at this time can be calculated as follows.

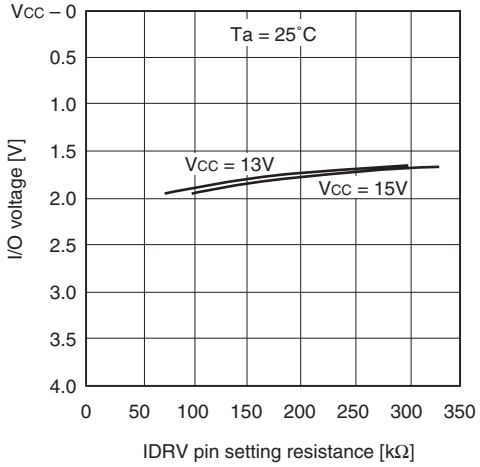
$$Isink = 58 \times IISF$$
$$= 2.9mA$$

Note) This IC operation depends on IDRV and ISF.
This specification is described based on IDRV of 220kΩ when V_{CC} = 15V. However , set it to 180kΩ to occur the same current when using under the condition that V_{CC} = 13V.
[IDRV and ISF vs external resistor]

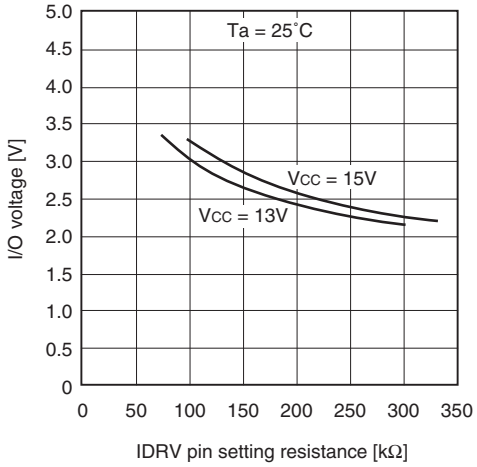
Current (μA)	90	68	50	35	26	Unit
When V_{CC} = 15V	100	150	220	330	470	kΩ
When V_{CC} = 13V	78	120	180	270	390	kΩ

Example of Representative Characteristics

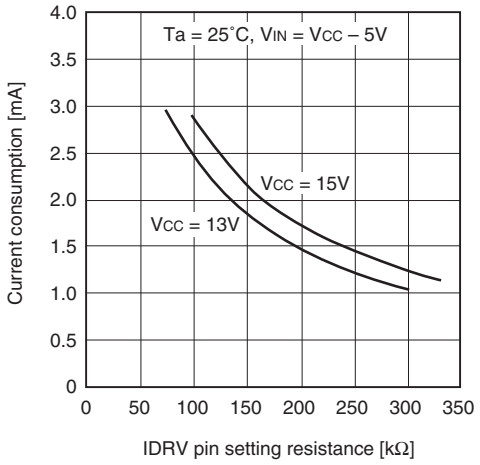
(Upper side) I/O voltage range vs. IDRV pin setting resistance



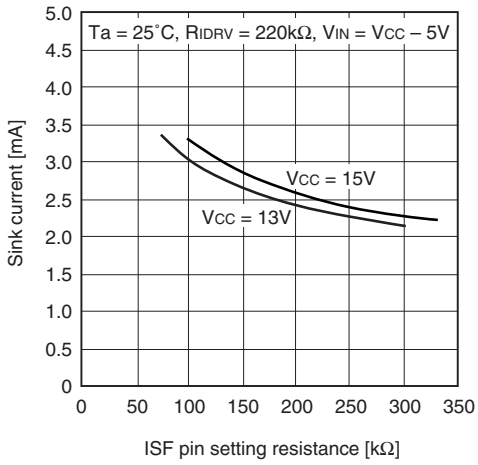
(Lower side) I/O voltage range vs. IDRV pin setting resistance



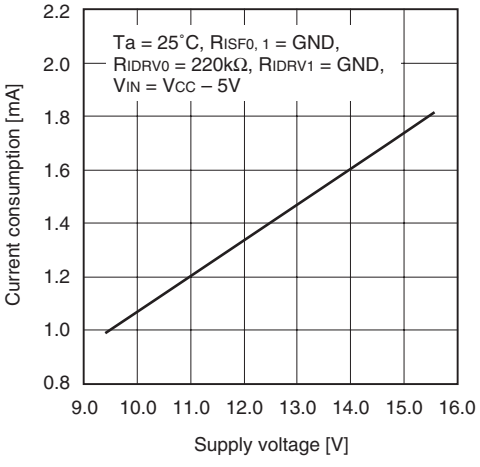
Current consumption vs. IDRV pin setting resistance



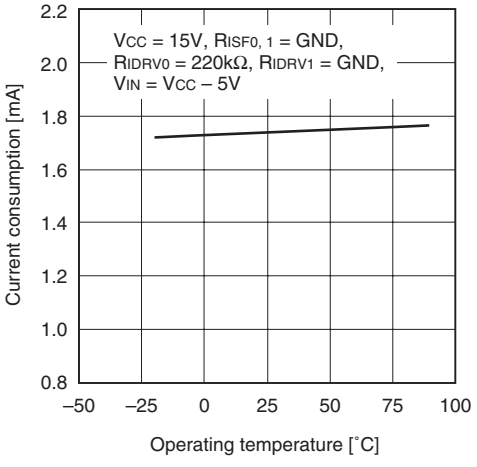
Sink current vs. ISF pin setting resistance



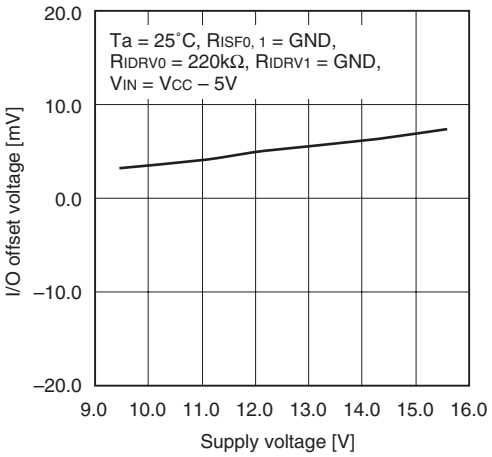
Current consumption vs. Supply voltage



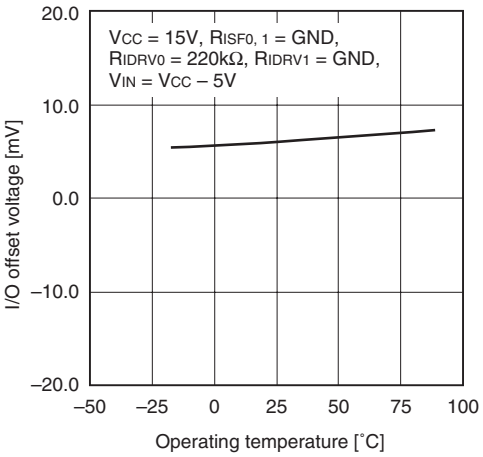
Current consumption vs. Operating temperature



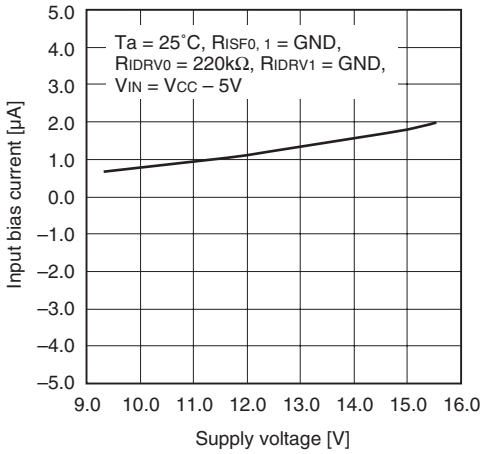
I/O offset voltage vs. Supply voltage



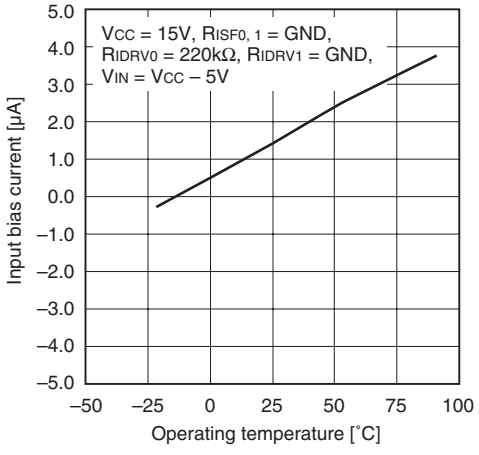
I/O offset voltage vs. Operating temperature



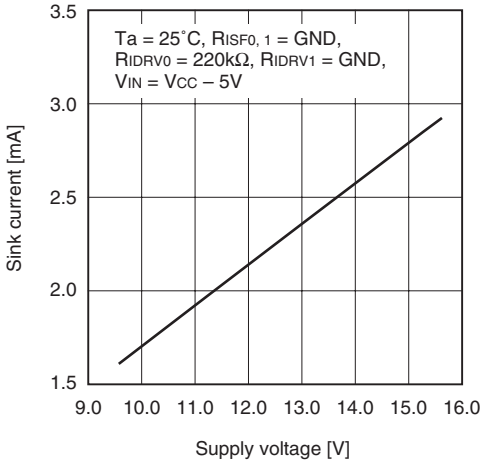
Input bias current vs. Supply voltage



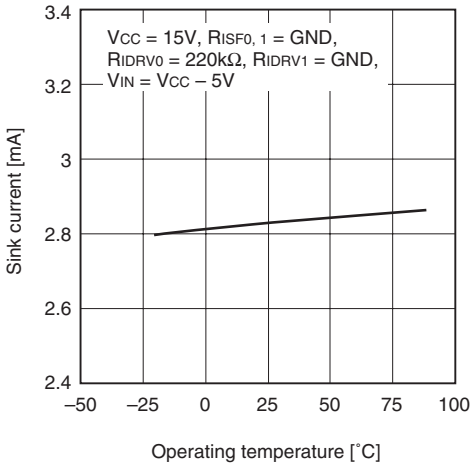
Input bias current vs. Operating temperature



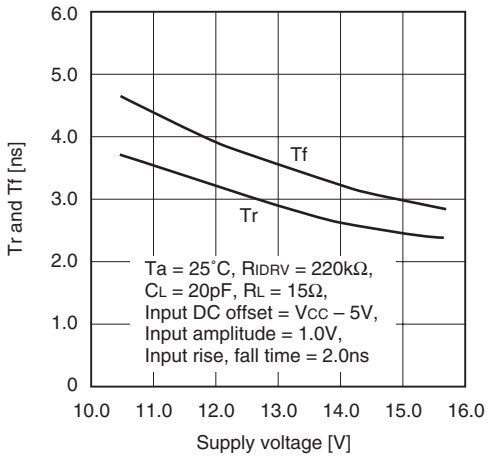
Sink current vs. Supply voltage



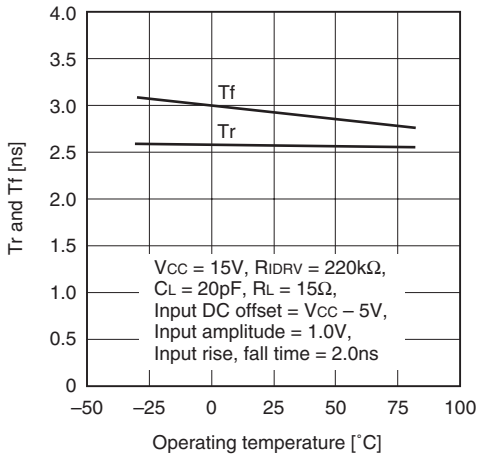
Sink current vs. Operating temperature



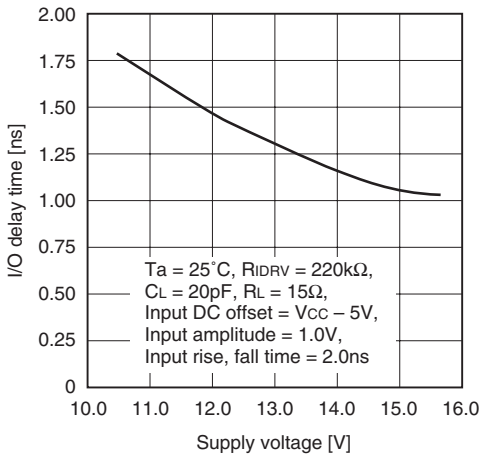
Tr and Tf vs. Supply voltage



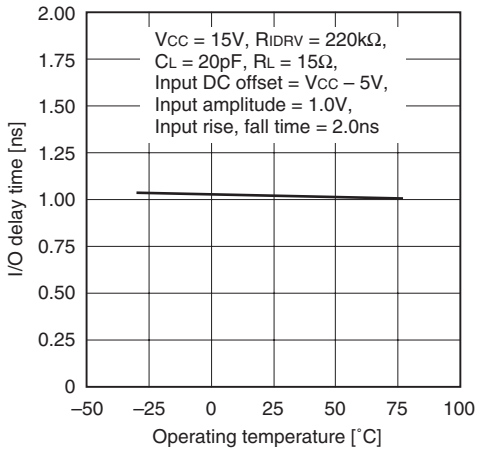
Tr and Tf vs. Operating temperature



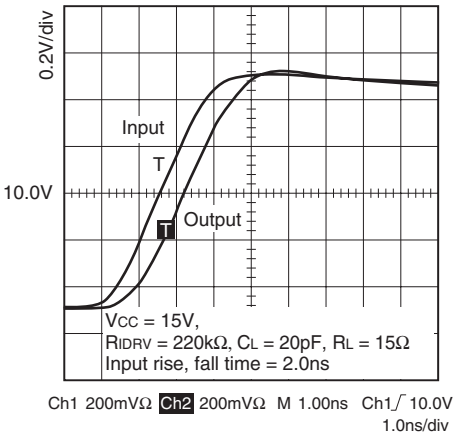
I/O delay time vs. Supply voltage



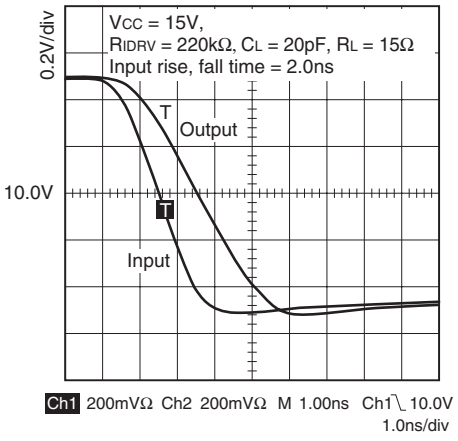
I/O delay time vs. Operating temperature



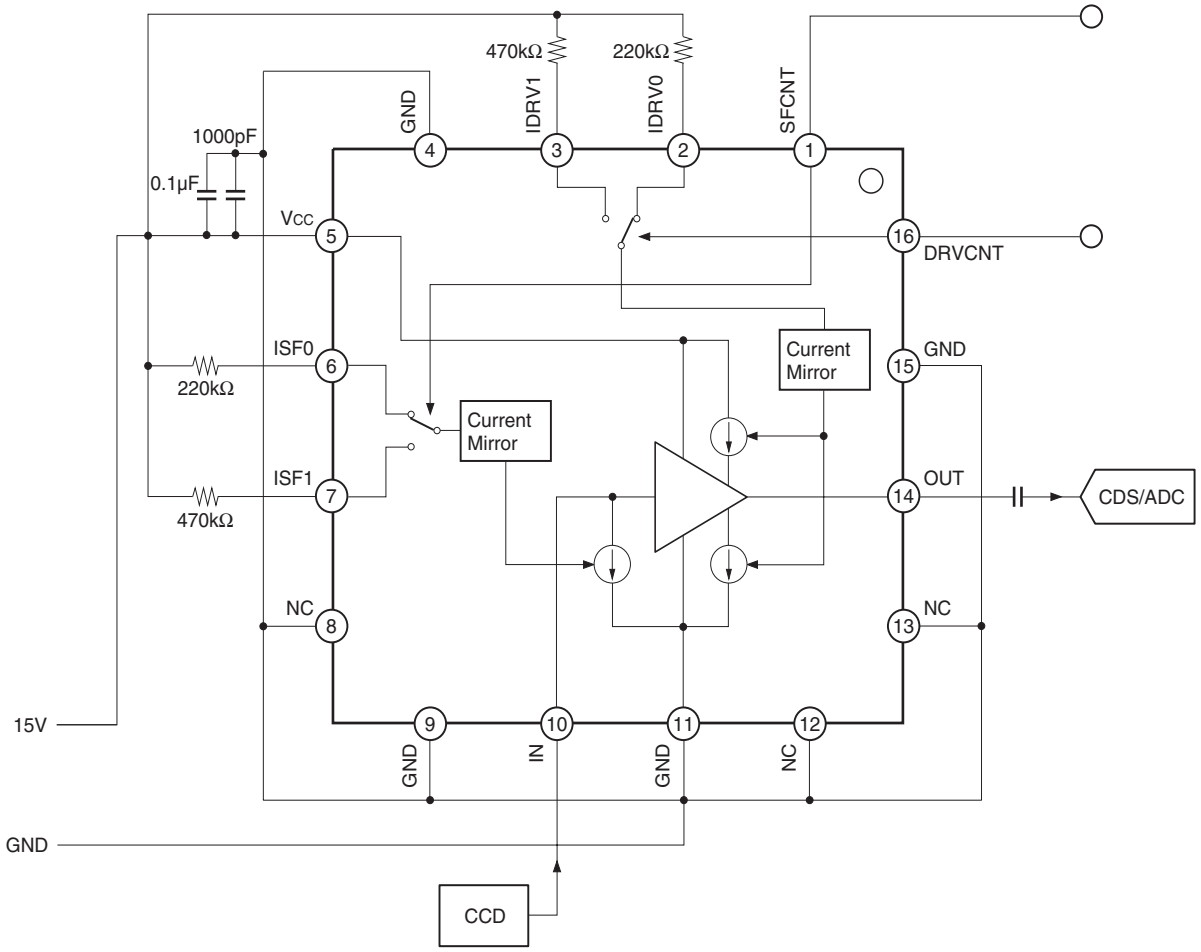
Positive pulse response



Negative pulse response

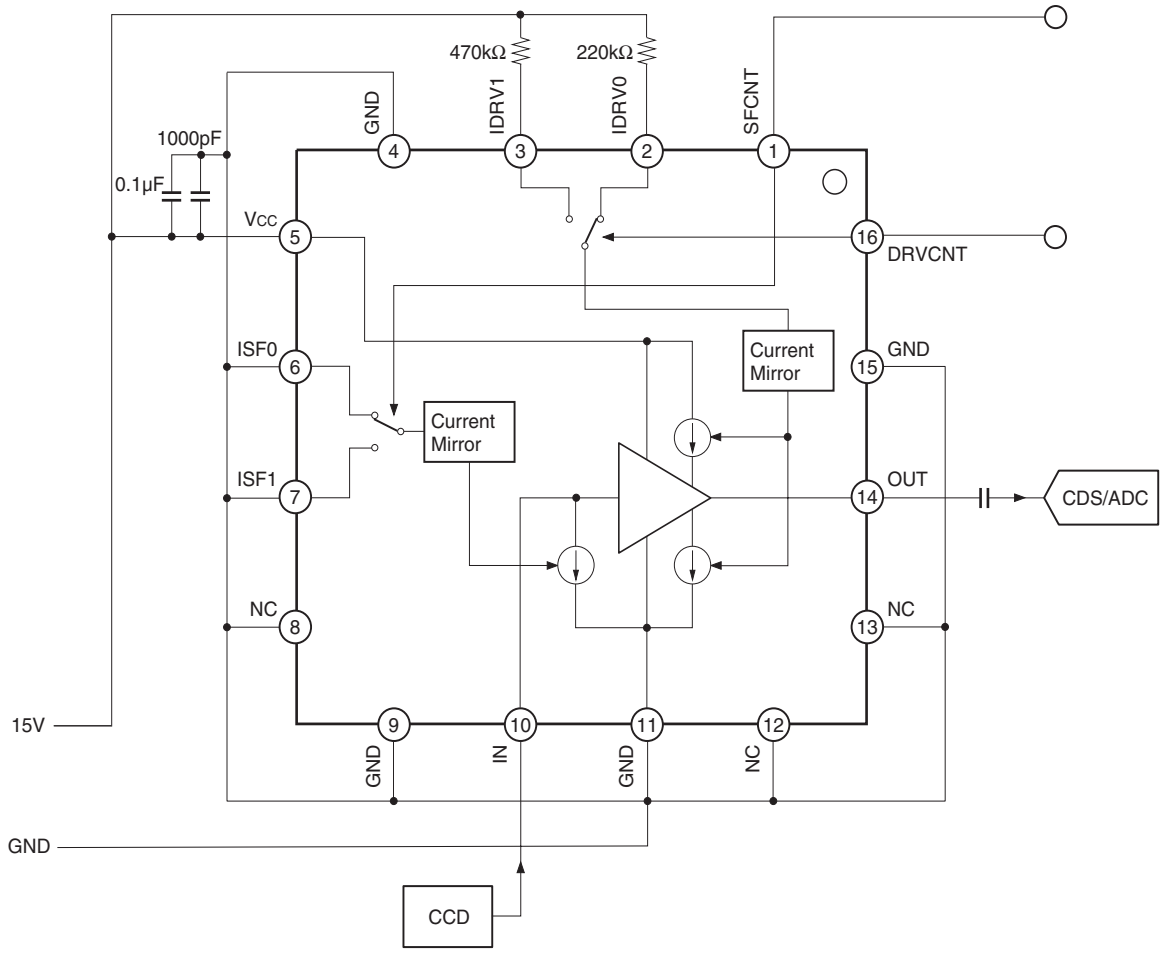


Application Circuit 1 (when using CCD with open source output)



Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2 (when using CCD with internal current source)



Application circuits shown are typical examples illustrating the operation of the devices.
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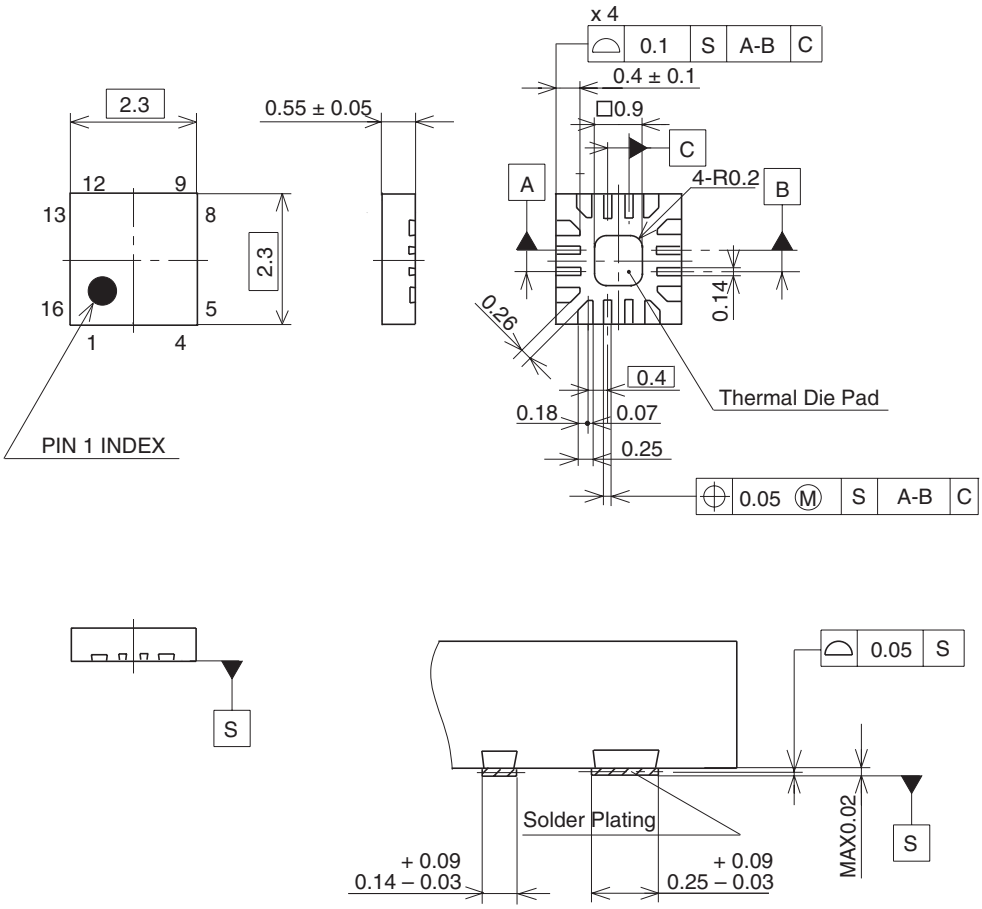
Notes On Handling

- Provide the widest GND pattern possible on the board.
- Use a 1000pF (recommended) ceramic capacitor and a 0.1μF (recommended) ceramic capacitor in parallel for the bypass capacitor connected between the power supply and GND, and connect them as close to the IC pins as possible.
- Load capacitance causes the input/output wiring response to worsen and results in noise. Use the short wiring layout, and shield it with GND.
- When the output pin (Pin 14) is shorted to either the power supply or GND, an overcurrent may flow to the IC and damage it.
- When the input pin (Pin 10) is shorted to GND, an overcurrent may flow to the internal parasitic elements and damage them.

Package Outline

(Unit: mm)

16PIN UQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	UQFN-16P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm