32Mx72 DDR SDRAM
iNTEGRATED Plastic Encapsulated Microcircuit

FEATURES

- DDR SDRAM Data Rate = 200, 250, 266, 333Mbps
- Package:
  - 208 Plastic Ball Grid Array (PBGA), 16 x 23mm-1.0mm pitch
- 2.5V ±0.2V core power supply
- 2.5V I/O (SSTL_2 compatible)
- Differential clock inputs (CLK and CLK#)
- Commands entered on each positive CLK edge
- Internal pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Programmable Burst length: 2,4 or 8
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture (one per byte)
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CLK
- Four internal banks for concurrent operation
- Two data mask (DM) pins for masking write data
- Programmable IOL/IOH option
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- Industrial, Enhanced and Military Temperature Ranges
- Organized as 32M x 72/80
- Weight: AS4DDR32M72PBG </= 2.0 grams typical

* This product and or it's specifications is subject to change without notice.

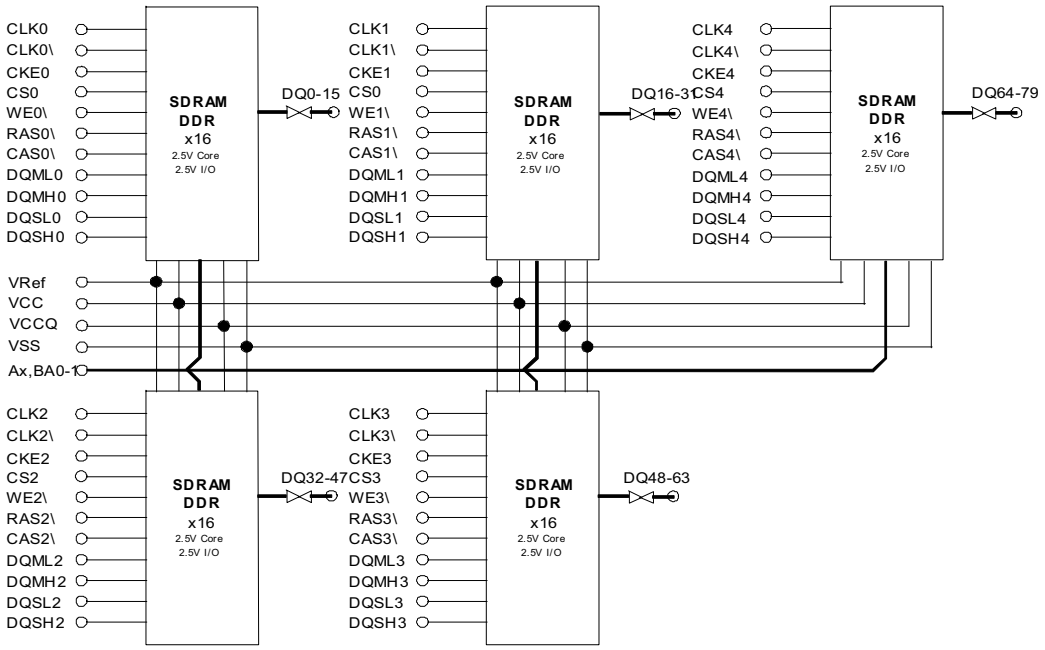
BENEFITS

- 40 - 70% SPACE SAVINGS
- Reduced part count
- Reduced I/O count
  - 34% I/O Reduction
- Reduced trace lengths for lower parasitic capacitance
- Suitable for hi-reliability applications
- Laminate interposer for optimum TCE match
- PIN/Function compatible to White W3E32M72S-xSBx

Configuration Addressing

Parameter	32 Meg x 72
Configuration	8 Meg x 16 x 4 Banks
Refresh Count	8K
Row Address	8K (A0-A12)
Bank Address	4 (BA0-BA1)
Column Address	1K (A0-A9)

FUNCTIONAL BLOCK DIAGRAM



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SDRAM-DDR Pinout Top View

Rev. A, 12/07, 208BGA-1.00MM PITCH - X72

	1	2	3	4	5	6	7	8	9	10	11	
A		VCC	VSS	VCCQ	VCCQ	VSS	VCCQ	VCCQ	VSS	VCC	VSS	A
B	VCCQ	VSS	CS2\	CS0\	CKE2	CKE0	CAS2\	RAS0\	RAS2\	VSS	VCCQ	B
C	VSS	CK0\	CK2\	CK0	CK2	DQML0	DQML2	CAS0\	WE0\	WE2\	VSS	C
D	DQMH2	DQMH0	DQSH2	DQSH0	DQ8	DQ40	DQ5	DQ39	DQ7	DQSL2	DQSL0	D
E	DQ41	DQ9	DQ10	DQ42	DQ43	DQ12	DQ3	DQ36	DQ4	DQ38	DQ6	E
F	DQ44	DQ11	DQ13	DQ45	DQ14	DQ33	DQ1	DQ34	DQ2	DQ37	DQ36	F
G	DQ64	DQ65	DQ15	DQ47	DQ48	VSS	DQ32	DQ0	DQ77	DQ79	DQ78	G
H	DNU	DQ66	DQ69	DNU	DQ67	VCC	DQ72	DQ73	DQ74	DQ75	DQ76	H
J	VCCQ	A12	BA1	A0	VCC	VSS	VCCQ	A7	A9	DNU	VCC	J
K	VSS	A10	A3	VCCQ	VSS	VREF	VSS	VCCQ	A4	A11	VSS	K
L	VCC	A2	BA0	A1	VCCQ	VSS	VCC	A6	A8	A5	VCCQ	L
M	DQ71	DQ70	DQSL4	DQML4	DQ68	VCC	DQSH4	DQMH4	CK4\	CK4	DNU	M
N	WE4\	CAS4\	RAS4\	DQ16	DQ48	VSS	DQ63	DQ31	DQ62	CKE4	CS4\	N
P	DQ22	DQ52	DQ18	DQ50	DQ17	DQ49	DQ30	DQ61	DQ29	DQ59	DQ27	p
R	DQ23	DQ54	DQ21	DQ19	DQ51	DQ60	DQ28	DQ58	DQ26	DQ57	DQ25	R
T	DQSL1	DQSL3	DQ55	DQ53	DQ20	DQ56	DQ24	DQMH3	DQMH1	DQSH1	DQSH3	T
U	VSS	CAS3\	WE3\	WE1\	DQML3	DQML1	CK1\	CK3\	CK1	CK3	VSS	U
V	VCCQ	VSS	CAS1\	RAS3\	RAS1\	CKE1	CKE3	CS1\	CS3\	VSS	VCCQ	V
W	VSS	VCC	VSS	VCCQ	VCCQ	VSS	VCCQ	VCCQ	VSS	VCC	VSS	W
	1	2	3	4	5	6	7	8	9	10	11	

Ground	Array Power	UNPOPULATED	Address
CNTRL	I/O Power	NC	DNU
Data I/O	Level REF.		

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PIN DEFINITIONS / FUNCTIONAL DESCRIPTION

BGA Location	Symbol	Type	Description
B5,B6,N10,V6,V7	CKEx	CNTL Input	Clock Enable, enabler of all on silicon clock circuitry
C4,C5,M10,U9,U10	CKx		Clock input (active HIGH) part of a differential pair (1 pair per x16 bits)
C2,C3,M9,U7,U8	CKx\		Clock input (active LOW) part of a differential pair (1pair per x16 bits)
B3,B4,N11,V8,V9	CSx\		Chip Selects, one per x16 bits (active LOW)
B7,C8,N2,U2,V3	CASx\		Column Address Select (1 per x16 bits)
B8,B9,N4,V4,V5	RASx\		Row Address Select (1 per x16 bits)
C9,C10,N1U3,U4	WEx\		WRITE enable input (active LOW, 1 per x16 bits)
C6,C7M4,U5,U6	DQMLx		
D1,D2,M8,T8,T9	DQMHx		
D10,D11M3,T1,T2	DQSLx		
D3,D4M7,T10,T11	DQSHx		
J4,L4,L2,K3,K9,L10, L8,J8,L9,J9,K2,K10, J2	Ax	ADDR Input	Array Address input providing ROW addresses for ACTIVE commands and the COLUMN address and AUTO PRECHARGE bit (A10) for READ/WRITE commands
L3, J3	BAx	Input	Bank Address select input
H1,H3,J10,M11	DNU	Future Use	
D5,D6,D7,D8,D9,E1,E2, E3,E4,E5,E6,E7,E8,E9, E10,E11,F1,F2,F3,F4, F5,F6,F7,F8,F9,F10, G1,G2,G3,G4,G5,G7, G8,G9,G10,G11,H2,H3, H5,H7,H8,H9,H10,H11, M1,M2,M5,N4,N5,N7,N8, N9,P1,P2,P3,P4,P5,P6, P7,P8,P9,P10,P11,R1, R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,T3,T4,T5, T6,T7,	DQx	Input/Output	Data, bi-directional Input/Output pins
K6	Vref	Supply	SSTL-25 Voltage Reference
A2,A10,H6,J5,J11,L1, L7,M6,W2,W10	VCC	Supply	Core Power Supply
A4,A5,A7,A8,B1,B2,J1, J7,K4,K8,L5,L11,V1, V11,W4,W5,W7,W8	VCCQ	Supply	IO Power Supply
A3,A6,A9,A11,B2,B10, C1,C11,G6,J6,K1,K5, K7,K11,L6,N6,U1,U11, V2,V10,W1,W3,W6,W9, W11	VSS	Supply	Ground Return
	UNPOPULATED		Unpopulated ball matrix location (location registration aid)

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GENERAL DESCRIPTION

The 2.4Gb DDR SDRAM MCM, is a high-speed CMOS, dynamic random-access, memory using 5 chips containing 536,870,912 bits. Each chip is internally configured as a quad-bank DRAM. Each of the chip's 134,217,728-bit banks is organized as 8,192 rows by 1024 columns by 32 bits.

The 256MB(2.4Gb) DDR SDRAM MCM uses a DDR architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256MB DDR SDRAM effectively consists of a single 2n-bit wide, one-clock-cycle data tansfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory contoller during WRITEs. DQS is edgealigned with data for READs and center-aligned with data for WRITEs. Each chip has two data strobes, one for the lower byte and one for the upper byte.

The 256MB DDR SDRAM operates from a differential clock (CLK and CLK#); the crossing of CLK going HIGH and CLK# going LOW will be referred to as the positive edge of CLK. Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a selftimed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a powersaving power-down mode.

FUNCTIONAL DESCRIPTION

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register defi nition, command descriptions and device operation.

INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to V_{CC} and V_{CCQ} simultaneously, and then to V_{REF} (and to the system V_{TT}). V_{TT} must be applied after V_{CCQ} to avoid device latch-up, which may cause permanent damage to the device. V_{REF} can be applied any time after V_{CCQ} but is expected to be nominally coincident with V_{TT}. Except for CKE, inputs are not recognized as valid until after V_{REF} is applied. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{CC} is applied. Maintaining an LVCMOS LOW level on CKE during powerup is required to ensure that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200µs delay prior to applying an executable command.

Once the 200µs delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a LOAD MODE REGISTER command should be issued for the extended mode register (BA1 LOW and BA0 HIGH) to enable the DLL, followed by another LOAD MODE REGISTER command to the mode register (BA0/ BA1 both LOW) to reset the DLL and to program the operating parameters. Two-hundred clock cycles are required between the DLL reset and any READ command. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed (t_{RFC} must be satisfi ed.) Additionally, a LOAD MODE REGISTER command for the mode register with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) is required. Following these requirements, the DDR SDRAM is ready for normal operation.

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REGISTER DEFINITION

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 3. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. (Except for bit A8 which is self clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The Mode Register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation. Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A12 specify the operating mode.

BURST LENGTH

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 3. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4 or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two; by A2-Ai when the burst length is set to four (where Ai is the most significant column address for a given configuration); and by A3-Ai when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

TABLE 1 - BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

NOTES:
1. For a burst length of two, A1-Ai select two-data-element block; A0 selects the starting column within the block.
2. For a burst length of four, A2-Ai select four-data-element block; A0-1 select the starting column within the block.
3. For a burst length of eight, A3-Ai select eight-data-element block; A0-2 select the starting column within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

READ LATENCY

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 2.5 clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge n+m. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

TABLE 2 - CAS LATENCY

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)	
	CAS LATENCY=2	CAS LATENCY=2.5
-10	≤ 75	≤ 100
-8	≤ 100	≤ 125
-75	≤ 100	≤ 133
-6	≤ 100	≤ 166

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OPERATING MODE

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7-A12 each set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. Although not required, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

EXTENDED MODE REGISTER

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, and QFC#. These functions are controlled via the bits shown in Figure 3. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

FIGURE 1 - MODE BURST DEFINITION

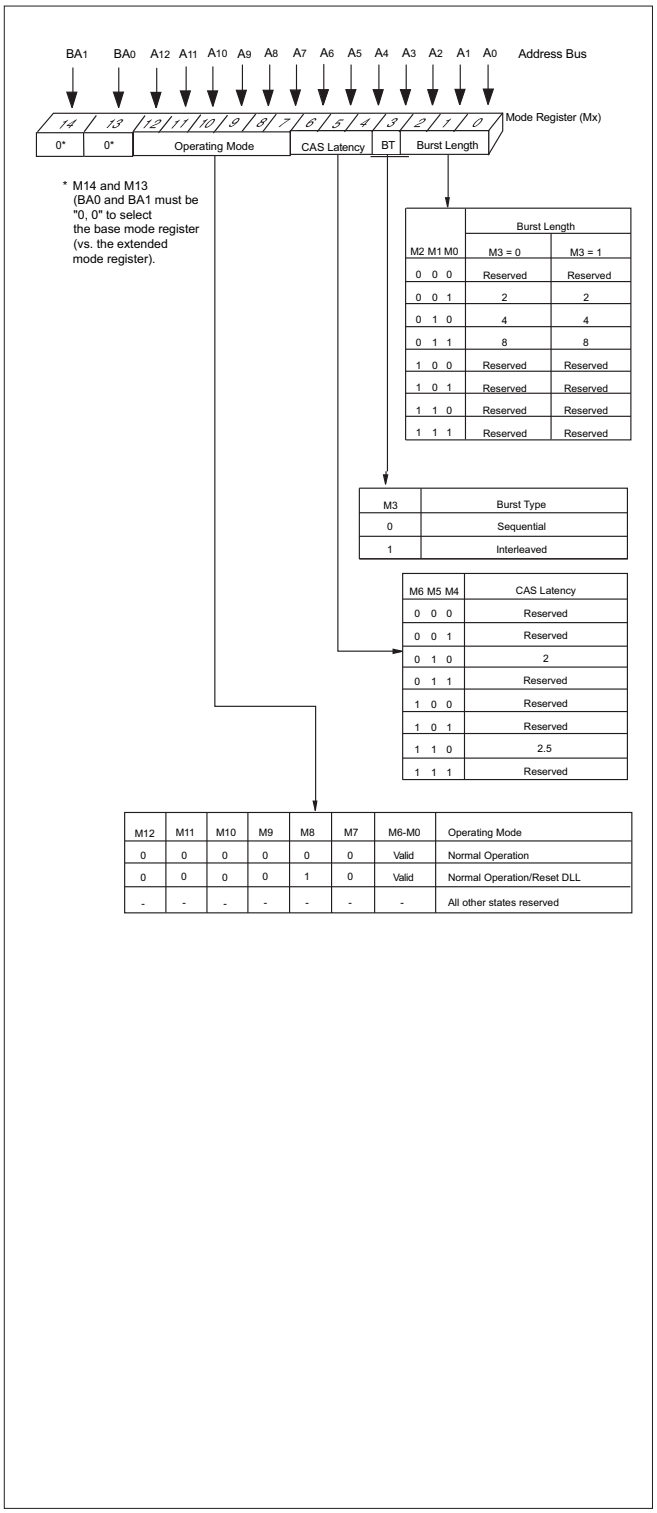

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FIGURE 2 - CAS LATENCY

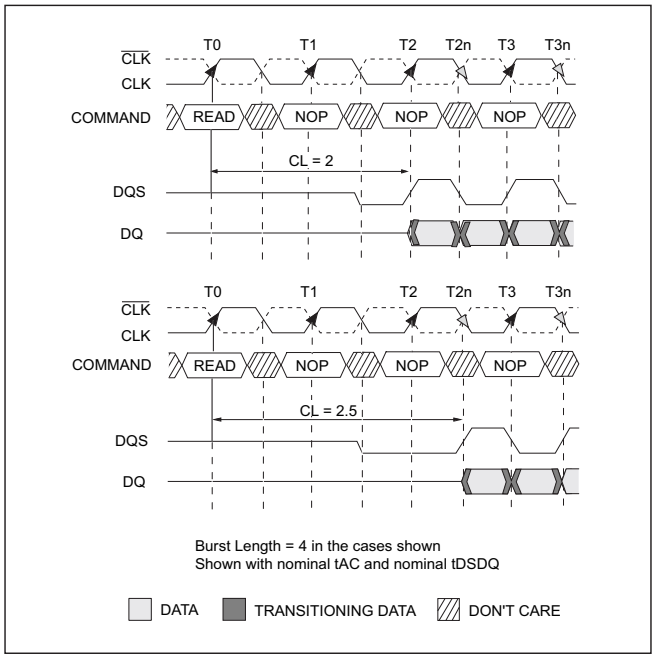
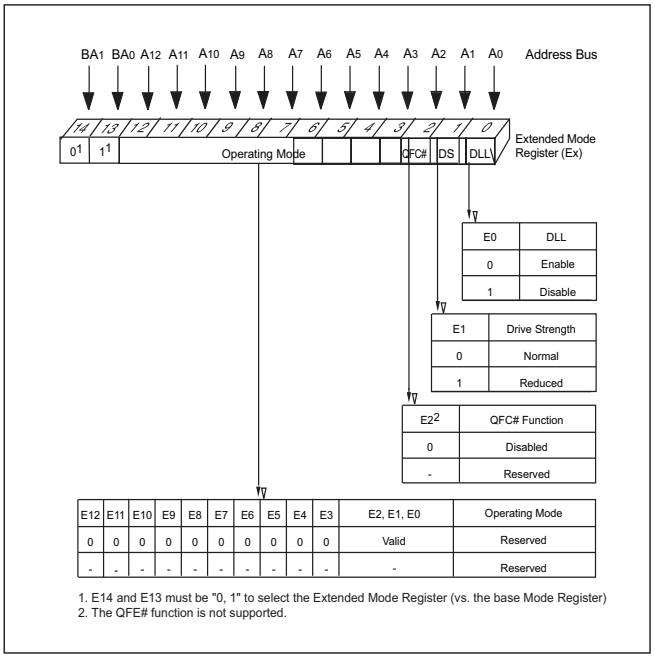


FIGURE 3 - EXTENDED MODE REGISTER DEFINITION



OUTPUT DRIVE STRENGTH

The normal full drive strength for all outputs are specified to be SSTL2, Class II. The DDR SDRAM supports an option for reduced drive. This option is intended for the support of the lighter load and/or point-to-point environments. The selection of the reduced drive strength will alter the DQs and DQSs from SSTL2, Class II drive strength to a reduced drive strength, which is approximately 54 percent of the SSTL2, Class II drive strength.

DLL ENABLE/DISABLE

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

COMMANDS

The Truth Table provides a quick reference of available commands. This is followed by a written description of each command.

DESELECT

The DESELECT function (CS# HiGH) prevents new commands from being executed by the DDR SDRAM. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to the selected DDR SDRAM (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The Mode Registers are loaded via inputs A0-12. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until t_{MRD} is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

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TRUTH TABLE - COMMANDS (NOTE 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR
DESELECT (NOP)(9)	H	X	X	X	X
NO OPERATION (NOP) (9)	L	H	H	H	X
ACTIVE (Select bank and activate row) (3)	L	L	H	H	Bank/Row
READ (Select bank and column, and start READ burst) (4)	L	H	L	H	Bank/Col
WRITE (Select bank and column, and start WRITE burst) (4)	L	H	L	L	Bank/Col
BURST TERMINATE (8)	L	H	H	L	X
PRECHARGE (Deactivate row in bank or banks) (5)	L	L	H	L	Code
AUTO REFRESH or SELF REFRESH (Enter self refresh mode) (6,7)	L	L	L	H	X
LOAD MODE REGISTER (2)	L	L	L	L	Op-Code

TRUTH TABLE - DM OPERATION

NAME (FUNCTION)	DM	DQs
WRITE ENABLE (10)	L	Valid
WRITE INHIBIT (10)	H	X

NOTES:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0-12 define the op-code to be written to the selected Mode Register. BA0, BA1 select either the mode register (0, 0) or the extended mode register (1, 0).
3. A0-12 provide row address, and BA0, BA1 provide bank address.
4. A0-8 provide column address; A10 HIGH enables the auto precharge feature (non-persistent), while A10 LOW disables the auto precharge feature; BA0, BA1 provide bank address.
5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
9. DESELECT and NOP are functionally interchangeable.
10. Used to mask write data; provided coincident with the corresponding data.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-9 selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the READ burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-9 selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the WRITE burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. Input data appearing on the D/Qs iswritten to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued. Except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

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AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank PRECHARGE function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. The device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. This "earliest valid stage" is determined as if an explicit precharge command was issued at the earliest possible time, without violating t_{RAS} (MIN).The user must not issue another command to the same bank until the precharge time (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating t_{RAS} (MIN).

BURST TERMINATE

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated. The open page which the READ burst was terminated from remains open.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. Each DDR SDRAM requires AUTO REFRESH cycles at an average interval of 7.8125µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 x 7.8125µs (70.3µs). This maximum absolute interval is to allow future support for DLL updates internal to the DDR SDRAM to be restricted to AUTO REFRESH cycles, without allowing excessive drift in t_{AC} between updates.

Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (High) during the AUTO REFRESH period. The AUTO REFRESH period begins when the AUTO REFRESH command is registered and ends t_{RFC} later.

SELF REFRESH*

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled upon exiting SELF REFRESH (200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are "Don't Care" during SELF REFRESH. The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for t_{XSNR}, because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

* Self refresh available in commercial and industrial temperatures only.

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ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on V_{CC}, V_{CCQ} Supply relative to V_{SS}	-1 ot 3.6	V
Voltage on I/O pins relative to V_{SS}	-1 ot 3.6	V
Operating Temperature T_A (Mil)	-55 to +125	^oC
Operating Temperature T_A (Ind)	-40 to +85	^oC
Storage Temperature, Plastic	-55 to +150	^oC

Note: Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational conditions for extended periods may affect reliability.

CAPACITANCE (NOTE 13)

Parameter	Symbol	Max	Unit
Input Capacitance: CLK	C_{11}	8	pF
Addresses, BA0-1 Input Capacitance	CA	30	pF
Input Capacitance: All other input-only pins	C_{12}	9	pF
Input/Output Capacitance: I/O's	C_{10}	12	pF

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DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS (NOTES 1,6)

V_{CC}, V_{CCQ} = +2.5V ± 0.2V; -55°C ± 0.2V, -55°C T_A +125°C

Parameter / Condition	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	2.3	2.7	V
I/O Supply Voltage	V_{CCQ}	2.3	2.7	V
Input Leakage Current: Any input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA
Input Leakage Address Current (All other pins not under test = 0V)	I_I	-10	10	µA
Output Leakage Current: I/O's are disabled; 0V ≤ V_{OUT} ≤ V_{CC}	I_{OZ}	-5	5	µA
Output Levels: Full drive option High Current (V_{OUT} = V_{CCQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OH}	-12	-	mA
Low Current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OL}	12	-	mA
Output Levels: Reduced drive option High Current (V_{OUT} = V_{CCQ} - 0.763V, minimum V_{REF}, minimum V_{TT})	I_{OHR}	-9	-	mA
Low Current (V_{OUT} = 0.763V, maximum V_{REF}, maximum V_{TT})	I_{OLR}	9	-	mA
I/O Reference Voltage (6)	V_{REF}	0.49 x V_{CCQ}	0.51 x V_{CCQ}	V
I/O Termination Voltage (53)	V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V

AC INPUT OPERATING CONDITIONS (NOTES 1,6)14, 28, 40

V_{CC}, V_{CCQ} = +2.5V ± 0.2V; -55°C ± 0.2V, -55°C T_A +125°C

Parameter / Condition	Symbol	Min	Max	Units
Input High (Logic 1) Voltage:	V_{IH} (AC)	V_{REF} + 0.310	-	V
Input Low (Logic) Voltage:	V_{IL} (AC)	-	V_{REF} - 0.310	V

I_{CC} SPECIFICATIONS AND CONDITIONS (NOTES 1-5, 10, 12, 14)

V_{CC}, V_{CCQ} = +2.5V ± 0.2V; -55°C ± 0.2V, -55°C T_A +125°C

Parameter / Condition		Symbol	Max		
			333, 266 250 Mbps	200 Mbps	Units
OPERATING CURRENT: One bank, Active-Precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles; (22, 48)		I_{CC0}	625	600	mA
OPERATING CURRENT: One bank, Active-Read- Precharge; Burst=2; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA; Address and control inputs changing once every two clock cycles; (22, 48)		I_{CC1}	850	775	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; t_{CK}=t_{CK} (MIN); CKE=LOW; (23, 32. 50)		I_{CC2P}	20	20	mA
IDLE STANDBY CURRENT: CS#=HIGH, All banks idle; t_{CK}=t_{CK} (MIN); CKE=HIGH; Address and other control inputs changing once per clock cycle. V_{IN}=V_{REF} for DQ, DQS and DM (51)		I_{CC2F}	225	225	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; t_{CK}=t_{CK} (MIN); CKE=LOW (23, 32, 50)		I_{CC3P}	150	150	mA
ACTIVE STANDBY CURRENT: CS#=HIGH; CKE=HIGH; One bank; Active Precharge; t_{RC}=t_{RAS} (MAX); t_{CK}=t_{CK} (MIN); DQ, DM and DQS inputs changin twicer per clock cycle; Address and other control inputs changing once per clock cycle (22)		I_{CC3N}	250	250	mA
OPERATING CURRENT: Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t_{CK}=t_{CK} (MIN); I_{OUT}=0mA (22,48)		I_{CC4R}	925	925	mA
OPERATING CURRENT: Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t_{CK}=t_{CK} (MIN); DQ, DM and DQS inputs changin twice per clock cycle (22)		I_{CC4W}	800	800	mA
AUTO REFRESH CURRENT	t_{REF}=t_{RC} (MIN) (27, 50)	I_{CC5}	1225	1225	mA
	t_{REF}=7.8125 µs (27, 50)	I_{CC5A}	30	30	mA
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard (11)	I_{CC6}	20	20	mA
OPERATING CURRENT: Four bank interleaving DEADs (BL=4) with auto precharge, t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); Addresses and control inputs change only during Active READ or WRITE commands. (22, 49)		I_{CC7}	2000	2000	mA

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CHARACTERISTICS (NOTES 1-5, 14-17, 33)

Parameter		Symbol	-6, 333 [266] Mbps @CL=2.5 [CL=2]		-75, 266 [250] Mbps @CL=2.5 [CL=2]		Units
			Min	Max	Min	Max	
Access window of DQs from CLK/CLK#		t_{AC}	-0.70	+0.70	-0.75	+0.75	ns
CLK high-level width (30)		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}
CLK low-level width (30)		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}
Clock cycle time	CL=2.5 (45, 52)	t_{CK} (2.5)	6	13	7.5	13	ns
	CL=2 (45, 52)	t_{CK} (2)	7.5	13	8	13	ns
DQ and DM input hold time relative to DQS (26, 31)		t_{DH}	0.45		0.5		ns
DQ and DM input setup time relative to DQS (26,31)		t_{DS}	0.45		0.5		ns
DQ and DM input pulse with (for each input) (31)		t_{DIPW}	1.75		1.75		ns
Access window of DQS from CLK/CLK#		t_{DQSCK}	-0.6	+0.6	-0.75	+0.75	ns
DQS input high pulse width		tDQSH	0.35		0.35		t_{CK}
DQS input high pulse width		t_{DQSL}	0.35		0.35		t_{CK}
DQS-DQ skew, DQS to last valid, per group, per access (25,26)		t_{DQSQ}		0.45		0.5	ns
Write command to first DQS latching transition		t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}
DQS falling edge to CLK rising - setup time		t_{DSS}	0.2		0.2		t_{CK}
DQS falling edge to CLK rising - hold time		t_{DSH}	0.2		0.2		t_{CK}
Half clock period (34)		t_{HP}	t_{CH}, t_{CL}		t_{CH}, t_{CL}		ns
Data-out high-impedance window from CLK/CLK# (18, 42)		t_{HZ}		+0.7		+0.75	ns
Data-out low-impedance window from CLK/CLK# (18, 43)		t_{LZ}	-0.7		-0.75		ns
Address and control input hold time (fast slew rate) (14)		t_{IHF}	0.75		0.9		ns
Address and control input setup time (fast slew rate) (14)		t_{ISF}	0.75		0.9		ns
Address and control input hold time (slow slew rate) (14)		t_{IHS}	0.8		1.0		ns
Address and control input setup time (slow slew rate) (14)		t_{ISS}	0.8		1.0		ns
LOAD MODE REGISTER command cycle time		t_{MRD}	12		15		ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access (25, 26)		t_{QH}	t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ns
Data hold skew factor		t_{QHS}		0.55		1	ns
ACTIVE to PRECHARGE command (35)		t_{RAS}	42	70,000	40	120,000	ns
ACTIVE to READ with Auto precharge command		t_{RAP}	15		15		ns
ACTIVE to ACTIVE/AUTO REFRESH command period		t_{RC}	60		60		ns
AUTO REFRESH command period (50)		t_{RFC}	72		75		ns
ACTIVE to READ or WRITE delay		t_{RCD}	15		15		ns
PRECHARGE command period		t_{RP}	15		15		ns
DQS read preamble (42)		t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}
Active bank a to ACTIVE bank b command		t_{RRD}	12		15		ns
DQS write preamble		t_{WPRE}	0.25		0.25		t_{CK}
DQS write preamble setup time (20,21)		t_{WPRES}	0		0		ns
DQS write postamble (19)		t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}
Write recovery time		t_{WR}	15		15		ns
Internal WRITE to READ command delay		t_{WTR}	1		1		t_{CK}
Data valid output window (25)		NA	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
REFRESH to REFRESH command interval (Commercial & Industrial temp		t_{REFC}		70.3		70.3	µs
REFRESH to REFRESH command interval (Military temp only) (23)		t_{REFC}		35		35	µs
Average periodic refresh interval (Commercial & Industrial temp only) (23)		t_{REFI}		7.8		7.8	µs
Average periodic refresh interval (Military temp only) (23)		t_{REFI}		3.9		3.9	µs
Terminating voltage delay to Vcc (53)		t_{VTD}	0		0		ns
Exit SELF REFRESH to non-READ command		t_{XSNR}	75		75		ns
Exit SELF REFRESH to READ command		t_{XSRD}	200		200		t_{CK}

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CHARACTERISTICS (NOTES 1-5, 14-17, 33)

Parameter		Symbol	-8, 250 [200] Mbps @CL=2.5 [CL=2]		-10, 200 [167] Mbps @CL=2.5 [CL=2]		Units
			Min	Max	Min	Max	
Access window of DQs from CLK/CLK#		t_{AC}	-0.8	+0.8	-0.8	+0.8	ns
CLK high-level width (30)		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}
CLK low-level width (30)		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}
Clock cycle time	CL=2.5 (45, 52)	t_{CK} (2.5)	8	13	10	13	ns
	CL=2 (45, 52)	t_{CK} (2)	10	13	13	15	ns
DQ and DM input hold time relative to DQS (26, 31)		t_{DH}	0.6		0.6		ns
DQ and DM input setup time relative to DQS (26,31)		t_{DS}	0.6		0.6		ns
DQ and DM input pulse with (for each input) (31)		t_{DIPW}	2		2		ns
Access window of DQS from CLK/CLK#		t_{DQSCK}	-0.8	+0.8	-0.8	+0.8	ns
DQS input high pulse width		t_{DQSH}	0.35		0.35		t_{CK}
DQS input high pulse width		t_{DQSL}	0.35		0.35		t_{CK}
DQS-DQ skew, DQS to last valid, per group, per access (25,26)		t_{DQSQ}		0.6		0.6	ns
Write command to first DQS latching transition		t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}
DQS falling edge to CLK rising - setup time		t_{DSS}	0.2		0.2		t_{CK}
DQS falling edge to CLK rising - hold time		t_{DSH}	0.2		0.2		t_{CK}
Half clock period (34)		t_{HP}	t_{CH}, t_{CL}		t_{CH}, t_{CL}		ns
Data-out high-impedance window from CLK/CLK# (18, 42)		t_{HZ}		+0.8		+0.8	ns
Data-out low-impedance window from CLK/CLK# (18, 43)		t_{LZ}	-0.8		-0.8		ns
Address and control input hold time (fast slew rate) (14)		t_{IHF}	1.1		1.1		ns
Address and control input setup time (fast slew rate) (14)		t_{ISF}	1.1		1.1		ns
Address and control input hold time (slow slew rate) (14)		t_{IHS}	1.1		1.1		ns
Address and control input setup time (slow slew rate) (14)		t_{ISS}	1.1		1.1		ns
LOAD MODE REGISTER command cycle time		t_{MRD}	16		16		ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access (25, 26)		t_{QH}	t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ns
Data hold skew factor		t_{QHS}		1		1	ns
ACTIVE to PRECHARGE command (35)		t_{RAS}	40	120,000	40	120,000	ns
ACTIVE to READ with Auto precharge command		t_{RAP}	20		20		ns
ACTIVE to ACTIVE/AUTO REFRESH command period		t_{RC}	70		70		ns
AUTO REFRESH command period (50)		t_{RFC}	80		80		ns
ACTIVE to READ or WRITE delay		t_{RCD}	20		20		ns
PRECHARGE command period		t_{RP}	20		20		ns
DQS read preamble (42)		t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}
Active bank a to ACTIVE bank b command		t_{RRD}	15		15		ns
DQS write preamble		t_{WPRE}	0.25		0.25		t_{CK}
DQS write preamble setup time (20,21)		t_{WPRES}	0		0		ns
DQS write postamble (19)		t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}
Write recovery time		t_{WR}	15		15		ns
Internal WRITE to READ command delay		t_{WTR}	1		1		t_{CK}
Data valid output window (25)		NA	t_{QH}-t_{DQSQ}		t_{QH}-t_{DQSQ}		ns
REFRESH to REFRESH command interval (Commercial & Industrial temp		t_{REFC}		70.3		70.3	µs
REFRESH to REFRESH command interval (Military temp only) (23)		t_{REFC}		35		35	µs
Average periodic refresh interval (Commercial & Industrial temp only) (23)		t_{REFI}		7.8		7.8	µs
Average periodic refresh interval (Military temp only) (23)		t_{REFI}		3.9		3.9	µs
Terminating voltage delay to Vcc (53)		t_{VTD}	0		0		ns
Exit SELF REFRESH to non-READ command		t_{XSNR}	80		80		ns
Exit SELF REFRESH to READ command		t_{XSRD}	200		200		t_{CK}

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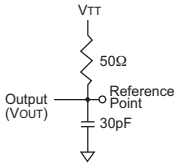
NOTES:

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{CC}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{CC} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CLK/CLK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal V_{CCQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from V_{CCQ}/2, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} by-pass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. V_{ID} is the magnitude of the difference between the input level on CLK and the input level on CLK#.
9. The value of V_{IX} and V_{MP} are expected to equal V_{CCQ}/2 of the transmitting device and must track variations in the DC level of the same.
10. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time with the outputs open.
11. Enables on-chip refresh and address counters.
12. I_{CC} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
13. This parameter is not tested but guaranteed by design. t_A = 25°C, f = 1 MHz
14. Command/Address input slew rate = 0.5V/ns. For 266 MHz with slew rates 1V/ns and faster, t_{IS} and t_{IH} are reduced to 900ps. If the slew rate is less than 0.5V/ns, timing must be derated: t_{IS} has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns. t_{IH} has 0ps added, that is, it remains constant. If the level, slew rate exceeds 4.5V/ns, functionality is uncertain.
15. The CLK/CLK# input reference level (for timing referenced to CLK/CLK#) is the point at which CLK and CLK# cross; the input reference level for signals other than CLK/CLK# is V_{REF}.
16. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stablizes, CKE < 0.3 x VCCQ is recognized as LOW.
17. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
18. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
19. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
20. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
21. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on t_{DQSS}.
22. MIN (t_{RC} or t_{RFC}) for I_{CC} measurements is the smallest multiple of t_{CK} that meets the minimum absolute value for the respective parameter. t_{RAS} (MAX) for I_{CC} measurements is the largest multiple of t_{CK} that meets the maximum absolute value for t_{RAS}.
23. The refresh period 64ms. This equates to an average refresh rate of However, an AUTO REFRESH command must be asserted at least once every 70.3µs; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
24. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
25. The valid data window is derived by achieving other specifications - t_{HP} (t_{CK}/2), t_{DQSQ}, and t_{QH} (t_{QH} = t_{HP} - t_{QHS}). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided
26. Referenced to each output group: LDQS with DQ0-DQ7; and UDQS with DQ8-DQ15 of each chip.
27. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH below for duty cycles ranging between 50/50 and 45/55. during REFRESH command period (t_{RFC} [MIN]) else CKE is LOW (i.e., during standby)
28. To maintain a valid level, the transitioning edge of the input must:
    a) Sustain a constant slew rate from the current AC level through to the target AC level, V_{IL}(AC) or V_{IH}(AC).
    b) Reach at least the target AC level.
    c) After the AC target level is reached, continue to maintain at least the target DC level, V_{IL}(DC) or V_{IH}(DC).

FIGURE A - PULL-DOWN CHARACTERISTICS

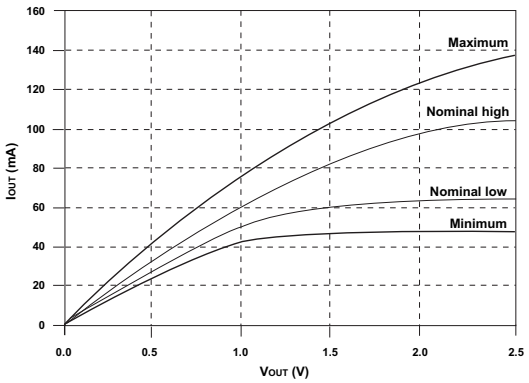
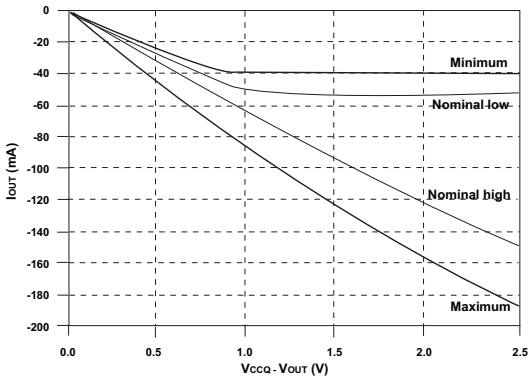


FIGURE B - PULL-UP CHARACTERISTICS



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29. The Input capacitance per pin group will not differ by more than this maximum amount for any given device.
30. CLK and CLK# input slew rate must be ≥ 1V/ns (≥2V/ns differentially).
31. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to t_{DS} and t_{DH} for each 100mV/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.
32. V_{CC} must not vary more than 4% if CKE is not active while any bank is active.
33. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
34. t_{HP} min is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CLK and CLK# inputs, collectively during bank active.
35. READs and WRITEs with auto precharge are not allowed to be issued until t_{RAS}(MIN) can be satisfied prior to the internal precharge command being issued.
36. Any positive glitch must be less than 1/3 of the clock and not more than +400mV or 2.9 volts, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2 volts, whichever is more positive.
37. Normal Output Drive Curves:
    a) The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure A.
    b) The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure A.
    c) The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure B.
    d) The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure B.
    e) The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between .71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0 Volt, and at the same voltage and temperature.
    f) The full variation in the ratio of the nominal pull-up to pull-down current should be unity ¡À10%, for device drain-to-source voltages from 0.1V to 1.0 Volt.
38. Reduced Output Drive Curves:
    a) The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure C.
    b) The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure C.
    c) The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure D.
    d) The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure B.
    e) The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between .71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0 Volt, and at the same voltage and temperature.
    f) The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10%, for device drain-to-source voltages from 0.1V to 1.0 Volt.
39. The voltage levels used are derived from a minimum V_{CC} level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
40. V_{IH} overshoot: V_{IH}(MAX) = V_{CCQ}+1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
41. V_{CC} and V_{CCQ} must track each other.
42. This maximum value is derived from the referenced test load. In practice, the values obtained in a typical terminated design may reflect up to 310ps less for t_{HZ}(MAX) and the last DVW. t_{HZ}(MAX) will prevail over t_{DQSCK}(MAX) + t_{RPST}(MAX) condition. t_{LZ}(MIN) will prevail over t_{DQSCK}(MIN) + t_{RPRE}(MAX) condition.
43. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
44. During initialization, V_{CCQ}, V_{TT}, and V_{REF} must be equal to or less than V_{CC} + 0.3V. Alternatively, V_{TT} may be 1.35V maximum during power up, even if V_{CC}/V_{CCQ} are 0 volts, provided a minimum of 42 ohms of series resistance is used between the V_{TT} supply and the input pin.
45. The current part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
46. Reserved for future use.
47. Reserved for future use.
48. Random addressing changing 50% of data changing at every transfer.
49. Random addressing changing 100% of data changing at every transfer.
50. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until t_{RFC} has been satisfied.
51. I_{CC2N} specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. I_{CC2Q} is similar to I_{CC2F} except I_{CC2Q} specifies the address and control inputs to remain stable. Although I_{CC2F}, I_{CC2N}, and I_{CC2Q} are similar, I_{CC2F} is "worst case."
52. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles before any READ command.
53. V_{TT} is not applied directly to the device; however, t_{VTD} should be greater than or equal to zero to avoid device latch-up. V_{CCQ}, V_{TT} and V_{REF} must be equal to or less than V_{CC} + 0.3V. Alternatively V_{TT} may be 1.35V max during power-up even if V_{CC}/V_{CCQ} are 0V, provided a minimum of 42 &! of series resistance is used between the V_{TT} supply and the input pin. Once initialized, V_{REF} must always be powered within the specified range.

FIGURE C - PULL-DOWN CHARACTERISTICS

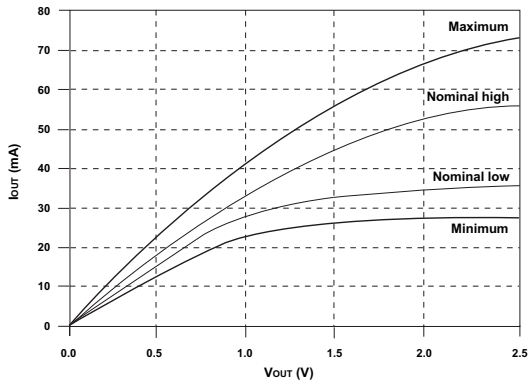
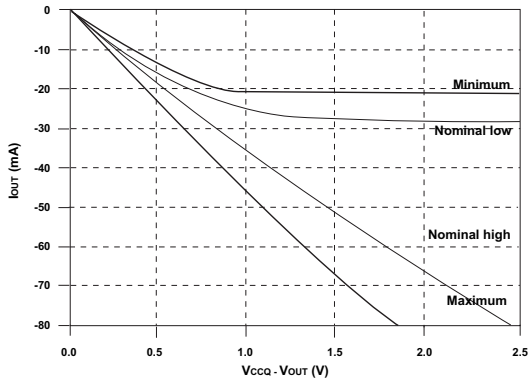


FIGURE D - PULL-UP CHARACTERISTICS



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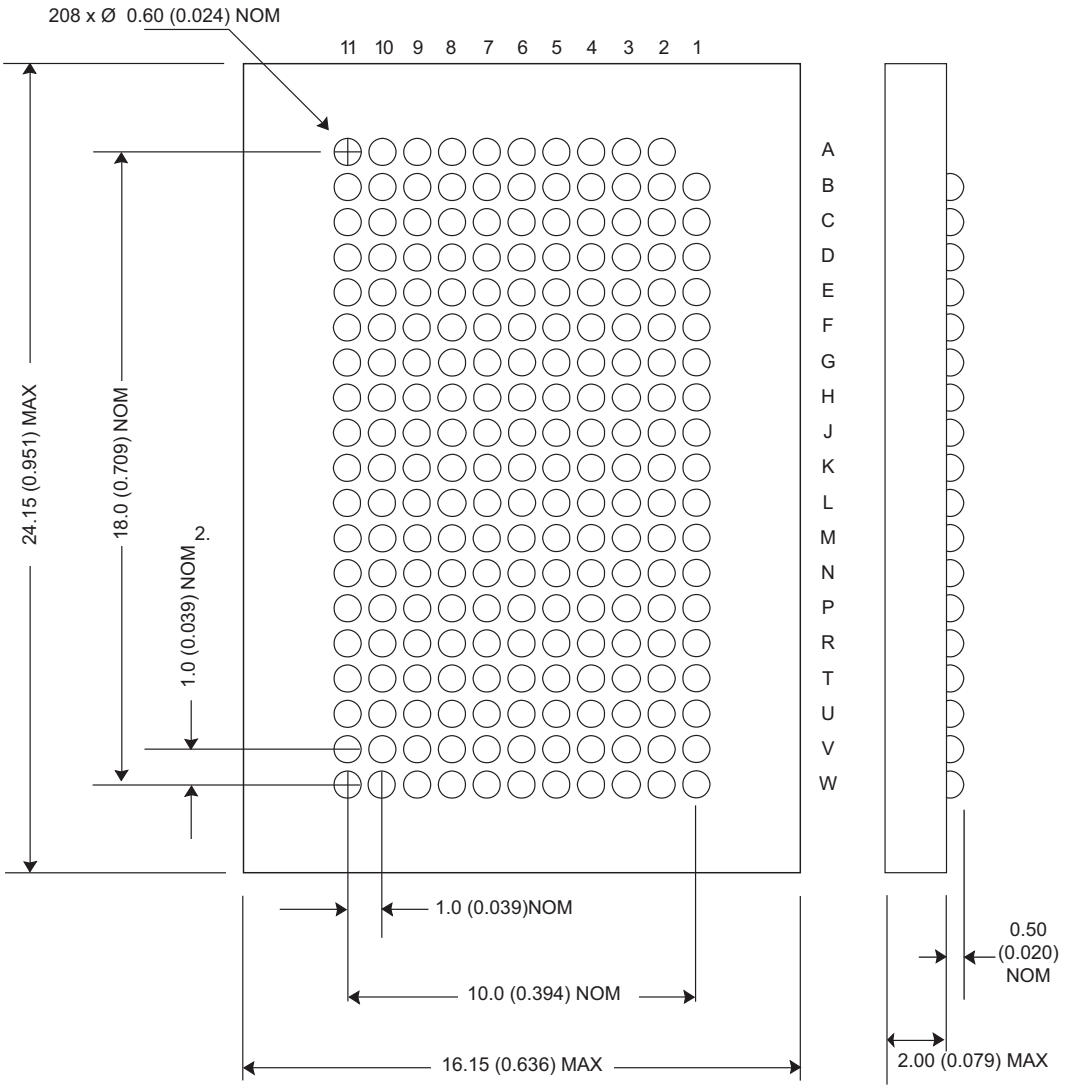
MECHANICAL DIAGRAM



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ORDERING INFORMATION

Part Number	Core Freq.	Data Transfer Rate	Package	Process
AS4DDR32M72PBG1-6/IT	166 MHz	333 Mbps	208-PBGA	Industrial
AS4DDR32M72PBG1-75/IT	133 MHz	266 Mbps	208-PBGA	Industrial
AS4DDR32M72PBG1-8/IT	125 MHz	250 Mbps	208-PBGA	Industrial
AS4DDR32M72PBG1-10/IT	100 MHz	200 Mbps	208-PBGA	Industrial
AS4DDR32M72PBG1-6/ET	166 MHZ	333 Mbps	208-PBGA	Enhanced
AS4DDR32M72PBG1-75/ET	133 MHz	266 Mbps	208-PBGA	Enhanced
AS4DDR32M72PBG1-8/ET	125 MHz	250 Mbps	208-PBGA	Enhanced
AS4DDR32M72PBG1-10/ET	100 MHz	200 Mbps	208-PBGA	Enhanced
AS4DDR32M72PBG1-6/XT	166 MHZ	333 Mbps	208-PBGA	Extended
AS4DDR32M72PBG1-75/XT	133 MHz	266 Mbps	208-PBGA	Extended
AS4DDR32M72PBG1-8/XT	125 MHz	250 Mbps	208-PBGA	Extended
AS4DDR32M72PBG1-10/XT	100 MHz	200 Mbps	208-PBGA	Extended

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DOCUMENT TITLE

32M x 72 DDR SDRAM Multi-Chip Packaged in a 32mm x 25mm - 208 PBGA

REVISION HISTORY

Rev #	History	Release Date	Status
0.0	INITIAL RELEASE	September 2008	Advance
0.1	Updated Order Chart Changed “Extended” to “Military” Temp	June 2008	Advance

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