XCM519 Series

600mA Synchronous Step-Down DC/DC Converter + Low Voltage Input LDO

■GENERAL DESCRIPTION

The XCM519 series is a multi combination module IC which comprises of a 600mA driver transistor built-in synchronous step–down DC/DC converter and a low voltage input LDO regulator. The device is housed in small USP-12B01 package which is ideally suited for space conscious applications. Battery operated portable products require high efficiency so that a dual DC/DC converter is often used. The XCM519 can replace this dual DC/DC to eliminate one inductor and reduce output noise. The DC/DC converter and the LDO regulator blocks are isolated in the package so that noise interference from the DC/DC to the LDO regulator is minimal.
A low output voltage and low On-resistance LDO regulator is added in series to the DC/DC output so that one another low output voltage is created with a high efficiency and low noise. With comparison to the dual DC/DC solution, one inductor can be eliminated which results in parts reduction and board space saving.

■APPLICATIONS

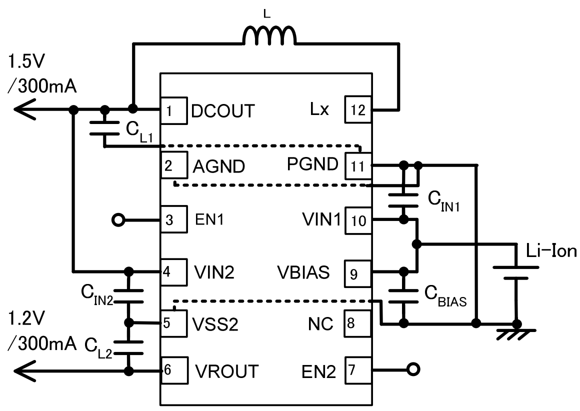
●Mobile phones, Smart phones

●Bluetooth equipment

●Portable communication modems

●Portable game consoles

■ TYPICAL APPLICATION CIRCUIT

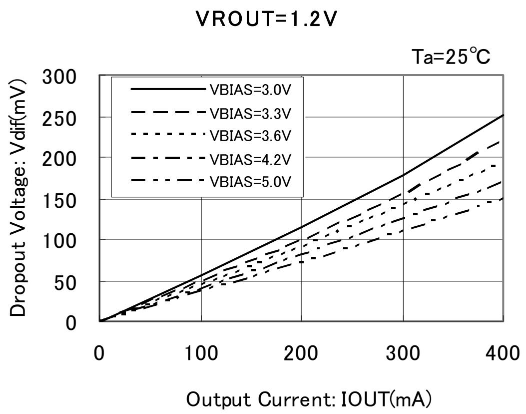


(TOP VIEW)

* The dashed lines denote the connection using through-holes at the backside of the PC board.

■TYPICAL PERFORMANCE CHARACTERISTICS

Dropout Voltage vs. Output Current



■FEATURES

<DC/DC Convertor Block>

Input Voltage Range : 2.7V ~ 6.0V
Output Voltage Range : 0.8V ~ 4.0V
High Efficiency : 92% (TYP.)
Output Current : 600mA (MAX.)
Oscillation Frequency : 1.2MHz, 3.0MHz (±15%)
Maximum Duty Cycle : 100%
Soft-Start Circuit Built-In
Current Limiter Circuit(Constant Current & Latching) Built-In
Control Methods : PWM (XCM519A)
PWM/PFM Auto (XCM519B)

*Performance depends on external components and wiring on PCB wiring.

<Regulator Block>

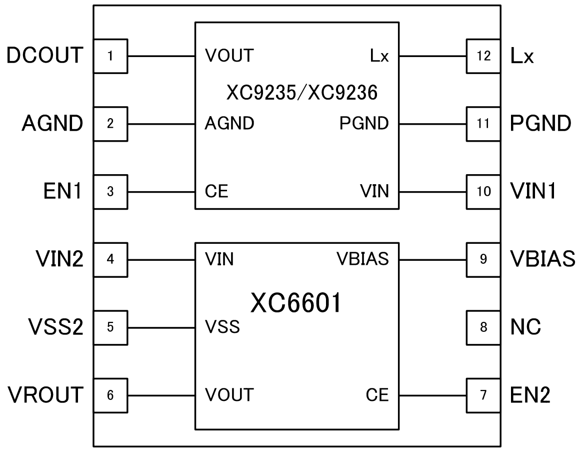
Maximum Output Current : 400mA (Limiter 550mA TYP.)
Dropout Voltage : 35mV@I_{OUT}=100mA (TYP.)
(at V_{BIAS} - $V_{ROUT(E)}$=2.4V)
Bias Voltage Range : 2.5V ~ 6.0V (V_{BIAS} - $V_{ROUT(E)}$=0.9V)
Input Voltage Range : 1.0V ~ 3.0V ($V_{IN2} \leqq V_{BIAS}$)
Output Voltage Range : 0.7V ~ 1.8V (0.05V increments)
High Output Accuracy : ±20mV
Supply Current : I_{BIAS}=25μA , I_{IN2}=1.0μA (TYP.)
Stand-by Current : I_{BIAS}=0.01μA , I_{IN2}=0.01μA (TYP.)
UVLO : V_{BIAS}=2.0V , V_{IN2}=0.4V (TYP)
Thermal Shut Down : Detect 150℃, Release 125℃ (TYP.)
Soft-start Time : 240μs@V_{ROUT}=1.2V(TYP.)
C_L High Speed Auto-Discharge

Low ESR Capacitor : Ceramic Capacitor Compatible
Operating Temperature Range : -40℃ ~ +85℃
Package : USP-12B01

Standard Voltage Combinations	DC/DC	VR
XCM519xx01Dx	1.8V	1.2V
XCM519xx02Dx	1.8V	1.5V
XCM519xx03Dx	1.5V	1.2V
XCM519xx04Dx	1.8V	1.0V
XCM519xx05Dx	1.5V	1.0V

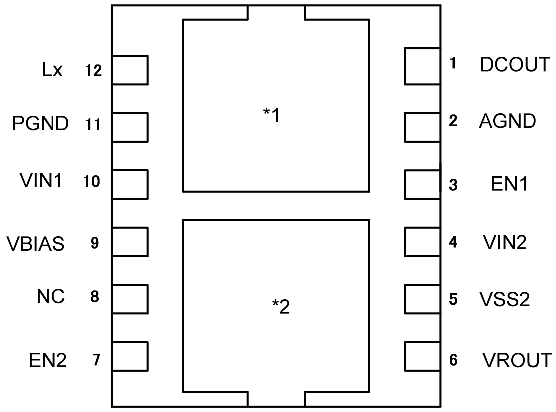
*Other combinations are available as semi-custom products.

■PIN CONFIGURATIOIN



(TOP VIEW)

PIN No.	XCM519	XC9235/XC9236	XC6601
1	DCOUT	V_{OUT}	—
2	AGND	AGND	—
3	EN1	CE	—
4	V_{IN2}	—	V_{IN}
5	V_{SS2}	—	V_{SS}
6	VROUT	—	V_{OUT}
7	EN2	—	CE
8	NC	—	—
9	V_{BIAS}	—	V_{BIAS}
10	V_{IN1}	V_{IN}	—
11	PGND	PGND	—
12	Lx	Lx	—



(BOTTOM VIEW)

NOTE:
* A dissipation pad on the reverse side of the package should be electrically isolated.
*1: Electrical potential of the XC9235/XC9236's dissipation pad should be V_{SS} level.
*2: Electrical potential of the XC6601's dissipation pad should be V_{SS} level.
Care must be taken for an electrical potential of each dissipation pad so as to enhance mounting strength and heat release when the pad needs to be connected to the circuit.

■PIN ASSIGNMENT

PIN No	XCM519	FUNCTIONS
1	DCOUT	DC/DC Block: Output Voltage
2	AGND	DC/DC Block: Analog Ground
3	EN1	DC/DC Block: Chip Enable
4	V_{IN2}	Voltage Regulator Block: Power Input
5	V_{SS2}	Voltage Regulator Block: Ground
6	VROUT	Voltage Regulator Block: Output
7	EN2	Voltage Regulator Block: Enable
8	NC	No Connection
9	V_{BIAS}	Voltage Regulator Block: Power Input
10	V_{IN1}	DC/DC Block: Power Input
11	PGND	DC/DC Block: Power Ground
12	Lx	DC/DC Block: Switching

■PRODUCT CLASSIFICATION

●Ordering Information

XCM519A①②③④⑤ DC/DC BLOCK：PWM fixed control

XCM519B①②③④⑤ DC/DC BLOCK：PWM/PFM automatic switching control

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Oscillation Frequency and Options	–	See the chart below
② ③	Output Voltage	–	Internally set sequential number relating to output voltage (See the chart below)
④	Package	D	USP-12B01
⑤	Device Orientation	R	Embossed tape, standard feed

●DESIGNATOR①

①	DC/DC BLOCK			Voltage Regulator BLOCK
	OSCILLATION FREQUENCY	C_L AUTO DISCHARGE	SOFT START	Pull-down
A	1.2M	Not Available	Standard	Not Available
B	3.0M	Not Available	Standard	Not Available
C	1.2M	Available	High Speed	Not Available
D	3.0M	Available	High Speed	Not Available

●DESIGNATOR②③

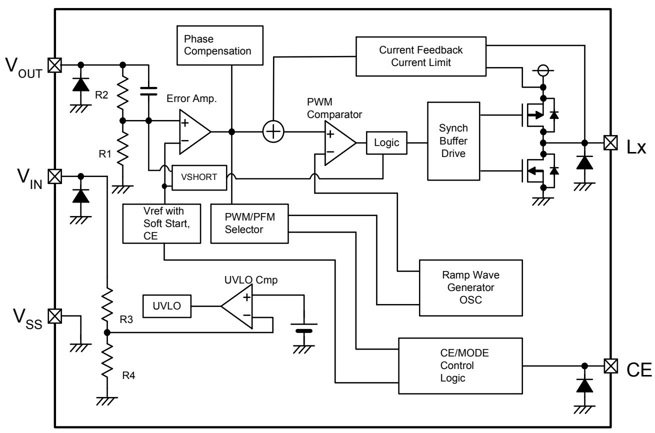
②③	DCOUT	VROUT
01	1.8V	1.2V
02	1.8V	1.5V
03	1.5V	1.2V
04	1.8V	1.0V
05	1.5V	1.0V

*When the DCOUT pin is connected to V_{IN2}, DCOUT pin output voltage can be fixed in the range of 1.0V～3.0V.

*This series are semi-custom products. For other combinations of output voltages please consult with your Torex sales contact.

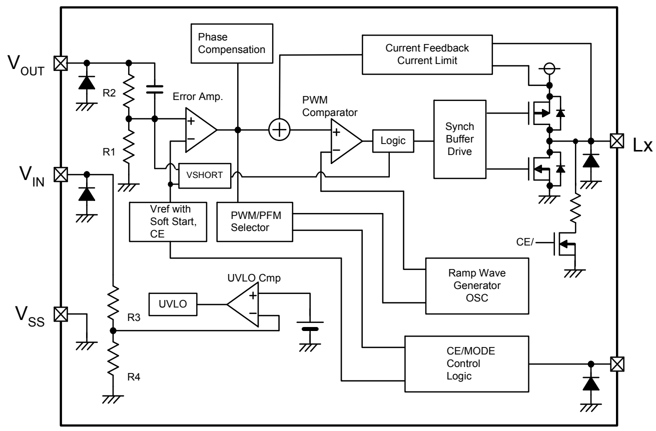
■BLOCK DIAGRAMS

XC9235A/XC9236A

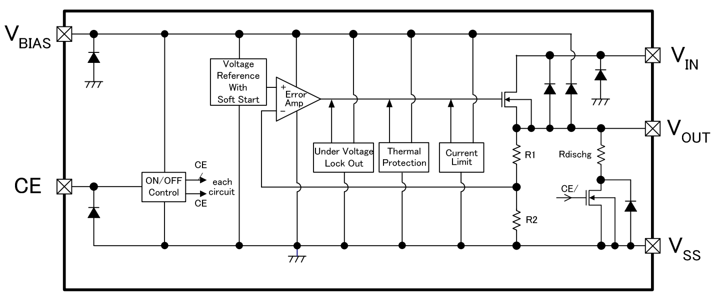


XC9235B/XC9236B

Available with C_L Discharge, High Speed Soft-Start



XC6601B (Without Pull-down)



* XC9235 control scheme is a fixed PWM because that the “CE/MODE Control Logic” outputs a low level signal to the “PWM/PFM Selector”.
* XC9236 control scheme is an auto PWM/PFM switching because the “CE/MODE Control Logic” outputs a high level signal to the “PWM/PFM Selector”.
*Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■MAXIMUM ABSOLUTE RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
V_{IN1}Voltage		V_{IN1}	- 0.3 ～ 6.5	V
Lx Voltage		V_{Lx}	- 0.3 ～ V_{IN1} + 0.3 or 6.5	V
DCOUT Voltage		V_{DCOUT}	- 0.3 ～ 6.5	V
EN1 Voltage		V_{EN1}	- 0.3 ～ 6.5	V
Lx Current		I_{Lx}	±1500	mA
V_{BIAS} Voltage		V_{BIAS}	V_{SS} - 0.3 ～ 7.0	V
V_{IN2} Voltage		V_{IN2}	V_{SS} - 0.3 ～ 7.0	V
VROUT Current		I_{VROUT}	700 (*1)	mA
VROUT Voltage		V_{ROUT}	V_{SS} - 0.3～V_{BIAS} + 0.3	V
			V_{SS} - 0.3～V_{IN2} + 0.3	
EN2 Voltage		V_{EN2}	V_{SS} - 0.3 ～ 6.5	V
Power Dissipation (Ta=25℃)	USP-12B01	Pd	150	mW
Junction Temperature		Tj	125	℃
Operating Temperature Range		Topr	-40～+85	℃
Storage Temperature Range		Tstg	-55～+125	℃

(*1) I_{VROUT}=Less than Pd / (V_{IN2}-V_{ROUT})

■ELECTRICAL CHARACTERISTICS

●XCM519xA (DC/DC BLOCK) V_{DCOUT}=1.8V, f_{OSC}=1.2MHz, Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage	V_{DCOUT}	When connected to external components, V_{IN1} = V_{EN1} =5.0V, I_{OUT1} =30mA	1.764	1.800	1.836	V	①
Operating Voltage Range	V_{IN1}		2.7	-	6.0	V	①
Maximum Output Current	$I_{OUT1MAX}$	When connected to external components, V_{IN1}=DCOUT(E)+2.0V, V_{EN1}=1.0V (*8)	600	-	-	mA	①
UVLO Voltage	V_{UVLO}	V_{EN1}=V_{IN1}, DCOUT=0V, Voltage which Lx pin holding “L” level (*1, *10)	1.00	1.40	1.78	V	③
Supply Current	I_{DD}	V_{IN1}=V_{EN1}=5.0V, DCOUT=DCOUT(E)×1.1V (XCM519AA)	-	22	50	②	–
		V_{IN1}=V_{EN1}=5.0V, DCOUT=DCOUT(E)×1.1V (XCM519BA)	-	15	33		
Stand-by Current	I_{STB}	V_{IN1}=5.0V, V_{EN1}=0V, DCOUT=DCOUT(E)×1.1V	-	0	1.0	μA	②
Oscillation Frequency	f_{OSC}	When connected to external components, V_{IN1}=DCOUT(E)+2.0V,V_{EN1}=1.0V, I_{OUT1}=100mA (*11)	1020	1200	1380	kHz	①
PFM Switching Current	I_{PFM}	When connected to external components, V_{IN1}=$V_{DCOUT(E)}$+2.0V, V_{EN1} =V_{IN1}, I_{OUT1}=1mA (*11)	120	160	200	mA	①
PFM Duty Limit	D_{LIMIT_PFM}	V_{EN1}=V_{IN1}=(C-1), I_{OUT1}=1mA (*11)	-	200	-	%	①
Maximum Duty Ratio	D_{MAX}	V_{IN1}= V_{EN1} =5.0V, DCOUT=DCOUT(E)×0.9V	100	-	-	%	②
Minimum Duty Ratio	D_{MIN}	V_{IN1}= V_{EN1} =5.0V, DCOUT=DCOUT(E)×1.1V	-	-	0	%	②
Efficiency (*2)	EFFI	When connected to external components, V_{EN1}=V_{IN1}=DCOUT(E)+1.2V (*7), I_{OUT1} =100mA	-	92	-	%	①
Lx SW "H" ON Resistance 1	R_{LXH}	V_{IN1}= V_{EN1} =5.0V, DCOUT=0V,I_{LX}=100mA (*3)	-	0.35	0.55	Ω	④
Lx SW "H" ON Resistance 2	R_{LXH}	V_{IN1}= V_{EN1} =3.6V, DCOUT=0V,I_{LX}=100mA (*3)	-	0.42	0.67	Ω	④
Lx SW "L" ON Resistance 1	R_{LXL}	V_{IN1}= V_{EN1} =5.0V (*4)	-	0.45	0.66	Ω	–
Lx SW "L" ON Resistance 2	R_{LXL}	V_{IN1}= V_{EN1}=3.6V (*4)	-	0.52	0.77	Ω	–
Lx SW "H" Leak Current (*5)	I_{LEAKH}	V_{IN1}= DCOUT=5.0V, V_{EN1} =0V, V_{LX}=0V	-	0.01	1.0	μA	⑤
Lx SW "L" Leak Current (*5)	I_{LEAKL}	V_{IN1}= DCOUT=5.0V, V_{EN1} =0V, V_{LX}=5.0V	-	0.01	1.0	μA	⑤
Current Limit (*9)	I_{LIM}	V_{IN1}=V_{EN1}=5.0V, DCOUT=DCOUT(E)×0.9V	900	1050	1350	mA	⑥
Output Voltage Temperature Characteristics	△DCOUT / (DCOUT•△topr)	I_{OUT1} =30mA -40℃≦Topr≦85℃	-	±100	-	ppm/ ℃	①
EN1 "H" Level Voltage	V_{EN1H}	DCOUT=0V, Applied voltage to V_{EN}, Voltage changes Lx to “H” level (*10)	0.65	-	6.0	V	③
EN1 "L" Level Voltage	V_{EN1L}	DCOUT=0V, Applied voltage to V_{EN}, Voltage changes Lx to “L” level (*10)	V_{SS}	-	0.25	V	③
EN1 "H" Current	I_{EN1H}	V_{IN1}=V_{EN1}=5.0V, DCOUT=0V	- 0.1	-	0.1	μA	⑤
EN1 "L" Current	I_{EN1L}	V_{IN1}=5.0V, V_{EN1} =0V, DCOUT=0V	- 0.1	-	0.1	μA	⑤
Soft Start Time	t_{SS}	When connected to external components, V_{EN1} =0V → V_{IN1}, I_{OUT1}=1mA	0.5	1.0	2.5	ms	①
Latch Time	t_{LAT}	V_{IN}= V_{EN}=5.0V, DCOUT=0.8× DCOUT(E) Short Lx at 1Ω resistance (*6)	1.0	-	20.0	ms	⑦
Short Protection Threshold Voltage	V_{SHORT}	Sweeping DCOUT, V_{IN1}=V_{EN1}= 5.0V, Short Lx at 1Ω resistance, DCOUT voltage which Lx becomes “L” level within 1ms	0.675	0.900	1.125	V	⑦

Test conditions: Unless otherwise stated, V_{IN} = 5.0V, $V_{DCOUT(E)}$= Setting voltage

NOTE:

*1: Including hysteresis width of operating voltage.

*2: EFFI = { (output voltage×output current) / (input voltage×input current) }×100

*3: ON resistance (Ω)= (V_{IN} - Lx pin measurement voltage) / 100mA

*4: Design value

*5: When temperature is high, a current of approximately 10μA (maximum) may leak.

*6: Time until it short-circuits DCOUT with GND via 1Ω of resistor from an operational state and is set to Lx=0V from current limit pulse generating.

*7: $V_{DCOUT (E)}$+1.2V<2.7V, V_{IN}=2.7V.

*8: When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.

*9: Current limit denotes the level of detection at peak of coil current.

*10: "H"=V_{IN}~V_{IN} - 1.2V, "L"=+ 0.1V ~ - 0.1V

*11: XCM519A series exclude I_{PFM} and $MAXI_{PFM}$ because those are only for the PFM control’s functions.

* The electrical characteristics above are when the other channel is in stop mode.

■ELECTRICAL CHARACTERISTICS (Continued)

●XCM519xB 1ch (DC/DC BLOCK) V_{DCOUT}=1.8V, f_{OSC}=3.0MHz, Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage	V_{DCOUT}	When connected to external components, V_{IN1} = V_{EN1} =5.0V, I_{OUT1} =30mA	1.764	1.800	1.836	V	①
Operating Voltage Range	V_{IN1}		2.7	-	6.0	V	①
Maximum Output Current	$I_{OUT1MAX}$	When connected to external components, V_{IN1}=$V_{DCOUT(E)}$+2.0V, V_{EN1}=1.0V (*8)	600	-	-	mA	①
UVLO Voltage	V_{UVLO}	V_{EN1}=$V_{IN1,}$ DCOUT=0V, Voltage which Lx pin holding "L" level (*1, *10)	1.00	1.40	1.78	V	③
Supply Current	I_{DD}	V_{IN1}=V_{EN1}=5.0V, DCOUT=DCOUT(E)×1.1V (XCM519AB)	-	46	65	②	–
		V_{IN1}=V_{EN1}=5.0V, DCOUT=DCOUT(E)×1.1V (XCM519BB)	-	21	35	②	–
Stand-by Current	I_{STB}	V_{IN1}=5.0V, V_{EN1}=0V, DCOUT=DCOUT(E)×1.1V	-	0	1.0	μA	②
Oscillation Frequency	f_{OSC}	When connected to external components, V_{IN1}=DCOUT(E)+2.0V,V_{EN1}=1.0V, I_{OUT1}=100mA	2550	3000	3450	kHz	①
PFM Switching Current	I_{PFM}	When connected to external components, V_{IN1}=DCOUT(E)+2.0V, V_{EN1} =V_{IN1}, I_{OUT1}=1mA (*11)	170	220	270	mA	①
PFM Duty Limit	D_{LIMIT_PFM}	V_{EN1}=V_{IN1}=(C-1) I_{OUT1}=1mA (*11)	-	200	300	%	①
Maximum Duty Ratio	D_{MAX}	V_{IN1}=V_{EN1} =5.0V, DCOUT=DCOUT(E)×0.9V	100	-	-	%	②
Minimum Duty Ratio	D_{MIN}	V_{IN1}=V_{EN1} =5.0V, DCOUT=DCOUT(E)×1.1V	-	-	0	%	②
Efficiency	EFFI	When connected to external components, V_{EN1}=V_{IN1}＝DCOUT(E)+1.2V, I_{OUT1} =100mA	-	86	-	%	①
Lx SW "H" ON Resistance 1	R_{LXH}	V_{IN1}= V_{EN1} =5.0V, DCOUT=0V,I_{LX}=100mA (*3)	-	0.35	0.55	Ω	④
Lx SW "H" ON Resistance 2	R_{LXH}	V_{IN1}= V_{EN1} =3.6V, DCOUT=0V,I_{LX}=100mA (*3)	-	0.42	0.67	Ω	④
Lx SW "L" ON Resistance 1	R_{LXL}	V_{IN1}= V_{EN1} =5.0V (*4)	-	0.45	0.66	Ω	–
Lx SW "L" ON Resistance 2	R_{LXL}	V_{IN1}= V_{EN1}=3.6V (*4)	-	0.52	0.77	Ω	–
Lx SW "H" Leak Current (*5)	I_{LEAKH}	V_{IN1}= DCOUT=5.0V, V_{EN1} =0V, V_{LX}=0V	-	0.01	1.0	μA	⑤
Lx SW "L" Leak Current (*5)	I_{LEAKL}	V_{IN1}= DCOUT=5.0V, V_{EN1} =0V, V_{LX}=5.0V	-	0.01	1.0	μA	⑤
Current Limit (*9)	I_{LIM}	V_{IN1}=V_{EN1}=5.0V, DCOUT=DCOUT(E)×0.9V	900	1050	1350	mA	⑥
Output Voltage Temperature Characteristics	△DCOUT / (DCOUT・△topr)	I_{OUT1} =30mA -40℃≦Topr≦85℃	-	±100	-	ppm/ ℃	①
EN1 "H" Level Voltage	V_{EN1H}	DCOUT=0V, Applied voltage to $V_{EN,}$ Voltage changes Lx to "H" level (*10)	0.65	-	6.0	V	③
EN1 "L" Level Voltage	V_{EN1L}	DCOUT=0V, Applied voltage to $V_{EN,}$ Voltage changes Lx to "L" level (*10)	V_{SS}	-	0.25	V	③
EN1 "H" Current	I_{EN1H}	V_{IN1}=V_{EN1}=5.0V, DCOUT=0V	- 0.1	-	0.1	μA	⑤
EN1 "L" Current	I_{EN1L}	V_{IN1}=5.0V, V_{EN1} =0V, DCOUT=0V	- 0.1	-	0.1	μA	⑤
Soft Start Time	t_{SS}	When connected to external components, V_{EN1} =0V → V_{IN1}, I_{OUT1}=1mA	0.5	0.9	2.5	ms	①
Latch Time	t_{LAT}	V_{IN1}=V_{EN1}=5.0V, DCOUT=0.8×DCOUT(E) Short Lx at 1Ω resistance (*6)	1.0	-	20	ms	⑦
Short Protection Threshold Voltage	V_{SHORT}	Sweeping DCOUT, V_{IN1}=V_{EN1}=5.0V, Short Lx at 1Ω resistance, DCOUT voltage which Lx becomes "L" level within 1ms	0.675	0.900	1.125	V	⑦

Test conditions: Unless otherwise stated, V_{IN1}=5.0V, $V_{DCOUT(E)}$= Nominal voltage

NOTE:

*1: Including hysteresis width of operating voltage.
*2: EFFI = { (output voltage×output current) / (input voltage×input current) }×100
*3: ON resistance (Ω)= (V_{IN} - Lx pin measurement voltage) / 100mA
*4: Design value
*5: When temperature is high, a current of approximately 10μA (maximum) may leak.
*6: Time until it short-circuits DCOUT with GND via 1Ω of resistor from an operational state and is set to Lx=0V from current limit pulse generating.
*7: $V_{DCOUT(E)}$+1.2V<2.7V, V_{IN}=2.7V.
*8: When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.
*9: Current limit denotes the level of detection at peak of coil current.
*10: "H"＝V_{IN}～V_{IN} - 1.2V, "L"＝+ 0.1V ～ - 0.1V
*11: XCM519A series exclude I_{PFM} and D_{LIMIT_PFM} because those are only for the PFM control's functions.
* The electrical characteristics above are when the other channel is in stop mode.

■ELECTRICAL CHARACTERISTICS (Continued)

●XCM519xC 1ch (DC/DC BLOCK) V_{DCOUT}=1.8V, f_{OSC}=1.2MHz, Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage	V_{DCOUT}	When connected to external components, V_{IN1}=V_{EN1}=5.0V,I_{OUT1}=30mA	1.764	1.800	1.836	V	①
Operating Voltage Range	V_{IN1}		2.7	-	6.0	V	①
Maximum Output Current	$I_{OUT1MAX}$	When connected to external components, V_{IN1}=DCOUT(E)V+2.0V,V_{EN1}=1.0V (*8)	600	-	-	mA	①
UVLO Voltage	V_{UVLO}	V_{EN1}=V_{IN1}, DCOUT=0V, Voltage which Lx pin holding "L" level (*1, *10)	1.00	1.40	1.78	V	②
Supply Current	I_{DD}	V_{IN1}=V_{EN1}=5.0V,DCOUT=DCOUT(E)×1.1V (XCM519AC)	-	22	50	μA	③
		V_{IN1}=V_{EN1}=5.0V,DCOUT=DCOUT(E)×1.1V (XCM519BC)	-	15	33	μA	③
Stand-by Current	I_{STB}	V_{IN1}=5.0V,V_{EN1}=0V,DCOUT=DCOUT(E)×1.1V	-	0	1.0	μA	③
Oscillation Frequency	f_{OSC}	When connected to external components, V_{IN1}=DCOUT(E)V+2.0V,V_{EN1}=1.0V, I_{OUT1}=100mA	1020	1200	1380	kHz	①
PFM Switching Current	I_{PFM}	When connected to external components, V_{IN1}=DCOUT(E)V+2.0V,V_{EN1}=V_{IN1}, I_{OUT1}=1mA (*11)	120	160	200	mA	①
PFM Duty Limit	D_{LIMIT_PFM}	V_{EN1}=V_{IN1}=(C-1)I_{OUT1}=1mA (*11)	-	200		%	②
Maximum Duty Ratio	D_{MAX}	V_{IN1}=V_{EN1}=5.0V,DCOUT=DCOUT(E)×0.9V	100	-	-	%	②
Minimum Duty Ratio	D_{MIN}	V_{IN1}=V_{EN1}=5.0V,DCOUT=DCOUT(E)×1.1V	-	-	0	%	②
Efficiency	EFFI	When connected to external components, V_{EN1}=V_{IN1}＝DCOUT(E)+1.2V (*7), I_{OUT1}=100mA	-	92	-	%	①
Lx SW "H" ON Resistance 1	RL_XH	V_{IN1}=V_{EN1}=5.0V,DCOUT=0V,IL_X=100mA (*3)	-	0.35	0.55	Ω	④
Lx SW "H" ON Resistance 2	RL_XH	V_{IN1}=V_{EN1}=3.6V,DCOUT=0V,IL_X=100mA (*3)	-	0.42	0.67	Ω	④
Lx SW "L" ON Resistance 1	RL_XL	V_{IN1}=V_{EN1}=5.0V (*4)	-	0.45	0.66	Ω	－
Lx SW "L" ON Resistance 2	RL_XL	V_{IN1}=V_{EN1}=3.6V (*4)	-	0.52	0.77	Ω	－
Lx SW "H" Leak Current (*5)	I_{LEAKH}	V_{IN1}=DCOUT=5.0V,V_{EN1}=0V,L_X=0V	-	0.01	1.0	μA	⑨
Current Limit (*9)	I_{LIM}	V_{IN1}=V_{EN1}=5.0V,DCOUT=DCOUT(E)×0.9V	900	1050	1350	mA	⑥
Output Voltage Temperature Characteristics	△DCOUT / (DCOUT•△topr)	I_{OUT1}=30mA, -40℃≦Topr≦85℃	-	±100	-	ppm/℃	①
EN1 "H" Level Voltage	V_{EN1H}	DCOUT=0V, Applied voltage to V_{EN1}, Voltage changes Lx to "H" level (*10)	0.65	-	6.0	V	③
EN1 "L" Level Voltage	V_{EN1L}	DCOUT=0V, Applied voltage to V_{EN1}, Voltage changes Lx to "L" level (*10)	V_{SS}	-	0.25	V	③
EN1 "H" Current	I_{EN1H}	V_{IN1}=V_{EN1}=5.0V,DCOUT=0V	- 0.1	-	0.1	μA	⑤
EN1 "L" Current	I_{EN1L}	V_{IN1}=5.0V,V_{EN1}=0V,DCOUT=0V	- 0.1	-	0.1	μA	⑤
Soft Start Time	t_{SS}	When connected to external components, V_{EN1}=0V→V_{IN1}, I_{OUT1}=1mA	-	0.25	0.40	ms	①
Latch Time	T_{LAT}	V_{IN1}=V_{EN1}=5.0V, DCOUT=0.8×DCOUT(E) Short Lx at 1Ω resistance (*6)	1.0	-	20	ms	⑦
Short Protection Threshold Voltage	V_{SHORT}	Sweeping DCOUT, V_{IN1}=V_{EN1}=5.0V, Short Lx at 1Ω resistance, DCOUT voltage which Lx becomes "L" level within 1ms	0.675	0.900	1.150	V	⑦
C_L Discharge	R_{DCHG}	V_{IN1}=5.0V, L_X=5.0V,V_{EN1}=0V, DCOUT=Open	200	300	450	Ω	⑧

Test conditions: Unless otherwise stated, V_{IN1}=5.0V, $V_{DCOUT(E)}$= Nominal voltage

NOTE:

*1: Including hysteresis width of operating voltage.
*2: EFFI = { (output voltage×output current) / (input voltage×input current) }×100
*3: ON resistance (Ω)= (V_{IN} - Lx pin measurement voltage) / 100mA
*4: Design value
*5: When temperature is high, a current of approximately 10μA (maximum) may leak.
*6: Time until it short-circuits DCOUT with GND via 1Ω of resistor from an operational state and is set to Lx=0V from current limit pulse generating.
*7: $V_{DCOUT (E)}$+1.2V<2.7V, V_{IN}=2.7V.
*8: When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.
*9: Current limit denotes the level of detection at peak of coil current.
*10: "H"＝V_{IN}～V_{IN} - 1.2V, "L"＝+ 0.1V ～ - 0.1V
*11: XCM519A series exclude I_{PFM} and D_{LIMT_PFM} because those are only for the PFM control's functions.

* The electrical characteristics above are when the other channel is in stop mode.

■ELECTRICAL CHARACTERISTICS (Continued)

●XCM519xD 1ch (DC/DC BLOCK) DCOUT=1.8V, f_{OSC}=3.0MHz, Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage	V_{DCOUT}	When connected to external components, V_{IN1}=V_{EN1}=5.0V, I_{OUT1}=30mA	1.764	1.800	1.836	V	①
Operating Voltage Range	V_{IN1}		2.7	-	6.0	V	①
Maximum Output Current	$I_{OUT1MAX}$	When connected to external components, V_{IN1}=DCOUT(E)V+2.0V,V_{EN1}=1.0V (*8)	600	-	-	mA	①
UVLO Voltage	V_{UVLO}	V_{EN1}=V_{IN1}, DCOUT=0V, Voltage which Lx pin holding "L" level (*1, *10)	1.00	1.40	1.78	V	②
Supply Current	I_{DD}	V_{IN1}=V_{EN1}=5.0V,DCOUT=DCOUT(E)×1.1V (XCM519AD)	-	46	65	μA	③
		V_{IN1}=V_{EN1}=5.0V,DCOUT=DCOUT(E)×1.1V (XCM519BD)	-	21	35	μA	③
Stand-by Current	I_{STB}	V_{IN1}=5.0V,V_{EN1}=0V, DCOUT=DCOUT(E)×1.1V	-	0	1.0	μA	③
Oscillation Frequency	f_{OSC}	When connected to external components, V_{IN1}=DCOUT(E)V+2.0V, V_{EN1}=1.0V, I_{OUT1}=100mA	2550	3000	3450	kHz	①
PFM Switching Current	I_{PFM}	When connected to external components, V_{IN1}=DCOUT(E)V+2.0V, V_{EN1}=V_{IN1}, I_{OUT1}=1mA (*11)	170	220	270	mA	①
PFM Duty Limit	D_{LIMIT_PFM}	V_{EN1}=V_{IN1}=(C-1)I_{OUT1}=1mA (*11)	-	200	300	%	②
Maximum Duty Ratio	D_{MAX}	V_{IN1}=V_{EN1}=5.0V, DCOUT=DCOUT(E)×0.9V	100	-	-	%	②
Minimum Duty Ratio	D_{MIN}	V_{IN1}=V_{EN1}=5.0V, DCOUT=DCOUT(E)×1.1V	-	-	0	%	②
Efficiency	EFFI	When connected to external components, V_{EN1}=V_{IN1}=DCOUT(E)+1.2V (*7),I_{OUT1}=100mA	-	86	-	%	①
Lx SW "H" ON Resistance 1	RL_XH	V_{IN1}=V_{EN1}=5.0V, DCOUT=0V, IL_X=100mA (*3)	-	0.35	0.55	Ω	④
Lx SW "H" ON Resistance 2	RL_XH	V_{IN1}=V_{EN1}=3.6V, DCOUT=0V, IL_X=100mA (*3)	-	0.42	0.67	Ω	④
Lx SW "L" ON Resistance 1	RL_XL	V_{IN1}=V_{EN1}=5.0V (*4)	-	0.45	0.66	Ω	−
Lx SW "L" ON Resistance 2	RL_XL	V_{IN1}=V_{EN1}=3.6V (*4)	-	0.52	0.77	Ω	−
Lx SW "H" Leak Current (*5)	I_{LEAKH}	V_{IN1}=DCOUT=5.0V,V_{EN1}=0V, L_X=0V	-	0.01	1.0	μA	⑨
Current Limit (*9)	I_{LIM}	V_{IN1}=V_{EN1}=5.0V, DCOUT=DCOUT(E)×0.9V	900	1050	1350	mA	⑥
Output Voltage Temperature Characteristics	△DCOUT / (DCOUT･△topr)	I_{OUT1}=30mA -40℃≦Topr≦85℃	-	±100	-	ppm/℃	①
EN1 "H" Level Voltage	V_{EN1H}	DCOUT=0V, Applied voltage to V_{EN1}, Voltage changes Lx to "H" level (*10)	0.65	-	6.0	V	③
EN1 "L" Level Voltage	V_{EN1L}	DCOUT=0V, Applied voltage to V_{EN1}, Voltage changes Lx to "L" level (*10)	V_{SS}	-	0.25	V	③
EN1 "H" Current	I_{EN1H}	V_{IN1}=V_{EN1}=5.0V, DCOUT=0V	- 0.1	-	0.1	μA	⑤
EN1 "L" Current	I_{EN1L}	V_{IN1}=5.0V,V_{EN1}=0V, DCOUT=0V	- 0.1	-	0.1	μA	⑤
Soft Start Time	t_{SS}	When connected to external components, V_{EN1}=0V→V_{IN1}, I_{OUT1}=1mA	-	0.32	0.50	ms	①
Latch Time	t_{LAT}	V_{IN1}=V_{EN1}=5.0V, DCOUT=0.8×DCOUT(E) Short Lx at 1Ω resistance (*6)	1.0	-	20	ms	⑦
Short Protection Threshold Voltage	V_{SHORT}	Sweeping DCOUT, V_{IN1}=V_{EN1}=5.0V, Short Lx at 1Ω resistance, DCOUT voltage which Lx becomes "L" level within 1ms	0.675	0.900	1.150	V	⑦
C_L Discharge	R_{DCHG}	V_{IN1}=5.0V, L_X=5.0V, V_{EN1}=0V, DCOUT=Open	200	300	450	Ω	⑧

Test conditions: Unless otherwise stated, V_{IN1}=5.0V, $V_{DCOUT(E)}$= Nominal voltage

NOTE:

*1: Including hysteresis width of operating voltage.
*2: EFFI = { (output voltage×output current) / (input voltage×input current) }×100
*3: ON resistance (Ω)= (V_{IN} - Lx pin measurement voltage) / 100mA
*4: Design value
*5: When temperature is high, a current of approximately 10μA (maximum) may leak.
*6: Time until it short-circuits DCOUT with GND via 1Ω of resistor from an operational state and is set to Lx=0V from current limit pulse generating.
*7: $V_{DCOUT (E)}$+1.2V<2.7V, V_{IN}=2.7V.
*8: When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.
*9: Current limit denotes the level of detection at peak of coil current.
*10: "H"＝V_{IN}〜V_{IN} - 1.2V, "L"＝+ 0.1V 〜 - 0.1V
*11: XCM519A series exclude I_{PFM} and D_{LIMT_PFM} because those are only for the PFM control's functions.

* The electrical characteristics above are when the other channel is in stop mode.

■ELECTRICAL CHARACTERISTICS (Continued)

●PFM Switching Current (I_{PFM}) by Oscillation Frequency and Output Voltage

1.2MHz (mA)

SETTING VOLTAGE	MIN.	TYP.	MAX.
$V_{DCOUT(E)} \leqq 1.2V$	140	180	240
$1.2V < V_{DCOUT(E)} \leqq 1.75V$	130	170	220
$1.8V \leqq V_{DCOUT(E)}$	120	160	200

3.0MHz (mA)

SETTING VOLTAGE	MIN.	TYP.	MAX.
$V_{DCOUT(E)} \leqq 1.2V$	190	260	350
$1.2V < V_{DCOUT(E)} \leqq 1.75V$	180	240	300
$1.8V \leqq V_{DCOUT(E)}$	170	220	270

●Measuring Maximum I_{PFM} Limit, V_{IN} Voltage

f_{OSC}	1.2MHz	3.0MHz
(C-1)	$V_{DCOUT(E)}$+0.5V	$V_{DCOUT(E)}$+1.0V

Minimum operating voltage is 2.7V

ex.) Although when $V_{DCOUT(E)}$=1.2V, f_{OSC}=1.2MHz, (C-1)=1.7V the (C-1) becomes 2.7V because of the minimum operating voltage 2.7V.

●Soft-Start Time Chart (XCM519xC/ XCM519xD Series Only)

PRODUCT SERIES	f_{OSC}	OUTPUT VOLTAGE	MIN.	TYP.	MAX.
XCM519AC	1200kHz	$0.8 \leqq V_{DCOUT(E)} < 1.5$	-	250	400μs
	1200kHz	$1.5 \leqq V_{DCOUT(E)} < 1.8$	-	320	500μs
	1200kHz	$1.8 \leqq V_{DCOUT(E)} < 2.5$	-	250	400μs
	1200kHz	$2.5 \leqq V_{DCOUT(E)} < 4.0$	-	320	500μs
XCM519BC	1200kHz	$0.8 \leqq V_{DCOUT(E)} < 2.5$	-	250	400μs
	1200kHz	$2.5 \leqq V_{DCOUT(E)} < 4.0$	-	320	500μs
XCM519xD	3000kHz	$0.8 \leqq V_{DCOUT(E)} < 1.8$	-	250	400μs
	3000kHz	$1.8 \leqq V_{DCOUT(E)} < 4.0$	-	320	500μs

■ELECTRICAL CHARACTERISTICS (Continued)

●XCM519xx 2ch (REGULATOR BLOCK)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Bias Voltage (*1)	V_{BIAS}	$V_{EN2}=V_{BIAS}$, $V_{IN2}=V_{ROUT(T)}+0.3V$	2.5	-	6.0	V	–
Input Voltage (*2)	V_{IN2}	$V_{BIAS}=V_{EN2}=3.6V$	1.0	-	3.0	V	–
Output Voltage	$V_{ROUT(E)}$ (*3)	$V_{BIAS}=V_{EN2}=3.6V$, $V_{IN2}=V_{ROUT(T)}+0.3V$, $IR_{OUT}=1mA$	-0.02	$V_{OUT(T)}$ (*4)	+0.02	V	–
			E-0 (*5)				
Maximum Output Current1	$I_{OUTMAX1}$	$V_{EN2}=V_{BIAS}$, $V_{BIAS}-V_{ROUT(T)}\geqq1.2V$ $V_{IN2}=V_{ROUT(T)}+0.5V$	200	-	-	mA	⑩
Maximum Output Current2	$I_{OUTMAX2}$	$V_{EN2}=V_{BIAS}$, $V_{BIAS}-V_{ROUT(T)}\geqq1.3V$ $V_{IN2}=V_{ROUT(T)}+0.5V$	300	-	-	mA	⑩
Maximum Output Current3	$I_{OUTMAX3}$	$V_{EN2}=V_{BIAS}$, $V_{BIAS}-V_{ROUT(T)}\geqq1.5V$ $V_{IN2}=V_{ROUT(T)}+0.5V$	400	-	-	mA	⑩
Load Regulation	△VROUT	$V_{BIAS}=V_{EN2}=3.6V$, $V_{IN2}=V_{ROUT(T)}+0.3V$, $1mA\leqq I_{VROUT}\leqq100mA$	-	8	17	mV	–
Dropout Voltage1	Vdif1 (*7)	$V_{EN2}=V_{BIAS}$, $I_{OUT}=100mA$	E-1 (*6)			mV	⑩
Dropout Voltage2	Vdif2 (*7)	$V_{EN2}=V_{BIAS}$, $I_{OUT}=200mA$	E-2 (*6)			mV	⑩
Dropout Voltage3	Vdif3 (*7)	$V_{EN2}=V_{BIAS}$, $I_{OUT}=300mA$	E-3 (*6)			mV	⑩
Dropout Voltage4	Vdif4 (*7)	$V_{EN2}=V_{BIAS}$, $I_{OUT}=400mA$	E-4 (*6)			mV	⑩
Supply Current 1	I_{BIAS}	$V_{BIAS}=V_{EN2}=3.6V$, $V_{IN2}=V_{ROUT(T)}+0.3V$ $V_{ROUT(T)}$=OPEN	8	25	45	μA	⑩
Supply Current 2	I_{IN2}	$V_{BIAS}=V_{EN2}=3.6V$, $V_{IN2}=V_{ROUT(T)}+0.3V$ $V_{ROUT(T)}$=OPEN	-	1.0	2.5	μA	⑩
Bias Current (*10)	$I_{BIASMAX}$	$V_{ROUT(T)}\geqq0.95V$, $V_{BIAS}=V_{EN2}=3.6V$, $V_{IN2}=V_{ROUT(T)}+0.05V$, $V_{ROUT}=V_{ROUT(T)}-0.05V$	-	1.0	2.5	mA	⑩
		$V_{ROUT(T)}<0.95V$, $V_{BIAS}=V_{EN2}=3.6V$, $V_{IN2}=1.0V$, $V_{ROUT}=V_{ROUT(T)}-0.05V$					
Stand-by Current 1	I_{BIAS_STB}	$V_{BIAS}=6.0V$, $V_{IN2}=3.0V$, $V_{EN2}=V_{SS2}$	-	0.01	0.10	μA	⑩
Stand-by Current 2	I_{IN_STB}	$V_{BIAS}=6.0V$, $V_{IN2}=3.0V$, $V_{EN2}=V_{SS2}$	-	0.01	0.35	μA	⑩
Bias Regulation	$\triangle V_{ROUT}/(\triangle V_{BIAS}\cdot V_{ROUT})$	$V_{ROUT(T)}\geqq1.3V$ $V_{ROUT(T)}+1.2V\leqq V_{BIAS}\leqq6.0V$, $V_{IN2}=V_{ROUT(T)}+0.3V$, $V_{EN2}=V_{BIAS}$, $I_{OUT}=1mA$	-	0.01	0.3	%/V	⑩
		$V_{ROUT(T)}<1.3V$ $2.5V\leqq V_{BIAS}\leqq6.0V$, $V_{IN2}=V_{ROUT(T)}+0.3V$, $V_{EN2}=V_{BIAS}$, $I_{OUT}=1mA$					
Input Regulation	$\triangle V_{ROUT}/(\triangle V_{IN2}\cdot V_{ROUT})$	$V_{ROUT(T)}\geqq0.90V$, $V_{ROUT(T)}+0.1V\leqq V_{IN2}\leqq3.0V$, $V_{BIAS}=V_{EN2}=3.6V$, $I_{OUT}=1mA$	-	0.01	0.1	%/V	⑩
		$V_{ROUT(T)}<0.90V$, $1.0V\leqq V_{IN2}\leqq3.0V$ $V_{BIAS}=V_{EN2}=3.6V$, $I_{OUT}=1mA$					
Bias Voltage UVLO	V_{BIAS_UVLO}	$V_{EN2}=V_{BIAS}$, $V_{IN2}=V_{ROUT(T)}+0.3V$, $I_{OUT}=1mA$	1.37	2.0	2.5	V	⑩
Input Voltage UVLO	V_{IN_UVLO}	$V_{BIAS}=V_{EN2}=3.6V$, $I_{VROUT}=1mA$	0.07	0.4	0.6	V	⑩
V_{BIAS} Ripple Rejection	V_{BIAS_PSRR}	$V_{BIAS}=3.6V_{DC}+0.2Vp\text{-}p_{AC}$, $V_{IN2}=V_{ROUT(T)}+0.3V$, $I_{OUT}=30mA$, f=1kHz	-	40	-	dB	⑪
V_{IN2} Ripple Rejection	V_{IN_PSRR}	$V_{IN2}=V_{OUT(T)}+0.3V_{DC}+0.2Vp\text{-}p_{AC}$, $V_{BIAS}=3.6V$, $I_{OUT}=30mA$, f=1kHz	-	60	-	dB	⑪

■ELECTRICAL CHARACTERISTICS (Continued)

●XCM519xx 2ch (REGULATOR BLOCK) (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage Temperature Characteristics	$\triangle V_{ROUT}$/ ($\triangle$Topr • V_{ROUT})	V_{BIAS}=V_{EN2}=3.6V, V_{IN2}=$V_{ROUT(T)}$+0.3V , I_{OUT}=30mA, - 40℃≦ Topr ≦85℃	-	±100	-	ppm/℃	⑩
Limit Current	I_{LIM}	V_{ROUT}=$V_{ROUT(T)}$×0.95, V_{BIAS}=V_{EN2}=3.6V, V_{IN2}=$V_{ROUT(T)}$+0.3V	400	-	-	mA	⑩
Short Current	I_{SHORT}	V_{BIAS}=V_{EN2}=3.6V, V_{IN2}=$V_{ROUT(T)}$+0.3V, V_{ROUT}=0V	-	80	-	mA	⑩
Thermal Shutdown Detect Temperature	T_{TSD}	Junction Temperature	-	150	-	℃	⑩
Thermal Shutdown Release Temperature	T_{TSR}	Junction Temperature	-	125	-	℃	⑩
TSD Hysteresis Width	$T_{TSD}-T_{TSR}$		-	25	-	℃	⑩
CL Auto-Discharge Resistance	R_{DCHG}	V_{BIAS}=3.6V, V_{IN2}= $V_{ROUT(T)}$+0.3V, V_{EN2}= V_{SS} V_{ROUT}=$V_{ROUT(T)}$	290	430	610	Ω	⑩
EN2 "H" Level Voltage	V_{EN2H}	V_{BIAS}=3.6V,V_{IN2}=$V_{ROUT(T)}$+0.3V	0.75	-	6.0	V	⑩
EN2 "L" Level Voltage	V_{EN2L}	V_{BIAS}=3.6V,V_{IN2}=$V_{ROUT(T)}$+0.3V	-	-	0.16	V	⑩
EN2 "H" Level Current	I_{EN2H}	V_{BIAS}=V_{EN2}=6.0V, V_{IN2}=$V_{ROUT(T)}$+0.3V	-0.1	-	0.1	μA	⑩
EN2 "L" Level Current	I_{EN2L}	V_{BIAS}=6.0V, V_{EN2}=V_{SS},V_{IN2}=$V_{ROUT(T)}$+0.3V	-0.1	-	0.1	μA	⑩
Soft Start Time (*11)	t_{SS}	V_{BIAS}=3.6V、V_{IN2}=$V_{ROUT(T)}$+0.3V、I_{OUT}=1mA V_{EN2}=0V→3.6V	100	-	410	μs	⑫

NOTE:
* 1: Please use Bias voltage V_{BIAS} within the range V_{BIAS}–$V_{ROUT(T)}$≧0.9V
* 2: Please use Input voltage V_{IN} within the range V_{IN}≦V_{BIAS}
* 3: $V_{ROUT(E)}$: Effective output voltage
* 4: $V_{ROUT(T)}$: Specified output voltage
* 5: E-0 = Please refer to the table named OUTPUT VOLTAGE CHART
* 6: E-1 = Please refer to the table named DROPOUT VOLTAGE CHART
* 7: Vdif={V_{IN21}(*8) -V_{ROUT1}(*9)}
* 8: V_{IN21} : The input voltage when V_{OUT1} appears as input voltage is gradually decreased.
* 9: V_{ROUT1} : A voltage equal to 98% of the output voltage while maintaining an amply stabilized output voltage when V_{BIAS}<3.0V at V_{IN2}= V_{BIAS}, V_{BIAS}≧3.0V at V_{IN2}=V_{BIAS} input to the V_{BIAS} pin.
*10 : $I_{BIASMAX}$: A supply current at the V_{BIAS} pin providing for the output current (I_{VROUT}) .
*11: t_{SS} : Time that V_{ROUT} becomes more than $V_{ROUT(E)}$×0.9V after the EN2 pin is input 0.75V as EN2 "H" level voltage.
* The electrical characteristics above are when the other channel is in stop mode.

■OUTPUT VOLTAGE CHART

NOMINAL OUTPUT VOLTAGE (V)	E-0 OUTPUT VOLTAGE (V) V_{ROUT}	
$V_{ROUT(T)}$	MIN.	MAX.
0.70	0.680	0.720
0.75	0.730	0.770
0.80	0.780	0.820
0.85	0.830	0.870
0.90	0.880	0.920
0.95	0.930	0.970
1.00	0.980	1.020
1.05	1.030	1.070
1.10	1.080	1.120
1.15	1.130	1.170
1.20	1.180	1.220
1.25	1.230	1.270

NOMINAL OUTPUT VOLTAGE (V)	E-0 OUTPUT VOLTAGE (V) V_{ROUT}	
$V_{ROUT(T)}$	MIN.	MAX.
1.30	1.280	1.320
1.35	1.330	1.370
1.40	1.380	1.420
1.45	1.430	1.470
1.50	1.480	1.520
1.55	1.530	1.570
1.60	1.580	1.620
1.65	1.630	1.670
1.70	1.680	1.720
1.75	1.730	1.770
1.80	1.780	1.820

■DROPOUT VOLTAGE CHART

NOMINAL OUTPUT VOLTAGE (V)	E-1 DROPOUT VOLTAGE1 (mV) Vdif1														
	V_{BIAS} =3.0(V)			V_{BIAS} =3.3(V)			V_{BIAS} =3.6(V)			V_{BIAS} =4.2(V)			V_{BIAS} =5.0(V)		
	Vgs(*1)	Vdif (mV)		Vgs	Vdif (mV)		Vgs	Vdif (mV)		Vgs	Vdif (mV)		Vgs	Vdif (mV)	
$V_{ROUT(T)}$	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.
0.70	2.30	40	300	2.60	35	300	2.90	33	300	3.50	30	300	4.30	27	300
0.75	2.25	41	250	2.55	36	250	2.85	34	250	3.45	31	250	4.25	28	250
0.80	2.20		200	2.50		200	2.80		200	3.40		200	4.20		200
0.85	2.15	42	150	2.45	38	150	2.75	34	150	3.35	31	150	4.15	28	150
0.90	2.10		100	2.40		100	2.70		100	3.30		100	4.10		100
0.95	2.05	43	68	2.35	40	61	2.65	35	56	3.25	32	50	4.05	28	50
1.00	2.00			2.30			2.60			3.20		49	4.00		44
1.05	1.95	46	72	2.25	41	63	2.55	36	58	3.15	32	50	3.95	29	45
1.10	1.90			2.20			2.50			3.10			3.90		
1.15	1.85	48	75	2.15	42	65	2.45	38	59	3.05	32	51	3.85	29	46
1.20	1.80			2.10			2.40			3.00			3.80		
1.25	1.75	51	81	2.05	43	68	2.35	40	61	2.95	33	52	3.75	29	47
1.30	1.70			2.00			2.30			2.90			3.70		
1.35	1.65	54	87	1.95	46	72	2.25	41	63	2.85	34	53	3.65	30	47
1.40	1.60			1.90			2.20			2.80			3.60		
1.45	1.55	57	92	1.85	48	75	2.15	42	65	2.75	34	54	3.55	30	48
1.50	1.50			1.80			2.10			2.70			3.50		
1.55	1.45	61	94	1.75	51	81	2.05	43	68	2.65	35	56	3.45	31	48
1.60	1.40	63	97	1.70			2.00			2.60			3.40		
1.65	1.35	67	104	1.65	54	87	1.95	46	72	2.55	36	58	3.35	31	49
1.70	1.30	70	113	1.60			1.90			2.50			3.30		
1.75	1.25	74	131	1.55	57	92	1.85	48	75	2.45	38	59	3.25	32	49
1.80	1.20	79	154	1.50			1.80			2.40			3.20		

*1): Vgs is a Gate –Source voltage of the driver transistor that is defined as the value of V_{BIAS} - $V_{ROUT\ (T)}$.

■DROPOUT VOLTAGE CHART (Continued)

NOMINAL OUTPUT VOLTAGE (V)	E-2 DROPOUT VOLTAGE 2 (mV) Vdif2														
	V_{BIAS} =3.0(V)			V_{BIAS} =3.3(V)			V_{BIAS} =3.6(V)			V_{BIAS} =4.2(V)			V_{BIAS} =5.0(V)		
	Vgs[(*1)]	Vdif (mV)		Vgs	Vdif (mV)		Vgs	Vdif (mV)		Vgs	Vdif (mV)		Vgs	Vdif (mV)	
$V_{ROUT(T)}$	(V)	TYP	MAX	(V)	TYP	MAX	(V)	TYP	MAX	(V)	TYP	MAX	(V)	TYP	MAX
0.70	2.30	81	300	2.60	74	300	2.90	68	300	3.50	62	300	4.30	57	300
0.75	2.25	85	250	2.55	76	250	2.85	70	250	3.45	63	250	4.25	58	250
0.80	2.20		200	2.50		200	2.80		200	3.40		200	4.20		200
0.85	2.15	88	150	2.45	78	150	2.75	72	150	3.35	63	150	4.15	58	150
0.90	2.10		131	2.40		117	2.70		110	3.30		100	4.10		100
0.95	2.05	90	139	2.35	81	123	2.65	74	111	3.25	64	98	4.05	58	88
1.00	2.00			2.30			2.60			3.20			4.00		
1.05	1.95	96	146	2.25	85	127	2.55	76	114	3.15	65	101	3.95	59	90
1.10	1.90			2.20			2.50			3.10			3.90		
1.15	1.85	101	154	2.15	88	131	2.45	78	117	3.05	67	103	3.85	59	91
1.20	1.80			2.10			2.40			3.00			3.80		
1.25	1.75	108	170	2.05	90	139	2.35	81	123	2.95	68	106	3.75	60	92
1.30	1.70			2.00			2.30			2.90			3.70		
1.35	1.65	115	179	1.95	96	146	2.25	85	127	2.85	70	108	3.65	61	93
1.40	1.60			1.90			2.20			2.80			3.60		
1.45	1.55	122	192	1.85	101	154	2.15	88	131	2.75	72	110	3.55	62	94
1.50	1.50			1.80			2.10			2.70			3.50		
1.55	1.45	129	197	1.75	108	170	2.05	90	139	2.65	74	111	3.45	63	95
1.60	1.40	135	206	1.70			2.00			2.60			3.40		
1.65	1.35	145	223	1.65	115	179	1.95	96	146	2.55	76	114	3.35	63	97
1.70	1.30	154	248	1.60			1.90			2.50			3.30		
1.75	1.25	165	293	1.55	122	192	1.85	101	154	2.45	78	117	3.25	64	98
1.80	1.20	175	353	1.50			1.80			2.40			3.20		

*1): Vgs is a Gate –Source voltage of the driver transistor that is defined as the value of V_{BIAS} - $V_{ROUT (T)}$.

■DROPOUT VOLTAGE CHART (Continued)

NOMINAL OUTPUT VOLTAGE (V)	E-3														
	DROPOUT VOLTAGE 3 (mV)														
	Vdif3														
	V_{BIAS} =3.0(V)			V_{BIAS} =3.3(V)			V_{BIAS} =3.6(V)			V_{BIAS} =4.2(V)			V_{BIAS} =5.0(V)		
	Vgs(*1) (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)	
$V_{VROUT(T)}$		TYP	MAX		TYP	MAX		TYP	MAX		TYP	MAX		TYP	MAX
0.70	2.30	130	300	2.60	115	300	2.90	107	300	3.50	95	300	4.30	89	300
0.75	2.25	134	250	2.55	117	250	2.85	109	250	3.45	96	250	4.25	90	250
0.80	2.20		200	2.50		200	2.80		200	3.40		200	4.20		200
0.85	2.15	138	204	2.45	119	181	2.75	111	167	3.35	97	150	4.15	90	150
0.90	2.10			2.40			2.70			3.30		148	4.10		132
0.95	2.05	145	216	2.35	130	190	2.65	115	170	3.25	98	151	4.05	91	134
1.00	2.00			2.30			2.60			3.20			4.00		
1.05	1.95	153	227	2.25	134	197	2.55	117	176	3.15	101	153	3.95	92	137
1.10	1.90			2.20			2.50			3.10			3.90		
1.15	1.85	161	239	2.15	138	204	2.45	119	181	3.05	105	155	3.85	93	139
1.20	1.80			2.10			2.40			3.00			3.80		
1.25	1.75	173	264	2.05	145	216	2.35	130	190	2.95	107	159	3.75	93	140
1.30	1.70			2.00			2.30			2.90			3.70		
1.35	1.65	184	289	1.95	153	227	2.25	134	197	2.85	109	163	3.65	94	141
1.40	1.60			1.90			2.20			2.80			3.60		
1.45	1.55	196	313	1.85	161	239	2.15	138	204	2.75	111	167	3.55	95	142
1.50	1.50			1.80			2.10			2.70			3.50		
1.55	1.45	209	323	1.75	173	264	2.05	145	216	2.65	115	170	3.45	96	145
1.60	1.40	222	344	1.70			2.00			2.60			3.40		
1.65	1.35	239	388	1.65	184	289	1.95	153	227	2.55	117	176	3.35	97	148
1.70	1.30	256	442	1.60			1.90			2.50			3.30		
1.75	1.25	-	-	1.55	196	313	1.85	161	239	2.45	119	181	3.25	98	151
1.80	1.20			1.50			1.80			2.40			3.20		

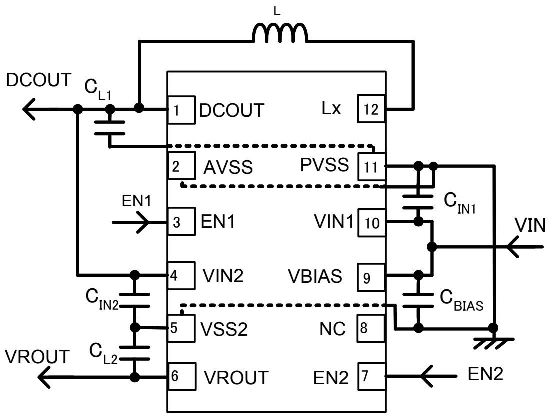
*1): Vgs is a Gate –Source voltage of the driver transistor that is defined as the value of V_{BIAS} - $V_{ROUT (T)}$.

■DROPOUT VOLTAGE CHART (Continued)

NOMINAL OUTPUT VOLTAGE (V)	E-4 DROPOUT VOLTAGE 4(mV) Vdif4														
	V_{BIAS} =3.0(V)			V_{BIAS} =3.3(V)			V_{BIAS} =3.6(V)			V_{BIAS} =4.2(V)			V_{BIAS} =5.0(V)		
	Vgs[*1] (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)		Vgs (V)	Vdif(mV)	
$V_{VROUT(T)}$		TYP	MAX		TYP	MAX		TYP	MAX		TYP	MAX		TYP	MAX
0.70	2.30	189	300	2.60	157	300	2.90	146	300	3.50	129	300	4.30	116	300
0.75	2.25	195	277	2.55	164	272	2.85	150	250	3.45	131	250	4.25	118	250
0.80	2.20			2.50			2.80			3.40		246	4.20		231
0.85	2.15	201	277	2.45	170	272	2.75	153	250	3.35	134	246	4.15	119	231
0.90	2.10			2.40			2.70			3.30			4.10		
0.95	2.05	206	277	2.35	189	272	2.65	157	250	3.25	136	246	4.05	121	231
1.00	2.00			2.30			2.60			3.20			4.00		
1.05	1.95	218	277	2.25	195	272	2.55	164	250	3.15	139	246	3.95	125	231
1.10	1.90			2.20			2.50			3.10			3.90		
1.15	1.85	231	227	2.15	201	272	2.45	170	250	3.05	142	246	3.85	128	231
1.20	1.80		334	2.10		277	2.40		248	3.00		215	3.80		189
1.25	1.75	248	376	2.05	206	296	2.35	189	255	2.95	146	219	3.75	128	191
1.30	1.70			2.00			2.30			2.90			3.70		
1.35	1.65	264	418	1.95	218	315	2.25	195	266	2.85	150	224	3.65	129	193
1.40	1.60			1.90			2.20			2.80			3.60		
1.45	1.55	281	460	1.85	231	334	2.15	201	277	2.75	153	228	3.55	129	195
1.50	1.50			1.80			2.10			2.70			3.50		
1.55	1.45	-	-	1.75	248	376	2.05	206	296	2.65	157	234	3.45	131	198
1.60	1.40			1.70			2.00			2.60			3.40		
1.65	1.35	-	-	1.65	264	418	1.95	218	315	2.55	164	241	3.35	134	202
1.70	1.30			1.60			1.90			2.50			3.30		
1.75	1.25	-	-	1.55	281	460	1.85	231	334	2.45	170	248	3.25	136	205
1.80	1.20			1.50			1.80			2.40			3.20		

*1): Vgs is a Gate –Source voltage of the driver transistor that is defined as the value of V_{BIAS} - $V_{ROUT\ (T)}$.

■TYPICAL APPLICATION CIRCUIT



● DC/DC BLOCK f_{OSC}=3.0MHz

L	:	1.5μH	(NR3015 TAIIYO YUDEN)
CIN1	:	10μF	(Ceramic)
CL1	:	10μF	(Ceramic)
CBIAS	:	1μF	(Ceramic)
CIN2	:	1μF	(Ceramic)
CL2	:	4.7μF	(Ceramic)

● DC/DC BLOCK f_{OSC}=1.2MHz

L	:	4.7μH	(NR4018 TAIIYO YUDEN)
CIN1	:	10μF	(Ceramic)
CL1	:	10μF	(Ceramic)
CBIAS	:	1μF	(Ceramic)
CIN2	:	1μF	(Ceramic)
CL2	:	4.7μF	(Ceramic)

■OPERATIONAL EXPLANATION

●DC/DC BLOCK

The DC/DC block of the XCM519 series consists of a reference voltage source, ramp wave circuit, error amplifier, PWM comparator, phase compensation circuit, output voltage adjustment resistors, P-channel MOSFET driver transistor, N-channel MOSFET switching transistor for the synchronous switch, current limiter circuit, UVLO circuit and others. (See the block diagram above.)
The series ICs compare, using the error amplifier, the voltage of the internal voltage reference source with the feedback voltage from the DCOUT pin through split resistors, R1 and R2. Phase compensation is performed on the resulting error amplifier output, to input a signal to the PWM comparator to determine the turn-on time during PWM operation. The PWM comparator compares, in terms of voltage level, the signal from the error amplifier with the ramp wave from the ramp wave circuit, and delivers the resulting output to the buffer driver circuit to cause the Lx pin to output a switching duty cycle. This process is continuously performed to ensure stable output voltage. The current feedback circuit monitors the P-channel MOS driver transistor current for each switching operation, and modulates the error amplifier output signal to provide multiple feedback signals. This enables a stable feedback loop even when a low ESR capacitor such as a ceramic capacitor is used ensuring stable output voltage.

<Reference Voltage Source>
The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Ramp Wave Circuit>
The ramp wave circuit determines switching frequency. The frequency is fixed internally and can be selected from 1.2MHz or 3.0MHz. Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation, and to synchronize all the internal circuits.

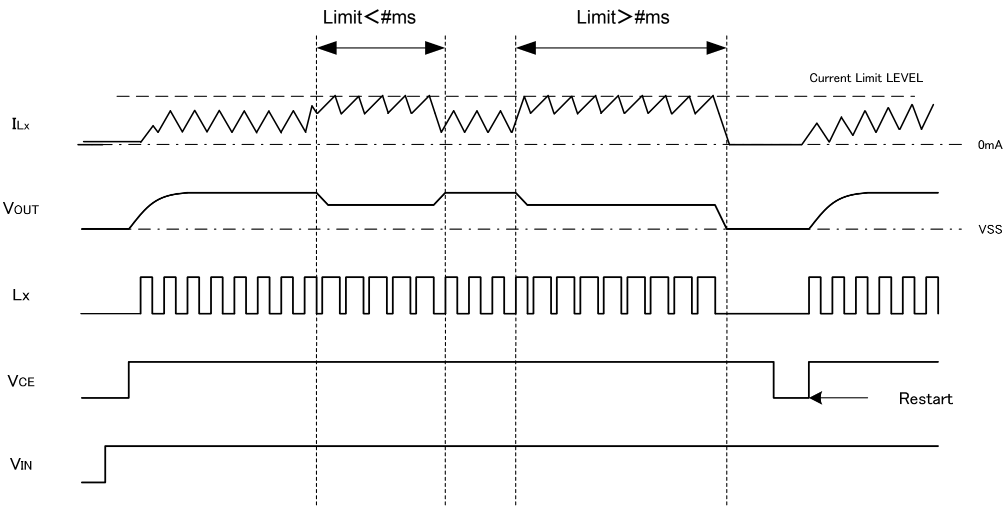
<Error Amplifier>
The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal split resistors, R1 and R2. When a voltage is lower than the reference voltage is fed back, the output voltage of the error amplifier increases. The gain and frequency characteristics of the error amplifier output are fixed internally to deliver an optimized signal to the mixer.

■OPERATIONAL EXPLANATION (Continued)

<Current Limit>
The current limiter circuit of the XCM519 series monitors the current flowing through the P-channel MOS driver transistor connected to the Lx pin, and features a combination of the current limit mode and the operation suspension mode.

① When the driver current is greater than a specific level, the current limit function operates to turn off the pulses from the Lx pin at any given timing.
② When the driver transistor is turned off, the limiter circuit is then released from the current limit detection state.
③ At the next pulse, the driver transistor is turned on. However, the transistor is immediately turned off in the case of an over current state.
④ When the over current state is eliminated, the IC resumes its normal operation.

The IC waits for the over current state to end by repeating the steps ① through ③. If an over current state continues for a few ms and the above three steps are repeatedly performed, the IC performs the function of latching the OFF state of the driver transistor, and goes into operation suspension mode. Once the IC is in suspension mode, operations can be resumed by either turning the IC off via the CE/MODE pin, or by restoring power to the V_{IN} pin. The suspension mode does not mean a complete shutdown, but a state in which pulse output is suspended; therefore, the internal circuitry remains in operation. The current limit of the XCM519 series can be set at 1050mA at typical. Besides, care must be taken when laying out the PC Board, in order to prevent miss-operation of the current limit mode. Depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, the board should be laid out so that input capacitors are placed as close to the IC as possible.



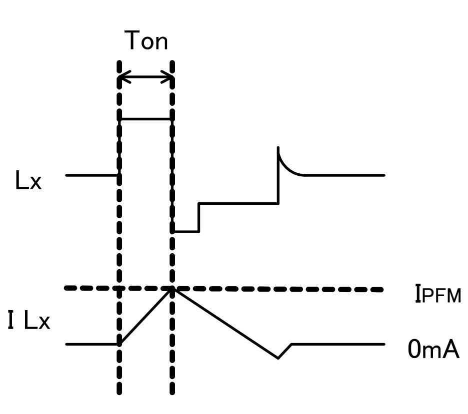
<Short-Circuit Protection>
The short-circuit protection circuit monitors the internal R1 and R2 divider voltage from the DCOUT pin. In case where output is accidentally shorted to the Ground and when the FB point voltage decreases less than half of the reference voltage (Vref) and a current more than the I_{LIM} flows to the driver transistor, the short-circuit protection quickly operates to turn off and to latch the driver transistor. In latch state, the operation can be resumed by either turning the IC off and on via the EN1 pin, or by restoring power supply to the V_{IN1} pin.
When sharp load transient happens, a voltage drop at the DCOUT pin is propagated to FB point through C_{FB}, as a result, short circuit protection may operate in the voltage higher than 1/2 V_{OUT} voltage.

<UVLO Circuit>
When the V_{IN1} pin voltage becomes 1.4V or lower, the P-channel output driver transistor is forced OFF to prevent false pulse output caused by unstable operation of the internal circuitry. When the V_{IN1} pin voltage becomes 1.8V or higher, switching operation takes place. By releasing the UVLO function, the IC performs the soft start function to initiate output startup operation. The soft start function operates even when the V_{IN} pin voltage falls momentarily below the UVLO operating voltage. The UVLO circuit does not cause a complete shutdown of the IC, but causes pulse output to be suspended; therefore, the internal circuitry remains in operation.

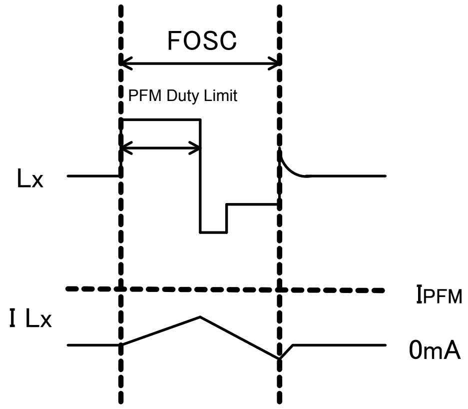
■OPERATIONAL EXPLANATION (Continued)

<PFM Switch Current>
In the PFM control operation, until coil current reaches to a specified level (D_{LIMIT_PFM}), the IC keeps the P-ch MOSFET on. In this case, on-time (t_{ON}) that the P-ch MOSFET is kept on can be given by the following formula.
$t_{ON} = L \times I_{PFM} \ (V_{IN1} - V_{DCOUT})$ →IPFM①

<PFM duty Limit>
In the PFM control operation, the PFM duty limit (D_{LIMT_PFM}) is set to 200% (TYP.). Therefore, under the condition that the duty increases (e.g. the condition that the step-down ratio is small), it's possible for P-ch MOSFET to be turned off even when coil current doesn't reach to IPFM. →IPFM②



IPFM ①



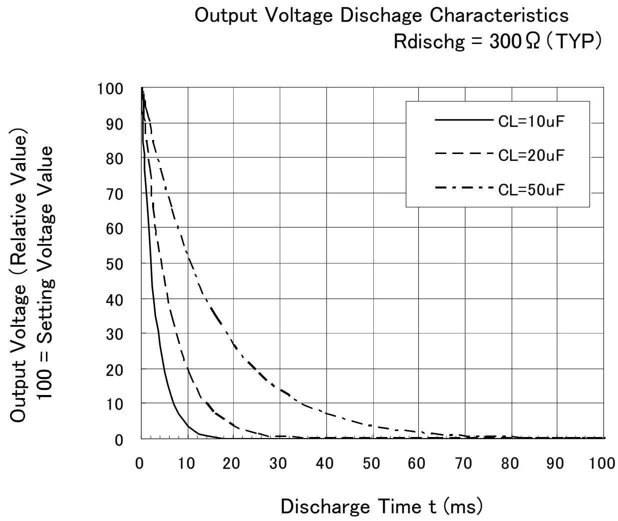
IPFM ②

＜C_L High Speed Discharge＞
XCM519xC/ XCM519xD series can quickly discharge the electric charge at the output capacitor (C_L) when a low signal to the CE pin which enables a whole IC circuit put into OFF state, is inputted via the N-channel transistor located between the L_X pin and the V_{SS} pin. When the IC is disabled, electric charge at the output capacitor (C_L) is quickly discharged so that it may avoid application malfunction. Discharge time of the output capacitor (C_L) is set by the C_L auto-discharge resistance (R) and the output capacitor (C_L). By setting time constant of a C_L auto-discharge resistance value [R] and an output capacitor value (C_L) as τ (τ =C x R), discharge time of the output voltage after discharge via the N channel transistor is calculated by the following formula.

$V = V_{DCOUT(T)} \times e^{-t/\tau}$ or $t = \tau \ Ln \ (V / V_{DCOUT(T)})$

V : Output voltage after discharge
$V_{DCOUT\ (T)}$: Output voltage
t: Discharge time
τ : C×R

C= Capacitance of Output capacitor (C_L)
R= C_L auto-discharge resistance



■OPERATIONAL EXPLANATION (Continued)

●Voltage Regulator BLOCK

The voltage divided by resistors R1 & R2 is compared with the internal reference voltage by the error amplifier. The N-channel MOSFET which is connected to the V_{ROUT} pin is then driven by the subsequent output signal. The output voltage at the V_{ROUT} pin is controlled & stabilized by a system of negative feedback.
V_{BIAS} pin is power supply pin for output voltage control circuit, protection circuit and CE circuit. When output current increase, the V_{BIAS} pin supplies output current also. V_{IN2} pin is connected to a driver transistor and provides output current.
In order to obtain high efficient output current through low on-resistance, please take enough Vgs (=V_{BIAS} – $V_{ROUT (T)}$) of the driver transistor. Output current triggers operation of constant current limiter and fold-back circuit, heat generation triggers operation of thermal shutdown circuit, the driver transistor circuit is forced OFF when V_{BIAS} or V_{IN2} voltage goes lower than UVLO voltage.
Further, the IC's internal circuitry can be shutdown via the EN2 pin's signal.

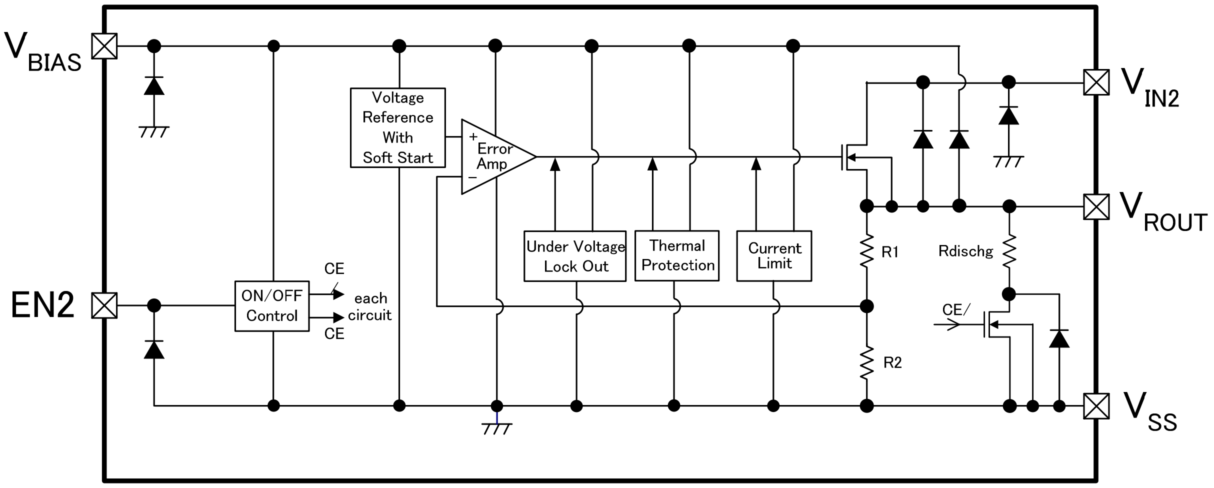


Figure 1: XC6601B Series

<Low ESR Capacitor>
With the XCM519 series, a stable output voltage is achievable even if used with low ESR capacitors, as a phase compensation circuit is built-in. The output capacitor (C_{L2}) should be connected as close to V_{ROUT} pin and V_{SS} pin to obtain stable phase compensation. Values required for the phase compensation are as the table below.
For a stable power input, please connect an bias capacitor (C_{BIAS}) of 1.0μF between the V_{BIAS} pin and the V_{SS} pin. Also, please connect an input capacitor (C_{IN2}) of 1.0μF between the V_{IN2} pin and the V_{SS} pin. In order to ensure the stable phase compensation while avoiding run-out of values, please use the capacitor (C_{BIAS}, C_{IN2}, C_{L2}) which does not depend on bias or temperature too much. The table below shows recommended values of C_{BIAS}, C_{IN}, C_L.

NOMINAL VOLTAGE	BIAS CAPACITOR	INPUT CAPACITOR	OUTPUT CAPACITOR
	C_{BIAS}	C_{IN2}	C_{L2}
0.7V～1.8V	C_{BIAS}=1.0μF	C_{IN2}=1.0μF	C_{L2}=4.7μF

Recommended Values of C_{BIAS}, C_{IN2}, C_{L2}

■OPERATIONAL EXPLANATION (Continued)

<Soft-start>

With the XCM519, the inrush current from V_{IN2} to V_{ROUT} for charging C_L at start-up can be reduced and makes the V_{IN2} stable. The soft-start time is optimized to 240 μA (TYP.) at V_{ROUT}=1.2V internally. Soft-start time is defined as the V_{ROUT} reaches 90% of $V_{ROUT (E)}$ from the time when CE H threshold 0.75V is input to the CE pin.

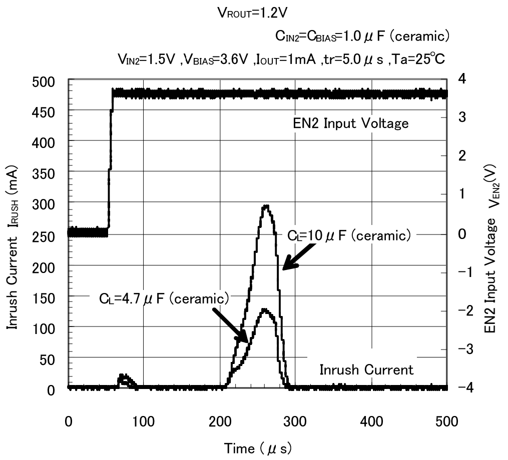


Figure2: Example of the inrush current wave form at IC start-up.

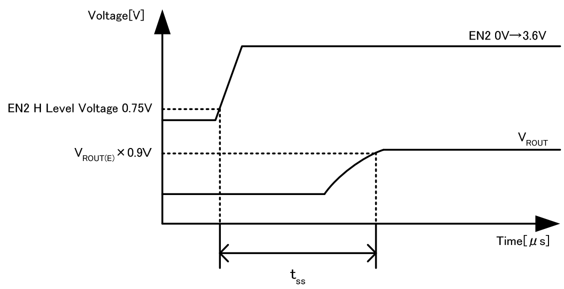


Figure3: Timing chart at IC start-up

<CL High Speed Auto-Discharge>

XCM519 series can quickly discharge the electric charge at the output capacitor (CL) when a low signal to the EN2 pin which enables a whole IC circuit put into OFF state, is inputted via the N-channel transistor located between the V_{ROUT} pin and the VSS pin. When the IC is disabled, electric charge at the output capacitor (CL) is quickly discharged so that it could avoids malfunction. At that time, CL discharge resistance is depended on a bias voltage. Discharge time of the output capacitor (CL) is set by the CL auto-discharge resistance (R) and the output capacitor (CL). By setting time constant of a CL auto-discharge resistance value [R] and an output capacitor value (CL) as τ (τ =C x R), the output voltage after discharge via the N channel transistor is calculated by the following formulas.

$V = V_{ROUT(E)} \times e^{-t/\tau}$, or $t = \tau \ln(V_{ROUT(E)} / V)$

V : Output voltage after discharge, $V_{ROUT(E)}$: Output voltage, t: Discharge time,

τ : CL auto-discharge resistance R×Output capacitor (CL) value C

<Current Limit, Short-Circuit Protection>

The XCM519 series' fold-back circuit operates as an output current limiter and a short protection of the output pin. When the load current reaches the current limit level, the fixed current limiter circuit operates and output voltage drops. When the output pin is shorted to the V_{SS} level, current flows about 50mA.

<Thermal Shutdown Circuit (TSD) >

When the junction temperature of the built-in driver transistor reaches the temperature limit level (150℃ TYP.), the thermal shutdown circuit operates and the driver transistor will be set to OFF. The IC resumes its operation when the thermal shutdown function is released and the IC's operation is automatically restored because the junction temperature drops to the level of the thermal shutdown release temperature (135℃ TYP.).

<Under Voltage Lock Out (UVLO) >

When the V_{BIAS} pin voltage drops below 2.0V (TYP.) or V_{IN2} pin voltage drops below 0.4V (TYP.), the output driver transistor is forced OFF by UVLO function to prevent false output caused by unstable operation of the internal circuitry. When the V_{BIAS} pin voltage rise at 2.2V (TYP.) or the V_{IN2} pin voltage rises at 0.4V (TYP.), the UVLO function is released. The driver transistor is turned in the ON state and start to operate voltage regulation.

■OPERATIONAL EXPLANATION (Continued)

<EN2 Pin>

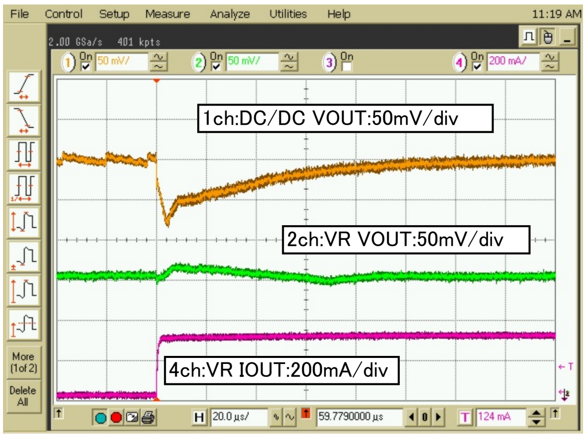
The IC internal circuitry can be shutdown via the signal from the EN2 pin with the XCM519 series. In shutdown mode, output at the V_{ROUT} pin will be pulled down to the V_{SS} level via R1 & R2. However, as for the XCM519 series, the CL auto-discharge resistor is connected in parallel to R1 and R2 while the power supply is applied to the V_{IN2} pin. Therefore, time until the VROUT pin reaches the V_{SS} level becomes short.

The EN2 pin of XCM519 has pull-down circuitry so that EN2 input current increase during IC operation. The EN2 pin of XCM519 does not have pull-down circuitry so that logic is not fixed when the CE pin is open. If the EN2 pin voltage is taken from V_{BIAS} pin or V_{SS} pin then logic is fixed and the IC will operate normally. However, supply current may increase as a result of through current in the IC's internal circuitry when medium voltage is input.

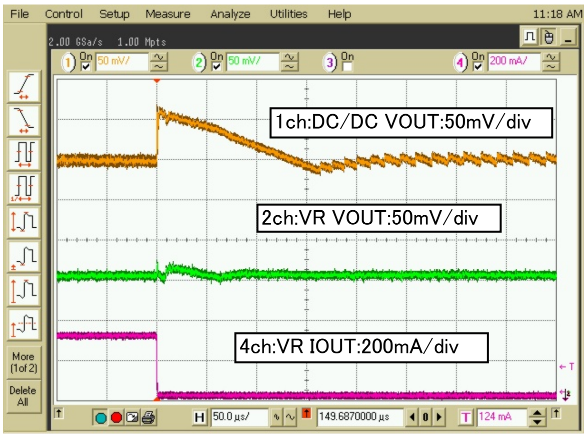
■NOTE ON USE

When the DC/DC converter and the VR are connected as V_{IN1}=V_{BIAS}, V_{DCOUT}=V_{IN2}, the following points should be noted.

1. When the DC/DC load is changed drastically during a light load of the VR, a fluctuation may happen in tenths of mV. This value can be reduced by increasing C_{L1} load capacitance at the DC/DC in order to reduce a voltage drop during load transient.

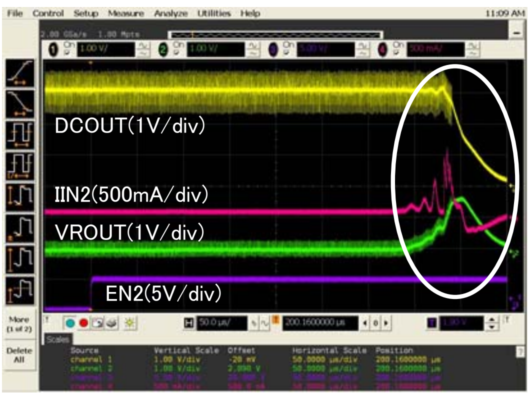


20 μ s/div



50 μ s/div

2. It is recommended that both C_{IN1} and C_{BIAS} are connected to each pin separately. When one capacitor is used instead of the two, this capacitor should be placed in 10 μ F or more as close as the VIN1 and the PGND (AGND) pins of the DC/DC circuit. Please ensure it by testing on the actual product design.
3. It is recommended that both C_{L1} and C_{IN2} are connected to each pin separately. When one capacitor is used instead of the two, this capacitor should be selected in 4.7 μ F or bigger. Please ensure it by testing on the actual product design.
4. C_{L2} of the VR is recommended 4.7 μ A. When larger value is used in C_{L2}, the larger value is also used in C_{L1} as in proportional. Please be noted that when C_{L2} capacitance of the VR is getting large, an inrush current increases at VR start-up, DC/DC short circuit protection starts to operate, as a result, the IC may happen to stop.



50us/div

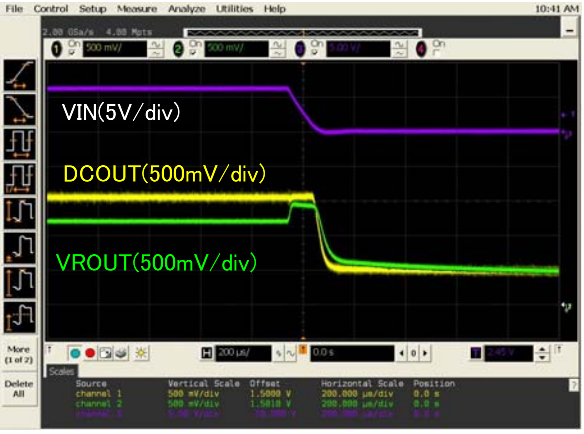
* VR inrush current I_{IN2} makes DC/DC short-circuit protection to start, as a result, the IC may happen to stop.

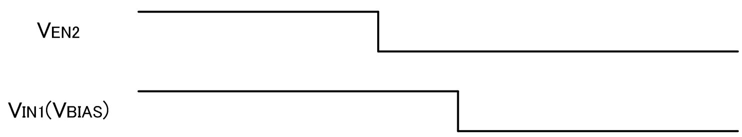
The left waver forms are taken at C_{L1}=10 μ , C_{L2}=10 μ F(in contrast to the recommended 4.7 μ F).

However, it improves when C_{L1}=20 μ F.

■NOTE ON USE (Continued)

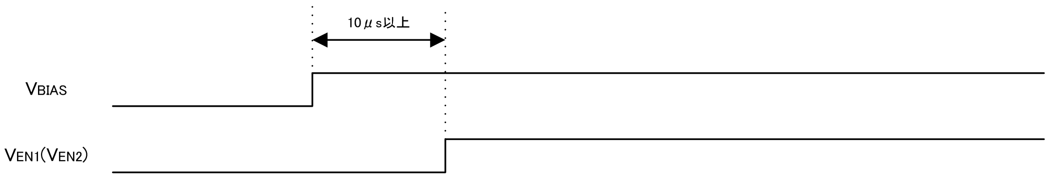
5. When the input-output voltage differential is small in the DC/DC converter and heavy load condition, a duty cycle is getting large and keeps the 100% duty cycle in a several period cycles. At the time of duty cycle transition to 100% or from 100%, noise may appear on the voltage regulator output. Please evaluate this on the actual design board when the condition is in small input-output voltage differential and heavy load.
6. When the load is changed at the DC/DC converter, ringing may happen in some load conditions of DC/DC and VR at the timing of turn on and turn off. The ringing can be reduced by increasing C_{IN1} capacitance or placing a resistor over 10kΩ between V_{IN1} and V_{BIAS} pins.
7. In order to turn off the input voltage, the EN2 pin should be turned off first. If the input voltage is turned off with keeping VR operation, the VROUT voltage goes up instantaneously as a result of the VR bias voltage transient.





200us/div

8. When the DCOUT pin is connected to the V_{IN2} pin and the bias voltage (V_{BIAS}) is taken from the other power supply, EN1 and EN2 should be started up 10μs later than V_{BIAS}. If EN1 and EN2 is turned on within 10μs, inrush current like 1A may happen which result in starting the DC/DC short-circuit protection.



9. It is recommended to test this in the actual product design board.

<DC/DC BLOCK>

1. The XCM519 series is designed for use with ceramic output capacitors. If, however, the potential difference is too large between the input voltage and the output voltage, a ceramic capacitor may fail to absorb the resulting high switching energy and oscillation could occur on the output. If the input-output potential difference is large, connect an electrolytic capacitor in parallel to compensate for insufficient capacitance.
2. Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.
3. As a result of input-output voltage and load conditions, oscillation frequency goes to 1/2, 1/3, and continues, then a ripple may increase.
4. When input-output voltage differential is large and light load conditions, a small duty cycle comes out. After that, 0%duty cycle may continue in several periods.
5. When input-output voltage differential is small and heavy load conditions, a large duty cycle comes out and may continues100% duty cycle in several periods.
6. With the IC, the peak current of the coil is controlled by the current limit circuit. Since the peak current increases when dropout voltage or load current is high, current limit starts operation, and this can lead to instability. When peak current becomes high, please adjust the coil inductance value and fully check the circuit operation. In addition, please calculate the peak current according to the following formula:

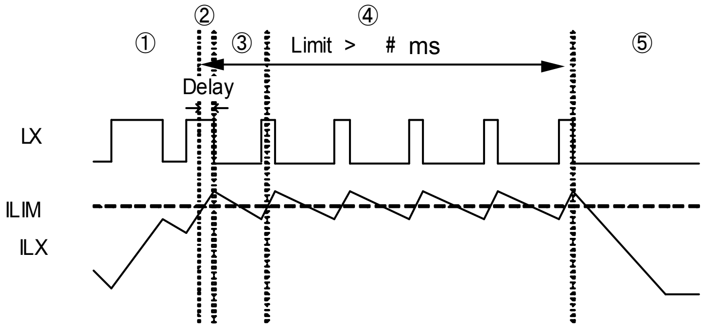
   $I_{pk} = (V_{IN1}-V_{DCOUT})\times OnDuty /(2\times L\times f_{OSC}) + I_{OUT}$

   L: Coil Inductance Value

   f_{OSC}: Oscillation Frequency

■NOTE ON USE (Continued)

7. When the peak current which exceeds limit current flows within the specified time, the built-in P-ch driver transistor turns off. During the time until it detects limit current and before the built-in transistor can be turned off, the current for limit current flows; therefore, care must be taken when selecting the rating for the external components such as a coil.
8. Care must be taken when laying out the PC Board, in order to prevent misoperation of the current limit mode. Depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, the board should be laid out so that input capacitors are placed as close to the IC as possible.
9. Use of the IC at voltages below the recommended voltage range may lead to instability.
10. This IC should be used within the stated absolute maximum ratings in order to prevent damage to the device.
11. When the IC is used in high temperature, output voltage may increase up to input voltage level at no load because of the leak current of the driver transistor.
12. The current limit is set to 1350mA (MAX.) at typical. However, the current of 1350mA or more may flow. In case that the current limit functions while the DCOUT pin is shorted to the GND pin, when P-ch MOSFET is ON, the potential difference for input voltage will occur at both ends of a coil. For this, the time rate of coil current becomes large. By contrast, when N-ch MOSFET is ON, there is almost no potential difference at both ends of the coil since the DCOUT pin is shorted to the GND pin. Consequently, the time rate of coil current becomes quite small. According to the repetition of this operation, and the delay time of the circuit, coil current will be converged on a certain current value, exceeding the amount of current, which is supposed to be limited originally. Even in this case, however, after the over current state continues for several ms, the circuit will be latched. A coil should be used within the stated absolute maximum rating in order to prevent damage to the device.
   ①Current flows into P-ch MOSFET to reach the current limit (I_{LIM}).
   ②The current of I_{LIM} or more flows since the delay time of the circuit occurs during from the detection of the current limit to OFF of P-ch MOSFET.
   ③Because of no potential difference at both ends of the coil, the time rate of coil current becomes quite small.
   ④Lx oscillates very narrow pulses by the current limit for several ms.
   ⑤The circuit is latched, stopping its operation.

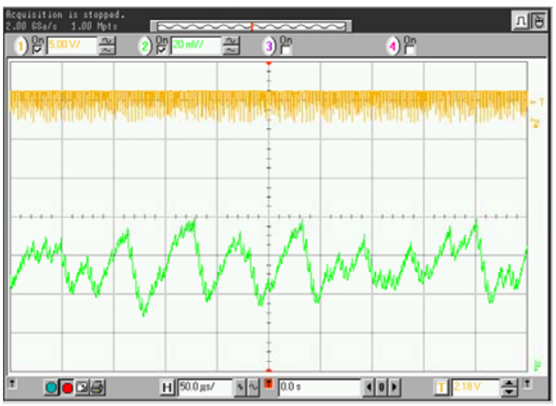


13. In order to stabilize V_{IN1}'s voltage level and oscillation frequency, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{IN1} & V_{SS} pins.
14. High step-down ratio and very light load may lead an intermittent oscillation.
15. During PWM / PFM automatic switching mode, operating may become unstable at transition to continuous mode. Please verify with actual parts.

VOUT=3.3V,FOSC=1.2MHz
VIN=3.7V,IOUT=100mA

CH1:Lx 5/div

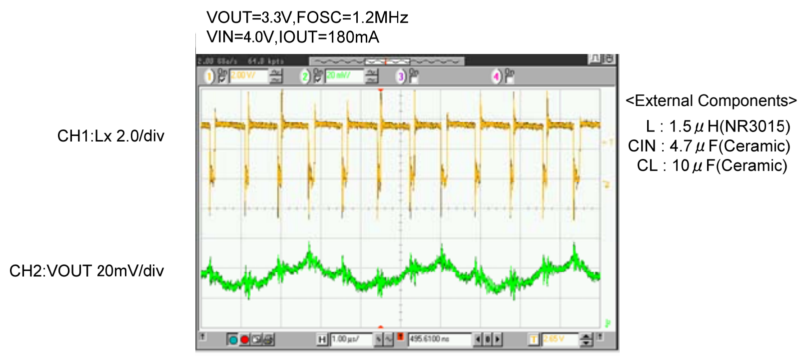
CH2:VOUT 20mV/div



<External Components>
L : 4.7μH(NR4018)
CIN : 4.7μF(Ceramic)
CL : 10μF(Ceramic)

■NOTE ON USE (Continued)

16. Please note the inductance value of the coil. The IC may enter unstable operation if the combination of ambient temperature, setting voltage, oscillation frequency, and L value are not adequate.
In the operation range close to the maximum duty cycle, The IC may happen to enter unstable output voltage operation even if using the L values listed below.



●The Range of L Value

f_{OSC}	V_{OUT}	L Value
3.0MHz	0.8V＜V_{OUT}<4.0V	1.0μH～2.2μH
1.2MHz	V_{OUT}≦2.5V	3.3μH～6.8μH
	2.5V＜V_{OUT}	4.7μH～6.8μH

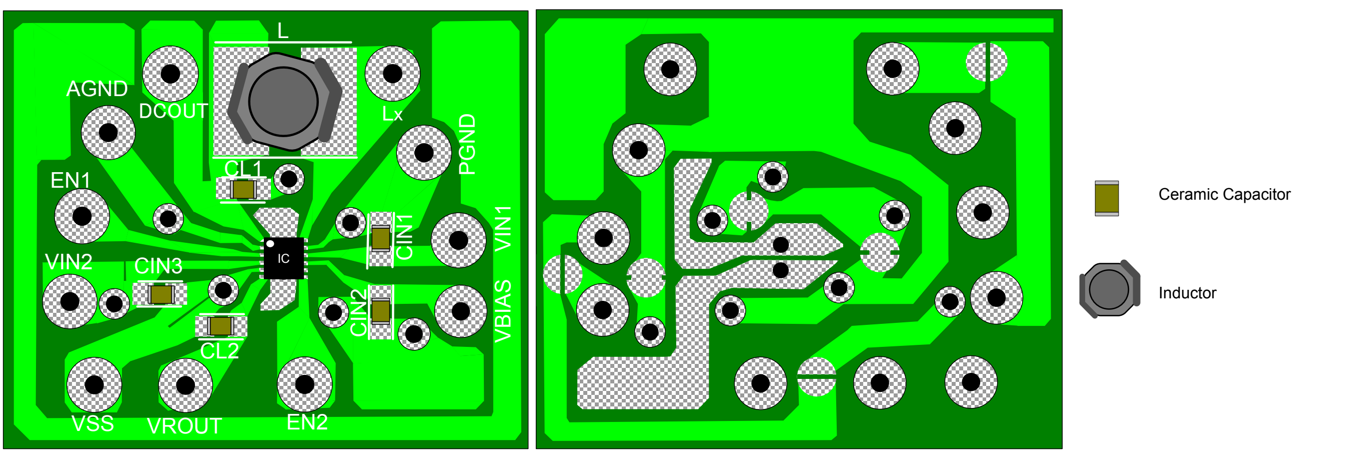
*When a coil less value of 4.7μH is used at f_{OSC}=1.2MHz or when a coil less value of 1.5μH is used at f_{OSC}=3.0MHz, peak coil current more easily reach the current limit ILMI. In this case, it may happen that the IC can not provide 600mA output current.

<Regulator BLOCK>

1. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please keep the resistance low between V_{BIAS}, V_{IN2} and V_{SS} wiring in particular.
2. Please wire the bias capacitor (C_{BIAS}), input capacitor (C_{IN2}) and the output capacitor (C_{L2}) as close to the IC as possible.
3. Capacitance values of these capacitors (C_{BIAS}, C_{IN2}, C_{L2}) are decreased by the influences of bias voltage and ambient temperature. Care shall be taken for capacitor selection to ensure stability of phase compensation from the point of ESR influence.
4. In case of the output capacitor more than C_L=22μF is used, ringing of input current occurs when rising time.
5. V_{IN2} and EN2 should be applied at least 10μs after the bias voltage V_{BIAS} reaches the requested voltage.
If V_{IN2} and EN2 are applied within 10μs, inrush current like 1A may occurs.

●Instructions of pattern layouts

1. Please use this IC within the stated absolute maximum ratings. The IC is liable to malfunction should the ratings be exceeded.
2. In order to stabilize V_{IN1} • V_{IN2} • V_{BIAS} • DCOUT・V_{ROUT} voltage level, we recommend that a by-pass capacitor (C_{IN1} • C_{IN2}・C_{BIAS} • C_{L1} • C_{L2}) be connected as close as possible to the V_{IN1} • V_{IN2} • V_{BIAS} • DCOUT・V_{ROUT} and GND・V_{SS} pins.
3. Please mount each external component as close to the IC as possible.
4. Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
5. V_{SS}（AGND • PGND • V_{SS}）ground wiring is recommended to get large area. The IC may goes into unstable operation as a result of VSS voltage level fluctuation during the switching.
6. This series' internal driver transistors bring on heat because of the output current (I_{OUT}) and ON resistance of driver transistors.



Front　　　　　　Back

■TEST CIRCUITS

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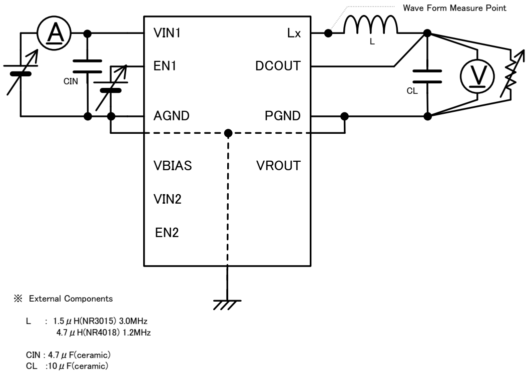

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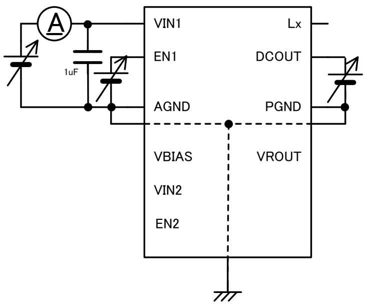

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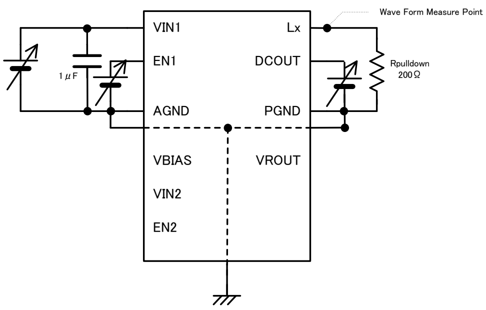

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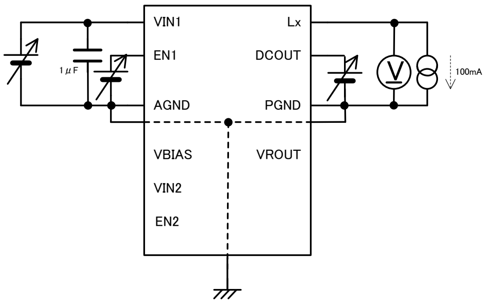

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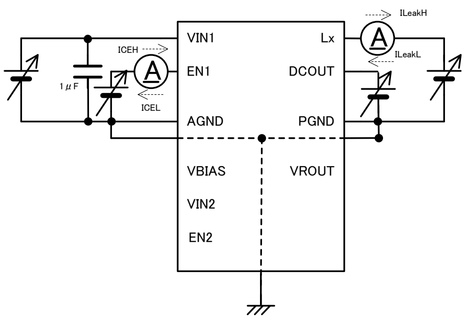

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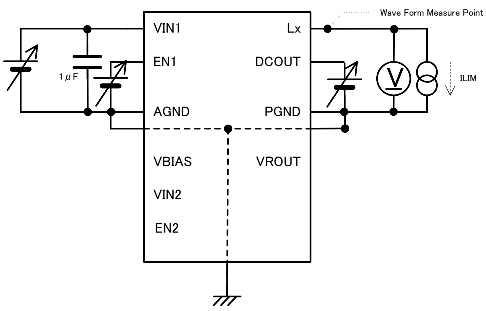

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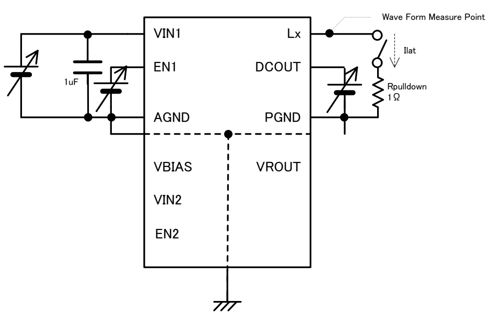

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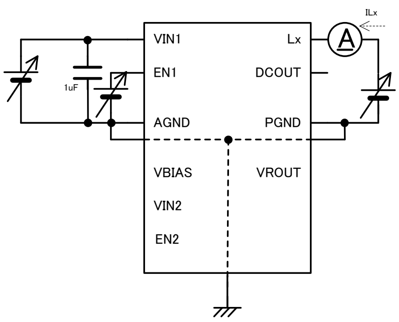

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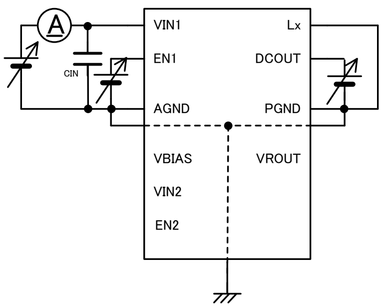

■TEST CIRCUITS (Continued)

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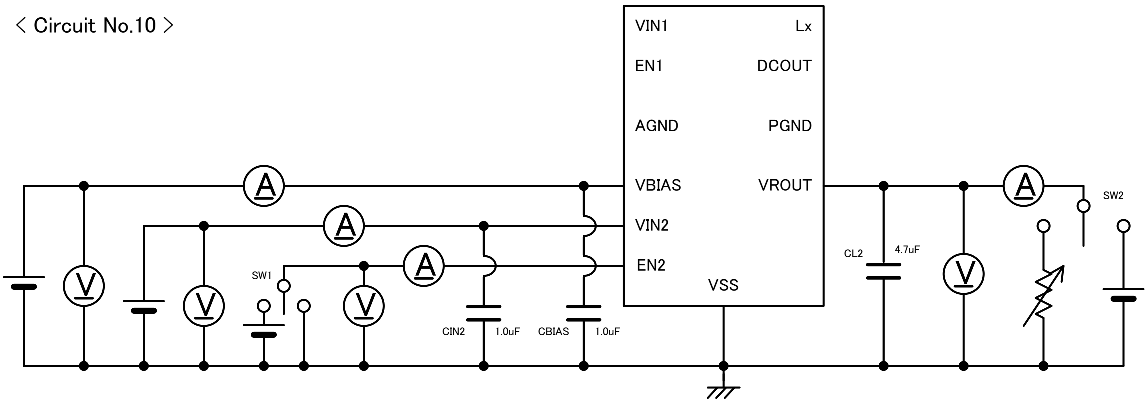

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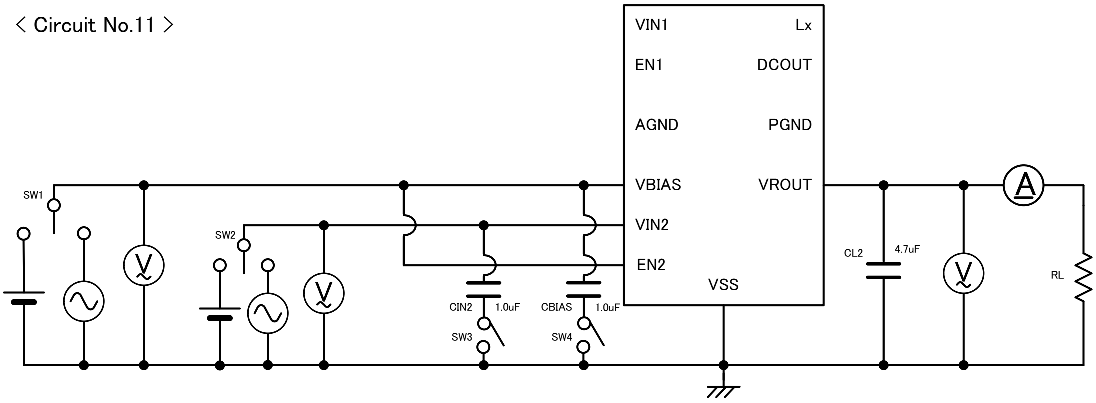

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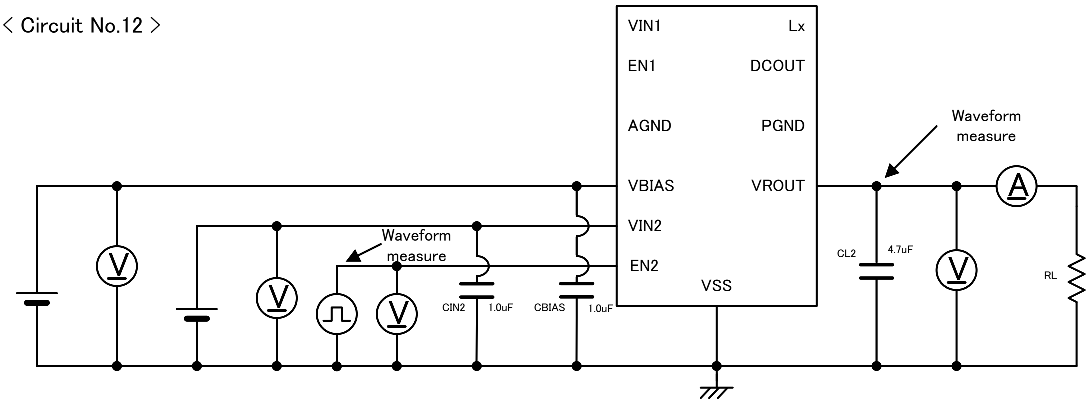


* For the timing chart, please refer to <Soft-start> on page 20.

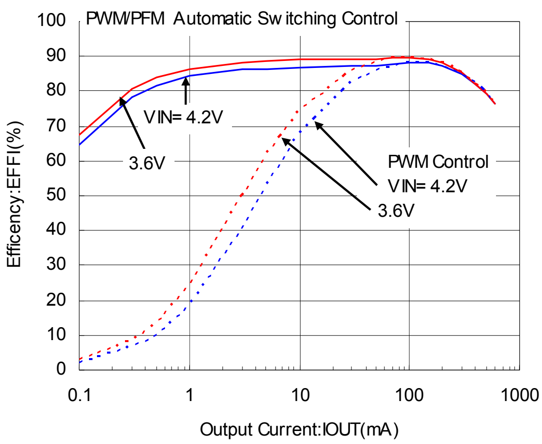
■TYPICAL PERFORMANCE CHARACTERISTICS

●1ch:DC/DC Block

(1) Efficiency vs. Output Current

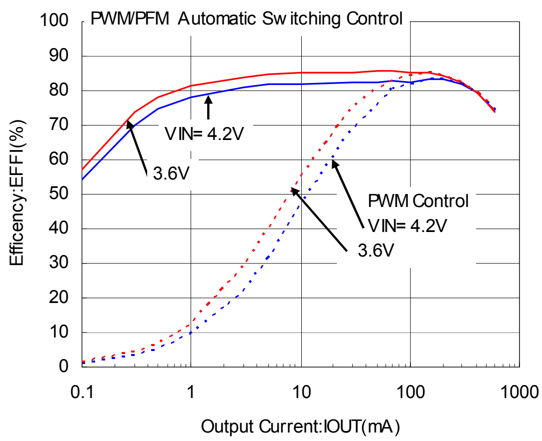
DCOUT=1.8V,1.2MHz

L=4.7μH(NR4018), C_{IN1}=10μF, C_{L1}=10μF



DCOUT=1.8V,3.0MHz

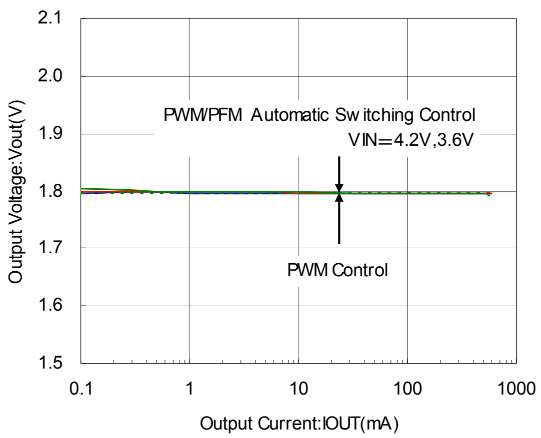
L=1.5μH(NR3015), C_{IN1}=10μF, C_{L1}=10μF



(2) Output Voltage vs. Output Current

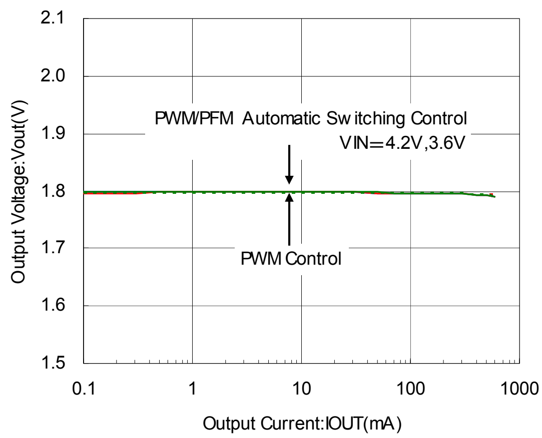
DCOUT=1.8V,1.2MHz

L=4.7μH(NR4018), C_{IN1}=10μF, C_{L1}=10μF



DCOUT=1.8V,3.0MHz

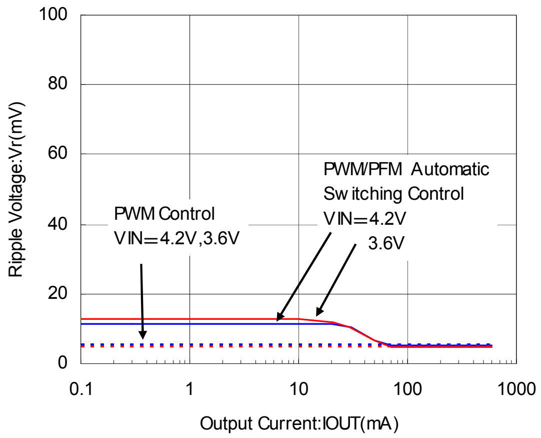
L=1.5μH(NR3015), C_{IN1}=10μF, C_{L1}=10μF



(3) Ripple Voltage vs. Output Current

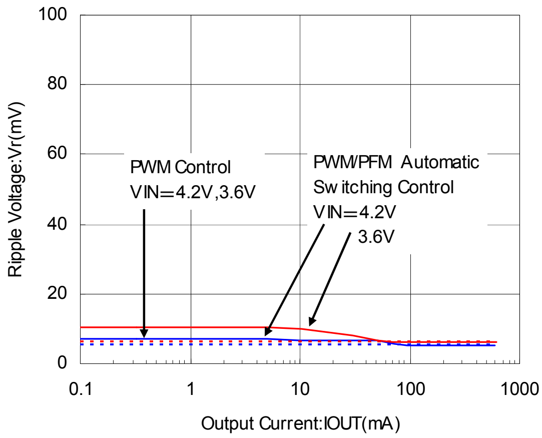
DCOUT=1.8V,1.2MHz

L=4.7μH(NR4018), C_{IN1}=10μF, C_{L1}=10μF



DCOUT=1.8V,3.0MHz

L=1.5μH(NR3015), C_{IN1}=10μF, C_{L1}=10μF

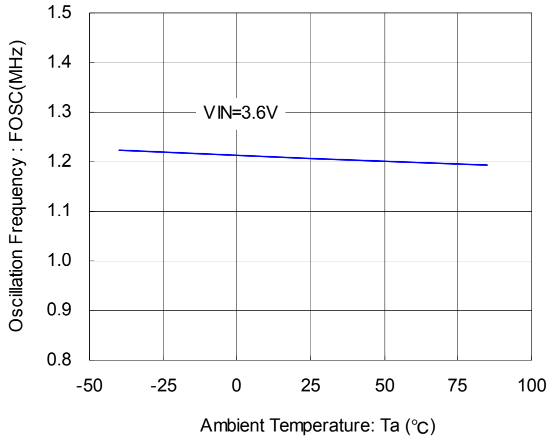


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(4) Oscillation Frequency vs. Ambient Temperature

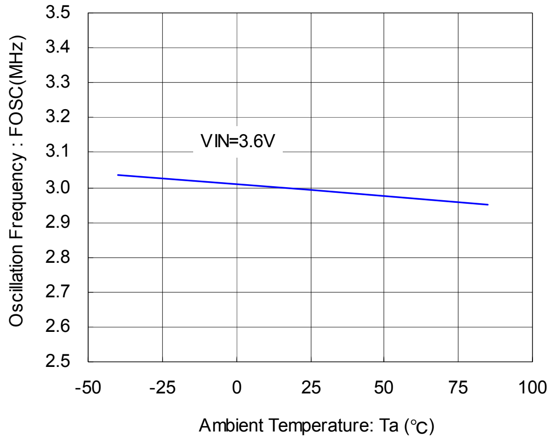
DCOUT=1.8V,1.2MHz

L=4.7μH(NR4018), C_{IN1}=10μF, C_{L1}=10μF



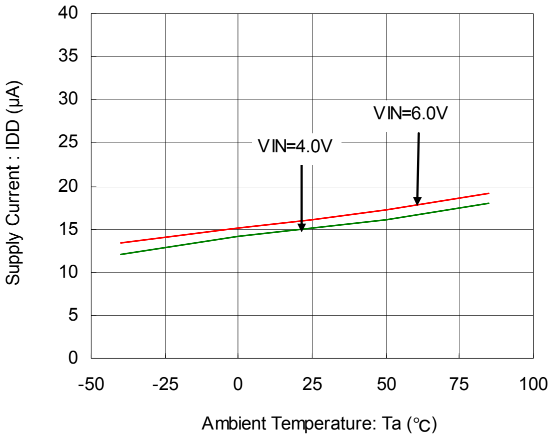
DCOUT=1.8V,3.0MHz

L=1.5μH(NR3015), C_{IN1}=10μF, C_{L1}=10μF

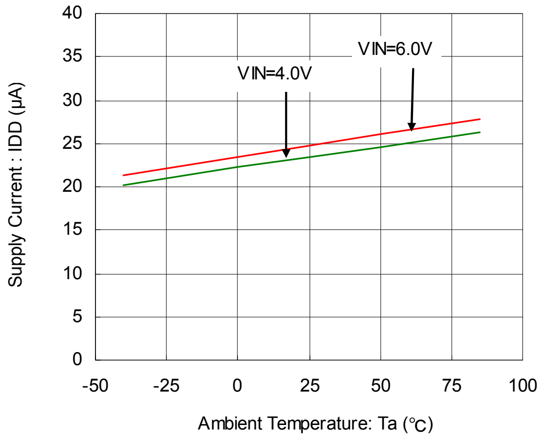


(5) Supply Current vs. Ambient Temperature

DCOUT=1.8V,1.2MHz

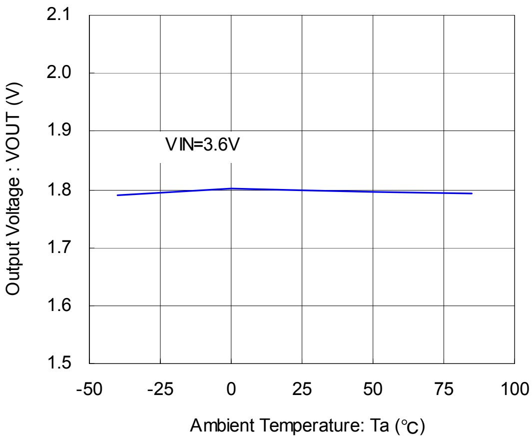


DCOUT=1.8V,3.0MHz



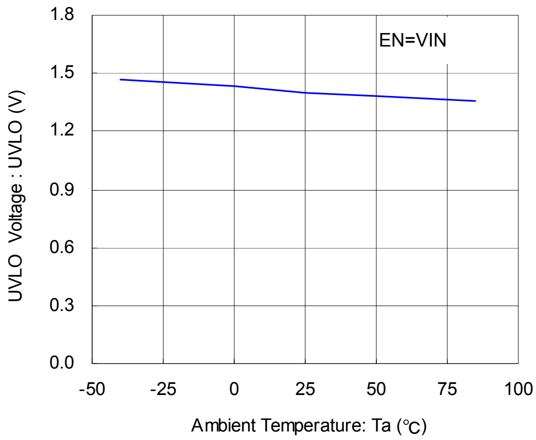
(6) Output Voltage vs. Ambient Temperature

DCOUT=1.8V,3.0MHz



(7) UVLO Voltage vs. Ambient Temperature

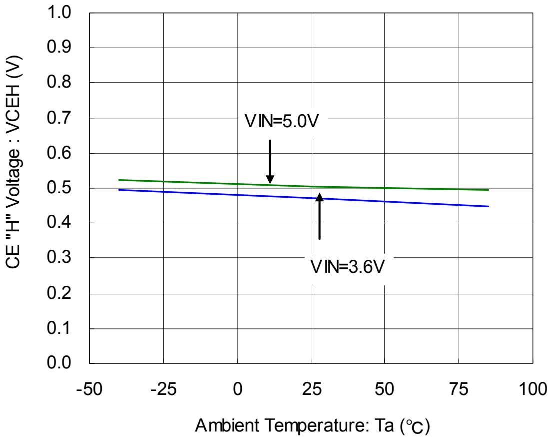
DCOUT=1.8V,3.0MHz



■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

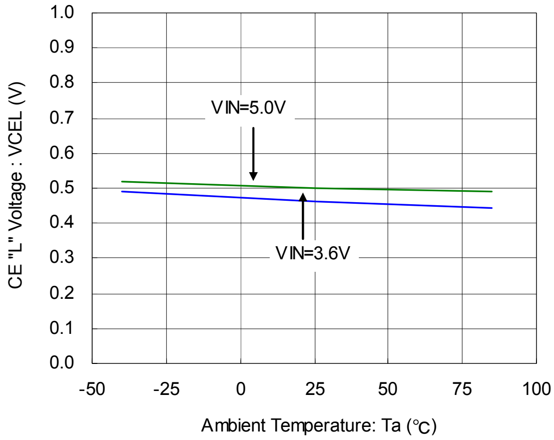
(8) EN "H" Voltage vs. Ambient Temperature

DCOUT=1.8V,3.0MHz



(9)EN" L" Voltage vs. Ambient Temperature

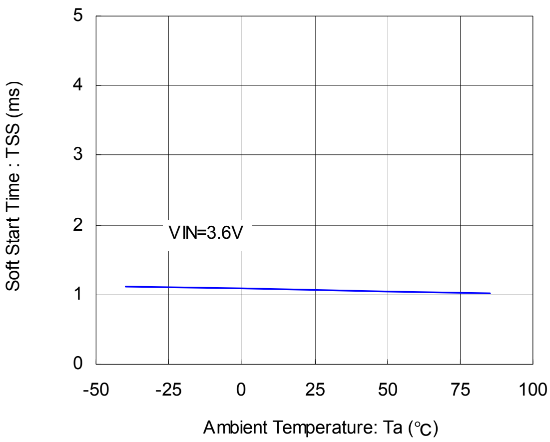
DCOUT=1.8V,3.0MHz



(10) Soft Start Time vs. Ambient Temperature

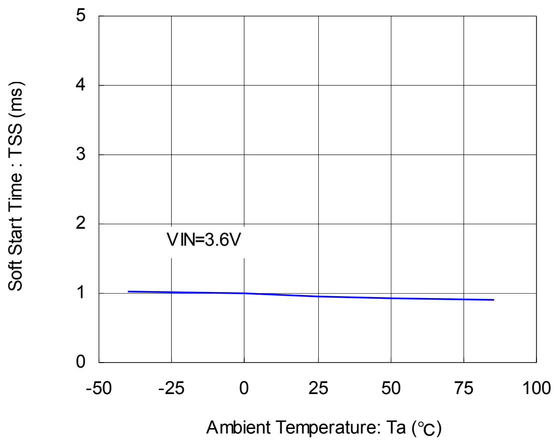
DCOUT=1.8V,3.0MHz

L=4.7µH(NR4018), CIN1=10µF, CL1=10µF



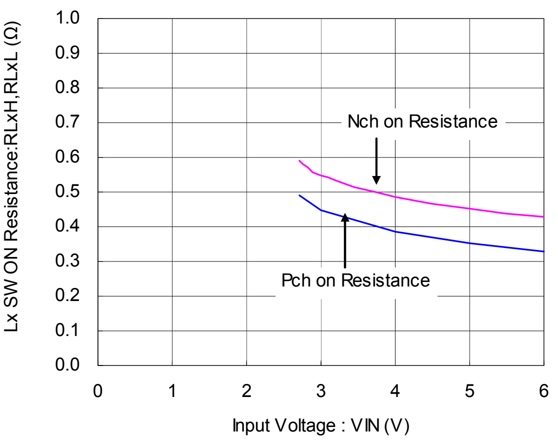
DCOUT=1.8V,3.0MHz

L=1.5µH(NR3015), CIN1=10µF, CL1=10µF



(11) "Pch / Nch" Driver on Resistance vs. Input Voltage

DCOUT=1.8V,3.0MHz

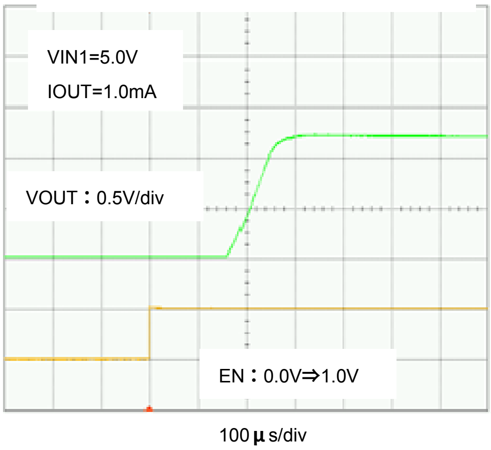


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(12) XCM519xC/ XCM519xD Rise Wave Form

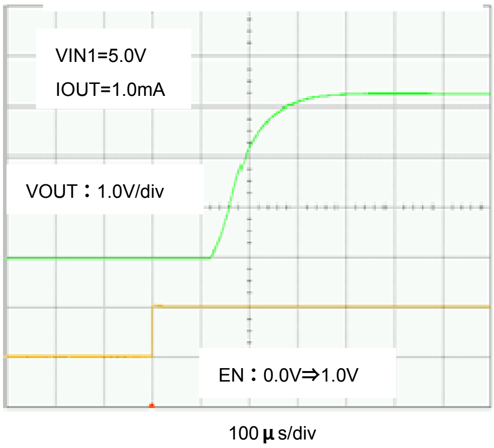
DCOUT=1.2V,1.2MHz

L=4.7μH (NR4018), CIN1=10μF, CL1=10μF



DCOUT=3.3V,3.0MHz

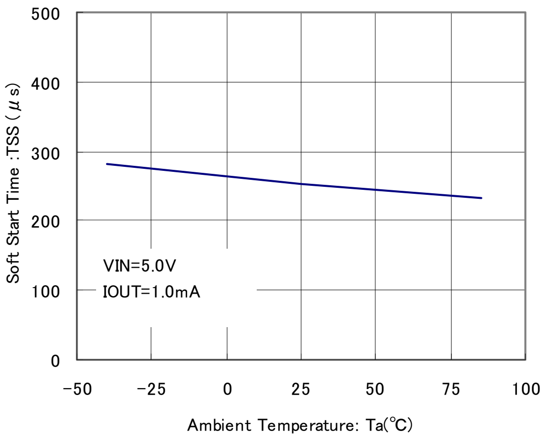
L=1.5μH (NR3015), CIN1=10μF, CL1=10μF



(13) XCM519xC/ XCM519xD Soft-Start Time vs. Ambient Temperature

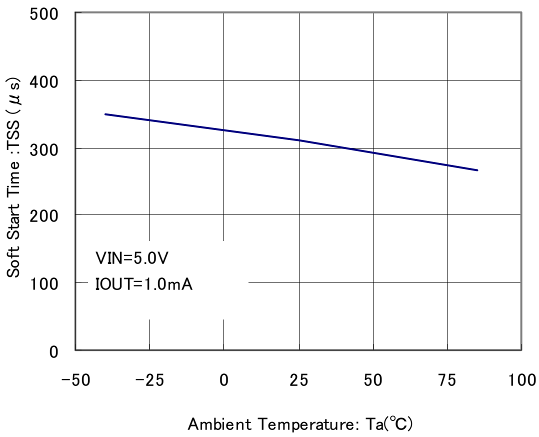
DCOUT=1.2V,1.2MHz

L=4.7μH(NR4018), CIN1=10μF, CL1=10μF



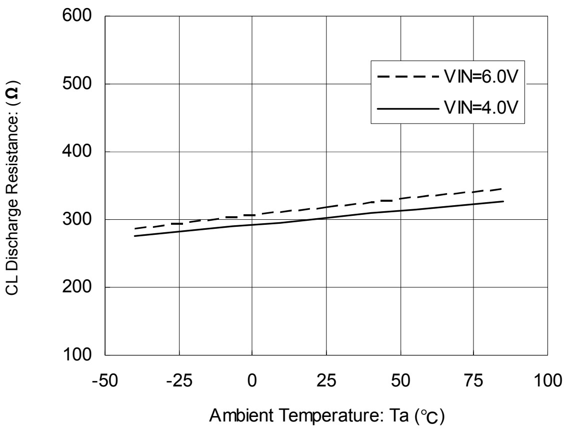
DCOUT=3.3V,3.0MHz

L=1.5μH(NR3015), CIN1=10μF, CL1=10μF



(14) XCM519xC/ XCM519xD CL Discharge Resistance vs. Ambient Temperature

DCOUT=3.3V,3.0MHz



■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(15) Load Transient Response

DCOUT=1.2V,1.2MHz(PWM/PFM Automatic Switching Control)

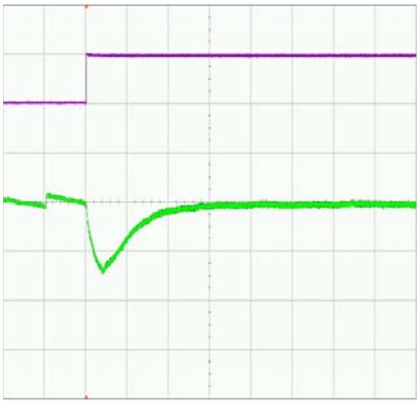
L=4.7μH(NR4018), C_{IN1}=10μF(ceramic), C_{L1}=10μF(ceramic), Topr=25℃

V_{IN1}=3.6V, EN1=V_{IN1}

I_{OUT}=1mA → 100mA

1ch : I_{OUT}

2ch
V_{OUT} : 50mV/div

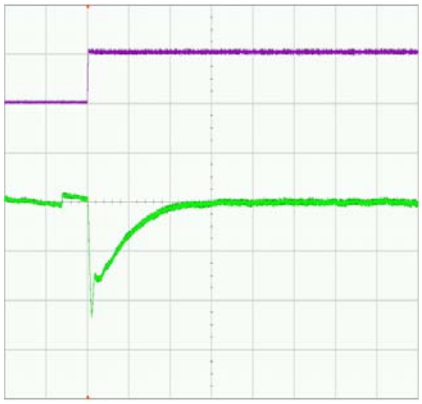


50μs/div

I_{OUT} =1mA → 300mA

1ch : I_{OUT}

2ch
V_{OUT} : 50mV/div

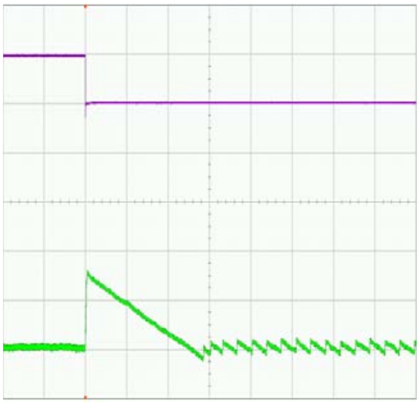


50μs/div

I_{OUT}=100mA → 1mA

1ch : I_{OUT}

2ch
V_{OUT}: 50mV/div

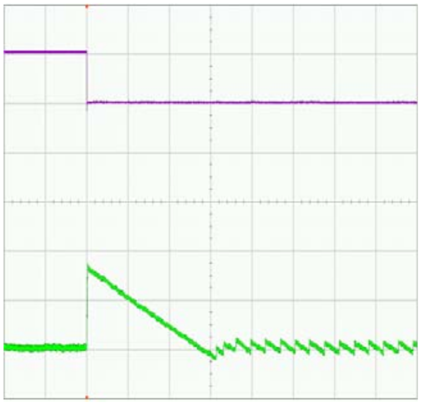


200μs/div

I_{OUT}=300mA → 1mA

1ch : I_{OUT}

2ch
V_{OUT}: 50mV/div



200μs/div

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

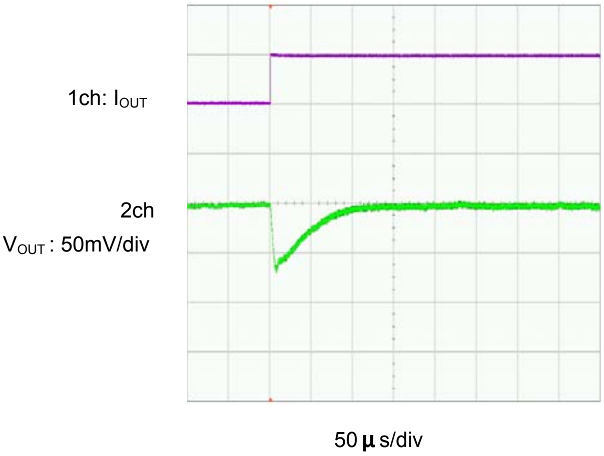
(15) Load Transient Response (Continued)

DCOUT=1.2V,1.2MHz(PWM Control)

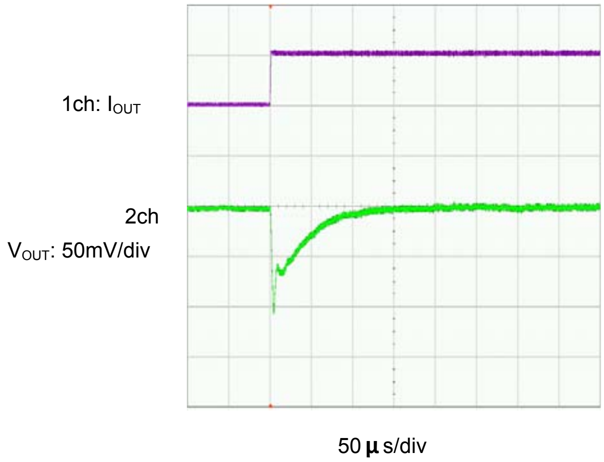
L=4.7μH(NR4018), C_{IN1}=10μF(ceramic), C_{L1}=10μF(ceramic), Topr=25℃

V_{IN1}=3.6V, EN1=V_{IN1}

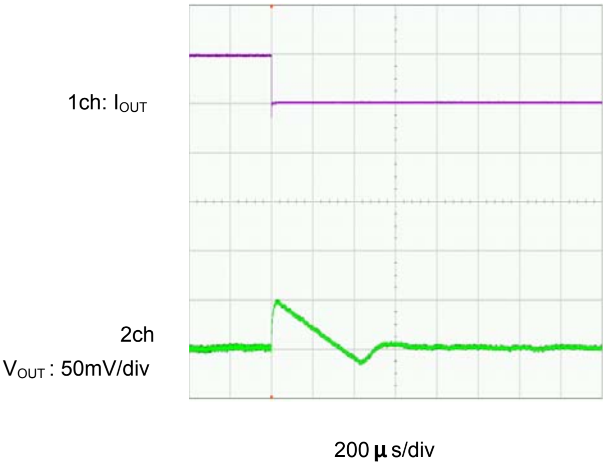
I_{OUT}=1mA → 100mA



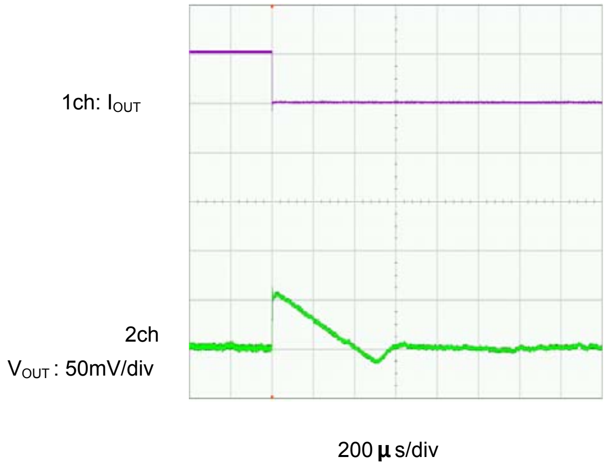
I_{OUT}=1mA → 300mA



I_{OUT}=100mA → 1mA



I_{OUT}=300mA → 1mA



■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(15) Load Transient Response (Continued)

$DCOUT_T$=1.8V,3.0MHz(PWM/PFM Automatic Switching Control)

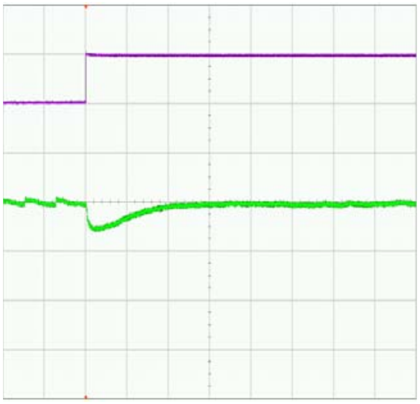
L=1.5μH(NR3015), C_{IN1}=10μF(ceramic), C_{L1}=10μF(ceramic),Topr=25℃

V_{IN1}=3.6V, EN=V_{IN1}

I_{OUT}=1mA → 100mA

1ch : I_{OUT}

2ch
V_{OUT} : 50mV/div

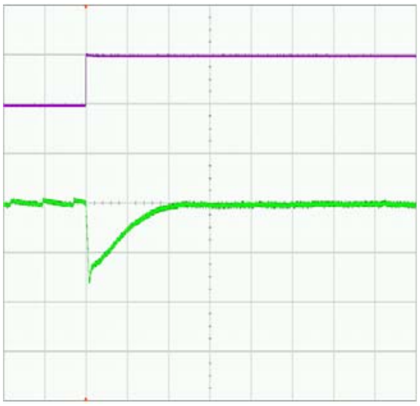


50μs/div

I_{OUT}=1mA → 300mA

1ch : I_{OUT}

2ch
V_{OUT} : 50mV/div

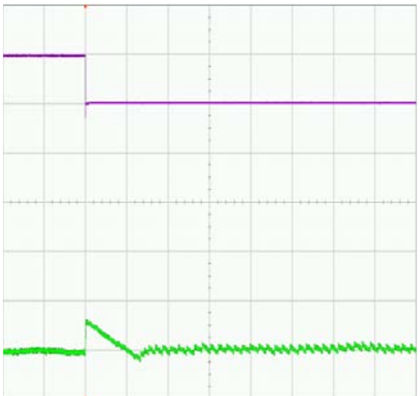


50μs/div

IOUT=100mA → 1mA

1ch : I_{OUT}

2ch
V_{OUT} : 50mV/div

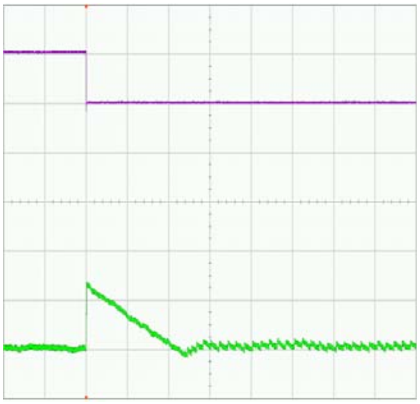


200μs/div

IOUT=300mA → 1mA

1ch : I_{OUT}

2ch
V_{OUT} : 50mV/div



200μs/div

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

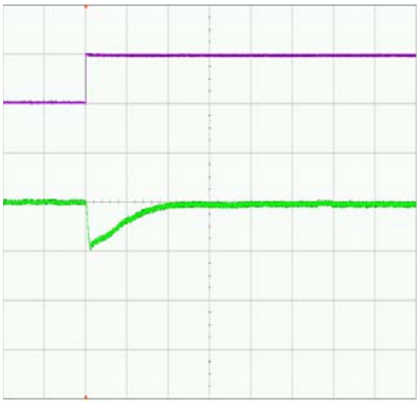
(15) Load Transient Response (Continued)

DCOUT=1.8V,3.0MHz(PWM Control)

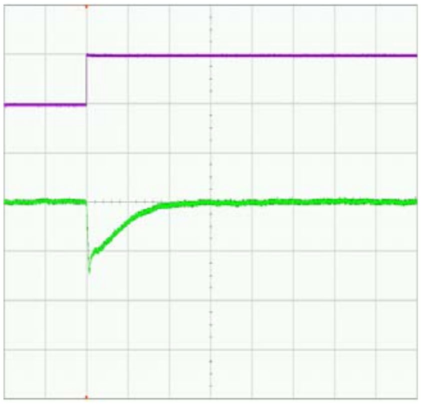
L=1.5μH(NR3015), C_{IN1}=10μF(ceramic), C_{L1}=10μF(ceramic), Topr=25℃

V_{IN1}=3.6V, EN1=V_{IN1}

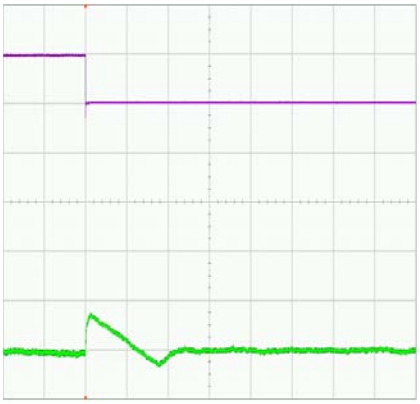
I_{OUT}=1mA → 100mA



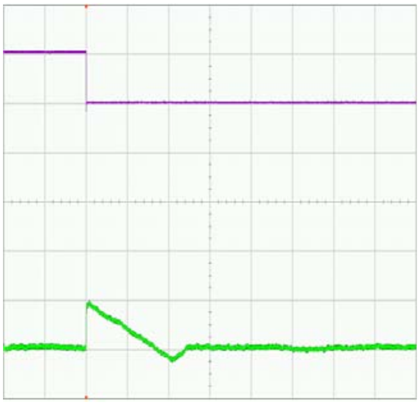
I_{OUT}=1mA → 300mA



I_{OUT}=100mA → 1mA



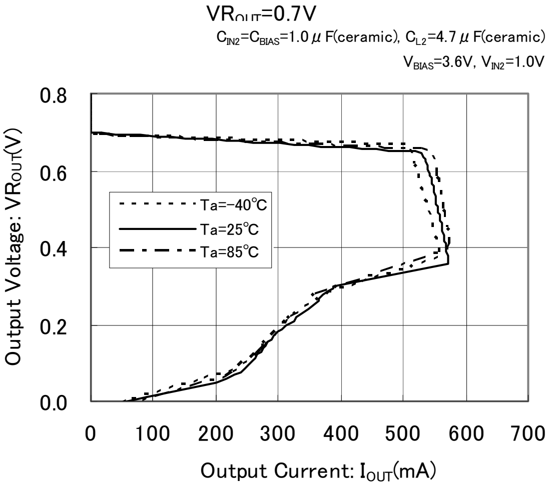
I_{OUT}=300mA → 1mA

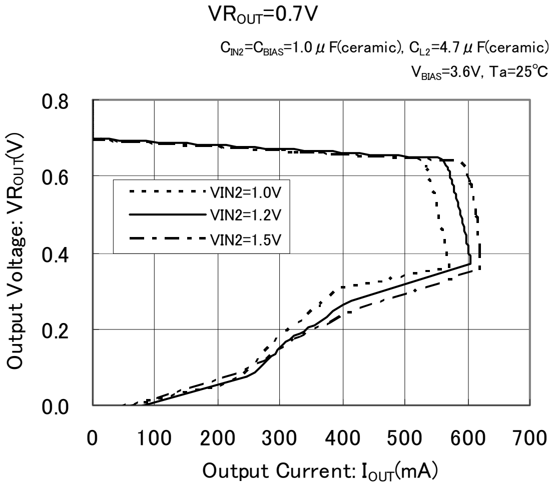


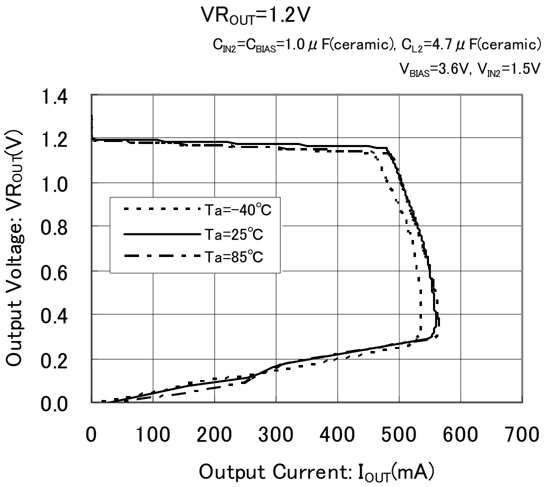
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

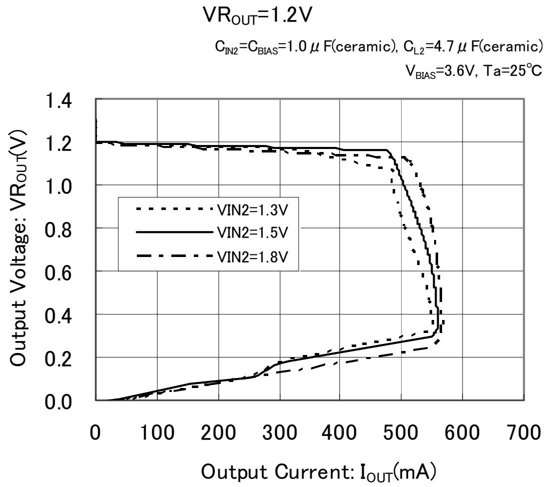
●2ch:Regulator Block

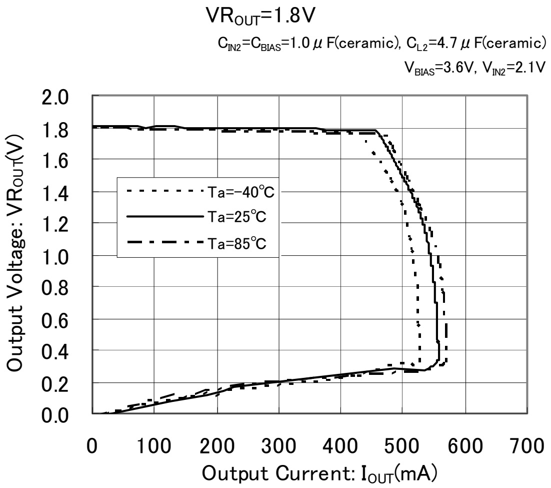
(1) Output Voltage vs. Output Current

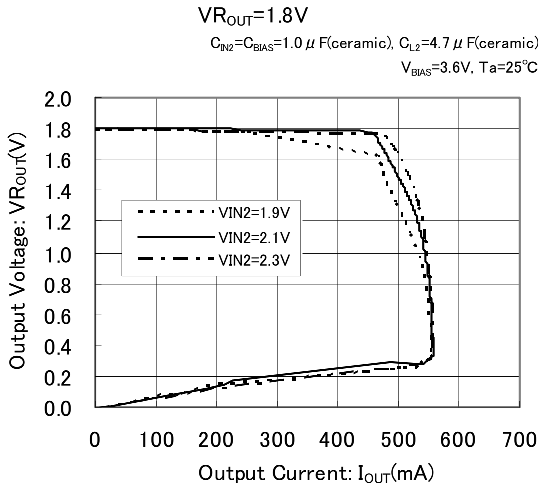






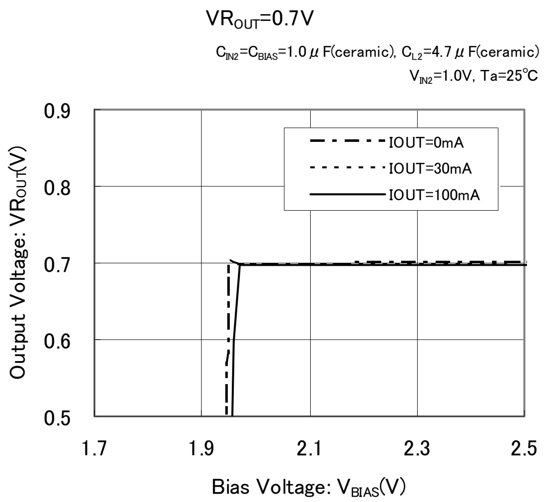


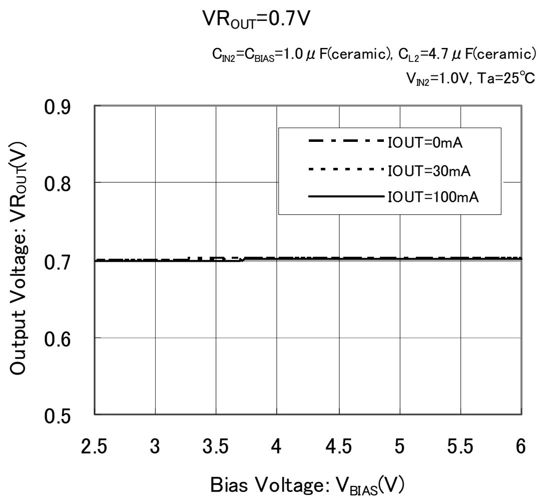


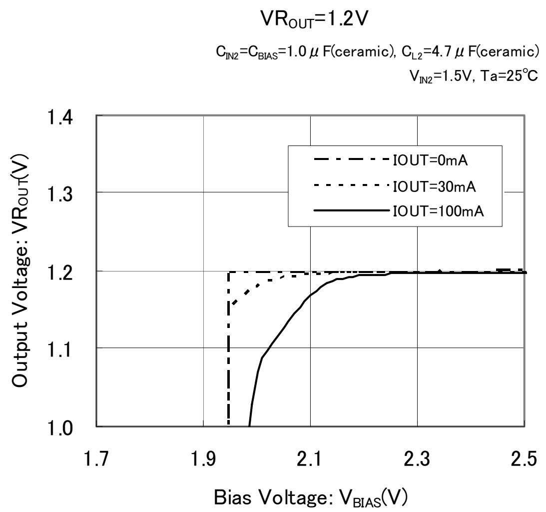


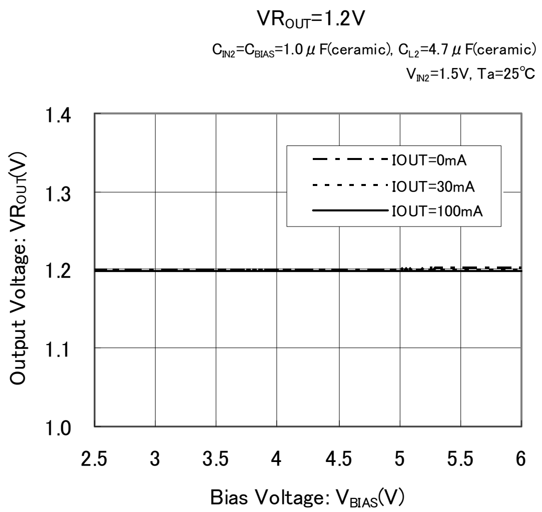
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

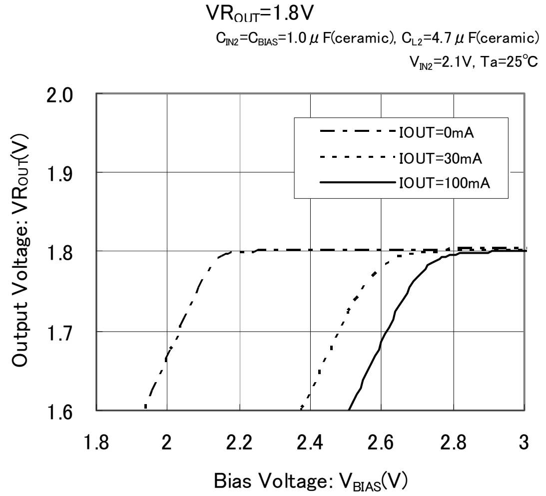
(2) Output Voltage vs. Bias Voltage

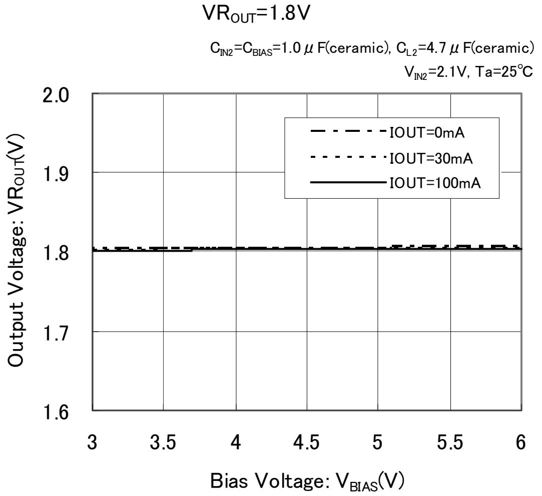










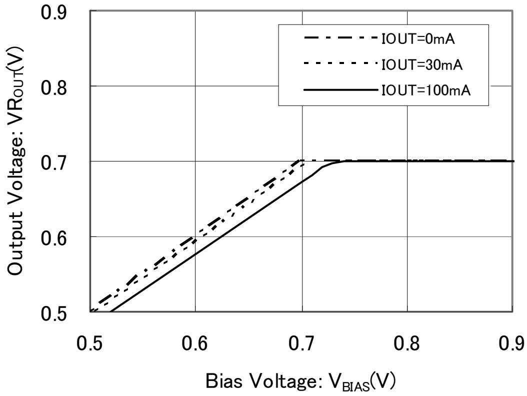


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(3) Output Voltage vs. Input Voltage

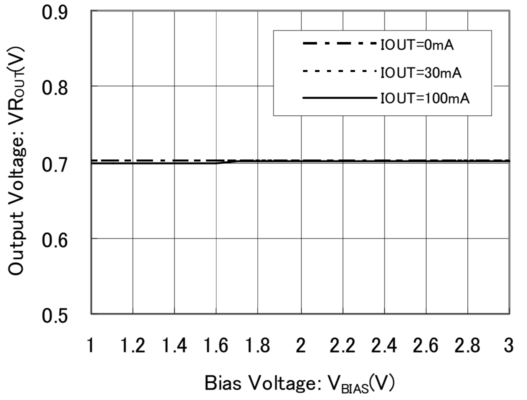
VR_{OUT}=0.7V

$C_{IN2}=C_{BIAS}$=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, Ta=25℃



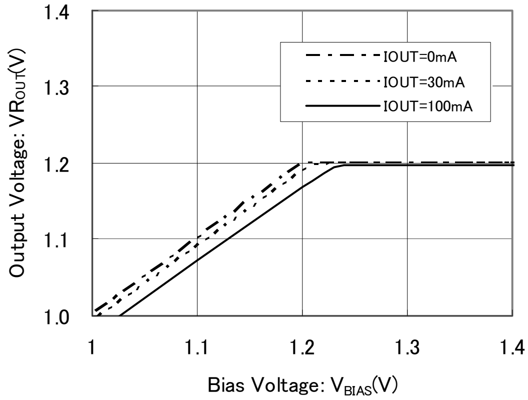
VR_{OUT}=0.7V

$C_{IN2}=C_{BIAS}$=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, Ta=25℃



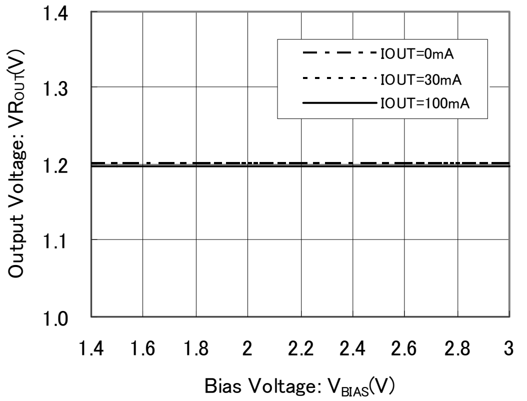
VR_{OUT}=1.2V

$C_{IN2}=C_{BIAS}$=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, Ta=25℃



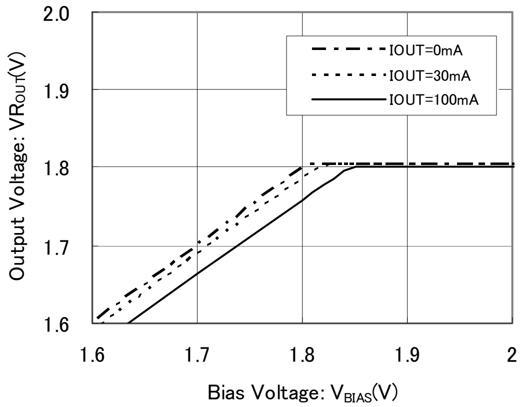
VR_{OUT}=1.2V

$C_{IN2}=C_{BIAS}$=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, Ta=25℃



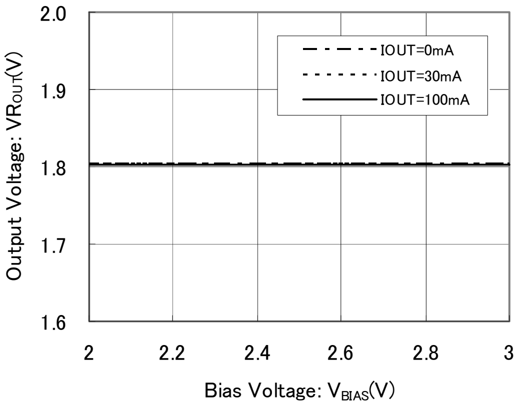
VR_{OUT}=1.8V

$C_{IN2}=C_{BIAS}$=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, Ta=25℃



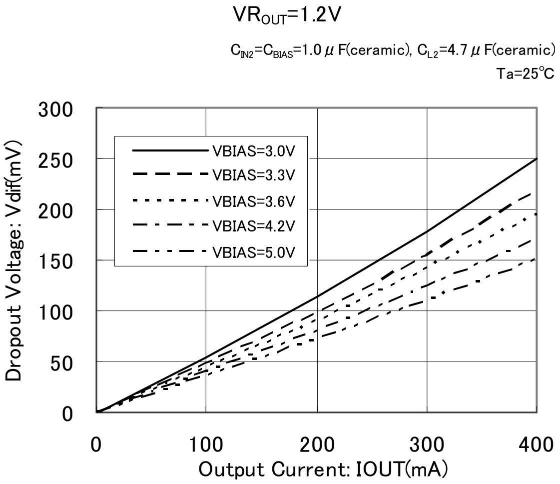
VR_{OUT}=1.8V

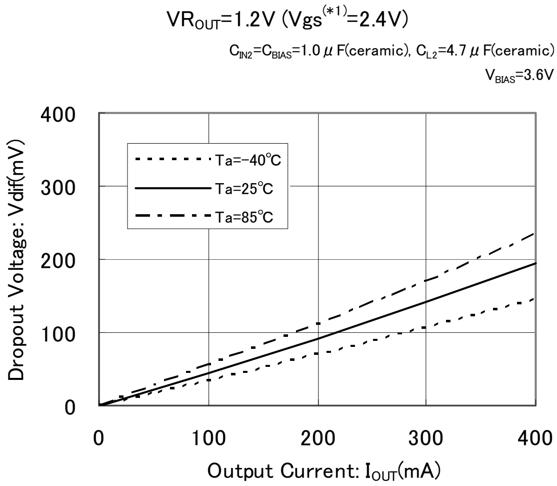
$C_{IN2}=C_{BIAS}$=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, Ta=25℃

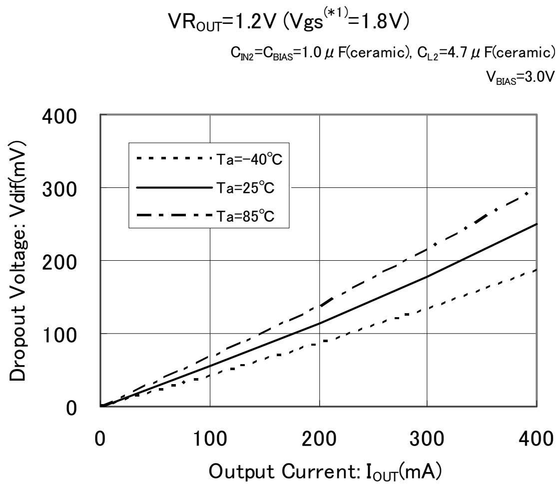


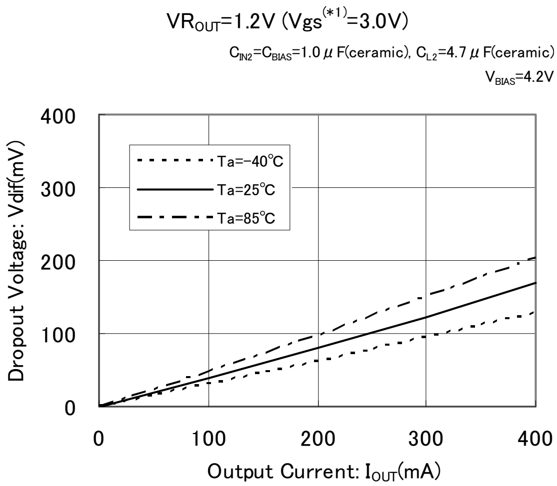
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

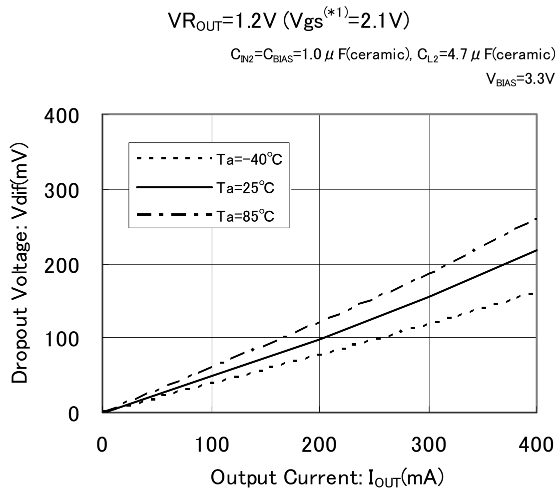
(4) Dropout Voltage vs. Output Current

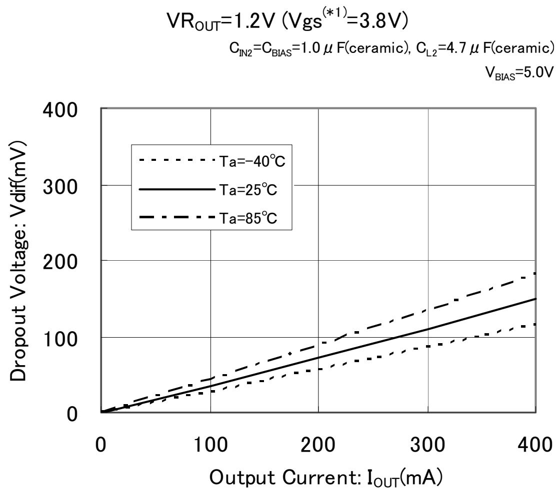








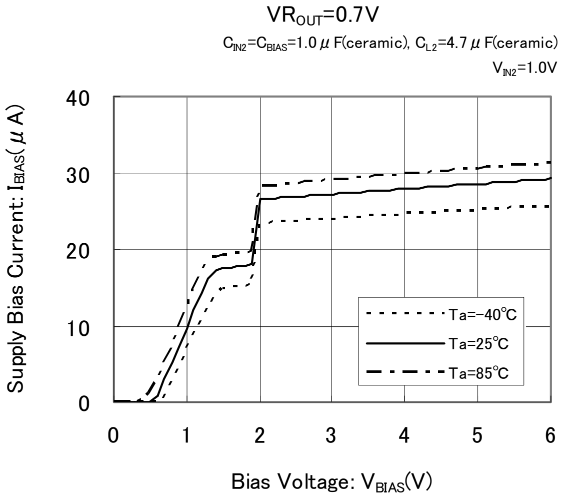


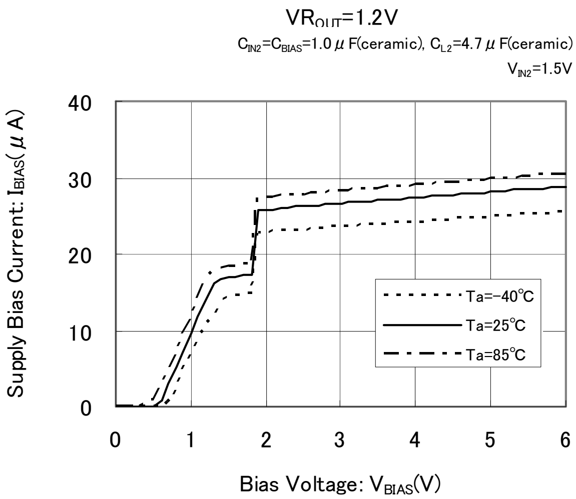


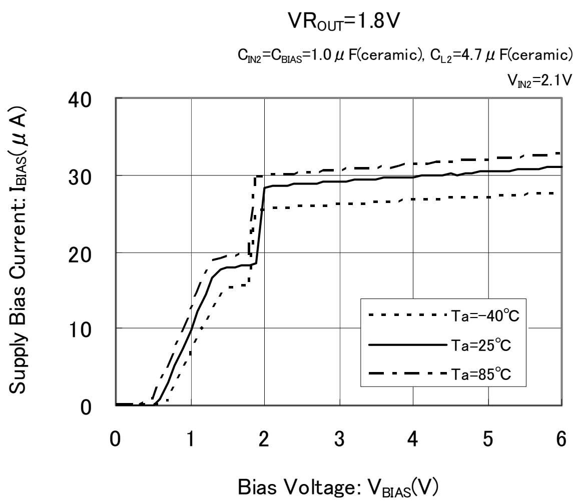
*1): Vgs is a Gate –Source voltage of the driver transistor that is defined as the value of V_{BIAS} - $V_{OUT(T)}$.
A value of the dropout voltage is determined by the value of the Vgs.

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

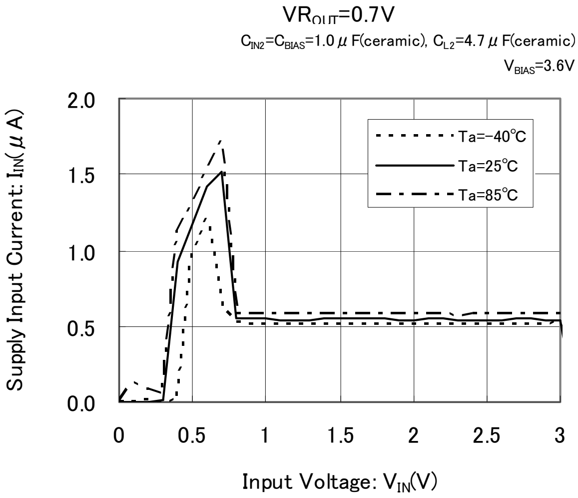
(5) Supply Bias Current vs. Bias Voltage

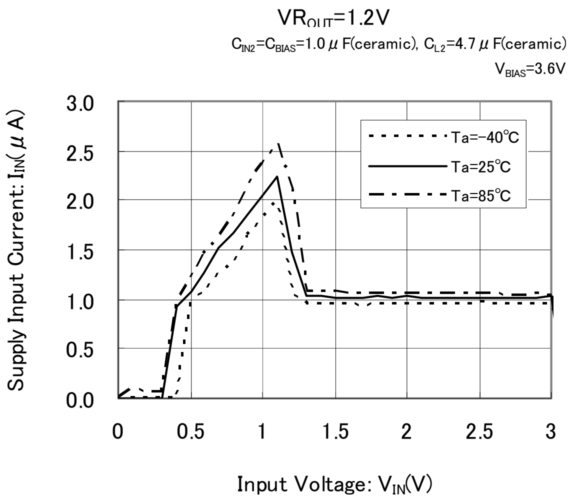


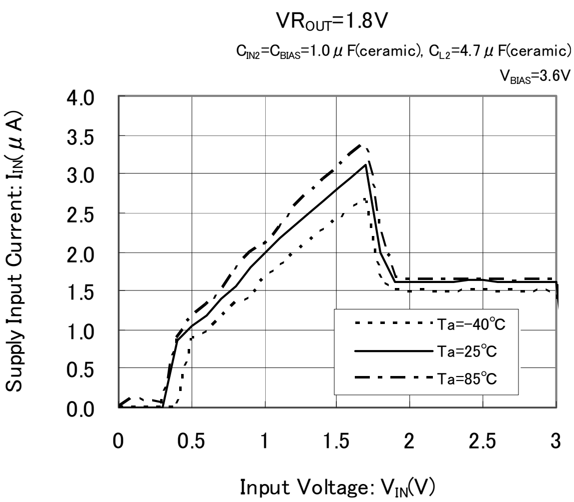




(6) Supply Input Current vs. Input Voltage

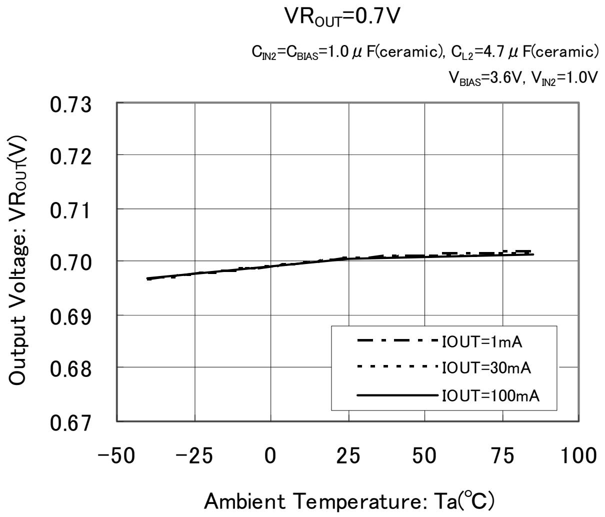


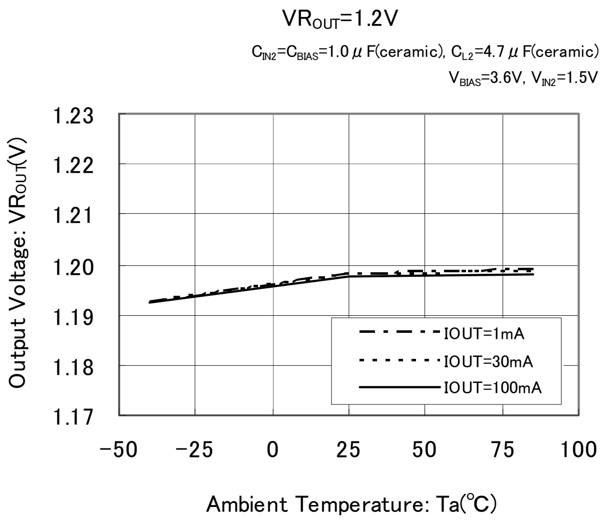


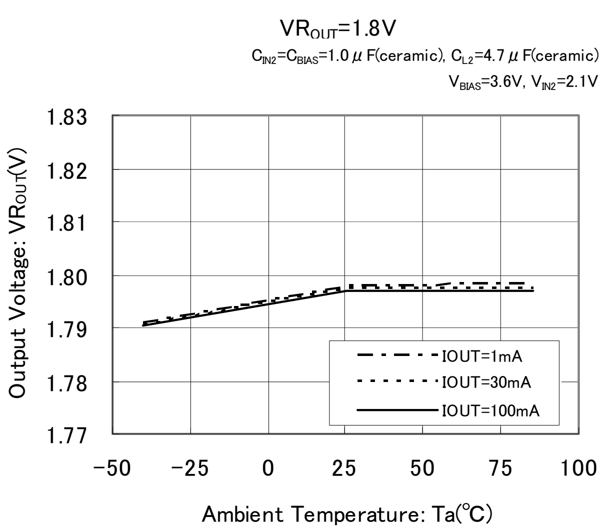


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

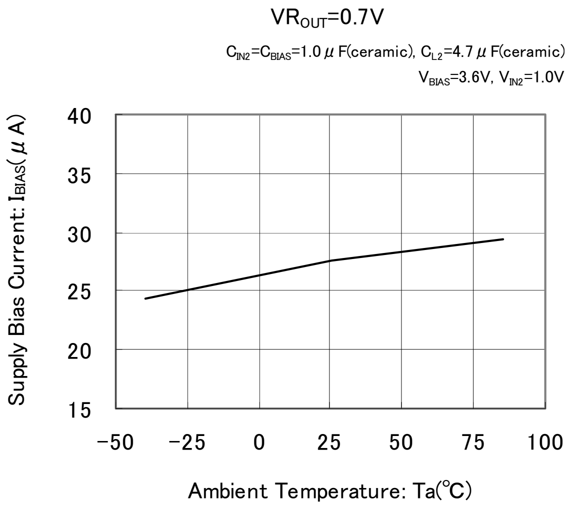
(7) Output Voltage vs. Ambient Temperature

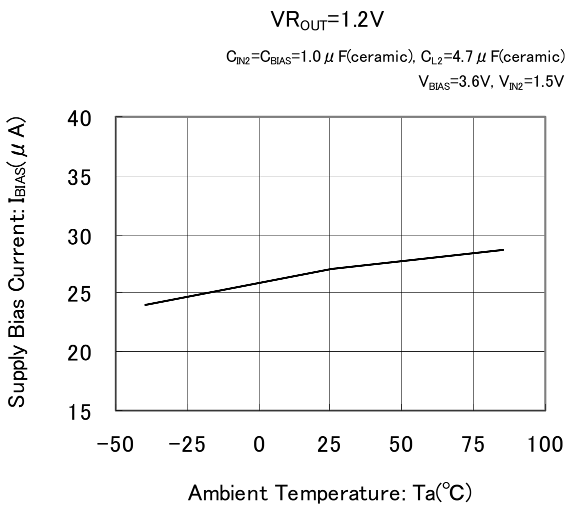


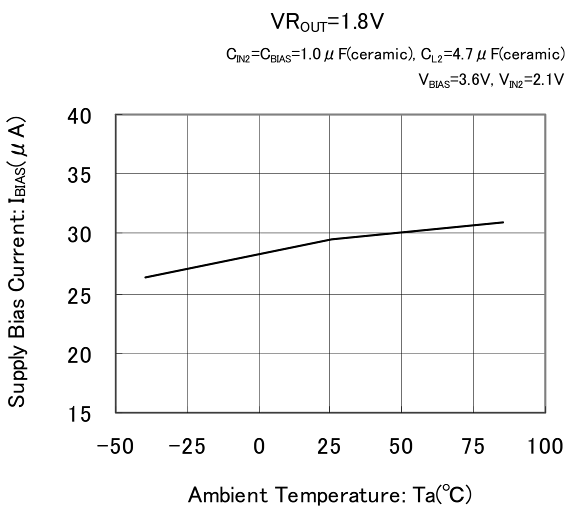




(8) Supply Bias Current vs. Ambient Temperature





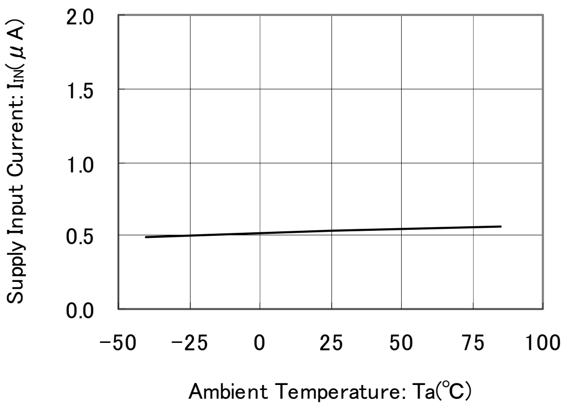


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(9) Supply Input Current vs. Ambient Temperature

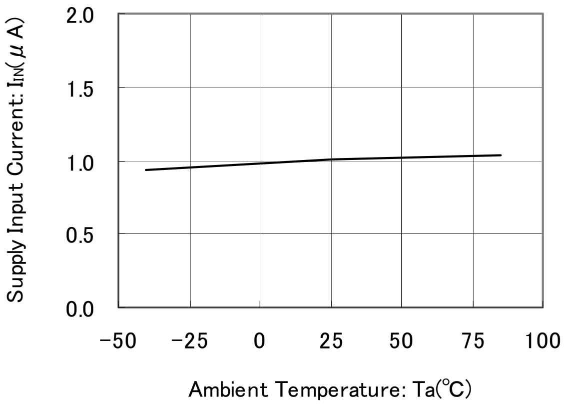
VR_{OUT}=0.7V

C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN2}=1.0V



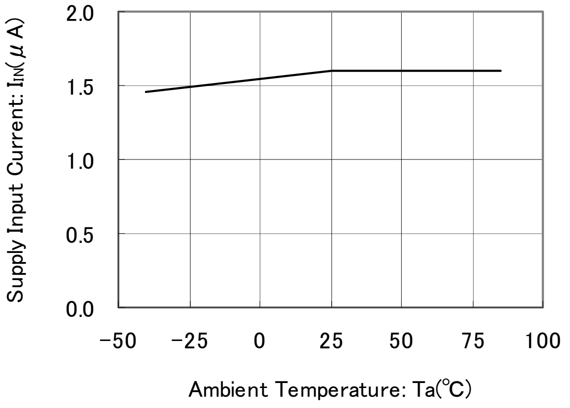
VR_{OUT}=1.2V

C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN2}=1.5V



VR_{OUT}=1.8V

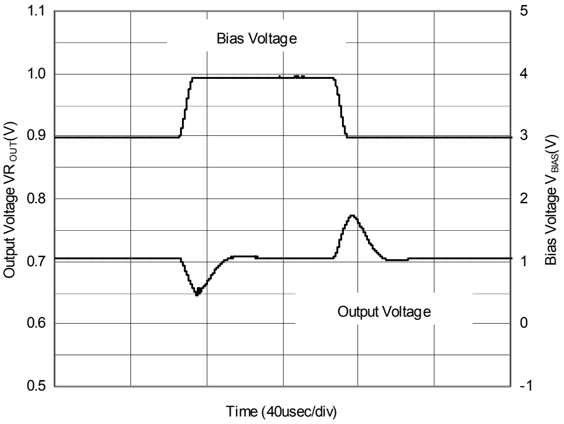
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN2}=2.1V



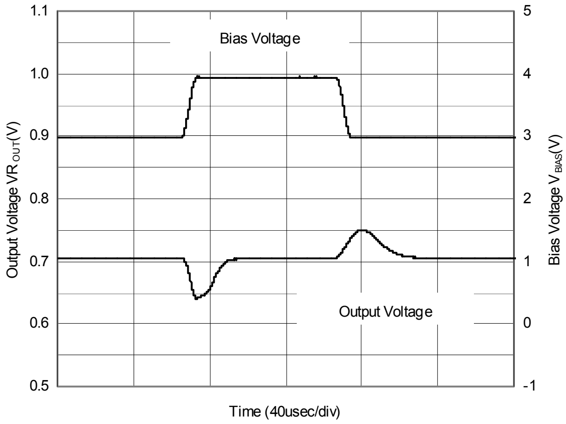
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(10) Bias Transient Response

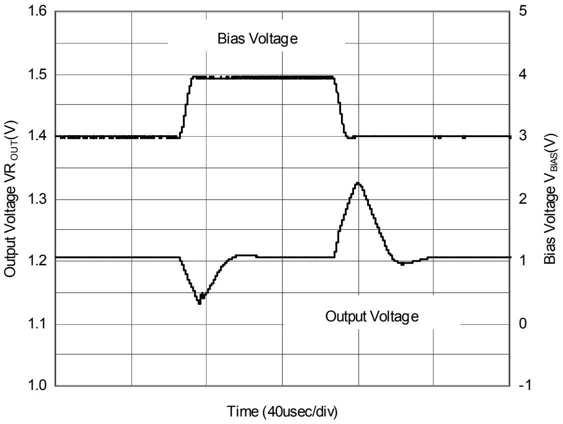
VR_{OUT}=0.7V
C_{IN2}=1.0μF(ceramic), C_{BIAS}=0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=1.0V, I_{OUT}=30mA, tr=tf=5.0μsec, Ta=25℃



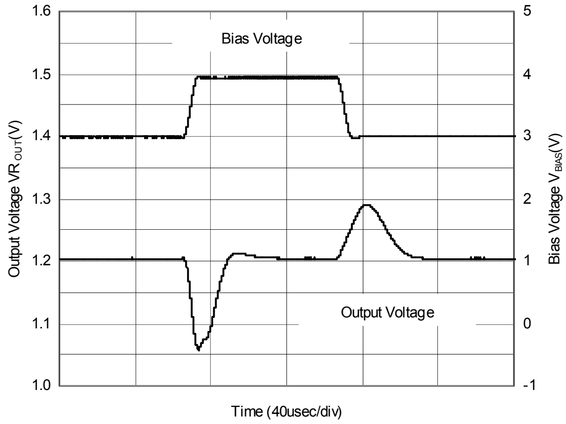
VR_{OUT}=0.7V
C_{IN2}=1.0μF(ceramic), C_{BIAS}=0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=1.0V, I_{OUT}=200mA, tr=tf=5.0μsec, Ta=25℃



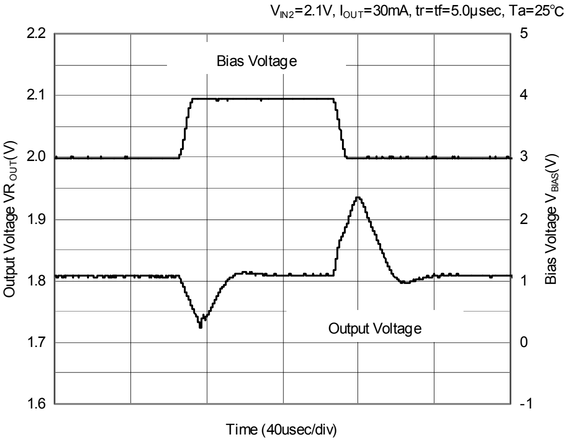
VR_{OUT}=1.2V
C_{IN2}=1.0μF(ceramic), C_{BIAS}=0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=1.5V, I_{OUT}=30mA, tr=tf=5.0μsec, Ta=25℃



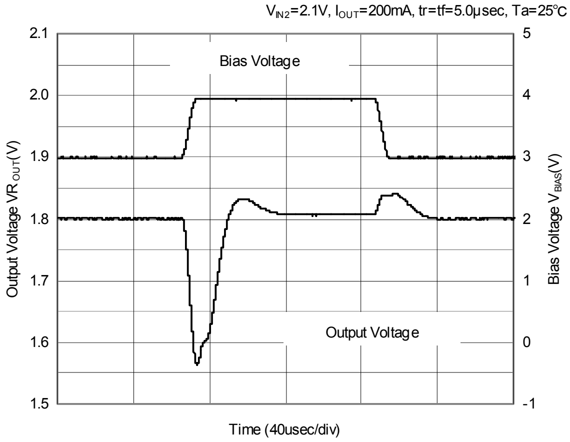
VR_{OUT}=1.2V
C_{IN2}=1.0μF(ceramic), C_{BIAS}=0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=1.5V, I_{OUT}=200mA, tr=tf=5.0μsec, Ta=25℃



VR_{OUT}=1.8V
C_{IN2}=1.0μF(ceramic), C_{BIAS}=0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=2.1V, I_{OUT}=30mA, tr=tf=5.0μsec, Ta=25℃



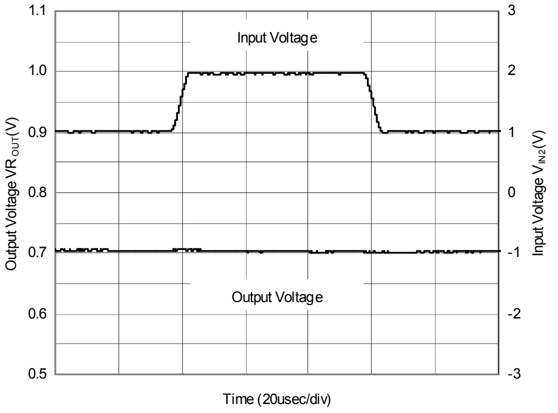
VR_{OUT}=1.8V
C_{IN2}=1.0μF(ceramic), C_{BIAS}=0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=2.1V, I_{OUT}=200mA, tr=tf=5.0μsec, Ta=25℃



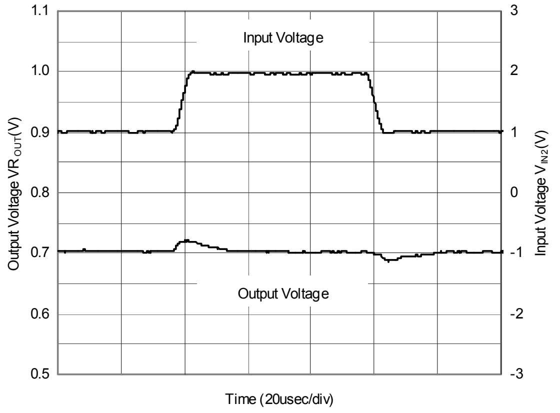
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(11) Input Transient Response

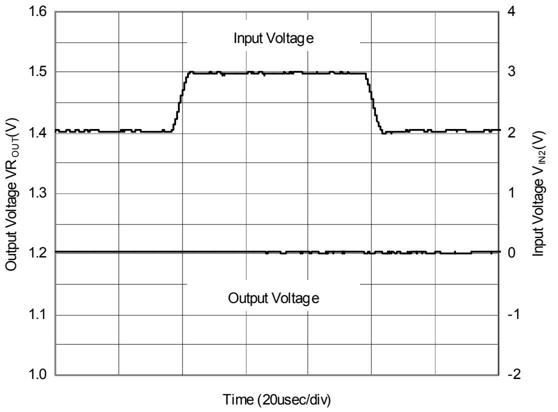
VR_{OUT}=0.7V
C_{IN2}=0.1μF(ceramic), C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, I_{OUT}=30mA, tr=tf=5.0μsec, Ta=25℃



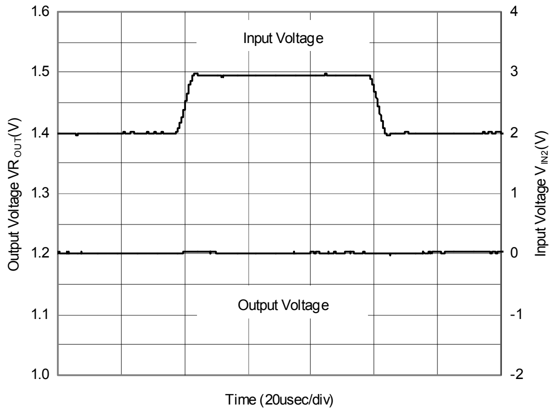
VR_{OUT}=0.7V
C_{IN2}=0.1μF(ceramic), C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, I_{OUT}=200mA, tr=tf=5.0μsec, Ta=25℃



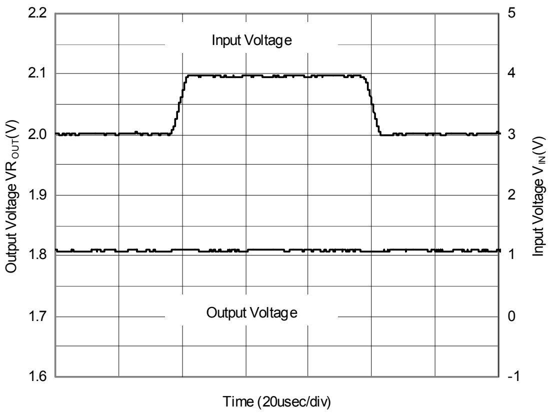
VR_{OUT}=1.2V
C_{IN2}=0.1μF(ceramic), C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, I_{OUT}=30mA, tr=tf=5.0μsec, Ta=25℃



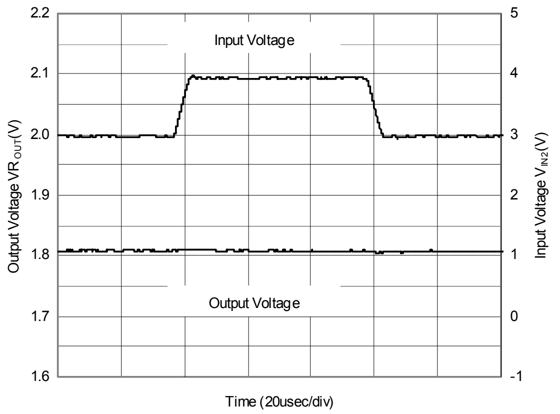
VR_{OUT}=1.2V
C_{IN2}=0.1μF(ceramic), C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, I_{OUT}=200mA, tr=tf=5.0μsec, Ta=25℃



VR_{OUT}=1.8V
C_{IN2}=0.1μF(ceramic), C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, I_{OUT}=30mA, tr=tf=5.0μsec, Ta=25℃



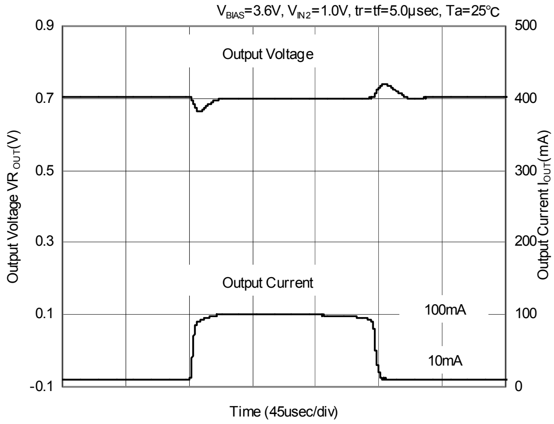
VR_{OUT}=1.8V
C_{IN2}=0.1μF(ceramic), C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, I_{OUT}=200mA, tr=tf=5.0μsec, Ta=25℃



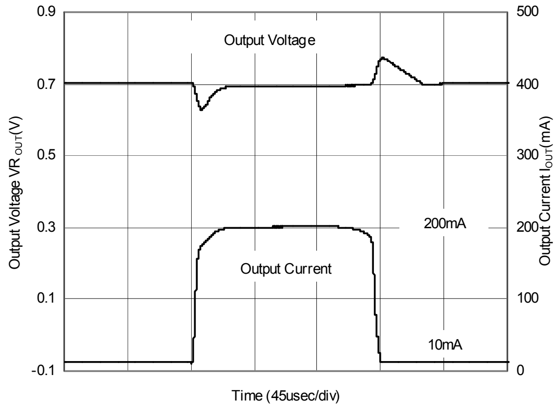
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(12) Load Transient Response

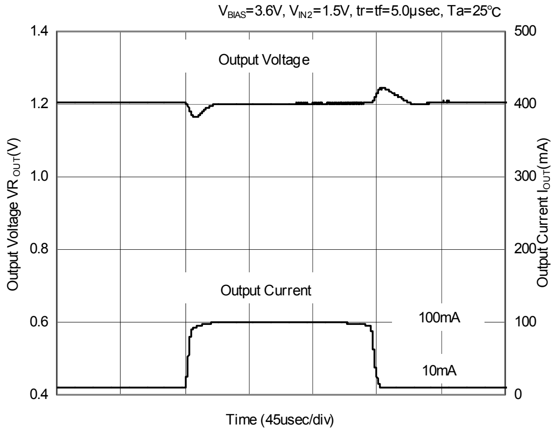
VR_{OUT}=0.7V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN2}=1.0V, tr=tf=5.0μsec, Ta=25℃



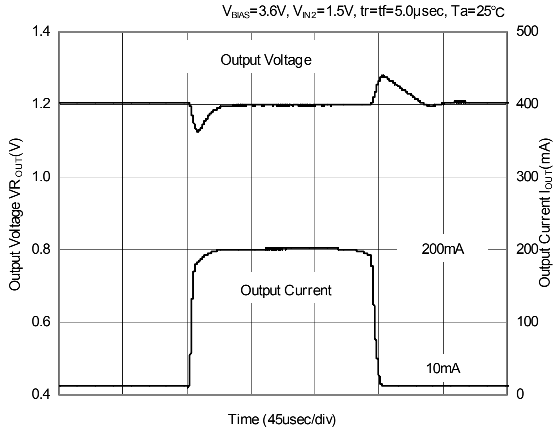
VR_{OUT}=0.7V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN2}=1.0V, tr=tf=5.0μsec, Ta=25℃



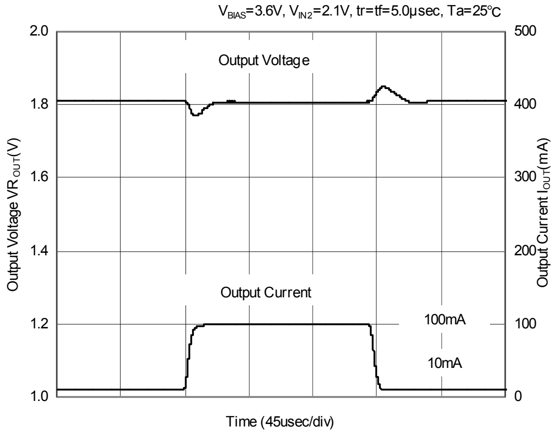
VR_{OUT}=1.2V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN2}=1.5V, tr=tf=5.0μsec, Ta=25℃



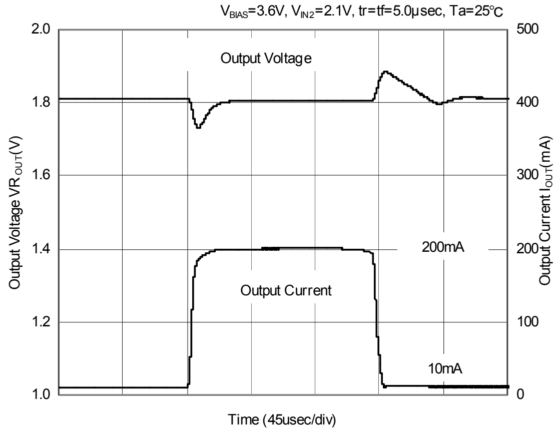
VR_{OUT}=1.2V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN2}=1.5V, tr=tf=5.0μsec, Ta=25℃



VR_{OUT}=1.8V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN2}=2.1V, tr=tf=5.0μsec, Ta=25℃



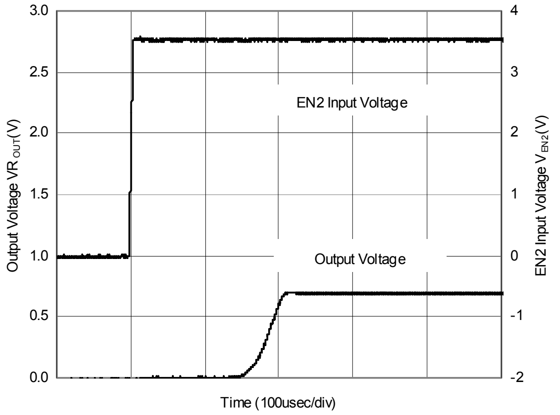
VR_{OUT}=1.8V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{BIAS}=3.6V, V_{IN2}=2.1V, tr=tf=5.0μsec, Ta=25℃



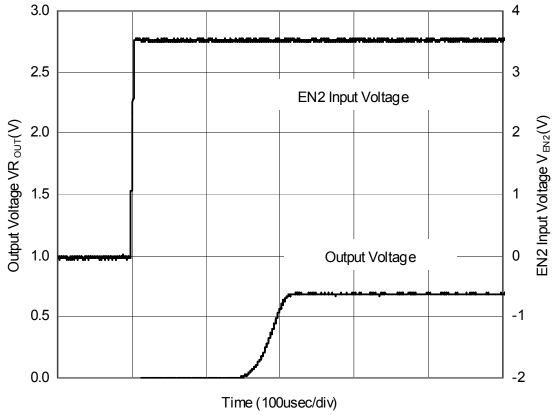
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(13) CE Rising Response Time

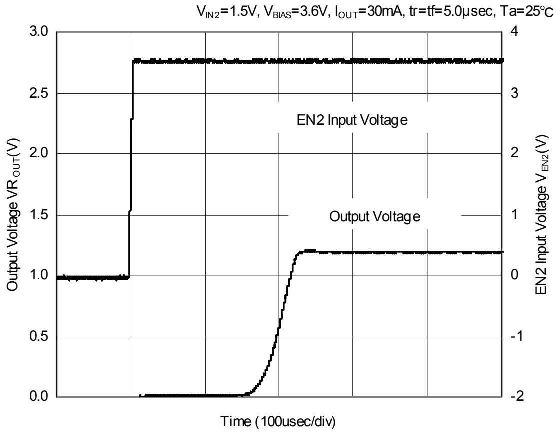
VR_{OUT}=0.7V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=1.0V, V_{BIAS}=3.6V, I_{OUT}=30mA, tr=tf=5.0μsec, Ta=25℃



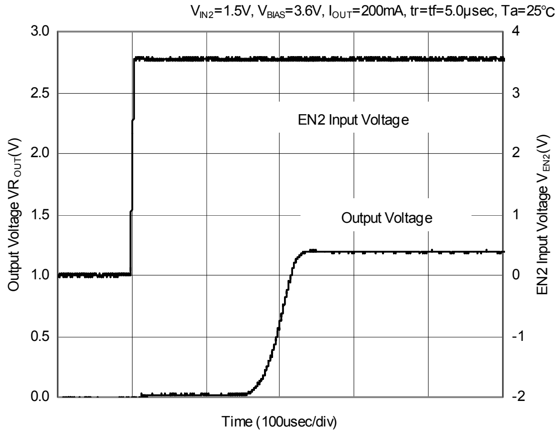
VR_{OUT}=0.7V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=1.0V, V_{BIAS}=3.6V, I_{OUT}=200mA, tr=tf=5.0μsec, Ta=25℃



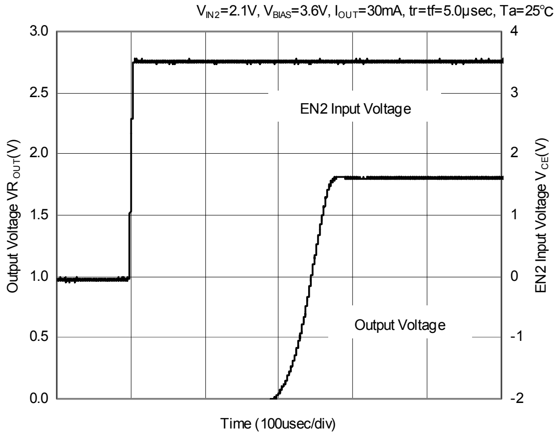
VR_{OUT}=1.2V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=1.5V, V_{BIAS}=3.6V, I_{OUT}=30mA, tr=tf=5.0μsec, Ta=25℃



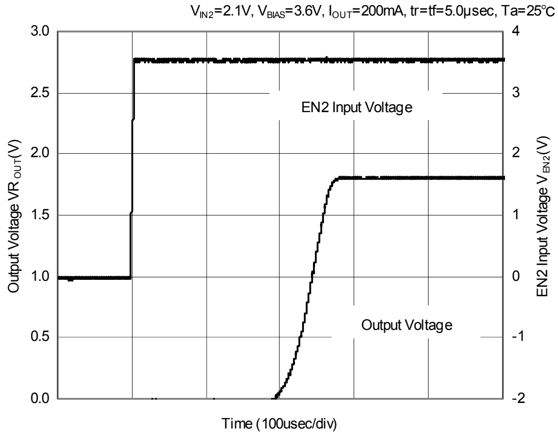
VR_{OUT}=1.2V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=1.5V, V_{BIAS}=3.6V, I_{OUT}=200mA, tr=tf=5.0μsec, Ta=25℃



VR_{OUT}=1.8V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=2.1V, V_{BIAS}=3.6V, I_{OUT}=30mA, tr=tf=5.0μsec, Ta=25℃

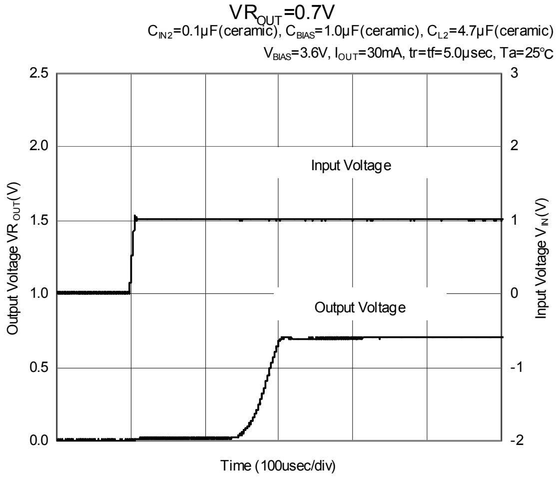


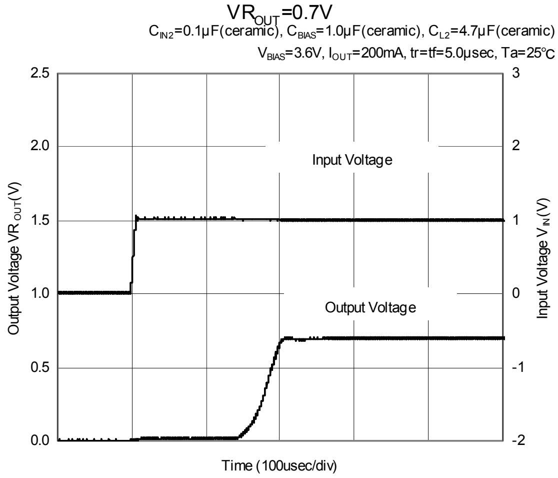
VR_{OUT}=1.8V
C_{IN2}=C_{BIAS}=1.0μF(ceramic), C_{L2}=4.7μF(ceramic)
V_{IN2}=2.1V, V_{BIAS}=3.6V, I_{OUT}=200mA, tr=tf=5.0μsec, Ta=25℃

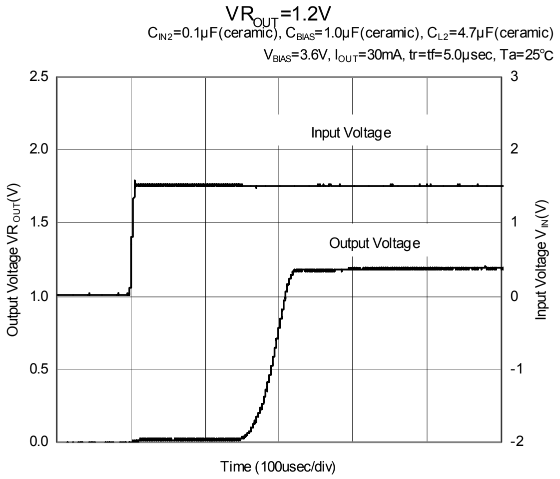


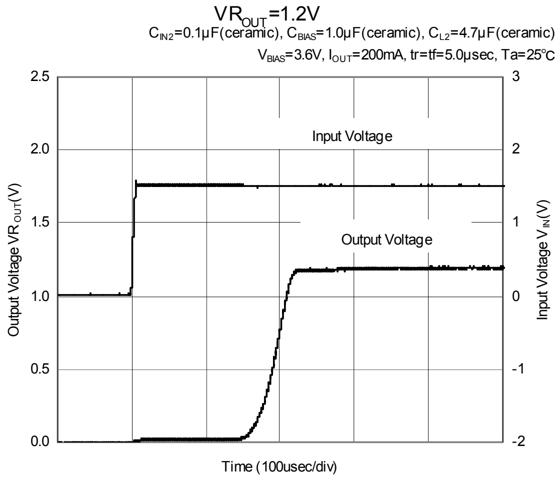
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

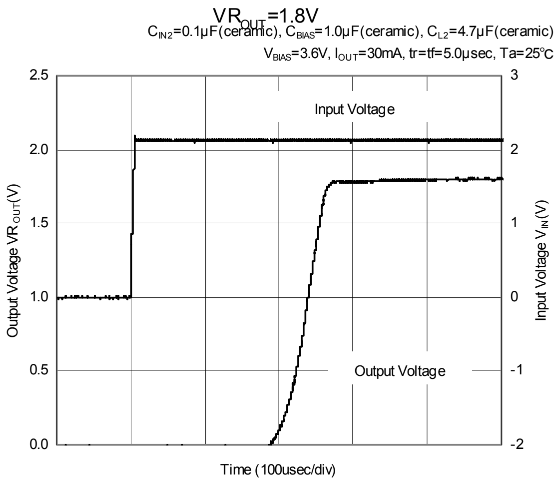
(14) V_{IN} Rising Response Time

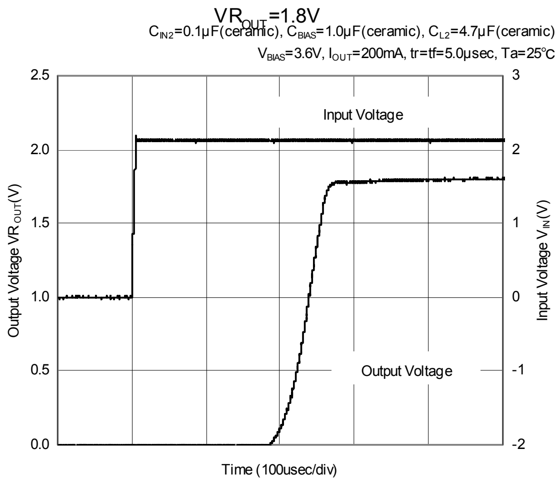






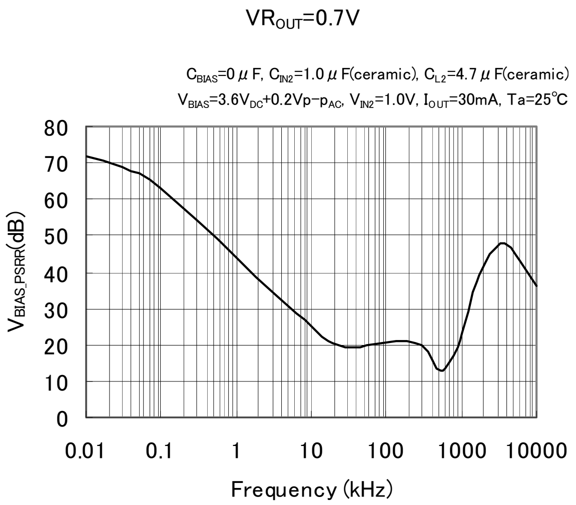


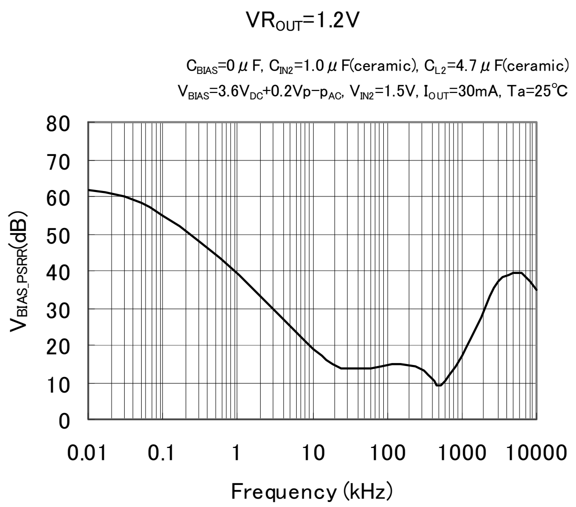


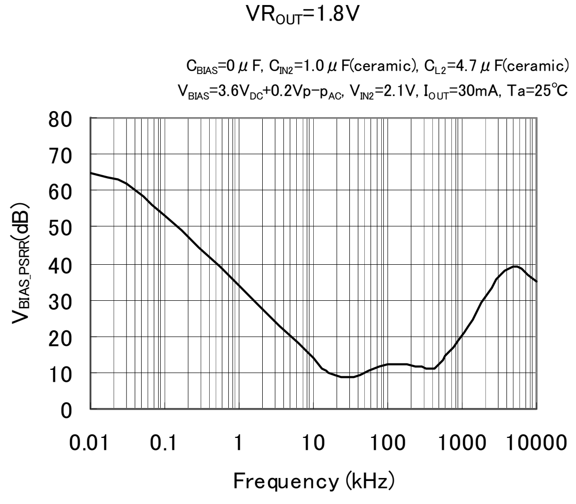


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

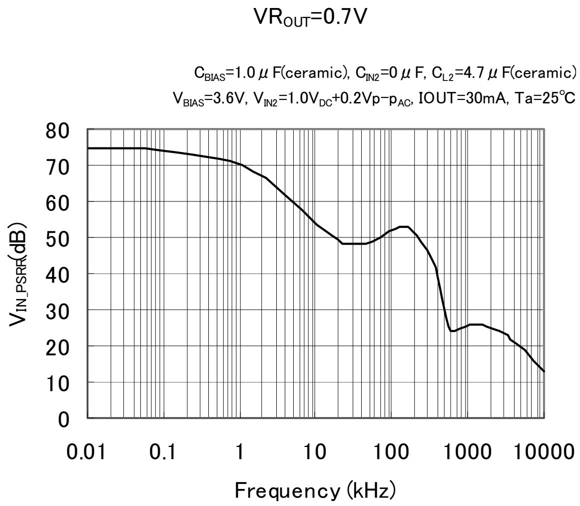
(15) Bias Voltage Ripple Rejection Rate

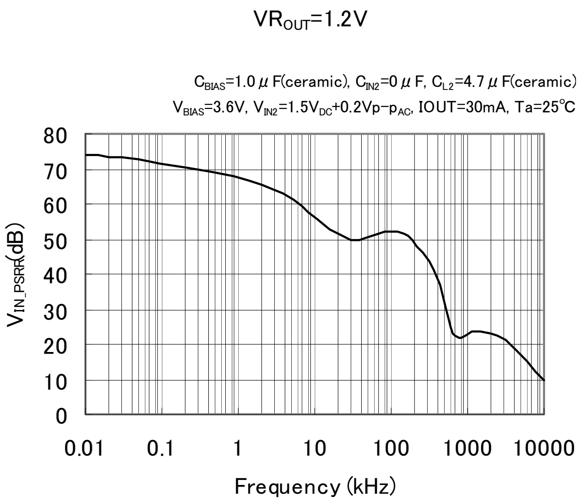


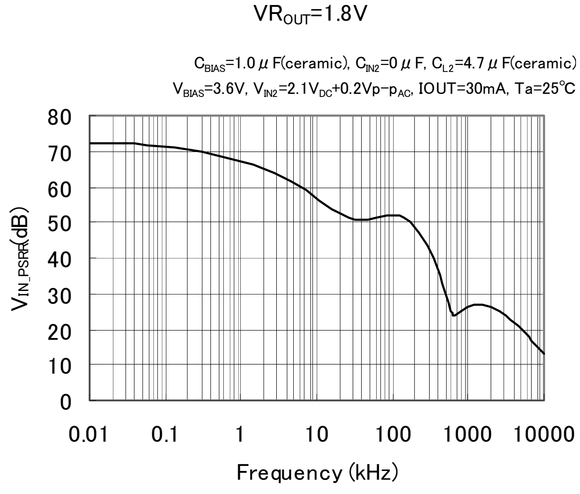




(16) Input Voltage Ripple Rejection Rate

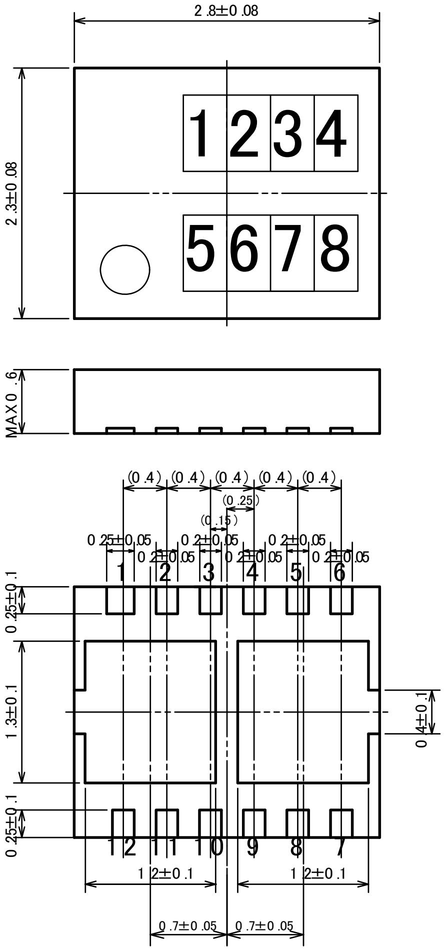


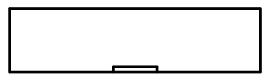




■PACKAGING INFORMATION

●USP-12B01





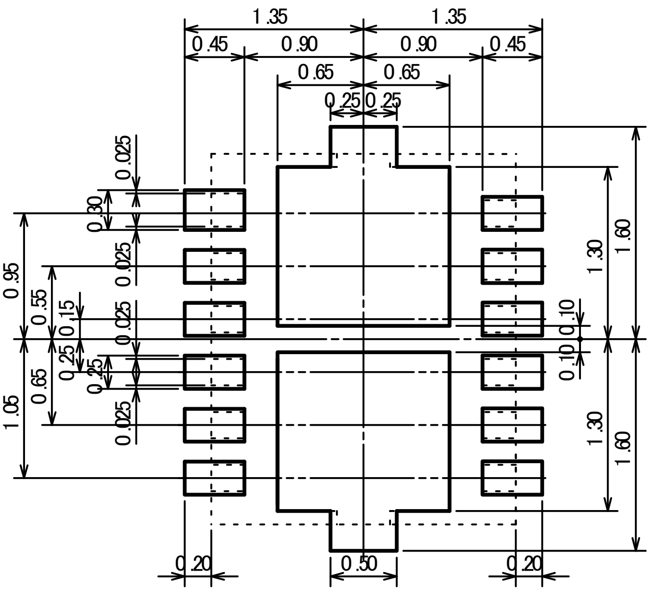
* Au plate thickness: Minimum 0.3 μm

*The side of pins is not plated, nickel is exposed.

*Pin #1 is wider than other pins.

UNIT: mm

●USP-12B01 Reference Pattern Layout



●USP-12B01 Reference Metal Mask Design