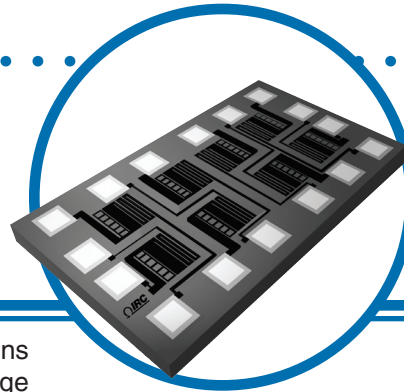


# Wire Bondable Resistor Network Arrays

## Chip Network Array Series

- Absolute tolerances to  $\pm 0.1\%$
- Tight TCR tracking to  $\pm 5\text{ppm}/^\circ\text{C}$
- Ratio match tolerances to  $\pm 0.05\%$
- Ultra-stable tantalum nitride resistors



IRC's TaNSil<sup>®</sup> network array resistors are ideally suited for applications that demand a small footprint. The small wire bondable chip package provides higher component density, lower resistor cost and high reliability.

The tantalum nitride film system on silicon provides precision tolerance, exceptional TCR tracking and low cost. Excellent performance in harsh, humid environments is a trademark of IRC's self-passivating TaNSil<sup>®</sup> resistor film.

For applications requiring high performance resistor networks in a low cost, wire bondable package, specify IRC network array die.

## Electrical Data

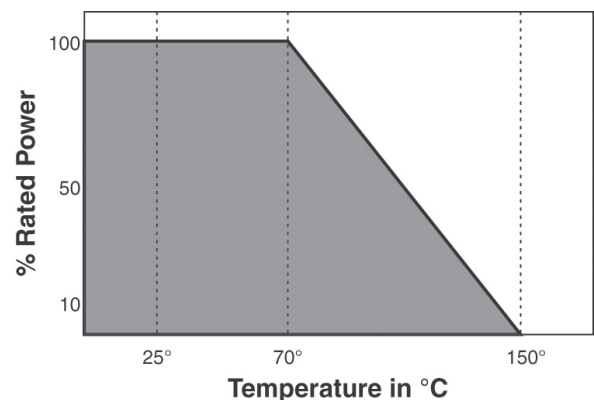
	Isolated	Bussed
<b>Resistance Range</b>	10 $\Omega$ to 2.5M $\Omega$	10 $\Omega$ to 1.25M $\Omega$
<b>Absolute Tolerance</b>	to $\pm 0.1\%$	
<b>Ratio Tolerance to R1</b>	to $\pm 0.05\%$	to $\pm 0.1\%$
<b>Absolute TCR</b>	to $\pm 25\text{ppm}/^\circ\text{C}$	
<b>Tracking TCR</b>	to $\pm 5\text{ppm}/^\circ\text{C}$	
<b>Element Power Rating</b>	100mW @ 70 $^\circ\text{C}$	50mW @ 70 $^\circ\text{C}$
<b>Package Power Rating</b>	8-Pad 400mW @ 70 $^\circ\text{C}$ 16-Pad 800mW @ 70 $^\circ\text{C}$ 24-Pad 1.0W @ 70 $^\circ\text{C}$	
<b>Rated Operating Voltage (not to exceed <math>\sqrt{P \times R}</math>)</b>	100V	
<b>Operating Temperature</b>	-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$	
<b>Noise</b>	<-30dB	
<b>Substrate Material</b>	Oxidized Silicon (10K $\text{\AA}$ SiO <sub>2</sub> minimum)	
<b>Substrate Thickness</b>	0.016" $\pm 0.001$ (0.406mm $\pm 0.01$ )	
<b>Bond Pad Metallization</b>	Aluminum	10K $\text{\AA}$ minimum
	Gold	15K $\text{\AA}$ minimum
<b>Backside</b>	Silicon (gold available)	
<b>Passivation</b>	Silicon Dioxide or Silicon Nitride	

## TCR/Inspection Code Table

Absolute TCR	Commercial Code	MIL Inspection Code*
$\pm 300\text{ppm}/^\circ\text{C}$	00	04
$\pm 100\text{ppm}/^\circ\text{C}$	01	05
$\pm 50\text{ppm}/^\circ\text{C}$	02	06
$\pm 25\text{ppm}/^\circ\text{C}$	03	07

\*Notes: Product supplied to Class H of MIL-PRF 38534 include 100% visual inspection

## Power Derating Data



### General Note

IRC reserves the right to make changes in product specification without notice or liability. All information is subject to IRC's own data and is considered accurate at time of going to print.

# Wire Bondable Resistor Network Arrays



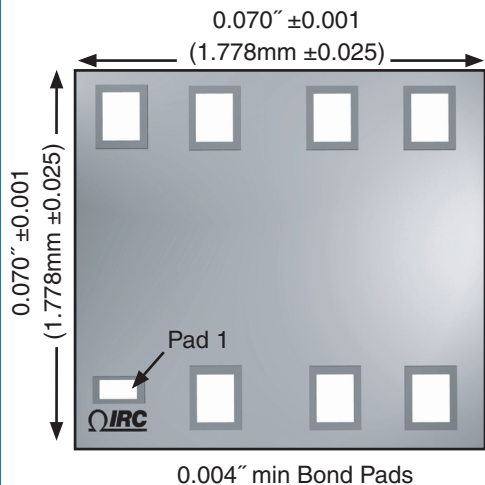
## Manufacturing Capabilities Data

Absolute TCR ( $\pm$ ppm/ $^{\circ}$ C)	Isolated schematic A				Bussed schematic B			
	Ohmic range ( $\Omega$ )	Available tolerances	Available ratio tolerances	Best TCR tracking ( $\pm$ ppm/ $^{\circ}$ C)	Ohmic range ( $\Omega$ )	Available tolerances	Available ratio tolerances	Best TCR tracking ( $\pm$ ppm/ $^{\circ}$ C)
300	10 - 25	F G J	F G	50	10 - 25	F G J	F G	200
	26 - 50	D F G J	C D F	10	26 - 50	F G J	D F G	100
	51 - 200	C D F G J	C D F G	5	51 - 100	D F G J	C D F G	50
	201 - 2.5M	B C D F G J	A B C D F G	5	101 - 200	D F G J	B C D F G	25
					201 - 500	B C D F G J	B C D F G	20
					501 - 1.25M	B C D F G J	A B C D F G	5
100	26 - 50	D F G J	C D F G	10	26 - 50	F G J	D F G	100
	51 - 200	C D F G J	C D F G	5	51 - 100	D F G J	C D F G	50
	201 - 2.5M	B C D F G J	A B F G	5	101 - 200	D F G J	B C D F G	25
					201 - 500	B C D F G J	B C D F G	20
					501 - 350K	B C D F G J	A B C D F G	5
50	26 - 50	D F G J	C D F G	10	51 - 100	D F G J	C D F G	50
	51 - 200	C D F G J	C D F G	5	101 - 200	D F G J	B C D F G	25
	201 - 2.5M	B C D F G J	A B F G	5	201 - 500	B C D F G J	B C D F G	20
					501 - 1.25M	B C D F G J	A B C D F G	5
25	51 - 200	C D F G J	C D F G	5	201 - 500	B C D F G J	B C D F G	20
	201 - 2.5M	B C D F G J	A B F G	5	501 - 1.25M	B C D F G J	A B C D F G	5

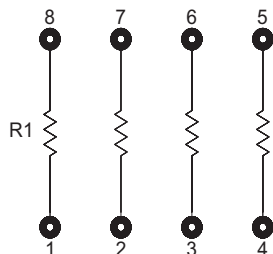
# Wire Bondable Resistor Network Arrays

## Physical Data

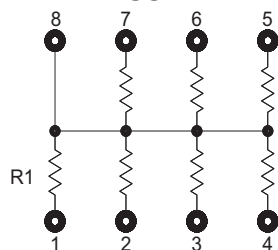
**DSS4X**



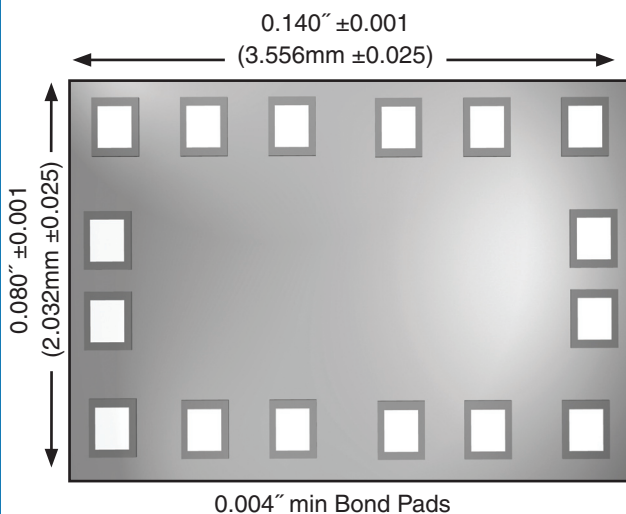
**DSS4A**



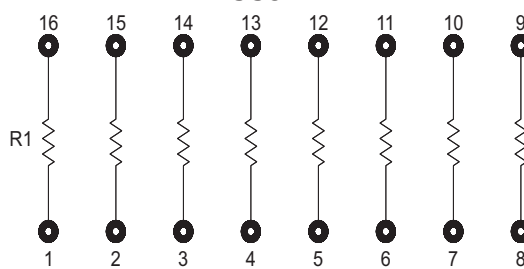
**DSS4B**



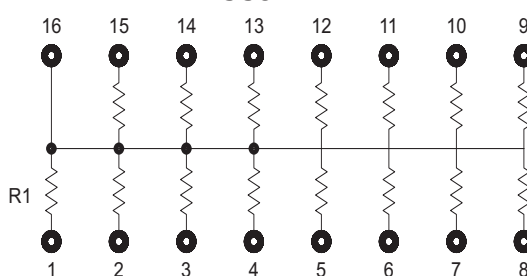
**DSS8X**



**DSS8A**



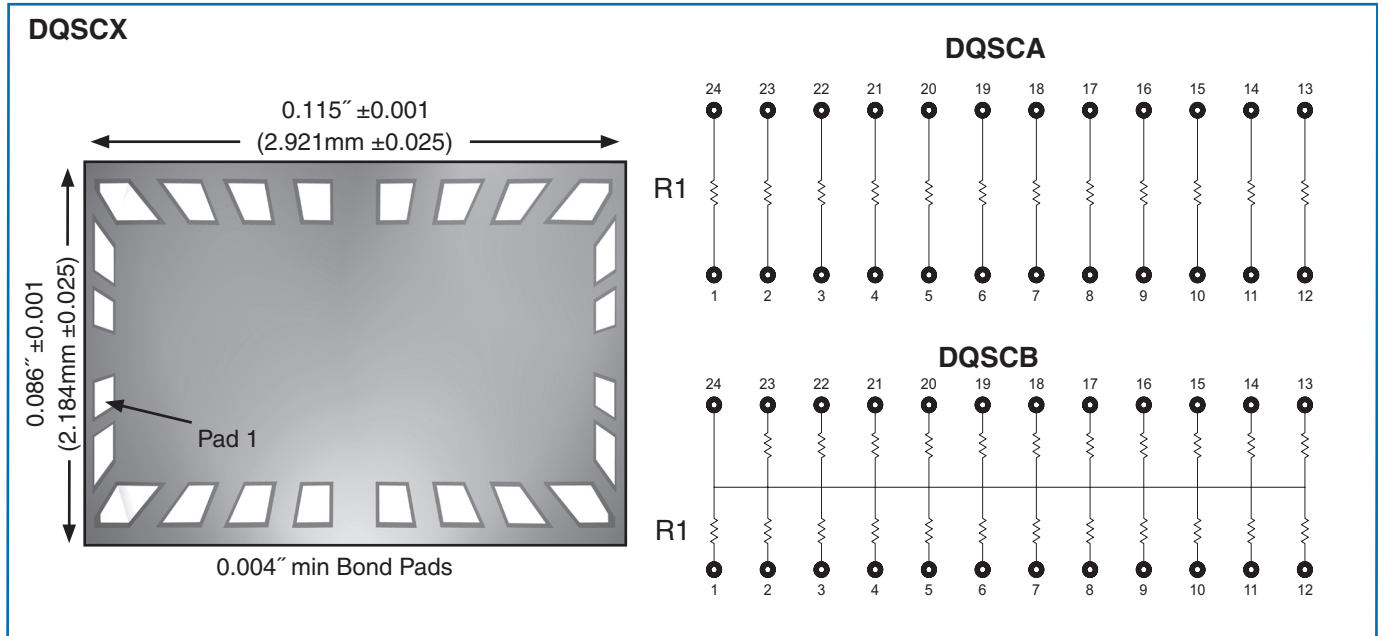
**DSS8B**



# Wire Bondable Resistor Network Arrays



## Physical Data



## Environmental Data

Test	Method	Max $\Delta R$	Typical $\Delta R$
Thermal Shock	MIL-STD-202 Method 107 Test condition F	$\pm 0.1\%$	$\pm 0.02\%$
High Temperature Exposure	MIL-STD-883 Method 1008 150°C, 1000 hours	$\pm 0.1\%$	$\pm 0.05\%$
Low Temperature Storage	-55°C, 1000 hours	$\pm 0.03\%$	$\pm 0.01\%$
Life	MIL-STD-202 Method 108 70°C, 1000 hours	$\pm 0.5\%$	$\pm 0.01\%$
Life at Elevated Temperature	MIL-STD-202 Method 108 125°C, 1000 hours	$\pm 0.5\%$	$\pm 0.05\%$

## Ordering Data

Prefix ..... **WBD** **DSS8** **B** **01** **1002** **F** **B**

Style .....  
 DSS4 = 8-pad Network  
 DSS8 = 6-pad Network  
 DQSC = 24-pad Network

Schematic and Termination .....  
 A = Isolated; B = Bussed

TCR/Inspection Code .....  
 Reference TCR/Inspection Code Table

Resistance Code .....  
 4-Digit Resistance Code  
 Ex: 1002 = 10K $\Omega$ , 50R1 = 50.1 $\Omega$

Absolute Tolerance Code .....  
 J =  $\pm 5\%$ ; G =  $\pm 2\%$ ; F =  $\pm 1\%$ ;  
 D =  $\pm 0.5\%$ ; C =  $\pm 0.25\%$ ; B =  $\pm 0.1\%$

Ratio Tolerance Code (optional) .....  
 G =  $\pm 2\%$ ; F =  $\pm 1\%$ ; D =  $\pm 0.5\%$ ;  
 C =  $\pm 0.25\%$ ; B =  $\pm 0.1\%$ ; A = 0.05%

Packaging  
 Standard packaging is 2" x 2" chip tray. For additional information or to discuss your specific requirements, please contact our Applications Team using the contact details below.