3.3V/2.5V 1:9 LVCMOS Clock Fanout Buffer

Features

- 9 LVCMOS Compatible Clock Outputs
- 2 Selectable, LVCMOS Compatible Inputs
- Maximum Clock Frequency of 350 MHz
- Maximum Clock Skew of 150 pS
- Synchronous Output Stop in Logic Low State Eliminates Output Runt Pulses
- High–Impedance Output Control
- 3.3V or 2.5V Power Supply
- Drives up to 18 Series Terminated Clock Lines
- Ambient Temperature Range -40°C to +85°C
- 32 Lead LQFP and TQFP Packaging
- Supports Clock Distribution in Networking, Telecommunications and Computer Applications
- Pin and Function Compatible to MPC947 and MPC9447

Functional Description

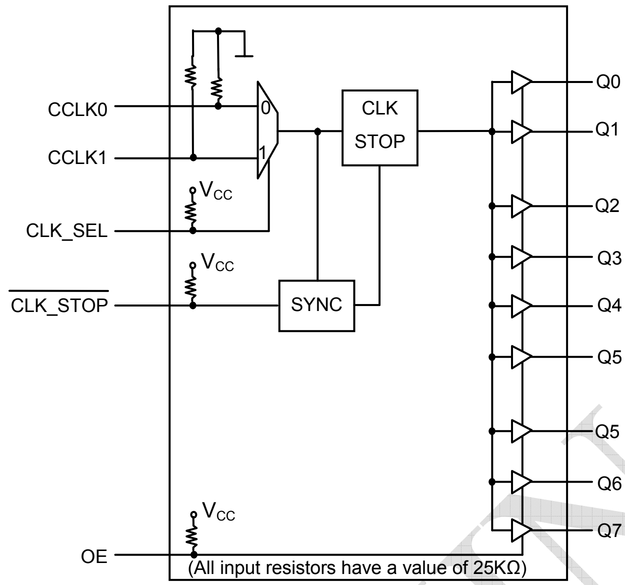
The PCS2I99447 is a 3.3V or 2.5V compatible, 1:9 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 350 MHz and output skews less than 150 pS, the device meets the needs of most demanding clock applications.

PCS2I99447 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 350 MHz. Each output provides a precise copy of the input signal with a near zero skew. The outputs buffers support driving of 50Ω terminated transmission lines on the incident edge: each is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable independent LVCMOS compatible clock inputs are available, providing support of redundant clock source systems. The PCS2I99447 $\overline{\text{CLK\_STOP}}$ control is synchronous to the falling edge of the input clock. It allows the start and stop of the output clock signal only in a logic low state, thus eliminating potential output runt pulses. Applying the OE control will force the outputs into high impedance mode.

All inputs have an internal pull–up or pull–down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of –40°C to +85°C. The PCS2I99447 is pin and function compatible but performance enhanced to the MPC947 and MPC9447.

Block Diagram



Pin Configuration

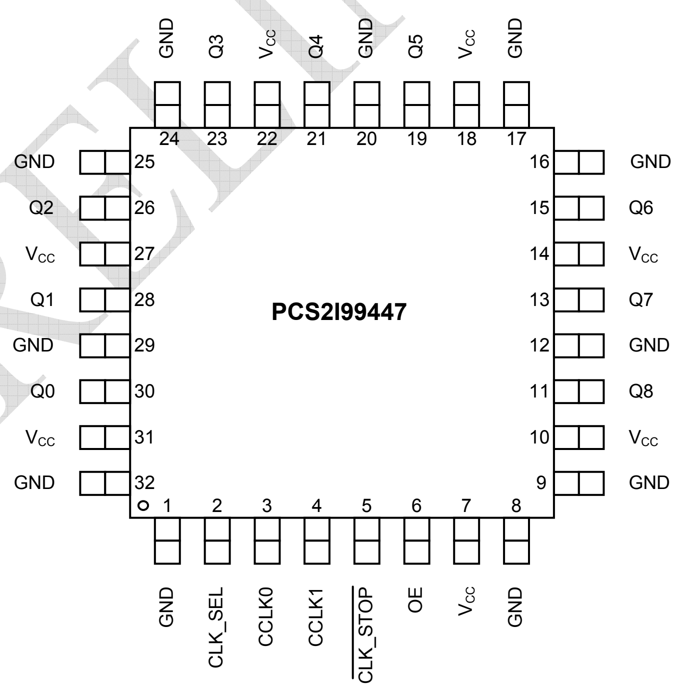


Table 1. Function Table

Control	Default	0	1
CLK_SEL	1	CLK0 input selected	CLK1 input selected
OE	1	Outputs disabled (high–impedance state)[1]	Outputs enabled
$\overline{\text{CLK\_STOP}}$	1	Outputs synchronously stopped in logic low state	Outputs active

Note: 1. OE = 0 will high–impedance tristate all outputs independent on $\overline{\text{CLK\_STOP}}$

Table 2. Pin Configuration

Pin #	Pin Name	I/O	Type	Function
3	CCLK0	Input	LVCMOS	Clock signal input
4	CCLK1	Input	LVCMOS	Alternative clock signal input
2	CLK_SEL	Input	LVCMOS	Clock input select
5	$\overline{\text{CLK\_STOP}}$	Input	LVCMOS	Clock output enable/disable
6	OE	Input	LVCMOS	Output enable/disable (high–impedance tristate)
11,13,15,19,21,23,26,28,30	Q0 – Q8	Output	LVCMOS	Clock outputs
1,8,9,12,16,17,20,24,25,29,32	GND	Supply	Ground	Negative power supply (GND) for Output and Core
7,10,14,18,22,27,31	V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		V_{CC} ÷2		V	
MM	ESD protection (Machine model)	200			V	
HBM	ESD protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C_{PD}	Power dissipation capacitance		10		pF	Per output
C_{IN}	Input capacitance		4.0		pF	Inputs

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-65	125	°C	

Note: 1.These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Table 5. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	-0.3		0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance		17		W	
I_{IN}	Input Current[2]			±300	mA	V_{IN} = V_{CC} or GND
I_{CCQ}	Maximum Quiescent Supply Current[3]			2.0	mA	All V_{CC} Pins

Note: 1. The PCS2I99447 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines (for V_{CC}=3.3V).
2. Inputs have pull-down or pull-up resistors affecting the input current.
3. ICCQ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 6. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C)[1]

Symbol	5Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		350	MHz	
f_{max}	Output Frequency	0		350	MHz	
$f_{P,REF}$	Reference Input Pulse Width	1.4			nS	
t_r, t_f	CCLK0, CCLK1 Input Rise/Fall Time			1.0[2]	nS	0.8 to 2.0V
$t_{PLH/HL}$	Propagation Delay CCLK0 or CCLK1 to any Q	1.3		3.3	nS	
$t_{PLZ,\ HZ}$	Output Disable Time			11	nS	
$t_{PZL,\ ZH}$	Output Enable Time			11	nS	
t_S	Setup Time CCLK0 or CCLK1 to $\overline{\text{CLK\_STOP}}$[3]	0.0			nS	
t_H	Hold Time CCLK0 or CCLK1 to $\overline{\text{CLK\_STOP}}$[3]	1.0			nS	
$t_{sk(O)}$	Output-to-Output Skew			150	pS	
$t_{sk(PP)}$	Device-to-Device Skew			2.0	nS	
$t_{SK(P)}$ DCQ	Output Pulse Skew[4] Output Duty Cycle fQ<170 MHz	45	50	300 55	pS %	DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time	0.1		1.0	nS	0.55 to 2.4V
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1σ)		TBD		pS	

Note: 1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. Violation of the 1.0 nS maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
3. Setup and hold times are referenced to the falling edge of the selected clock signal input.
4. Output pulse skew is the absolute difference of the propagation delay times: | t_{PLH} - t_{PHL} |.

Table 7. DC Characteristics (V_{CC} = 2.5V ± 5%, TA = -40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	-0.3		0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH} =-15 mA[1]
V_{OL}	Output Low Voltage			0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output Impedance		19		Ω	
I_{IN}	Input Current[2]			±300	mA	V_{IN} = V_{CC} or GND
I_{CCQ}	Maximum Quiescent Supply Current[3]			2.0	mA	All V_{CC} Pins

Note: 1.The PCS2I99447 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives one 50Ω series terminated transmission lines per output (V_{CC}=2.5V).
2. Inputs have pull-down or pull-up resistors affecting the input current.
3. ICCQ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 8. AC Characteristics (V_{CC} = 2.5V ± 5%, TA = -40°C to +85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		350	MHz	
f_{max}	Output frequency	0		350	MHz	
$f_{P,REF}$	Reference Input Pulse Width	1.4			nS	
t_r, t_f	CCLK0, CCLK1 Input Rise/Fall Time			1.0[2]	nS	0.7 to 1.7V
$t_{PLH/HL}$	Propagation Delay CCLK0 or CCLK1 to any Q	1.7		4.4	nS	
$t_{PLZ, HZ}$	Output Disable Time			11	nS	
$t_{PZL, ZH}$	Output Enable Time			11	nS	
t_S	Setup Time CCLK0 or CCLK1 to $\overline{CLK\_STOP}$[3]	0.0			nS	
t_H	Hold Time CCLK0 or CCLK1 to $\overline{CLK\_STOP}$[3]	1.0			nS	
$t_{sk(O)}$	Output-to-Output Skew			150	pS	
$t_{sk(PP)}$	Device-to-Device Skew			2.7	nS	
$t_{SK(P)}$ DC_Q	Output Pulse Skew[4] Output Duty Cycle f_Q<350 MHz	 45	 50	200 55	pS %	 DC_{REF}=50%
t_r, t_f	Output Rise/Fall Time	0.1		1.0	nS	0.6 to 1.8V
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ)		TBD		pS	

Note: 1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. Violation of the 1.0 nS maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
3. Setup and hold times are referenced to the falling edge of the selected clock signal input.
4. Output pulse skew is the absolute difference of the propagation delay times: | t_{PLH} - t_{PHL} |.

APPLICATIONS INFORMATION

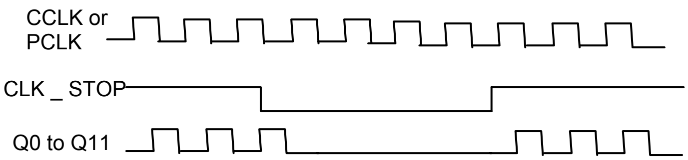


Figure 1. Output Clock Stop (CLK_STOP) Timing Diagram

Driving Transmission Lines

The PCS2I99447 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of 17Ω (V_{CC}=3.3V), the outputs can drive either parallel or series terminated transmission lines. In most high performance clock networks, point–to–point distribution of signals is the method of choice. In a point–to–point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC÷2.

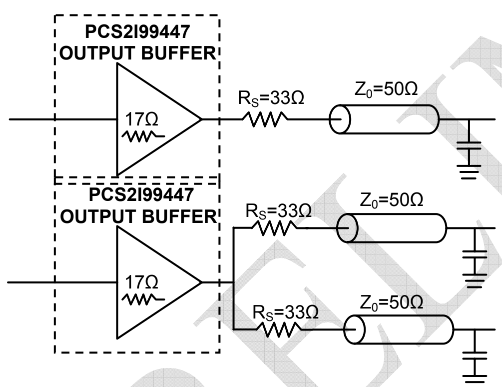


Figure 2. Single versus Dual Transmission Lines

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the PCS2I99447 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 2 "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the PCS2I99447 clock driver is effectively doubled due to its capability to drive multiple lines at V_{CC}=3.3V.

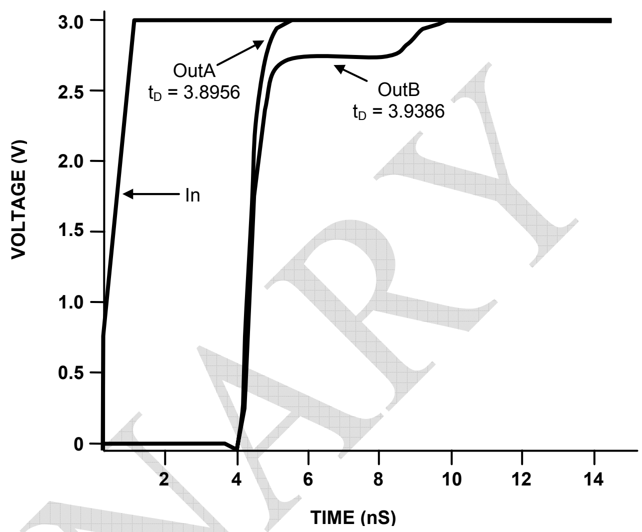
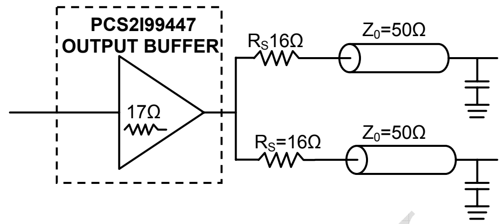


Figure 3. Single versus Dual Line Termination Waveforms

The waveform plots in Figure 3 "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the PCS2I99447 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43pS exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the PCS2I99447. The output waveform in Figure 3 "Single versus Dual Line Termination Waveforms" shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 33Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S\,(Z_0 \mid (R_S+R_0+Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 33\Omega \parallel 33\Omega$$
$$R_0 = 17\Omega$$
$$V_L = 3.0\,(25 \div (16.5+17+25))$$
$$= 1.28V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns). Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 4 "Optimized Dual Line Termination" should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



17Ω + 16Ω ‖ 16Ω = 50Ω ‖ 50Ω
25Ω = 25Ω

Figure 4. Optimized Dual Line Termination

The Following Figures Illustrate the Measurement Reference for the PCS2I99447 Clock Driver Circuit

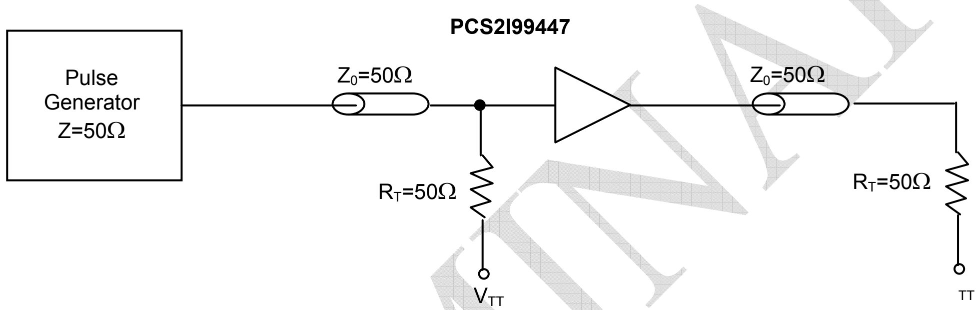


Figure 5. CCLK PCS2I99447 AC Test Reference for Vcc = 3.3V and Vcc = 2.5V

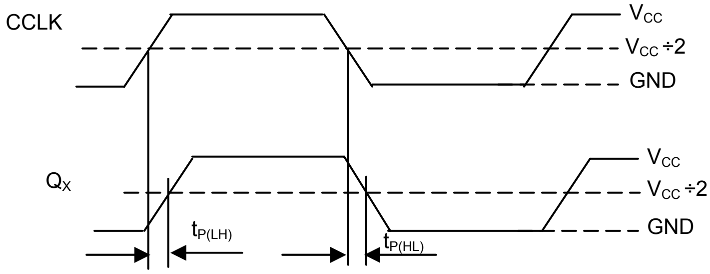
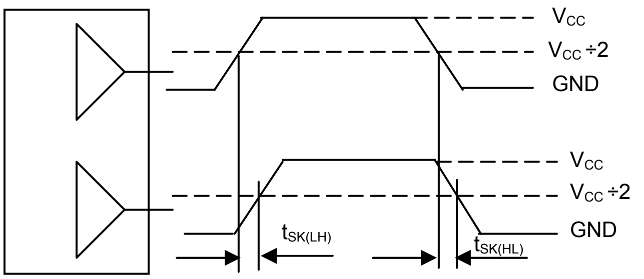


Figure 6. Propagation Delay (t_{PD}) Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation between any similar delay path within a single device

Figure 7. Output–to–Output Skew $t_{SK(LH, HL)}$

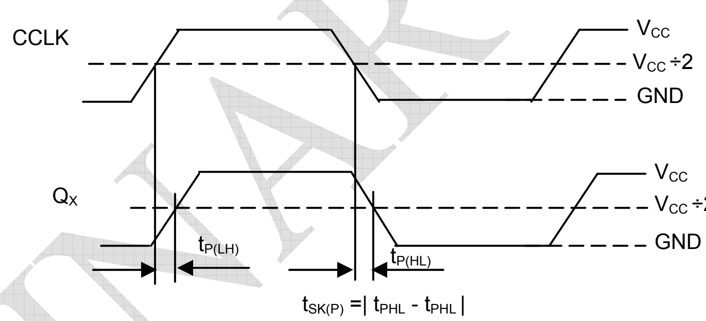
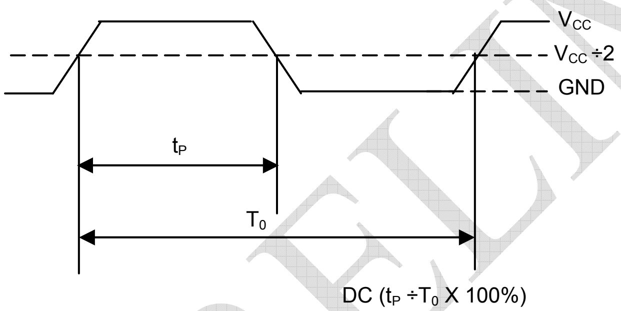
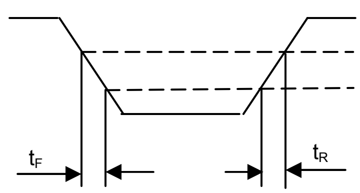


Figure 8. Output Pulse Skew ($t_{SK(P)}$) Test



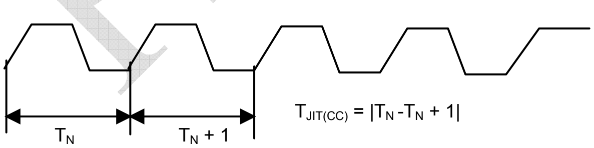
The time from the output controlled edge to the non-controlled edge, divided by the time output controlled edge, expressed as a percentage.

Figure 9. Output Duty Cycle (DC)



V_{CC} = 3.3V	V_{CC} = 2.5V
2.4 0.5	1.8V 0.6V

Figure 10. Output Transition Time Test Reference



The variation in cycle time of a single between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 11. Cycle–to–Cycle Jitter Reference

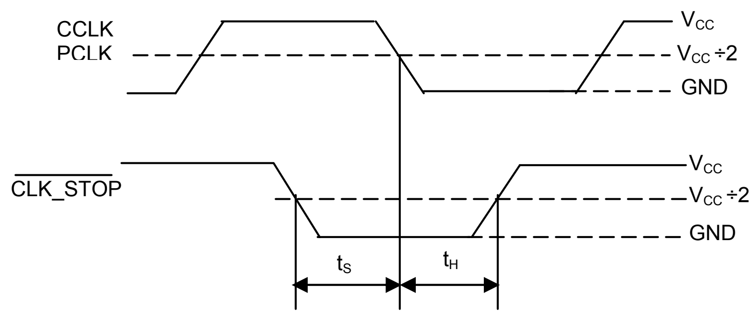


Figure 12. Setup and Hold Time (t_S, t_H) Test Reference

Power Consumption of the PCS2I99447 and Thermal Management

The PCS2I99447 AC specification is guaranteed for the entire operating frequency range up to 350MHz. The PCS2I99447 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the PCS2I99447 die junction temperature and the associated device reliability.

Table 9. Die junction temperature and MTBF

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the PCS2I99447 needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the PCS2I99447 is represented in equation 1.Where I_{CCQ} is the static current consumption of the PCS2I99447, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 12 in case of the PCS2I99447). The PCS2I99447 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL}, I_{OL}, V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

Where Rthja is the thermal impedance of the package (junction to ambient) and TA is the ambient temperature. According to Table 9, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the PCS2I99447 in a series terminated transmission line system, equation 4

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] \cdot V_{CC} \qquad \textit{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_M C_L \right) \right] + \sum_P \left[DC_Q \cdot I_{OH} (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \qquad \textit{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \qquad \textit{Equation 3}$$

$$f_{CLOCKMAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{JMAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \qquad \textit{Equation 4}$$

T_J,MAX should be selected according to the MTBF system requirements and Table 9. R_{thja} can be derived from Table 10. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

Table 10. Thermal package impedance of the 32LQFP

Convection, LFPM	R_{thja} (1P2S board), °C/W	R_{thja} (2P2S board), °C/W
Still air	86	61
100 lfpm	76	56
200 lfpm	71	54
300 lfpm	68	53
400 lfpm	66	52

If the calculated maximum frequency is below 350 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the PCS2I99447. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to an estimated MTBF of 9.1 years (4 years), a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.

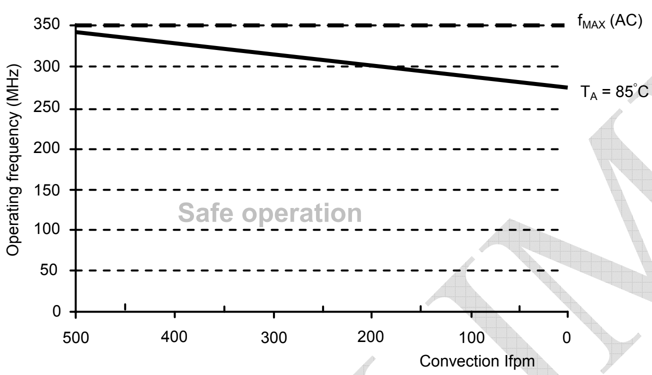


Figure 13. Maximum PCS2I99447 frequency V_{CC} = 3.3V, MTBF 9.1 years, driving series terminated transmission lines, 2s2p board

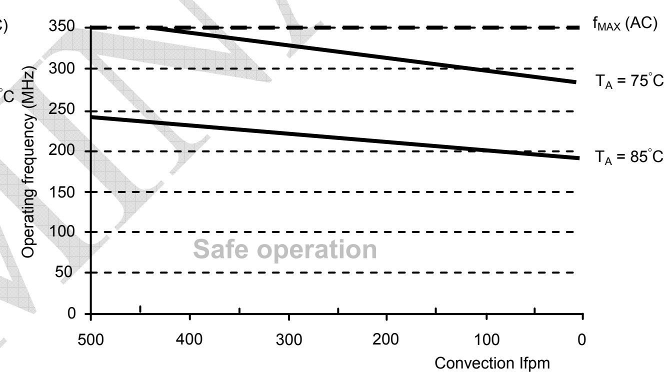


Figure 14. Maximum PCS2I99447 frequency V_{CC} = 3.3V, MRBF 9.1 years, 4pF load per line, 2s2p board

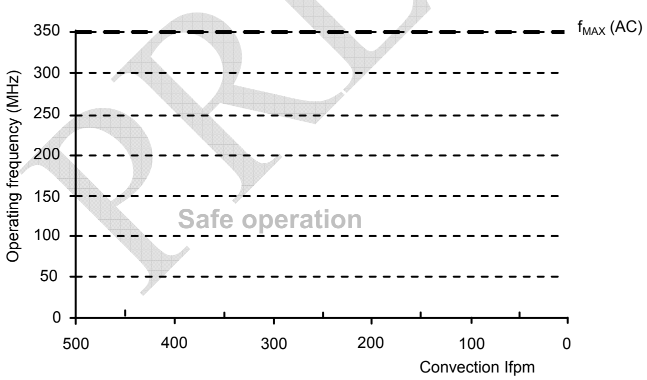


Figure 15. No maximum frequency limitation for V_{CC} = 3.3V, MTBF 4 years, driving series terminated transmission lines, 2s2p board

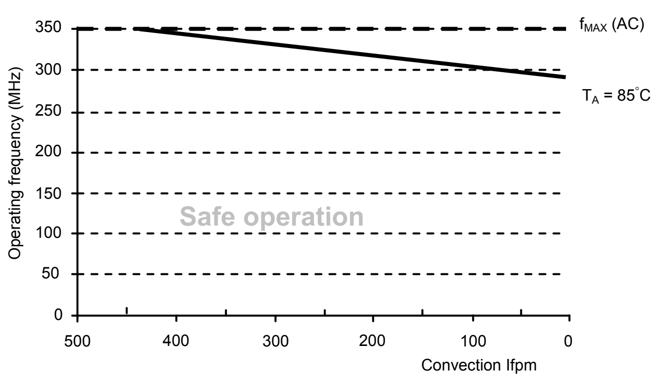
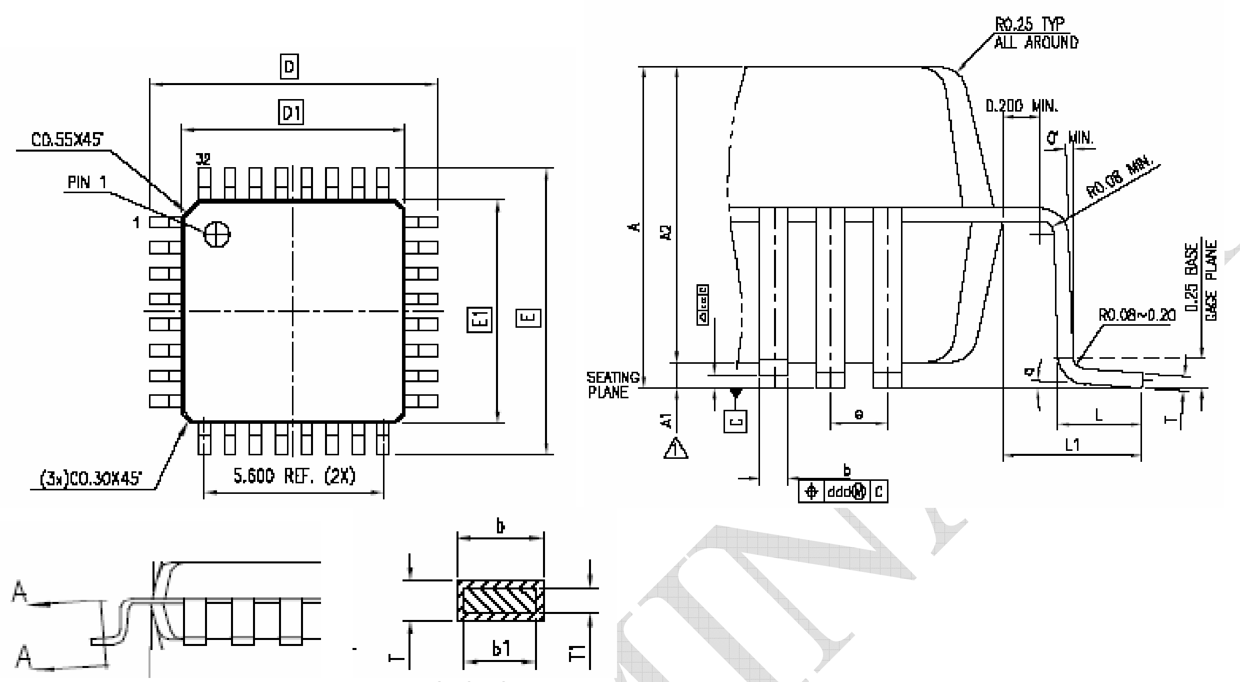


Figure 16. Maximum PCS2I99447 frequency V_{CC} = 3.3V, MRBF 4 years, 4pF load per line, 2s2p board

Package Information

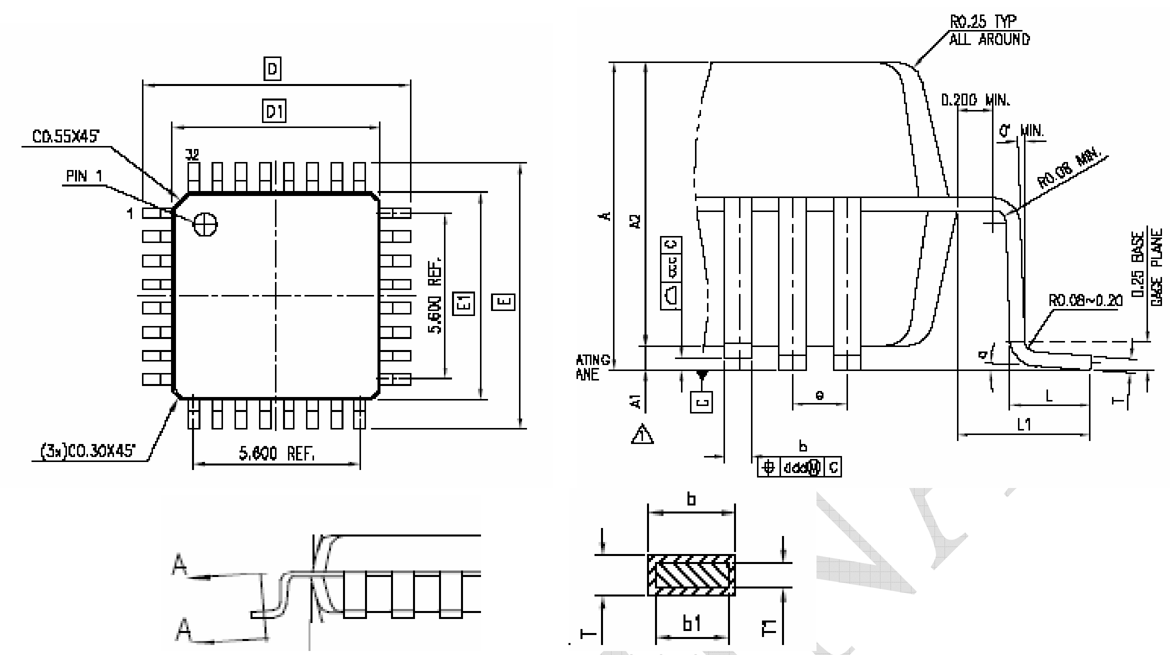
32-lead TQFP



SECTION A-A

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.0472	…	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.0374	0.0413	0.95	1.05
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.2
a	0°	7°	0°	7°
e	0.031 BASE		0.8 BASE	

32-lead LQFP



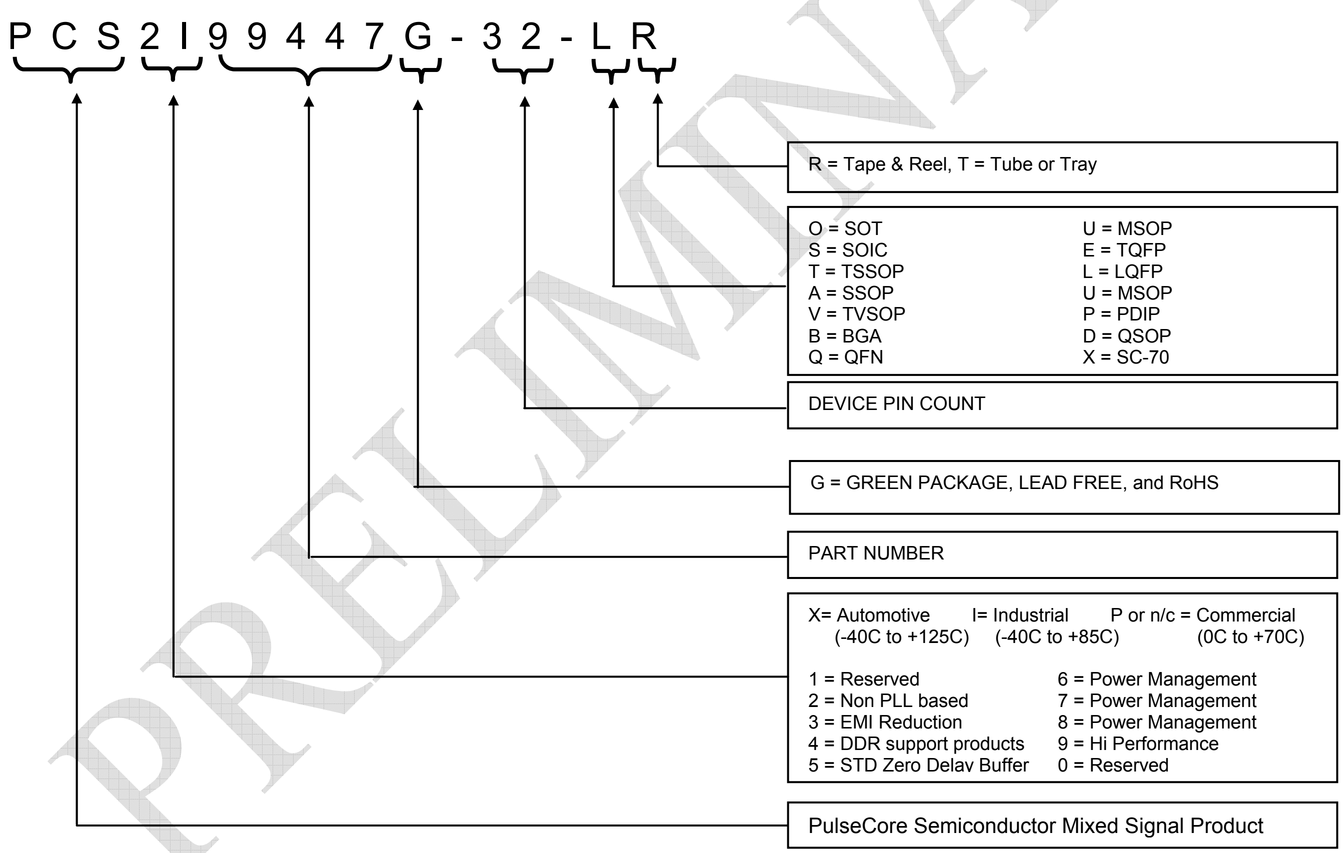
SECTION A-A

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.0630	…	1.6
A1	0.0020	0.0059	0.05	0.15
A2	0.0531	0.0571	1.35	1.45
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.20
e	0.031 BASE		0.8 BASE	
a	0°	7°	0°	7°

Ordering Information

Part Number	Marking	Package Type	Operating Range
PCS2P99447G-32-LT	PCS2P99447GL	32-pin LQFP, Tray, Green	Commercial
PCS2P99447G-32-LR	PCS2P99447GL	32-pin LQFP, Tape and Reel, Green	Commercial
PCS2P99447G-32-ET	PCS2P99447GE	32-pin TQFP, Tray, Green	Commercial
PCS2P99447G-32-ER	PCS2P99447GE	32-pin TQFP, Tape and Reel, Green	Commercial
PCS2I99447G-32-LT	PCS2I99447GL	32-pin LQFP, Tray, Green	Industrial
PCS2I99447G-32-LR	PCS2I99447GL	32-pin LQFP, Tape and Reel, Green	Industrial
PCS2I99447G-32-ET	PCS2I99447GE	32-pin TQFP, Tray, Green	Industrial
PCS2I99447G-32-ER	PCS2I99447GE	32-pin TQFP, Tape and Reel, Green	Industrial

Device Ordering Information



Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

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Preliminary Information
Part Number: PCS2I99447
Document Version: 0.4

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003