

## 2.5V and 3.3V LVCMOS Clock Distribution Buffer

### Features

- Configurable 10 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3V/2.5V Voltage supply
- Wide range output clock frequency up to 250MHz
- Designed for mid-range to high-performance telecom, networking and computer applications
- Supports applications requiring clock redundancy
- Max. output skew of 200pS (150pS within one bank)
- Selectable output configurations per output bank
- Tristatable outputs
- 32 lead LQFP & TQFP Packages
- Pin and Function compatible with MPC9446
- Ambient operating temperature range of -40 to 85°C

### Functional Description

The PCS2I99446 is a 2.5V and 3.3V compatible 1:10 clock distribution buffer designed for low-voltage mid-range to high-performance telecom, networking and computing applications. Both 3.3V, 2.5V and dual supply voltages are supported for mixed-voltage applications. The PCS2I99446 offers 10 low-skew outputs and 2 selectable inputs for clock redundancy. The outputs are configurable and support 1:1 and 1:2 output to input frequency ratios. The PCS2I99446

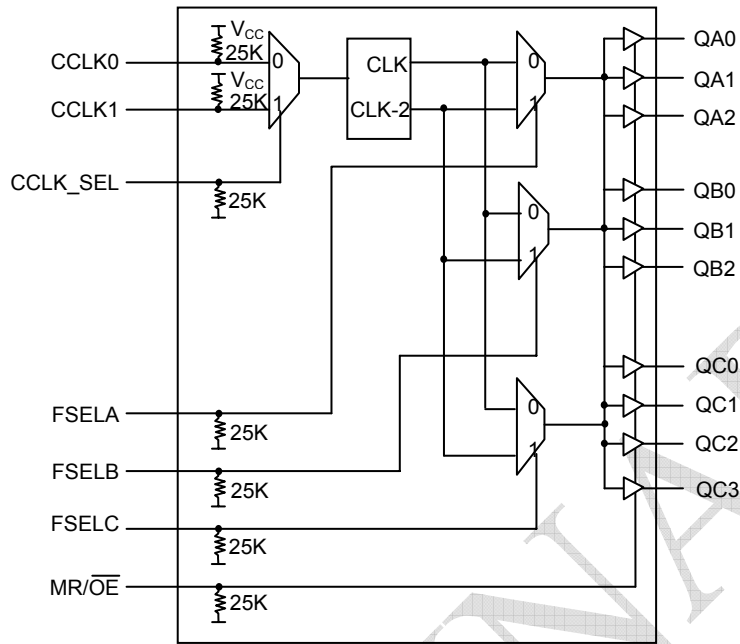
is specified for the extended temperature range of -40°C to 85°C.

The PCS2I99446 is a full static fanout buffer design supporting clock frequencies up to 250MHz. The signals are generated and retimed on-chip to ensure minimal skew between the three output banks. Two independent LVCMOS compatible clock inputs are available. This feature supports redundant clock sources or the addition of a test clock into the system design. Each of the three output banks can be individually supplied by 2.5V or 3.3V supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the three output banks. The PCS2I99446 can be reset and the outputs are disabled by deasserting the MR/ $\overline{OE}$  pin (logic high state). Asserting MR/ $\overline{OE}$  will enable the outputs.

All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 $\Omega$  transmission lines. Please consult the PCS2I99456 specification for a 1:10 mixed voltage buffer with LVPECL compatible inputs. For series terminated transmission lines, each of the PCS2I99446 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a 7x7mm<sup>2</sup> 32-lead LQFP and TQFP Packages.

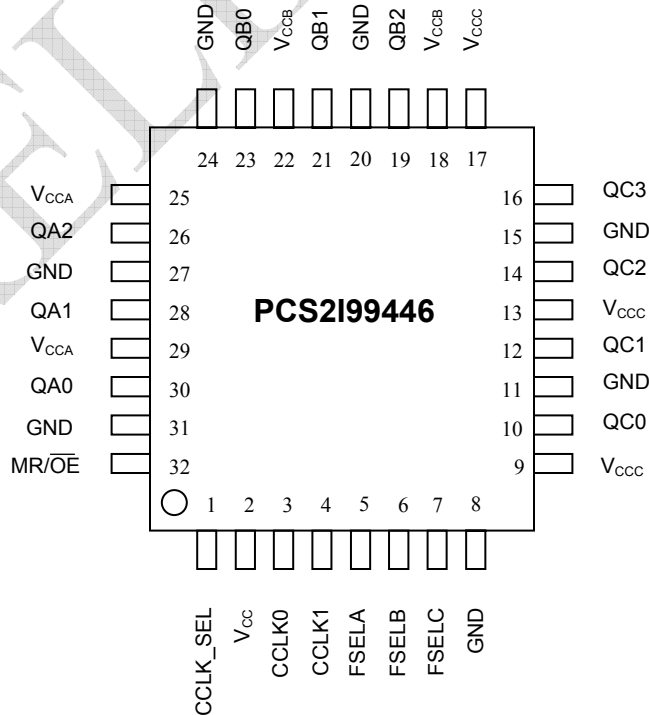
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Block Diagram



Pin Configuration

32 – LEAD PACKAGE PINOUT -- Top View



**Table 1: Pin Configuration**

Pin Number	Pin	I/O	Type	Function
3,4	CCLK0, CCLK1	Input	LVC MOS	LVC MOS clock inputs
5,6,7	FSELA, FSELB, FSELC	Input	LVC MOS	Output bank divide select input
32	MR/ $\overline{OE}$	Input	LVC MOS	Internal reset and output (high impedance) control
8,11,15,20,24,27,31	GND		Supply	Negative voltage supply (GND)
25,29 18,22 9,13,17	V <sub>CCA</sub> , V <sub>CCB</sub> , V <sub>CCC</sub>		Supply	Positive voltage supply for output banks
2	V <sub>CC</sub>		Supply	Positive voltage supply for core (V <sub>CC</sub> )
30,28, 26	QA0 - QA2	Output	LVC MOS	Bank A outputs
23,21,19	QB0 - QB2	Output	LVC MOS	Bank B outputs
10,12,14,16	QC0 - QC3	Output	LVC MOS	Bank C outputs

Note: V<sub>CCB</sub> is internally connected to V<sub>CC</sub>.

**Table 2: Supported Single and Dual Supply Configurations**

Supply voltage configuration	V <sub>CC</sub> <sup>1</sup>	V <sub>CCA</sub> <sup>2</sup>	V <sub>CCB</sub> <sup>3</sup>	V <sub>CCC</sub> <sup>4</sup>	GND
3.3V	3.3V	3.3V	3.3V	3.3V	0V
Mixed voltage supply	3.3V	3.3V or 2.5V	3.3V	3.3V or 2.5V	0 V
2.5V	2.5V	2.5V	2.5V	2.5V	0 V

Note: 1 V<sub>CC</sub> is the positive power supply of the device core and input circuitry. V<sub>CC</sub> voltage defines the input threshold and levels

2 V<sub>CCA</sub> is the positive power supply of the bank A outputs. V<sub>CCA</sub> voltage defines bank A output levels

3 V<sub>CCB</sub> is the positive power supply of the bank B outputs. V<sub>CCB</sub> voltage defines bank B output levels. V<sub>CCB</sub> is internally connected to V<sub>CC</sub>.

4 V<sub>CCC</sub> is the positive power supply of the bank C outputs. V<sub>CCC</sub> voltage defines bank C output levels.

**Table 3: Function Table (Controls)**

Control	Default	0	1
CCLK_SEL	0	CCLK0	CCLK1
FSELA	0	f <sub>QA0:2</sub> = f <sub>REF</sub>	f <sub>QA0:2</sub> = f <sub>REF</sub> ÷ 2
FSELB	0	f <sub>QB0:2</sub> = f <sub>REF</sub>	f <sub>QB0:2</sub> = f <sub>REF</sub> ÷ 2
FSELC	0	f <sub>QC0:3</sub> = f <sub>REF</sub>	f <sub>QC0:3</sub> = f <sub>REF</sub> ÷ 2
MR/OE	0	Outputs enabled	Internal reset Outputs disabled (tristate)

**Table 4: Absolute Maximum Ratings<sup>1</sup>**

Symbol	Characteristics	Min	Max	Unit	Condition
V <sub>CC</sub>	Supply Voltage	-0.3	3.6	V	
V <sub>IN</sub>	DC Input Voltage	-0.3	V <sub>CC</sub> +0.3	V	
V <sub>OUT</sub>	DC Output Voltage	-0.3	V <sub>CC</sub> +0.3	V	
I <sub>IN</sub>	DC Input Current		±20	mA	
I <sub>OUT</sub>	DC Output Current		±50	mA	
T <sub>S</sub>	Storage temperature	-65	125	°C	

Note: 1 These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

**Table 5: General Specifications**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V <sub>TT</sub>	Output Termination Voltage		V <sub>CC</sub> ±2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C <sub>PD</sub>	Power Dissipation Capacitance		10		pF	Per output
C <sub>IN</sub>	Input Capacitance		4.0		pF	

**Table 6: DC CHARACTERISTICS** (V<sub>CC</sub> = V<sub>CCA</sub> = V<sub>CCB</sub> = V<sub>CC3</sub> = 3.3V ±5%, T<sub>A</sub> = -40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V <sub>IH</sub>	Input High Voltage	2.0		V <sub>CC</sub> + 0.3	V	LVC MOS
V <sub>IL</sub>	Input Low Voltage	-0.3		0.8	V	LVC MOS
I <sub>IN</sub>	Input Current <sup>1</sup>			200	µA	V <sub>IN</sub> =GND or V <sub>IN</sub> =V <sub>CC</sub>
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> =-24 mA <sup>2</sup>
V <sub>OL</sub>	Output Low Voltage			0.55 0.30	V V	I <sub>OL</sub> = 24mA <sup>3</sup> I <sub>OL</sub> = 12mA
Z <sub>OUT</sub>	Output Impedance		14 - 17		Ω	
I <sub>CCQ</sub> <sup>3</sup>	Maximum Quiescent Supply Current			2.0	mA	All V <sub>CC</sub> Pins

Note: 1 Input pull-up / pull-down resistors influence input current.

2 The PCS2I99446 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V<sub>TT</sub>. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

3 I<sub>CCQ</sub> is the DC current consumption of the device with all outputs open and the input in its default state or open.

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**Table 7: AC CHARACTERISTICS** ( $V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )<sup>1</sup>

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
$f_{ref}$	Input Frequency		0		250 <sup>2</sup>	MHz	
$f_{MAX}$	Maximum Output Frequency	±1 output	0		250 <sup>2</sup>	MHz	FSELx=0
		±2 output	0		125	MHz	FSELx=1
$t_{P, REF}$	Reference Input Pulse Width		1.4			nS	
$t_r, t_f$	CCLK Input Rise/Fall Time				1.0 <sup>3</sup>	nS	0.8 to 2.0V
$t_{PLH}$	Propagation delay	CCLK0,1 to any Q	2.2	2.8	4.45	nS	
$t_{PHL}$		CCLK0,1 to any Q	2.2	2.8	4.2	nS	
$t_{PLZ, HZ}$	Output Disable Time				10	nS	
$t_{PZL, LZ}$	Output Enable Time				10	nS	
$t_{sk(O)}$	Output-to-output Skew	Within one bank			150	pS	
		Any output Bank, Same output divider			200	pS	
		Any output, Any output divider			350	pS	
$t_{sk(PP)}$	Device-to-device Skew				2.25	nS	
$t_{SK(P)}$	Output pulse skew <sup>4</sup>				200	pS	
DC <sub>Q</sub>	Output Duty Cycle	±1 output	47	50	53	%	DC <sub>REF</sub> = 50%
		±2 output	45	50	55	%	DC <sub>REF</sub> = 25%-75%
$t_r, t_f$	Output Rise/Fall Time		0.1		1.0	nS	0.55 to 2.4V

Note: 1 AC characteristics apply for parallel output termination of 50Ω to V<sub>TT</sub>

2 The PCS2I99446 is functional up to an input and output clock frequency of 350MHz and is characterized up to 250MHz.

3 Violation of the 1.0nS maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.

4 Output pulse skew is the absolute difference of the propagation delay times |  $t_{PLH} - t_{PHL}$  |.

**Table 8: DC CHARACTERISTICS** ( $V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V <sub>IH</sub>	Input High Voltage	1.7		V <sub>CC</sub> + 0.3	V	LVC MOS
V <sub>IL</sub>	Input Low Voltage	-0.3		0.7	V	LVC MOS
V <sub>OH</sub>	Output High Voltage	1.8			V	I <sub>OH</sub> =-15 mA <sup>1</sup>
V <sub>OL</sub>	Output Low Voltage			0.6	V	I <sub>OL</sub> = 15 mA
Z <sub>OUT</sub>	Output Impedance		17 - 20 <sup>2</sup>		Ω	
I <sub>IN</sub>	Input Current <sup>2</sup>			±200	μA	V <sub>IN</sub> =GND or V <sub>IN</sub> =V <sub>CC</sub>
I <sub>CCQ</sub> <sup>3</sup>	Maximum Quiescent Supply Current			2.0	mA	All V <sub>CC</sub> Pins

Note: 1 The PCS2I99446 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V<sub>TT</sub>. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

2 Input pull-up / pull-down resistors influence input current.

3 I<sub>CCQ</sub> is the DC current consumption of the device with all outputs open and the input in its default state or open.

**Table 9: AC CHARACTERISTICS** ( $V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )<sup>1,2</sup>

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
$f_{ref}$	Input Frequency		0		250 <sup>3</sup>	MHz	
$f_{MAX}$	Maximum Output Frequency	$\pm 1$ output	0		250 <sup>2</sup>	MHz	FSELx=0
		$\pm 2$ output	0		125	MHz	FSELx=1
$t_{P, REF}$	Reference Input Pulse Width		1.4			nS	
$t_r, t_f$	CCLK Input Rise/Fall Time				1.0 <sup>4</sup>	nS	0.7 to 1.7V
$t_{PLH}$ $t_{PHL}$	Propagation delay	CCLK0,1 to any Q	2.6		5.6	nS	
		CCLK0,1 to any Q	2.6		5.5	nS	
$t_{PLZ, HZ}$	Output Disable Time				10	nS	
$t_{PZL, LZ}$	Output Enable Time				10	nS	
$t_{sk(O)}$	Output-to-output Skew	Within one bank			150	pS	
		Any output Bank, Same output divider			200	pS	
		Any output, Any output divider			350	pS	
$t_{sk(PP)}$	Device-to-device Skew				3.0	nS	
$t_{sk(P)}$	Output pulse skew <sup>5</sup>				200	pS	
DC <sub>Q</sub>	Output Duty Cycle	$\pm 1$ or $\pm 2$ output	45	50	55	%	DC <sub>REF</sub> = 50%
$t_r, t_f$	Output Rise/Fall Time		0.1		1.0	nS	0.6 to 1.8V

Note: 1 AC characteristics apply for parallel output termination of 50Ω to V<sub>TT</sub>.

2 AC specifications are design targets, final specification is pending device characterization.

3 The PCS2I99446 is functional up to an input and output clock frequency of 350MHz and is characterized up to 250MHz.

4 Violation of the 1.0nS maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.

5 Output pulse skew is the absolute difference of the propagation delay times:  $|t_{pLH} - t_{pHL}|$ .

**Table 10: AC CHARACTERISTICS** ( $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCA}, V_{CCB}, V_{CCC} = 2.5V \pm 5\%$  or  $3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )<sup>1,2</sup>

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
$t_{sk(O)}$	Output-to-output Skew	Within one bank			150	pS	
		Any output Bank, Same output divider			250	pS	
		Any output, Any output divider			350	pS	
$t_{sk(PP)}$	Device-to-device Skew				2.5	nS	
$t_{PLH, HL}$	Propagation delay	CCLK0,1 to any Q		See 3.3V table			
$t_{sk(P)}$	Output pulse skew <sup>3</sup>				250	pS	
DC <sub>Q</sub>	Output Duty Cycle	$\pm 1$ or $\pm 2$ output	45	50	55	%	DC <sub>REF</sub> = 50%

Note: 1 AC characteristics apply for parallel output termination of 50Ω to V<sub>TT</sub>.

2 For all other AC specifications, refer to 2.5V or 3.3V tables according to the supply voltage of the output bank.

3 Output pulse skew is the absolute difference of the propagation delay times:  $|t_{pLH} - t_{pHL}|$ .

APPLICATIONS INFORMATION

Driving Transmission Lines

The PCS2I99446 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to  $V_{CC}+2$ .

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the PCS2I99446 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 1. "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the PCS2I99446 clock driver is effectively doubled due to its capability to drive multiple lines.

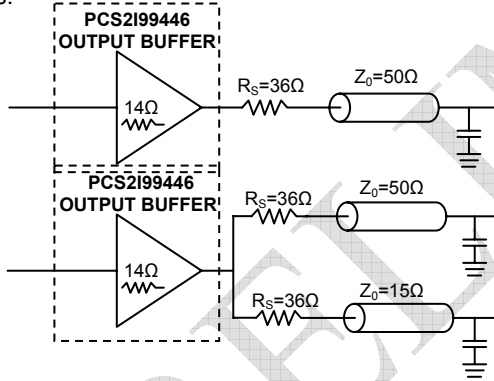


Figure 1. Single versus Dual Transmission Lines

The waveform plots in Figure 2. "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the PCS2I99446 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43pS exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the PCS2I99446. The output waveform in Figure 2 "Single versus Dual Line Termination Waveforms" shows a step in the waveform. This step is caused by the

impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S ( Z_0 \div (R_S + R_0 + Z_0))$$

$$Z_0 = 50\Omega \parallel 50\Omega$$

$$R_S = 36\Omega \parallel 36\Omega$$

$$R_0 = 14\Omega$$

$$V_L = 3.0 ( 25 \div (18+14+25)) = 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0nS).

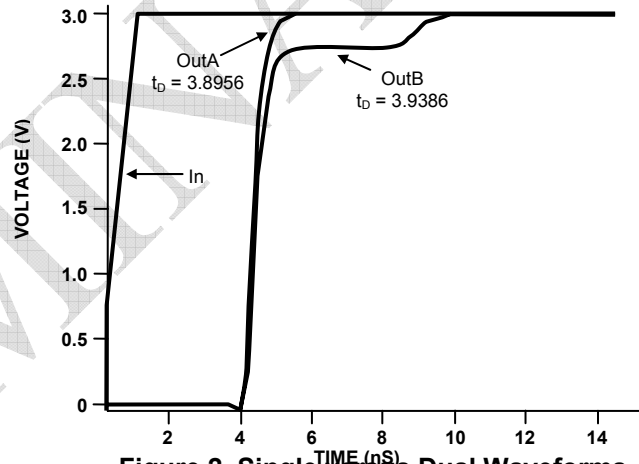


Figure 2. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 3. "Optimized Dual Line Termination" should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

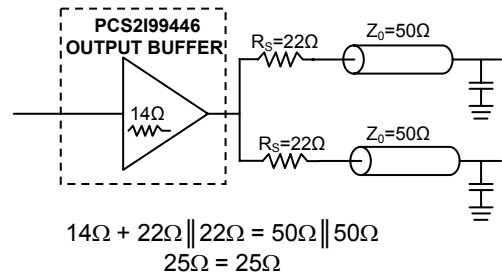


Figure 3. Optimized Dual Line Termination

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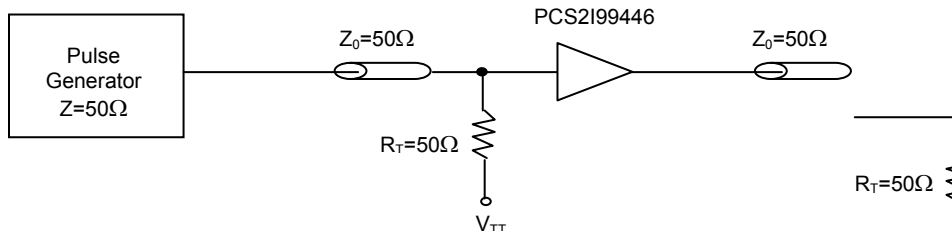


Figure 4. CCLK0, 1 PCS2I99446 AC test reference for  $V_{CC} = 3.3V$  and  $V_{CC} = 2.5V$

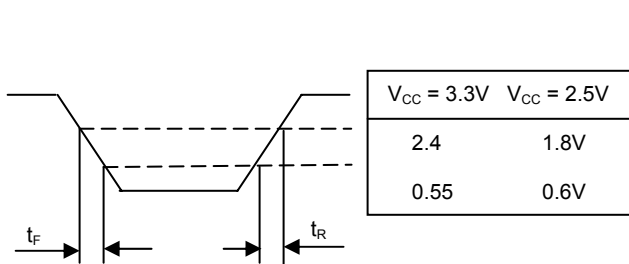


Figure 5. Output Transition Time Test Reference

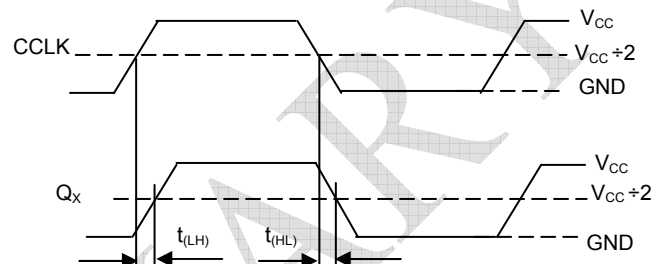
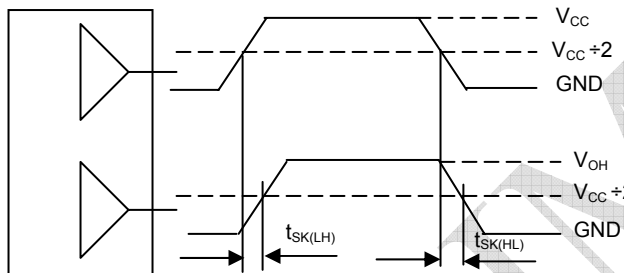


Figure 6. Propagation Delay ( $t_{PD}$ ) Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 7. Output-to-Output Skew  $t_{SK(LH,HL)}$

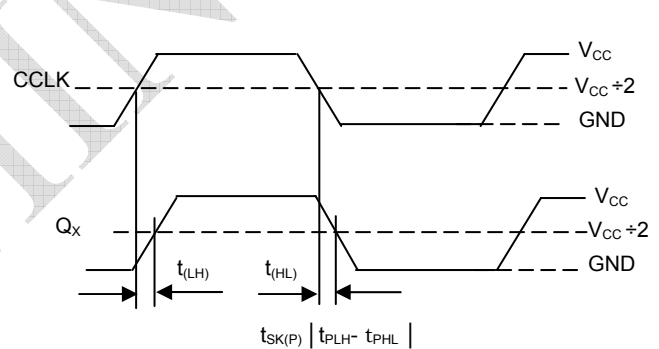
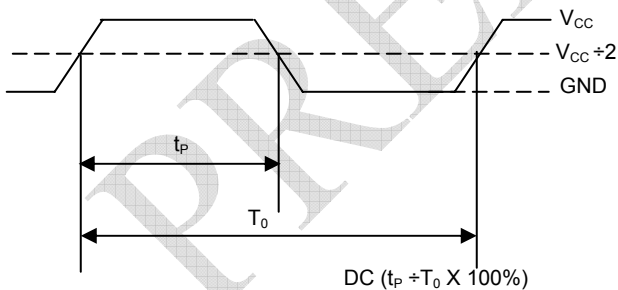
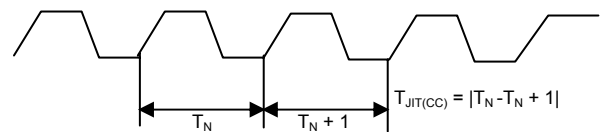


Figure 8. Propagation Delay ( $t_{SK(P)}$ ) Test Reference



The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 9. Output Duty Cycle (DC) Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 10. Cycle-to-Cycle Jitter



**Power Consumption of the PCS2199446 and Thermal Management**

The PCS2199446 AC specification is guaranteed for the entire operating frequency range up to 250MHz. The PCS2199446 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the PCS2199446 die junction temperature and the associated device reliability.

**Table 11. Die junction temperature and MTBF**

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the PCS2199446 needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the PCS2199446 is represented in equation 1.

Where  $I_{CCQ}$  is the static current consumption of the PCS2199446,  $C_{PD}$  is the power dissipation capacitance per output,  $(M)\Sigma C_L$  represents the external capacitive output load,  $N$  is the number of active outputs ( $N$  is always 12 in case of the PCS2199446). The PCS2199446 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore,  $\Sigma C_L$  is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2,  $P$  stands for the number of outputs with a parallel or thevenin termination,  $V_{OL}$ ,  $I_{OL}$ ,  $V_{OH}$  and  $I_{OH}$  are a function of the output termination technique and  $DC_Q$  is the clock signal duty cycle. If transmission lines are used  $\Sigma C_L$  is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature  $T_J$  as a function of the power consumption.

Where  $R_{thja}$  is the thermal impedance of the package (junction to ambient) and  $T_A$  is the ambient temperature. According to Table 11, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the PCS2199446 in a series terminated transmission line system, equation 4.

$$P_{TOT} = \left[ I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left( N \cdot C_{PD} + \sum_M C_L \right) \right] \cdot V_{CC} \tag{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[ I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left( N \cdot C_{PD} + \sum_M C_L \right) \right] + \sum_P \left[ DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \tag{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \tag{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[ \frac{T_{J,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \tag{Equation 4}$$

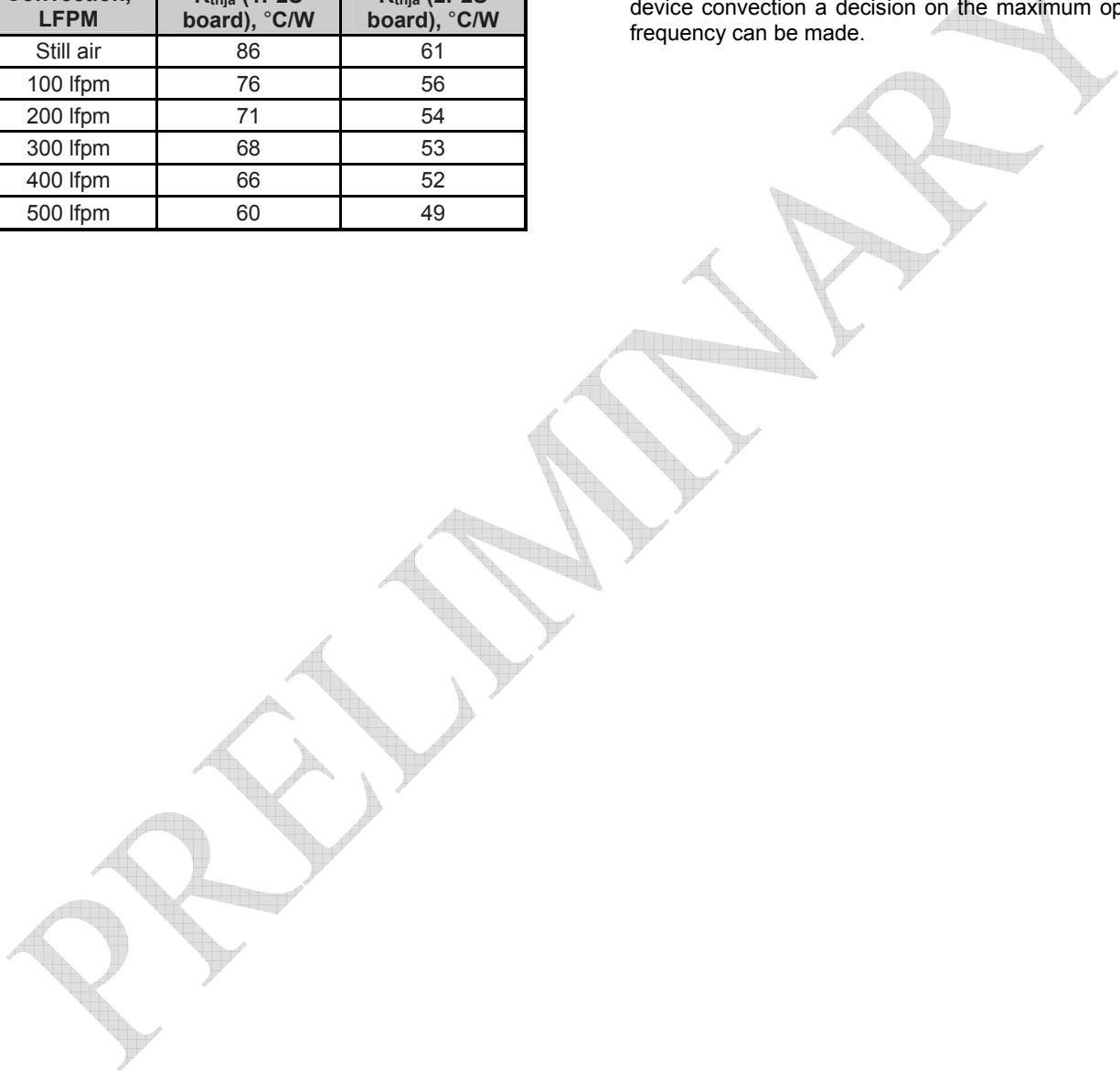
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$T_{j,MAX}$  should be selected according to the MTBF system requirements and Table 11.  $R_{thja}$  can be derived from Table 12. The  $R_{thja}$  represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

**Table 12. Thermal package impedance of the 32LQFP**

Convection, LFPM	$R_{thja}$ (1P2S board), °C/W	$R_{thja}$ (2P2S board), °C/W
Still air	86	61
100 lfpm	76	56
200 lfpm	71	54
300 lfpm	68	53
400 lfpm	66	52
500 lfpm	60	49

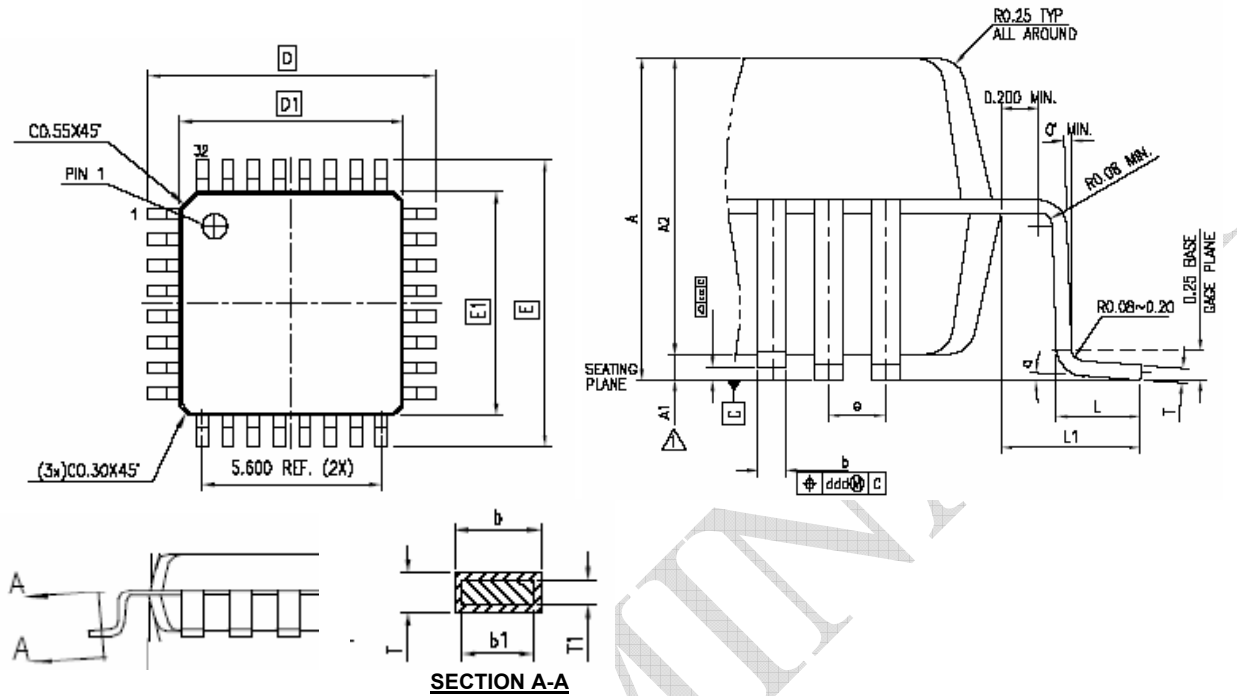
If the calculated maximum frequency is below 350 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the PCS2I99446. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to an estimated MTBF of 9.1 years (4 years), a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.



rev 0.5

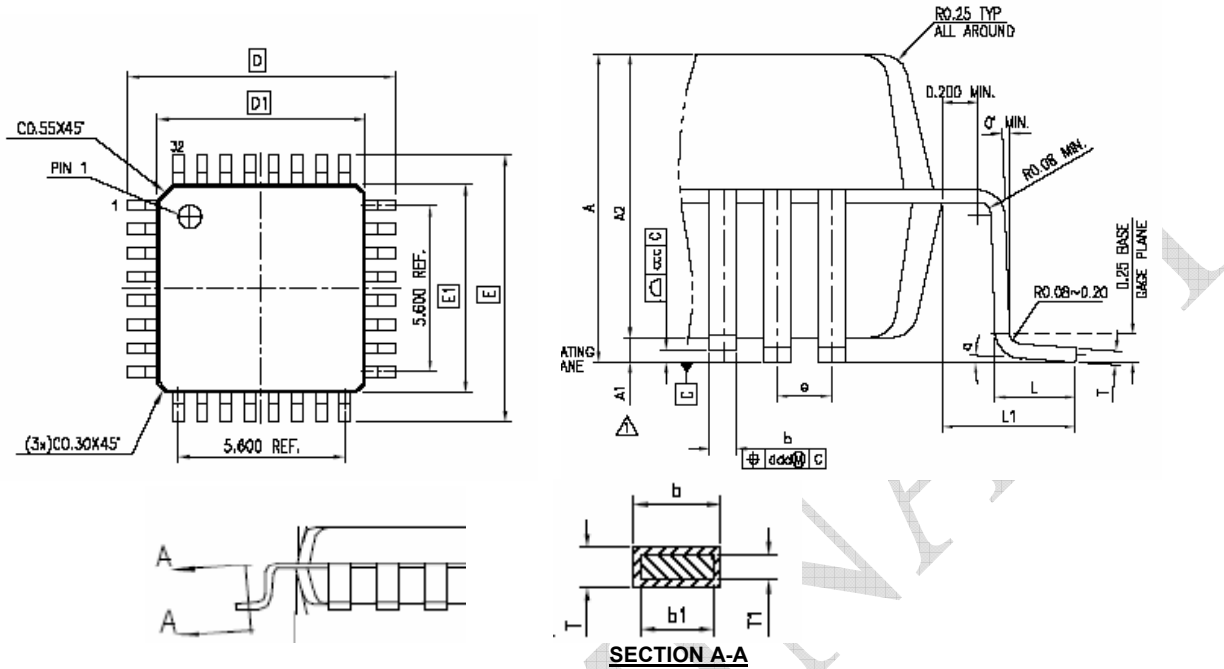
Package Information

32-lead TQFP



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	....	0.0472	...	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.0374	0.0413	0.95	1.05
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.2
a	0°	7°	0°	7°
e	0.031 BASE		0.8 BASE	

32-lead LQFP



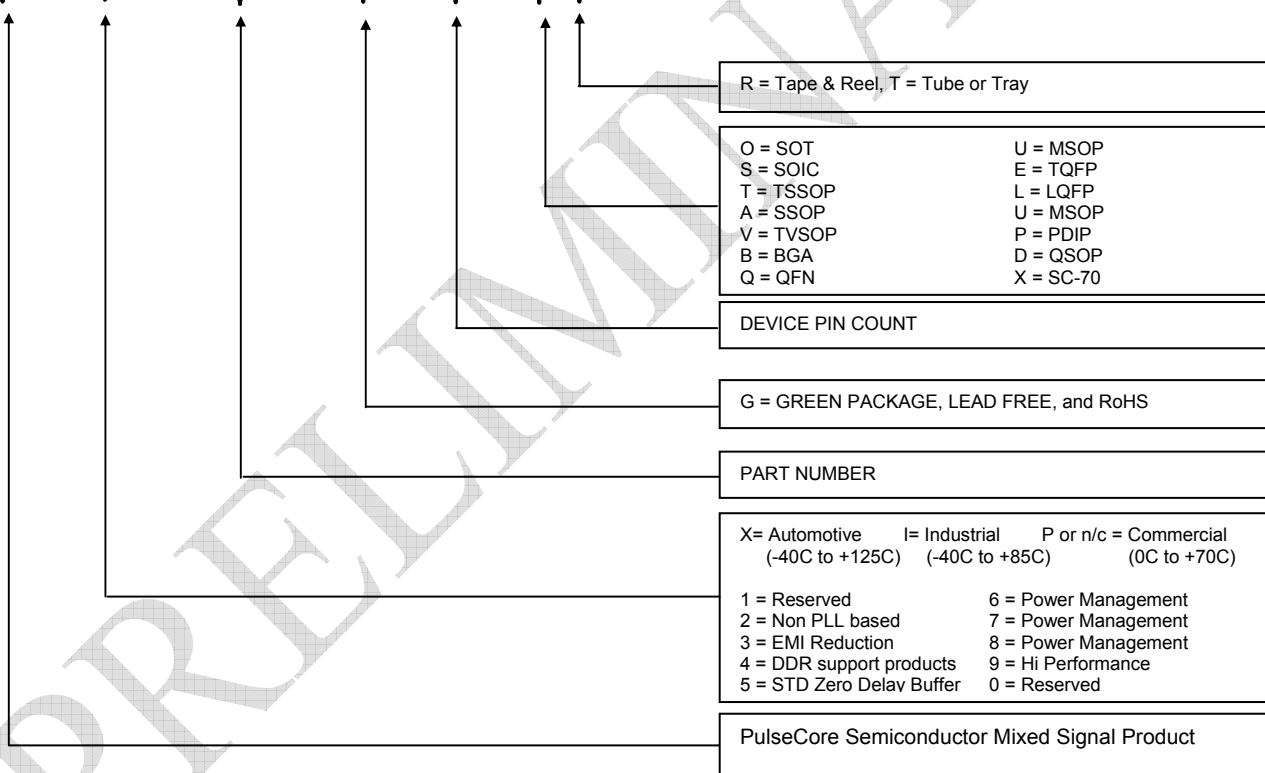
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	....	0.0630	...	1.6
A1	0.0020	0.0059	0.05	0.15
A2	0.0531	0.0571	1.35	1.45
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.20
e	0.031 BASE		0.8 BASE	
a	0°	7°	0°	7°

Ordering Information

Part Number	Marking	Package Type	Operating Range
PCS2P99446G-32-LT	PCS2P99446GL	32-pin LQFP, Tray, Green	Commercial
PCS2P99446G-32-LR	PCS2P99446GL	32-pin LQFP, Tape and Reel, Green	Commercial
PCS2P99446G-32-ET	PCS2P99446GE	32-pin TQFP, Tray, Green	Commercial
PCS2P99446G-32-ER	PCS2P99446GE	32-pin TQFP, Tape and Reel, Green	Commercial
PCS2I99446G-32-LT	PCS2I99446GL	32-pin LQFP, Tray, Green	Industrial
PCS2I99446G-32-LR	PCS2I99446GL	32-pin LQFP, Tape and Reel, Green	Industrial
PCS2I99446G-32-ET	PCS2I99446GE	32-pin TQFP, Tray, Green	Industrial
PCS2I99446G-32-ER	PCS2I99446GE	32-pin TQFP, Tape and Reel, Green	Industrial

Device Ordering Information

PCS2I99446G-32-LT





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Preliminary Information  
Part Number: PCS2I99446  
Document Version: 0.5

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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