ST-NXP Wireless

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ST-NXP Wireless

ISP1512A

ULPI Hi-Speed USB transceiver

Rev. 01 — 31 July 2008 Preliminary data sheet

1. General description

The ISP1512A is a UTMI+ Low Pin Interface (ULPI) Hi-Speed Universal Serial Bus (USB) transceiver that is fully compliant with *Universal Serial Bus Specification Rev. 2.0* and *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

The ISP1512A can transmit and receive USB data at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s), and provides a pin-optimized, physical layer front-end attachment to the USB host, peripheral and OTG controller with Single Data Rate (SDR) ULPI link. The ISP1512A can transparently transmit and receive UART signaling.

It is ideal for use in portable electronic devices, such as mobile phones, digital still cameras, digital video cameras, Personal Digital Assistants (PDAs) and digital audio players. It allows USB Application-Specific Integrated Circuits (ASICs), Programmable Logic Devices (PLDs) or any system chip set to interface with the physical layer of the USB through a 12-pin SDR interface.

The ISP1512A can interface to devices with digital I/O voltages in the range of 1.65 V to 1.95 V.

The ISP1512A is available in WLCSP25 package.

2. Features

- Fully complies with:
  - USB: *Universal Serial Bus Specification Rev. 2.0*
  - ULPI: *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*
- Interfaces to USB host or peripheral cores; optimized for portable devices or system ASICs with built-in ULPI link
- Complete Hi-Speed USB physical front-end solution that supports high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s)
  - Integrated 45 Ω ± 10 % high-speed termination resistors, 1.5 kΩ ± 5 % full-speed device pull-up resistor, and 15 kΩ ± 5 % host termination resistors
  - Integrated parallel-to-serial and serial-to-parallel converters to transmit and receive
  - USB clock and data recovery to receive USB data up to ±500 ppm
  - USB data synchronization from 60 MHz input to 480 MHz output during transmit
  - Insertion of stuff bits during transmit and discarding of stuff bits during receive
  - Non-Return-to-Zero Inverted (NRZI) encoding and decoding
  - Supports bus reset, suspend, resume and high-speed detection handshake (chirp)
- Partial USB OTG physical front-end support

- Supports Session Request Protocol (SRP) that adheres to *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*
- Complete control over USB termination resistors
- Data line and V_{BUS} pulsing session request methods
- Integrated V_{BUS} voltage comparators

- Flexible system integration and very low current consumption, optimized for portable devices
  - 3.0 V to 4.5 V power supply input range
  - Internal voltage regulator supplies 2.7 V or 3.3 V and 1.8 V
  - Supports interfacing I/O voltage of 1.65 V to 1.95 V; separate I/O voltage supply pins minimize crosstalk
  - Powers down internal regulators in power-down mode when $V_{CC(I/O)}$ is not present or when the chip is deasserted
  - Typical operating current of 10 mA to 48 mA, depending on the USB speed and bus utilization
  - Typical suspend current of 50 µA
  - Typical power-down state current 0.5 µA, max 10 µA
  - 3-state ULPI interface by the CHIP_SEL pin, allowing bus reuse by other applications
- Highly optimized ULPI compliant
  - 60 MHz, 12-pin interface between the core and the transceiver, including an 8-bit SDR data bus
  - Supports 60 MHz output clock configuration
  - Integrated Phase-Locked Loop (PLL) supporting input clock frequency of 19.2 MHz
  - Fully programmable ULPI-compliant register set
  - 3-pin or 6-pin full-speed or low-speed serial mode
  - Internal Power-On Reset (POR) circuit
- UART interface:
  - Supports transparent UART signaling on the DP and DM pins for UART accessory applications
  - 2.7 V UART signaling on the DP and DM pins
  - Entering UART mode by register setting
  - Exiting UART mode by asserting STP or by toggling the CHIP_SEL pin
- Full industrial grade operating temperature range from –40 °C to +85 °C
- ESD compliance:
  - JESD22-A114-B ±2 kV contact Human Body Model (HBM)
  - JESD22-A115-A ±200 V Machine Model (MM)
  - JESD22-C101-A ±500 V Charge Device Model (CDM)
  - IEC 61000-4-2 ±8 kV contact on the DP and DM pins
- Available in small WLCSP25 Restriction of Hazardous Substances (RoHS) compliant, halogen-free and lead-free package

3. Applications

- Mobile phone
- Digital still camera

- MP3 player
- PDA
- Digital TV
- Digital Video Disc (DVD) recorder
- External storage device
- Printer
- Scanner
- Set-Top Box (STB)
- Video camera

4. Ordering information

Table 1. Ordering information

Part			Package			
Type number	**CHIP_SEL polarity**	**Frequency**	**Name**	**Description**	**Bump pitch**	**Version**
ISP1512AUK	active LOW	19.2 MHz	WLCSP25	wafer level chip-size package; 25 bumps; body 2.24 × 2.21 × 0.6 mm	0.4 mm	ISP1512xUK

5. Marking

Table 2. Marking codes

Type number	Marking code[1]
ISP1512AUK	1512A

[1] The package marking is the first line of text on the IC package and can be used for IC identification.

6. Block diagram

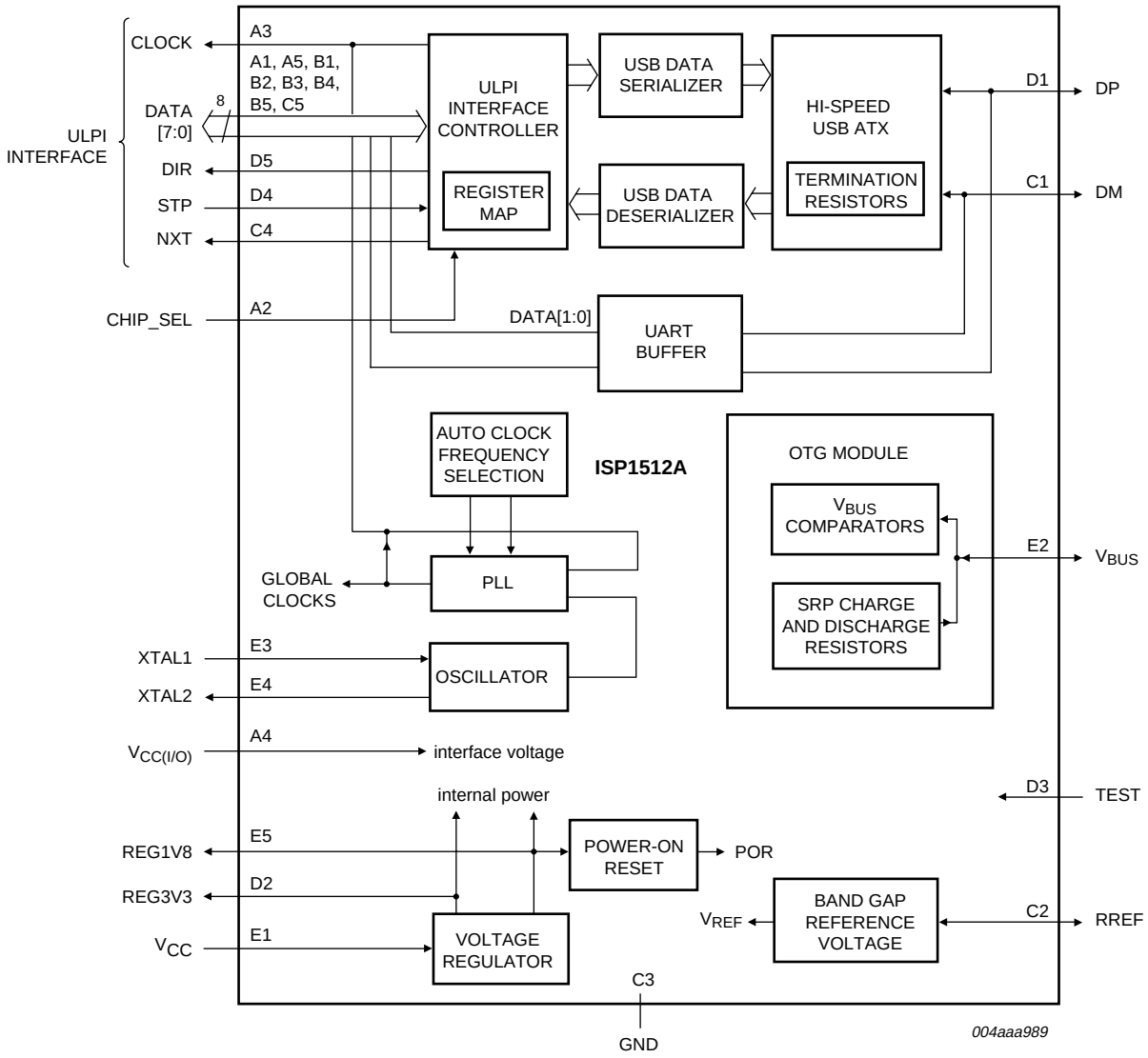


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

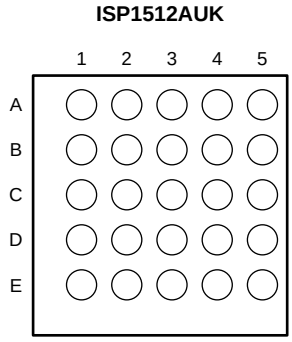


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol[1]	Pin	Type[2]	Description[3]
DATA0	A1	I/O	ULPI data pin 0 3-state output; plain input
CHIP_SEL	A2	I	• When this pin is deasserted, ULPI pins will be in 3-state and the ISP1512A is in power-down mode. • When this pin is asserted, ULPI pins will operate normally. The ISP1512A is an active-LOW chip select input. A HIGH level on this pin sets the ISP1512A into power-down mode. If the CHIP_SEL pin is not in use, connect it to GND. plain input
CLOCK	A3	O	60 MHz clock output 3-state output
$V_{CC(I/O)}$	A4	P	input I/O supply voltage; 1.65 V to 1.95 V
DATA5	A5	I/O	ULPI data pin 5 3-state output; plain input
DATA1	B1	I/O	ULPI data pin 1 3-state output; plain input
DATA2	B2	I/O	ULPI data pin 2 3-state output; plain input
DATA3	B3	I/O	ULPI data pin 3 3-state output; plain input
DATA4	B4	I/O	ULPI data pin 4 3-state output; plain input

Table 3. Pin description *...continued*

Symbol[1]	Pin	Type[2]	Description[3]
DATA6	B5	I/O	ULPI data pin 6 3-state output; plain input
DM	C1	AI/O	connect to the D– pin of the USB connector • USB mode: D– input or output • UART mode: TXD output
RREF	C2	AI/O	resistor reference; connect through 12 kΩ ± 1 % resistor to GND
GND	C3	P	ground supply
NXT	C4	O	ULPI next signal 3-state output
DATA7	C5	I/O	ULPI data pin 7 3-state output; plain input
DP	D1	AI/O	connect to the D+ pin of the USB connector • USB mode: D+ input or output • UART mode: RXD input
REG3V3	D2	P	3.3 V regulator output for USB mode or 2.7 V regulator output for UART mode; requiring parallel 0.1 µF and 4.7 µF capacitors; internally powers ATX and other analog circuits; must not be used to power external circuits
TEST	D3	I	connect to ground for normal operation
STP	D4	I	ULPI stop signal plain input
DIR	D5	O	ULPI direction signal 3-state output
V_{CC}	E1	P	input supply voltage or battery source; 3.0 V to 4.5 V **Remark:** Below 3.0 V, USB full-speed and low-speed transactions are not guaranteed to work, though some devices may work with the ISP1512A at these voltages.
V_{BUS}	E2	AI/O	connect to the V_{BUS} pin of the USB connector; if this pin is not in use, leave it open ($R_{I(idle)(VBUS)}$ is present on this pin)
XTAL1	E3	AI/O	crystal oscillator or clock input; if this pin is not in use, connect it to the REG1V8 pin
XTAL2	E4	AI/O	crystal oscillator output; if a crystal is not attached, leave this pin open
REG1V8	E5	P	1.8 V regulator output; internally powers the digital core; must not be used to power external circuits

[1] Symbol names ending with underscore N (for example, NAME_N) indicate active-LOW signals.

[2] I = input; O = output; I/O = digital input/output; AI/O = analog input/output; P = power or ground pin.

[3] A detailed description of these pins can be found in Section 8.10.

8. Functional description

8.1 ULPI interface controller

The ISP1512A provides a 12-pin interface that is compliant with *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*. This interface must be connected to a USB link.

The ULPI interface controller provides the following functions:

- ULPI-compliant interface and register set
- Allows full control over USB peripheral or host functionality
- Parses the USB transmit and receive data
- Prioritizes the USB receive data, USB transmit data, interrupts and register operations
- Low-power mode
- 3-pin serial mode
- 6-pin serial mode
- Generates RXCMDs (status updates)
- Maskable interrupts

8.2 USB serializer and deserializer

The USB data serializer prepares data to transmit on the USB bus. To transmit data, the USB link sends a transmit command and data on the ULPI bus. The serializer performs parallel-to-serial conversion, bit stuffing and NRZI encoding. For packets with a PID, the serializer adds a SYNC pattern to the start of the packet, and an EOP pattern to the end of the packet. When the serializer is busy and cannot accept any more data, the ULPI interface controller deasserts NXT.

The USB data deserializer decodes data received from the USB bus. When data is received, the deserializer strips the SYNC and EOP patterns, and then performs serial-to-parallel conversion, NRZI decoding and discarding of stuff bits on the data payload. The ULPI interface controller sends data to the USB link by asserting DIR, and then asserting NXT whenever a byte is ready. The deserializer also detects various receive errors, including bit stuff errors, elasticity buffer underrun or overrun, and byte-alignment errors.

8.3 Hi-Speed USB (USB 2.0) ATX

The Hi-Speed USB ATX block is an analog front-end containing the circuitry needed to transmit, receive and terminate the USB bus in high-speed, full-speed and low-speed, for USB peripheral, host or OTG implementations. The following circuitry is included:

- Differential drivers to transmit data at high-speed, full-speed and low-speed
- Differential and single-ended receivers to receive data at high-speed, full-speed and low-speed
- Squelch circuit to detect high-speed bus activity
- High-speed disconnect detector
- 45 Ω high-speed bus terminations on pins DP and DM
- 1.5 kΩ pull-up resistor on pin DP

- 15 kΩ bus terminations on pins DP and DM

For details on controlling resistor settings, see Table 12.

8.4 Voltage regulator

The ISP1512A contains a built-in voltage regulator that conditions the V_{CC} supply for use inside the ISP1512A. The voltage regulator:

- Supports input supply range 3.0 V < V_{CC} < 4.5 V.
- Can be supplied from a battery with the voltage range mentioned above.
- Supplies internal digital circuitry with 1.8 V and analog circuitry with 3.3 V or 2.7 V.
- In USB mode, automatically bypasses the internal 3.3 V regulator when V_{CC} < 3.5 V, the internal analog circuitry directly draws power from the V_{CC} pin. In UART mode, the bypass switch will be disabled.
- Will be shut down when $V_{CC(I/O)}$ is not present or when the CHIP_SEL pin is deasserted.

8.5 Crystal oscillator and PLL

The ISP1512A has a built-in crystal oscillator and a Phase-Locked Loop (PLL) for clock generation. When a crystal is in use, the built-in crystal oscillator generates a square wave clock for internal use. A square wave clock of the same frequency can also be driven directly into the XTAL1 pin. Using an existing square wave clock can save the cost of a crystal and also reduce the board space.

The PLL takes the square wave clock from the crystal oscillator, and multiplies or divides it into various frequencies for internal use.

The PLL produces the following frequencies, irrespective of the clock source:

- 1.5 MHz for low-speed USB data
- 12 MHz for full-speed USB data
- 60 MHz clock for the ULPI interface controller
- 480 MHz for high-speed USB data
- Other internal frequencies for data conversion and data recovery

8.6 UART buffer

The UART buffer includes circuits to support the transparent UART signaling between the DATA0 or DATA1 pin and the DP or DM pin.

When the ISP1512A is put into UART mode, it acts as a voltage level shifter between following pins:

- From DATA0 ($V_{CC(I/O)}$ level) to DM (2.7 V level) for UART TXD signaling path.
- From DP (2.7 V level) to DATA1 ($V_{CC(I/O)}$ level) for UART RXD signaling path.

8.7 OTG module

This module contains several sub-blocks that provide some functionality required by the USB OTG specification. Specifically, it provides the following circuits:

- V_{BUS} comparators to determine the V_{BUS} voltage level.
- Resistors to temporarily charge and discharge V_{BUS}. This is required for SRP.

8.7.1 V_{BUS} comparators

The ISP1512A provides three comparators to detect the V_{BUS} voltage level. The comparators are explained in the following subsections.

8.7.1.1 V_{BUS} valid comparator

This comparator is used by hosts and A-devices to determine whether the voltage on V_{BUS} is at a valid level for operation. The ISP1512A minimum threshold for the V_{BUS} valid comparator is 4.4 V. Any voltage on V_{BUS} below this threshold is considered invalid. During power-up, it is expected that the comparator output will be ignored.

8.7.1.2 Session valid comparator

The session valid comparator is a TTL-level input that determines when V_{BUS} is high enough for a session to start. Peripherals, A-devices and B-devices use this comparator to detect when a session is started. The A-device also uses this comparator to determine when a session is completed. The session valid threshold of the ISP1512A is between 0.8 V to 2.0 V.

8.7.1.3 Session end comparator

The session end comparator determines when V_{BUS} is below the B-device session end threshold of 0.2 V to 0.8 V. The B-device uses this threshold to determine when a session has ended.

8.7.2 SRP charge and discharge resistors

The ISP1512A provides on-chip resistors for short-term charging and discharging of V_{BUS}. These are used by the B-device to request a session, prompting the A-device to restore the V_{BUS} power. First, the B-device ensures that V_{BUS} is fully discharged from the previous session by setting the DISCHRG_VBUS register bit to logic 1 and waiting for SESS_END to be logic 1. Then the B-device charges V_{BUS} by setting the CHRG_VBUS register bit to logic 1. The A-device sees that V_{BUS} is charged above the session valid threshold and starts a session by turning on the V_{BUS} power.

8.8 Band gap reference voltage

The band gap circuit provides a stable internal voltage reference to bias the analog circuitry. This band gap requires an accurate external reference resistor. Connect a 12 kΩ ± 1 % resistor between the RREF pin and GND.

8.9 Power-On Reset (POR)

An internal POR pulse is generated when REG1V8 rises above $V_{POR(trip)}$. The internal POR pulse will be generated whenever REG1V8 drops below $V_{POR(trip)}$ for more than $t_{w(REG1V8\_L)}$.

To give a better view of the functionality, Figure 3 shows a possible curve of REG1V8. The internal POR starts with logic 0 at t0. At t1, the detector will see the passing of the trip level so that a POR pulse is generated to reset all internal circuits. If REG1V8 dips from t2

to t3 for greater than $t_{w(REG1V8\_L)}$, another POR pulse is generated. If the dip from t4 to t5 is less than $t_{w(REG1V8\_L)}$, the internal POR pulse will not be generated and will remain LOW.

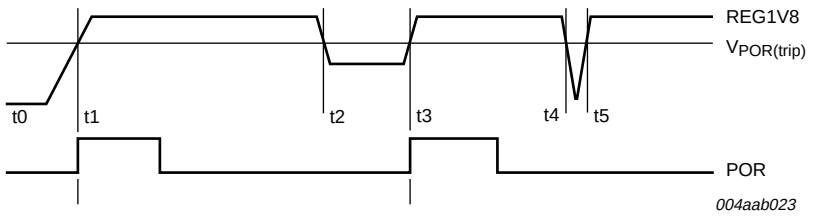


Fig 3. Internal power-on reset timing

8.10 Detailed description of pins

8.10.1 DATA[7:0]

Bidirectional data bus pins. The USB link must drive DATA[7:0] to LOW when the ULPI bus is idle. When the link has data to transmit to the PHY, it drives a nonzero value. Weak pull-down resistors are incorporated into DATA[7:0] pins as part of the interface protect feature.

DATA[7:0] pins can also be 3-stated when pin CHIP_SEL is deasserted.

The data bus can be reconfigured to carry various data types. For details, see Section 9.2.

8.10.2 $V_{CC(I/O)}$

The input power pin that sets the I/O voltage level. A 0.1 µF decoupling capacitor is recommended on this pin.

8.10.3 RREF

Resistor reference analog I/O pin. A 12 kΩ ± 1 % resistor must be connected between the RREF pin and GND. This provides an accurate voltage reference that biases the internal analog circuitry. Less accurate resistors cannot be used and will render the ISP1512A unusable.

8.10.4 DP and DM

When the ISP1512A is in USB mode, the DP pin functions as the USB data plus line, and the DM pin functions as the USB data minus line.

When the ISP1512A is in transparent UART mode, the DP pin functions as the UART RXD input pin, and the DM pin functions as the UART TXD output pin.

The DP and DM pins must be connected to the D+ and D– pins of the USB receptacle.

8.10.5 V_{CC}

Main input supply voltage for the ISP1512A. The ISP1512A operates correctly when V_{CC} is between 3.0 V and 4.5 V. A 0.1 µF decoupling capacitor is recommended.

8.10.6 V_{BUS}

This I/O pin acts as an input to V_{BUS} comparators, and also as a power pin for SRP charge and discharge resistors. For details, see Figure 4.

The V_{BUS} pin requires a capacitive load. Table 4 provides the recommended capacitor values for various applications.

Table 4. Recommended V_{BUS} capacitor value

Application	V_{BUS} capacitor (C_{VBUS})
OTG	1 µF to 6.5 µF, 10 V
Standard host	120 µF ± 20 %, 10 V
Standard peripheral	1 µF to 10 µF, 10 V

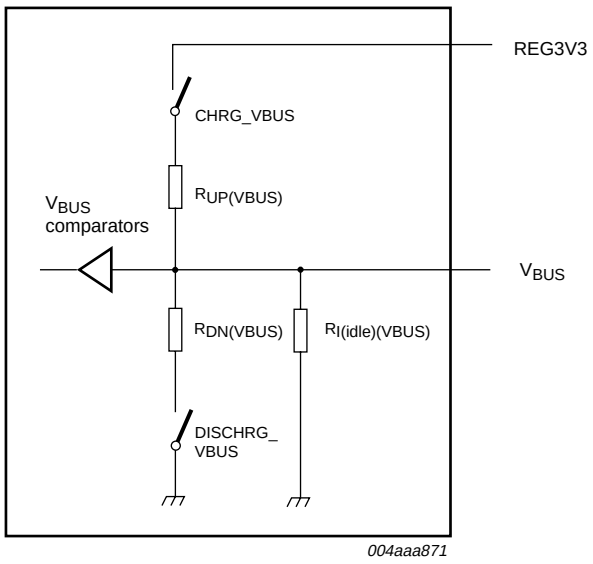


Fig 4. Internal circuit of the V_{BUS} pin

8.10.7 REG3V3 and REG1V8

These are output voltage pins from the internal regulator. These supplies are used internally to power digital and analog circuits.

For proper operation of the regulator, pins REG3V3 and REG1V8 must each be connected to a 0.1 µF capacitor in parallel with a 4.7 µF low ESR capacitor.

8.10.8 XTAL1 and XTAL2

XTAL1 is the crystal oscillator input, and XTAL2 is the crystal oscillator output.

If the link requires a 60 MHz clock from the ISP1512A, then either a crystal must be attached, or a clock of the same frequency must be driven into XTAL1, with XTAL2 left unconnected.

If a crystal is attached, it requires a capacitor on each terminal of the crystal to GND. The values of the maximum series resistance of the crystal and required external capacitors are given in Table 5.

Table 5. External capacitor values for 19.2 MHz clock frequency

Load capacitance of the crystal[1]	Maximum series resistance of the crystal	External capacitor C_{XTAL} value
10 pF	< 180 Ω	18 pF
20 pF	< 100 Ω	39 pF

[1] Specified by the crystal manufacturer.

8.10.9 CHIP_SEL

The CHIP_SEL pin has two functions: chip select and power-down control. When CHIP_SEL is deasserted, ULPI pins DATA[7:0], CLOCK, DIR and NXT are 3-stated and ignored. Internal circuits are powered-down. When CHIP_SEL is asserted, the ISP1512A will operate normally.

8.10.10 DIR

ULPI direction output pin. Synchronous to the rising edge of CLOCK. Controls the direction of the data bus. By default, the ISP1512A holds DIR at LOW, causing the data bus to be an input. When DIR is LOW the ISP1512A listens for data from the link. The ISP1512A pulls DIR to HIGH only when it has data to send to the link, which is for one of two reasons:

- To send data (USB receive or register reads) and RXCMD status updates to the link.
- To block the link from driving the data bus during power-up, reset and low power mode (suspend).

8.10.11 STP

ULPI stop input pin. Synchronous to the rising edge of CLOCK. The link must assert STP to signal the end of a USB transmit packet or a register write operation. When DIR is asserted, the link can optionally assert STP for one clock cycle to abort the ISP1512A, causing it to deassert DIR in the next clock cycle.

8.10.12 NXT

ULPI next data output pin. Synchronous to the rising edge of CLOCK. The ISP1512A holds NXT at LOW, by default. When DIR is LOW and the link is sending data to the ISP1512A, NXT will be asserted to notify the link to provide the next data byte. When DIR is HIGH and the ISP1512A is sending data to the link, NXT will be asserted to notify the link that another valid byte is on the bus. NXT is not used for register read data or the RXCMD status update.

8.10.13 CLOCK

A 60 MHz interface clock to synchronize the ULPI bus. In SDR mode, all ULPI pins are synchronous to the rising edge of CLOCK.

The ISP1512A provides two clocking options:

- A crystal is attached between the XTAL1 and XTAL2 pins.
- A clock driven into the XTAL1 pin, with the XTAL2 pin left unconnected.

8.10.14 GND

Global ground signal. To ensure the correct operation of the ISP1512A, GND must be soldered to the cleanest ground available.

9. Modes of operation

9.1 Power modes

When both $V_{CC(I/O)}$ and V_{CC} are not powered, there will be no leakage from the V_{BUS} pin to all the remaining pins, including V_{CC} and $V_{CC(I/O)}$. Applying V_{BUS} within the normal range will not damage the ISP1512A chip.

When both V_{CC} and $V_{CC(I/O)}$ are powered and are within the operating voltage range, the ISP1512A will be fully functional as in normal mode.

When $V_{CC(I/O)}$ is powered and the V_{CC} voltage is below the operating range of the ISP1512A, the application system must detect the low voltage condition and set the CHIP_SEL pin to deassert (that is, put the ISP1512A in power-down mode). This is to protect the ULPI and USB interfaces from driving wrong levels. Under this condition, the $V_{CC(I/O)}$ voltage will not leak to USB pins (V_{BUS}, DP and DM) and the V_{CC} pin. All the digital pins powered by $V_{CC(I/O)}$ are configured as high-impedance inputs. These pins must be driven to their defined states, or terminated by using pull-up or pull-down resistors to avoid floating input condition. Other pins are not powered.

9.1.1 Normal mode

In normal mode, both V_{CC} and $V_{CC(I/O)}$ are powered. The CHIP_SEL pin is asserted. The ISP1512A is fully functional.

9.1.2 Power-down mode

When $V_{CC(I/O)}$ is not present or when the CHIP_SEL pin is deasserted, the ISP1512A is put into power-down mode. In this mode, internal regulators are powered down to keep the V_{CC} current to a minimum. The voltage on the V_{CC} pin will not leak to the $V_{CC(I/O)}$ and/or V_{BUS} pins. In this mode, the ISP1512A pin states are given in Table 6.

Table 6. Pin states in power-down mode

Pin name	Pin state when $V_{CC(I/O)}$ is not present	Pin state when CHIP_SEL is deasserted
V_{CC}	3.0 V to 4.5 V	3.0 V to 4.5 V
$V_{CC(I/O)}$	not powered[1]	1.65 V to 1.95 V
CHIP_SEL	not powered	HIGH
TEST, CLOCK, STP, NXT, DIR, DATA[7:0]	not powered[1]	high-Z (inputs are ignored)
REG3V3, REG1V8, DP, DM, XTAL1, XTAL2, RREF	not powered[1]	not powered[1]

[1] These pins must not be externally driven to HIGH. Otherwise, the ISP1512A behavior is undefined and leakage current will occur.

When $V_{CC(I/O)}$ is not present, all pins are not powered.

When the ISP1512A is put into power-down mode by disabling the CHIP_SEL pin, all the digital pins that are powered by $V_{CC(I/O)}$ are configured as high-impedance inputs. These pins must be driven to their defined states or terminated by using pull-up or pull-down resistors to avoid floating input condition. Other pins are not powered. In this mode, minimum current will be drawn by $V_{CC(I/O)}$ to detect the CHIP_SEL pin status.

9.2 ULPI modes

The ISP1512A ULPI interface can be programmed to operate in three modes. In each mode, the signals on the data bus are reconfigured as described in the following subsections. Setting more than one mode will lead to undefined behavior.

9.2.1 Synchronous mode

This is default mode. On power-up, and when CLOCK is stable, the ISP1512A will enter synchronous mode.

In synchronous mode, the link must synchronize all ULPI signals to CLOCK, meeting the set-up and hold times as defined in Section 14.

This mode is used by the link to perform the following tasks:

- High-speed detection handshake (chirp)
- Transmit and receive USB packets
- Read and write to registers
- Receive USB status updates (RXCMDs) from the ISP1512A

Table 7. ULPI signal description

Signal name	Direction on the ISP1512A[1]	Signal description
CLOCK	O	**60 MHz interface clock**: If a crystal is attached or a clock is driven into the XTAL1 pin, the ISP1512A will drive a 60 MHz output clock. During low-power and serial modes, the clock can be turned off to save power.
DATA[7:0]	I/O	**4-bit or 8-bit data bus**: In synchronous mode, the link drives DATA[7:0] to LOW by default. The link initiates transfers by sending a nonzero data pattern called a TXCMD (transmit command). In synchronous mode, the direction of DATA[7:0] is controlled by DIR. Contents of DATA[7:0] lines must be ignored for exactly one clock cycle whenever DIR changes value. This is called a turnaround cycle. Data lines have fixed directions and different meanings in low-power and 3-pin serial modes.

Table 7. ULPI signal description *…continued*

Signal name	Direction on the ISP1512A[1]	Signal description
DIR	O	**Direction**: Controls the direction of data bus DATA[7:0]. In synchronous mode, the ISP1512A drives DIR to LOW by default, making the data bus an input so the ISP1512A can listen for TXCMD from the link. The ISP1512A drives DIR to HIGH only when it has data for the link. When DIR and NXT are HIGH, the byte on the data bus contains decoded USB data. When DIR is HIGH and NXT is LOW, the byte contains status information called an RXCMD (receive command). The only exception to this rule is when the PHY returns register read data, where NXT is also LOW, replacing the usual RXCMD byte. Every change in DIR causes a turnaround cycle on the data bus, during which DATA[7:0] are not valid and must be ignored by the link. DIR is always asserted during low-power and serial modes.
STP	I	**Stop**: In synchronous mode, the link drives STP to HIGH for one cycle after the last byte of data is sent to the ISP1512A. The link can optionally assert STP to force DIR to be deasserted. In low-power and serial modes, the link holds STP at HIGH to wake up the ISP1512A, causing the ULPI bus to return to synchronous mode.
NXT	O	**Next**: In synchronous mode, the ISP1512A drives NXT to HIGH to throttle data. If DIR is LOW, the ISP1512A asserts NXT to notify the link to place the next data byte on DATA[7:0] in the following clock cycle. If DIR is HIGH, the ISP1512A asserts NXT to notify the link that a valid USB data byte is on DATA[7:0] in the current cycle. The ISP1512A always drives an RXCMD when DIR is HIGH and NXT is LOW, unless register read data is to be returned to the link in the current cycle. NXT is not used in low-power and serial modes.

[1] I = input; O = output; I/O = digital input/output.

9.2.2 Low-power mode

When the USB bus is idle, the link can place the ISP1512A into low-power mode (also called suspend mode). In low-power mode, the data bus definition changes to that shown in Table 8. To enter low-power mode, the link sets the SUSPENDM bit in the FUNC_CTRL register to logic 0. To exit low-power mode, the link asserts the STP signal. After exiting low-power mode, the ISP1512A will send an RXCMD to the link if a change was detected in any interrupt source, and the change still exists. An RXCMD may not be sent if the interrupt condition is removed before exiting.

The ISP1512A will draw only suspend current from the V_{CC} supply; see Table 41.

During low-power mode, the clock on XTAL1 may be stopped. The clock must be started again before asserting STP to exit low-power mode.

For more information on low-power mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 8. Signal mapping during low-power mode

Signal	Maps to	Direction[1]	Description
LINESTATE0	DATA0	O	combinatorial LINESTATE0 directly driven by the analog receiver
LINESTATE1	DATA1	O	combinatorial LINESTATE1 directly driven by the analog receiver

Table 8. Signal mapping during low-power mode *…continued*

Signal	Maps to	Direction[1]	Description
Reserved	DATA2	-	reserved; the ISP1512A will drive this pin to LOW
INT	DATA3	O	active-HIGH interrupt indication; will be asserted whenever any unmasked interrupt occurs
Reserved	DATA[7:0]	-	reserved; the ISP1512A will drive this pin to LOW

[1] O = output.

9.2.3 6-pin full-speed or low-speed serial mode

If the link requires a 6-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the ISP1512A to 6-pin serial mode. In 6-pin serial mode, the data bus definition changes to that shown in Table 9. To enter 6-pin serial mode, the link sets the 6PIN_FSLS_SERIAL bit in the INTF_CTRL register to logic 1. To exit 6-pin serial mode, the link asserts the STP signal. This is provided primarily for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective upgrade path to high-speed functionality. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 6-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1 before entering 6-pin serial mode.

For more information on 6-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 9. Signal mapping for 6-pin serial mode

Signal	Maps to	Direction[1]	Description
TX_ENABLE	DATA0	I	active-HIGH transmit enable
TX_DAT	DATA1	I	transmit differential data on DP and DM
TX_SE0	DATA2	I	transmit single-ended zero on DP and DM
INT	DATA3	O	active-HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
RX_DP	DATA4	O	single-ended receive data from DP
RX_DM	DATA5	O	single-ended receive data from DM
RX_RCV	DATA6	O	differential receive data from DP and DM
Reserved	DATA7	-	reserved; the ISP1512A will drive this pin to LOW

[1] I = input; O = output.

9.2.4 3-pin full-speed or low-speed serial mode

If the link requires a 3-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the ISP1512A to 3-pin serial mode. In 3-pin serial mode, the data bus definition changes to that shown in Table 10. To enter 3-pin serial mode, the link sets the 3PIN_FSLS_SERIAL bit in the INTF_CTRL register to logic 1. To exit 3-pin serial mode, the link asserts STP. This is provided primarily for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective upgrade path to high-speed functionality. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 3-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1 before entering 3-pin serial mode.

For more information on the 3-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 10. Signal mapping for 3-pin serial mode

Signal	Maps to	Direction[1]	Description
TX_ENABLE	DATA0	I	active-HIGH transmit enable
DAT	DATA1	I/O	transmit differential data on DP and DM when TX_ENABLE is HIGH receive differential data from DP and DM when TX_ENABLE is LOW
SE0	DATA2	I/O	transmit single-ended zero on DP and DM when TX_ENABLE is HIGH receive single-ended zero from DP and DM when TX_ENABLE is LOW
INT	DATA3	O	active-HIGH interrupt indication; will be asserted and latched whenever any unmasked interrupt occurs
Reserved	DATA[7:4]	-	reserved; the ISP1512A will drive these pins to LOW

[1] I = input; O = output; I/O = digital input/output.

9.2.5 Transparent UART mode

In transparent UART mode, the ISP1512A functions as a voltage level shifter between following pins:

- From pin DATA0 ($V_{CC(I/O)}$ level) to pin DM (2.7 V level)
- From pin DP (2.7 V level) to pin DATA1 ($V_{CC(I/O)}$ level)

The USB transceiver is used to drive the UART transmitting signal on the DM line. The rise time and the fall time of the transmitting signal is determined by whether a full-speed or low-speed transceiver is in use. It is recommended to use a full-speed transceiver if the UART bit rate is equal to or above 921 kbit/s. If the UART bit rate is below 921 kbit/s, a low-speed transceiver may be selected for better EMI performance.

In transparent UART mode, data bus definitions change to that shown in Table 11.

Table 11. UART signal mapping

Signal	Maps to	Direction[1]	Description
TXD	DATA0	I	UART TXD signal that is routed to the DM pin
RXD	DATA1	O	UART RXD signal that is routed from the DP pin
Reserved	DATA2	-	reserved
INT	DATA3	O	active-HIGH interrupt indication; must be asserted and latched whenever any unmasked interrupt occurs
Reserved	DATA[7:4]	-	reserved; the ISP1512A will drive these pins to LOW

[1] I = input; O = output.

Transparent UART mode is entered by setting some register bits in ULPI registers. The recommended sequence is:

1. Set the XCVRSELECT[1:0] bits in the FUNC_CTRL register (see Section 10.5) to 10b (low-speed) or 01b (full-speed). This setting affects the rise time and the fall time of the UART transmitting signal on the DM line.
2. Set the DP_PULLDOWN and DM_PULLDOWN bits in the OTG_CTRL register (see Section 10.7) to logic 0.
3. Set the TERMSELECT bit in the FUNC_CTRL register (see Section 10.5) to logic 0 (power-on default value).

Remark: Mandatory when a full-speed driver is used and optional for a low-speed driver.

4. Set the TXD_EN and RXD_EN bits in the CARKIT_CTRL register (see Section 10.14) to logic 1. These two bits must be set together in one TXCMD.
5. Set the CARKIT_MODE bit in the INTF_CTRL register (see Section 10.6) to logic 1.

   Remark: The CARKIT_MODE, TXD_EN and RXD_EN bits must be set to logic 1. The sequence of setting these register bits is ignored.

After the register configuration is complete:

1. A weak pull-up resistor will be enabled on the DP and DATA0 pins. This is to avoid the possible floating condition on these input pins when UART mode is enabled.
2. The 39 Ω serial termination resistors on the DP and DM pins will be enabled.
3. One clock cycle after DIR goes from LOW to HIGH, the ISP1512A will drive the data bus for five clock cycles. This is to charge the DATA0 pin to a HIGH level for a slow link. However, the link can start driving DATA0 to HIGH immediately after the turnaround cycle.
4. UART buffers between DATA0 or DATA1 and DM or DP are enabled. Transparent UART mode is entered.

   Remark: The DP pin will be slowly charged up to HIGH by the weak pull-up resistor. The time needed depends on the capacitive loading on DP.

By default, the clock is powered down when the ISP1512A enters UART mode. If the link requires CLOCK to be running in UART mode, it can set the CLOCK_SUSPENDM bit in the INTF_CTRL register to logic 1 before entering UART mode.

Transparent UART mode is exited by asserting the STP pin to HIGH or by toggling the CHIP_SEL pin.

The INT pin is asserted and latched whenever an unmasked interrupt event occurs. When the link detects INT as HIGH, it must wake up the clock (if powered down) by asserting STP. If the clock is already running, the link asserts STP for one or more clock cycles to switch the interface to synchronous mode. When the PHY is in synchronous mode, the link can read the USB_INTR_L register to determine the source of the interrupt. Note that ISP1512A does not implement optional Carkit Interrupt registers.

An alternative way to exit UART mode is to set the CHIP_SEL pin to deassert for more than t_{PWRDN} and then set it to assert. A power-on reset will be generated and the ULPI bus will be put in default synchronous mode.

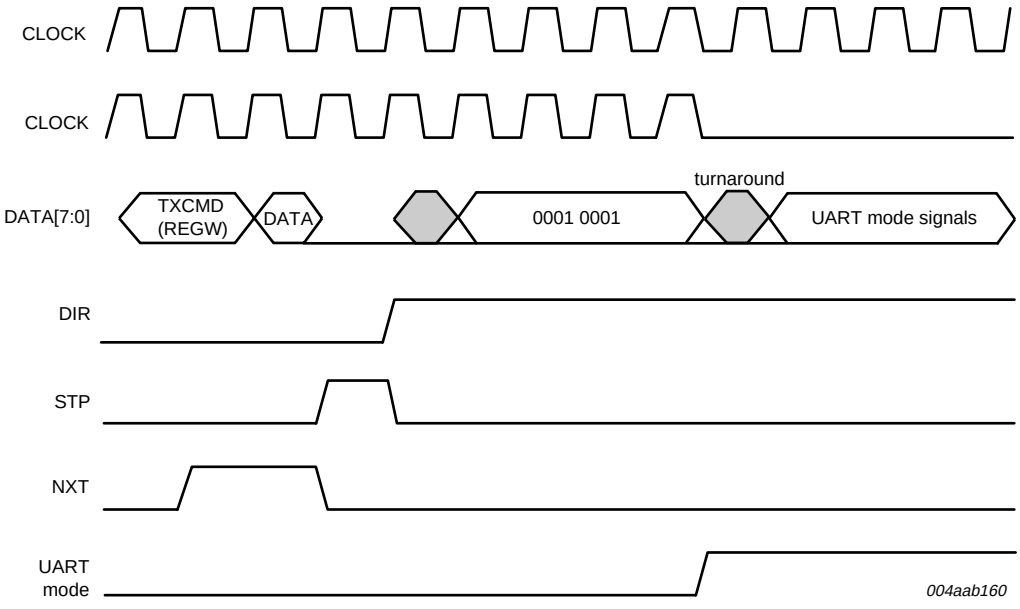


Fig 5. Interface behavior when entering UART mode and the clock is powered down

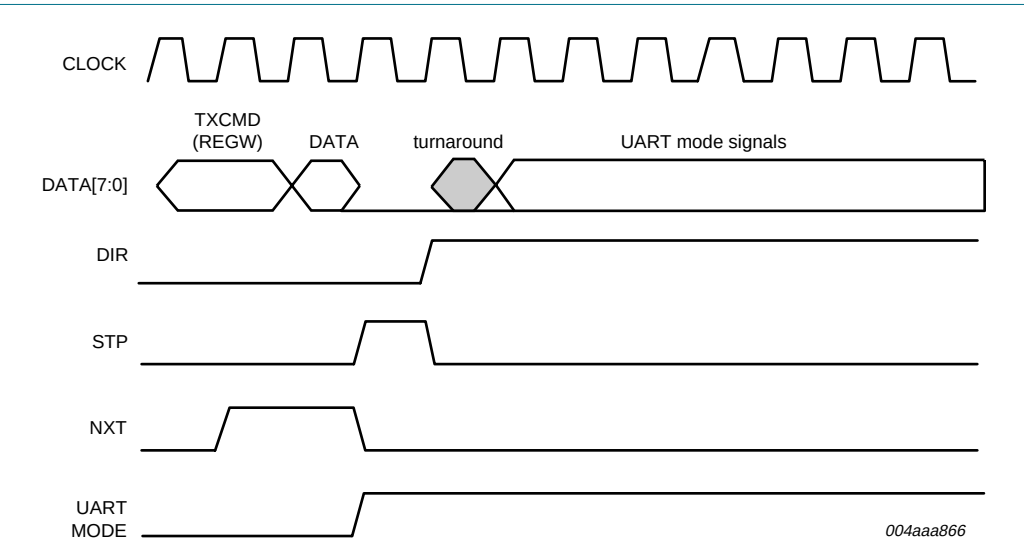


Fig 6. Interface behavior when entering UART mode and the clock remains powered

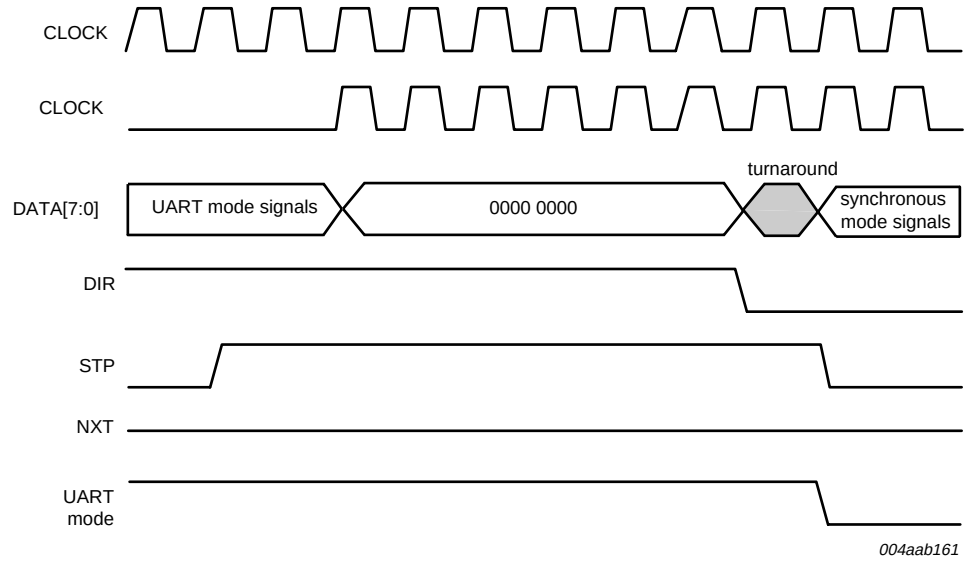


Fig 7. Interface behavior when exiting UART mode and the clock is not running

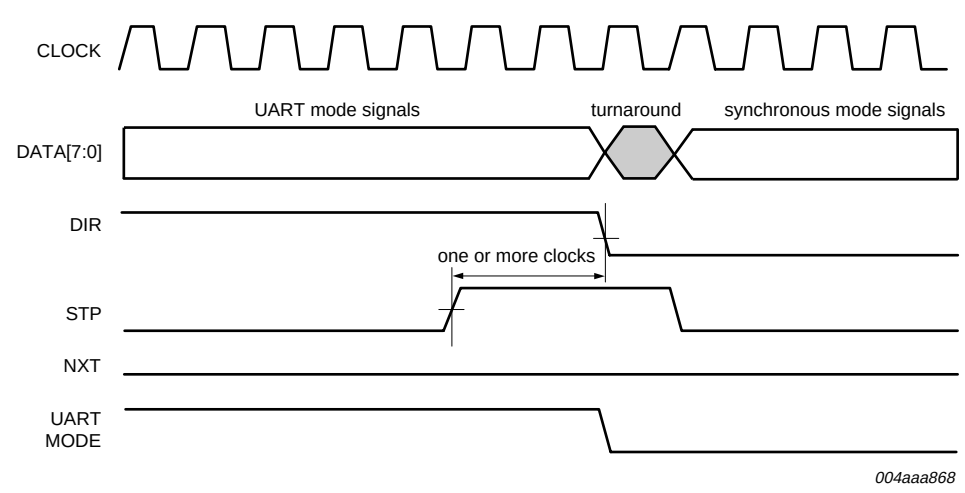


Fig 8. Interface behavior when exiting UART mode and the clock is running

9.3 USB state transitions

A Hi-Speed USB peripheral, host or OTG device handles more than one electrical state as defined in *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*. The ISP1512A accommodates various states through register settings of the XCVRSELECT[1:0], TERMSELECT, OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN bits.

Table 12 summarizes operating states. The values of register settings in Table 12 will force resistor settings as also given in Table 12. Resistor setting signals are defined as follows.

- RPU_DP_EN enables the 1.5 kΩ pull-up resistor on DP

- RPD_DP_EN enables the 15 kΩ pull-down resistor on DP
- RPD_DM_EN enables the 15 kΩ pull-down resistor on DM
- HSTERM_EN enables the 45 Ω termination resistors on DP and DM

It is up to the link to set the desired register settings.

Table 12. Operating states and their corresponding resistor settings

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_ PULL DOWN	DM_ PULL DOWN	RPU_DP _EN	RPD_DP _EN	RPD_ DM_EN	HSTERM_ EN
General settings									
3-state drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b
Power-up or $V_{BUS} < V_{B\_SESS\_END}$	01b	0b	00b	1b	1b	0b	1b	1b	0b
Host settings									
Host chirp	00b	0b	10b	1b	1b	0b	1b	1b	1b
Host high-speed	00b	0b	00b	1b	1b	0b	1b	1b	1b
Host full-speed	X1b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed suspend	01b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed resume	01b	1b	10b	1b	1b	0b	1b	1b	0b
Host low-speed	10b	1b	00b	1b	1b	0b	1b	1b	0b
Host low-speed suspend	10b	1b	00b	1b	1b	0b	1b	1b	0b
Host low-speed resume	10b	1b	10b	1b	1b	0b	1b	1b	0b
Host Test J or Test K	00b	0b	10b	1b	1b	0b	1b	1b	1b
Peripheral settings									
Peripheral chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral high-speed	00b	0b	00b	0b	0b	0b	0b	0b	1b
Peripheral full-speed	01b	1b	00b	0b	0b	1b	0b	0b	0b
Peripheral high-speed or full-speed suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b
Peripheral high-speed or full-speed resume	01b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral Test J or Test K	00b	0b	10b	0b	0b	0b	0b	0b	1b
OTG settings									
OTG device peripheral chirp	00b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed	00b	0b	00b	0b	1b	0b	0b	1b	1b

Table 12. Operating states and their corresponding resistor settings *…continued*

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_ PULL DOWN	DM_ PULL DOWN	RPU_DP _EN	RPD_DP _EN	RPD_ DM_EN	HSTERM_ EN
OTG device peripheral full-speed	01b	1b	00b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed and full-speed suspend	01b	1b	00b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed and full-speed resume	01b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral Test J or Test K	00b	0b	10b	0b	1b	0b	0b	1b	1b

10. Register map

Table 13. Register map

Field name	Size (bit)	Address (6 bit)				References
		R[1]	W[2]	S[3]	C[4]	
VENDOR_ID_LOW	8	00h	-	-	-	Section 10.1 on page 23
VENDOR_ID_HIGH	8	01h	-	-	-	Section 10.2 on page 23
PRODUCT_ID_LOW	8	02h	-	-	-	Section 10.3 on page 24
PRODUCT_ID_HIGH	8	03h	-	-	-	Section 10.4 on page 24
FUNC_CTRL	8	04h to 06h	04h	05h	06h	Section 10.5 on page 24
INTF_CTRL	8	07h to 09h	07h	08h	09h	Section 10.6 on page 25
OTG_CTRL	8	0Ah to 0Ch	0Ah	0Bh	0Ch	Section 10.7 on page 26
USB_INTR_EN_R	8	0Dh to 0Fh	0Dh	0Eh	0Fh	Section 10.8 on page 27
USB_INTR_EN_F	8	10h to 12h	10h	11h	12h	Section 10.9 on page 28
USB_INTR_STAT	8	13h	-	-	-	Section 10.10 on page 28
USB_INTR_L	8	14h	-	-	-	Section 10.11 on page 29
DEBUG	8	15h	-	-	-	Section 10.12 on page 29
SCRATCH	8	16h to 18h	16h	17h	18h	Section 10.13 on page 30
CARKIT_CTRL	8	19h to 1Bh	19h	1Ah	1Bh	Section 10.14 on page 30
Reserved	8		1Ch to 3Ch			-
PWR_CTRL	8	3Dh to 3Fh	3Dh	3Eh	3Fh	Section 10.15 on page 30

[1] Read (R): A register can be read. Read-only if this is the only mode given.

[2] Write (W): The pattern on the data bus will be written over all bits of a register.

[3] Set (S): The pattern on the data bus is OR-ed with and written to a register.

[4] Clear (C): The pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit will be set to zero (cleared).

10.1 VENDOR_ID_LOW register

Table 14 shows the bit description of the register.

Table 14. VENDOR_ID_LOW - Vendor ID Low register (address R = 00h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ ID_LOW[7:0]	R	CCh*	**Vendor ID Low**: Lower byte of the NXP vendor ID supplied by USB-IF; fixed value of CCh

10.2 VENDOR_ID_HIGH register

Table 15 shows the bit description of the register.

Table 15. VENDOR_ID_HIGH - Vendor ID High register (address R = 01h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ ID_HIGH[7:0]	R	04h*	**Vendor ID High**: Upper byte of the NXP vendor ID supplied by USB-IF; fixed value of 04h

10.3 PRODUCT_ID_LOW register

The bit description of the PRODUCT_ID_LOW register is given in Table 16.

Table 16. PRODUCT_ID_LOW - Product ID Low register (address R = 02h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_LOW[7:0]	R	12h*	**Product ID Low**: Lower byte of the NXP product ID number; fixed value of 12h

10.4 PRODUCT_ID_HIGH register

The bit description of the register is given in Table 17.

Table 17. PRODUCT_ID_HIGH - Product ID High register (address R = 03h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_HIGH[7:0]	R	15h*	**Product ID High**: Upper byte of the NXP product ID number; fixed value of 15h

10.5 FUNC_CTRL register

This register controls UTMI function settings of the PHY. The bit allocation of the register is given in Table 18.

Table 18. FUNC_CTRL - Function Control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	SUSPENDM	RESET	OPMODE[1:0]		TERM SELECT	XCVRSELECT[1:0]	
Reset	0	1	0	0	0	0	0	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 19. FUNC_CTRL - Function Control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit description

Bit	Symbol	Description
7	-	reserved
6	SUSPENDM	**Suspend LOW**: Active-LOW PHY suspend. Places the PHY into low-power mode. The PHY will power down all blocks, except the full-speed receiver, OTG comparators and ULPI interface pins. To come out of low-power mode, the link must assert STP. The PHY will automatically clear this bit when it exits low-power mode. **0b —** Low-power mode **1b —** Powered
5	RESET	**Reset**: Active-HIGH transceiver reset. After the link sets this bit, the PHY will assert DIR and reset the digital core. This does not reset the ULPI interface or the ULPI register set. When the reset is completed, the PHY will deassert DIR and automatically clear this bit, followed by an RXCMD update to the link. The link must wait for DIR to be deasserted before using the ULPI bus. **0b —** Do not reset **1b —** Reset
4 to 3	OPMODE[1:0]	**Operation Mode**: Selects the required bit-encoding style during transmit. **00b —** Normal operation **01b —** Non-driving **10b —** Disable bit-stuffing and NRZI encoding **11b —** Do not automatically add SYNC and EOP when transmitting; must be used only for high-speed packets
2	TERMSELECT	**Termination Select**: Controls the internal 1.5 kΩ full-speed pull-up resistor and 45 Ω high-speed terminations. Control over bus resistors changes, depending on XCVRSELECT[1:0], OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN, as shown in Table 12.
1 to 0	XCVRSELECT [1:0]	**Transceiver Select**: Selects the required transceiver speed. **00b —** Enable the high-speed transceiver **01b —** Enable the full-speed transceiver **10b —** Enable the low-speed transceiver **11b —** Enable the full-speed transceiver for low-speed packets (full-speed preamble is automatically prefixed)

10.6 INTF_CTRL register

The INTF_CTRL register enables alternative interfaces. All of these modes are optional features provided for legacy link cores. Setting more than one of these fields results in undefined behavior. Table 20 provides bit allocation of the register.

Table 20. INTF_CTRL - Interface Control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				CLOCK_ SUSPENDM	CARKIT_ MODE	3PIN_ FSLS_ SERIAL	6PIN_ FSLS_ SERIAL
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 21. INTF_CTRL - Interface Control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit description

Bit	Symbol	Description
7 to 4	-	reserved
3	CLOCK_SUSPENDM	**Clock Suspend**: active-LOW clock suspend. Powers down the internal clock circuitry only. By default, the clock will not be powered in 6-pin serial mode or 3-pin serial mode. Valid only in 6-pin serial mode and 3-pin serial mode. Valid only when SUSPENDM is set to logic 1, otherwise this bit is ignored. **0b —** Clock will not be powered in 3-pin or 6-pin serial mode or UART mode **1b —** Clock will be powered in 3-pin and 6-pin serial mode or UART mode
2	CARKIT_MODE	**Carkit Mode**: Changes the ULPI interface to the carkit interface (UART mode). Bits TXD_EN and RXD_EN in the CARKIT_CTRL register must change as well. The PHY must automatically clear this bit when carkit mode is exited. **0b —** Disable carkit mode **1b —** Enable carkit mode
1	3PIN_FSLS_SERIAL	**3-Pin Full-Speed Low-Speed Serial Mode**: Changes the ULPI interface to a 3-bit serial interface. The ISP1512A will automatically clear this bit when 3-pin serial mode is exited. **0b —** Full-speed or low-speed packets are sent using the parallel interface **1b —** Full-speed or low-speed packets are sent using the 3-pin serial interface
0	6PIN_FSLS_SERIAL	**6-Pin Full-Speed Low-Speed Serial Mode**: Changes the ULPI interface to a 6-bit serial interface. The ISP1512A will automatically clear this bit when 6-pin serial mode is exited. **0b —** Full-speed or low-speed packets are sent using the parallel interface **1b —** Full-speed or low-speed packets are sent using the 6-pin serial interface

10.7 OTG_CTRL register

This register controls various OTG functions of the ISP1512A. The bit allocation of the OTG_CTRL register is given in Table 22.

Table 22. OTG_CTRL - OTG Control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			CHRG_VBUS	DISCHRG_VBUS	DM_PULLDOWN	DP_PULLDOWN	reserved
Reset	0	0	0	0	0	1	1	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 23. OTG_CTRL - OTG Control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit description

Bit	Symbol	Description
7 to 5	-	reserved
4	CHRG_VBUS	**Charge V_{BUS}**: Charges V_{BUS} through a resistor. Used for the V_{BUS} pulsing of SRP. The link must first check that V_{BUS} is discharged (see bit DISCHRG_VBUS), and that both the DP and DM data lines have been LOW (SE0) for 2 ms. **0b —** Do not charge V_{BUS} **1b —** Charge V_{BUS}
3	DISCHRG_VBUS	**Discharge V_{BUS}**: Discharges V_{BUS} through a resistor. If the link sets this bit to logic 1, it waits for an RXCMD indicating that SESS_END has changed from logic 0 to logic 1, and then resets this bit to logic 0 to stop the discharge. **0b —** Do not discharge V_{BUS} **1b —** Discharge V_{BUS}
2	DM_PULLDOWN	**DM Pull Down**: Enables the 15 kΩ pull-down resistor on DM. **0b —** Pull-down resistor is not connected to DM **1b —** Pull-down resistor is connected to DM
1	DP_PULLDOWN	**DP Pull Down**: Enables the 15 kΩ pull-down resistor on DP. **0b —** Pull-down resistor is not connected to DP **1b —** Pull-down resistor is connected to DP
0	-	reserved

10.8 USB_INTR_EN_R register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB_INTR_STAT register change from logic 0 to logic 1. By default, all transitions are enabled. Table 24 shows the bit allocation of the register.

Table 24. USB_INTR_EN_R - USB Interrupt Enable Rising register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				SESS_END_R	SESS_VALID_R	VBUS_VALID_R	HOST_DISCON_R
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 25. USB_INTR_EN_R - USB Interrupt Enable Rising register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit description

Bit	Symbol	Description
7 to 4	-	reserved
3	SESS_END_R	**Session End Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_END.
2	SESS_VALID_R	**Session Valid Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_VLD.
1	VBUS_VALID_R	**V_{BUS} Valid Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on A_VBUS_VLD.
0	HOST_DISCON_R	**Host Disconnect Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on HOST_DISCON.

10.9 USB_INTR_EN_F register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB_INTR_STAT register change from logic 1 to logic 0. By default, all transitions are enabled. See Table 26.

Table 26. USB_INTR_EN_F - USB Interrupt Enable Falling register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				SESS_END_F	SESS_VALID_F	VBUS_VALID_F	HOST_DISCON_F
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 27. USB_INTR_EN_F - USB Interrupt Enable Falling register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit description

Bit	Symbol	Description
7 to 4	-	reserved
3	SESS_END_F	**Session End Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_END.
2	SESS_VALID_F	**Session Valid Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_VLD.
1	VBUS_VALID_F	**V_{BUS} Valid Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on A_VBUS_VLD.
0	HOST_DISCON_F	**Host Disconnect Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on HOST_DISCON.

10.10 USB_INTR_STAT register

This register (see Table 28) indicates the current value of the interrupt source signal.

Table 28. USB_INTR_STAT - USB Interrupt Status register (address R = 13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				SESS_END	SESS_VALID	VBUS_VALID	HOST_DISCON
Reset	X	X	X	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 29. USB_INTR_STAT - USB Interrupt Status register (address R = 13h) bit description

Bit	Symbol	Description
7 to 4	-	reserved
3	SESS_END	**Session End**: Reflects the current value of the session end voltage comparator.
2	SESS_VALID	**Session Valid**: Reflects the current value of the session valid voltage comparator.
1	VBUS_VALID	**V_{BUS} Valid**: Reflects the current value of the V_{BUS} valid voltage comparator.
0	HOST_DISCON	**Host Disconnect**: Reflects the current value of the host disconnect detector.

10.11 USB_INTR_L register

The bits of the USB_INTR_L register are automatically set by the ISP1512A when an unmasked change occurs on the corresponding interrupt source signal. The ISP1512A will automatically clear all bits when the link reads this register, or when the PHY enters low-power mode.

Remark: It is optional for the link to read this register when the clock is running because all signal information will automatically be sent to the link through the RXCMD byte.

The bit allocation of this register is given in Table 30.

Table 30. USB_INTR_L - USB Interrupt Latch register (address R = 14h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				SESS_END_L	SESS_VALID_L	VBUS_VALID_L	HOST_DISCON_L
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 31. USB_INTR_L - USB Interrupt Latch register (address R = 14h) bit description

Bit	Symbol	Description
7 to 4	-	reserved
3	SESS_END_L	**Session End Latch**: Automatically set when an unmasked event occurs on SESS_END. Cleared when this register is read.
2	SESS_VALID_L	**Session Valid Latch**: Automatically set when an unmasked event occurs on SESS_VLD. Cleared when this register is read.
1	VBUS_VALID_L	**V_{BUS} Valid Latch**: Automatically set when an unmasked event occurs on A_VBUS_VLD. Cleared when this register is read.
0	HOST_DISCON_L	**Host Disconnect Latch**: Automatically set when an unmasked event occurs on HOST_DISCON. Cleared when this register is read.

10.12 DEBUG register

The bit allocation of the DEBUG register is given in Table 32. This register indicates the current value of signals useful for debugging.

Table 32. DEBUG - Debug register (address R = 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						LINESTATE1	LINESTATE0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 33. DEBUG - Debug register (address R = 15h) bit description

Bit	Symbol	Description
7 to 2	-	reserved
1	LINESTATE1	**Line State 1**: Contains the current value of LINESTATE 1
0	LINESTATE0	**Line State 0**: Contains the current value of LINESTATE 0

10.13 SCRATCH register

This is a 1-byte empty register for testing purposes, see Table 34.

Table 34. SCRATCH - Scratch register (address R = 16h to 18h, W = 16h, S = 17h, C = 18h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	SCRATCH[7:0]	R/W/S/C	00h	**Scratch**: This is an empty register byte for testing purposes. Software can read, write, set and clear this register. The functionality of the PHY will not be affected.

10.14 CARKIT_CTRL register

This register controls transparent UART mode. This register is only valid when the CARKIT_MODE register bit in the INTF_CTRL register is set. When entering UART mode set the CARKIT_MODE bit, and then set the TXD_EN and RXD_EN bits. After entering UART mode, the ULPI interface is not available. When exiting UART mode, assert the STP pin or perform a hardware reset using the CHIP_SEL pin.

For bit allocation, see Table 35.

Table 35. CARKIT_CTRL - Carkit Control register (address R = 19h to 1Bh, W = 19h, S = 1Ah, C = 1Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				RXD_EN	TXD_EN	reserved	
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 36. CARKIT_CTRL - Carkit Control register (address R = 19h to 1Bh, W = 19h, S = 1Ah, C = 1Bh) bit description

Bit	Symbol	Description
7 to 4	-	reserved; the link must never write logic 1 to these bits
3	RXD_EN	**RXD Enable**: Routes the UART RXD signal from the DP pin to the DATA1 pin. This bit will automatically be cleared when UART mode is exited.
2	TXD_EN	**TXD Enable**: Routes the UART TXD signal from the DATA0 pin to the DM pin. This bit will automatically be cleared when UART mode is exited.
1 to 0	-	reserved; the link must never write logic 1 to these bits

10.15 PWR_CTRL register

This vendor-specific register controls the power feature of the ISP1512A. The bit allocation of the register is given in Table 37.

Table 37. PWR_CTRL - Power Control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			DP_WKPU_EN	BVALID_FALL	BVALID_RISE	reserved	
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 38. PWR_CTRL - Power Control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit description

Bit	Symbol	Description
7 to 5	-	reserved; the link must never write logic 1 to these bits
4	DP_WKPU_EN	**DP Weak Pull-Up Enable**: Enables the weak pull-up resistor on the DP pin ($R_{weakUP(DP)}$) in synchronous mode when V_{BUS} is above the $V_{A\_SESS\_VLD}$ threshold. Note that when the ISP1512A is in UART mode, the DP weak pull-up will be enabled, regardless of the value of this register bit. **0b —** DP weak pull-up is disabled **1b —** DP weak pull-up is enabled when $V_{BUS} > V_{A\_SESS\_VLD}$
3	BVALID_FALL	**BVALID Fall**: Enables RXCMDs for HIGH-to-LOW transitions on BVALID. When BVALID changes from HIGH to LOW, the ISP1512A will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.
2	BVALID_RISE	**BVALID Rise**: Enables RXCMDs for LOW-to-HIGH transitions on BVALID. When BVALID changes from LOW to HIGH, the ISP1512A will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.
1 to 0	-	reserved; the link must never write logic 1 to these bits

11. Limiting values

Table 39. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+5.5	V
$V_{CC(I/O)}$	input/output supply voltage			–0.5	+2.5	V
V_I	input voltage	on pin V_{BUS}	[1]	–0.5	+5.5	V
		on pins CLOCK, STP, DATA[7:0] and CHIP_SEL		–0.5	+2.5	V
		on pins DP and DM	[2]	–0.5	+4.6	V
		on pin XTAL1		–0.5	+2.5	V
V_{ESD}	electrostatic discharge voltage	human body model (JESD22-A114D)		–2000	+2000	V
		machine model (JESD22-A115-A)		–200	+200	V
		charge device model (JESD22-C101-A)		–500	+500	V
		IEC 61000-4-2 contact on pins DP and DM	[3]	–8	+8	kV
I_{lu}	latch-up current			-	100	mA
T_{stg}	storage temperature			–60	+125	°C

[1] When an external series resistor is added to the V_{BUS} pin, it can withstand higher voltages for longer periods of time because the resistor limits the current flowing into the V_{BUS} pin. For example, with an external 1 kΩ resistor, V_{BUS} can tolerate 10 V for at least 5 seconds. Actual performance may vary depending on the resistor used and whether other components are connected to V_{BUS}.

[2] The ISP1512A has been tested according to the additional requirements listed in *Universal Serial Bus Specification Rev. 2.0, Section 7.1.1*. The AC stress test was performed for 24 hours, and the ISP1512A was found to be fully operational after the test completed. The ISP1512A was found to be fully functional after shorting the high-speed DP and DM pins to ground for 24 hours. Transmit and receive were occurring 50 % of the time.

[3] The ISP1512A has been tested in-house according to the IEC 61000-4-2 standard on the DP and DM pins. It is recommended that customers perform their own ESD tests, depending on application requirements.

12. Recommended operating conditions

Table 40. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3.0	3.6	4.5	V
$V_{CC(I/O)}$	input/output supply voltage		1.65	1.8	1.95	V
V_I	input voltage	on pin V_{BUS}	0	-	5.25	V
		on pins CLOCK, STP, DATA[7:0] and CHIP_SEL	0	-	$V_{CC(I/O)}$	V
		on pins DP and DM	0	-	3.6	V
		on pin XTAL1	0	-	1.95	V
T_{amb}	ambient temperature		–40	+25	+85	°C
T_j	junction temperature		–40	-	+125	°C

13. Static characteristics

Table 41. Static characteristics: supply pins

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR(trip)}$	power-on reset trip voltage	on pin REG1V8	0.95	-	1.5	V
I_{CC}	supply current	power-down mode ($V_{CC(I/O)}$ is lost or chip select is deasserted)	-	0.5	10	µA
		full-speed transceiver; bus idle; no USB activity	-	14	-	mA
		full-speed transceiver; 100 % transmission; no inter-packet delay	-	26	-	mA
		high-speed transceiver; 100 % transmission; no inter-packet delay	-	55	-	mA
		low-power mode (SUSPENDM = 0); V_{BUS} valid detector disabled (bits VBUS_VALID_R and VBUS_VALID_F are cleared)				
		for host	-	70	100	µA
		for peripheral	-	240	330	µA
		UART mode; low-speed transceiver; idle	-	750	-	µA
		UART mode; full-speed transceiver; idle	-	600	-	µA
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$	power-down mode (chip select is deasserted)	-	-	10	µA
		ULPI bus idle; 15 pF load on pin CLOCK [1]	-	2	-	mA

[1] The actual value of $I_{CC(I/O)}$ varies depending on the capacitance loading, interface voltage and bus activity. Use the value provided here only for reference.

Table 42. Static characteristics: digital pins (CLOCK, DIR, STP, NXT, DATA[7:0], CHIP_SEL)

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CC(I/O)}$	-	-	V
I_{LI}	input leakage current		−1	-	+1	µA
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = −2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = +2 mA	$V_{CC(I/O)}$ − 0.4	-	-	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC(I/O)}$ − 0.4 V	−4.8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4.2	-	-	mA
Impedance						
Z_L	load impedance		-	50	-	Ω

Table 42. Static characteristics: digital pins (CLOCK, DIR, STP, NXT, DATA[7:0], CHIP_SEL) *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pull up and pull down						
I_{pd}	pull-down current	interface protect enabled; DATA[7:0] pins only; $V_I = V_{CC(I/O)}$	18	55	93	µA
I_{pu}	pull-up current	interface protect enabled; STP pin only; V_I = 0 V	−17	−55	−82	µA
		UART mode; DATA0 pin only	−17	−55	−82	µA
Capacitance						
C_{in}	input capacitance		1.0	3.0	3.3	pF

Table 43. Static characteristics: analog pins (DP, DM)

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Original USB transceiver (full-speed and low-speed)						
Input levels (differential data receiver)						
V_{DI}	differential input sensitivity voltage	$\|V_{DP} - V_{DM}\|$	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	0.8	-	2.5	V
Input levels (single-ended receivers)						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	pull-up on pin DP; R_L = 1.5 kΩ to 3.6 V	0.0	-	0.3	V
V_{OH}	HIGH-level output voltage	pull-down on pins DP and DM; R_L = 15 kΩ to GND	2.8	-	3.6	V
V_{CRS}	output signal crossover voltage	excluding the first transition from the idle state	1.3	-	2.0	V
Termination						
V_{TERM}	termination voltage for upstream facing port pull-up	for 1.5 kΩ pull-up resistor	3.0	-	3.6	V
Resistance						
$R_{UP(DP)}$	pull-up resistance on pin DP		1425	1500	1575	Ω
$R_{weakUP(DP)}$	weak pull-up resistance on pin DP	bit DP_WKPU_EN = 1 and $V_{BUS} > V_{A\_SESS\_VLD}$	104	130	156	kΩ
High-speed USB transceiver (HS)						
Input levels						
V_{HSSQ}	high-speed squelch detection threshold voltage (differential signal amplitude)		100	-	150	mV
V_{HSDSC}	high-speed disconnect detection threshold voltage (differential signal amplitude)		525	-	625	mV
V_{HSDI}	high-speed differential input sensitivity	$\|V_{DP} - V_{DM}\|$	300	-	-	mV

Table 43. Static characteristics: analog pins (DP, DM) *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HSCM}	high-speed data signaling common mode voltage range (guideline for receiver)	includes V_{DI} range	–50	-	+500	mV
Output levels						
V_{HSOI}	high-speed idle level voltage		–10	-	+10	mV
V_{HSOL}	high-speed data signaling LOW-level voltage		–10	-	+10	mV
V_{HSOH}	high-speed data signaling HIGH-level voltage		360	-	440	mV
V_{CHIRPJ}	Chirp J level (differential voltage)		700	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)		–900	-	–500	mV
Leakage current						
I_{LZ}	off-state leakage current		–1.0	-	+1.0	µA
Capacitance						
C_{in}	input capacitance	pin to GND	-	-	5	pF
Resistance						
$R_{DN(DP)}$	pull-down resistance on pin DP		14.25	15	24.8	kΩ
$R_{DN(DM)}$	pull-down resistance on pin DM		14.25	15	24.8	kΩ
Termination						
$Z_{O(drv)(DP)}$	driver output impedance on pin DP	steady-state drive	40.5	45	49.5	Ω
$Z_{O(drv)(DM)}$	driver output impedance on pin DM	steady-state drive	40.5	45	49.5	Ω
Z_{INP}	input impedance exclusive of pull-up/pull-down (for low-/full-speed)		1	-	-	MΩ
UART mode						
Input levels						
V_{IL}	LOW-level input voltage	pin DP	-	-	0.8	V
V_{IH}	HIGH-level input voltage	pin DP	2.35	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	pin DM; I_{OL} = –4 mA	-	-	0.3	V
V_{OH}	HIGH-level output voltage	pin DM; I_{OH} = 4 mA	2.4	-	-	V

Table 44. Static characteristics: analog pin V_{BUS}

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Comparators						
$V_{A\_VBUS\_VLD}$	A-device V_{BUS} valid voltage		4.4	-	4.75	V
$V_{A\_SESS\_VLD}$	A-device session valid voltage	for A-device and B-device	0.8	1.6	2.0	V
$V_{hys(A\_SESS\_VLD)}$	A-device session valid hysteresis voltage	for A-device and B-device	-	100	-	mV
$V_{B\_SESS\_END}$	B-device session end voltage		0.2	-	0.8	V

Table 44. Static characteristics: analog pin V_{BUS} *…continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Resistance						
$R_{UP(VBUS)}$	pull-up resistance on pin V_{BUS}	connect to REG3V3 when CHRG_VBUS = 1	281	680	-	Ω
$R_{DN(VBUS)}$	pull-down resistance on pin V_{BUS}	connect to GND when DISCHRG_VBUS = 1	656	1200	-	Ω
$R_{I(idle)(VBUS)}$	idle input resistance on pin V_{BUS}	not in power-down mode	75	90	100	kΩ
		chip deasserted (power-down mode)	40	-	100	kΩ
		$V_{CC(I/O)}$ lost (power-down mode)	140	-	220	kΩ

Table 45. Static characteristics: resistor reference

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(RREF)}$	output voltage on pin RREF	SUSPENDM = 1	-	1.22	-	V

Table 46. Static characteristics: pin XTAL1

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage		-	-	0.37	V
V_{IH}	HIGH-level input voltage		1.32	-	-	V

14. Dynamic characteristics

Table 47. Dynamic characteristics: reset and power

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{W(POR)}$	internal power-on reset pulse width		0.2	-	-	µs
$t_{w(REG1V8\_H)}$	REG1V8 HIGH pulse width		-	-	2	µs
$t_{w(REG1V8\_L)}$	REG1V8 LOW pulse width		-	-	11	µs
$t_{startup(PLL)}$	PLL start-up time	measured after $t_{d(det)clk(osc)}$	-	-	640	µs
$t_{d(det)clk(osc)}$	oscillator clock detector delay	measured from regulator start-up time	-	-	640	µs
t_{PWRUP}	regulator start-up time	4.7 µF ± 20 % capacitor each on the REG1V8 and REG3V3 pins	-	-	1	ms
t_{PWRDN}	regulator power-down time	4.7 µF ± 20 % capacitor each on the REG1V8 and REG3V3 pins	-	-	100	ms

Table 48. Dynamic characteristics: clock applied to XTAL1

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{i(XTAL1)}$	input frequency on pin XTAL1		-	19.200	-	MHz
$t_{jit(i)(XTAL1)RMS}$	RMS input jitter on pin XTAL1		-	-	200	ps
$\Delta f_{i(XTAL1)}$	input frequency tolerance on pin XTAL1		-	-	200	ppm
$\delta_{i(XTAL1)}$	input duty cycle on pin XTAL1	[1]	-	50	-	%
$t_{r(XTAL1)}$	rise time on pin XTAL1		-	-	5	ns
$t_{f(XTAL1)}$	fall time on pin XTAL1		-	-	5	ns

[1] The internal PLL is triggered only on the positive edge from the crystal oscillator. Therefore, the duty cycle is not critical.

Table 49. Dynamic characteristics: CLOCK output

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{o(CLOCK)}$	output frequency on pin CLOCK		59.970	60.000	60.030	MHz
$t_{jit(o)(CLOCK)RMS}$	RMS output jitter on pin CLOCK		-	-	500	ps
$\delta_{o(CLOCK)}$	output clock duty cycle on pin CLOCK		40	50	60	%

Table 50. Dynamic characteristics: digital I/O pins

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{su}	set-up time	set-up time with respect to the positive edge of CLOCK; input-only pin (STP) and bidirectional pins (DATA[7:0]) as inputs		-	-	6.0	ns
t_h	hold time	hold time with respect to the positive edge of CLOCK; input-only pin (STP) and bidirectional pins (DATA[7:0]) as inputs		0.0	-	-	ns
$t_{d(o)}$	output delay time	output delay with respect to the positive edge of CLOCK; output-only pins (DIR, NXT)		-	-	9.0	ns
		output delay with respect to the positive edge of CLOCK; bidirectional pins as output (DATA[7:0])		-	-	9.0	ns
C_L	load capacitance	DATA[7:0], CLOCK, DIR, NXT, STP	[1]	-	-	20	pF

[1] Load capacitance on each ULPI pin.

Table 51. Dynamic characteristics: analog I/O pins (DP, DM) in USB mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-speed driver characteristics						
t_{HSR}	rise time (10 % to 90 %)	drive 45 Ω to GND on pins DP and DM	500	-	-	ps
t_{HSF}	fall time (10 % to 90 %)	drive 45 Ω to GND on pins DP and DM	500	-	-	ps
Full-speed driver characteristics						
t_{FR}	rise time	C_L = 50 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_{FR}/t_{FF}; excluding the first transition from the idle state	90	-	111.1	%
Low-speed driver characteristics						
t_{LR}	transition time: rise time	C_L = 200 pF to 600 pF; 1.5 kΩ pull up on pin DM enabled; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LF}	transition time: fall time	C_L = 200 pF to 600 pF; 1.5 kΩ pull up on pin DM enabled; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LRFM}	rise and fall time matching	t_{LR}/t_{LF}; excluding the first transition from the idle state	80	-	125	%

Table 52. Dynamic characteristics: analog I/O pins (DP, DM) in transparent UART mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Full-speed driver characteristics (DM only)						
$t_{r(UART)}$	rise time for UART TXD	C_L = 185 pF; 0.37 V to 2.16 V	25	-	75	ns
$t_{f(UART)}$	fall time for UART TXD	C_L = 185 pF; 2.16 V to 0.37 V	25	-	75	ns
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	C_L = 185 pF; DATA0 to DM	-	-	39	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	C_L = 185 pF; DATA0 to DM	-	-	34	ns

Table 52. Dynamic characteristics: analog I/O pins (DP, DM) in transparent UART mode *...continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Low-speed driver characteristics (DM only)						
$t_{r(UART)}$	rise time for UART TXD	C_L = 185 pF; 0.37 V to 2.16 V	100	-	400	ns
$t_{f(UART)}$	fall time for UART TXD	C_L = 185 pF; 2.16 V to 0.37 V	100	-	400	ns
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	C_L = 185 pF; DATA0 to DM	-	-	614	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	C_L = 185 pF; DATA0 to DM	-	-	614	ns
Full-speed receiver characteristics (DP only)						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP to DATA1	-	-	7	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP to DATA1	-	-	7	ns
Low-speed receiver characteristics (DP only)						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP to DATA1	-	-	7	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP to DATA1	-	-	7	ns

Table 53. Dynamic characteristics: analog I/O pins (DP, DM) in serial mode

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver timing						
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	TX_DAT, TX_SE0 to DP, DM; see Figure 10	-	-	20	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	TX_DAT, TX_SE0 to DP, DM; see Figure 10	-	-	20	ns
t_{PHZ}	driver disable delay from HIGH level	TX_ENABLE to DP, DM; see Figure 11	-	-	12	ns
t_{PLZ}	driver disable delay from LOW level	TX_ENABLE to DP, DM; see Figure 11	-	-	12	ns
t_{PZH}	driver enable delay to HIGH level	TX_ENABLE to DP, DM; see Figure 11	-	-	20	ns
t_{PZL}	driver enable delay to LOW level	TX_ENABLE to DP, DM; see Figure 11	-	-	20	ns
Receiver timing						
Differential receiver						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 12	-	-	20	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 12	-	-	20	ns

Table 53. Dynamic characteristics: analog I/O pins (DP, DM) in serial mode *...continued*

V_{CC} = 3.0 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 1.95 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical case refers to V_{CC} = 3.6 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Single-ended receiver						
$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 12	-	-	20	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 12	-	-	20	ns

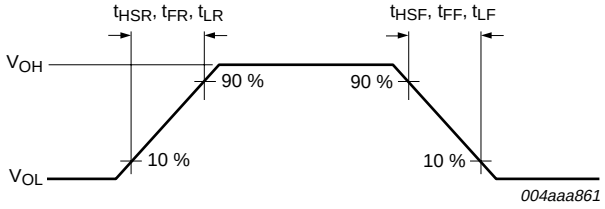


Fig 9. Rise time and fall time

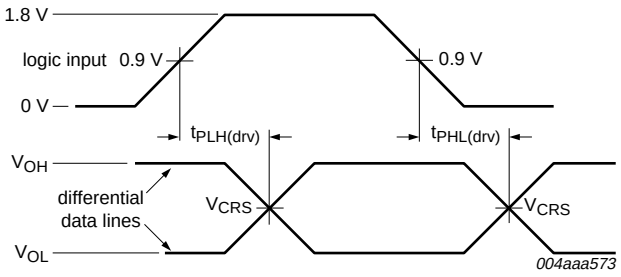


Fig 10. Timing of TX_DAT and TX_SE0 to DP and DM

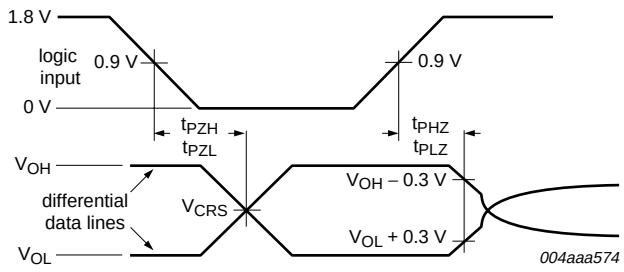


Fig 11. Timing of TX_ENABLE to DP and DM

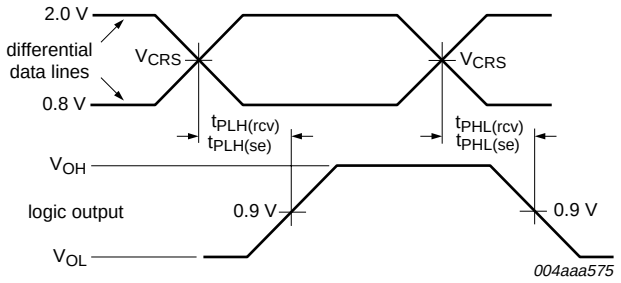


Fig 12. Timing of DP and DM to RX_RCV, RX_DP and RX_DM

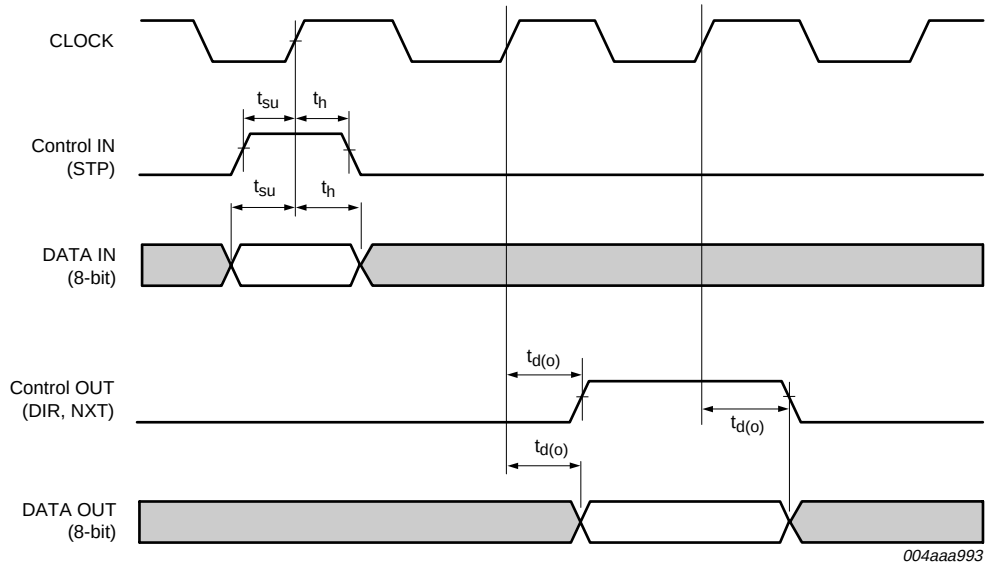


Fig 13. ULPI timing interface

15. Application information

Table 54. Recommended bill of materials

Designator	Application	Part type	Remark
R_{RREF}	mandatory in all applications	12 kΩ ± 1 %	-
$R_{s(VBUS)}$	optional; for peripheral or external 5 V applications	1 kΩ ± 5 %	-
C_{XTAL}	mandatory in output clock mode only	18 pF ± 20 %	-
C_{VBUS}	mandatory for peripherals	1 µF to 10 µF	-
	mandatory for host	96 µF (min)	-
	mandatory for OTG	1 µF to 6.5 µF	-
C_{bypass}	highly recommended for all applications	0.1 µF ± 20 %	-
C_{filter}	highly recommended for all applications	4.7 µF ± 20 %	use a low ESR capacitor (0.2 Ω to 2 Ω) for best performance
D_{ESD}	recommended to prevent damages from ESD	-	IP4359CX4/LF; Wafer-Level Chip-Scale Package (WLCSP); ESD IEC 61000-4-2 level 4; ±15 kV contact; ±15 kV air discharge compliant protection ISP1512A and IP4359CX4/LF together have an IEC 61000-4-2 contact discharge tolerance of ±20 kV
XTAL	mandatory; alternatively pin XTAL1 can be driven by a square wave of the same frequency	19.2 MHz	C_L = 10 pF; R_S < 220 Ω; C_{XTAL} = 18 pF

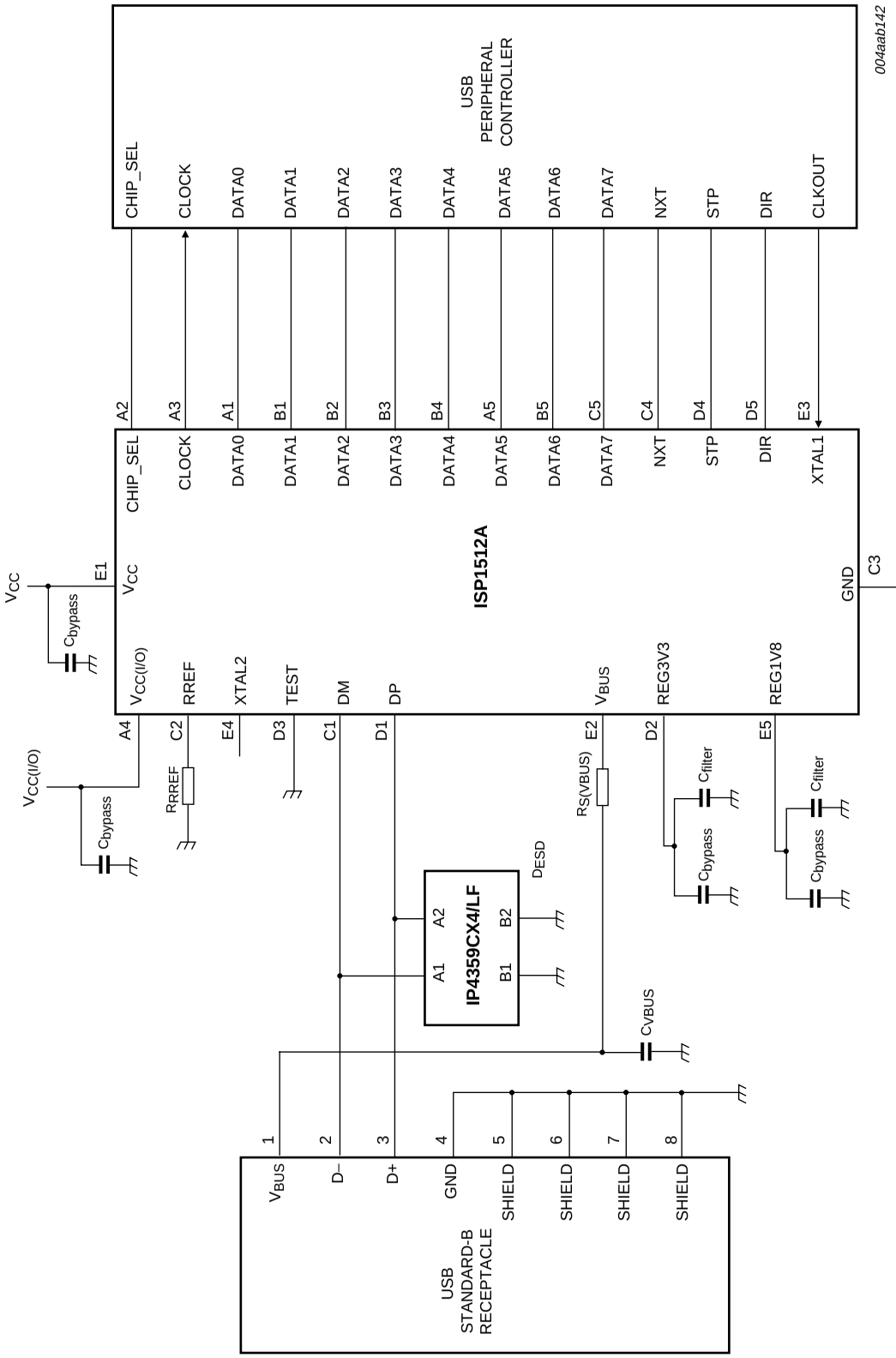


Fig 14. Using the ISP1512A with a standard USB peripheral controller

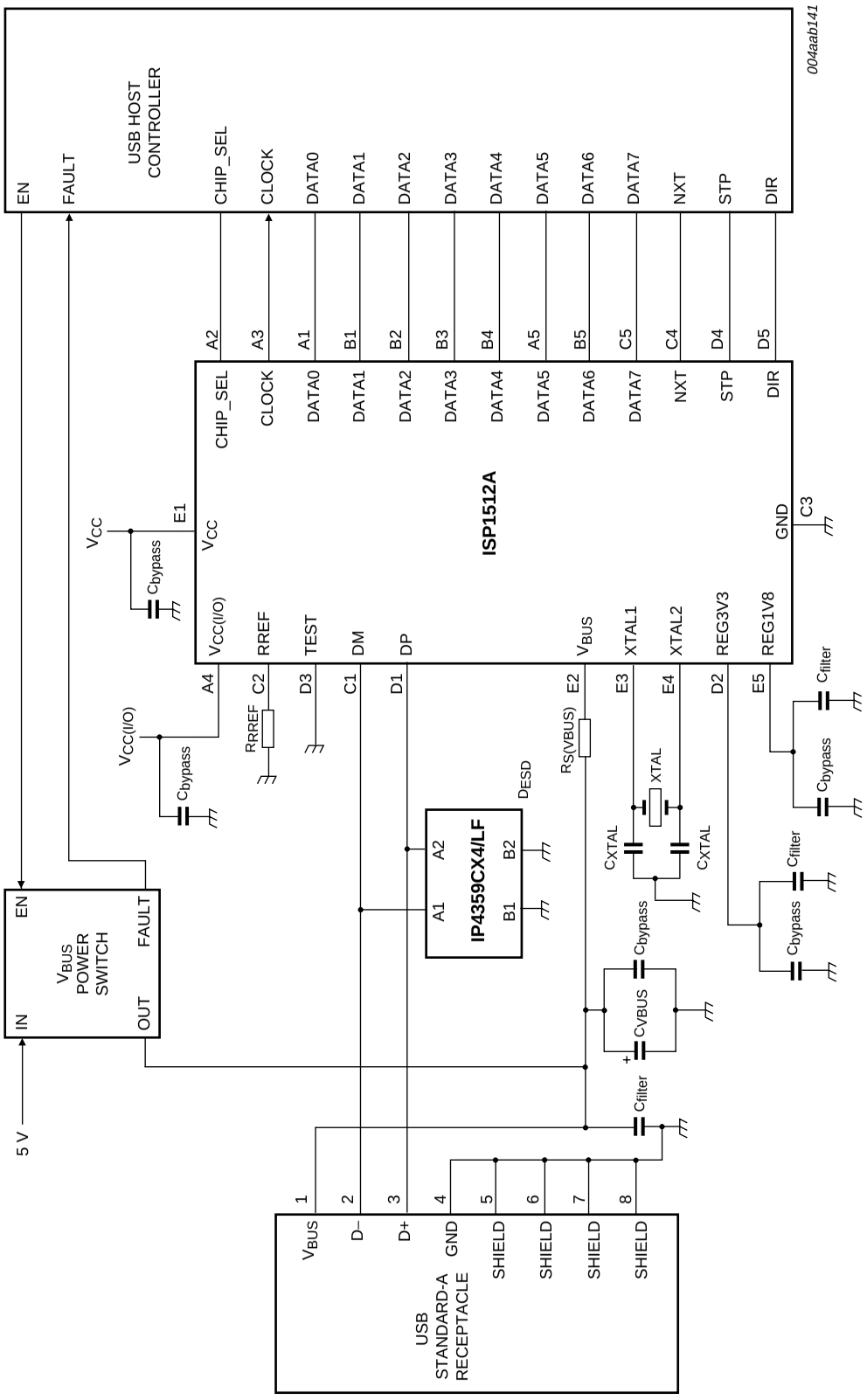


Fig 15. Using the ISP1512A with a standard USB host controller

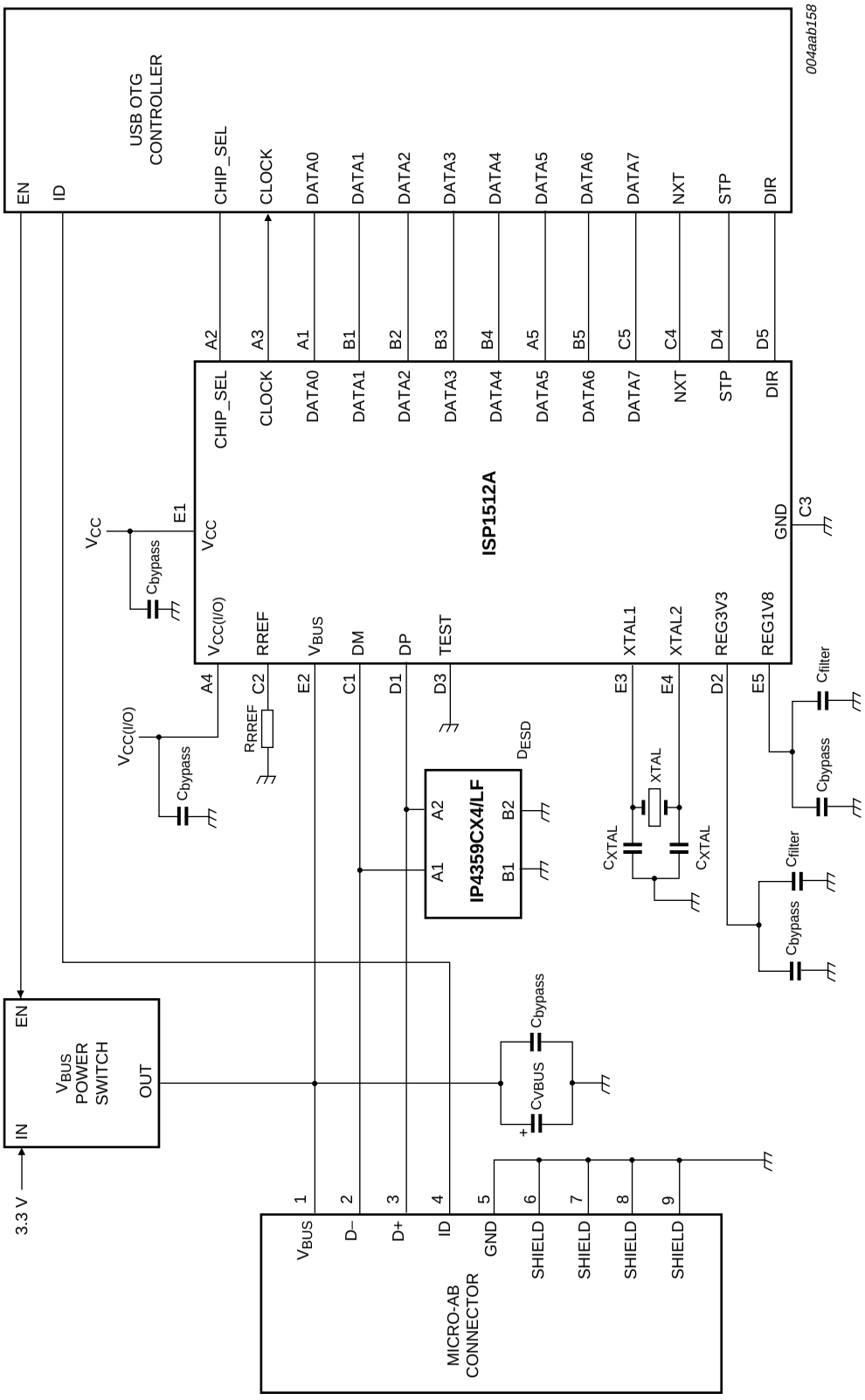
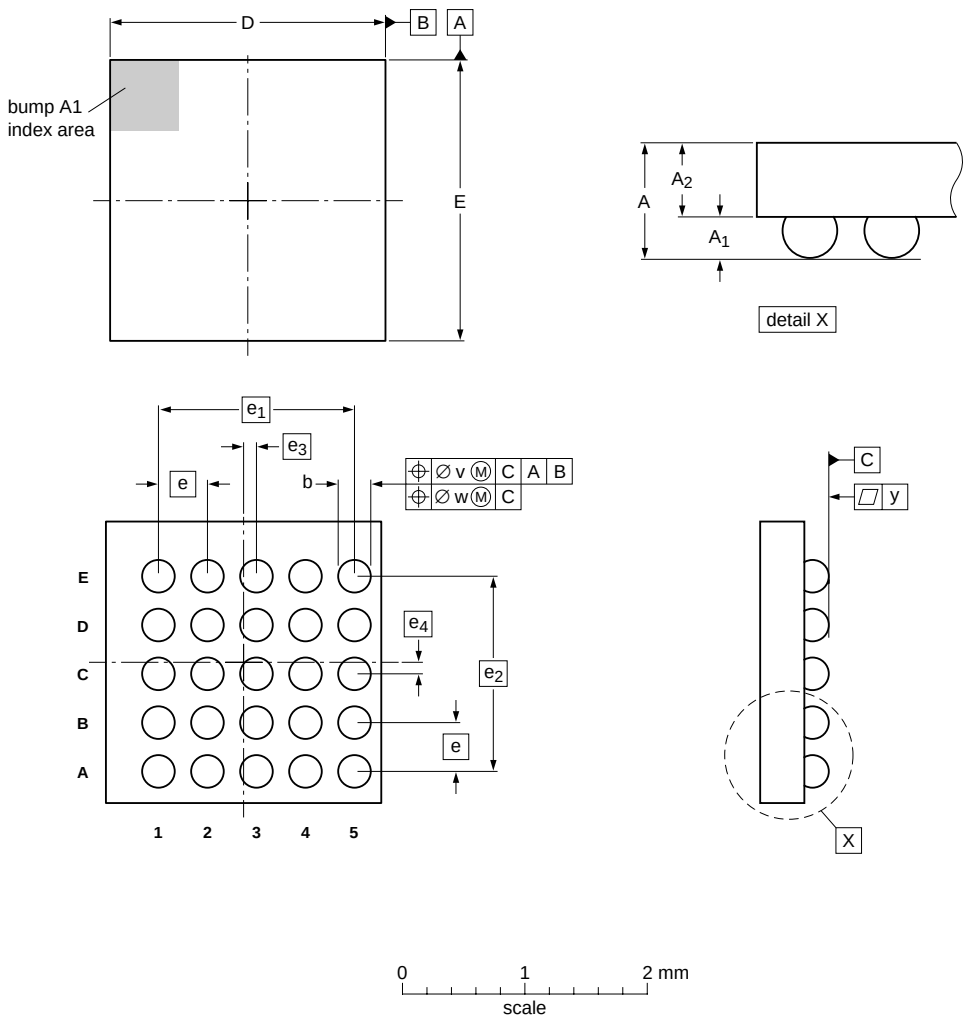


Fig 16. Using the ISP1512A with a standard USB OTG controller

16. Package outline

WLCSP25: wafer level chip-size package; 25 bumps; 2.24 x 2.21 x 0.6 mm **ISP1512xUK**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	e_3	e_4	v	w	y
mm	max	0.6	0.22	0.38	0.30	2.27	2.24	0.4	1.6	1.6	0.105	0.09	0.01	0.04	0.03
	nom														
	min		0.18	0.34	0.26	2.21	2.18								

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
ISP1512xUK						~~08-07-03~~ 08-07-08

Fig 17. Package outline ISP1512xUK (WLCSP25)

17. Soldering of WLCSP packages

17.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

17.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

17.3 Reflow soldering

Key characteristics in reflow soldering are:

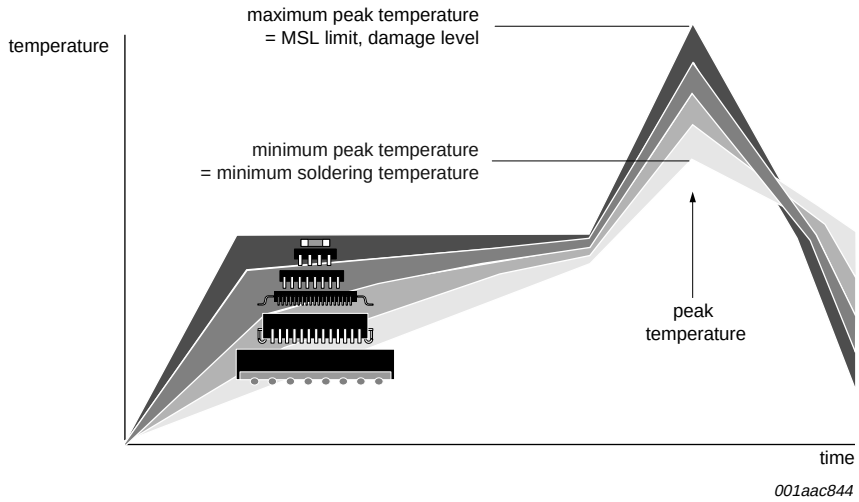
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 55

Table 55. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

17.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

17.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

17.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

17.3.4 Cleaning

Cleaning can be done after reflow soldering.

18. Abbreviations

Table 56. Abbreviations

Acronym	Description
ASIC	Application-Specific Integrated Circuit
ATX	Analog USB Transceiver
CDM	Charge Device Model
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
ESR	Effective Series Resistance
FPGA	Field Programmable Gate-Array
HBM	Human Body Model
IEC	International Electrotechnical Commission
MM	Machine Model
NRZI	Non-Return-to-Zero Inverted
OTG	On-The-Go
PDA	Personal Digital Assistant
PHY	Physical
PID	Packet Identifier
PLL	Phase-Locked Loop
POR	Power-On Reset
RoHS	Restriction of Hazardous Substances
RXCMD	Receive Command
RXD	Receive Data
SDR	Single Data Rate
SE0	Single-Ended Zero
SOC	System-On-Chip
SRP	Session Request Protocol
SYNC	Synchronous
TTL	Transistor-Transistor Logic
TXCMD	Transmit Command

Table 56. Abbreviations *...continued*

Acronym	Description
TXD	Transmit Data
UART	Universal Asynchronous Receiver-Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB-IF	USB Implementers Forum
UTMI	USB Transceiver Macrocell Interface
UTMI+	USB Transceiver Macrocell Interface Plus
WLCSP	Wafer-Level Chip-Scale Package

19. Glossary

A-device — An OTG device with an attached micro-A plug.

B-device — An OTG device with an attached micro-B plug.

Link — ASIC, SOC or FPGA that contains the USB host or peripheral core.

PHY — Physical layer containing USB transceiver.

20. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3

[3] UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1

[4] UTMI+ Specification Rev. 1.0

[5] USB 2.0 Transceiver Macrocell Interface (UTMI) Specification Ver. 1.05

[6] Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) (JESD22-A114D)

[7] Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) (JESD22-A115-A)

[8] Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components (JESD22-C101-C)

[9] Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test (IEC 61000-4-2)

21. Revision history

Table 57. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1512A_1	20080731	Preliminary data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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24. Tables

25. Figures

26. Contents

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