

16 Pin DIP 3 Bit Programmable TTL Delay Lines With I/O Completely Buffered

PART NUMBER	MIN DELAY (INHERENT) ± 2 nS	TOTAL DELAY* nS	DELAY per STEP **	OUTPUT DELAY TIME PROGRAMMING (nS)							
				DATA INPUT (CBA)							
				000	001	010	011	100	101	110	111
EPA563-1A	14	7	1 \pm 0.5 nS	14	15	16	17	18	19	20	21
EPA563-2A	14	14	2 \pm 0.5 nS	14	16	18	20	22	24	26	28
EPA563-3A	14	21	3 \pm 0.6 nS	14	17	20	23	26	29	32	35
EPA563-4A	14	28	4 \pm 0.8 nS	14	18	22	26	30	34	38	42
EPA563-5A	14	35	5 \pm 1.0 nS	14	19	24	29	34	39	44	49
EPA563-6A	14	42	6 \pm 1.0 nS	14	20	26	32	38	44	50	56
EPA563-7A	14	49	7 \pm 1.0 nS	14	21	28	35	42	49	56	63
EPA563-8A	14	56	8 \pm 1.0 nS	14	22	30	38	46	54	62	70
EPA563-9A	14	63	9 \pm 1.0 nS	14	23	32	41	50	59	68	77
EPA563-10A	14	70	10 \pm 1.0 nS	14	24	34	44	54	64	74	84

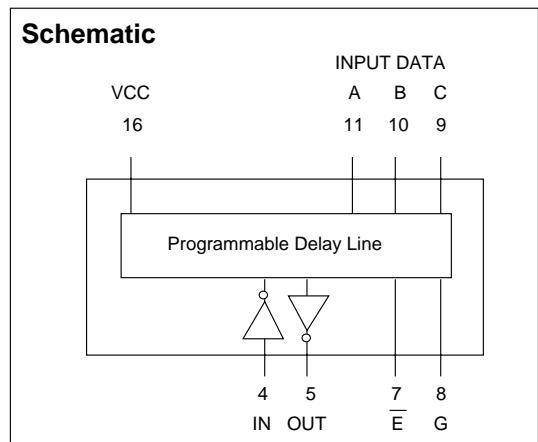
Total delay tolerances ± 2 nS or $\pm 5\%$ whichever is greater.

All delays measured at 1.5V level on leading edge, no load (enable = "0"), at 25° C / 5.0 Vdc.

*This value does not include the inherent delay.

**Tolerance is from step to step.

DC Electrical Characteristics			Min	Max	Unit
Parameter	Test Conditions				
V_{OH}	High-Level Output Voltage	$V_{CC} = \text{min. } V_{IL} = \text{max. } I_{OH} = \text{max}$	2.7		V
V_{OL}	Low-Level Output Voltage	$V_{CC} = \text{min. } V_{IH} = \text{min. } I_{OL} = \text{max}$		0.5	V
V_{IK}	Input Clamp Voltage	$V_{CC} = \text{min. } I_I = I_{IK}$		-1.2	V
I_{IH}	High-Level Input Current	$V_{CC} = \text{max. } V_{IN} = 2.7V$		50	μA
		$V_{CC} = \text{max. } V_{IN} = 5.25V$		1.0	mA
I_{IL}	Low-Level Input Current	$V_{CC} = \text{max. } V_{IN} = 0.5V$		-2	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{max. } V_{OUT} = 0.$ (One output at a time)	-40	-100	mA
I_{CCH}	High-Level Supply Current	$V_{CC} = \text{max. } V_{IN} = \text{OPEN}$		130	mA
I_{CCL}	Low-Level Supply Current	$V_{CC} = \text{max. } V_{IN} = 0$		150	mA
T_{RO}	Output Rise Time	$T_d \leq 500$ nS (0.75 to 2.4 Volts)		4	nS
N_H	Fanout High-Level Output	$V_{CC} = \text{max. } V_{OH} = 2.7V$		20 TTL LOAD	
N_L	Fanout Low-Level Output	$V_{CC} = \text{max. } V_{OL} = 0.5V$		10 TTL LOAD	



Recommended Operating Conditions			Min	Max	Unit
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IH}	High-Level Input Voltage		2.0		V
V_{IL}	Low-Level Input Voltage			0.8	V
I_{IK}	Input Clamp Current			-18	mA
I_{OH}	High-Level Output Current			-1.0	mA
I_{OL}	Low-Level Output Current			20	mA
PW^*	Pulse Width of Total Delay		100		%
d^*	Duty Cycle			20	%
T_A	Operating Free-Air Temperature		0	+70	°C

*These two values are inter-dependent.

Input Pulse Test Conditions			Unit
E_{IN}	Pulse Input Voltage		3.2 Volts
P_W	Pulse Width % of Total Delay		55 %
T_{RI}	Pulse Rise Time (0.75 - 2.4 Volts)		2.0 nS
F_{RR}	Pulse Repetition Rate @ $T_d \leq 500$ nS		9.09 MHz
V_{CC}	Supply Voltage		5.0 Volts

