

S518324-44Z

UPSTREAM CATV AMPLIFIER



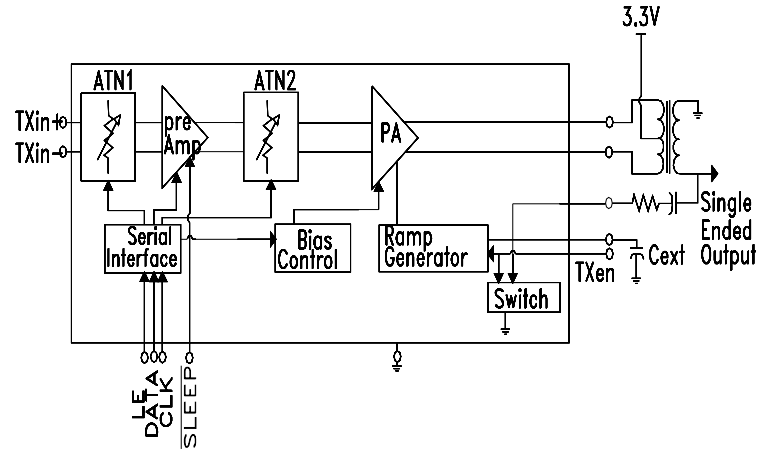
FEATURES

- **SINGLE 3.3 V SUPPLY OPERATION**
- **LOW POWER CONSUMPTION:**
143 mA typical
- **63 dB DYNAMIC RANGE:**
-2.5 to 61 dBmV output
- **EXCELLENT LINEARITY**
2nd/3rd Harmonics >60 dBc typical
- **PROGRAMMABLE GAIN IN 0.5 dB STEPS**
- **ULTRA LOW ON/OFF TRANSIENTS**
- **DOCSIS 2.0 Plus and RoHS compliant**

DESCRIPTION

The S518324 is a high performance, CMOS, low power programmable power amplifier designed for use in CATV upstream applications. The amplifier operates over a frequency range from 5 to 65 MHz and has a maximum output of 61 dBmV. A 3-wire serial interface controls the gain over a 63.5 dB range in 0.5 dB steps. The S518324 is available in a thermally enhanced QFN20 4x4. The product is DOCSIS and RoHS compliant.

FUNCTIONAL DIAGRAM



APPLICATIONS

- Set-Top Boxes
- Cable Telephony
- Cable Modems
- CATV Infrastructure

RF ELECTRICAL CHARACTERISTICS (TA = 25°C, VDD = 3.3 V, unless otherwise specified)

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
RF Performance					
Av	Gain FIN = 5 MHz, Gain Code = 127	dB	26	31	
Av	Gain FIN = 65 MHz, Gain Code = 127	dB	25.2	28	
	Gain Flatness, FIN = 5 to 42 MHz	dB		1.75	2
	Gain Flatness, FIN = 5 to 65 MHz	dB		3.0	3.5
	Attenuation Range, Gain Code = 0 to 127	dB		63.5	
	Attenuation Step Size, Gain Code = 0 to 127	dB		0.5	
	Output Return Loss, 5 to 65 MHz	dB		15	10
	Isolation, 5 to 65 MHz, TXEN = 0 (Transmit Disable Mode)	dB		-90	
	Transmit Mode Noise, 5 to 65 MHz, BW = 160 KHz, Gain Code = 127 to 96	dBmV		-30	-28
	Transmit Mode Noise, 5 to 65 MHz, BW = 160 KHz, Gain Code = 95 to 32	dBmV		-45	-43
	Transmit Mode Noise, 5 to 65 MHz, BW = 160 KHz, Gain Code = 31 to 0	dBmV		-52	-50
	Transmit Disable Mode Noise, 5 to 65 MHz, BW = 160 KHz, TXEN = 0	dBmV		-68	
HD2	2 nd Harmonic Distortion, VOUT = 60 dBmV, 5 to 65 MHz	dBc		60	
HD3	3 rd Harmonic Distortion, VOUT = 60 dBmV, 5 to 65 MHz	dBc		58	

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DC ELECTRICAL CHARACTERISTICS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
DC Performance					
V _{DD}	Supply Voltage	V	3.2	3.3	3.5
I _{DD}	Supply Current	Gain Code = 127		143	160
	TXEN = 1, D7 = 0, SLEEP = 1	Gain Code = 63 to 0		70	
I _{DD}	Supply Current, TXEN = 0, D7 = 0, SLEEP = 1	mA		30	
I _{DD}	Supply Current, D7 = 1 or SLEEP = 0	uA			10
Logic Inputs					
V _{INH}	Input High Voltage	V	V _{DD} - 0.4		
V _{INL}	Input Low Voltage	V			0.4

ABSOLUTE MAXIMUM RATINGS

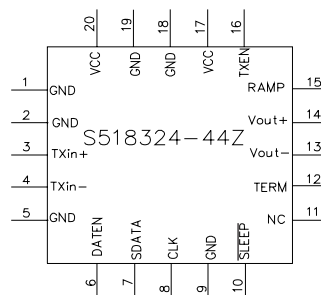
(T_c = 25°C unless otherwise noted)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V _{DD}	Supply Voltage	V	-0.3 to +3.6
T _{OP}	Operating Temperature	°C	-40 to +85
T _{STG}	Storage Temperature	°C	-65 to 150
T _{Jmax}	Junction Temperature	°C	150
θ _{Jc}	Thermal Resistance	°C/W	34

Note:

- Operation in excess of any one of these parameters may result in permanent damage.

PIN ASSIGNMENTS

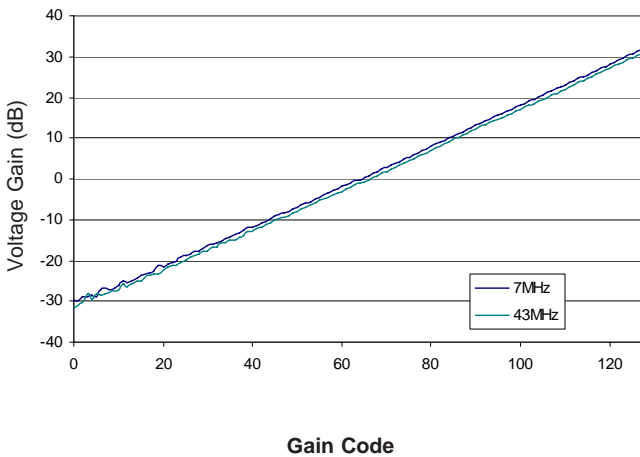


PIN FUNCTIONS

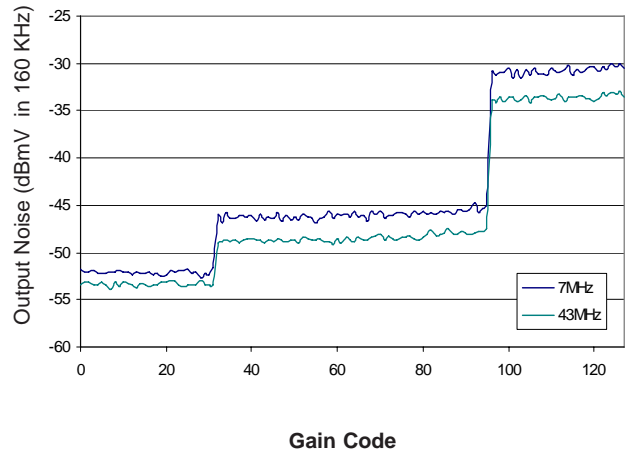
QFN 20	PIN NAME	DESCRIPTION
1	GND	Ground
2	GND	Ground
3	VIN+	Positive input.
4	VIN-	Negative input.
5	GND	Ground
6	LE	Serial Interface Enable. TTL compatible input. See Serial Interface section.
7	DATA	Serial Interface Data. TTL compatible input. See Serial Interface section
8	CLK	Serial Interface Clock. TTL compatible input. See Serial Interface section
9	GND	Ground
10	SLEEP	Hardware Shutdown. For fast shutdown, TXEN must be low when SLEEP is set low.
11	NC	No Connect
12	TERM	A resistor of 60ohms and a bypass cap must be connected in series to the output of the transformer to ensure proper output impedance when output-amp is disable.
13	VOUT-	Negative output of the output-amp stage. Along with VOUT+, the two ports form a differential impedance of 75 ohms.
14	VOUT+	Positive output of the output-amp stage. Along with VOUT-, the two ports form a differential impedance of 75 ohms.
15	RAMP	An external capacitor to ground is connected to control the ramp-up and ramp-down during transmit enable and disable.
16	TXEN	Transmit enable. Drive TXEN high to turn on the output stage.
17	VCC	3.3V
18	GND	Ground
19	GND	Ground
20	VCC	3.3V

TYPICAL PERFORMANCE CURVES

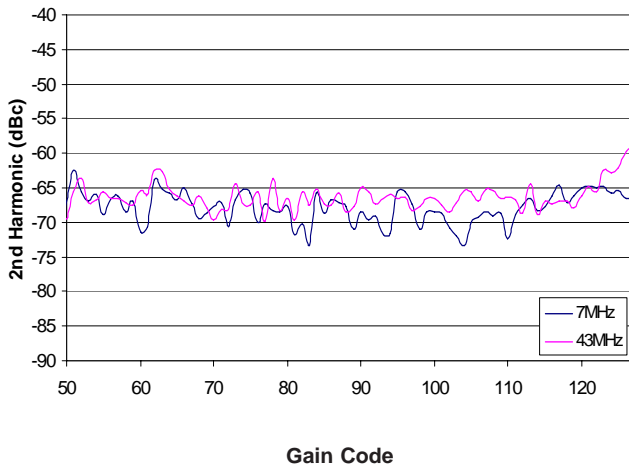
VOLTAGE GAIN vs. GAIN CODE



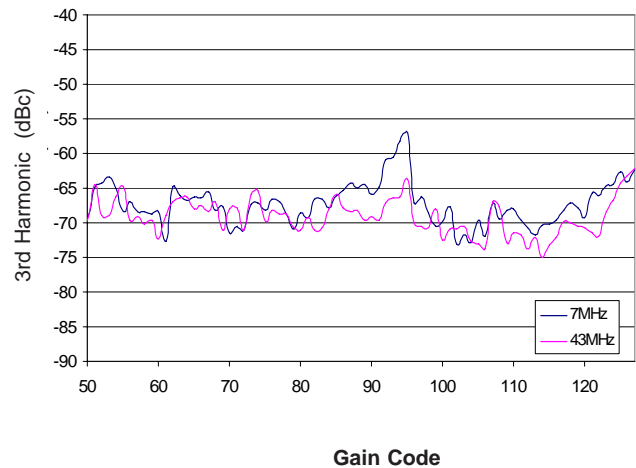
TRANSMIT NOISE vs. GAIN CODE



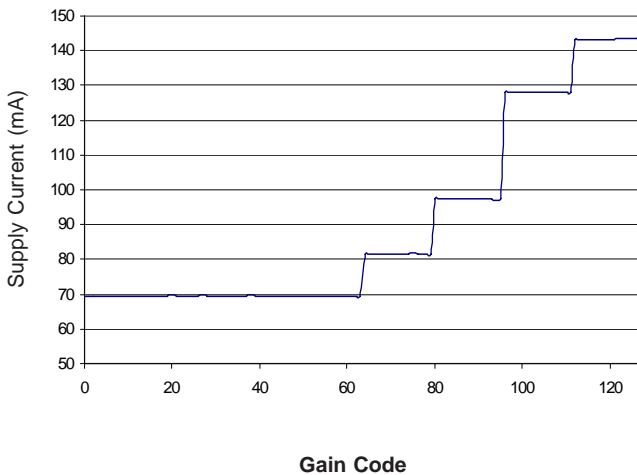
2ND HARMONIC vs. GAIN CODE
(POUT=60dBmV @ GCW=127)



3RD HARMONIC vs. GAIN CODE
(POUT = 60dBmV @ GCW = 127)



SUPPLY CURRENT vs. GAIN CODE



FUNCTIONAL DESCRIPTION

Upstream CATV Amplifier

The upstream CATV amplifier consists of an input attenuator (ATTN1), pre-amp, intermediate attenuator (ATTN2), power amp, serial data interface, bias control, ramp generator, and a switch. The amplifier and the attenuator blocks are capable of providing a gain range of 63.5 dB with 0.5 dB steps across the specified frequencies of operation. The gain and current of the whole chain is determined by a 7 bit word programmed using the serial data interface.

Input Interface

The differential input impedance of the upstream CATV amplifier is 150 ohms. The input anti-aliasing filter should be designed to the same impedance for proper operation. The output impedance of the DAC should also be set accordingly. In order to achieve the specified performance, the inputs should be driven differentially.

Output Interface

The differential output impedance of the upstream CATV amplifier is 75 ohms provided that the suggested value of the shunt feedback resistor of the power amp stage is used. The differential output is converted to a single-ended output with a 1:1 turn ratio transformer.

Switch

During transmit disable mode, the 75 ohm output impedance is maintained by switching in a shunt 60 ohm resistor connected from the single-ended output of the transformer to Pin 12. The switch is toggled by the TXen pin, SLEEP pin, and D7 bit. When TXEN and SLEEP are high and D7 = 0 (transmit mode), the switch is open. It is closed when TXEN or SLEEP is low or D7 = 1.

Power Amp (PA)

The power amplifier stage is a Class A differential amplifier with shunt feedback and series feedback. It is capable of providing an output level of 61 dBmV. The 3.3 V bias of the PA stage comes from the center-tap of the 1:1 turn ratio transformer. The transformer will suppress the even-order distortion and the transients caused by enabling and disabling the PA.

Ramp Generator

This block is a simple RC charging circuit consisting of an internal 1K ohm resistor and an external capacitor Cext. This circuit controls the ramp up and down time of the PA stage during bursts.

Bias Control

The bias control sets the current of the PA stage at various gain states. In the lower gain states, the current of the PA is reduced and overall power consumption decreases.

Serial Interface

The serial interface becomes active when LE (latch enable) is low. The overall gain, current, and chip shutdown are determined by the programming of the bits D0 - D7. See Table 1, Table 2, Table 3, and Serial-Interface Timing Diagram for programming details. For fast shutdown, TXEN must be low when D7 is set low.

FUNCTIONAL DESCRIPTION (CON'T)

Table 1. Attenuator States

TXen	SLEEP	D7	D6	D5	D4	D3	D2	D1	D0	Gain Code (Decimal)	State
0	0	X	X	X	X	X	X	X	X	X	Shutdown
0	1	X	X	X	X	X	X	X	X	X	Transmit Disable
0	X	1	X	X	X	X	X	X	X	X	Shutdown
1	1	0	1	1	1	1	1	1	1	127	Av = 30.0 dB
1	1	0	1	1	1	1	1	0	1	125	Av = 29.0 dB
1	1	0	1	1	1	1	0	0	1	121	Av = 27.0 dB
1	1	0	1	1	0	0	1	0	1	101	Av = 17.0 dB
1	1	0	1	1	0	0	0	0	1	97	Av = 15.0 dB
1	1	0	1	0	1	1	1	1	1	95	Av = 14.0 dB
1	1	0	1	0	1	1	1	0	1	93	Av = 13.0 dB
1	1	0	1	0	1	0	0	0	1	81	Av = 7.0 dB
1	1	0	1	0	0	0	0	0	1	65	Av = -1.0 dB
1	1	0	0	1	1	1	1	1	1	63	Av = -2.0 dB
1	1	0	0	1	1	1	1	0	1	61	Av = -3.0 dB
1	1	0	0	1	0	1	0	0	1	41	Av = -13.0 dB
1	1	0	0	1	0	0	0	0	1	33	Av = -17.0 dB
1	1	0	0	0	1	1	1	1	1	31	Av = -18.0 dB
1	1	0	0	0	1	1	1	0	1	29	Av = -19.0 dB
1	1	0	0	0	1	0	1	0	1	21	Av = -23.0 dB
1	1	0	0	0	0	0	0	0	1	1	Av = -33.0 dB
1	1	0	0	0	0	0	0	0	0	0	Av = -33.5 dB

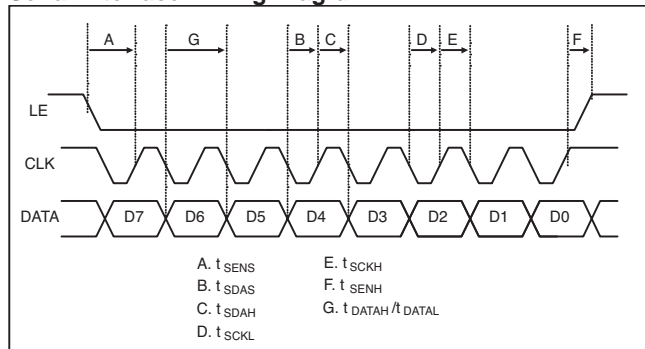
Table 2. Attenuator Values

BIT	ATTENUATION (dB)
D0	0.5
D1	1.0
D2	2.0
D3	4.0
D4	8.0
D5	16.0
D6	32.0

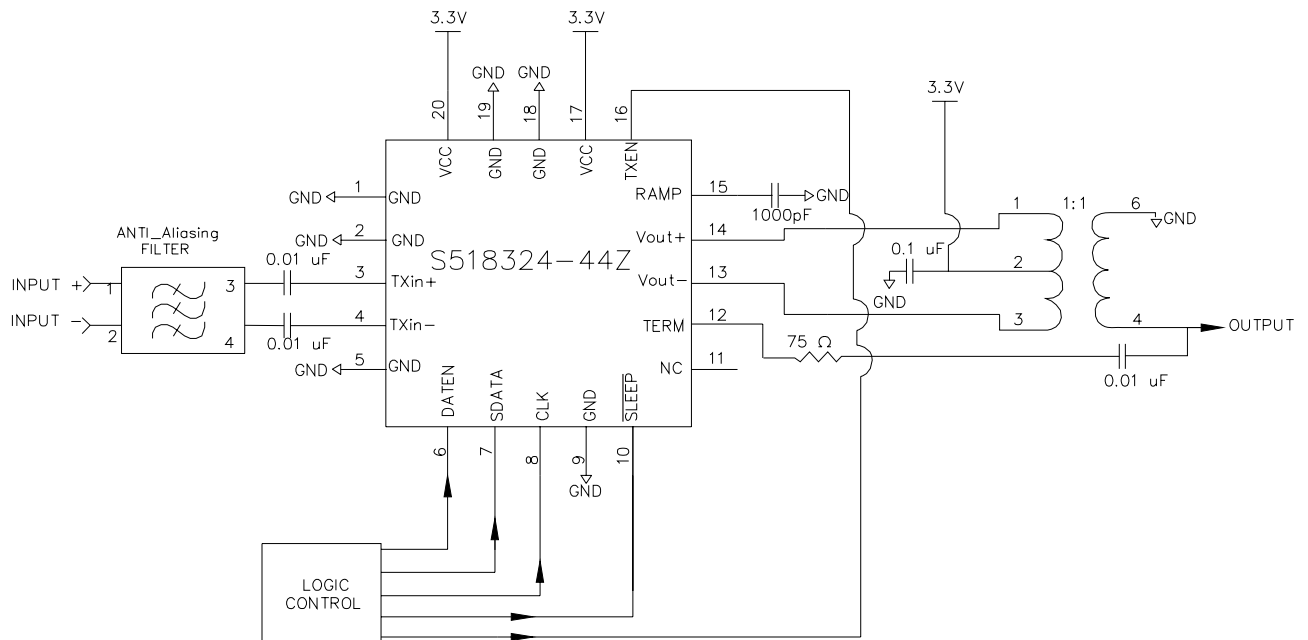
Table 3. Serial-Interface Control Word

BIT	MNEMONIC	DESCRIPTION
MSB 7	D7	Shutdown (TXEN = 0)
6	D6	Gain Control, Bit 6
5	D5	Gain Control, Bit 5
4	D4	Gain Control, Bit 4
3	D3	Gain Control, Bit 3
2	D2	Gain Control, Bit 2
1	D1	Gain Control, Bit 1
LSB 0	D0	Gain Control, Bit 0

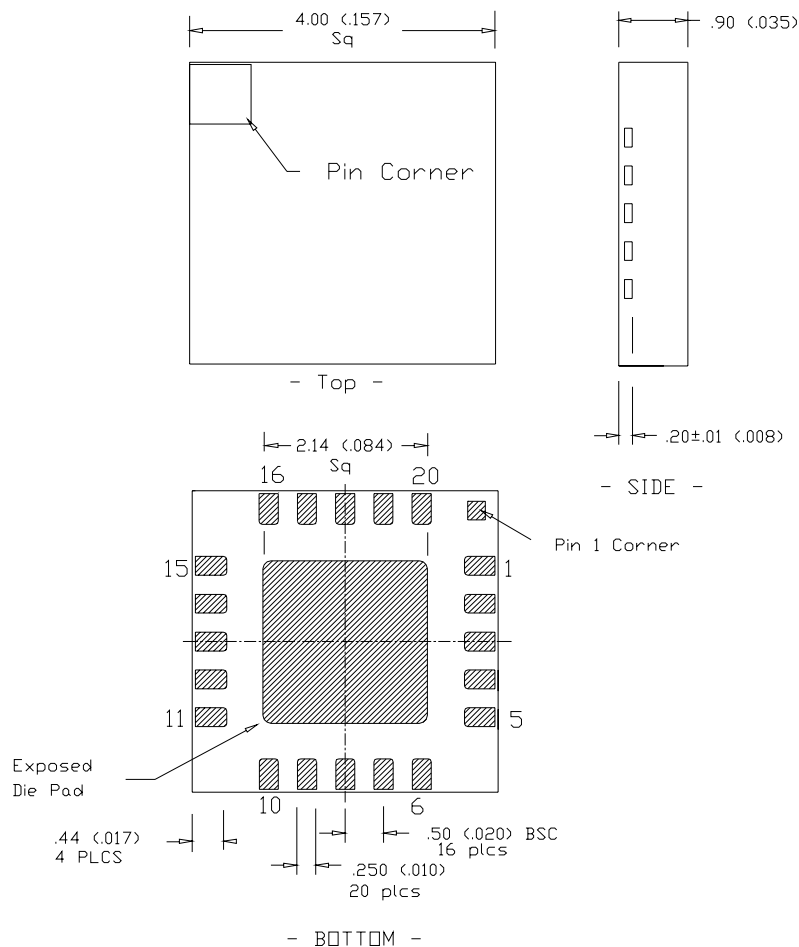
Serial-Interface Timing Diagram



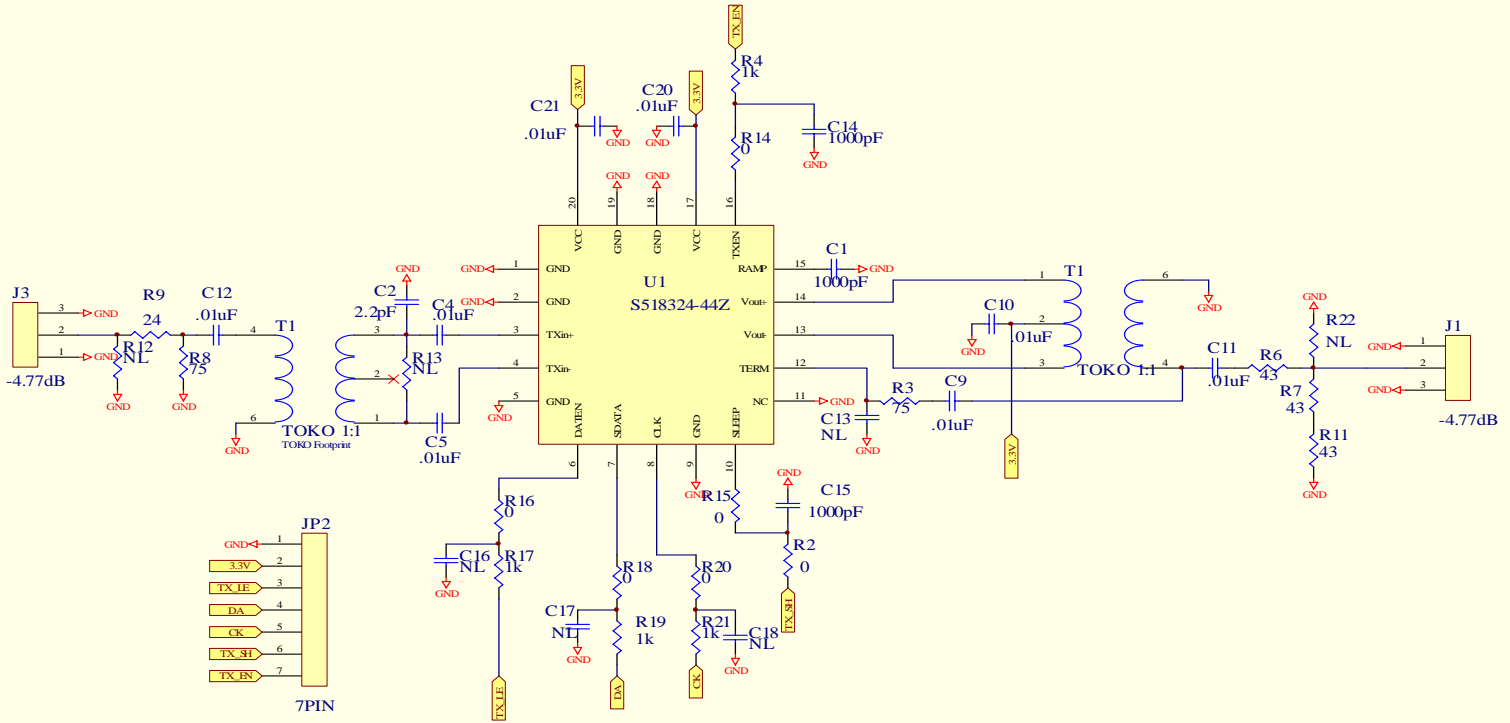
TYPICAL APPLICATION CIRCUIT



PACKAGE INFORMATION QFN 20 (Units in mm)



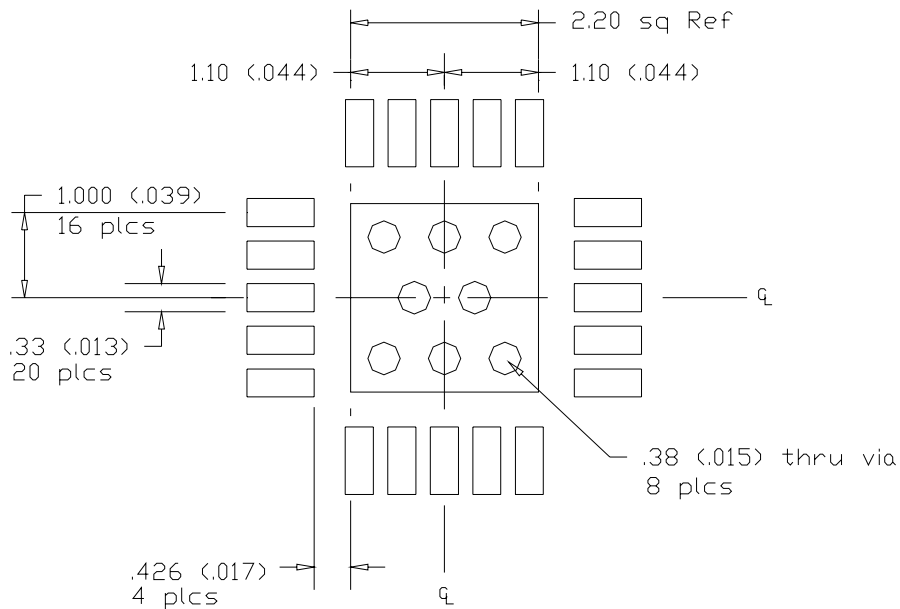
Evaluation Board Schematic



PACKAGE INFORMATION (CONT)

1. Dimensions and tolerances conform to ASME Y14.5-1994.
2. All dimensions are in millimeters. All angles are in degrees.
3. The exposed thermal pad is also an electrical ground .

LAND PATTERN FOR TERMINALS AND THERMAL/GROUND PAD



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