PO74HSTL85331A

3.3V 1:4 Crystal Oscillator/
Differential Clock or Data Fanout Buffer

03/01/07

700MHz HSTL Potato Chip

FEATURES:

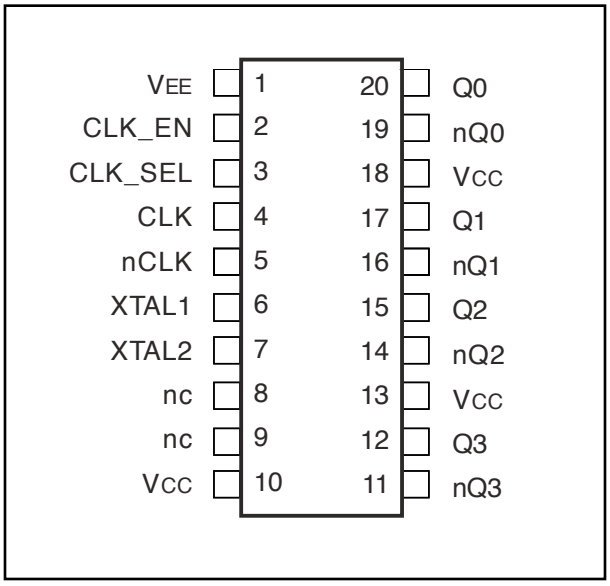
. Patented Technology
. Four HSTL differential outputs
. Selectable differential CLK, nCLK or crystal inputs
. CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
. Operating frequency up to 700MHz with 2pf load
. Operating frequency up to 550MHz with 5pf load
. Operating frequency up to 400MHz with 15pf load
. Very low output pin to pin skew < 50ps
. 3.3-ns propagation delay (typical)
. 2.4V to 3.6V power supply
. Industrial temperature range: –40°C to 85°C
. 20-pin TSSOP package

DESCRIPTION:

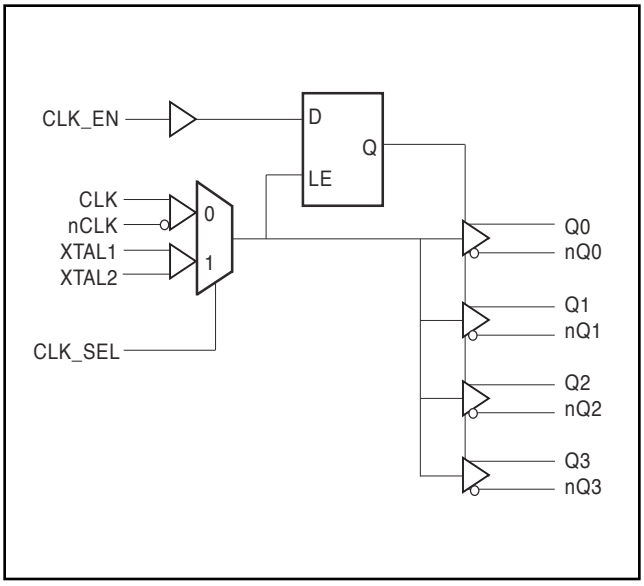
The PO74HSTL85331A is a low skew, high performance 1-to-4 Crystal Oscillator/Differential-to-3.3V HSTL fanout buffer of High Performance Clock Solutions from PotatoSemi. The PO74HSTL85331A has selectable differential clock or crystal inputs. The CLK, nCLK pair can accept most standard differential input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the PO74HSTL85331A ideal for those applications demanding well defined performance and repeatability.

Pin Configuration



Logic Block Diagram



Pin Definitions

Number	Name	Type		Description
1	V_{EE}	Power		GND Pin
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When LOW, selects CLK, nCLK input. When HIGH, selects XTAL input. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup	Inverting differential clock input.
6	XTAL1	Input	Pulldown	Crystal oscillator input.
7	XTAL2	Input	Pullup	Crystal oscillator input.
8, 9	nc	Unused		No connect.
10, 13, 18	V_{CC}	Power		Positive supply pins.
11, 12	nQ3, Q3	Output		Differential clock outputs. HSTL interface levels.
14, 15	nQ2, Q2	Output		Differential clock outputs. HSTL interface levels.
16, 17	nQ1, Q1	Output		Differential clock outputs. HSTL interface levels.
19, 20	nQ0, Q0	Output		Differential clock outputs. HSTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin characteristics, for typical values.

Function Table

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0:Q3	nQ0:nQ3
0	0	CLK, nCLK	Disabled; LOW	Disabled; HIGH
0	1	XTAL1, XTAL2	Disabled; LOW	Disabled; HIGH
1	0	CLK, nCLK	Enabled	Enabled
1	1	XTAL1, XTAL2	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled folowing a rising and falling input clock or crystal oscillator edge as shown in *Figure 1*.
In the active mode, the state of the outputs are a function of the CLK, nCLK and XTAL1, XTAL2 inputs as described in Table 3B.

Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			88		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			88		KΩ

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Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:
stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=V_{IH} or V_{IL}, I_{OH}= -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	Vcc=3V Vin=V_{IH} or V_{IL}, I_{OH}=12mA	-	0.3	0.5	V
V_{IK}	Clamp diode voltage	Vcc = Min. And I_{IN} = -18mA	-	-0.7	-1.2	V

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	**-**	**0.1**	**30**	**uA**

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Crystal Oscillator Test Conditions

Test Conditions	Output Frequency	Units
X1=3.579MHz, C4=100pf, C5=100pf	3.579	MHz
X1=14.318MHz, C4=50pf, C5=50pf	14.318	MHz
X1=28MHz, C4=50pf, C5=50pf, R1=5.1K	28	MHz
X1=50MHz, C4=50pf, C5=50pf, R1=3K	50	MHz
X1=250MHz, C4=0, C5=0, R1=1K	250	MHz
X1=400MHz, C4=0, C5=0, R1=1K	400	MHz
X1=462MHz, C4=0, C5=0, R1=1K	462	MHz

Notes:
See schematic example.

Switching Characteristics

Symbol	Description	Test Conditions (1)	Max	Unit
t_{PD}	Propagation Delay CLK to Output pair	CL = 15pF	**3.7**	**ns**
tr/tf	Rise/Fall Time	0.8V – 2.0V	**0.8**	**ns**
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	**50**	**ps**
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz	**300**	**ps**
fmax	Input Frequency	CL =15pF	**400**	**MHz**
fmax	Input Frequency	CL = 5pF	**570**	**MHz**
fmax	Input Frequency	CL = 2pF	**700**	**MHz**

Notes:
1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

Test Waveforms

FIGURE 1. LVDS/ PECL/ ECL/ HSTL /DIFFERENTIAL INPUT WAVEFORM DEFINITIONS

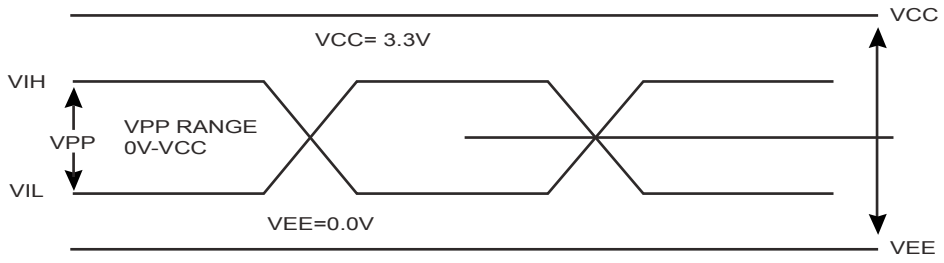


FIGURE 2. HSTL/HSTL OUTPUT

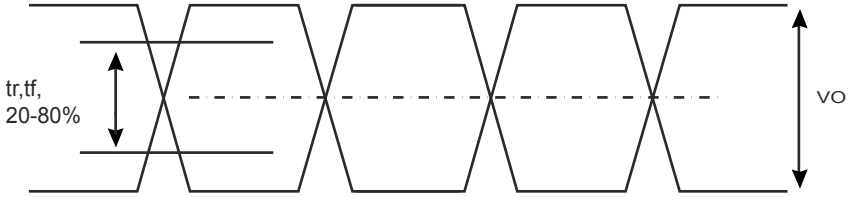


FIGURE 3. Propogation Delay, Output pulse skew, and output-to-output skew for both CLKA or CLKB to output pair

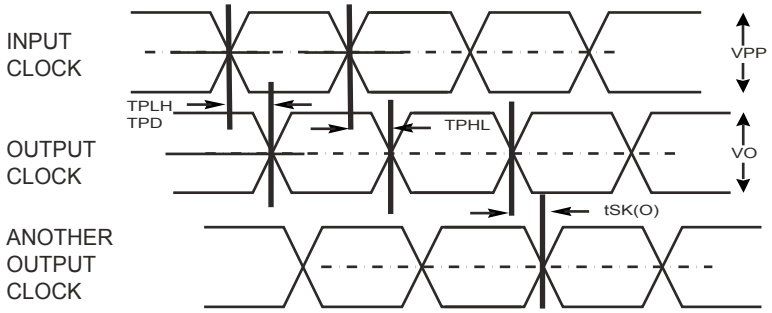
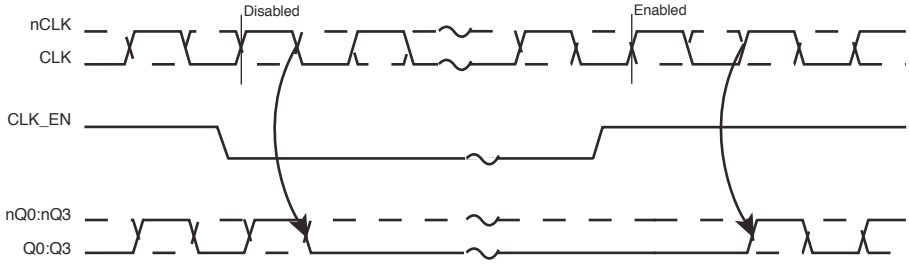
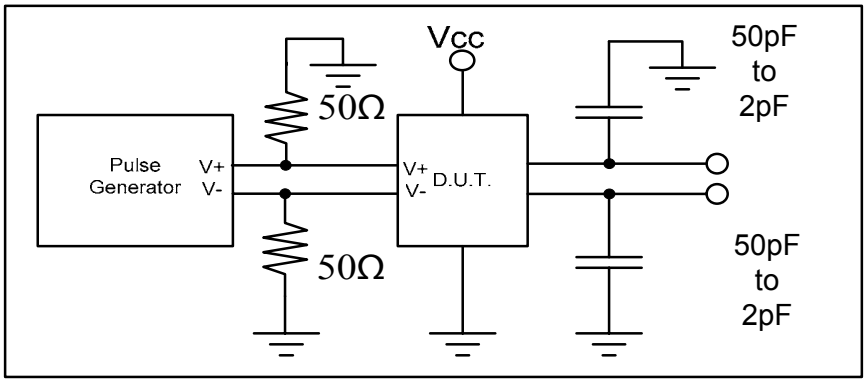


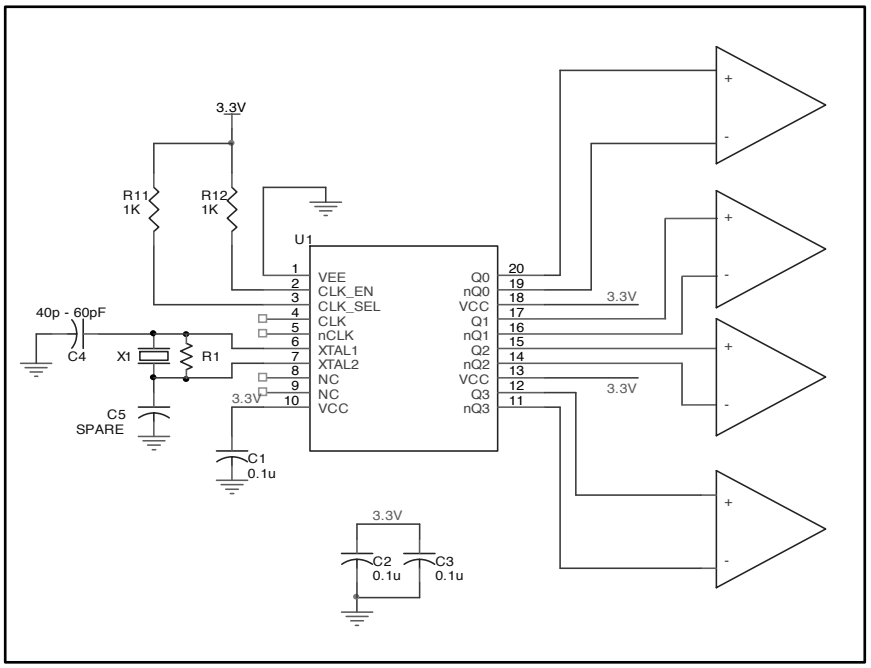
FIGURE 4. CLK_EN Timing Diagram



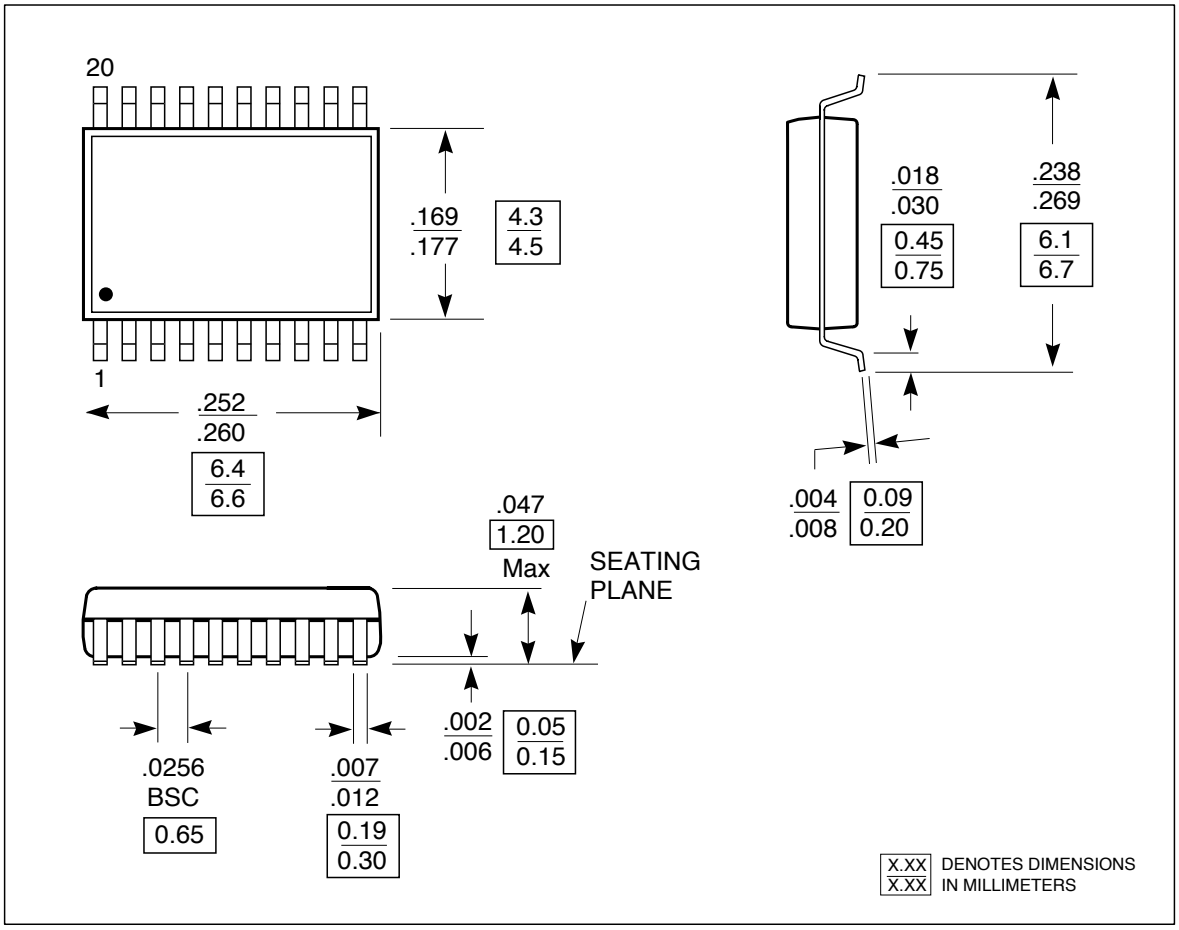
Test Circuit



Schematic Example



Packaging Mechanical Drawing: 20 pin TSSOP



Ordering Information

Ordering Code	Package			Top-Marking	T_A
PO74HSTL85331ATU	20pin TSSOP	Tube	Pb-free & Green	PO74HSTL85331AT	-40°C to 85°C
PO74HSTL85331ATR	20pin TSSOP	Tape and reel	Pb-free & Green	PO74HSTL85331AT	-40°C to 85°C