

32-bit Microcontroller

CMOS

FR60 MB91314A Series

MB91314A/MB91F314

■ DESCRIPTION

The FR family* is a line of single-chip microcontrollers based on the 32-bit high-performance RISC CPU while integrating a variety of I/O resources for embedded control applications which require high-performance, high-speed CPU processing.

The FR family contains multiple channels of data slicer and communication macros, best suited for embedded applications such as TV control.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Limited.

■ FEATURES

1. FR CPU

- 32-bit RISC, load/store architecture with a five-stage pipeline
- Operating frequency 33 MHz [PLL used : Oscillation frequency 16.5 MHz : Doubled]
- 16-bit fixed length instructions (basic instructions), 1 instruction per cycle
- Instruction set optimized for embedded applications : Memory-to-memory transfer, bit manipulation, barrel shift instructions etc.
- Instructions adapted for high-level languages : Function entry/exit instructions, multiple-register load/store instructions
- Register interlock functions : Facilitating coding in assemblers
- On-chip multiplier supported at the instruction level
 - Signed 32-bit multiplication : 5 cycles
 - Signed 16-bit multiplication : 3 cycles

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Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page

URL : <http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

MB91314A Series

- Interrupt (PC, PS save) : 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction prefetch feature added by a 4-word queue in the CPU
- Instruction set compatible with FR family

2. Simple External Bus interface

Capable of functioning 8-bit or 16-bit multiplex bus by setting with program

- Operating frequency : Max 16.5 MHz
- 8/16-bit data/address multiplex I/O
- Capable of chip-select signal output for completely independent four areas settable in 64 Kbytes minimum
- Basic bus cycle : 2 cycles
- Programmable automatic wait cycle generator capable of inserting wait cycles for each area

3. Internal Memory

MB91314A : 256 Kbytes Mask ROM, RAM 32 Kbytes

MB91F314 : 512 Kbytes Flash, RAM 32 Kbytes

4. DMAC (DMA Controller)

- 5 channels
- Two forwarding factors (internal peripheral/software)
- Addressing mode 20/24-bit address selection (increment/decrement/fixe)
- Transfer modes (burst transfer/step transfer/block transfer)
- Selectable transfer data size : 8, 16, or 32 bits

5. Bit Search Module (for REALOS)

Search for the position of the bit 1/0-changed first in one word from the MSB

6. Reload Timer (Including 1 Channel for REALOS)

- 16-bit timer ch.6
- The internal clock is optional from 2/8/32 division

7. Multi function Serial Interface

- 11 channels
- Full duplex double buffer
- Capable of selecting communication mode : asynchronous (Start-Stop synchronous) communication, clock synchronous communication (8.25 Mbps Max), I²C* standard mode (100 kbps Max), high-speed mode (400 kbps Max)
- Parity on/off selectable
- Baud rate generator per channel
- Abundant error detection functions are provided (parity, frame, and overrun)
- External clock can be used as transfer clock
- Ch.0 to ch.2 correspond to DMA transfer.
- Ch.0 to ch.2 have a pair of 16 bytes FIFO buffers for transmission and reception.
- I²C bridge feature (among channels 0, 1, and 2)
- SPI mode

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8. Interrupt Controller

- A total of 24 external interrupt lines (external interrupt pins INT23 to INT0)
- Interrupt from internal peripheral
- Programmable 16 priority levels
- Available for wakeup from STOP mode

9. A/D converter

- 10-bit resolution, 10 channels
- Successive approximation type : conversion time : About 8.0 μ s
- Conversion mode (Single-shot conversion mode, scan conversion mode)
- Startup sources (software/external trigger)

10. PPG

- 4 channels
- 16-bit down counter, 16-bit data register with cycle setting buffer
- The internal clock is optional from 1/4/16/64 division
- Support for automatic cycle setting by DMA transfer
- Function for supporting remote control transmission

11. PWC

- 1 channel (1 input)
- 16-bit up counter
- Simple digital lowpass filter

12. Multi-function timer

- 4 channels
- Lowpass filter eliminating noise below a pre-set clock frequency
- Capable of pulse width measurement using seven types of clock signals
- Pin input event count function
- Interval timer function using seven types of clock signals and external input clock
- Internal HSYNC counter mode

13. Closed caption decoder feature

- 1 channel
- CC decoder function
- ID-1 (480i/480p) decoder function

14. Other interval timers

- Watch timer (32 kHz, Count up to 2 seconds)
- Watchdog timer

15. I/O port

Max 78 ports

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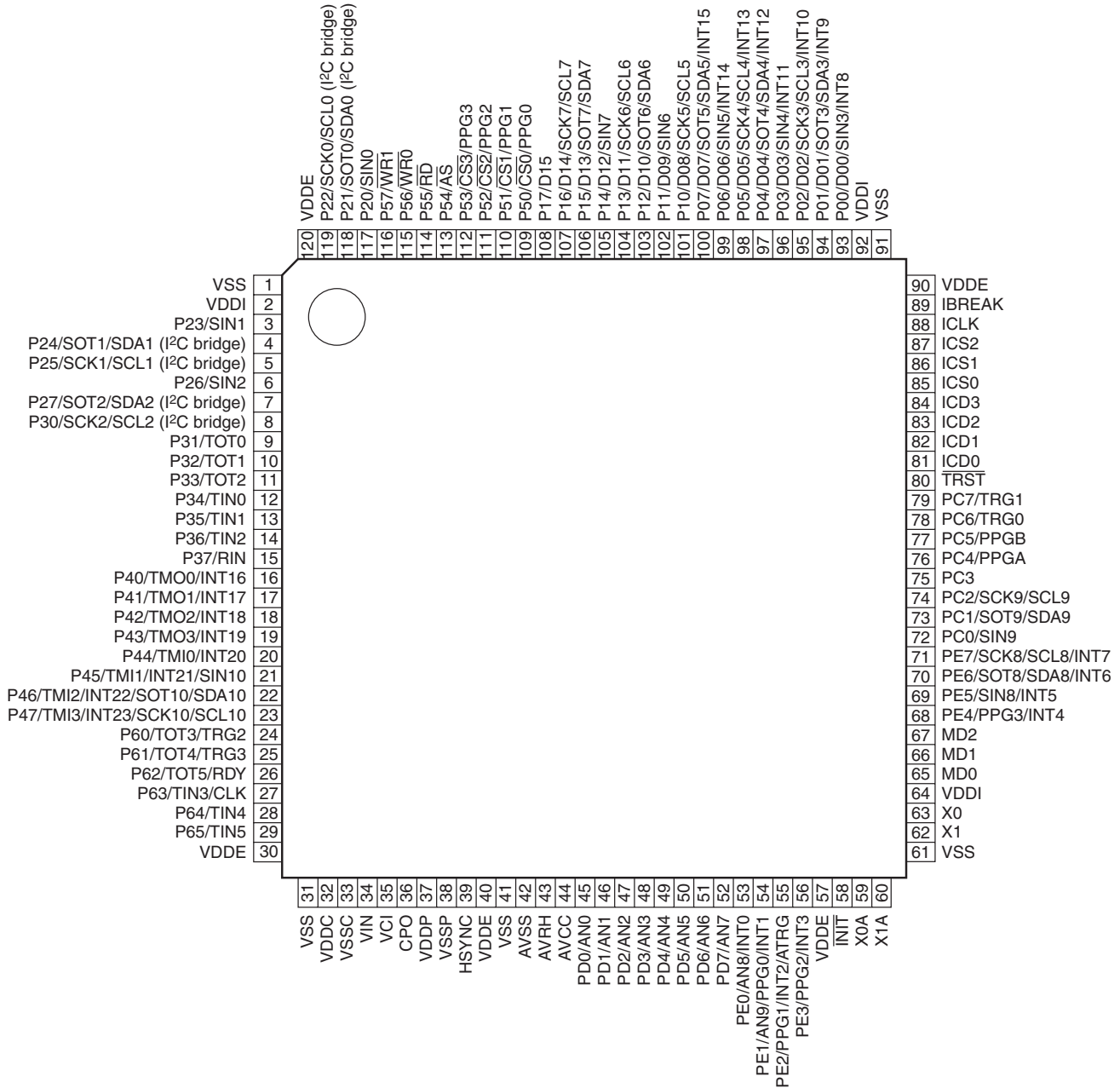
16. Other features

- Internal oscillator circuit as a clock source
- $\overline{\text{INIT}}$ is prepared as a reset terminal
- Watchdog timer reset and software reset are available
- Stop and sleep modes supported as low-power consumption modes
- Gear function
 - Built-in time base timer
 - 5 V tolerant I/O (some pins)
- Package LQFP-120, 0.50 mm pitch, 16.0 mm × 16.0 mm
- CMOS technology (0.18μm)
- Power supply voltage 3.3 V ± 0.3 V, 1.8 V ± 0.15 V dual-power

* : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

PIN ASSIGNMENT

(TOP VIEW)



(FPT-120P-M21)

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■ PIN DESCRIPTION

Pin no.	Pin name	I/O circuit type*	Description
1	VSS	—	GND pin
2	VDDI	—	1.8 V power supply
3	P23	D	General-purpose I/O port
	SIN1		Multi function serial 1 serial data input pin
4	P24	L	General-purpose I/O port
	SOT1/SDA1 (I ² C bridge)		Multi function serial 1 serial data output pin I ² C data I/O pin
5	P25	L	General-purpose I/O port
	SCK1/SCL1 (I ² C bridge)		Multi function serial 1 serial communication clock I/O pin I ² C clock I/O pin
6	P26	D	General-purpose I/O port
	SIN2		Multi function serial 2 serial data input pin
7	P27	L	General-purpose I/O port
	SOT2/SDA2 (I ² C bridge)		Multi function serial 2 serial data output pin I ² C data I/O pin
8	P30	L	General-purpose I/O port
	SCK2/SCL2 (I ² C bridge)		Multi function serial 2 serial communication clock I/O pin I ² C clock I/O pin
9	P31	D	General-purpose I/O port
	TOT0		Output pin for reload timer
10	P32	D	General-purpose I/O port
	TOT1		Output pin for reload timer
11	P33	D	General-purpose I/O port
	TOT2		Output pin for reload timer
12	P34	D	General-purpose I/O port
	TIN0		Event input pin for reload timer
13	P35	D	General-purpose I/O port
	TIN1		Event input pin for reload timer
14	P36	D	General-purpose I/O port
	TIN2		Event input pin for reload timer
15	P37	D	General-purpose I/O port
	RIN		PWC input pin
16	P40	B	General-purpose I/O port
	TMO0		Multifunction timer output
	INT16		External interrupt request input pin
17	P41	B	General-purpose I/O port
	TMO1		Multifunction timer output
	INT17		External interrupt request input pin

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Pin no.	Pin name	I/O circuit type*	Description
18	P42	B	General-purpose I/O port
	TMO2		Multifunction timer output
	INT18		External interrupt request input pin
19	P43	B	General-purpose I/O port
	TMO3		Multifunction timer output
	INT19		External interrupt request input pin
20	P44	B	General-purpose I/O port
	TMI0		Multifunction timer input
	INT20		External interrupt request input pin
21	P45	B	General-purpose I/O port
	TMI1		Multifunction timer input
	INT21		External interrupt request input pin
	SIN10		Multi function serial 10 serial data input pin
22	P46	B	General-purpose I/O port
	TMI2		Multifunction timer input
	INT22		External interrupt request input pin
	SOT10/SDA10		Multi function serial 10 serial data output pin I ² C data I/O pin
23	P47	B	General-purpose I/O port
	TMI3		Multifunction timer input
	INT23		External interrupt request input pin
	SCK10/SCL10		Multi function serial 10 serial communication clock I/O pin I ² C clock I/O pin
24	P60	C	General-purpose I/O port
	TOT3		Output pin for reload timer
	TRG2		PPG trigger input
25	P61	C	General-purpose I/O port
	TOT4		Output pin for reload timer
	TRG3		PPG trigger input
26	P62	C	General-purpose I/O port
	TOT5		Output pin for reload timer
	RDY		External ready input pin
27	P63	C	General-purpose I/O port
	TIN3		Event input pin for reload timer
	CLK		External clock output pin
28	P64	C	General-purpose I/O port
	TIN4		Event input pin for reload timer

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Pin no.	Pin name	I/O circuit type*	Description
29	P65	C	General-purpose I/O port
	TIN5		Event input pin for reload timer
30	VDDE	—	3.3 V power supply
31	VSS	—	GND pin
32	VDDC	—	Data slicer power supply
33	VSSC	—	Data slicer ground
34	VIN	N	Data slicer input
35	VCI	N	VCO control voltage input
36	CPO	N	Charge pump output
37	VDDP	—	Dot clock PLL power supply
38	VSSP	—	Dot clock PLL ground
39	HSYNC	M	Horizontal synchronous input
40	VDDE	—	3.3 V power supply
41	VSS	—	Ground pin
42	AVSS	—	Analog ground pin for A/D converter
43	AVRH	—	Analog reference power voltage input pin for A/D converter
44	AVCC	—	Analog power supply input pin for A/D converter
45	PD0	L	General-purpose I/O port
	AN0		A/D converter analog input pin
46	PD1	L	General-purpose I/O port
	AN1		A/D converter analog input pin
47	PD2	L	General-purpose I/O port
	AN2		A/D converter analog input pin
48	PD3	L	General-purpose I/O port
	AN3		A/D converter analog input pin
49	PD4	L	General-purpose I/O port
	AN4		A/D converter analog input pin
50	PD5	L	General-purpose I/O port
	AN5		A/D converter analog input pin
51	PD6	L	General-purpose I/O port
	AN6		A/D converter analog input pin
52	PD7	L	General-purpose I/O port
	AN7		A/D converter analog input pin
53	PE0	L	General-purpose I/O port
	AN8		A/D converter analog input pin
	INT0		External interrupt request input pin

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Pin no.	Pin name	I/O circuit type*	Description
54	PE1	L	General-purpose I/O port
	AN9		A/D converter analog input pin
	PPG0		Output pin for PPG
	INT1		External interrupt request input pin
55	PE2	B	General-purpose I/O port
	PPG1		Output pin for PPG
	INT2		External interrupt request input pin
	ATRG		Trigger input pin for A/D converter
56	PE3	B	General-purpose I/O port
	PPG2		Output pin for PPG
	INT3		External interrupt request input pin
57	VDDE	—	3.3 V power supply
58	$\overline{\text{INIT}}$	G	Initial reset pin
59	X0A	A	Sub clock input
60	X1A	A	Sub clock I/O
61	VSS	—	Ground pin
62	X1	A	Main clock I/O
63	X0	A	Main clock input
64	VDDI	—	1.8 V power supply
65	MD0	F	Input pins for specifying the operating mode
66	MD1	F	
67	MD2	F	
68	PE4	B	General-purpose I/O port
	PPG3		Output pin for PPG
	INT4		External interrupt request input pin
69	PE5	B	General-purpose I/O port
	SIN8		Multi function serial 8 serial data input pin
	INT5		External interrupt request input pin
70	PE6	B	General-purpose I/O port
	SOT8/SDA8		Multi function serial 8 serial data output pin I ² C data I/O pin
	INT6		External interrupt request input pin
71	PE7	B	General-purpose I/O port
	SCK8/SCL8		Multi function serial 8 serial communication clock I/O pin I ² C clock I/O pin
	INT7		External interrupt request input pin
72	PC0	B	General-purpose I/O port
	SIN9		Multi function serial 9 serial data input pin

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Pin no.	Pin name	I/O circuit type*	Description
73	PC1	B	General-purpose I/O port
	SOT9/SDA9		Multi function serial 9 serial data output pin I ² C data I/O pin
74	PC2	B	General-purpose I/O port
	SCK9/SCL9		Multi function serial 9 serial communication clock I/O pin I ² C clock I/O pin
75	PC3	B	General-purpose I/O port
76	PC4	B	General-purpose I/O port
	PPGA		Output pin for PPG
77	PC5	B	General-purpose I/O port
	PPGB		Output pin for PPG
78	PC6	B	General-purpose I/O port
	TRG0		PPG trigger input
79	PC7	B	General-purpose I/O port
	TRG1		PPG trigger input
80	$\overline{\text{TRST}}$	G	Reset pin for development tool
81	ICD0	K	Data pin for development tool
82	ICD1	K	
83	ICD2	K	
84	ICD3	K	
85	ICS0	H	Status pin for development tool
86	ICS1	H	
87	ICS2	H	
88	ICLK	H	Clock pin for development tool
89	IBREAK	I	Break pin for development tool
90	VDDE	—	3.3 V power supply
91	VSS	—	GND pin
92	VDDI	—	1.8 V power supply
93	P00	C	General-purpose I/O port
	D00		External address/ data bus I/O pin
	SIN3		Multi function serial 3 serial data input pin
	INT8		External interrupt request input pin
94	P01	C	General-purpose I/O port
	D01		External address/ data bus I/O pin
	SOT3/SDA3		Multi function serial 3 serial data output pin I ² C data I/O pin
	INT9		External interrupt request input pin

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Pin no.	Pin name	I/O circuit type*	Description
95	P02	C	General-purpose I/O port
	D02		External address/ data bus I/O pin
	SCK3/SCL3		Multi function serial 3 serial communication clock I/O pin I ² C clock I/O pin
	INT10		External interrupt request input pin
96	P03	C	General-purpose I/O port
	D03		External address/ data bus I/O pin
	SIN4		Multi function serial 4 serial data input pin
	INT11		External interrupt request input pin
97	P04	C	General-purpose I/O port
	D04		External address/ data bus I/O pin
	SOT4/SDA4		Multi function serial 4 serial data output pin I ² C data I/O pin
	INT12		External interrupt request input pin
98	P05	C	General-purpose I/O port
	D05		External address/ data bus I/O pin
	SCK4/SCL4		Multi function serial 4 serial communication clock I/O pin I ² C clock I/O pin
	INT13		External interrupt request input pin
99	P06	C	General-purpose I/O port
	D06		External address/ data bus I/O pin
	SIN5		Multi function serial 5 serial data input pin
	INT14		External interrupt request input pin
100	P07	C	General-purpose I/O port
	D07		External address/ data bus I/O pin
	SOT5/SDA5		Multi function serial 5 serial data output pin I ² C data I/O pin
	INT15		External interrupt request input pin
101	P10	C	General-purpose I/O port
	D08		External address/ data bus I/O pin
	SCK5/SCL5		Multi function serial 5 serial communication clock I/O pin I ² C clock I/O pin
102	P11	C	General-purpose I/O port
	D09		External address/ data bus I/O pin
	SIN6		Multi function serial 6 serial data input pin
103	P12	C	General-purpose I/O port
	D10		External address/ data bus I/O pin
	SOT6/SDA6		Multi function serial 6 serial data output pin I ² C data I/O pin

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Pin no.	Pin name	I/O circuit type*	Description
104	P13	C	General-purpose I/O port
	D11		External address/ data bus I/O pin
	SCK6/SCL6		Multi function serial 6 serial communication clock I/O pin I ² C clock I/O pin
105	P14	C	General-purpose I/O port
	D12		External address/ data bus I/O pin
	SIN7		Multi function serial 7 serial data input pin
106	P15	C	General-purpose I/O port
	D13		External address/ data bus I/O pin
	SOT7/SDA7		Multi function serial 7 serial data output pin I ² C data I/O pin
107	P16	C	General-purpose I/O port
	D14		External address/ data bus I/O pin
	SCK7/SCL7		Multi function serial 7 serial communication clock I/O pin I ² C clock I/O pin
108	P17	C	General-purpose I/O port
	D15		External address/ data bus I/O pin
109	P50	C	General-purpose I/O port
	$\overline{CS0}$		External chip select
	PPG0		Output pin for PPG
110	P51	C	General-purpose I/O port
	$\overline{CS1}$		External chip select
	PPG1		Output pin for PPG
111	P52	C	General-purpose I/O port
	$\overline{CS2}$		External chip select
	PPG2		Output pin for PPG
112	P53	C	General-purpose I/O port
	$\overline{CS3}$		External chip select
	PPG3		Output pin for PPG
113	P54	C	General-purpose I/O port
	\overline{AS}		External address strobe output pin
114	P55	C	General-purpose I/O port
	\overline{RD}		External read strobe output pin
115	P56	C	General-purpose I/O port
	$\overline{WR0}$		External data bus write strobe output pin
116	P57	C	General-purpose I/O port
	$\overline{WR1}$		External data bus write strobe output pin

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Pin no.	Pin name	I/O circuit type*	Description
117	P20	D	General-purpose I/O port
	SIN0		Multi function serial 0 serial data input pin
118	P21	D	General-purpose I/O port
	SOT0/SDA0 (I ² C bridge)		Multi function serial 0 serial data output pin I ² C data I/O pin
119	P22	D	General-purpose I/O port
	SCK0/SCL0 (I ² C bridge)		Multi function serial 0 serial communication clock I/O pin I ² C clock I/O pin
120	VDDE	—	3.3 V power supply

* : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

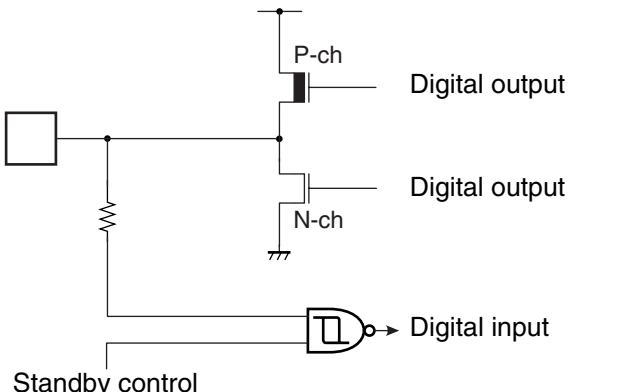
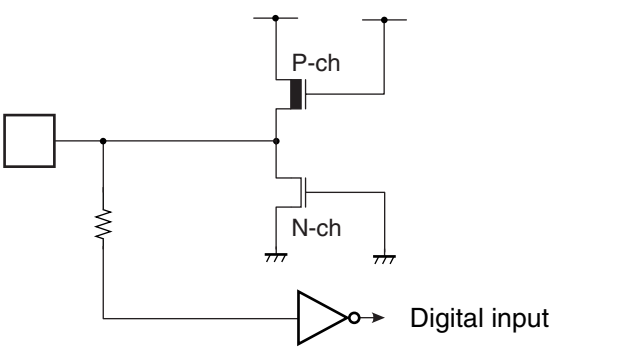
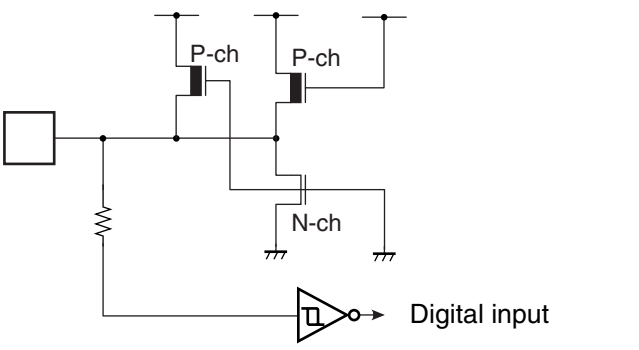
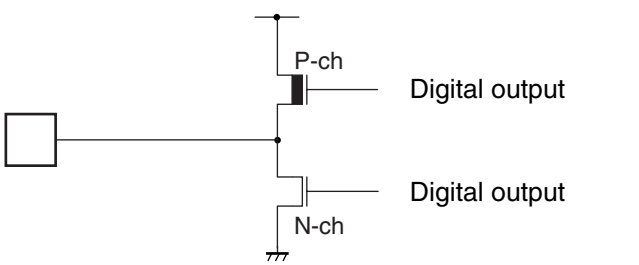
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■ I/O CIRCUIT TYPE

Type	Circuit type	Remarks
A		<ul style="list-style-type: none"> • Oscillation circuit • Built-in feedback resistance X0 pin – X1 pin : 1 MΩ X0A pin – X1A pin : No
B		<ul style="list-style-type: none"> • CMOS level output $I_{OH} = 4\text{mA}$ • CMOS level hysteresis input $V_{IH} = 0.7 \times V_{DDE}$ • With standby control • 5 V tolerant
C		<ul style="list-style-type: none"> • CMOS level output $I_{OH} = 4\text{mA}$ • CMOS level hysteresis input $V_{IH} = 0.8 \times V_{DDE}$ • With standby control • With pull-up resistor (33 kΩ)

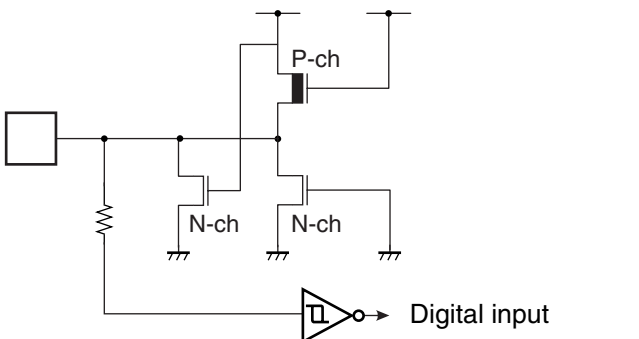
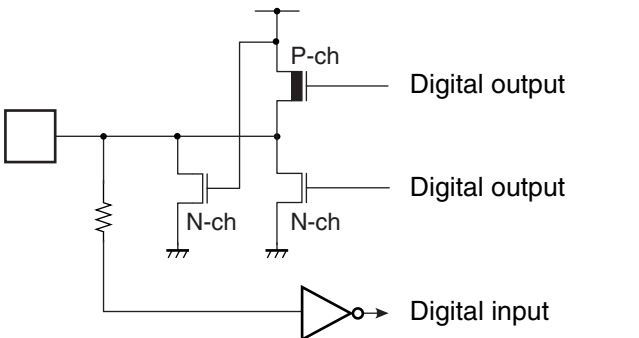
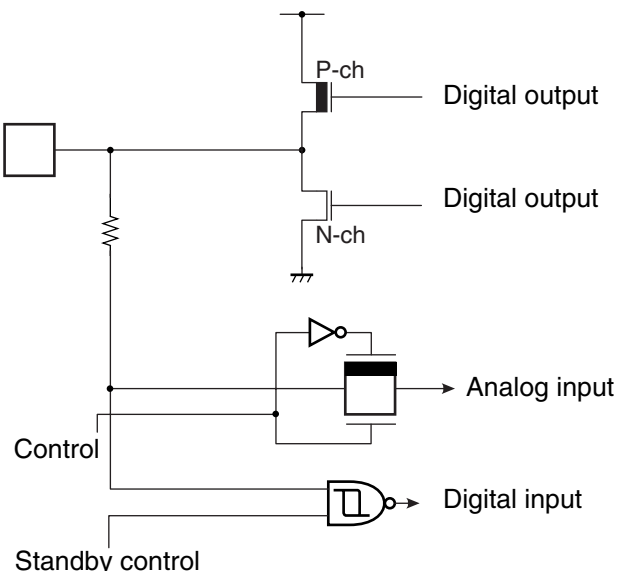
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Type	Circuit type	Remarks
D		<ul style="list-style-type: none"> • CMOS level output $I_{OH} = 4 \text{ mA}$ • CMOS level hysteresis input $V_{IH} = 0.8 \times V_{DDE}$ • With standby control • Without pull-up resistor
F		<ul style="list-style-type: none"> • CMOS level input • Without standby control
G		<ul style="list-style-type: none"> • CMOS hysteresis input • With pull-up resistor
H		<p>CMOS level output</p>

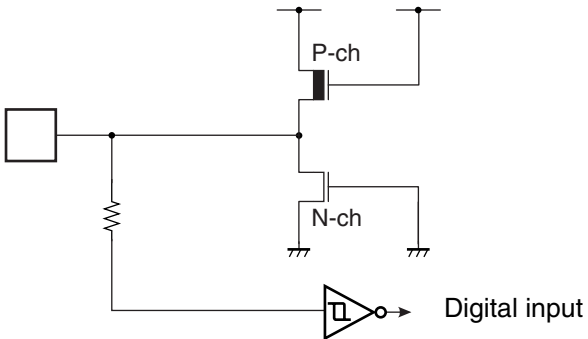
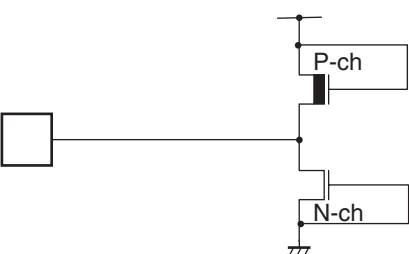
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Type	Circuit type	Remarks
I		<ul style="list-style-type: none"> • CMOS hysteresis input • With pull-down resistor • Without standby control
K		<ul style="list-style-type: none"> • CMOS level output • CMOS level input • Without standby control • With pull-down resistor
L		<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With standby control • Analog input with switch

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Type	Circuit type	Remarks
M	 <p>The diagram shows a CMOS input stage. A square box representing the external input is connected to the gate of a P-channel MOSFET (P-ch) and the gate of an N-channel MOSFET (N-ch). The source of the P-ch MOSFET is connected to a supply rail, and its drain is connected to the input node. The source of the N-ch MOSFET is connected to ground, and its drain is also connected to the input node. A resistor is connected between the supply rail and the input node. The input node is also connected to the input of a digital buffer (represented by a triangle with a '1' inside), which has its output labeled 'Digital input'.</p>	<ul style="list-style-type: none"> • CMOS level hysteresis input • Without standby control
N	 <p>The diagram shows a CMOS input stage. A square box representing the external input is connected to the gate of a P-channel MOSFET (P-ch) and the gate of an N-channel MOSFET (N-ch). The source of the P-ch MOSFET is connected to a supply rail, and its drain is connected to the input node. The source of the N-ch MOSFET is connected to ground, and its drain is also connected to the input node. A resistor is connected between the supply rail and the input node. The input node is also connected to an analog pin.</p>	<p>Analog pin</p>

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■ HANDLING DEVICES

- Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage greater than V_{DDE} or V_{DDI} , or less than V_{SS} is applied to input and output pins or if an above-rating voltage is applied between V_{DDE} or V_{DDI} pins and V_{SS} pin. A latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

- Treatment of Unused Input Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

- About power supply pins

If more than one V_{DDE} or V_{DDI} or V_{SS} pin exists, those that must be kept at the same potential are designed to be connected to one other inside the device to prevent malfunctions such as latch-up. Be sure to connect the pins to a power supply and ground external to the device to minimize undesired electromagnetic radiation, prevent strobe signal malfunctions due to an increase in ground level, and conform to the total output current rating. Given consideration to connecting the current supply source to V_{DDE} or V_{DDI} and V_{SS} pin of the device at the lowest impedance possible.

It is also recommended that a ceramic capacitor of around 0.1 μF be connected between V_{DDE} or V_{DDI} and V_{SS} pin at circuit points close to the device as a bypass capacitor.

- About Crystal oscillator circuit

Noise near the X0, X1, X0A and X1A pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, X0A and X1A pins the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0, X1, X0A and X1A pins surrounded by ground plane because stable operation can be expected with such a layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

- About Mode pins (MD0 to MD2)

These pins should be connected directly to V_{DDE} or V_{SS} pins. To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and V_{DDE} or V_{SS} pins is as short as possible and the connection impedance is low.

- Operation at start-up

Always use the $\overline{\text{INIT}}$ pin to perform a setting initialization reset (INIT) after turning on the power.

Immediately after the power supply is turned on, hold the Low level input to the $\overline{\text{INIT}}$ pin for the stabilization wait time required for the oscillator circuit to take the oscillation stabilization wait time for the oscillator circuit (For INIT via the INIT pin, the oscillation stabilization wait time setting is initialized to the minimum value).

- Source oscillation input at power on

When turning on the power, always input the clock for the duration of the oscillation stabilization delay time.

MB91314A Series

- Notes on the turning on/off VDDI pin (1.8 V internal power supply) and VDDE pin (3.3 V external pin power supply)

Do not apply only VDDE pin (external) voltage continuously (more than one minute) with VDDI pin (internal) disconnected as it adversely affects the reliability of the LSI.

When VDDE pin (external) returns from the OFF state to the ON state, the circuit may fail to hold its internal state, for example, due to power supply noise.

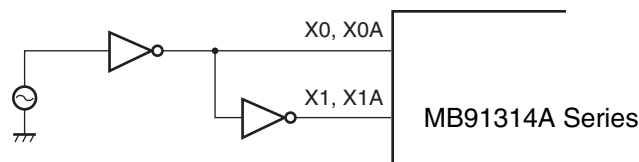
Power on	VDD pin (internal) → Analog → VDDE pin (external) → signal
Power off	Signal → VDDE pin (external) → Analog → VDDI pin (internal)

When the power is turned on, the output pin may remain unstable until the internal power supply becomes stable.

- About the attention when the external clock is used

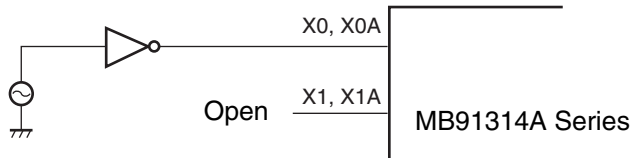
To use an external clock, in principle, supply the X1 (X1A) pin with a clock signal inverted in phase from the X0 (X0A) pin at the same time. However, in this case the stop mode (oscillator stop mode) must not be used. (This is because the X1 (X1A) pin stops at “H” output in STOP mode.) At 12.5 MHz or less, the device can be used only with the X0 (X0A) pin supplied with clock signals.

Using an External Clock (Normal Method)



The STOP mode (oscillation stop mode) cannot be used.

Using an External Clock (available at 12.5 MHz or less)

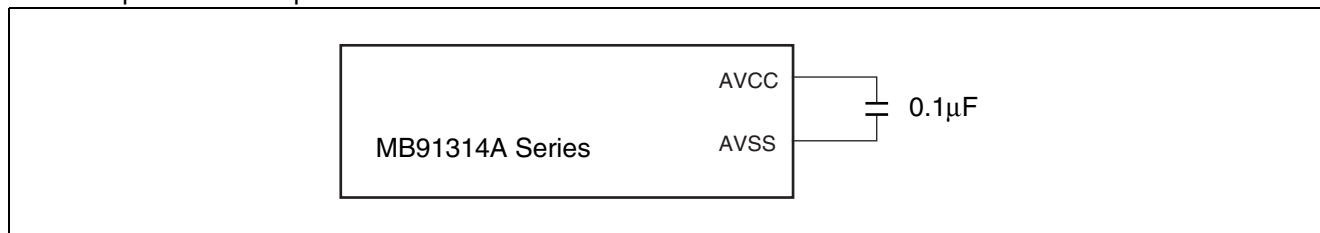


Note : With respect to the X0 (X0A) signal, design X1 such that the delay is within 15 ns at 10 MHz.

MB91314A Series

- AVCC pin

The device has an internal A/D converter. A capacitor of approximately 0.1 μ F must be connected between the AVCC pin and AVSS pin.



- Notes when the emulator is not used

To operate the evaluation MCU on the user system without connecting the emulator, treat each input pin on the evaluation MCU connected to the emulator interface on the user system as shown below.

Emulator Interface Pin Treatment

Evaluation MCU pin name	Pin operation
$\overline{\text{TRST}}$	Connected to the reset output circuit on the user system.
$\overline{\text{INIT}}$	Connected to the reset output circuit on the user system.
Others	Open

- Note on operation with the PLL clock selected

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

■ RESTRICTIONS

1) Clock control block

Take the oscillation stabilization wait time during “L” level input to the $\overline{\text{INIT}}$ pin.

2) Bit Search Module

The bit search data register for 0-detection (BSD0), and bit search data register for 1-detection (BSD1), and bit search data register for change point detection (BSDC) are only word-accessible.

3) I/O port

Ports are accessed only in bytes.

4) Low Power Consumption Mode

- To place the device in standby mode, use the synchronous standby mode (set with bit 8 (SYNCS bit) of the timebase counter control register, TBCR) and be sure to use the following sequence:

```
(ldi  #value_of_standby, r0)
(ldi  #_STCR, r12)
stb   r0, @r12 // set STOP/SLEEP bit
ldub  @r12, r0 // Must read STCR
ldub  @r12, r0 // after reading, go into standby mode
nop                    // Must insert NOP *5
nop
nop
nop
nop
```

- Please do not do the following when the monitor debugger is used.
 - Setting of the break point to the above-mentioned instruction row.
 - Execution of the step for the above-mentioned instruction row.

MB91314A Series

5) Notes on the PS register

Since some instructions write the information to PS register early time, the following exception operations may cause a break to occur in an interrupt processing routine when using the debugger or the updating of the PS flag. In either case, the processing is conducted properly again after return from an EIT, the operations before and after the EIT are designed to perform as specified.

- The following operations may be performed when the instruction immediately followed by a DIV0U/DIV0S instruction results in (a) acceptance of a user interrupt, (b) single-stepping, or (c) a break in response to a data event or emulator menu:
 - (1) D0 and D1 flags are updated in advance.
 - (2) An EIT handling routine (user interrupt, NMI, or emulator) is executed.
 - (3) Upon returning from the EIT, the DIV0U/DIV0S instructions are executed and the D0/D1 flags are updated back to the original value held before step (1).
- When a user interrupt source exists, executing either of the OR CCR, ST LIM and MOV Ri and PS instructions to enable the interrupt results in the following operations:
 - (1) The PS register is updated in advance.
 - (2) An EIT handling routine (user interrupt) is executed.
 - (3) Upon returning from the EIT, the above instructions are executed and the PS registers are updated back to the original value held before step (1).

6) Watchdog timer

The watchdog timer integrated in this model monitors the program to check that it delays a reset within a certain period of time and, if the program runs out of control and fails to delay the reset, resets the CPU in place. Once the watchdog timer is enabled, it keeps running until reset. As an exception, the watchdog timer delays the reset automatically when a condition which stops program execution by the CPU develops. For those conditions which correspond to this exception, refer to the function description of the watchdog timer in "HARDWARE MANUAL". A watchdog reset may not be generated in the above situation caused by the system running out of control. In that case, please reset (INIT) by external $\overline{\text{INIT}}$ terminal.

7) Notes on using the A/D converter

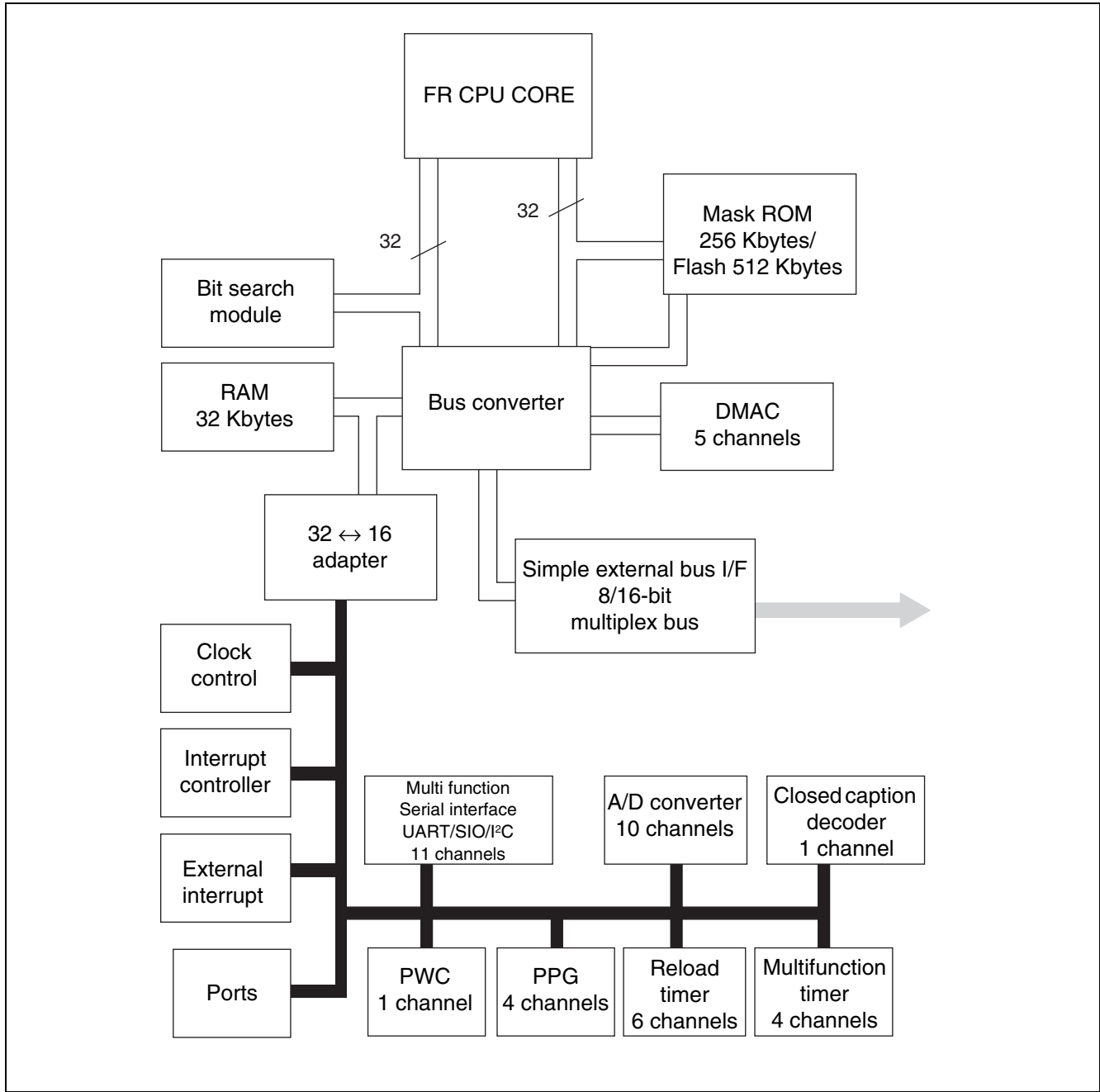
Although this series contains an A/D converter, do not apply a higher voltage to AVCC pin than to VDDE pin.

8) Software reset in synchronous mode

When using the software reset in synchronous mode, the following two conditions should be satisfied before setting "0" to the SRST bit in STCR (standby control register) .

- Set the interrupt enable flag (I-Flag) to the interrupt disable (I-Flag = 0) .
- Do not use NMI.

■ BLOCK DIAGRAM



MB91314A Series

■ CPU AND CONTROL UNIT

Internal architecture

The FR family of CPUs is a line of high-performance cores providing advanced instructions for embedded applications based on the RISC architecture.

1. Features

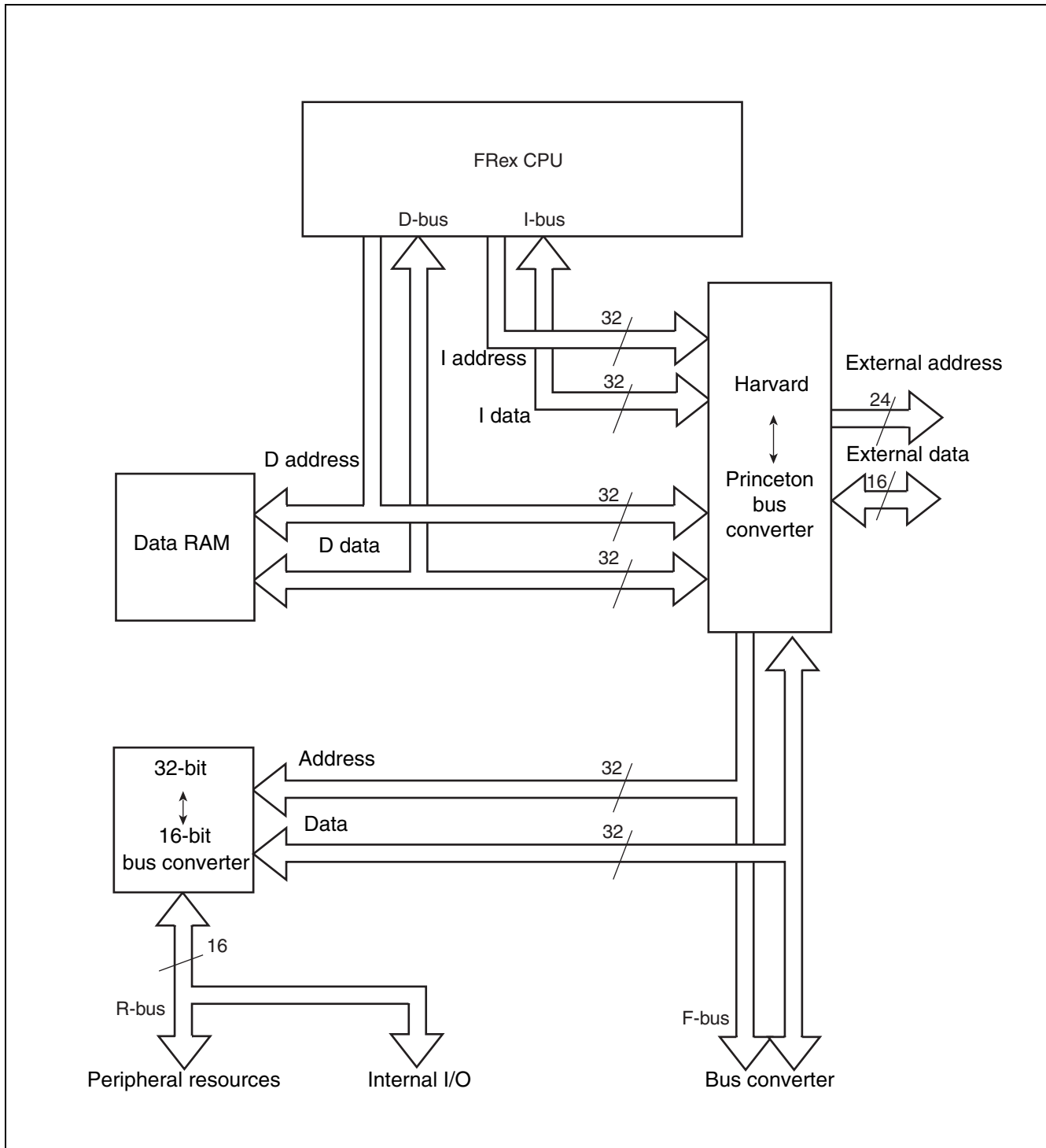
- RISC architecture adopted. Basic instructions : Executed at one instruction per cycle
- 32-bit architecture
 - General purpose registers : 32 bits × 16
- Four Gbytes of linear memory space
- Multiplier integrated
 - 32-bit × 32-bit multiplication : 5 cycles
 - 16-bit × 16-bit multiplication : 3 cycles
- Enhanced interrupt servicing
 - High-speed response (6 cycles)
 - Multi-level interrupt support
 - Level mask feature (16 levels)
- Enhanced I/O manipulation instructions
 - Memory-to-memory transfer instructions
 - Bit manipulation instructions
- High code efficiency
 - Basic instruction word length : 16 bits
- Lower-power consumption
 - Sleep mode/stop mode
 - Gear function

2. Internal architecture

The FR family of CPUs has a Harvard architecture in which the instruction bus and data bus are separated.

The 32-bit ↔ 16-bit bus converter is connected to the 32-bit bus (F-bus) to provide an interface between the CPU and peripheral resources.

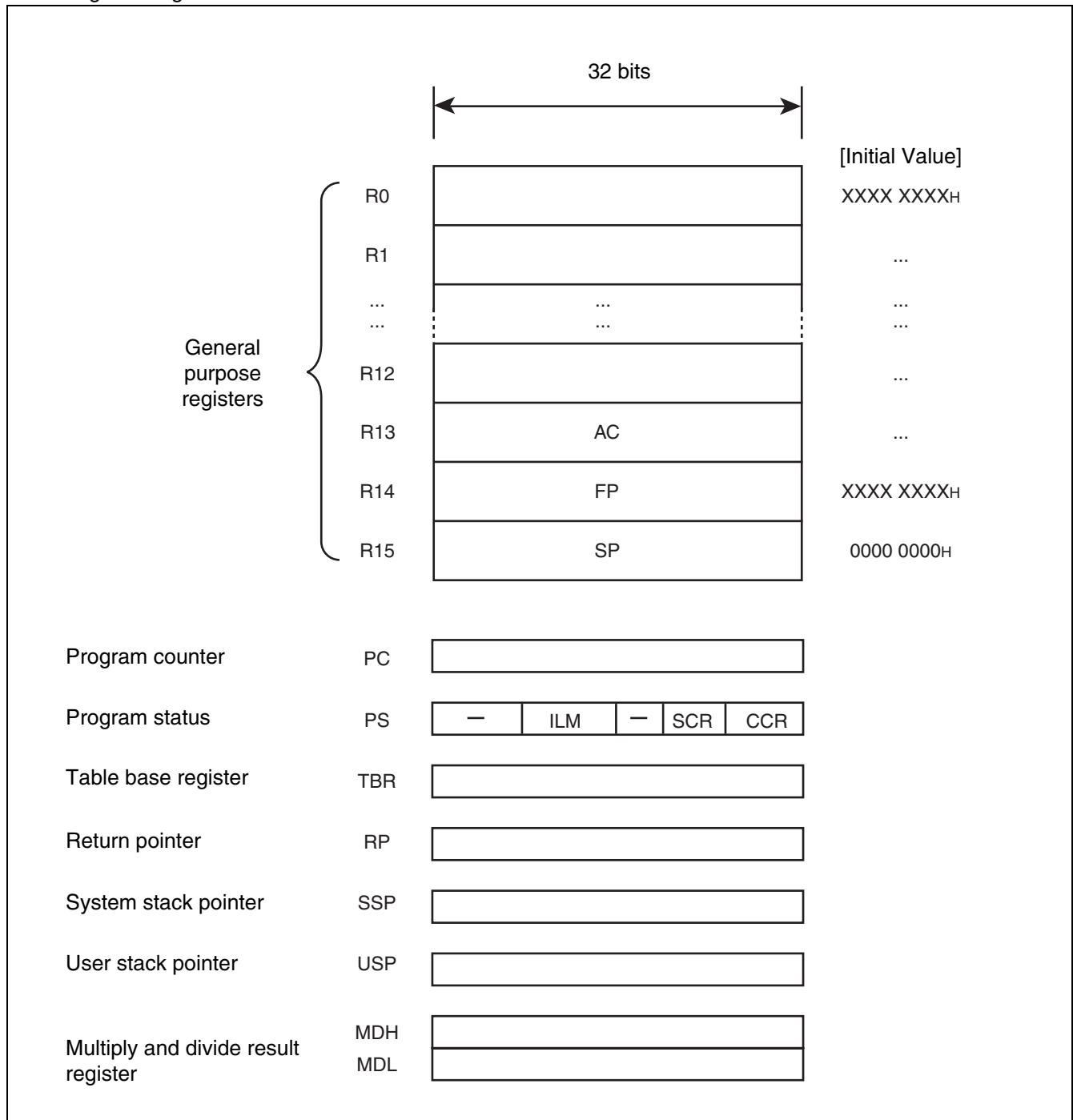
The Harvard ↔ Princeton bus converter is connected to both of the I-bus and D-bus, providing an interface between the CPU and the bus controller.



MB91314A Series

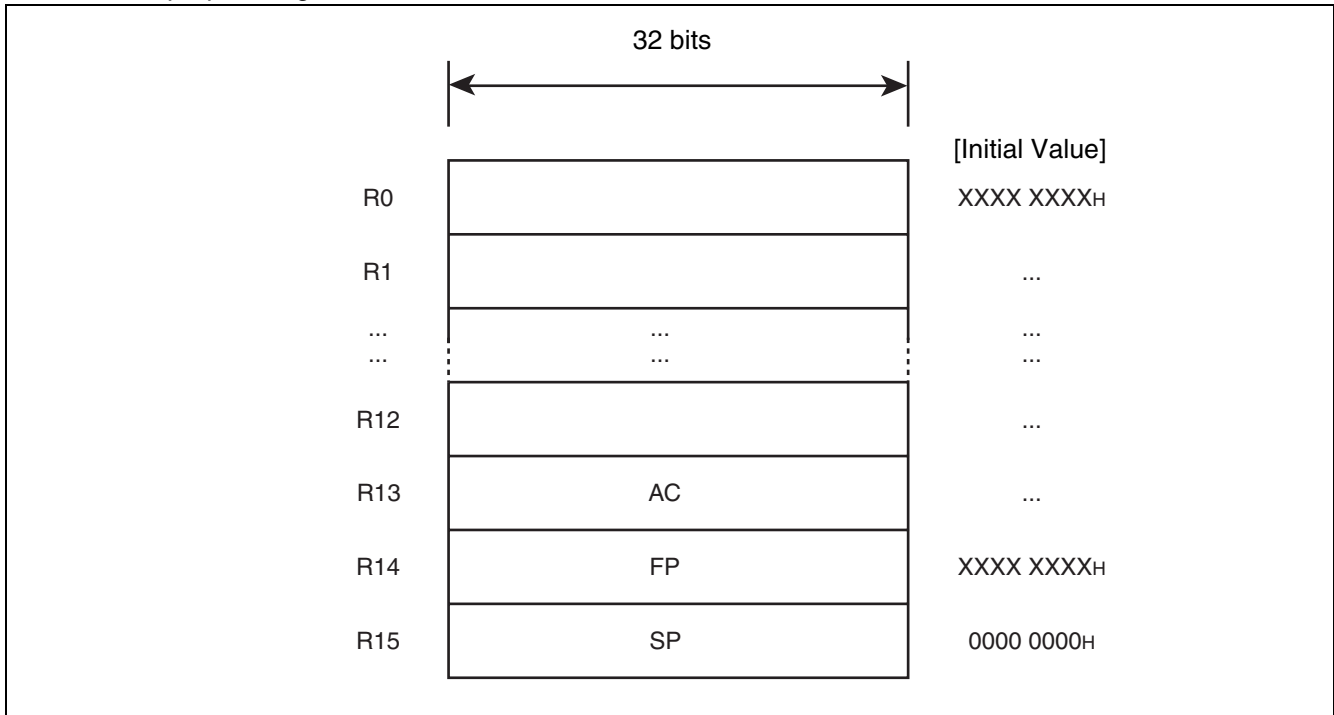
3. Programming model

- Programming model



4. Register

- General purpose registers



Registers R0 to R15 are general purpose registers. The registers are used as the accumulator and memory access pointers for CPU operations.

Of these 16 registers, the registers listed below are intended for special applications, for which some instructions are enhanced.

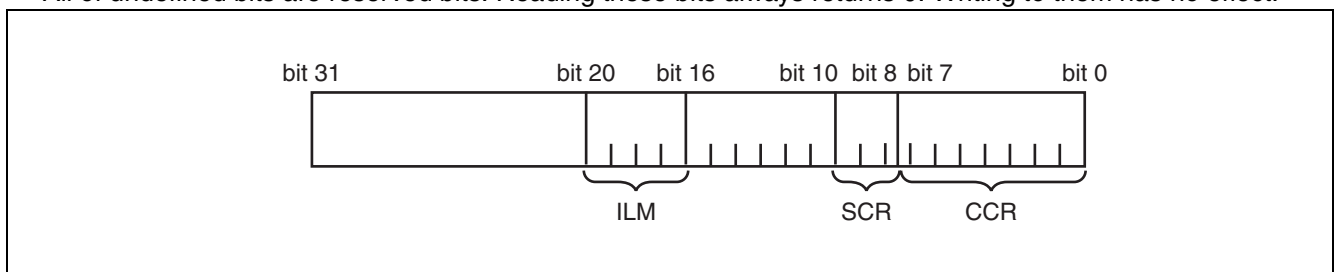
- R13 : Virtual accumulator (AC)
- R14 : Frame pointer (FP)
- R15 : Stack pointer (SP)

The initial values of R0 to R14 after a reset are indeterminate. R15 is initialized to 00000000H (SSP value).

- PS (Program Status)

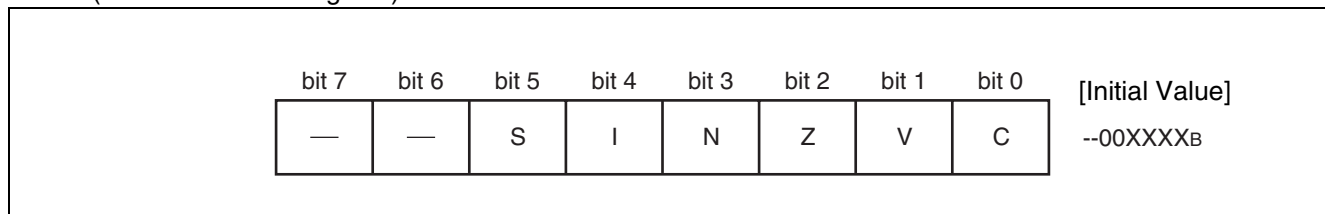
This register holds the program status and is divided into the ILM, SCR, and CCR.

All of undefined bits are reserved bits. Reading these bits always returns 0. Writing to them has no effect.



MB91314A Series

• CCR (Condition Code Register)



S : Stack flag

- Cleared to 0 at a reset.
- Set the flag to 0 for execution of the RETI instruction.

I : Interrupt Enable flag

Cleared to 0 at a reset.

N : Negative flag

Initial state by reset is irregular.

Z : Zero flag

Initial state by reset is irregular.

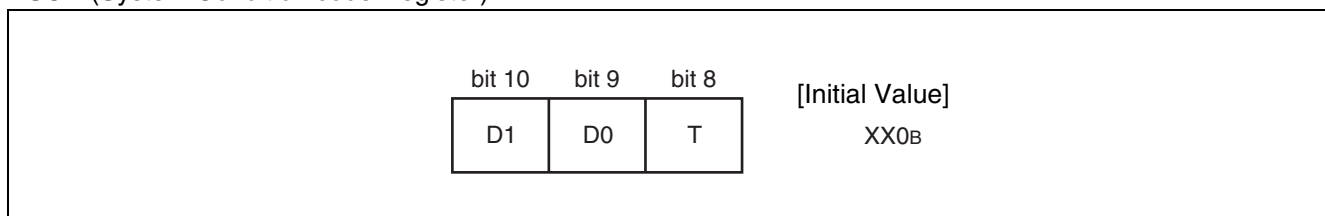
V : Overflow flag

Initial state by reset is irregular.

C : Carrying flag

Initial state by reset is irregular.

• SCR (System Condition code Register)



D1, D0 : Flag for step division

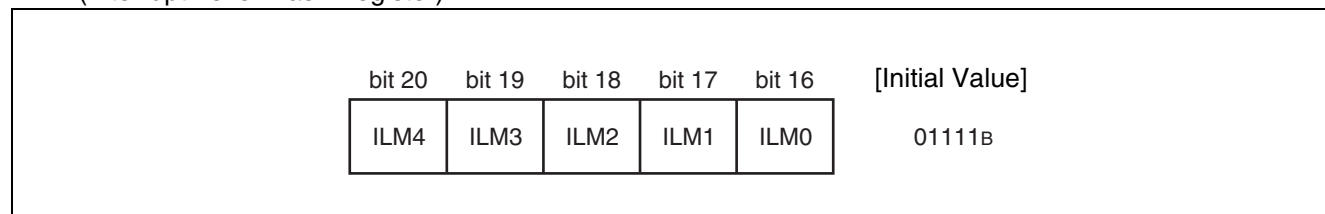
Stores intermediate data for stepwise division operations.

T : Step trace trap flag

A flag specifying whether the step trace trap function is enabled or not.

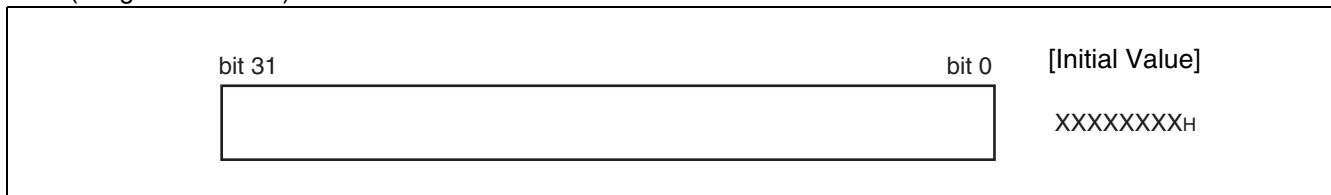
- The emulator uses the step trace trap function. The function cannot be used by the user program when using the emulator.

• ILM (Interrupt Level Mask Register)



This register stores the interrupt level mask value. The value in the ILM register is used as the level mask. Initialized to 15 (01111_B) by a reset.

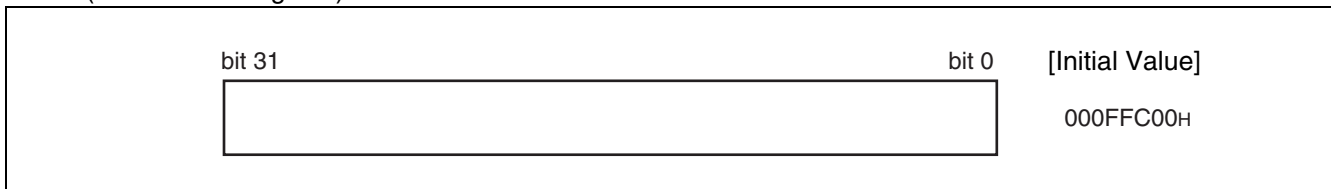
- PC (Program Counter)



The program counter contains the address of the instruction currently being executed.

The initial value after a reset is indeterminate.

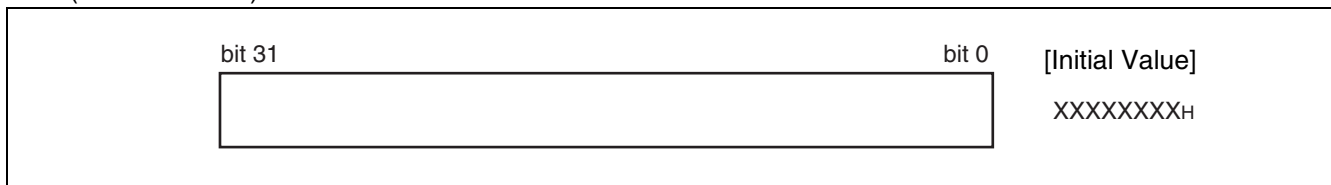
- TBR (Table Base Register)



The table base register contains the start address of the vector table used for servicing EIT events.

The initial value after a reset is 000FFC00H.

- RP (Return Pointer)



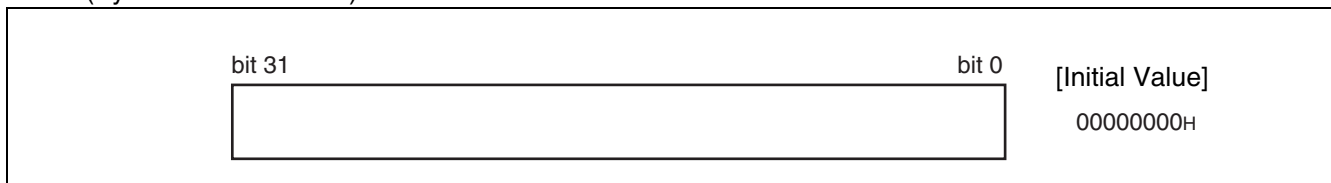
The return pointer contains the address to which to return from a subroutine.

When the CALL instruction is executed, the value in the PC is transferred to the RP.

When the RET instruction is executed, the value in the RP is transferred to the PC.

The initial value after a reset is indeterminate.

- SSP (System Stack Pointer)



The SSP is the system stack pointer.

The SSP functions as R15 when the S flag is "0".

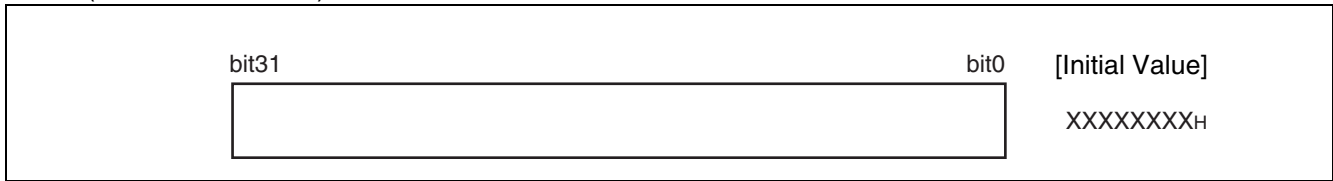
The SSP can be explicitly specified.

The SSP is also used as the stack pointer that specifies the stack for saving the PS and PC when an EIT event occurs.

The initial value after a reset is 00000000H.

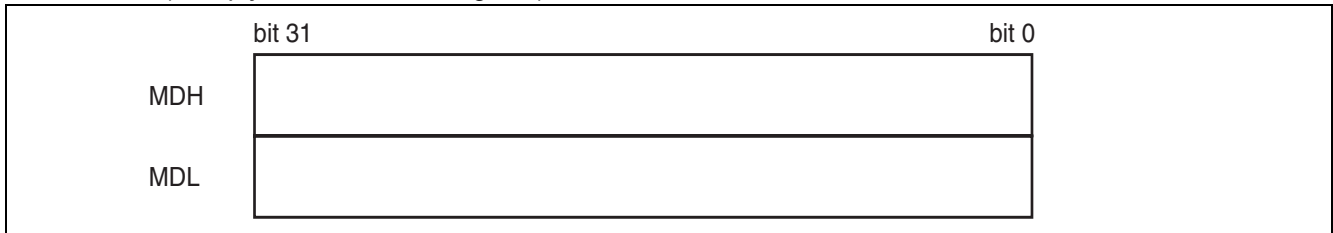
MB91314A Series

- USP (User Stack Pointer)



- The USP is the user stack pointer.
- The USP functions as R15 when the S flag is "1".
- The USP can be explicitly specified.
- The initial value after a reset is indeterminate.
- This pointer cannot be used by the RETI instruction.

- MDH, MDL (Multiply & Divide result register)



- These registers hold the results of a multiplication or division. Each of them is 32-bit long.
- The initial value after a reset is indeterminate.

■ MODE SETTINGS

The FR family sets the operation mode using mode pins (MD2, MD1, and MD0) and a mode register (MODR).

1. Mode Pins

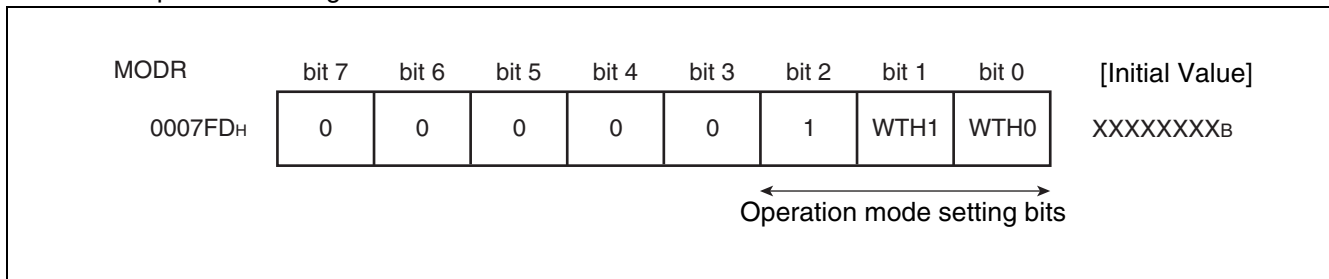
The MD2, MD1, and MD0 pins specify how the mode vector fetch is performed.

Mode Pins			Mode name	Reset vector access area
MD2	MD1	MD0		
0	0	0	Internal ROM mode vector	Internal

Note: Values other than those listed in the table are prohibited.

2. Mode Register (MODR)

- Detailed explanation of register



Data written to the mode register by mode vector fetch is referred to as mode data.

When the mode register is set, the operation mode set in this register is used for operation.

The mode register is set when any reset source occurs.

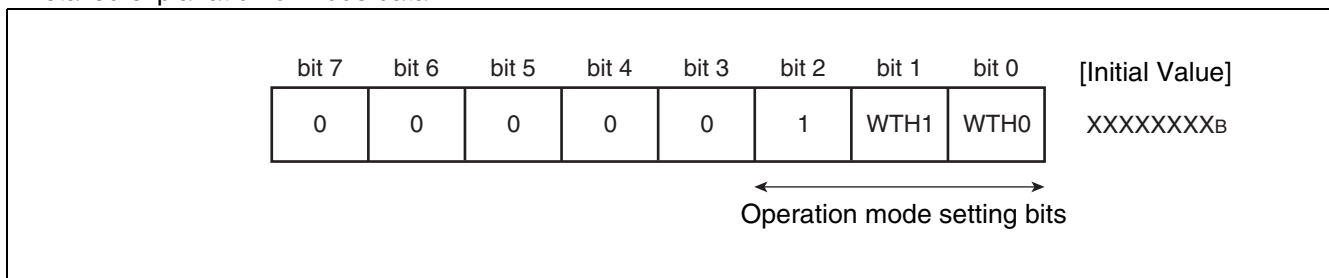
Mode data cannot be written by the user program.

Note : Conventionally, the address (000007FF_H) of the mode register for the FR family holds nothing.

The register can be updated in emulator mode. In this case, please use the instruction of the data transfer for the 8-bit length.

Any 16/32-bit length transfer instruction cannot be used to write data to the mode register.

- Detailed explanation of mode data



[bit 7 to bit 2] Reserved bits

Be sure to set these bits to "000001_B".

Setting the bits to any value other than "000001_B" may result in an unpredictable operation.

MB91314A Series

[bit 1, bit 0] WTH1, WTH0 (bus width setting bits)

Used to set the bus width to be used in external bus mode.

When the operation mode is the external bus mode, this value is set in bits BW1 and BW0 in AMD0 (CS0 area).

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	External bus mode
1	0	—	Setting disabled
1	1	Single chip mode	Single chip mode

■ MEMORY SPACE

1. Memory space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) linearly accessible to the CPU.

Direct Addressing Areas

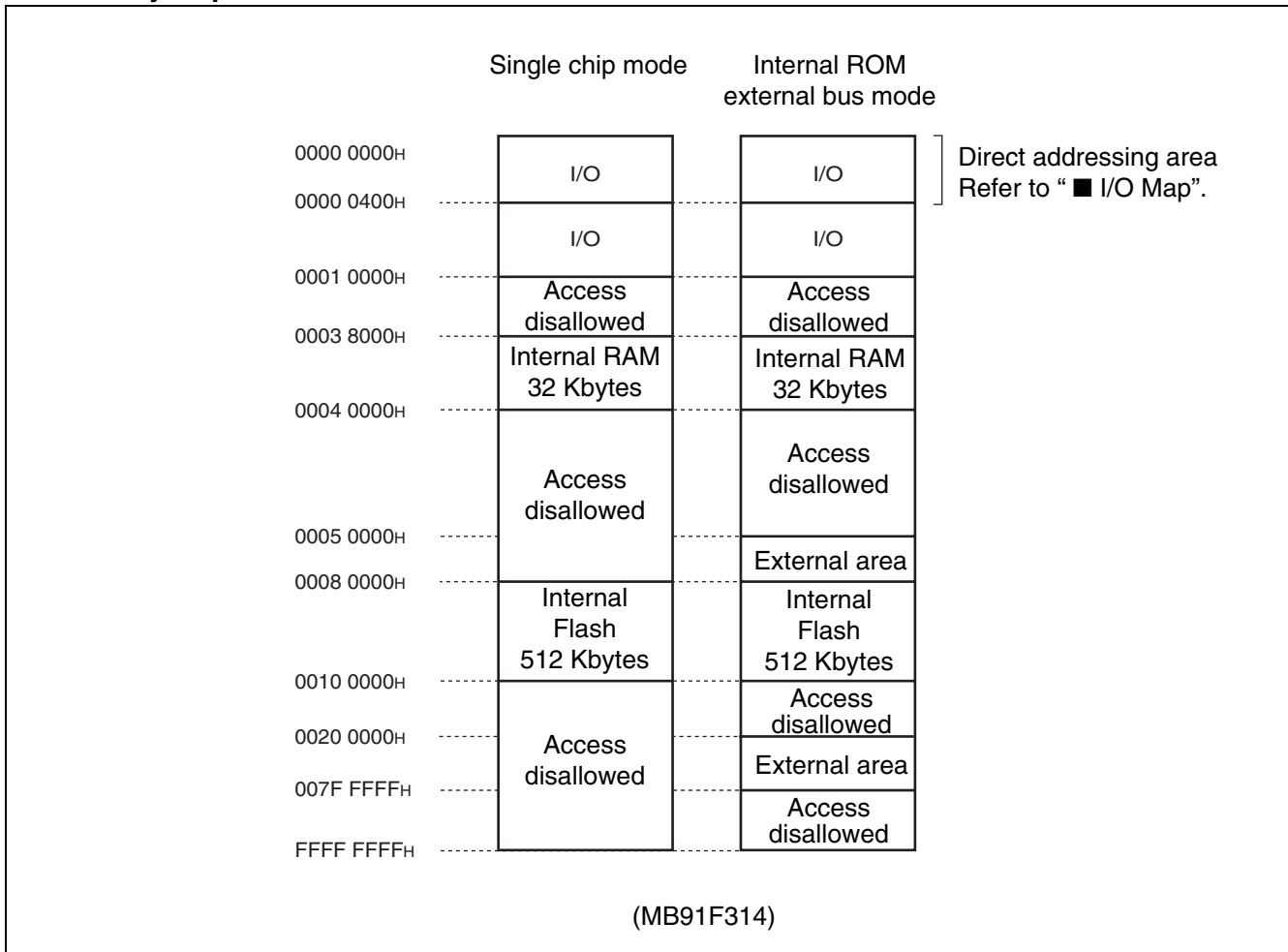
The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.

The direct area varies depending on the size of data to be accessed as follows:

- Byte data access : 000H to 0FFH
- Half word data access : 000H to 1FFH
- Word data access : 000H to 3FFH

2. Memory Map



MB91314A Series

	Single chip mode	Internal ROM external bus mode	
0000 0000H	I/O	I/O] Direct addressing area Refer to "■ I/O Map".
0000 0400H	I/O	I/O	
0001 0000H	Access disallowed	Access disallowed	
0003 8000H	Internal RAM 32 Kbytes	Internal RAM 32 Kbytes	
0004 0000H	Access disallowed	Access disallowed	
0005 0000H		External area	
0008 0000H	Mask ROM 256 Kbytes	Mask ROM 256 Kbytes	
000C 0000H		Access disallowed	
0020 0000H	Access disallowed	External area	
007F FFFFH		Access disallowed	
FFFF FFFFH			

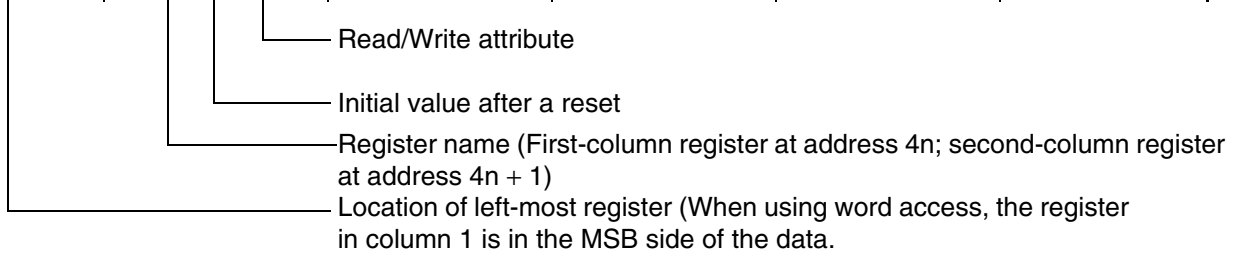
(MB91314A)

■ I/O MAP

The following table shows the correspondence between the memory space area and each register of the peripheral resource.

[How to read the table]

Address	Register				Block
	+0	+1	+2	+3	
000000 _H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit Port data register



Note : The bit values in the register represent the following initial values:

- "1" : initial values "1"
- "0" : initial values "0"
- "X" : initial values "X"
- "-" : No physical register at this location

Access is barred with an undefined data access attribute.

MB91314A Series

Address	Register				Block
	0	1	2	3	
000000 _H	PDR0 [R/W] B, H XXXXXXXX	PDR1 [R/W] B, H XXXXXXXX	PDR2 [R/W] B, H XXXXXXXX	PDR3 [R/W] B, H XXXXXXXX	Port data register
000004 _H	PDR4 [R/W] B, H XXXXXXXX	PDR5 [R/W] B, H XXXXXXXX	PDR6 [R/W] B, H --XXXXXX	—	
000008 _H	—				
00000C _H	PDRC [R/W] B, H XXXXXXXX	PDRD [R/W] B, H XXXXXXXX	PDRE [R/W] B, H XXXXXXXX	—	
000010 _H to 00001C _H	—				Reserved
000020 _H	ADCTH[R/W] XXXXXX00	ADCTL[R/W] 00000X00	ADCH[R/W] 00000000 00000000		10-bit A/D converter
000024 _H	ADAT0[R] XXXXXX00 00000000		ADAT1[R] XXXXXX00 00000000		
000028 _H	ADAT2[R] XXXXXX00 00000000		ADAT3[R] XXXXXX00 00000000		
00002C _H	ADAT4[R] XXXXXX00 00000000		ADAT5[R] XXXXXX00 00000000		
000030 _H	ADAT6[R] XXXXXX00 00000000		ADAT7[R] XXXXXX00 00000000		
000034 _H	ADAT8[R] XXXXXX00 00000000		ADAT9[R] XXXXXX00 00000000		
000038 _H to 00003C _H	—				
000040 _H	EIRR0 [R/W] 00000000	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		Ext. INT 0 to INT7
000044 _H	DICR [R/W] 00000000	HRCL [R, R/W] 0--11111	—		DLY / I-unit
000048 _H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload timer 0
00004C _H	—		TMCSR0 [R, RW] 00000000 00000000		
000050 _H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload timer 1
000054 _H	—		TMCSR1 [R, RW] 00000000 00000000		

(Continued)

MB91314A Series

Address	Register				Block
	0	1	2	3	
000058H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload timer 2
00005CH	—		TMCSR2 [R, RW] 00000000 00000000		
000060H	SCR0 [R, R/W] 0--00000	SMR0 [W, R/W] 00000000	SSR0 [R, R/W] 0-000011	ESCR0 [R/W] --000000	Multi function Serial interface 0 FIFO0
000064H	RDR0/TRD0 [R/W] -----0 00000000		BGR01 [R/W] 00000000	BGR00 [R/W] 00000000	
000068H	ISMK0 [R/W] 01111110	IBSA [R/W] 00000000	FCR01 [R/W] 00000000	FCR00 [R/W] 00000000	
00006CH	FBYTE01 [R/W] 00000000	FBYTE00 [R/W] 00000000	—		
000070H	SCR1/IBCR1 [R, R/W] 0--00000	SMR1 [W, R/W] 00000000	SSR1 [R, R/W] 0-000011	ESCR1/IBSR1 [R/W] --000000	
000074H	RDR1/TRD1 [R/W] -----0 00000000		BGR11 [R/W] 00000000	BGR10 [R/W] 00000000	Multi function Serial interface 1 FIFO1
000078H	ISMK1 [R/W] 01111110	IBSA1 [R/W] 00000000	FCR11 [R/W] 00000000	FCR10 [R/W] 00000000	
00007CH	FBYTE11 [R/W] 00000000	FBYTE10 [R/W] 00000000	—		
000080H	SCR2/IBCR2 [R, R/W] 0--00000	SMR2 [W, R/W] 00000000	SSR2 [R, R/W] 0-000011	ESCR2/IBSR2 [R/W] --000000	Multi function Serial interface 2
000084H	RDR2/TRD2 [R/W] -----0 00000000		BGR21 [R/W] 00000000	BGR20 [R/W] 00000000	
000088H	ISMK2 [R/W] 01111110	IBSA2 [R/W] 00000000	FCR21 [R/W] 00000000	FCR20 [R/W] 00000000	
00008CH	FBYTE21 [R/W] 00000000	FBYTE20 [R/W] 00000000	—		
000090H	SCR3/IBCR3 [R, R/W] 0--00000	SMR3 [W, R/W] 00000000	SSR3 [R, R/W] 0-000011	ESCR3/IBSR3 [R/W] --000000	Multi function Serial interface 3
000094H	RDR3/TRD3 [R/W] -----0 00000000		BGR31 [R/W] 00000000	BGR30 [R/W] 00000000	
000098H	ISMK3 [R/W] 01111110	IBSA3 [R/W] 00000000	—		
00009CH	—				

(Continued)

MB91314A Series

Address	Register				Block
	0	1	2	3	
0000A0 _H	SCR4/IBCR4 [R, R/W] 0--00000	SMR4 [W, R/W] 00000000	SSR4 [R, R/W] 0-000011	ESCR4/IBSR4 [R/W] --000000	Multi function Serial interface 4
0000A4 _H	RDR4/TRD4 [R/W] -----0 00000000		BGR41 [R/W] 00000000	BGR40 [R/W] 00000000	
0000A8 _H	ISMK4 [R/W] 01111110	IBSA4 [R/W] 00000000	—		
0000AC _H	—				
0000B0 _H	SCR5/IBCR5 [R, R/W] 0--00000	SMR5 [W, R/W] 00000000	SSR5 [R, R/W] 0-000011	ESCR5/IBSR5 [R/W] --000000	Multi function Serial interface 5
0000B4 _H	RDR5/TRD5 [R/W] -----0 00000000		BGR51 [R/W] 00000000	BGR50 [R/W] 00000000	
0000B8 _H	ISMK5 [R/W] 01111110	IBSA5 [R/W] 00000000	—		
0000BC _H	—				
0000C0 _H	EIRR1 [R/W] 00000000	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		Ext. INT 8 to INT15
0000C4 _H	EIRR2 [R/W] 00000000	ENIR2 [R/W] 00000000	ELVR2 [R/W] 00000000 00000000		Ext. INT 16 to INT23
0000C8 _H to 0000CC _H	—				Reserved
0000D0 _H	PWCCL[R/W] 0000--00	PWCCH[R/W] 00-00000	—		PWC
0000D4 _H	PWCD[R] XXXXXXXX XXXXXXXX		—		
0000D8 _H	PWCC2[R/W] 000-----	Reserved	—		
0000DC _H	PWCUD[R/W] XXXXXXXX XXXXXXXX		—		
0000E0 _H to 0000EC _H	—				Reserved
0000F0 _H	T0LPCR [R/W] ----000	T0CCR [R/W] 0-010000	T0TCR [R/W] 00000000	T0R [R/W] ---00000	Multifunction timer
0000F4 _H	T0DRR [R/W] XXXXXXXX XXXXXXXX		T0CRR [R/W] XXXXXXXX XXXXXXXX		

(Continued)

MB91314A Series

Address	Register				Block
	0	1	2	3	
0000F8 _H	T1LPCR [R/W] ----000	T1CCR [R/W] 0-000000	T1TCR [R/W] 00000000	T1R [R/W] ---00000	Multifunction timer
0000FC _H	T1DRR [R/W] XXXXXXXX XXXXXXXX		T1CRR [R/W] XXXXXXXX XXXXXXXX		
000100 _H	T2LPCR [R/W] ----000	T2CCR [R/W] 0-000000	T2TCR [R/W] 00000000	T2R [R/W] ---00000	
000104 _H	T2DRR [R/W] XXXXXXXX XXXXXXXX		T2CRR [R/W] XXXXXXXX XXXXXXXX		
000108 _H	T3LPCR [R/W] ----000	T3CCR [R/W] 0-000000	T3TCR [R/W] 00000000	T3R [R/W] ---00000	
00010C _H	T3DRR [R/W] XXXXXXXX XXXXXXXX		T3CRR [R/W] XXXXXXXX XXXXXXXX		
000110 _H	TMODE [R/W] -----0--		—		
000114 _H to 00011C _H	—				Reserved
000120 _H	PDUT0[W] XXXXXXXX XXXXXXXX		PCSR0[W] XXXXXXXX XXXXXXXX		PPG0
000124 _H	PTMR0[R] 11111111 11111111		PCNH0[R/W] 00000000	PCNL0[R/W] 00000000	
000128 _H	PDUT1[W] XXXXXXXX XXXXXXXX		PCSR1[W] XXXXXXXX XXXXXXXX		PPG1
00012C _H	PTMR1[R] 11111111 11111111		PCNH1[R/W] 00000000	PCNL1[R/W] 00000000	
000130 _H	PDUT2[W] XXXXXXXX XXXXXXXX		PCSR2[W] XXXXXXXX XXXXXXXX		PPG2
000134 _H	PTMR2[R] 11111111 11111111		PCNH2[R/W] 00000000	PCNL2[R/W] 00000000	
000138 _H	PDUT3[W] XXXXXXXX XXXXXXXX		PCSR3[W] XXXXXXXX XXXXXXXX		PPG3
00013C _H	PTMR3[R] 11111111 11111111		PCNH3[R/W] 00000000	PCNL3[R/W] 00000000	
000140 _H to 000144 _H	—				Reserved
000148 _H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload timer 3
00014C _H	—		TMCSR3 [R, RW] 00000000 00000000		

(Continued)

MB91314A Series

Address	Register				Block
	0	1	2	3	
000150 _H	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload timer 4
000154 _H	—		TMCSR4 [R, RW] 00000000 00000000		
000158 _H	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload timer 5
00015C _H	—		TMCSR5 [R, RW] 00000000 00000000		
000160 _H to 00019C _H	—				Reserved
0001A0 _H	PLLREG0[R/W] H ---00000 ---00000		PLLREG1[R/W] H ----0000 00000000		PLL of high multiplication
0001A4 _H	PLLREG2[R/W] H ----- 0000--0-		PLLREG3[R/W] H 0000---- ----00-0		
0001A8 _H to 0001AC _H	—				Reserved
0001B0 _H	SCR6/IBCR6 [R, R/W] 0--00000	SMR6 [W, R/W] 00000000	SSR6 [R, R/W] 0-000011	ESCR6/IBSR6 [R/W] --000000	Multi function Serial interface 6
0001B4 _H	RDR6/TRD6 [R/W] -----0 00000000		BGR61 [R/W] 00000000	BGR60 [R/W] 00000000	
0001B8 _H	ISMK6 [R/W] 01111110	IBSA6 [R/W] 00000000	—		
0001BC _H	—				
0001C0 _H	SCR7/IBCR7 [R, R/W] 0--00000	SMR7 [W, R/W] 00000000	SSR7 [R, R/W] 0-000011	ESCR7/IBSR7 [R/W] --000000	Multi function Serial interface 7
0001C4 _H	RDR7/TRD7 [R/W] -----0 00000000		BGR71 [R/W] 00000000	BGR70 [R/W] 00000000	
0001C8 _H	ISMK7 [R/W] 01111110	IBSA7 [R/W] 00000000	—		
0001CC _H	—				
0001D0 _H	SCR8/IBCR8 [R, R/W] 0--00000	SMR9 [W, R/W] 00000000	SSR8 [R, R/W] 0-000011	ESCR8/IBSR8 [R/W] --000000	Multi function Serial interface 8
0001D4 _H	RDR8/TRD8 [R/W] -----0 00000000		BGR81 [R/W] 00000000	BGR80 [R/W] 00000000	
0001D8 _H	ISMK8 [R/W] 01111110	IBSA8 [R/W] 00000000	—		
0001DC _H	—				

(Continued)

MB91314A Series

Address	Register				Block
	0	1	2	3	
0001E0 _H	SCR9/IBCR9 [R, R/W] 0--00000	SMR9 [W, R/W] 00000000	SSR9 [R, R/W] 0-000011	ESCR9/IBSR9 [R/W] --000000	Multi function Serial interface 9
0001E4 _H	RDR9/TRD9 [R/W] -----0 00000000		BGR91 [R/W] 00000000	BGR90 [R/W] 00000000	
0001E8 _H	ISMK9 [R/W] 01111110	IBSA9 [R/W] 00000000	—		
0001EC _H	—				
0001F0 _H	SCRA/IBCR9 [R, R/W] 0--00000	SMRA [W, R/W] 00000000	SSRA [R, R/W] 0-000011	ESCR9/IBSR9 [R/W] --000000	Multi function Serial interface 10
0001F4 _H	RDRA/TRDA [R/W] -----0 00000000		BGRA1 [R/W] 00000000	BGRA0 [R/W] 00000000	
0001F8 _H	ISMKA [R/W] 01111110	IBSAA [R/W] 00000000	—		
0001FC _H	—				
000200 _H	DMACA0 [R/W] 00000000 00000000 00000000 00000000				DMAC
000204 _H	DMACB0 [R/W] 00000000 00000000 00000000 00000000				
000208 _H	DMACA1 [R/W] 00000000 00000000 00000000 00000000				
00020C _H	DMACB1 [R/W] 00000000 00000000 00000000 00000000				
000210 _H	DMACA2 [R/W] 00000000 00000000 00000000 00000000				
000214 _H	DMACB2 [R/W] 00000000 00000000 00000000 00000000				
000218 _H	DMACA3 [R/W] 00000000 00000000 00000000 00000000				
00021C _H	DMACB3 [R/W] 00000000 00000000 00000000 00000000				
000220 _H	DMACA4 [R/W] 00000000 00000000 00000000 00000000				
000224 _H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000228 _H to 00023C _H	—				Reserved
000240 _H	DMACR [R/W] 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC

(Continued)

MB91314A Series

Address	Register				Block
	0	1	2	3	
000244 _H to 0003EC _H	—				Reserved
0003F0 _H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search
0003F4 _H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8 _H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC _H	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400 _H	DDR0 [R/W] B, H 00000000	DDR1 [R/W] B, H 00000000	DDR2 [R/W] B, H 00000000	DDR3 [R/W] B, H 00000000	Data direction register
000404 _H	DDR4 [R/W] B, H 00000000	DDR5 [R/W] B, H 00000000	DDR6 [R/W] B, H --000000	—	
000408 _H	—				
00040C _H	DDRC [R/W] B, H 00000000	DDRD [R/W] B, H 00000000	DDRE [R/W] B, H 00000000	—	
000410 _H	—				
000414 _H to 00041C _H	—				Reserved
000420 _H	PFR0 [R/W] B, H 00000000	PFR1 [R/W] B, H 00000000	PFR2 [R/W] B, H 00000000	PFR3 [R/W] B, H 00000000	Port function register
000424 _H	PFR4 [R/W] B, H 00000000	PFR5 [R/W] B, H 00000000	PFR6 [R/W] B, H --000000	—	
000428 _H	—				
00042C _H	PFRC [R/W] B, H 00000000	PFRD [R/W] B, H 00000000	PFRE [R/W] B, H 00000000	—	
000430 _H	—				Reserved
000434 _H to 00043C _H	—				

(Continued)

MB91314A Series

Address	Register				Block
	0	1	2	3	
000440 _H	ICR00 [R, R/W] ---11111	ICR01 [R, R/W] ---11111	ICR02 [R, R/W] ---11111	ICR03 [R, R/W] ---11111	Interrupt control unit
000444 _H	ICR04 [R, R/W] ---11111	ICR05 [R, R/W] ---11111	ICR06 [R, R/W] ---11111	ICR07 [R, R/W] ---11111	
000448 _H	ICR08 [R, R/W] ---11111	ICR09 [R, R/W] ---11111	ICR10 [R, R/W] ---11111	ICR11 [R, R/W] ---11111	
00044C _H	ICR12 [R, R/W] ---11111	ICR13 [R, R/W] ---11111	ICR14 [R, R/W] ---11111	ICR15 [R, R/W] ---11111	
000450 _H	ICR16 [R, R/W] ---11111	ICR17 [R, R/W] ---11111	ICR18 [R, R/W] ---11111	ICR19 [R, R/W] ---11111	
000454 _H	ICR20 [R, R/W] ---11111	ICR21 [R, R/W] ---11111	ICR22 [R, R/W] ---11111	ICR23 [R, R/W] ---11111	
000458 _H	ICR24 [R, R/W] ---11111	ICR25 [R, R/W] ---11111	ICR26 [R, R/W] ---11111	ICR27 [R, R/W] ---11111	
00045C _H	ICR28 [R, R/W] ---11111	ICR29 [R, R/W] ---11111	ICR30 [R, R/W] ---11111	ICR31 [R, R/W] ---11111	
000460 _H	ICR32 [R, R/W] ---11111	ICR33 [R, R/W] ---11111	ICR34 [R, R/W] ---11111	ICR35 [R, R/W] ---11111	
000464 _H	ICR36 [R, R/W] ---11111	ICR37 [R, R/W] ---11111	ICR38 [R, R/W] ---11111	ICR39 [R, R/W] ---11111	
000468 _H	ICR40 [R, R/W] ---11111	ICR41 [R, R/W] ---11111	ICR42 [R, R/W] ---11111	ICR43 [R, R/W] ---11111	
00046C _H	ICR44 [R, R/W] ---11111	ICR45 [R, R/W] ---11111	ICR46 [R, R/W] ---11111	ICR47 [R, R/W] ---11111	
000470 _H to 00047C _H	—				
000480 _H	RSRR [R, R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXXXX	Clock control unit
000484 _H	CLKR [R/W] 00000000	WPR [W] XXXXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488 _H	—		OSCCR [R/W] XXXXXXXXXX	—	
00048C _H	WPCR [R/W] B 00---000	—			Clock Timer
000490 _H	OSCR [R/W] 00000000	OSCT [R/W] XXXXXXXXXX	—		Main clock oscillation waits until stable timer
000494 _H to 0004FC _H	—				Reserved

(Continued)

MB91314A Series

Address	Register				Block
	0	1	2	3	
000500 _H	PCR0 [R/W] B, H 00000000	PCR1 [R/W] B, H 00000000	—		Port Pull-up control register
000504 _H	—	PCR5 [R/W] B, H 00000000	PCR6 [R/W] B, H --000000	—	
000508 _H to 000510 _H	—				
000514 _H to 00051C _H	—				Reserved
000520 _H	EPFR0 [R/W] B, H 00000000	EPFR1 [R/W] B, H 00000000	EPFR2 [R/W] B, H 11111111	EPFR3 [R/W] B, H 11111111	Extend Port Control Register
000524 _H	EPFR4 [R/W] B, H 11111111	EPFR5 [R/W] B, H 11111111	EPFR6 [R/W] B, H --001000	—	
000528 _H	—				Special Port Function Register
00052C _H	EPFRC [R/W] B, H 00000000	EPFRD [R/W] B, H 00000000	EPFRE [R/W] B, H 00000000	—	
000530 _H	—				Reserved
000534 _H to 00056C _H	—				
000570 _H	ADER[R/W] H 00000000 00000000		—		EXT/I ² C/ A/D converter
000574 _H	—				Reserved
000578 _H	NSF[R/W] -----000 00000000		—		I ² C noise filter
00057C _H to 00063C _H	—				Reserved
000640 _H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111XX00 00000000		T-Unit
000644 _H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648 _H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		

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MB91314A Series

Address	Register				Block
	0	1	2	3	
00064C _H	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		T-Unit
000650 _H to 00065C _H	—				
000660 _H	AWR0 [R/W] B, H, W 01111111 11111111		AWR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000664 _H	AWR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000668 _H to 00067C _H	—				
000680 _H	CSER[R/W]B, H, W 00000001	—			
000684 _H	—				
000688 _H to 0007F8 _H	—				Unused
0007FC _H	—	MODR [W] XXXXXXXX	—		—
000800 _H to 000AFC _H	—				Unused
000B00 _H	ESTS0 [R/W] B X0000000	ESTS1 [R/W] B XXXXXXXX	ESTS2 [R] B 1XXXXXXXX	—	DSU
000B04 _H	ECTL0 [R/W] B 0X000000	ECTL1 [R/W] B 00000000	ECTL2 [W] B 000X0000	ECTL3 [R/W] B 00X00X11	
000B08 _H	ECNT0 [W] B XXXXXXXX	ECNT1 [W] B XXXXXXXX	EUSA [W] B XXX00000	EDTC [W] B 0000XXXX	
000B0C _H	EWPT [R] H 00000000 00000000		ECTL4[R]([R/W])B -0X00000	ECTL5[R]([R/W])B ----000X	
000B10 _H	EDTR0 [W] H XXXXXXXX XXXXXXXX		EDTR1 [W] H XXXXXXXX XXXXXXXX		

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MB91314A Series

Address	Register				Block
	0	1	2	3	
000B14 _H to 000B1C _H	—				DSU
000B20 _H	EIA0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24 _H	EIA1 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B28 _H	EIA2 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B2C _H	EIA3 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30 _H	EIA4 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B34 _H	EIA5 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B38 _H	EIA6 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3C _H	EIA7 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40 _H	EDTA [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44 _H	EDTM [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B48 _H	EOA0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B4C _H	EOA1 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B50 _H	EPCR [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B54 _H	EPSR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B58 _H	EIAM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B5C _H	EIAM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B60 _H	EOAM0/EODM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B64 _H	EOAM1/EODM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

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MB91314A Series

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Address	Register				Block
	0	1	2	3	
000B68 _H	EOD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU
000B6C _H	EOD1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B70 _H to 000FFC _H	—				Reserved
001000 _H	DMASA0 [R/W] 00000000 00000000 00000000 00000000				DMAC
001004 _H	DMADA0 [R/W] 00000000 00000000 00000000 00000000				
001008 _H	DMASA1 [R/W] 00000000 00000000 00000000 00000000				
00100C _H	DMADA1 [R/W] 00000000 00000000 00000000 00000000				
001010 _H	DMASA2 [R/W] 00000000 00000000 00000000 00000000				
001014 _H	DMADA2 [R/W] 00000000 00000000 00000000 00000000				
001018 _H	DMASA3 [R/W] 00000000 00000000 00000000 00000000				
00101C _H	DMADA3 [R/W] 00000000 00000000 00000000 00000000				
001020 _H	DMASA4 [R/W] 00000000 00000000 00000000 00000000				
001024 _H	DMADA4 [R/W] 00000000 00000000 00000000 00000000				
001028 _H to 006FFC _H	—				Reserved
007000 _H	FLCR[R/W] 01101000			—	Flash I/F
007004 _H	FLWC[R/W] 00110011			—	

MB91314A Series

■ VECTOR TABLE

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA transfer	DMAC STOP factor
	Decimal	Hexadecimal					
Reset	0	00	—	3FC _H	000FFFFC _H	—	
Mode vector	1	01	—	3F8 _H	000FFFF8 _H	—	
System reserved	2	02	—	3F4 _H	000FFFF4 _H	—	
System reserved	3	03	—	3F0 _H	000FFFF0 _H	—	
System reserved	4	04	—	3EC _H	000FFFE _C	—	
System reserved	5	05	—	3E8 _H	000FFFE8 _H	—	
System reserved	6	06	—	3E4 _H	000FFFE4 _H	—	
Coprocessor absent trap	7	07	—	3E0 _H	000FFFE0 _H	—	
Coprocessor error trap	8	08	—	3DC _H	000FFFD _C	—	
INTE instruction	9	09	—	3D8 _H	000FFFD8 _H	—	
System reserved	10	0A	—	3D4 _H	000FFFD4 _H	—	
System reserved	11	0B	—	3D0 _H	000FFFD0 _H	—	
Step trace trap	12	0C	—	3CC _H	000FFFCC _H	—	
NMI request (tool)	13	0D	—	3C8 _H	000FFFC8 _H	—	
Undefined instruction exception	14	0E	—	3C4 _H	000FFFC4 _H	—	
System reserved	15	0F	15 (F _H) fixed	3C0 _H	000FFFC0 _H	—	
External interrupt 0	16	10	ICR00	3BC _H	000FFFB _C	—	
External interrupt 1	17	11	ICR01	3B8 _H	000FFFB8 _H	—	
External interrupt 2	18	12	ICR02	3B4 _H	000FFFB4 _H	—	
External interrupt 3	19	13	ICR03	3B0 _H	000FFFB0 _H	—	
External interrupt 4	20	14	ICR04	3AC _H	000FFFA _C	—	
External interrupt 5	21	15	ICR05	3A8 _H	000FFFA8 _H	—	
External interrupt 6	22	16	ICR06	3A4 _H	000FFFA4 _H	—	
External interrupt 7	23	17	ICR07	3A0 _H	000FFFA0 _H	—	
Reload timer 0	24	18	ICR08	39C _H	000FFF9 _C	—	
Reload timer 1	25	19	ICR09	398 _H	000FFF98 _H	—	
Reload timer 2	26	1A	ICR10	394 _H	000FFF94 _H	—	
UART0 RX/I ² C states	27	1B	ICR11	390 _H	000FFF90 _H	○	STOP
UART0 TX	28	1C	ICR12	38C _H	000FFF8 _C	○	
UART1 RX/I ² C states	29	1D	ICR13	388 _H	000FFF88 _H	○	STOP
UART1 TX	30	1E	ICR14	384 _H	000FFF84 _H	○	
UART2 RX/I ² C states	31	1F	ICR15	380 _H	000FFF80 _H	○	STOP
UART2 TX	32	20	ICR16	37C _H	000FFF7 _C	○	
UART3 RX/TX/I ² C states	33	21	ICR17	378 _H	000FFF78 _H	—	

(Continued)

MB91314A Series

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA transfer	DMAC STOP factor
	Decimal	Hexadecimal					
UART4 RX/TX/I ² C states	34	22	ICR18	374 _H	000FFF74 _H	—	
UART5 RX/TX/I ² C states	35	23	ICR19	370 _H	000FFF70 _H	—	
UART6 RX/TX/I ² C states	36	24	ICR20	36C _H	000FFF6C _H	—	
UART7 RX/TX/I ² C states	37	25	ICR21	368 _H	000FFF68 _H	—	
UART8 RX/TX/I ² C states	38	26	ICR22	364 _H	000FFF64 _H	—	
UART9 RX/TX/I ² C states	39	27	ICR23	360 _H	000FFF60 _H	—	
UART10 RX/TX/I ² C states	40	28	ICR24	35C _H	000FFF5C _H	—	
A/D converter	41	29	ICR25	358 _H	000FFF58 _H	—	
PPG0	42	2A	ICR26	354 _H	000FFF54 _H	○	
PWC	43	2B	ICR27	350 _H	000FFF50 _H	—	
CCD	44	2C	ICR28	34C _H	000FFF4C _H	—	
Watch timer	45	2D	ICR29	348 _H	000FFF48 _H	—	
Main oscillation wait	46	2E	ICR30	344 _H	000FFF44 _H	—	
Timebase timer	47	2F	ICR31	340 _H	000FFF40 _H	—	
Reload timer 3	48	30	ICR32	33C _H	000FFF3C _H	—	
Reload timer 4	49	31	ICR33	338 _H	000FFF38 _H	—	
Reload timer 5	50	32	ICR34	334 _H	000FFF34 _H	—	
PPG1	51	33	ICR35	330 _H	000FFF30 _H	○	
PPG2	52	34	ICR36	32C _H	000FFF2C _H	○	
PPG3	53	35	ICR37	328 _H	000FFF28 _H	○	
DMA0	54	36	ICR38	324 _H	000FFF24 _H	—	
DMA1	55	37	ICR39	320 _H	000FFF20 _H	—	
DMA2	56	38	ICR40	31C _H	000FFF1C _H	—	
DMA3	57	39	ICR41	318 _H	000FFF18 _H	—	
DMA4	58	3A	ICR42	314 _H	000FFF14 _H	—	
External interrupt 8 to 15	59	3B	ICR43	310 _H	000FFF10 _H	—	
External interrupt 16 to 23	60	3C	ICR44	30C _H	000FFF0C _H	—	
Multi-function timer 0, 1	61	3D	ICR45	308 _H	000FFF08 _H	—	
Multi-function timer 2, 3	62	3E	ICR46	304 _H	000FFF04 _H	—	
Delay interrupt source bit	63	3F	ICR47	300 _H	000FFF00 _H	—	
System reserved (Used by REALOS)	64	40	—	2FC _H	000FFEFC _H	—	
System reserved (Used by REALOS)	65	41	—	2F8 _H	000FFE8 _H	—	
System reserved	66	42	—	2F4 _H	000FFE4 _H	—	

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MB91314A Series

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	DMA transfer	DMAC STOP factor
	Decimal	Hexadecimal					
System reserved	67	43	—	2F0 _H	000FFEF0 _H	—	
System reserved	68	44	—	2EC _H	000FFEEC _H	—	
System reserved	69	45	—	2E8 _H	000FFEE8 _H	—	
System reserved	70	46	—	2E4 _H	000FFEE4 _H	—	
System reserved	71	47	—	2E0 _H	000FFEE0 _H	—	
System reserved	72	48	—	2DC _H	000FFEDC _H	—	
System reserved	73	49	—	2D8 _H	000FFED8 _H	—	
System reserved	74	4A	—	2D4 _H	000FFED4 _H	—	
System reserved	75	4B	—	2D0 _H	000FFED0 _H	—	
System reserved	76	4C	—	2CC _H	000FFEC _C	—	
System reserved	77	4D	—	2C8 _H	000FFEC8 _H	—	
System reserved	78	4E	—	2C4 _H	000FFEC4 _H	—	
System reserved	79	4F	—	2C0 _H	000FFEC0 _H	—	
Used by INT instruction	80 to 255	50 to FF	—	2BC _H to 000 _H	000FFEBC _H to 000FFC00 _H	—	

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V _{DDE} (3.3 V)	V _{SS} - 0.5	V _{SS} + 4.0	V	
	V _{DDI} (1.8 V)	V _{SS} - 0.3	V _{SS} + 2.5	V	
Analog power supply voltage	AV _{CC}	V _{SS} - 0.5	V _{SS} + 4.0	V	
Input voltage	V _I	V _{SS} - 0.5	V _{CC} + 0.5	V	
		V _{SS} - 0.5	V _{SS} + 6.0	V	5 V tolerant pin
Analog pin input voltage	V _{IA}	V _{SS} - 0.5	AV _{CC} + 0.5	V	
Output voltage	V _O	V _{SS} - 0.5	V _{CC} + 0.5	V	
Storage temperature	T _{stg}	- 40	+ 125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

Parameter	Symbol	Value		Unit
		Min	Max	
Operating temperature	T _a	- 10	+ 70	°C
Power supply voltage	V _{DDE} (3.3 V)	3.0	3.6	V
	V _{DDI} (1.8 V)	1.65	1.95	
Analog power supply voltage	AV _{CC}	3.0	V _{DDE}	V
5 V tolerant pin input voltage	V _I	—	V _{SS} + 5.5	V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

MB91314A Series

3. DC Characteristics

($V_{DDE} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Current Consumption (upper : 1.8 V lower : 3.3 V)	I _{CC} T	—	Clock mode	—	300	700	μA
		—	$T_a = +25 \text{ }^\circ\text{C}$, fclk = 32 kHz	—	700	1000	
	I _{CC}	—	During normal operation	—	100	120	mA
		—	$T_a = +25 \text{ }^\circ\text{C}$, fcp = 33 MHz, fcpp = 33 MHz	—	70	100	
	I _{CC} S	—	Main sleep mode	—	60	80	mA
		—	$T_a = +25 \text{ }^\circ\text{C}$, fcp = 33 MHz, fcpp = 33 MHz	—	60	90	
	I _{CC} L	—	Sub RUN mode	—	400	1000	μA
		—	$T_a = +25 \text{ }^\circ\text{C}$, fclk = 32 kHz	—	900	1300	
	I _{CC} H	—	Main Stop mode	—	160	600	μA
		—	$T_a = +25 \text{ }^\circ\text{C}$, fclk = 0	—	40	80	
—		$T_a = +70 \text{ }^\circ\text{C}$, fclk = 0	—	900	4000	μA	
—		—	240	400			
“H” level input voltage	V _{IH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P60 to P65, PD0 to PD7, PE0, PE1	V _{DDE} = 3.3 V	V _{DDE} × 0.8	—	V _{DDE}	V
		PE2 to PE7, PC0 to PC7, P40 to P47		V _{DDE} × 0.7	—	V _{DDE}	V
“L” level input voltage	V _{IL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57, P60 to P65, PD0 to PD7, PE0, PE1, HSYNC	V _{DDE} = 3.3 V	V _{SS}	—	V _{DDE} × 0.2	V
		PE2 to PE7, PC0 to PC7, P40 to P47		V _{SS}	—	V _{DDE} × 0.3	V
“H” level output voltage	V _{OH}	P00 to PE1	V _{DDE} = 3.3 V, I _{OH} = -4 mA	V _{DDE} - 0.5	—	V _{DDE}	V
“L” level output voltage	V _{OL}	P00 to PE1	V _{DDE} = 3.3 V, I _{OL} = 4 mA	V _{SS}	—	0.4	V

(Continued)

MB91314A Series

(Continued)

($T_a = -10\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Input leak current	I _{IL}	Other than PD0 to PD7, PE0, PE1	—	- 5	—	+ 5	μA
		PD0 to PD7, PE0, PE1		- 10	—	+ 10	μA
I ² C bus switch connection resistance	R _{BS}	Between P21 and P24 Between P22 and P25 Between P24 and P27 Between P25 and P30	—	—	—	130	Ω

MB91314A Series

4. AC Characteristics

(1) Clock Timing

($V_{DDE} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_c	X0, X1	—	10	16.5	33	MHz	PLL clock (self-oscillation 16.5 MHz doubled via PLL : internal operation at 33 MHz max.)
Sub clock frequency	f_{clk}	X0A, X1A	—	—	32.768	—	kHz	
Internal operating clock frequency	f_{CP}	—	—	—	—	33	MHz	CPU
	f_{CPP}			—	—	33	MHz	Peripheral
	f_{CPT}			—	—	16.5	MHz	External bus

(2) Clock Output Timing

($V_{DDE} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	60.7	—	ns	*1
CLK \uparrow \rightarrow CLK \downarrow	t_{CHCL}	CLK		$1/2 \times t_{CYC} - 3$	$1/2 \times t_{CYC} + 3$	ns	*2
CLK \downarrow \rightarrow CLK \uparrow	t_{CLCL}	CLK		$1/2 \times t_{CYC} - 3$	$1/2 \times t_{CYC} + 3$	ns	*3

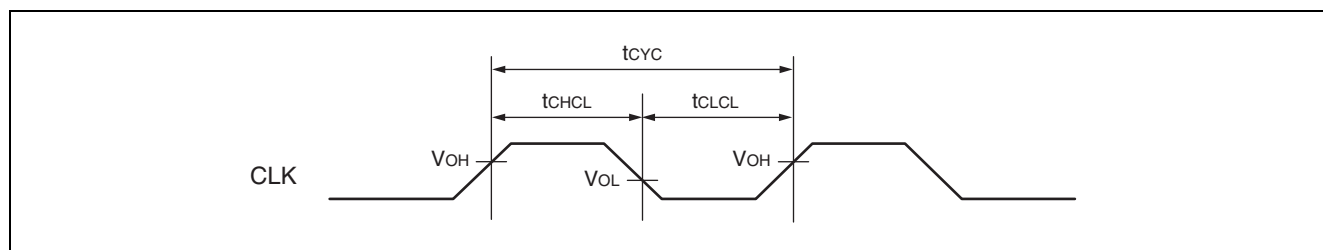
*1 : t_{CYC} is the frequency of one clock cycle after gearing.

*2 : The following ratings are for the gear ratio set to $\times 1$.

For the ratings when the gear ratio is set to between 1/2, 1/4 and 1/8, substitute 1/2, 1/4 or 1/8 for n in the following equation.

$$(1/2 \times 1/n) \times t_{CYC} - 10$$

*3 : The following rating are for the gear ratio set to $\times 1$.



(3) PLL Oscillation Stabilization Wait Time

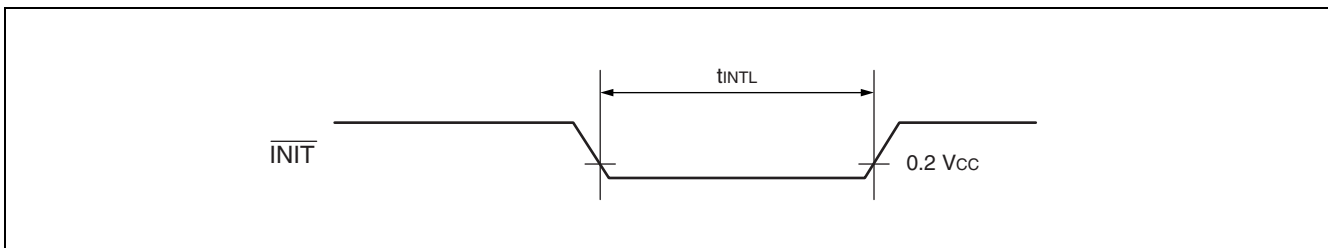
($V_{DDE} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
PLL oscillation stabilization wait time	t_{LOCK}	600	—	μs	The length of time to wait for the PLL oscillations to stabilize.

(4) Reset Input

($V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
$\overline{\text{INIT}}$ input time (at power-on)	t_{INTL}	$\overline{\text{INIT}}$	—	Oscillation stabilization delay time of oscillator + $t_{\text{cp}} \times 10$	—	μs
$\overline{\text{INIT}}$ input time (other than power-on)				$t_{\text{cp}} \times 10$	—	ns
$\overline{\text{INIT}}$ input time (Stop recovery time)				Oscillation stabilization delay time of oscillator + $t_{\text{cp}} \times 10$	—	μs



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(5) Multiplex Bus Access Read/Write Operation

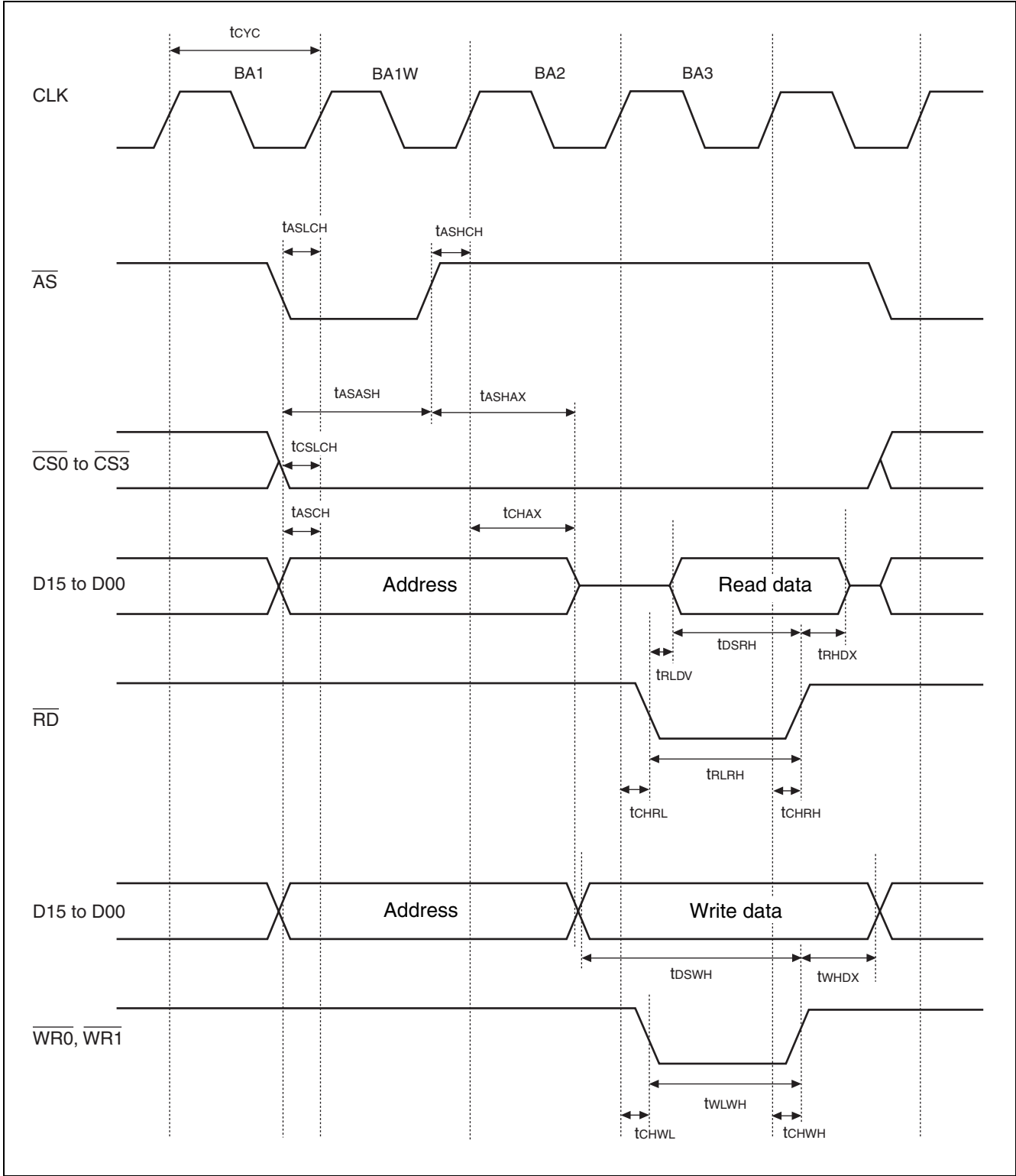
($V_{DDE} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS3}$ setup	t_{CSLCH}	CLK $\overline{CS0}$ to $\overline{CS3}$	—	3	—	ns	
D31 to D16 address setup time → CLK ↑	t_{ASCH}	CLK D31 to D16 (Address)		3	—	ns	
CLK ↑ → D31 to D16 address hold time	t_{CHAX}	CLK D31 to D16 (Address)		3	$t_{CYC} / 2 + 6$	ns	
D31 to D16 address setup time → \overline{AS} ↑	t_{ASASH}	\overline{AS} D31 to D16 (Address)		12	—	ns	*1
\overline{AS} ↑ → D31 to D16 address hold time	t_{ASHAX}	\overline{AS} D31 to D16 (Address)		$t_{CYC} - 3$	$t_{CYC} + 3$	ns	*1
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWL}	CLK $\overline{WR0}$, $\overline{WR1}$		—	6	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWH}	CLK $\overline{WR0}$, $\overline{WR1}$		—	6	ns	
$\overline{WR0}$, $\overline{WR1}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$, $\overline{WR1}$		$t_{CYC} - 3$	—	ns	
Data setup → \overline{WRx} ↑	t_{DSWH}	$\overline{WR0}$, $\overline{WR1}$ D15 to D00		t_{CYC}	—	ns	
\overline{WRx} ↑ → Data hold time	t_{WHDX}	$\overline{WR0}$, $\overline{WR1}$ D15 to D00		5	—	ns	
\overline{RD} delay time	t_{CHRL}	CLK \overline{RD}		—	6	ns	
\overline{RD} delay time	t_{CHRH}	CLK \overline{RD}		—	6	ns	
\overline{RD} ↓ → Valid data input time	t_{RLDV}	\overline{RD} D15 to D00		—	$t_{CYC} - 15$	ns	*2
Data setup → \overline{RD} ↑ Time	t_{DSRH}	\overline{RD} D15 to D00		15	—	ns	
\overline{RD} ↑ → Data hold time	t_{RHDX}	\overline{RD} D15 to D00		0	—	ns	
\overline{RD} minimum pulse width	t_{RLRH}	\overline{RD}		$t_{CYC} - 3$	—	ns	
\overline{AS} setup	t_{ASLCH}	CLK \overline{AS}		3	—	ns	
\overline{AS} hold	t_{ASHCH}	CLK \overline{AS}	3	—	ns		

*1 : At $\overline{CSx} \rightarrow \overline{RD}/\overline{WRx}$ setup extension = 1

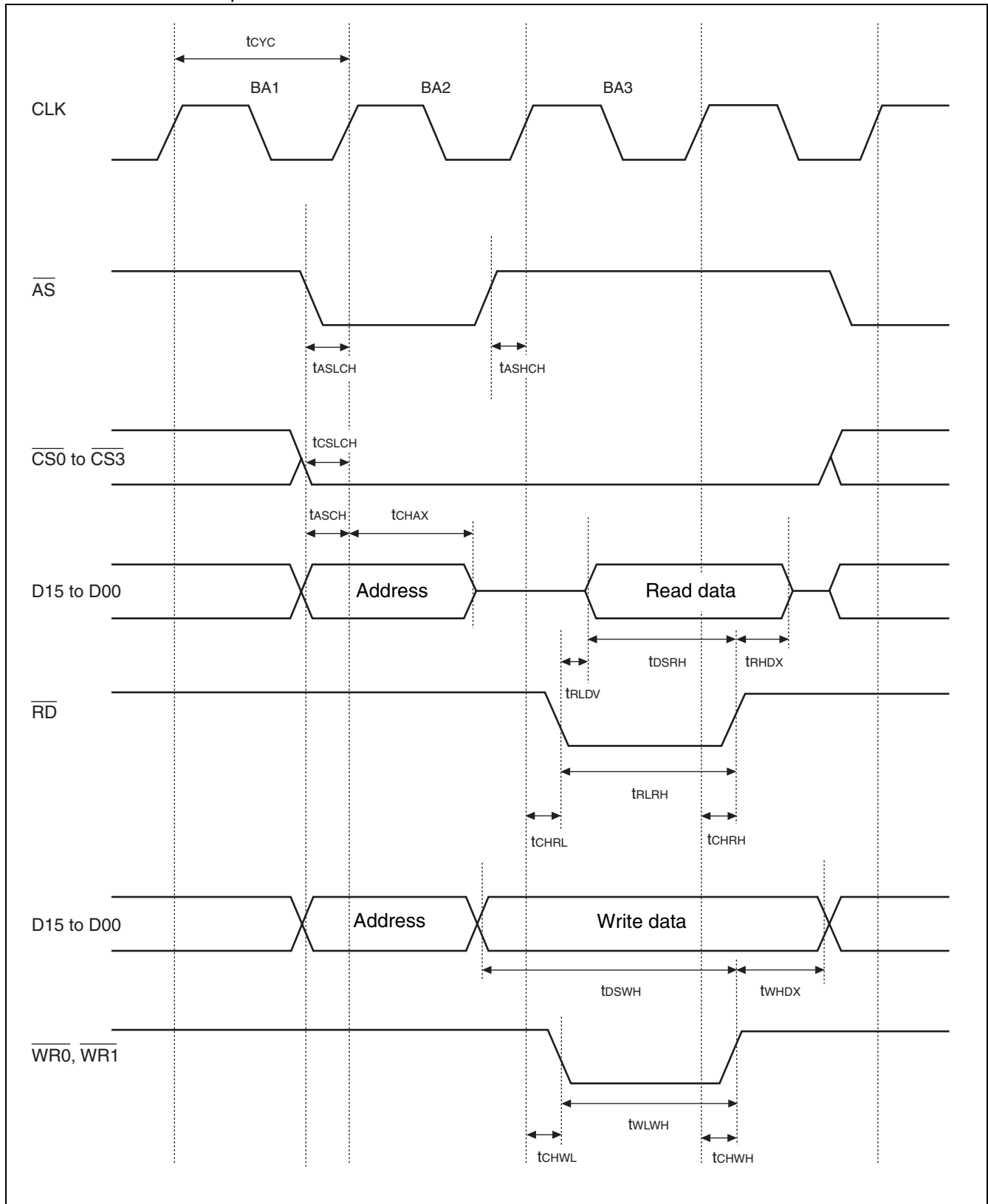
*2 : When the bus timing is delayed by automatic wait insertion or RDY input, add the time ($t_{CYC} \times$ the number of cycles added for the delay) to this rating.

• At $\overline{CS}_x \rightarrow \overline{RD}/\overline{WR}_x$ setup extension = 1



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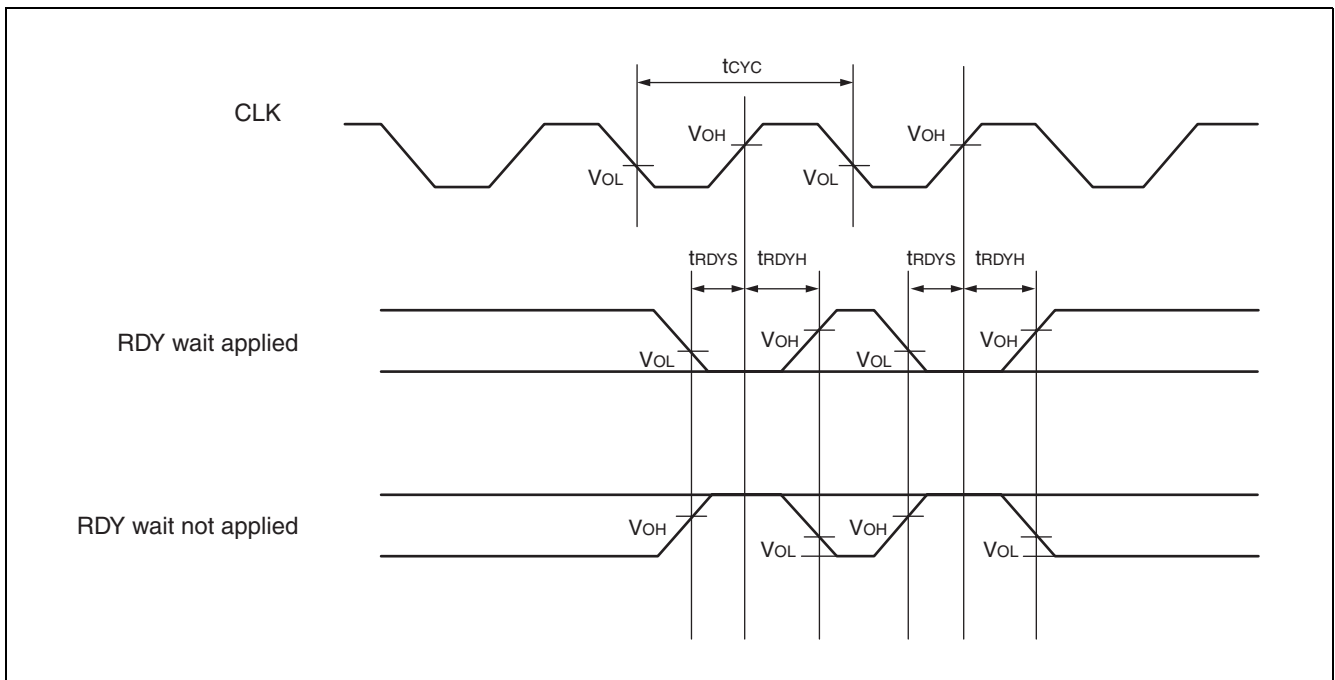
• At $\overline{CSx} \rightarrow \overline{RD}/\overline{WRx}$ setup extension = 0



(6) Ready Input Timings

($V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
RDY setup time → CLK ↓	t_{RDYS}	CLK, RDY	—	25	—	ns
CLK ↓ → RDY hold time	t_{RDYH}	CLK, RDY	—	0	—	ns



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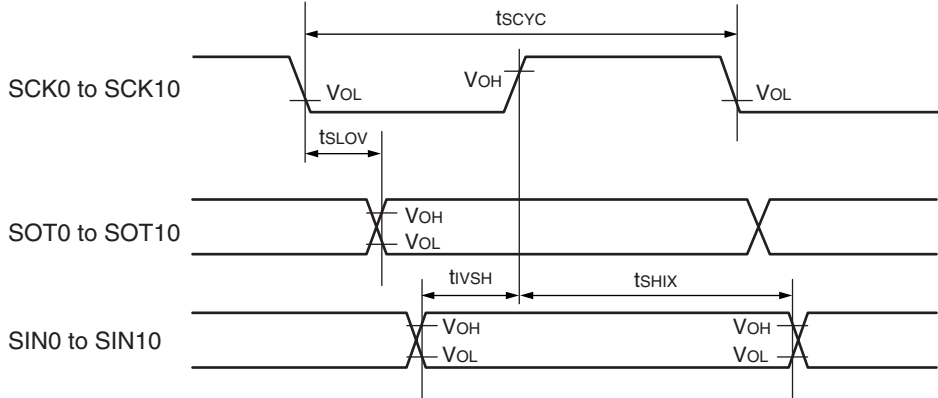
(7) UART timing

($V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

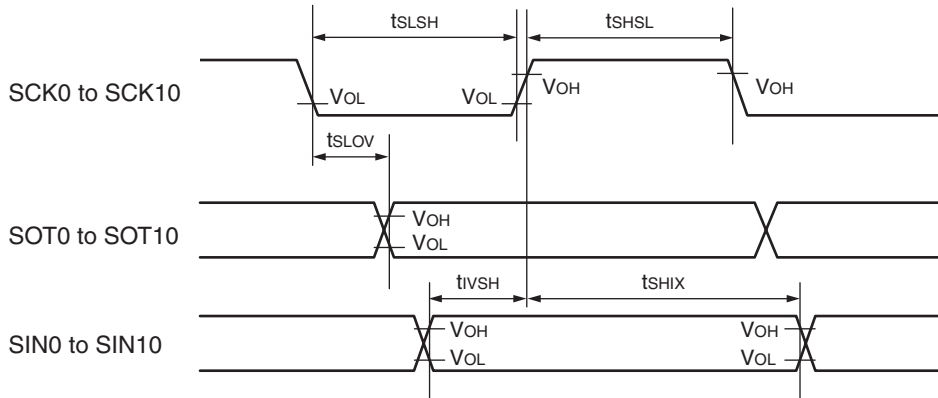
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK10	Internal shift clock operation	$4 t_{CYCP}$	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK10 SOT0 to SOT10		- 20	+ 20	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK10 SIN0 to SIN10		30	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK10 SIN0 to SIN10		20	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK10	External shift clock operation	$2 t_{CYCP}$	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK10		$2 t_{CYCP}$	—	ns
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK10 SOT0 to SOT10		—	30	ns
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK10 SIN0 to SIN10		20	—	ns
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK10 SIN0 to SIN10		20	—	ns

- Notes :
- The above standards apply to the CLK synchronous mode.
 - t_{CYCP} indicates the peripheral clock cycle time.

- Internal shift clock mode



- External shift clock mode



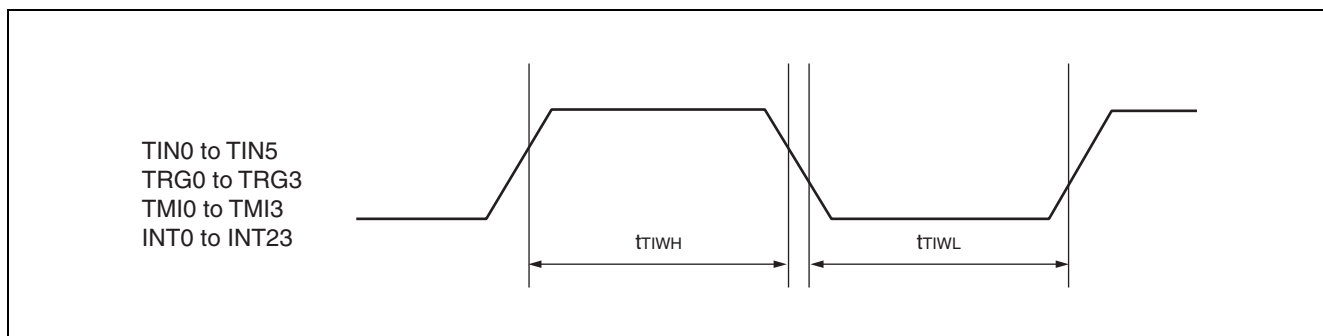
MB91314A Series

(8) Reload timer clock, PPG timer input, multi-function timer input timing, interrupt input timing

($V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0 to TIN5 TRG0 to TRG3 TMI0 to TMI3	—	$2 t_{CYCP}$	—	ns	
		INT0 to INT23	—	$3 t_{CYCP}$	—	ns	
					1.0	—	μs

Note : t_{CYCP} indicates the peripheral clock cycle time.

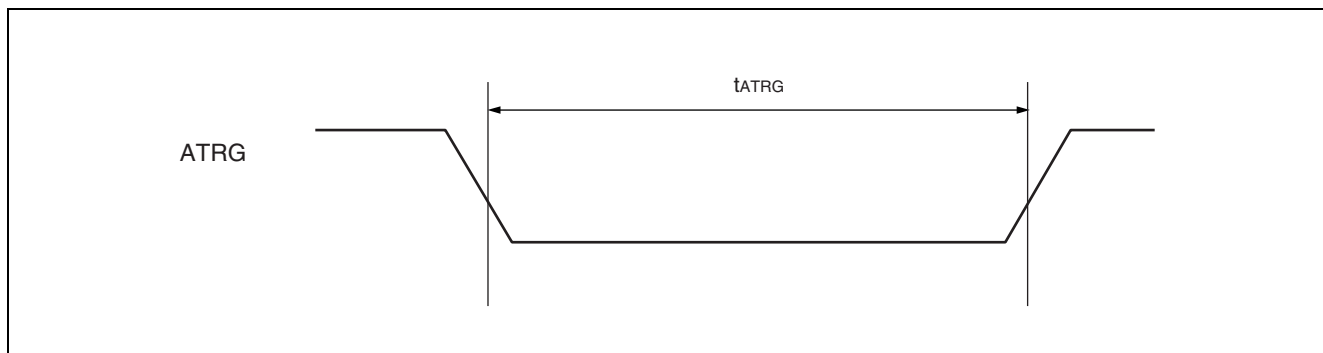


(9) Trigger Input Timing

($V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
A/D activation trigger input time	t_{ATRIG}	ATRIG	—	$5 t_{CYCP}$	—	ns

Note : t_{CYCP} indicates the peripheral clock cycle time.



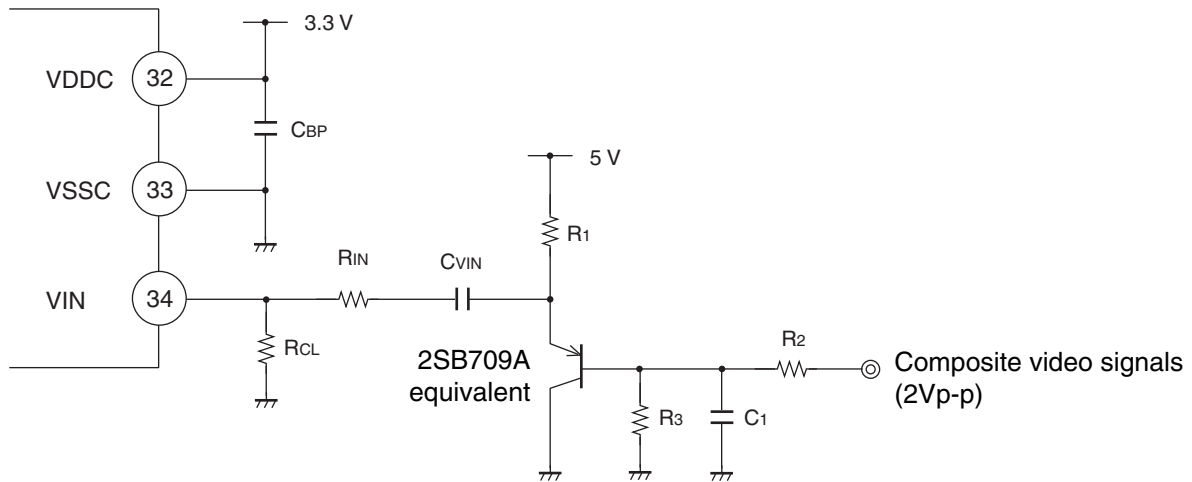
(10) External circuit for data slicer

($V_{DDE} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = -10 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

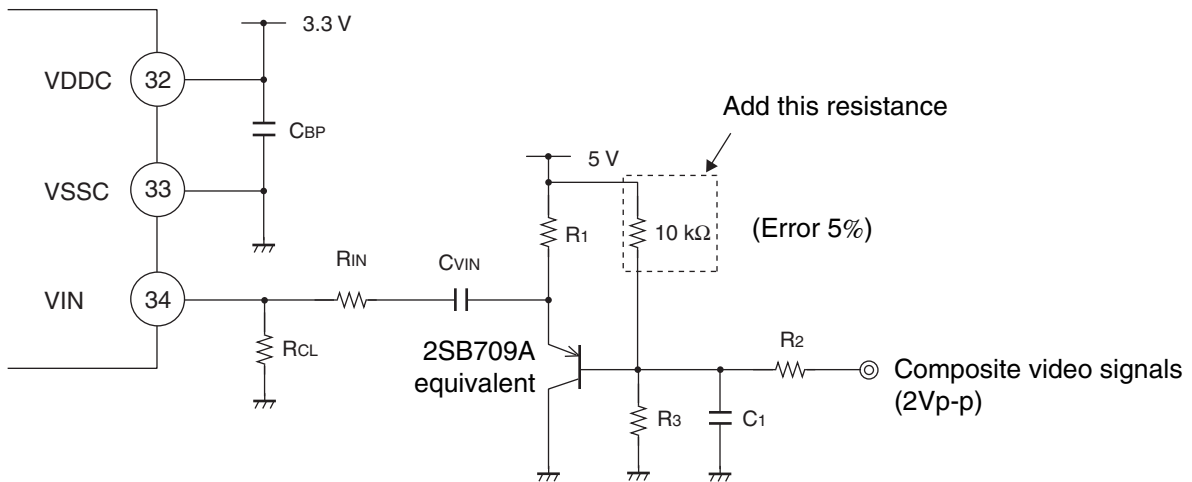
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Video signal input level	V_{VIN}	VIN	1.0	—	1.5	Vp-p	
VIN pin coupling capacitor	C_{VIN}	VIN	—	—	0.1	μF	Ceramic capacitor with an error of 10% exceeding B-characteristics
Resistance for clamp	R_{CL}	VIN	—	—	1	$\text{M}\Omega$	Error 5%
VIN pin input resistance	R_{IN}	VIN	—	—	0	Ω	Error 5%
VIN lowpass filter capacitor	C_1	—	—	—	82	pF	Ceramic capacitor with an error of 10% exceeding B-characteristics
Power supply bypass capacitor	C_{BP}	VDDC VSSC	—	—	0.1	μF	Ceramic condenser
Video signal input buffer resistance	R_1	—	—	—	2.2	$\text{k}\Omega$	Error 5%
Video signal level correction resistance	R_2	—	—	—	4.7	$\text{k}\Omega$	Error 5%
Video signal level correction resistance	R_3	—	—	10	12	$\text{k}\Omega$	Error 5%

MB91314A Series

- Input composite video signals are DC-clamped.



- Input composite video signals are not DC-clamped.



External recommended circuit for data slicer

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(11) I²C timing

- At master mode operating

($V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*3		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f _{SCL}	R = 1 kΩ, C = 50 pF*4	0	100	0	400	kHz	
"L" period of SCL clock	t _{LOW}		4.7	—	1.3	—	μs	
"H" period of SCL clock	t _{HIGH}		4.0	—	0.6	—	μs	
Bus free time between "STOP condition" and "START condition"	t _{BUS}		4.7	—	1.3	—	μs	
SCL ↓ → SDA output delay time	t _{DLDAT}		—	5 × M*1	—	5 × M*1	ns	
Repeated START condition setup time SCL ↑ → SDA ↓	t _{SUSTA}		4.7	—	0.6	—	μs	
Repeated START condition hold time SDA ↓ → SCL ↓	t _{HDSTA}		4.0	—	0.6	—	μs	The first clock pulse is generated after this.
STOP condition setup time SCL ↑ → SDA ↑	t _{SUSTO}		4.0	—	0.6	—	μs	
SDA data input hold time (vs. SCL ↓)	t _{HDDAT}		2 × M*1	—	2 × M*1	—	μs	
SDA data input setup time (vs. SCL ↑)	t _{SUDAT}		250	—	100*2	—	ns	

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- At slave mode operating

($V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*3		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	R = 1 k Ω , C = 50 pF*4	0	100	0	400	kHz	
“L” period of SCL clock	t_{LOW}		4.7	—	1.3	—	μs	
“H” period of SCL clock	t_{HIGH}		4.0	—	0.6	—	μs	
SCL $\downarrow \rightarrow$ SDA output delay time	t_{DLDAT}		—	$5 \times M^{*1}$	—	$5 \times M^{*1}$	ns	
Bus free time between “STOP condition” and “START condition”	t_{BUS}		4.7	—	1.3	—	μs	
SDA data input hold time (vs. SCL \downarrow)	t_{HDDAT}		$2 \times M^{*1}$	—	$2 \times M^{*1}$	—	μs	
SDA data input setup time (vs. SCL \uparrow)	t_{SUDAT}		250	—	100^{*2}	—	ns	
Repeated START condition setup time SCL $\uparrow \rightarrow$ SDA \downarrow	t_{SUSTA}		4.7	—	0.6	—	μs	
Repeated START condition hold time SDA $\downarrow \rightarrow$ SCL \downarrow	t_{HDSTA}		4.0	—	0.6	—	μs	The first clock pulse is generated after this.
STOP condition setup time SCL $\uparrow \rightarrow$ SDA \uparrow	t_{SUSTO}		4.0	—	0.6	—	μs	

*1 : M = Resource clock cycle (ns)

*2 : A high-speed mode I²C bus device can be used for a typical mode I²C bus system as long as the device satisfies a requirement of “ $t_{SUDAT} \geq 250\text{ ns}$ ”.

When a certain device does not extend the “L” period of the SCL signal, the next data must be output to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDAT}) in which the SCL line is released.

*3 : For use at over 100 kHz, set the resource clock to 6 MHz or higher.

*4 : R and C represent the pull-up resistor and load capacitor of the SCL and SDA output lines, respectively.

5. Electrical Characteristics for the A/D Converter

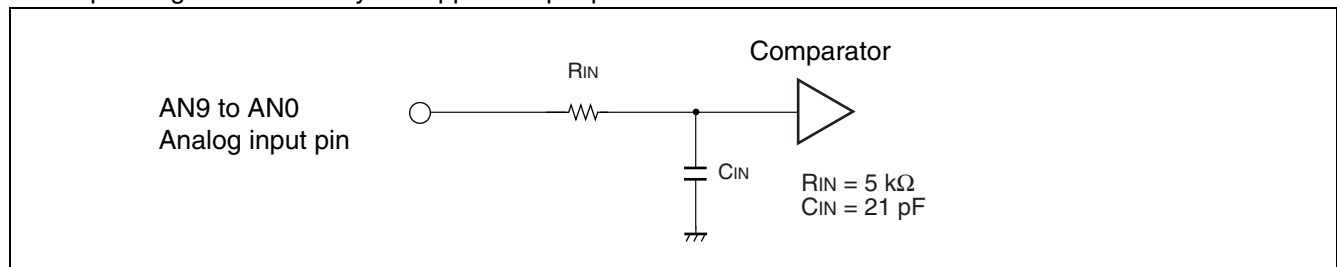
(1)Electrical Characteristics

($V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 1.8\text{ V} \pm 0.15\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	10	bit	
Total error *1	—	—	± 5.5	LSB	$AV_{CC} = 3.3\text{ V}$, $AV_{RH} = 3.3\text{ V}$ (CPU sleep)
Nonlinear error *1	—	—	± 3.5	LSB	
Differential linear error *1	—	—	± 2.0	LSB	
Zero transition voltage * 1	- 4.0	—	+ 6.0	LSB	
Full transition voltage*1	$AV_{RH} - 5.5$	—	$AV_{RH} + 3.0$	LSB	
Conversion time	7.94*2	—	—	μs	
Power supply current (analog + digital)	—	—	3	mA	
Reference power supply current (between AV_{RH} and AV_{RL})	—	—	100	μA	$AV_{RH} = 3.0\text{ V}$, $AV_{RL} = 0.0\text{ V}$
Analog input capacitance	—	—	21	pF	
Interchannel disparity	—	—	4	LSB	

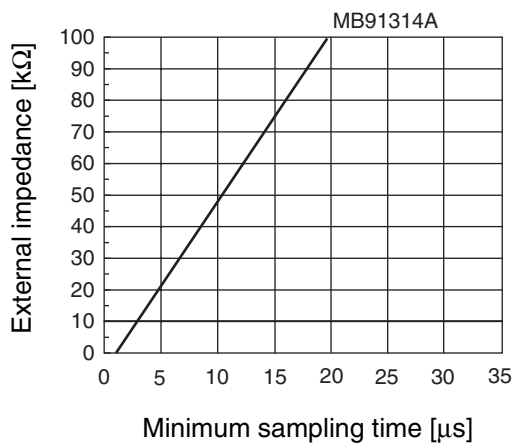
*1 : Measured in the CPU sleep state

*2 : Depending on the clock cycle supplied to peripheral resources

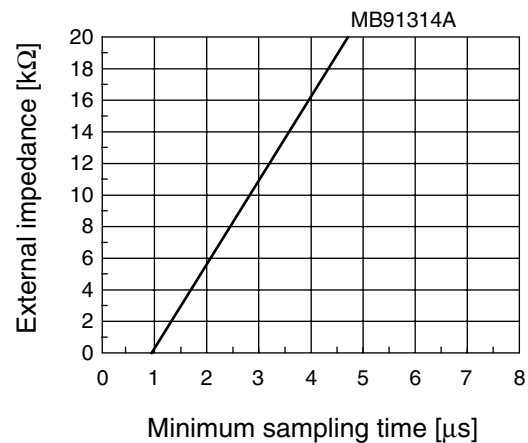


- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



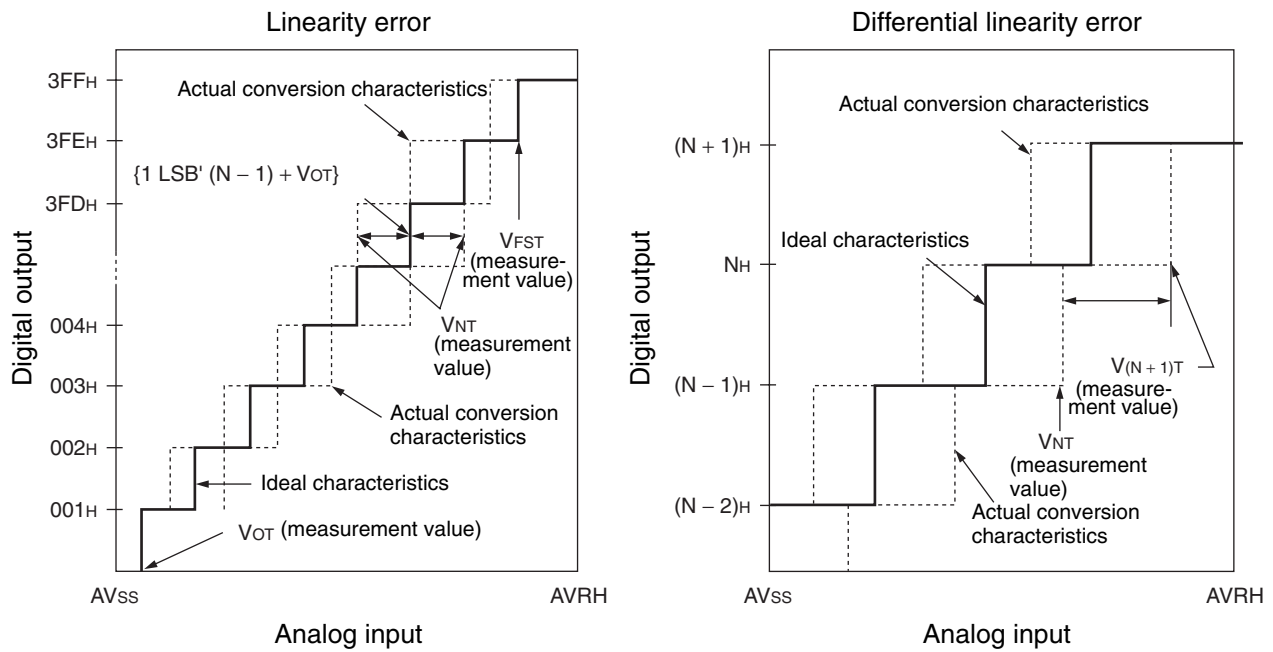
(External impedance = 0 kΩ to 20 kΩ)



MB91314A Series

(2) Definition of terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : The deviation between the actual conversion characteristics and a straight line connecting the device's zero transition point ("000000000" ↔ "000000001") and full scale transition point ("111111110" ↔ "111111111").
- Differential linear error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : This error indicates the difference between actual and ideal values, including the zero transition error/full-scale transition error/linearity error



$$\text{Linear error in digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + V_{OT}\}}{1 \text{ LSB}'} \text{ [LSB]}$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}'} - 1 \text{ [LSB]}$$

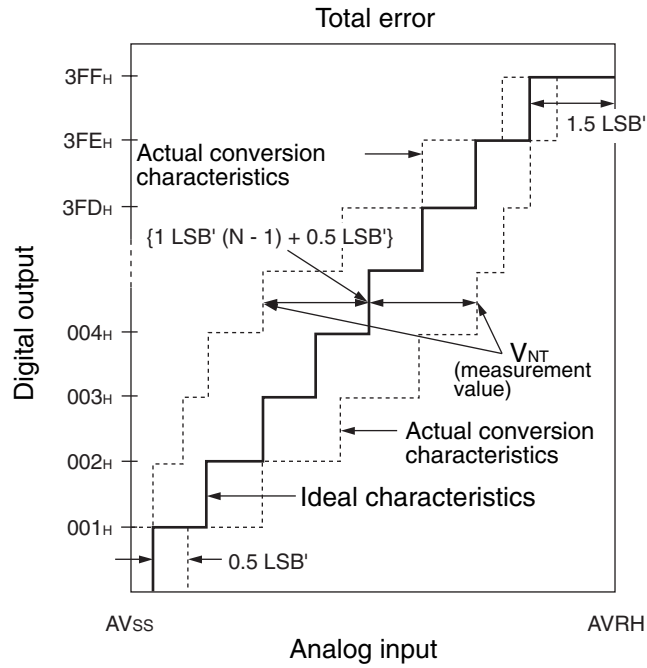
$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

V_{OT} : A voltage at which digital output transits from (000)_H to (001)_H

V_{FST} : A voltage at which digital output transits from (3FE)_H to (3FF)_H

V_{NT} : A voltage at which digital output transitions from (N-1)_H to N_H



$$1\text{LSB}' (\text{ideal value}) = \frac{\text{AVRH} - \text{AVSS}}{1024} [\text{V}]$$

$$\text{Total error of digital output } N = \frac{V_{\text{NT}} - \{1\text{LSB}' \times (N - 1) + 0.5\text{LSB}'\}}{1\text{LSB}'}$$

N : A/D converter digital output value

V_{NT} : A voltage at which digital output transits from (N + 1)_H to N_H

V_{OT'} (ideal value) = AV_{SS} + 0.5 LSB' [V]

V_{FST'} (ideal value) = AV_{RH} - 1.5 LSB' [V]

MB91314A Series

6. Flash Memory Write/Erase Characteristics

($T_a = +25\text{ }^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	—	0.5	2.0	s	Excludes internal programming prior erasure.
Byte write time	—	6	100	μs	Excludes system-level overhead.
Chip write time	—	1.8	29.5	s	Excludes system-level overhead.
Erase/write cycle	10000	—	—	cycle	

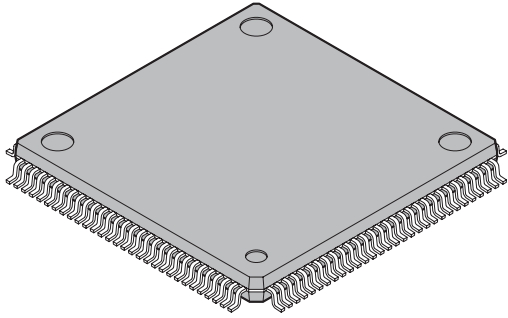
MB91314A Series

■ ORDERING INFORMATION

Part number	Package
MB91314APMC-GE1	120-pin plastic LQFP (FPT-120P-M21)
MB91F314PMC-GE1	

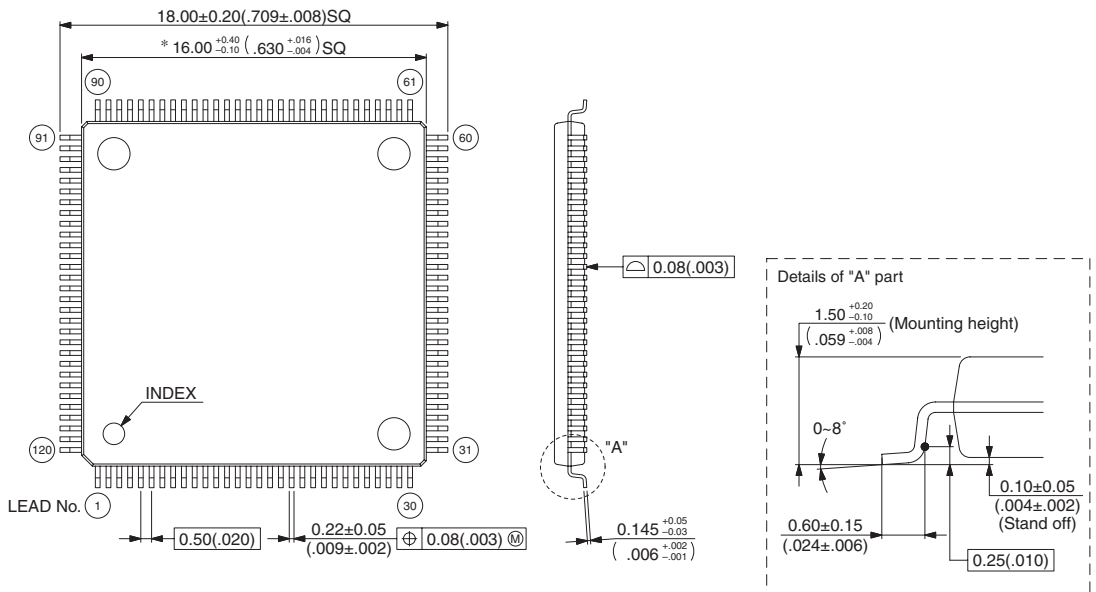
MB91314A Series

PACKAGE DIMENSION

<p>120-pin plastic LQFP</p>  <p>(FPT-120P-M21)</p>	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP (FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion. Resin protrusion is +0.25(.010) MAX(each side).
 Note 2) Pins width and pins thickness include plating thickness.
 Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
 Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/fj/DATASHEET/ef-ovpklv.html>

MB91314A Series

The information for microcontroller supports is shown in the following homepage.
<http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

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