

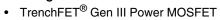
Vishay Siliconix

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)		
30	0.0019 at V _{GS} = 10 V	60	43.5 nC		
	0.00225 at $V_{GS} = 4.5 \text{ V}$	60	40.0110		

FEATURES



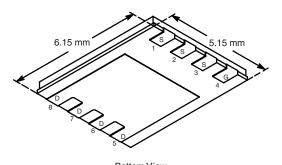




100 % Avalanche Tested

Po

PowerPAK® SO-8

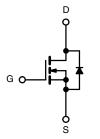


Bottom Viev

Ordering Information: Si7192DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- VRM, POL, Server
- High Current DC/DC
 - Low-Side



N-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V_{GS}	± 20	v	
	T _C = 25 °C		60 ^a		
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C	1-	60 ^a	7	
Continuous Brain Current (1) = 130 C)	T _A = 25 °C	I _D	42 ^{b, c}		
	T _A = 70 °C		34 ^{b, c}	A	
Pulsed Drain Current		I _{DM}	100	7 ^	
Continuous Source-Drain Diode Current	T _C = 25 °C	l _a	60 ^a		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	5.6 ^{b, c}		
Single Pulse Avalanche Current	l = 0.1 mH	I _{AS}	50		
Single Pulse Avalanche Energy L = 0.1 mH		E _{AS}	125	mJ	
	T _C = 25 °C		104		
Maximum Power Dissipation	T _C = 70 °C	P _D	66.6	w	
	T _A = 25 °C	' D	6.25 ^{b, c}	vv	
	T _A = 70 °C		4.0 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperature	_	260			

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	15	20	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	0.9	1.2] 0/**	

Notes:

- a. Package limited.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 54 °C/W.

Si7192DP

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SPECIFICATIONS $T_J = 25 ^{\circ}C$,	unless othe	rwise noted					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			٧	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	$\Delta V_{DS}/T_J$ $I_D = 250 \mu\text{A}$		26		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	η – 200 μπ		- 6.1		IIIV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1.0		2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	1		1		
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.00155	0.0019	Ω	
		$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$		0.00185	0.00225		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A		107		S	
Dynamic ^b			ı				
Input Capacitance	C _{iss}			5800		pF	
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1050			
Reverse Transfer Capacitance	C _{rss}			440			
		V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A		90	135	nC	
Total Gate Charge	Q_g	20 / 00 / 2		43.5	66		
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$		14			
Gate-Drain Charge	Q _{gd}			12.5			
Gate Resistance	R _g	f = 1 MHz		1.1	2	Ω	
Turn-On Delay Time	t _{d(on)}			15	30	ns	
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega$		10	20		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		47	80		
Fall Time	t _f			9	18		
Turn-On Delay Time	t _{d(on)}			41	75		
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega$		26	50		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		86	150		
Fall Time	t _f	Ç		32	60		
Drain-Source Body Diode Characteristic	cs				<u> </u>		
Continuous Source-Drain Diode Current	Is	T _C = 25 °C			60	А	
Pulse Diode Forward Current ^a	I _{SM}				100		
Body Diode Voltage	V _{SD}	I _S = 5 A		0.74	1.1	V	
Body Diode Reverse Recovery Time	t _{rr}	-		44	70	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			50	90	nC	
Reverse Recovery Fall Time	t _a	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		22			
Reverse Recovery Rise Time	t _b			22		ns	

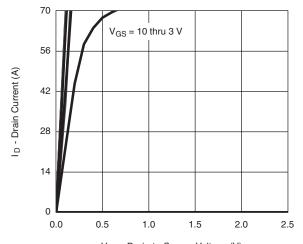
- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



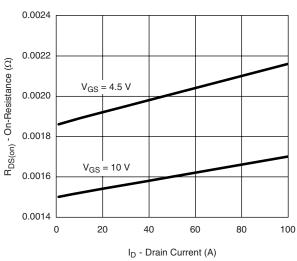
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

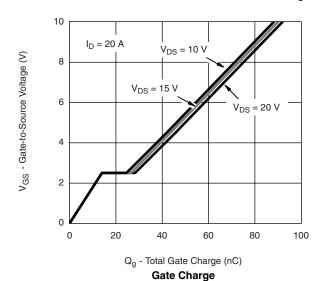


 $V_{\mbox{\footnotesize DS}}$ - Drain-to-Source Voltage (V)

Output Characteristics

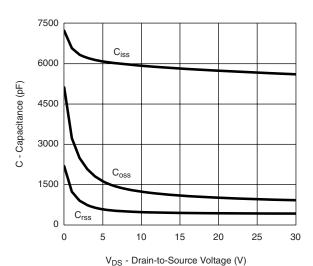


On-Resistance vs. Drain Current and Gate Voltage



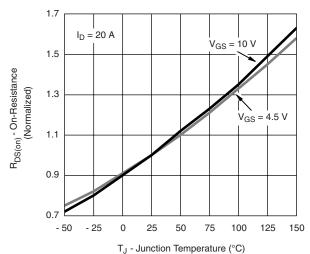
V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics



VDS - Diain-to-Source voltage (v)

Capacitance

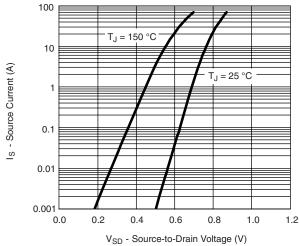


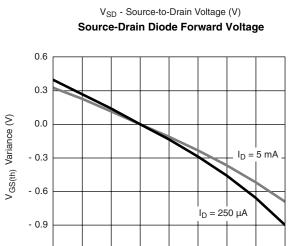
On-Resistance vs. Junction Temperature

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





T_J - Temperature (°C) **Threshold Voltage**

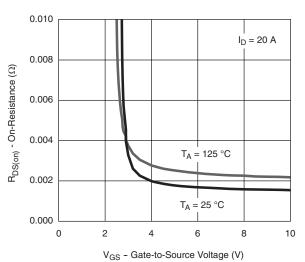
50

75

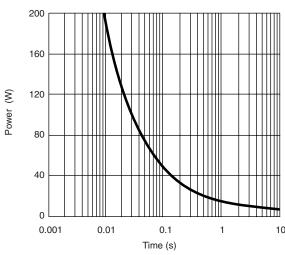
100

125

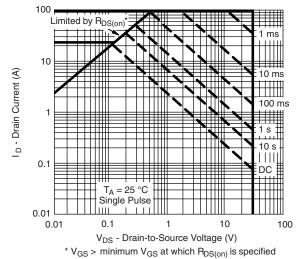
150



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

- 1.2

- 50

- 25

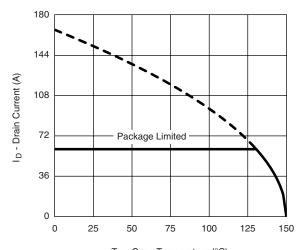
0

25



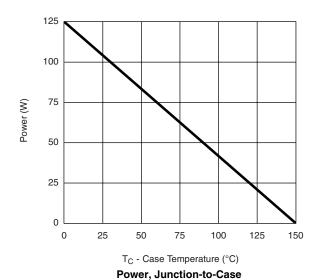
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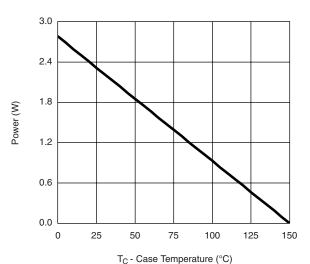
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



T_C - Case Temperature (°C)

Current Derating*





Power, Junction-to-Ambient

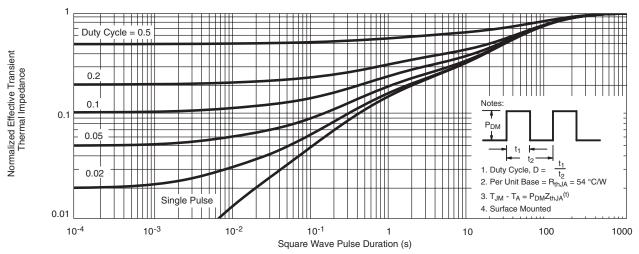
^{*} The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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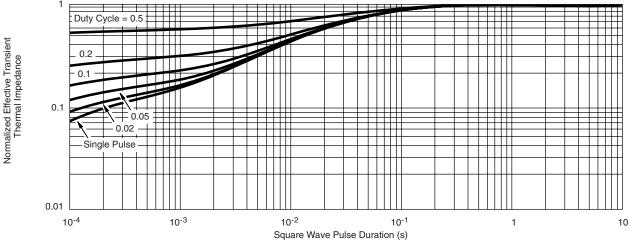
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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