Low Voltage Zero Delay Buffer

Features

- Fully Integrated PLL
- Up to 200MHz I/O Frequency
- LVCMOS Outputs
- Outputs Disable in High Impedance
- LVCMOS Reference Clock Options
- LQFP and TQFP Packaging
- ±50pS Cycle-Cycle Jitter
- 150pS Output Skews

Functional Description

The PCS5I961C is a 2.5V or 3.3V compatible, 1:18 PLL based zero delay buffer. With output frequencies of up to 200MHz, output skews of 150pS the device meets the needs of the most demanding clock tree applications.

The PCS5I961 is offered with two different input configurations. The PCS5I961C offers an LVCMOS reference clock while the PCS5I961P offers an LVPECL reference clock.

When pulled high the $\overline{OE}$ pin will force all of the outputs (except QFB) into a high impedance state. Because the $\overline{OE}$ pin does not affect the QFB output, down stream clocks can be disabled without the internal PLL losing lock.

The PCS5I961C is fully 2.5V or 3.3V compatible and requires no external loop filter components. All control inputs accept LVCMOS compatible levels and the outputs provide low impedance LVCMOS outputs capable of driving terminated 50Ω transmission lines. For series terminated lines the PCS5I961C can drive two lines per output giving the device an effective fanout of 1:36. The device is packaged in a 32 lead LQFP and TQFP Packages.

Block Diagram

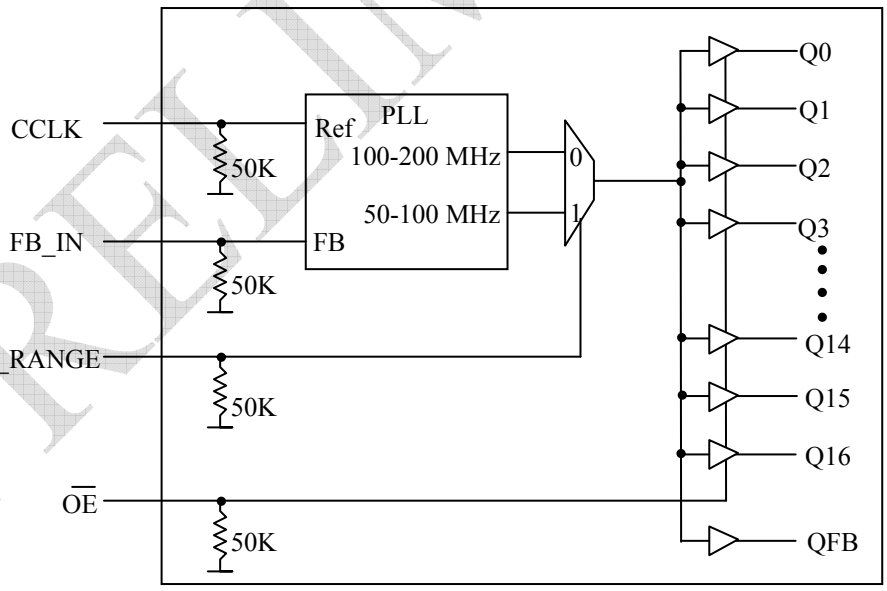
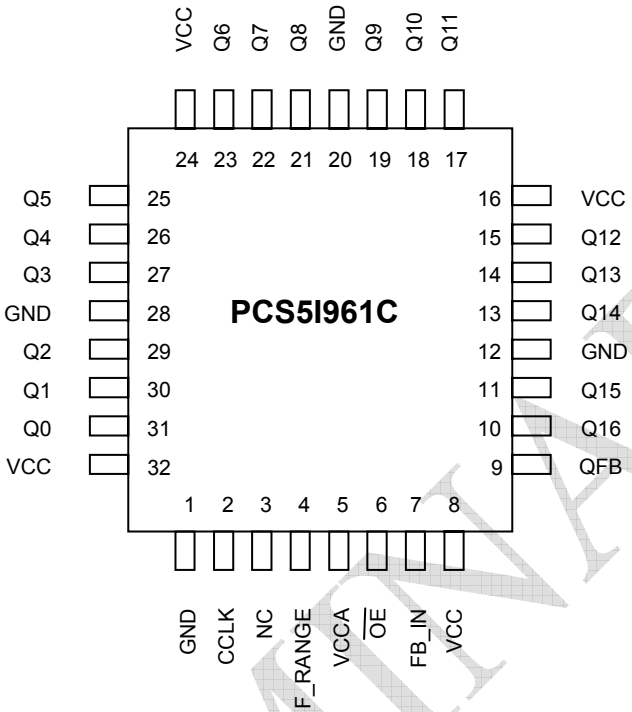


Figure 1. PCS5I961C Logic Diagram

Pin Configuration



c

Figure 2. PCS5I961C 32-Lead Package Pinout (Top View)

Table 1: Pin Configuration

Pin #	Pin Name	I/O	Type	Function
2	CCLK	Input	LVCMOS	PLL reference clock signal
7	FB_IN	Input	LVCMOS	PLL feedback signal input, connect to a QFB output
4	F_RANGE	Input	LVCMOS	PLL frequency range select
6	$\overline{OE}$	Input	LVCMOS	Output enable/disable
31,30,29,27,26,25,23,22,21, 19,18,17,15,14,13,11,10	Q0 - Q16	Output	LVCMOS	Clock outputs
9	QFB	Output	LVCMOS	PLL feedback signal output, connect to a FB_IN
1,12,20,28	GND	Supply	Ground	Negative power supply
5	VCCA	Supply	VCC	PLL positive power supply (analog power supply). The PCS5I961C requires an external RC filter for the analog power supply pin V_{CCA}. Please see applications section for details.
8,16,24,32	VCC	Supply	VCC	Positive power supply for I/O and core
3	NC			Not connected

Table 2: FUNCTION TABLE

Control	Default	0	1
F_RANGE	0	PLL high frequency range. PCS5I961C input reference and output clock frequency range is 100 – 200MHz	PLL low frequency range. PCS5I961C input reference and output clock frequency range is 50 – 100MHz
$\overline{OE}$	0	Outputs enabled	Outputs disabled (high–impedance state)

Table 3: ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	3.6	V
V_{IN}	DC Input Voltage	-0.3	V_{CC} + 0.3	V
V_{OUT}	DC Output Voltage	-0.3	V_{CC} + 0.3	V
I_{IN}	DC Input Current		±20	mA
I_{OUT}	DC Output Current		±50	mA
T_S	Storage Temperature Range	-40	125	°C

Note: 1 These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Table 4: DC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		VCC + 0.3	V	LVCMOS
V_{IL}	Input LOW Voltage	-0.3		0.8	V	LVCMOS
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA[1]
V_{OL}	Output LOW Voltage			0.55	V	I_{OL} = 20mA[1]
Z_{OUT}	Output Impedance		14	20	Ω	
I_{IN}	Input Current			±120	µA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current			TBD	mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage		V_{CC}÷2		V	

Note: 1. The PCS5I961C is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up two 50Ω series terminated transmission lines.

Table 5: AC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = 40°C to +85°C)[1]

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{max}	Maximum Output Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
t_r, t_f	TCLK Input Rise/Fall Time				3.0	nS	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)	CCLK to FB_IN	-80		120	pS	PLL locked
$t_{sk(O)}$	Output–to–Output Skew[2]			90	150	pS	
DC_O	Output Duty Cycle	F_RANGE = 0 F_RANGE = 1	42 45	50 50	55 55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	nS	0.55 to 2.4V
$t_{PLZ,HZ}$	Output Disable Time				10	nS	
$t_{PZL,LZ}$	Output Enable Time				10	nS	
$t_{JIT(CC)}$	Cycle–to–Cycle Jitter	RMS (1σ)[3]			15	pS	
$t_{JIT(PER)}$	Period Jitter	RMS (1σ)		7.0	10	pS	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1σ)			15	nS	
t_{lock}	Maximum PLL Lock Time				10	mS	

Note: 1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. See applications section for part–to–part skew calculation
3. See applications section for calculation for other confidence factors than 1σ

Table 6: DC CHARACTERISTICS (V_{CC} = 2.5V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	1.7		VCC + 0.3	V	LVCMOS
V_{IL}	Input LOW Voltage	-0.3		0.7	V	LVCMOS
V_{OH}	Output HIGH Voltage	1.8			V	I_{OH} = –15mA[1]
V_{OL}	Output LOW Voltage			0.6	V	I_{OL} = 15mA[1]
Z_{OUT}	Output Impedance		18	26	Ω	
I_{IN}	Input Current			±120	mA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current			TBD	mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage		V_{CC} ÷2		V	

Note: 1.The PCS5I961C is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up two 50Ω series terminated transmission lines.

Table 7: AC CHARACTERISTICS (V_{CC} = 2.5V ± 5%, T_A = 40°C to +85°C)[1]

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{max}	Maximum Output Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
t_r, t_f	TCLK Input Rise/Fall Time				3.0	nS	0.7 to 1.7V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)	CCLK to FB_IN	-80		120	pS	PLL locked
$t_{sk(O)}$	Output–to–Output Skew[2]			90	150	pS	
DC_O	Output Duty Cycle	F_RANGE = 0 F_RANGE = 1	40 45	50 50	60 55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	nS	0.6 to 1.8V
$t_{PLZ,HZ}$	Output Disable Time				10	nS	
$t_{PZL,LZ}$	Output Enable Time				10	nS	
$t_{JIT(CC)}$	Cycle–to–Cycle Jitter	RMS (1σ)[3]			15	pS	
$t_{JIT(PER)}$	Period Jitter	RMS (1σ)		7.0	10	pS	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1σ)			15	nS	
t_{lock}	Maximum PLL Lock Time				10	mS	

Note: 1 AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2 See applications section for part–to–part skew calculation
3 See applications section for calculation for other confidence factors than 1σ

APPLICATIONS INFORMATION

Power Supply Filtering

The PCS5I961C is a mixed analog/digital product and as such it exhibits some sensitivity that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The PCS5I961C provides separate power supplies for the output buffers (V_{CC}) and the phase–locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the PCS5I961C.

Figure 3. illustrates a typical power supply filter scheme. The PCS5I961C is most susceptible to noise with spectral content in the 10KHz to 10MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the PCS5I961C. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 2mA (5mA maximum), assuming that a minimum of 2.375V (V_{CC} = 3.3V or V_{CC} = 2.5V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 3. must have a resistance of 270Ω (V_{CC} = 3.3V) or 5 to 15Ω (V_{CC} = 2.5V) to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

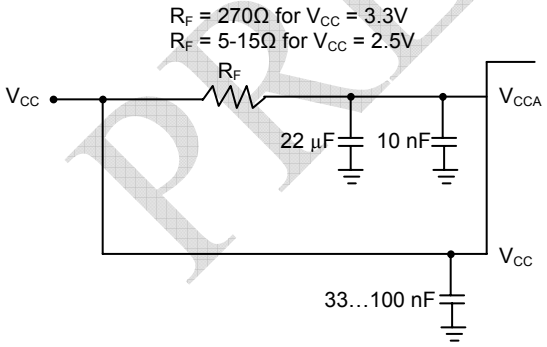


Figure 3. Power Supply Filter

Although the PCS5I961C has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The PCS5I961C clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15Ω the drivers can drive either parallel or series terminated transmission lines. In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the PCS5I961C clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4. illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the PCS5I961C clock driver is effectively doubled due to its capability to drive multiple lines.

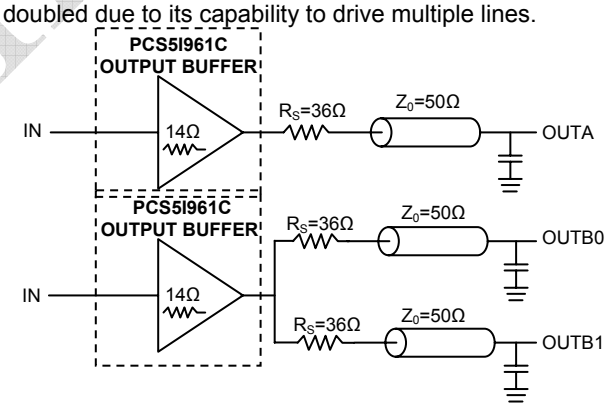


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5. show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the PCS5I961C output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43pS exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the PCS5I961C. The output waveform in Figure 5. shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the

output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS (Zo / (Rs + Ro +Zo))
Zo = 50Ω || 50Ω
Rs = 36Ω || 36Ω
Ro = 14Ω
VL = 3.0 (25 / (18 + 14 + 25) = 3.0 (25 / 57)
= 1.31V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0nS).

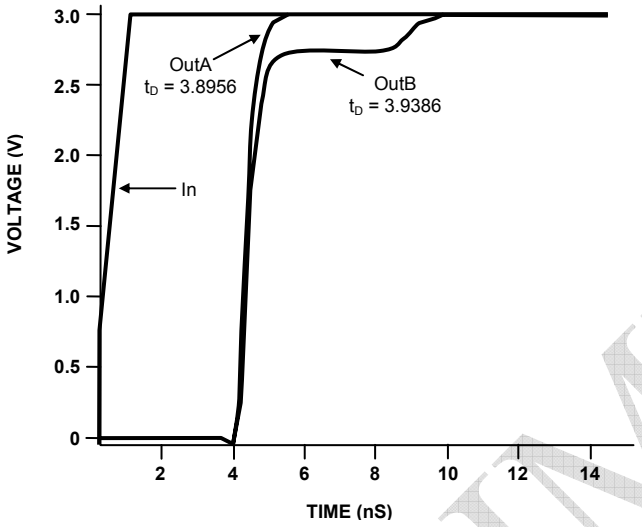
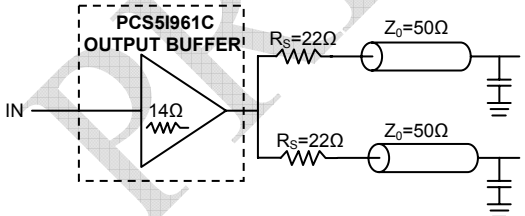


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6. should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



14Ω + 22Ω ‖ 22Ω = 50Ω ‖ 50Ω
25Ω = 25Ω

Figure 6. Optimized Dual Line Termination

Using the PCS5I961C in zero-delay applications

Nested clock trees are typical applications for the PCS5I961C. Designs using the PCS5I961C as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the PCS5I961C clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The PCS5I961C zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more PCS5I961C are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$t_{SK(PP)} = t_{(\varphi)} + t_{SK(O)} + t_{PD}, L_{INE(FB)} + t_{JIT(\varphi)}$ CF

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

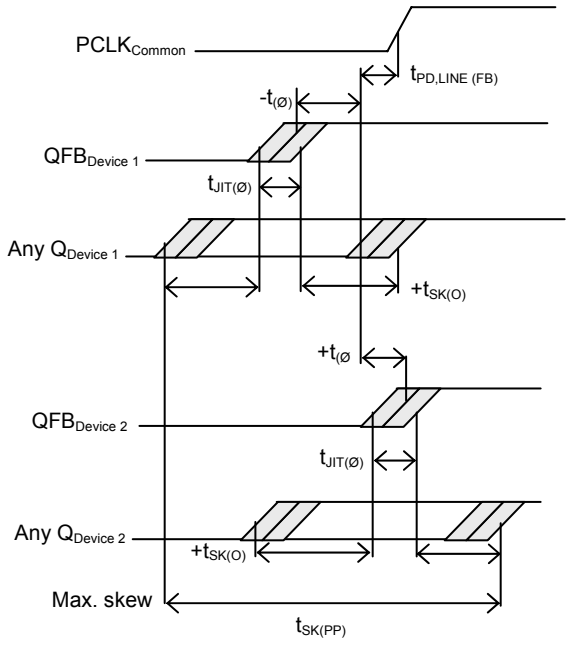


Figure 7. PCS5I961C max. device-to-device skew

Due to the statistical nature of I/O jitter a rms value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8: Confidence Factor C_F

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3 σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -275 pS to 315 pS relative to CCLK:

$t_{SK(PP)}$ = *[–80pS...120pS] + [–150pS...150pS] + [(15pS* –3)...(15pS* 3)] +* $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = *[–275pS...315pS]* + $t_{PD,\ LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 8. “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

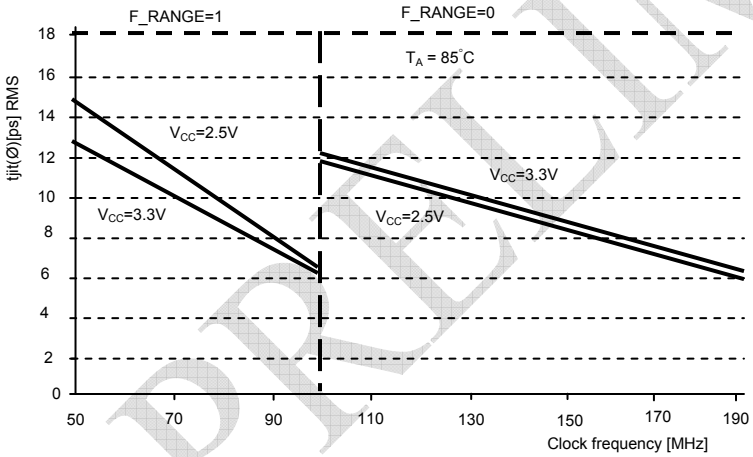


Figure 8. Max. I/O Jitter versus frequency

Power Consumption of the PCS5I961C and Thermal Management

The PCS5I961C AC specification is guaranteed for the entire operating frequency range up to 200MHz. The PCS5I961C power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the PCS5I961C die junction temperature and the associated device reliability.

Table 9: Die junction temperature and MTBF

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the PCS5I961C needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the PCS5I961C is represented in equation 1. Where I_{CCQ} is the static current consumption of the PCS5I961C, CPD is the power dissipation capacitance per output, (M)ΣC_L represents the external capacitive output load, N is the number of active outputs (N is always 27 in case of the PCS5I961C). The PCS5I961C supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation. In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL}, I_{OL}, V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \quad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[DC_Q \cdot I_{OH} \left(V_{CC} - V_{OH} \right) + \left(1 - DC_Q \right) \cdot I_{OL} \cdot V_{OL} \right] \quad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \quad \text{Equation 3}$$

$$f_{CLOCKMAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{JMAX} - T_A}{R_{thja}} - \left(I_{CCQ} \cdot V_{CC} \right) \right] \quad \text{Equation 4}$$

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 9, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the PCS5I961C in a series terminated transmission line system.

Table 10: Thermal package impedance of the 32LQFP

Convection, LFPM	Rthja (1P2S board), °C/W
Still air	80
100 lfpm	70
200 lfpm	61
300 lfpm	57
400 lfpm	56
500 lfpm	55

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 9. R_{thja} can be derived from Table 10. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below. If the calculated maximum frequency is below 200MHz, it becomes the upper clock speed limit for the given application conditions. The following two derating charts describe the safe frequency operation range for the PCS5I961C. The charts were calculated for a maximum tolerable die junction temperature of 110°C, corresponding to an estimated MTBF of 9.1 years, a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made. There are no operating frequency limitations if a 2.5V power supply or the system specifications allow for a MTBF of 4 years (corresponding to a max. junction temperature of 120°C.

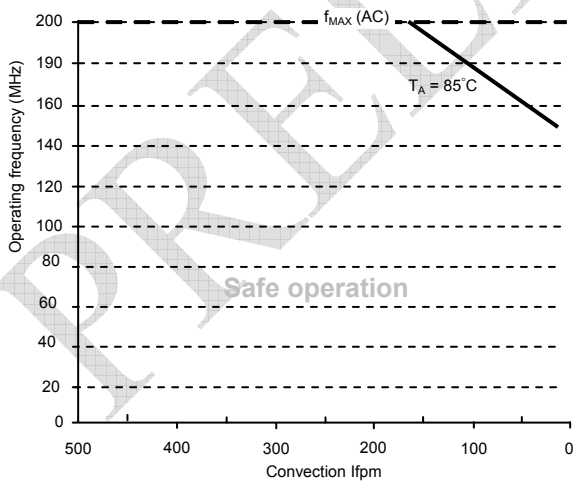


Figure 9. Maximum PCS5I961C frequency, V_{CC} = 3.3V, MTBF 9.1 years, driving series terminated transmission lines

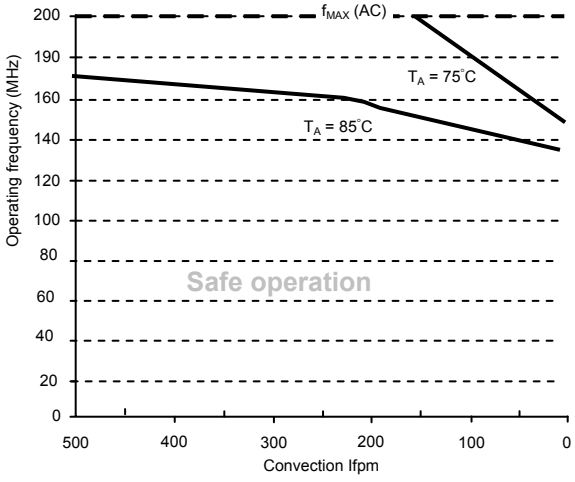


Figure 10. Maximum PCS5I961C frequency, V_{CC} = 3.3V, MTBF 9.1 years,4pF load per line

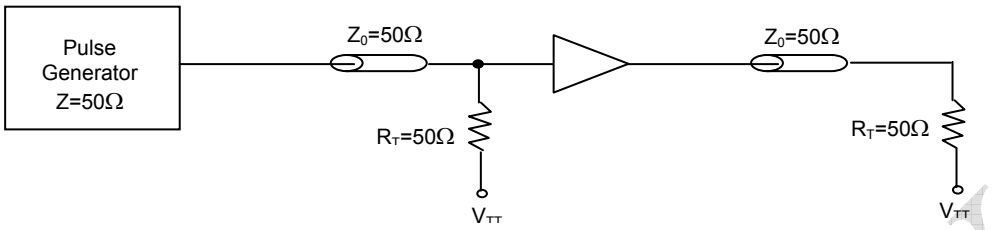
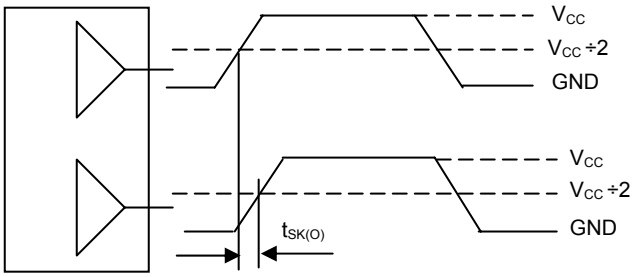


Figure 11. TCLK PCS5I961C AC test reference for V_{CC} = 3.3V and V_{CC} = 2.5V



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 12. Output–to–Output Skew $t_{SK(O)}$

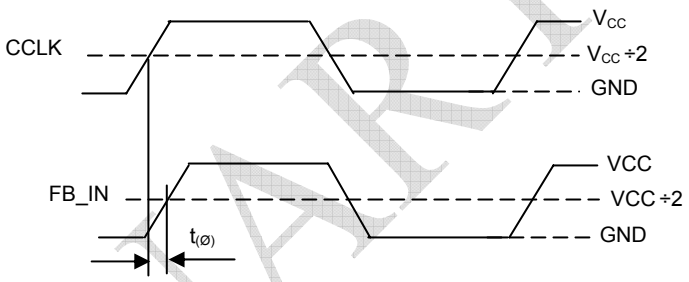
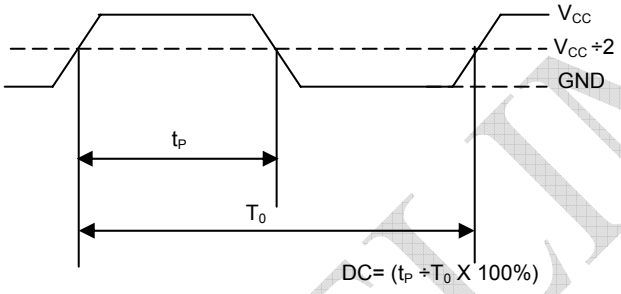
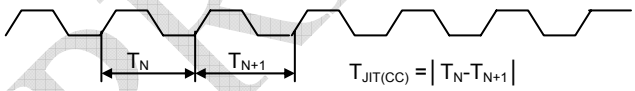


Figure 13. Propagation delay (t_{PD}, static phase offset) test reference



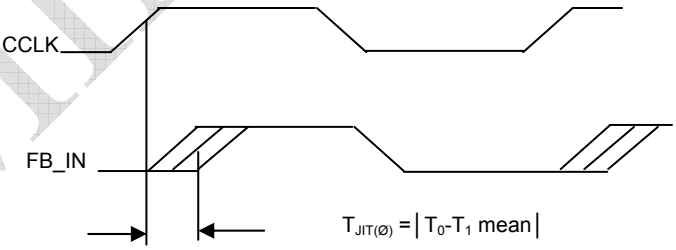
The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 14. Output Duty Cycle (DC)



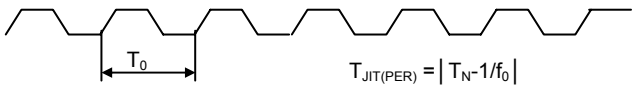
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-cycle Jitter



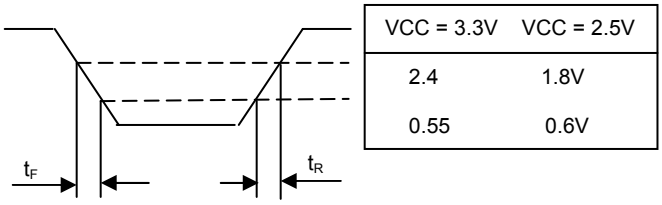
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 15.I/O Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 17. Period Jitter

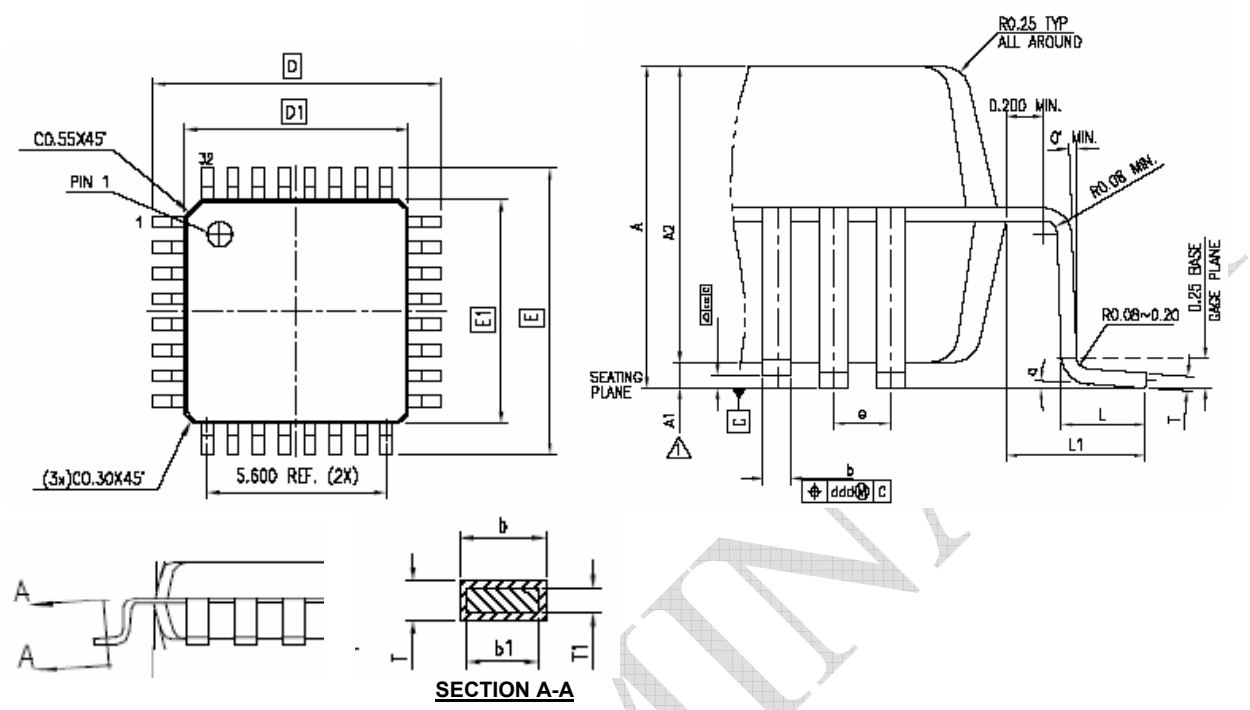


VCC = 3.3V	VCC = 2.5V
2.4	1.8V
0.55	0.6V

Figure 18. Output Transition Time Test Reference

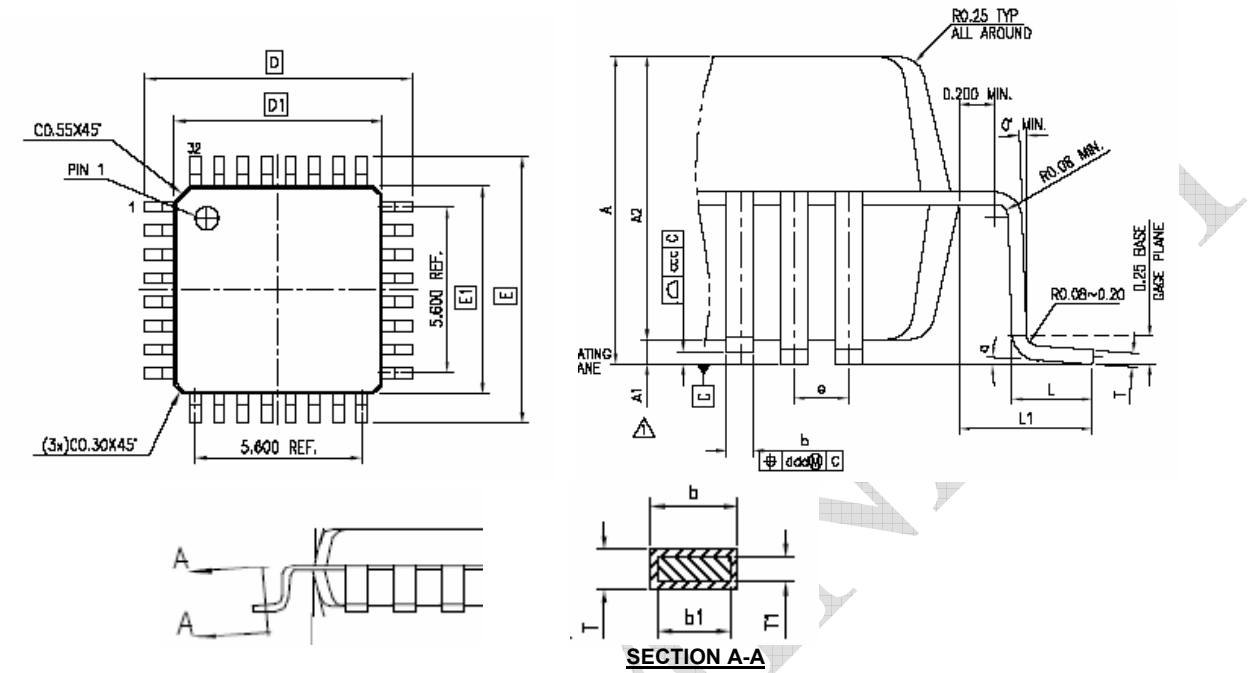
Package Diagram

32-lead TQFP



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	....	0.0472	...	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.0374	0.0413	0.95	1.05
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.2
a	0°	7°	0°	7°
e	0.031 BASE		0.8 BASE	

32-lead LQFP



SECTION A-A

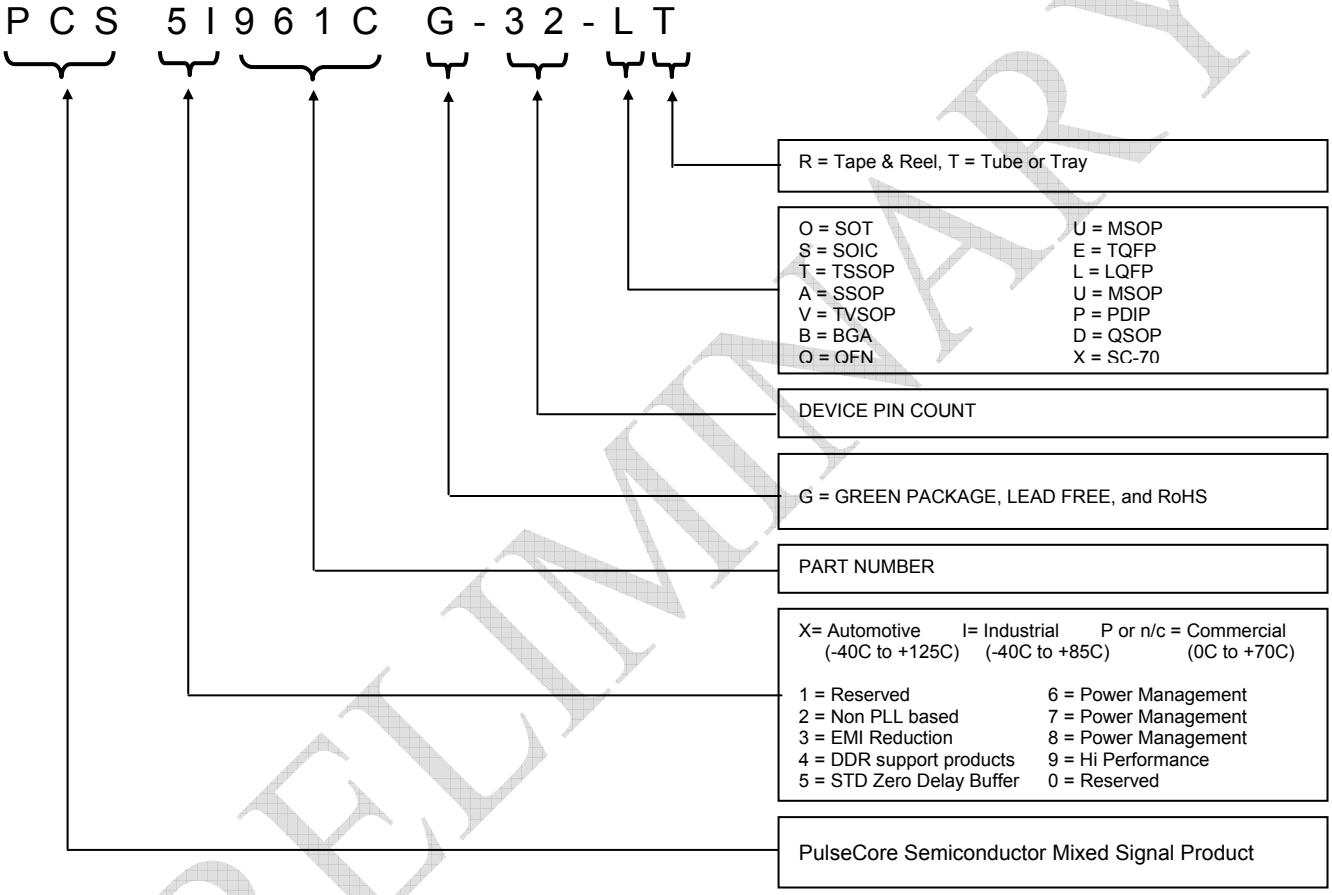
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.0630	…	1.6
A1	0.0020	0.0059	0.05	0.15
A2	0.0531	0.0571	1.35	1.45
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.20
e	0.031 BASE		0.8 BASE	
a	0°	7°	0°	7°

rev 0.3

Ordering Information

Part Number	Marking	Package Type	Temperature
PCS5I961CG-32-ET	PCS5I961CG	32 pin TQFP, Green	Industrial
PCS5I961CG-32-LT	PCS5I961CG	32 pin LQFP – Tape and Reel, Green	Industrial

Device Ordering Information



PulseCore Semiconductor Corporation
1715 S. Bascom Ave Suite 200
Campbell, CA 95008
Tel: 408-879-9077
Fax: 408-879-9018
www.pulsecoresemi.com

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003