M61558FP

Power driver IC for 30-W × 1-channel digital amplifiers

REJ03F0060-0100Z
Rev.1.0
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Description

The M61558FP is a power driver IC for digital power amplifiers. The IC incorporates both pre-drivers and the output-stage n-channel power MOS FET, for a single chip implementation of a 30-W single-channel digital amplifier for audio applications.

Features

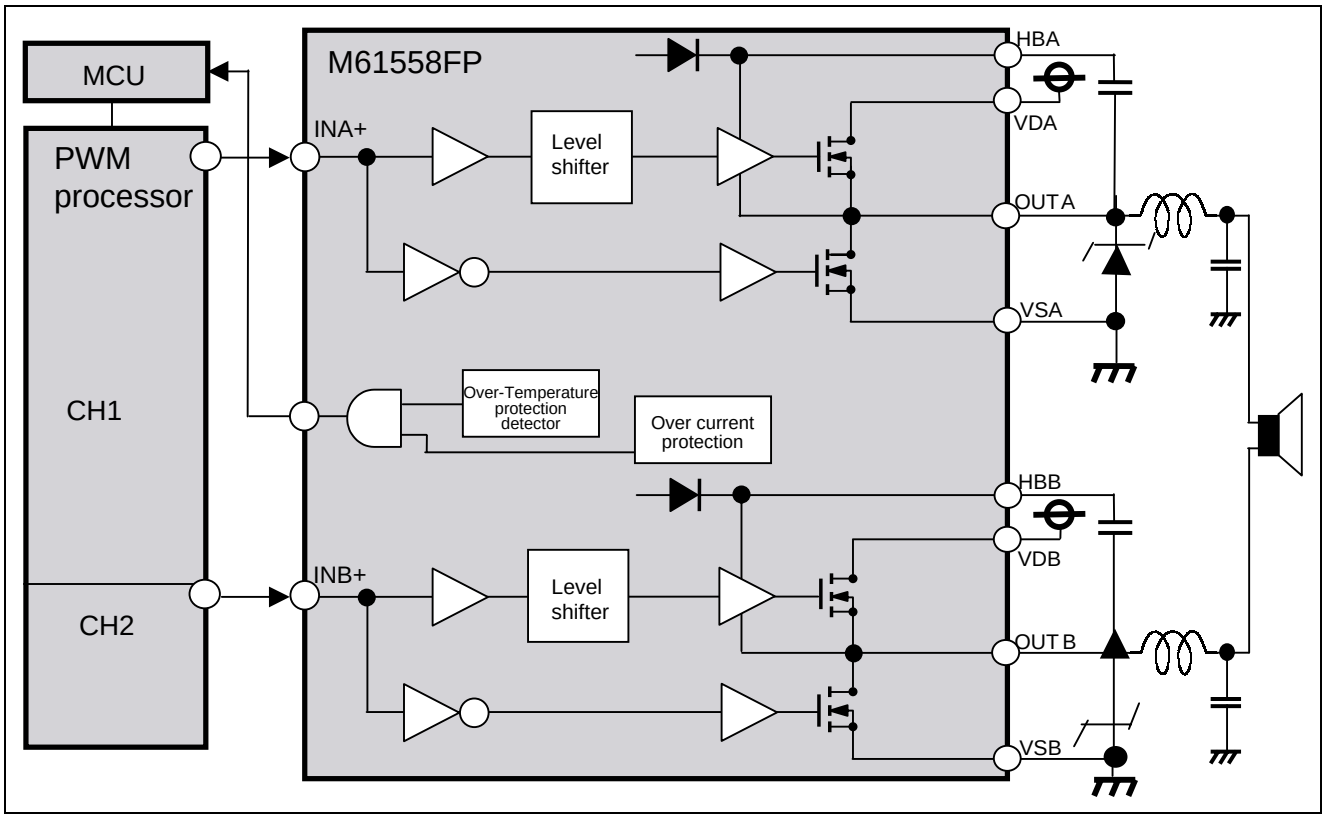
- On-chip n-channel power MOS FET
- Fast PWM switching operation
- On-chip diode for boot strap
- Various on-chip protective circuits
  - VDD under detection circuit
  - Over-Temperature protection circuit
  - Over-current protection circuit

Recommended Operating Conditions

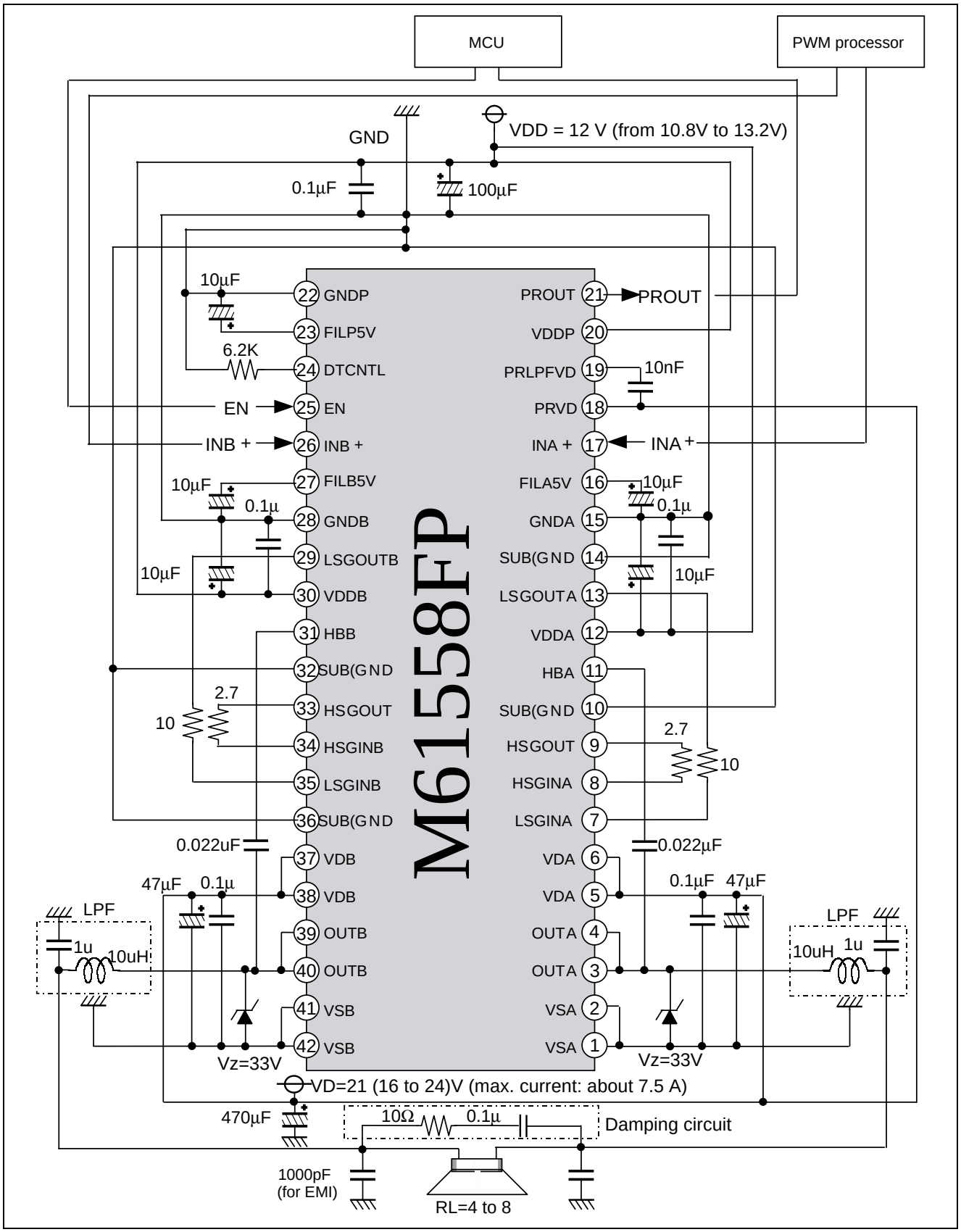
Power-supply voltage for pre-drive stage: VDD = 12 V (pre-driver stage power-supply voltage)

Output-stage power-supply voltage: VD = 21 V (typ.) < 16 V (min.) to 24 V (max.), RL = 4 (min.), 6 (typ.), 8 (max.) Ω

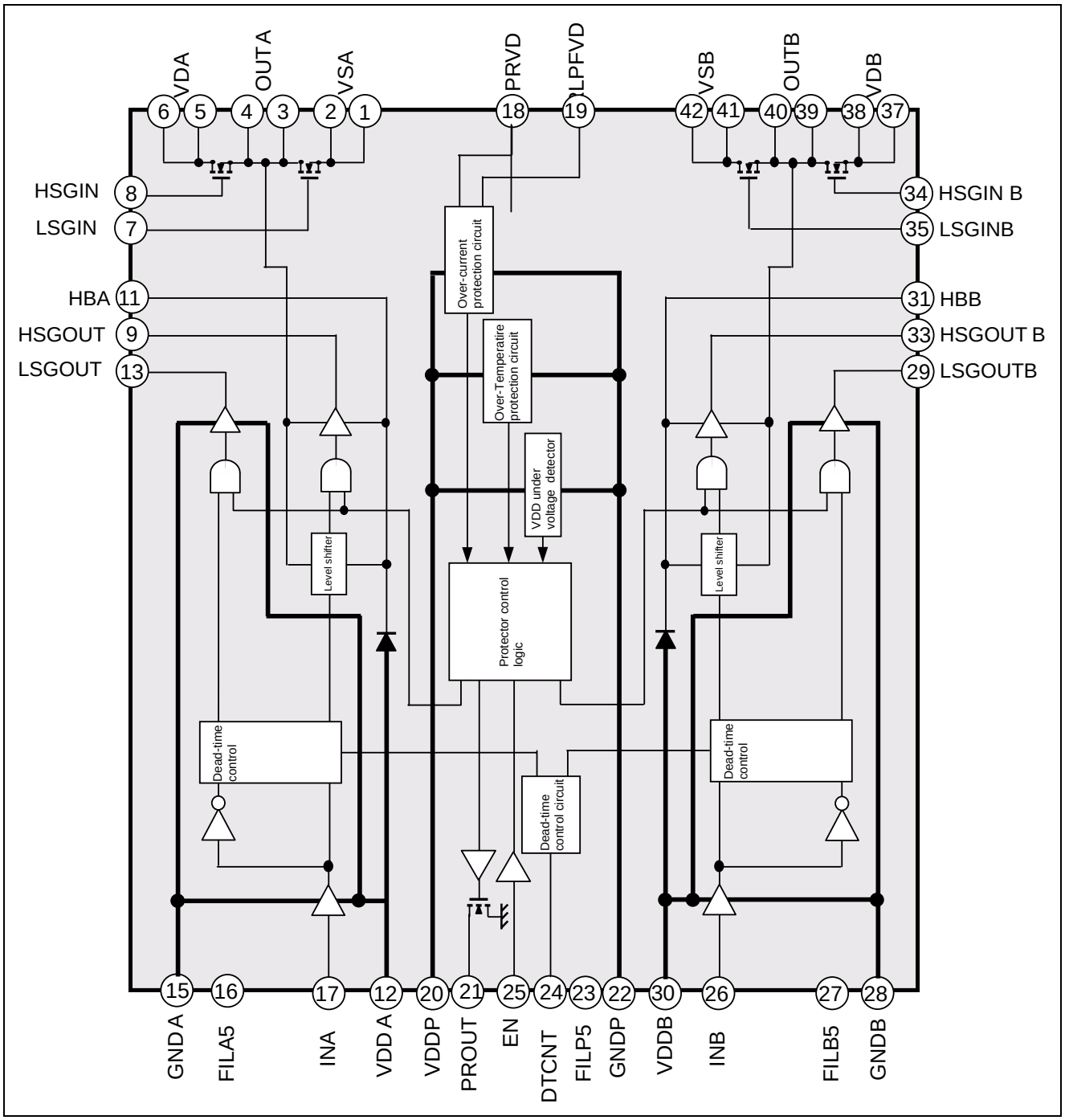
System block diagram



Sample application circuit and pin assignments



Block diagram



Pin Descriptions

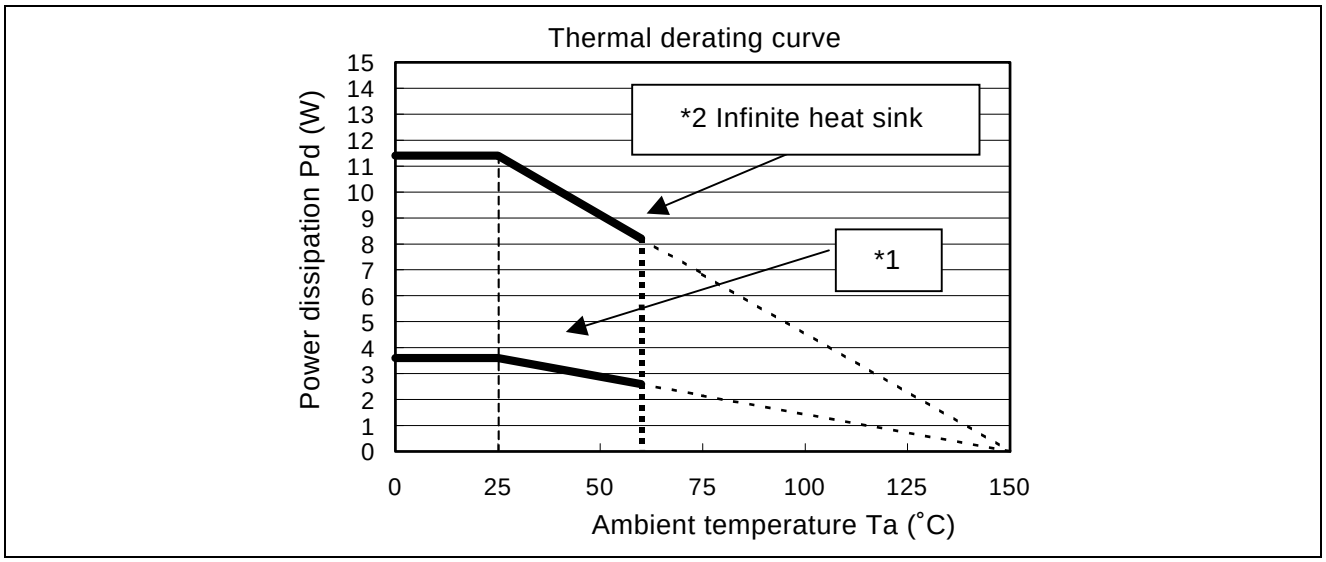
	Pin No.	Pin Name	Pin Description
A-side power module	1, 2	VSA	Ground pin for the A-side power-output stage
	3, 4	OUTA	A-side power-output pin
	5, 6	VDA	Power-supply pin for A-side power-output stage
	7	LSGINA	MOS FET input pin for A-side (L)
	8	HSGINA	MOS FET input pin for A side (H)
A-side pre-control module	9	HSGOUTA	A side (H) pre-buffer output
	10	NC	Connected to ground
	11	HBA	A pin for A side (H) boot strap.*
	12	VDDA	A-side pre-driver power-supply pin
	13	LSGOUTA	A-side (L) pre-buffer output
	14	NC	Connected to ground
	15	GNDA	A-side pre-driver ground pin
	16	FILA5V	Filter pin for A-side 5-V internal generation power-supply
	17	INA+	A-side PWM + input pin (CMOS input)
A, B common protec-tion module	18	PRVD	Power-supply pin for over current protection. Connected to VD power supply.
	19	PRLPFVD	Filter pin for over-current protection circuit
	20	VDDP	Power-supply pin for protection circuit block
	21	PROUT	Protection detector output pin. When protection condition is detected, low level (if pin is pulled up) is output (open drain output).
	22	GNDP	Ground pin for protection circuit block
	23	FILP5V	Filter pin for generation of 5-V internal power-supply for protection circuits
	24	DTCNTL	For connection to a resistor for dead-time control
	25	EN	Enable pin that release from the protection state
B-side pre-control module	26	INB+	B-side PWM + input pin (CMOS input)
	27	FILB5V	B-side 5-V internal generation power-supply filter pin
	28	GNDB	B-side pre-driver ground pin
	29	LSGOUTB	B-side (L) pre-buffer output
	30	VDDB	B pre-driver power-supply pin
	31	HBB	Apm for B-side (H) boot-strap capacitor circuit.
	32	NC	Connected to ground
	33	HSGOUTB	B–side (H) pre-buffer output
B-side power module	34	HSGINB	B side (H) MOS FET input pin
	35	LSGINB	B side (L) MOS FET input pin
	36	NC	Connected to ground
	37, 38	VDB	B-side power-output stage power-supply pin
	39, 40	OUTB	B-side power-output pin
	41, 42	VSB	B-side power-output stage ground pin

Note: * Adjacent power-module pins that have the same names must be connected with the shortest possible wiring lengths.

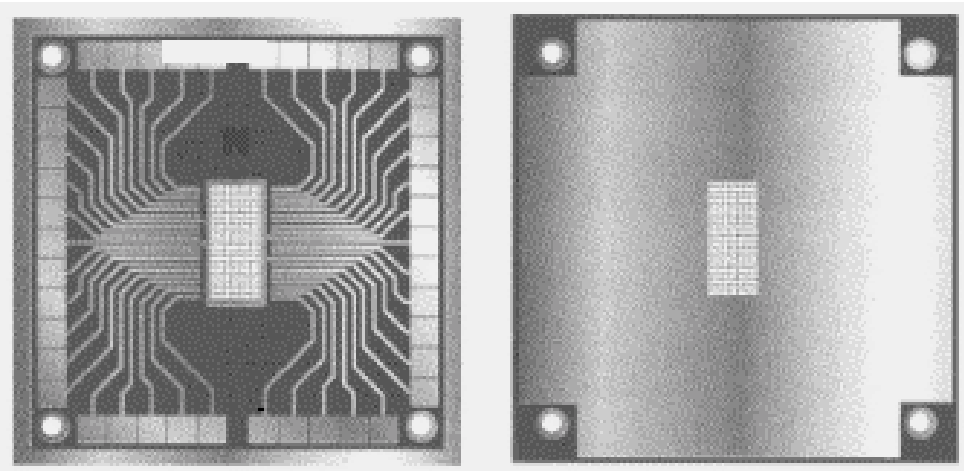
Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Conditions
HBA, HBB max. operating voltage	HBA, HBB	39	V	HBA, HBB pin voltage (operational setting)
VDA, VDB max. operating voltage	VDA, VDB	25	V	VDA, VDB pin voltage (operational setting)
Absolute max. voltage rating	VDD	15	V	VDD power-supply voltage
Voltage applied to input pins	Vin	–0.3 to 5.5	V	
Allowable dissipation	Pd	3.6	W	Ta = 25°C (when mounted on the board specified by Renesas; see note 1)
Thermal derating	Kθ	28.8	mW/°C	When mounted on the board specified by Renesas; see note 1)
Junction temperature	Tj	150	°C	
Operating temperature	Ta	–20 to +60	°C	
Storage temperature	Tstg	–40 to +125	°C	

Notes: 1. The specifications of the board specified by Renesas are given below for reference.
2. Maximum allowable power dissipation Pd = 11.4 W (ambient temperature Ta = 25°C) with an ideal heat sink.



Layer 1 (surface) Layer 2 (rear)



*1 Thermal derating characteristics measured for the board specified by Renesas

(Board specifications)
Material: Glass epoxy FR-4
Dimensions: 70 × 70 mm
Thickness: t = 1.6 mm

(Wiring specifications for layers 1 and 2)
Material: Copper
Thickness: t = 18 mm

Precautions on Usage

1. This product radiates heat even during normal operation, and reaches high temperatures. There is a possibility that characteristics failure or breakdown, including in peripheral components and circuits, may cause this product or peripherals to reach abnormally high temperatures. Also, please take special care when using this product as the final stage, since it may then be susceptible to damage because of external factors. This product is designed for consumer applications. Accordingly, please use it within the specified thermal conditions. Usage of the product in more relaxed thermal conditions may lead to malfunctions or damage to the product.
2. This product incorporates an over-current protection circuit which terminates the PWM operation when the peak instantaneous current from the VDA or the VDB power supply exceeds 7.5 A (designed value). Please note that it is never required to supply more current than this.
   The maximum-current value is roughly below 3 A during operation with a standard 4-Ω load.
   In usage, care is required with regard to the stability of the power-supply voltage.
3. Detection of an abnormality (when the PROUT pin (pin 21) becomes low) indicates a possibility of over current, so eliminate the cause, such as shorting of the output pins, and release the IC from the protection state (input low level on the EN pin (pin 25)).
4. This product includes MOS FET and CMOS logic circuits. Accordingly, electrostatic break down or latch-up may be generated within these elements. Please take the same care in using this product as in any case where MOS FET and CMOS logic LSIs are in use.

Recommended Operating Condition

Item	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
VD power-supply voltage	VD	16	21	24	V	VDA (pins 5, 6), VDB (pins 37, 38)
VDD power-supply voltage	VDD	10.8	12.0	13.2	V	VDDA (pin 12), VDDB (pin 30), VDDP (pin 20)
PWM frequency	fpwm		0.7	1.5	MHz	INA+ (pin 17), INB+ (pin 26)
Min. operating pulse width	Tpw MIN	40	—	—	ns	INA+ (pin 17), INB+ (pin 26)
High input voltage	VinH	4.0	—	5.0	V	INA+ (pin 17), INB+ (pin 26)
Low input voltage	VinL	0.0	—	0.8	V	INA+ (pin 17), INB+ (pin 26), EN (pin 25)

Notes:

1. PWM operation
   Do not input a signal shorter than the minimum pulse width, since this may lead to unstable operation or, in the worst case, damage to the product. Since boot-strap operation is performed, an input signal with aperiodical high and low levels may lead to abnormal operation. Ensure that the PWM signal has periodical high and low levels. The capacitance of the capacitor for boot-strapping in the sample application diagram is for the product in operation at 768 kHz. The thermal conditions, etc., become looser with operation at lower PWM frequencies.
2. Power-supply voltage
   The normal operating condition for this product is VDD voltage < VD voltage, so ensure that this is the state during normal operation. Setting a lower VDD voltage increases the margin against damage but carries the danger of the under voltage detection circuit malfunctioning, so please ensure that VDD is maintained at 9 V or more.
3. Mounting (board)
   The board layout must be capable of handling the same high frequencies and high levels of power as are handled by this IC. Furthermore, components must be selected in consideration of both audio-frequency and high-frequency characteristics. Please external note that large surges are generated by parasitic inductances during high-speed switching. This IC is designed specifically for bridge-tied load (BTL) operation, so the design focus was on symmetry of sides A and B. The pattern on the board must also be highly symmetrical for BTL configuration.

Electrical characteristics

(Unless otherwise noted, Ta = 25°C, VDDP, VDDA, B = 12 V, VDA, B = 21 V)

Item	Symbol	Limits			Unit	Condition of measurement
		Min.	Typ.	Max.		
Current drawn by the circuit						
VDD current circuit (suspended)	IDDQS	—	15	—	mA	PWM-suspended state
VDD current circuit	IDDQ	—	35	—	mA	No signal (f = 768 kHz, duty cycle = 50%)
VD current circuit		—	40	—	mA	No signal (f = 768 kHz, duty cycle = 50%)
Signal interfaces						
High input signal	VIH	2.3	—	—	V	Pins INA+, INB+, EN
Low input signal	VIL	—	—	1.0	V	Pins INA+, INB+, EN
High level input current	IIH	–10		10	µA	Pin EN
Low level input current	IIL	–260	–130	–65	µA	Pin EN
Low output voltage	VOL		—	0.4	V	Pin PROUT: IOL = 1 mA
High-output (leakage) current	IOH		—	10	µA	Pin PROUT: VOH = 5 V
Protection detectors						
VDD under voltage detection level	VDDR	5.0	7.0	9.0	V	Between VDD and GND, drop-detected to normal
Hysteresis in VDD-detection voltage	VDDH	—	0.5	—	V	Normal to under voltage
Over Temperature protection start temperature	Tsd+		150		°C	Normal to over-temperature protection state*
Over Temperature protection end temperature	Tsd–		130		°C	Over-temperature to normal state*
Diode characteristics for boot-strap						
Diode forward-direction voltage	VFL	—	0.75	—	V	HB output current = 100 µA
Diode forward-direction voltage	VFH	—	1.0	—	V	HB output current = 100 mA
Diode dynamic resistance	RDON	—	0.7	—	Ω	HB output current = 100 mA
Gate driver for low-side power transistor: “on” voltage						
Low level output voltage	VOL	—	0.5	—	V	ILO = 100 mA
High level output voltage	VOH	—	–0.75	—	V	IHO = –100 mA
		—		—		
Gate driver for high-side power transistor: “on” voltage						
Low level output voltage	VOL	—	0.5	—	V	ILO = 100 mA
High level output voltage	VOH	—	–0.75	—	V	IHO = –100 mA
		—		—		

*: Note that Tsd+, Tsd– are designed values for the IC’s internal temperature.

(Unless otherwise noted, Ta = 25°C, VDDP and VDDA/B = 12 V, VDA/B = 21 V)

Item	Symbol	Limits			Unit	Condition of measurement
		Min.	Typ.	Max.		
Output-stage DMOS transistor ON resistance						
Breakdown voltage between drain and source	BVds	35	—	—	V	Ileak=1mA
ON resistance between drain and source	rDS(ON)	—	0.20	—	Ω	ID=100mA
Input/output timing						
Reference input operating frequency	1/tpf	—	768	—	KHz	Boot-strap C = 0.022 uF
Min. input pulse width	tpw	40	—	—	ns	Period = 1.3 us (f = 768 kHz)
Dead-time setting						
Pin 24 output voltage	VDTC	—	1.35	—	V	Connected resistance: 6.2 kΩ

(Data for reference) AC characteristics

Note: The reference values when the evaluation board specified by Renesas is used.

(Unless otherwise specified, Ta = 25°C, VDDP and VDDA/B = 12 V, VDA/B = 21 V)

Item	Symbol	Rated value			Unit	Reference board setting condition	Measurement condition
		Min.	Typ.	Max.			
Output power 1	Po1	—	30	—	W	Sine, 1 kHz/0 dB, modulation depth = 90%	THD+N=1%,RL=6Ω, VDA/B=24V LPF=20KHz, HPF=400Hz
Output power 2	Po2	—	30	—	W	Sine, 1 kHz/0 dB, modulation depth = 90%	THD+N=1%,RL=4Ω, VDA/B=21V LPF=20KHz, HPF=400Hz
Total harmonic distortion	THD+N	—	0.04	—	%	Sine, 1 kHz/0 dB, modulation depth = 50%	RL=4Ω, LPF=20KHz, HPF=400Hz
Noise voltage	Vno	—	150	—	μVrms	The MUTE signal is inputed	A-Weighted filter/ LPF=20KHz
Power efficiency	Eff	—	85	—	%	Sine, 1 kHz/0 dB, modulation depth = 90%	Po=30W, RL=4Ω

Note: In the heat-radiation state of attachment to the board specified by Renesas, the M61558FP can continuously output 10 W (refer to the thermal derating curve on page 5). When more than 10 W is continuously output, heat-radiation design measures such as heat sinks are required.

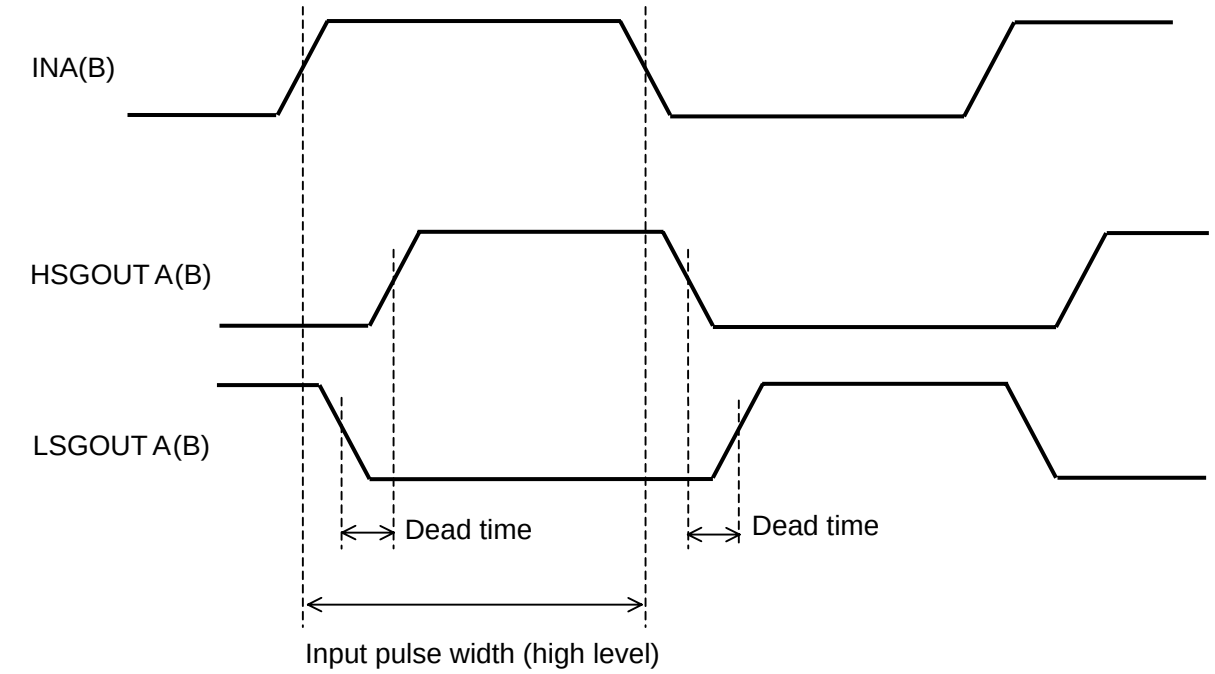
Description of additional functions

Dead-time control

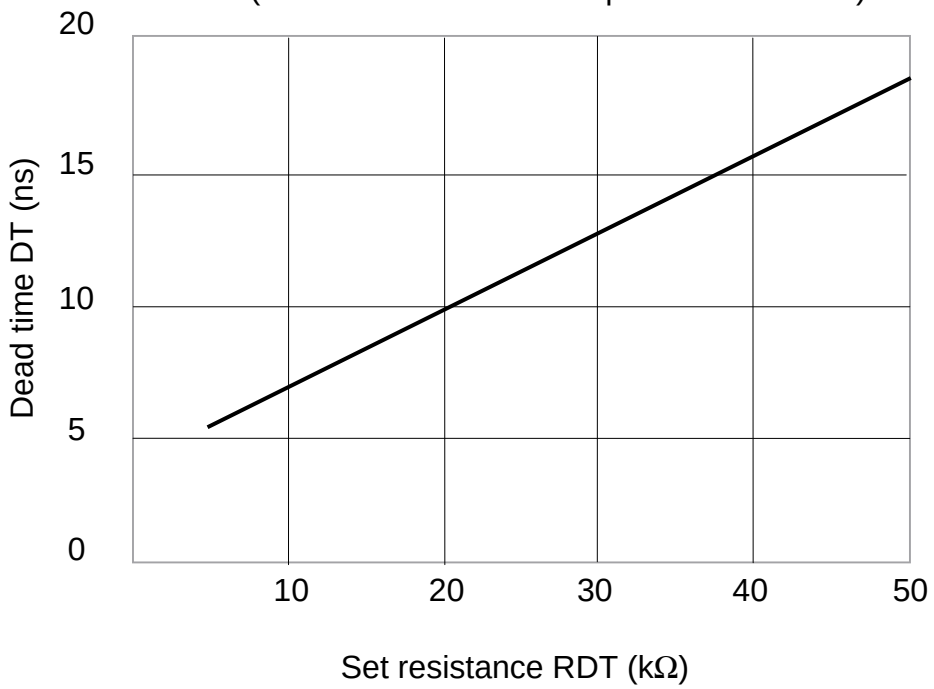
The dead-time value given below sets a period between LSGOUTA(B) and HSGOUTA(B) at the gate-driver outputs. This prevents through-current-induced damage to the output-stage power transistor. The dead-time setting is adjusted by the value of the external resistor on DTCNTL (pin 24).

Note : The given values are design values, and the actual dead time is affected by the operating conditions (gate-resistor value, switching characteristics, etc.) of the power transistor.

Timing of input and output operations



Dead time and resistance setting
(reference values for the pre-driver module)



Internal protective circuits

1. VDD under voltage detection circuit
   When the VDD power-supply voltage falls by a certain amount, the VDD under voltage protective circuit operates to prevent malfunctions of the IC. When an abnormality is detected, the output transistor on the H side is switched off, the output transistor on the L side is switched on, and a low level is output from the output pin. For the sake of automatic resumption, a low level is not output from PROUT (pin 21). Of the protection states, this is only the case for abnormal voltage-drop detection. The VDD detection circuit is connected to the common VDD power-supply pin, VDDP (pin 20). Please set up IC-external wiring to connect the VDDA/B (pins 12, 30) to VDDP.
2. Over Temperature protection circuit
   The IC incorporates an over temperature protection circuit (thermal shutdown circuit) that protects the IC from thermal damage when the temperature of the IC (chip) rises because of an abnormality. The protection circuit is activated before the IC's internal junctions, etc., reach the thermal-damage temperature, and remains so until the temperature falls to the hysteresis condition, regardless of the state of the EN pin (pin 25). In the excessive-temperature condition, all output transistors are turned off, the output pins are released (open), and a low level is output from PROUT to issue a notification about the abnormal state.
3. Over current protection circuit
   This IC incorporates an excessive current protection circuit which terminates the PWM operation when the peak instantaneous value of current supplied from the VDA or VDB power supply exceeds 7.5 A (designed value). In the protection mode, all output transistors are switched off, all output pins are released (open), and a low level is output from PROUT to notify the system of the abnormal state.
   Note: The abnormality is detected on the positive side of the power-stage power supply. The conditions for detecting a load short between output pin and VDD. VDD are not more strict short between both output pins or between output pin and ground. Note that when shorting between VDD occurs, detection is not possible until the abnormality affects the positive side of the power supply, so the protective operation may not be performed.

Functions when an abnormality is detected

When an abnormality is detected, the IC operates asynchronously with respect to the PWM inputs (INA+, INB+), controls the output-stage n-channel transistor (H or L side) and enters the protection state. The states of the PROUT and OUT outputs and the states of each output-stage transistor are given in the table below. After the low level has been placed on PROUT, the protection state is maintained until the EN signal is low.

State of output stage during protection operation

Protection	PROUT output in case of abnormality	OUTA output pin	OUTB output pin	OUTA output-stage transistor		OUTB output-stage transistor	
				H side	L side	H side	L side
VDD voltage-drop protection	No change (high)	Low	Low	Off	On	Off	On
Over Temperature, over-current protection	Output low, held until low level is placed on EN	Open	Open	Off	Off	Off	Off

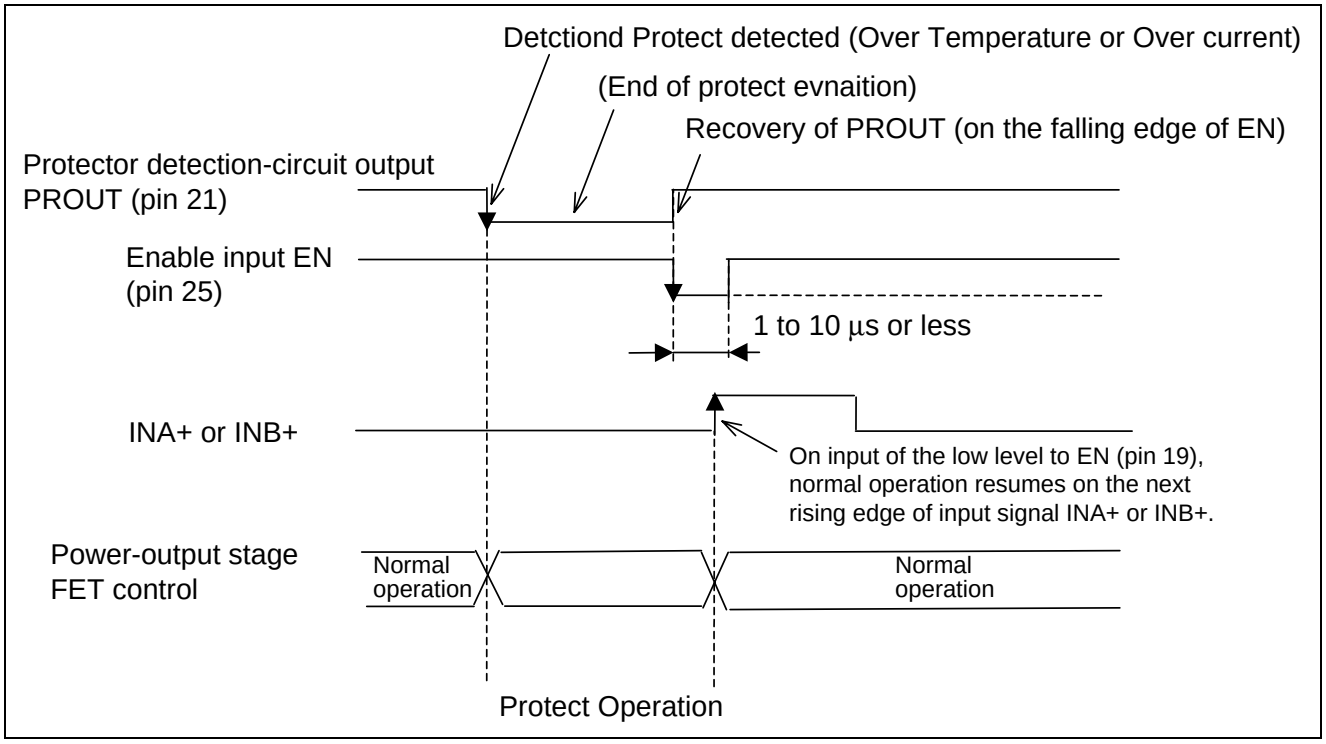
Resuming from abnormality detection

Resumption to signal output from the individual abnormal state varies with the corresponding protective circuit. After the conditions for resumption have been satisfied, resumption occurs on the rising edge of either INA+ or INB+, whichever is earlier. The conditions for resumption from each abnormal state are given in the table below.

Conditions required for resumption from abnormal states

Abnormal state	Condition for resumption
VDD under voltage	After the voltage has returned to the normal level and this has been confirmed by the internal VDD detection circuit, the IC resumes normal operation on the next rising edge of either INA+ or INB+.
Over Temperature, over current	After the state has returned to normal, the condition for resumption is the falling edge of EN. The IC then returns to normal operation on the next rising edge of either INA+ or INB+.

Timing chart for protector detection-output PROUT (pin 21) and enable input EN (pin 25)



LPF circuit

The output LPF circuit must have characteristics in accord with the signal-frequency band and characteristic impedance value of the speaker that constitutes the load. The simplest example is a second-order Butterworth filter in an LC configuration.

Damping circuit

When the speaker is removed, the frequency characteristics of the low-pass filter may lead to problems of high-band characteristics such as peaking. Accordingly, a high-band damping circuit should be installed in parallel with the speaker. (Take the allowable power, etc., of the damping resistor into consideration.)

Zener diode for surge protection

Ringing, etc., occurs during the high-speed switching operation of this IC. During short-circuit, connection to ground or VDD of load, very large surge voltages are generated. When the surge voltage exceeds the voltage tolerance of the transistors (step-down voltage between source and drain, etc.), the IC may be damaged. We recommend that you prevent damage to this IC by connecting a Zener diode for surge protection to the output pins (select a Zener voltage slightly below 35 V).

Precautions on wiring for the protective circuits

PRVD (pin 18) is wired to the protective detection circuits.

Use as short a wiring run as is possible to connect this pin to a point on the VD power-supply line near the VD pin. This point should not be readily affected by variation in voltages due to power supply and the operating conditions.

Please take care because this may affect the characteristics of the protective circuits or damage the IC.

Measures against EMI

Please note the need to reduce the levels of unwanted radiation components produced by high-speed switching operation. For example, apply countermeasures such as raising the order of the output LPF circuit, or attaching a capacitor with a value of about 1000 pF to the speaker pin.

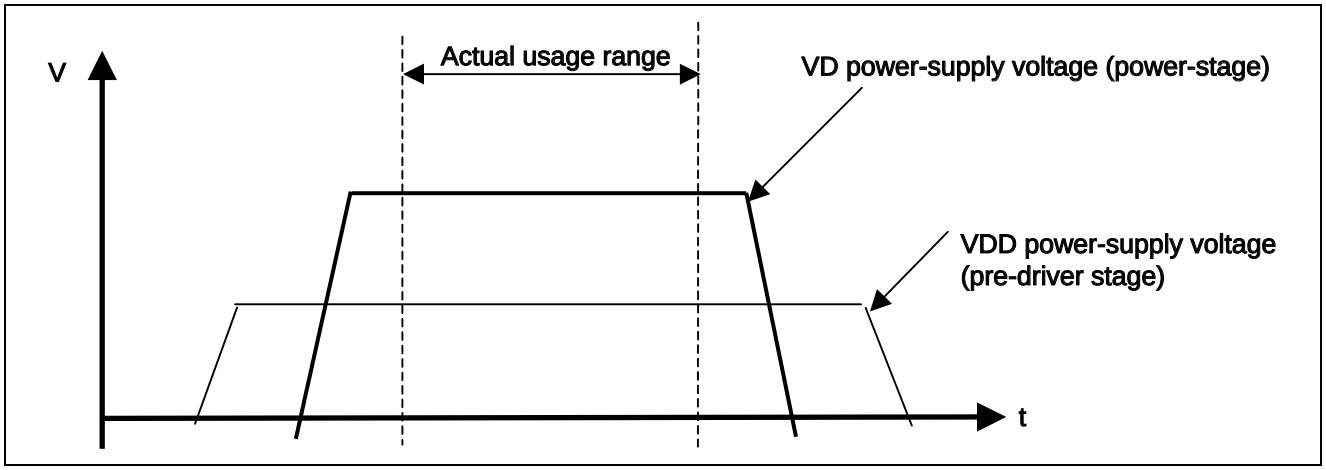
Single-ended operation

This IC is for bridge-tied load (BTL) operation, but single-ended operation for an independent half-bridge configuration is possible. In this case, note that performance changes (e.g. 30 W x 1 ch. becomes 7.5 W x 2 ch). Also, other parts of the IC are designed on the specific assumption of BTL operation, so sufficient evaluation and examination is required.

Pop noise when turning the power supply on and off

One simple countermeasure against pop noise is to ensure that VD (power-stage power-supply voltage) is only turned on and off while VDD (power-supply voltage of the pre-driver stage) is applied. If this measure is ignored, pop noise may occur when the power supply is turned on or off.

We also recommend operation under the condition VDD < VD. Consider turning the power supply on and off in the following sequence.



Heat sink

Unlike the molded resin surface, the metal side of the package for heat radiation is slightly concave.Take this structure into consideration when designing a heat sink for use with high output levels.

Capacitor for boot-strapping

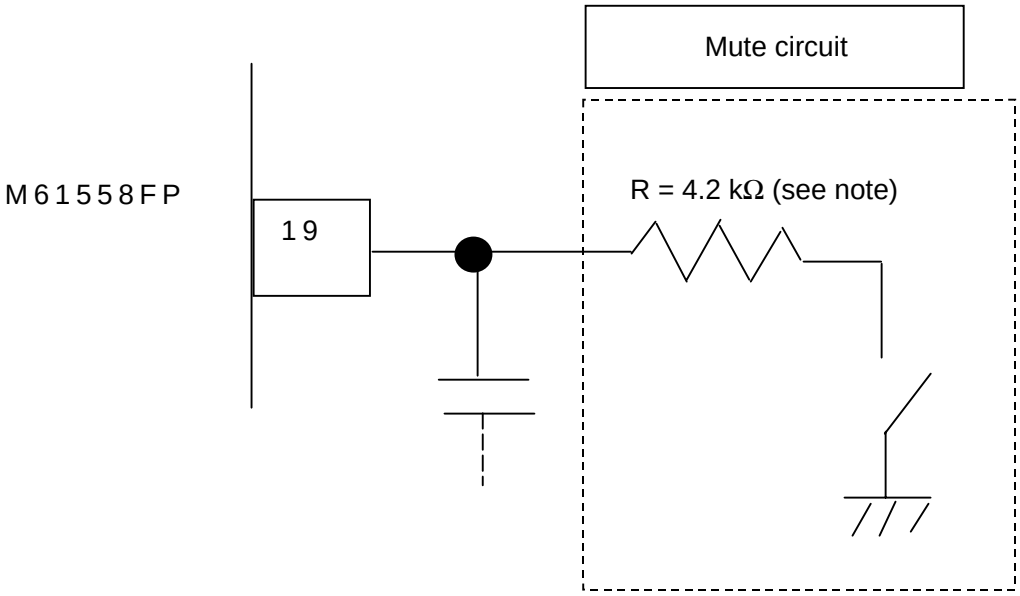
This IC is designed for PWM operation at around 768 kHz (high-speed PWM operation in the hundreds of kHz order). Accordingly, the value of the capacitor for boot-strapping in the diagram of the example application circuit is for such operation. If a large change is to be made to the PWM frequency, a correspondingly change in the value of this capacitor is required. Note that such usage was not presupposed in the design of this IC.

Muting operation by force

The output is forcibly muted by using a resistor to pull the PRLPFVD pin (pin 19) down to ground (signal output is terminated and the output terminals enter the Hi-Z open state; refer to the figure below). To cancel muting, release pin 19 from the pulled-down state, and then input a cancellation pulse on the EN pin (pin 25) in the same way as is used to cancel the protection state.

Please note the following points:

- Muted operation is only possible during normal operation; that is, it is not possible in transient states, such as while turning the power supply on or off.
- For actual usage, please thoroughly evaluate and examine the forcible mute operation.



Note: The above setting assures operation by ensuring the flow of a strong current. Decreasing the resistance below this level has no effect.

Package Dimensions

42P9R-E

Note : Please contact Renesas Technology Corporation for further details.

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