TEA1781T; TEA1782T

GreenChip PC secondary control ICs

Rev. 01 — 13 February 2009 Preliminary data sheet

1. General description

The TEA1781T and TEA1782T are designed to cooperate with the TEA1771T primary side controller in a unique converter topology based on the active clamp forward converter. On the secondary side the output voltages are regulated via bidirectional switches. A typical application area of this converter is a power supply for a desktop PC.

The TEA1781T and TEA1782T are secondary control ICs and regulate each output voltage independently of the primary duty cycle and other secondary output voltages. Because of these separated regulations, the system does not show any cross regulation and makes the design of the transformer easier.

As each output can also be completely turned off, the system allows for an integrated standby supply. To maximize the efficiency in Standby mode, the duty cycle and operating frequency are minimized in Standby mode.

The TEA1781T and TEA1782T have integrated drivers and individual output voltage regulators. In this way the 3.3 V, 5 V, 12 V and 5 V standby outputs of a typical PC power supply are regulated separately giving accurate output voltages and fast transient response.

All requirements according to the Intel ATX specification (V 2.0) are integrated, such as soft start, a PS_ON# connection, a PwrOK signal and all required protections like OverCurrent Protection (OCP) and OverVoltage Protection (OVP). These voltage and current levels are monitored at each output separately. The system also has an OverTemperature Protection (OTP) function.

The system fulfills the current and proposed efficiency standards such as 80+ gold, energy star and blue angel.

The TEA1781T and TEA1782T are implemented in a high voltage (ABCD) Silicon On Insulator (SOI) process.

2. Features

- Designed for ATX PC power supplies
- Integrated standby supply
- Enhanced efficiency in Standby mode
- No cross regulation
- Accurate output voltage regulation
- Fast transient response
- Integrated soft start for all output voltages
- Flexible transformer design without the need of a post regulator

- Overvoltage protection
- Overcurrent protection
- Overtemperature protection
- System failure detection
- Soft (re)start
- Low external component count

3. Applications

- PC desktop power supply

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1781T	SO28	Plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TEA1782T	SO28	Plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

5. Block diagram

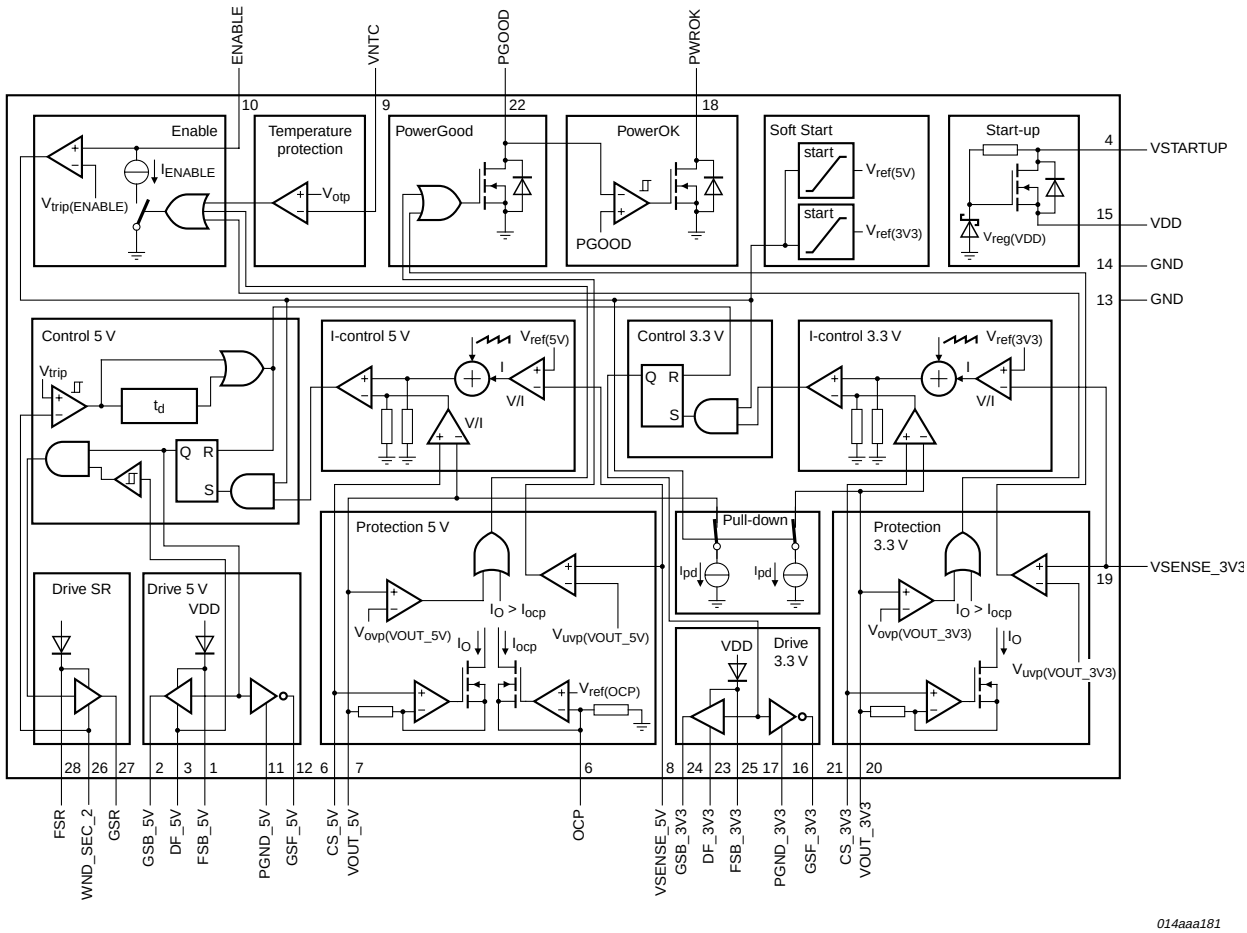


Fig 1. TEA1781T block diagram

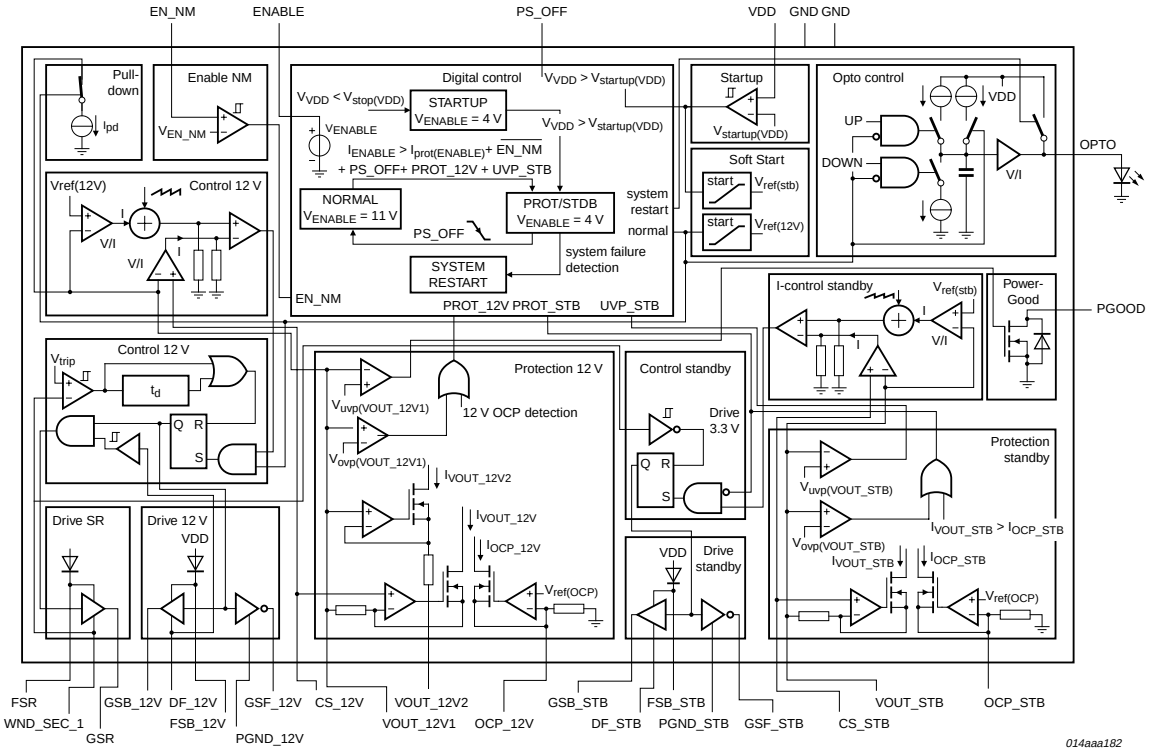


Fig 2. TEA1782T block diagram

6. Pinning information

6.1 Pinning

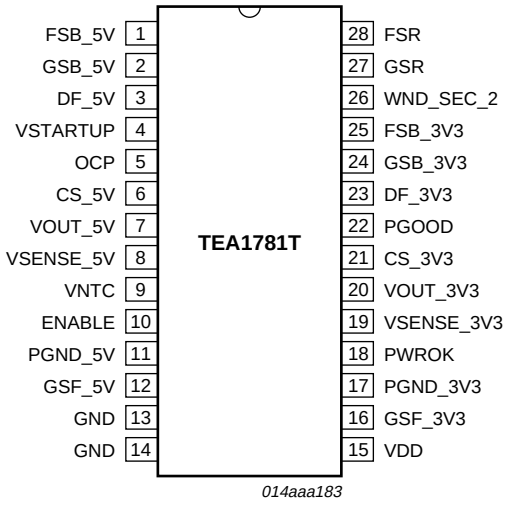


Fig 3. TEA1781T pin configuration

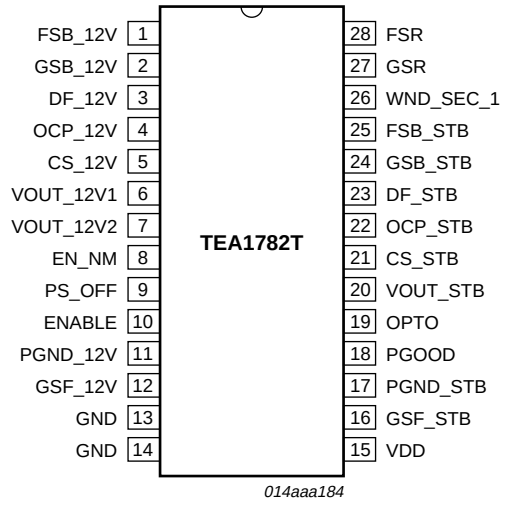


Fig 4. TEA1782T pin configuration

6.2 Pin description

Table 2. TEA1781T pin description

Symbol	Pin	Description
FSB_5V	1	floating supply switch SB_5V
GSB_5V	2	gate driver switch SB_5V
DF_5V	3	drain voltage of switch SF_5V
VSTARTUP	4	start-up voltage connected to rectified secondary winding voltage
OCP	5	overcurrent protection
CS_5V	6	current sense 5 V output
VOUT_5V	7	output voltage 5 V output
VSENSE_5V	8	sense voltage 5 V output
VNTC	9	NTC voltage
ENABLE	10	enabling Normal mode
PGND_5V	11	power ground 5 V output
GSF_5V	12	gate driver switch SF_5V
GND	13	ground
GND	14	ground
VDD	15	supply voltage
GSF_3V3	16	gate driver switch SF_3V3
PGND_3V3	17	power ground 3V3 output
PWROK	18	power OK
VSENSE_3V3	19	sense voltage 3.3 V output
VOUT_3V3	20	output voltage 3.3 V output
CS_3V3	21	current sense 5 V output
PGOOD	22	PowerGood (delay setting for power OK)
DF_3V3	23	drain voltage of switch SF_3V3
GSB_3V3	24	gate driver switch SB_3V3
FSB_3V3	25	gate driver switch SB_3V3
WND_SEC_2	26	secondary transformer 3.3 V / 5 V winding voltage
GSR	27	gate driver switch SR (3.3 V / 5 V)
FSR	28	floating supply switch SR (3.3 V / 5 V)

Table 3. TEA1782T Pin description

Symbol	Pin	Description
FSB_12V	1	floating supply switch SB_12V
GSB_12V	2	gate driver switch SB_12V
DF_12V	3	drain voltage of switch SF_12V
OCP_12V	4	overcurrent protection 12 V output
CS_12V	5	current sense 12 V output
VOUT_12V1	6	output voltage 12 V1 output
VOUT_12V2	7	output voltage 12 V2 output
EN_NM	8	enable Normal mode

Table 3. TEA1782T Pin description *…continued*

Symbol	Pin	Description
PS_OFF	9	power supply off (via delay network connected to PS_ON#)
ENABLE	10	enabling Normal mode
PGND_12V	11	power ground 12 V output
GSF_12V	12	gate driver switch SF_12V
GND	13	ground
GND	14	ground
VDD	15	supply voltage
GSF_STB	16	gate driver switch SF_stb
PGND_STB	17	power ground standby output
PGOOD	18	PowerGood (delay setting for power OK)
OPTO	19	opto coupler
VOUT_STB	20	output voltage standby output
CS_STB	21	current sense standby output
OCP_STB	22	overcurrent protection standby output
DF_STB	23	drain voltage of switch SF_stb
GSB_STB	24	gate driver switch SB_stb
FSB_STB	25	gate driver switch SB_stb
WND_SEC_1	26	secondary transformer 12 V / standby winding voltage
GSR	27	gate driver switch SR (12 V)
FSR	28	floating supply switch SR (12 V)

7. Functional description

7.1 Introduction

A PC power supply has to supply a number of different supply voltages: 12 V, 5 V, 3.3 V, −12 V and 5 V standby. To achieve the required output voltage accuracy, the systems of today require dissipative post regulations.

Because the system must be able to switch off the main supplies (12 V, 5 V, 3.3 V, −12 V) in Standby mode but keep the 5 V standby in operation, a separate standby supply is still common practice.

With the GreenChip PC chip set (TEA1771T, TEA1781T, TEA1782T) a system configuration is introduced that integrates the post regulation and combines the main and standby converter into a single system. This high level of integration reduces the total cost of the system.

Because the output voltages are regulated separately, it makes the design of the converter easier as none of the output voltages is directly related to the number of turns on the transformer.

One of the main differences of this topology compared to commonly used solutions is the use of switches instead of Schottky diodes, although the rectifying switch is a so-called bidirectional switch. This switch is built up by two standard FETs in anti-series.

The freewheel switch behaves like an ideal diode so the setup runs in a discontinuous mode at low loads. Negative currents are avoided by the control ICs through this switch.

Replacement of the rectifying Schottky diode by two switches in anti-series allows:

- Integration of the 5 V standby supply, because in Standby mode the main secondary outputs can be switched off.

The supply voltages can be individually and more accurately regulated, eliminating ubiquitous post regulators.

- As the output voltages is now regulated by the secondary switches, the duty cycle of the primary control switch can be kept constant, preventing ringing at the primary reset voltage. A lower reset voltage results in lower required breakdown voltages of all applied FETs, both primary and secondary. This reduces costs.
- The use of Zero Voltage Switching (ZVS) at the primary side to fulfill the required standby efficiency.

To fulfill the ATX12V specification on standby efficiency requirements, the system has a Standby mode in which the frequency, duty cycle and supply currents are reduced.

The TEA1781T and TEA1782T are secondary control ICs. Together with the TEA1771T primary controller they form a unique system that fulfills the 80+ gold requirements at minimum costs, eliminating any cross regulation and maximizing standby efficiency.

7.2 Supply

When the voltage on the primary side from the rectified input mains reaches its starting value, the primary side starts up and switches the primary main switch. From that moment, the secondary rectified transformer voltage at $V_{startup}$, see Figure 5, is a ratio of the input voltage.

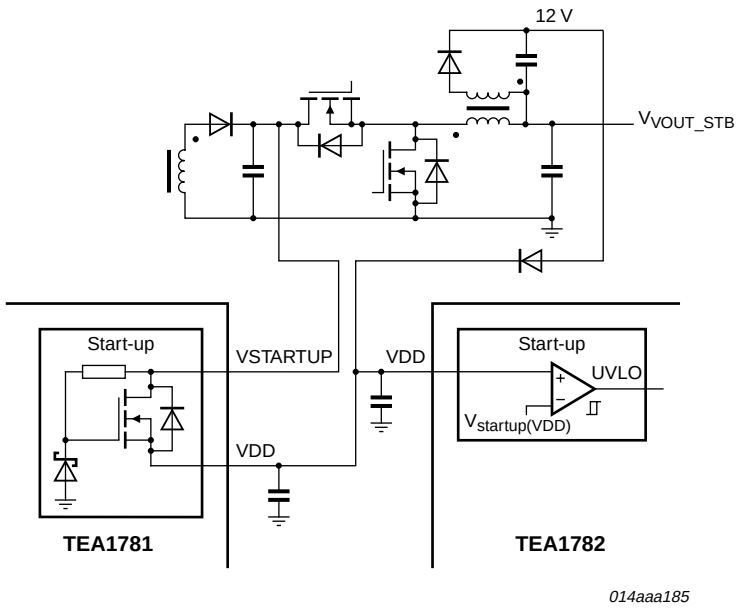


Fig 5. Start-up sequence TEA1771T

The VDD capacitor is charged and regulated to the $V_{reg(VDD)}$ level via a linear regulator in the TEA1781T. This VDD voltage is the supply voltage for both secondary ICs.

Once the VDD voltage reaches the $V_{startup(VDD)}$ level, measured in the TEA1782T, the 5 V standby is started up via a so-called soft start. This implies that during a certain time, $t_{start(soft)}$, the output voltage slowly ramps up from zero to the required value. Once the system is started up, the VDD voltage is taken over by an auxiliary winding of the 5 V standby output, as shown in Figure 5. This ensures an efficient 12 V VDD voltage during standby and normal operation.

As the secondary ICs are supplied via the TEA1781T and measured in the TEA1782T, both ICs are disabled in case of an open connection in the supply chain.

If the VDD voltage drops below its $V_{stop(VDD)}$ level, the system disables all output voltages by actively turning off all switches. This avoids undefined conditions resulting from charged gate capacitances.

7.3 Mode of operation

After the system has started up, the TEA1782T defines the mode of operation. It features four operation modes: Start-up mode, Protection/Standby mode, Normal mode and System restart mode, as depicted in Figure 6.

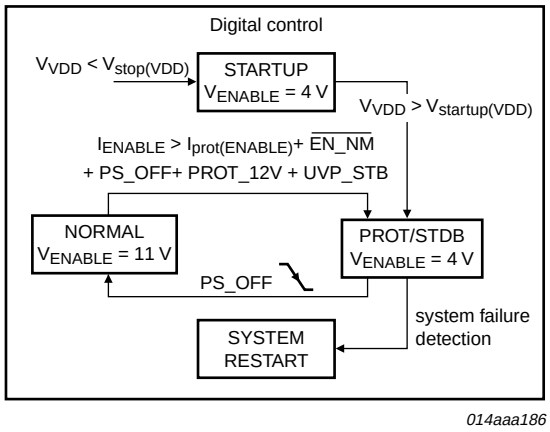


Fig 6. State diagram TEA1771T

When the VDD voltage is below its stop level, the TEA1782T enters the Start-up mode and the TEA1781T charges the VDD capacitors to $V_{reg(VDD)}$ via the start-up pin. When it has charged the VDD capacitor above $V_{startup(VDD)}$, the TEA1782T jumps into Protection/Standby mode and the 5 V standby output slowly rises from zero to its required value.

When the PS_OFF signal becomes active low, the system switches to Normal mode enabling the main outputs (3.3 V, 5 V, 12 V and −12 V). The 12 V (and −12 V) output is regulated by the TEA1782T itself, whereas the 3.3 V and 5 V output are regulated by the TEA1781T. The TEA1781T activates the 3.3 V and 5 V outputs via the ENABLE signal.

At any failure condition or as soon as the PS_OFF signal is high, the system switches to Protection / Standby mode. When a failure, such as a shorted or overloaded output, is detected, the system enters the Protection mode, disabling the main output circuits but leaving the standby output in operation. However, when, for example, a secondary FET is shorted, the system enters the System restart mode and switches off the primary side.

When VDD is discharged below its minimum level, $V_{stop(VDD)}$, the IC enters the Start-up mode and all switches are disabled.

When the system is in Protection / Standby mode, the systems lowers its duty cycle and operating frequency to optimize the system's efficiency.

7.4 Enable Normal mode

In Standby mode, an optional PFC may be switched off. When switched to Normal mode, the system has a programmable delay before the main outputs (3.3 V, 5 V and 12 V) are switched on. During this delay the PFC can be activated.

An extra safety feature has been built in when enabling Normal mode. If the input voltage is too low, which can occur when the PFC fails, the system stays in Standby mode.

The input voltage is measured on a rectified secondary voltage, reflecting the input voltage; see Figure 7.

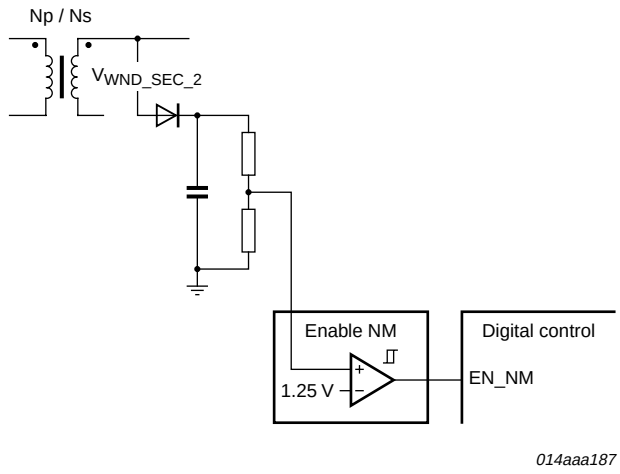


Fig 7. Enable Normal mode assures a proper start-up of the forward converter

In addition to a minimum input voltage, a delay can also be made to assure a proper start-up of the PFC before the system switches to Normal mode. A circuit according to Figure 8 must be built between the PS_ON# signal from the motherboard and the PS_OFF pin of the TEA1782T.

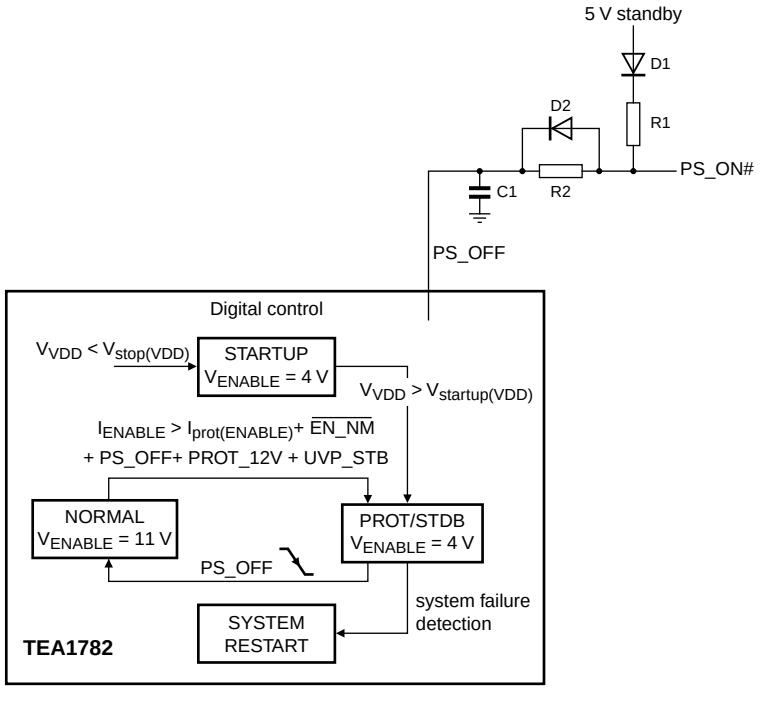


Fig 8. Enable Normal mode assures a proper start-up of the PFC

7.5 Soft start

When the TEA1782T enters the Protection/Standby mode after start-up, the 5 V standby output is started up via a soft start. The main output voltages, 3.3 V, 5 V, 12 V and −12 V are started up via a soft start when the TEA1782T enters the Normal mode. A soft start implies that the outputs will rise gradually and simultaneously from zero to their required value during a defined period (≈ 15 ms).

When PS_OFF is turned low, the main outputs of the TEA178x chip set ensure that power sequencing is applied according to the ATX12V specification of Intel, i.e., the 12 V and 5 V outputs must be equal to, or greater than, the 3.3 V output during power-up and normal operation.

7.6 Enable

The TEA1782T is the master of the system. The required duty cycle is communicated to the primary controller TEA1771T via the opto coupler. The TEA1782T communicates to the TEA1781T via the enable signal, see Figure 9, if the main outputs are enabled or disabled. If the system is in Normal mode, the voltage of the enable signal exceeds the trip level, $V_{trip(ENABLE)}$, enabling all outputs. Otherwise the main outputs are disabled.

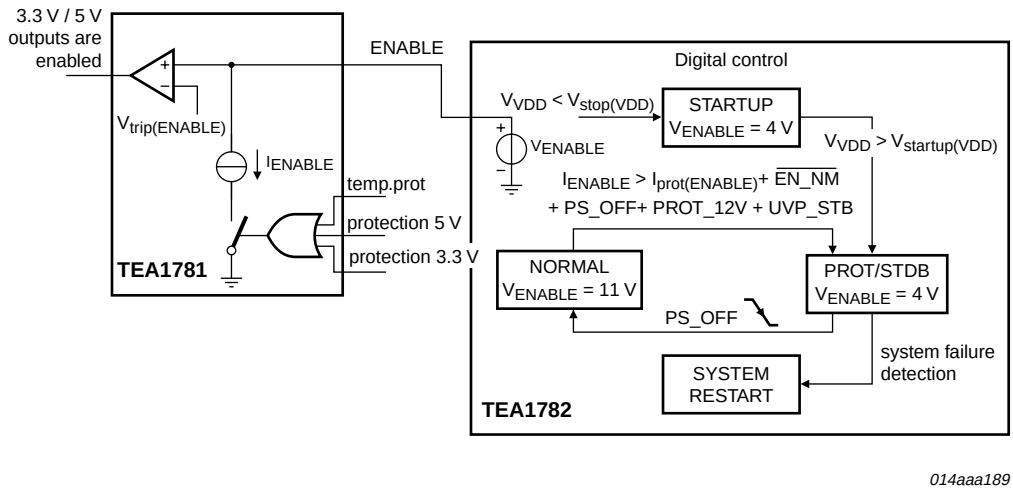
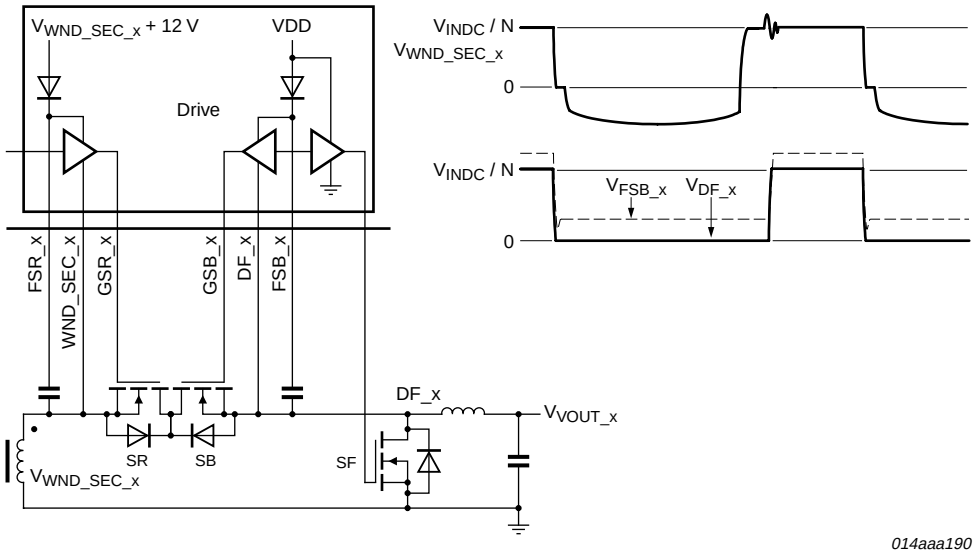


Fig 9. The ENABLE signal is for communicating between the secondary control ICs

7.7 Output drivers

Figure 10 shows a part of the secondary side output circuitry and the applied gate drive system.



(1) WND_SEC_x: The “x” stands for either 1 or 2

(2) FSR_x,, GSR_x, GSB_x, DF_x, FSB_x:
The “x” for these pins and symbols stands for either 3V3, 5V or 12V

(3) VOUT_x: The “x” stands for either 3V3, 5V, 12V1 or 12V2.

Fig 10. Output driver circuit

The freewheel switch SF is turned on and off between the VDD voltage (12 V) and ground level as the source of SF is connected to ground. The source of switch SB varies between zero (actually a small negative voltage when the SF or its back gate diode is conducting) and the maximum secondary transformer voltage. Therefore the driver of SB requires a bootstrap circuit.

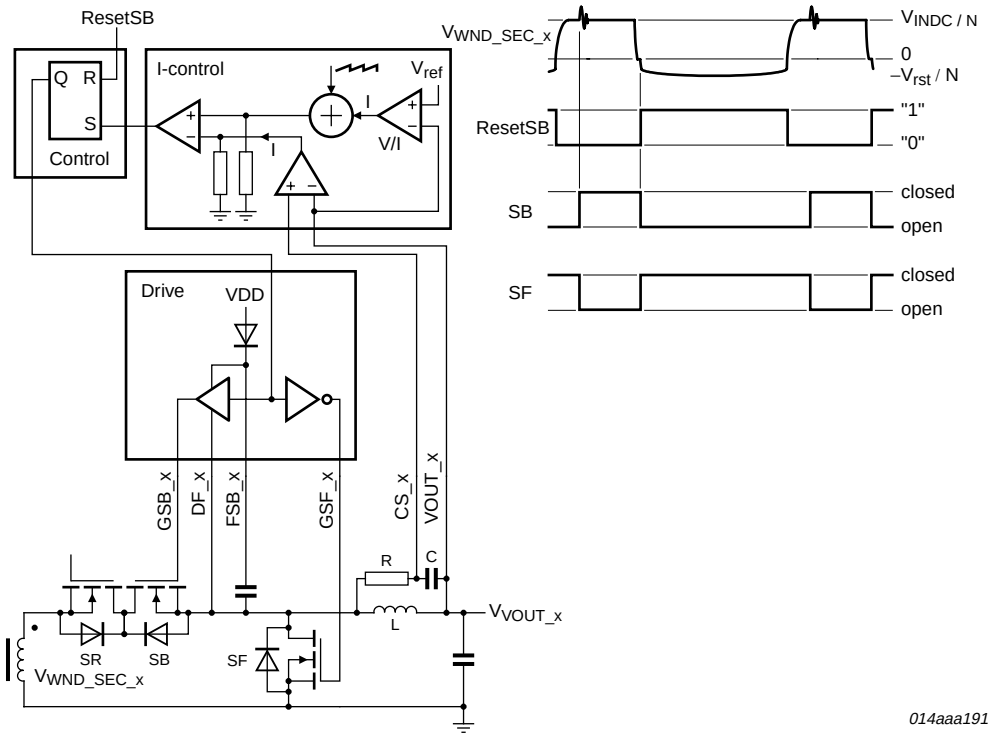
When V_{DF_x} (V_{DF_3V3}, V_{DF_5V}, or V_{DF_12V}) is (about) zero, the FSB capacitor is charged to the VDD level. Switch SB can then be turned on via this charged capacitor, as it ensures a VDD voltage with respect to DF_x (pins DF_3V3, DF_5V, or DF_12V). As this capacitor will be discharged when charging the gate source capacitance of SB, the driving voltage will be slightly less than the VDD voltage.

The source of the rectifying switch SR is connected to the transformer, which can be positive or negative. Therefore the FSR capacitor is charged via a boost circuit with a special voltage source that is about 12 V higher than the secondary transformer voltage at the appropriate time.

As the source of the rectifying switch SR is connected to the transformer, which can be either negative or positive, the TEA1781T and TEA1782T are developed in a special process (ABCD - SOI) which is capable of handling these (high) negative and positive voltages.

7.8 Output voltage regulation

The output voltage is regulated to the required voltage level via a current mode control loop.



(1) WND_SEC_x: The “x” stands for either 1 or 2

(2) GSB_x, DF_x, FSB_x, GSF_x, CS_x:
The “x” for these pins and symbols stands for either 3V3, 5V or 12V

(3) VOUT_x: The “x” stands for either 3V3, 5V, 12V1 or 12V2.

Fig 11. Output voltage regulation

When the secondary side transformer voltage is negative, switch SB is turned off to avoid negative currents, see Figure 11. Once the secondary side transformer voltage is positive and the output current in the secondary coil has dropped below a certain value, switch SB is turned on again. This value is proportional to the difference between the output voltage and the reference voltage, increased with a ramp voltage. This type of regulation is called current mode control. A ramp voltage is required to stabilize the control loop for duty cycles smaller than 0.5 and is called slope compensation.

The output current is measured using the output inductor series resistance. When the parallel RC network is $R \cdot C = \frac{L}{R_L}$ the voltage across the parallel capacitor equals the voltage across the inductors resistance. L and R_L represent the inductance and the resistance value of the output inductor.

7.9 PowerOK

The PowerOK signal is active HIGH when the main output voltages (12 V, 5 V and 3.3 V) are within their regulation limits. Figure 12 shows the corresponding block diagram.

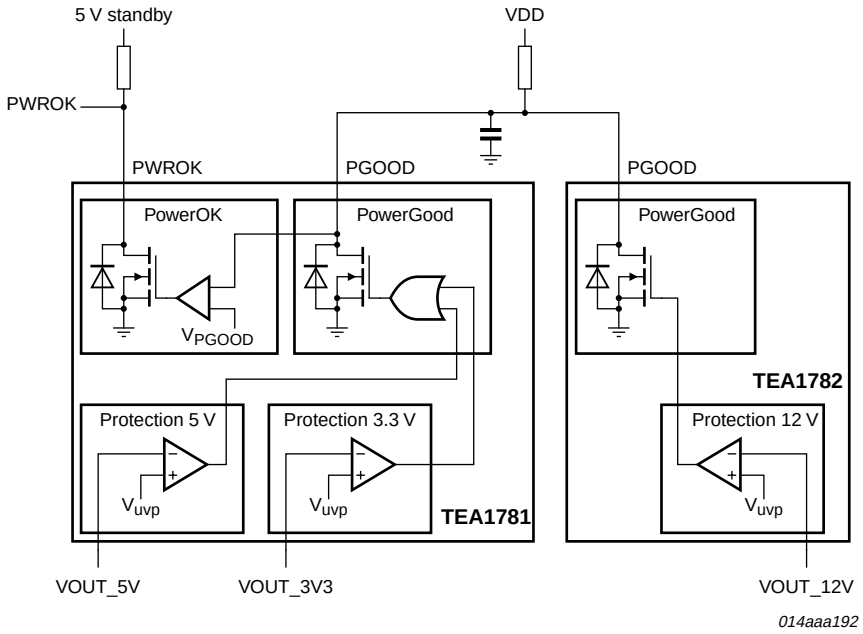


Fig 12. PowerOK circuit diagram

The PGOOD output is pulled down by the TEA1781T when either the 5 V or 3.3 V is below its lower limit, or by the TEA1782T when the 12 V is below its lower limit. When all main outputs are above their minimum value, the PGOOD signal slowly rises from zero to the VDD level. Once the PGOOD signal exceeds V_{PGOOD}, the PWROK signal becomes active high.

A delay can be set between the output voltages reaching their end value and the PWROK signal being active high via an RC network connected to the PGOOD pins.

7.10 Pull-down main outputs

According to the Intel ATX specification, the main outputs (3.3 V, 5 V and 12 V) must be at ground level in Standby mode. Therefore, these outputs are pulled low when the system is in Standby mode.

The pull-down transistors for the 3.3 V and 5 V outputs are integrated in the TEA1781T, whereas the pull-down transistor for the 12 V is integrated in the TEA1782T.

7.11 OPTO control

The TEA1782T defines the mode of operation of the system. It communicates with the TEA1781T via the ENABLE pin and with the TEA1771T primary controller via the opto coupler connected to the OPTO control block. Depending on the mode of operation, the current to the opto coupler has the following values:

Table 4. OPTO control modes

Mode of operation	I_{OPTO}
Standby mode	0 mA to ≈ 3.5 mA
Normal mode	≈ 3.5 mA
System restart	≈ 30 mA

In Standby mode, a higher I_{OPTO} current implies a higher duty cycle / frequency of the system. In Normal mode, the systems duty cycle/frequency is defined by the primary controller being related to the inverse of the input voltage. The OPTO control block diagram is given in Figure 13.

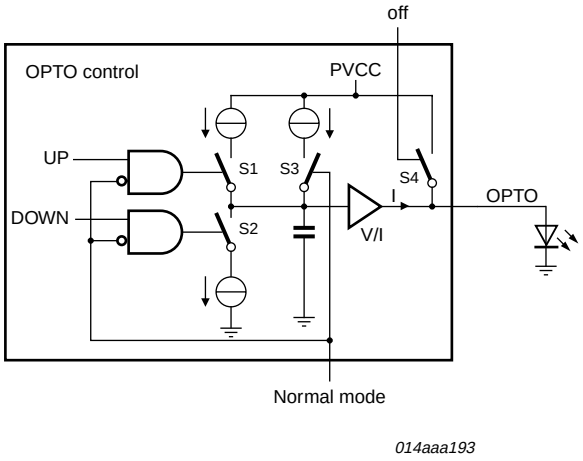


Fig 13. TEA1782T OPTO control diagram

At system start-up, the secondary controllers are supplied via a rectified secondary winding voltage. Therefore the secondary controllers are started up after the primary side has started up.

As the voltage at the OPTO pin is zero when the secondary controllers are not yet supplied, the primary side starts up at the minimum duty cycle/frequency. Once the secondary side has started, it increases the operating duty cycle/frequency of the system depending on the standby load and mode of operation.

When the system is in Normal mode, switch S3 is closed and the opto coupler current is increased to I_{OPTO} (Normal mode). In this mode, the primary duty cycle is defined by the primary controller TEA1771T and is related to the inverse of the input voltage.

When the secondary protection mode fails, switch S4 is closed and a maximum current flows through the opto coupler. This high current triggers the primary controller into Protection mode, switching off the primary main switch. A safe restart of the system will follow. This implies that the system will start up again after all the supply voltages, primary and secondary, are below their UVLO levels resulting in a total reset of the system.

In Standby mode, the system minimizes the duty cycle of the primary control switch to reduce the magnetic losses in the transformer to a minimum. As the primary duty cycle has to be at least equal to the secondary duty cycle, the system will equalize both duty cycles in Standby mode. This is regulated in the opto control block.

The opto control compares the primary and secondary standby duty cycle and defines if the primary duty cycle has to be changed, see Figure 14.

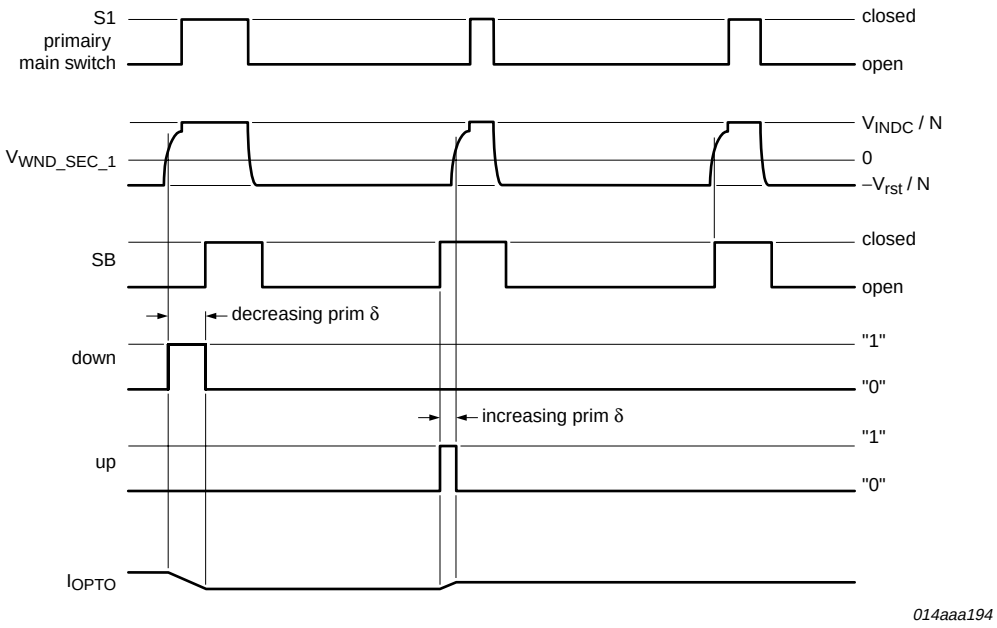


Fig 14. TEA1782T OPTO control duty cycles

The primary duty cycle is derived from the secondary transformer voltage. If $V_{WND\_SEC\_1}$ is above a certain positive level before the switch SB is turned on, a down pulse is generated. An up pulse is generated when $V_{WND\_SEC\_1}$ is high after SB is turned on.

The current into the opto coupler is regulated until it reaches a stable value via the down pulse and up pulse. Through the opto coupler, the primary duty cycle and frequency eventually stabilize to provide the duty cycle required by the secondary standby converter.

7.12 Protections

7.12.1 General

All outputs have an OVP and an OCP function. The OVP and OCP functions have a delay of $t_{d(prot)}$, which is typically 18 μs.

If the output voltage or the output current on one of the main outputs (3.3 V, 5 V, 12 V1, or 12 V2) exceeds their upper limit, the system will enter Protection mode. In this mode all main outputs are switched off by switching off all corresponding secondary switches. The system will enter the Normal mode again after toggling the PS_ON# signal or after a mains interruption.

A 12 V OVP / OCP is detected in the TEA1782T. When detecting a 12 V OVP or OCP, the pin ENABLE is pulled down and as a result both the TEA1782T and the TEA1781T will disable the main outputs. The 5 V standby output remains on.

A 3.3 V or 5 V OVP or OCP is detected in the TEA1781T and communicated to the TEA1782 via the pin ENABLE. As a result the TEA1782T will pull down the pin ENABLE, disabling all main outputs.

When the 5 V standby voltage / current exceeds its upper limit the output will be switched off. It will be turned on again at the next cycle as soon as the output voltage/current level drops below the upper limit.

7.12.2 Undervoltage protection

When undervoltage is detected on one of the main outputs (3.3 V, 5 V, 12 V) the pin PGOOD is pulled low which again pulls the PWROK signal low.

When undervoltage on the 5 V standby output is detected, the system switches to Standby mode and returns back to Normal mode once the 5 V standby is above its minimum level.

7.12.3 Overvoltage protection

As stated previously, all outputs have an OVP function. However, the 12 V1 and 12 V2 have one OVP function. It is assumed that the 12 V2 is directly coupled to the 12 V1 voltage and therefore these voltages are about equal.

All OVP levels are integrated and cannot be set externally.

7.12.4 Overcurrent protection

The OCP levels can be set externally. The maximum output current of the 12 V1 and 12 V2 are supposed to be about equal, therefore have the same OCP setting. Figure 15 gives the 12 V OCP block diagram.

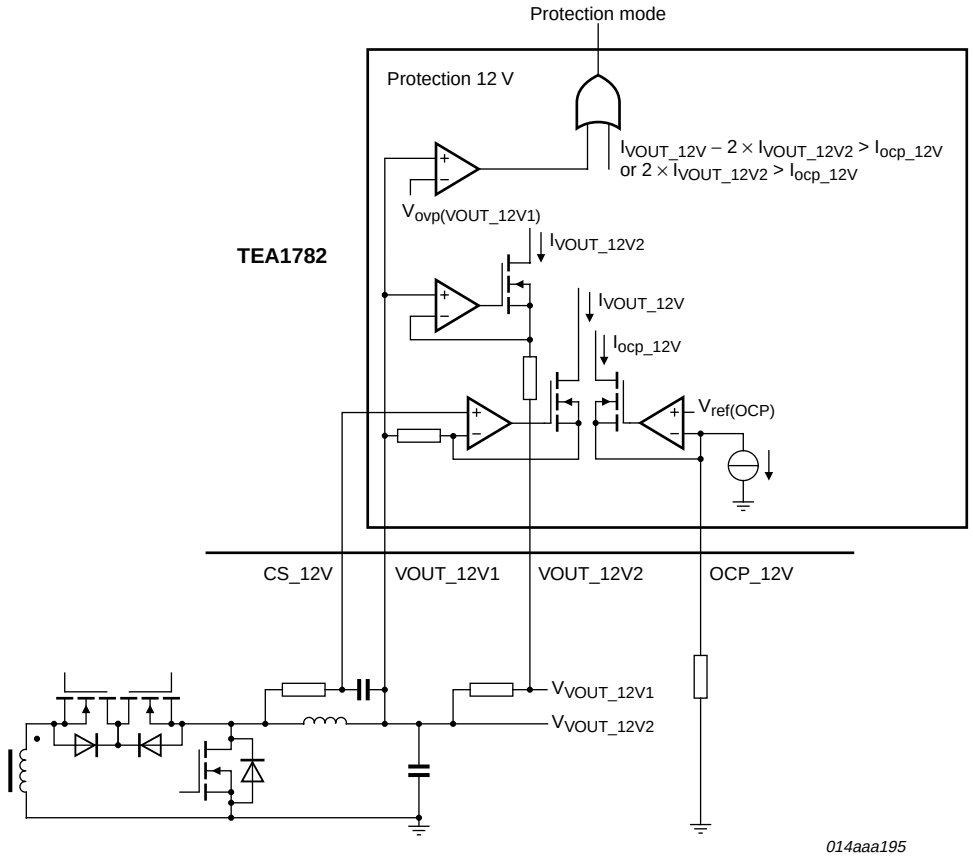


Fig 15. 12 V output overcurrent protection

The total output current (equal to $I_{out\_12V1} + I_{out\_12V2}$) is measured via an RC network across the output inductor, using the series resistance of the output inductor. The 12V2 output current is measured using a series resistance. Subtracting these two then gives the 12V1 output current.

Both output currents are then compared to the I_{ocp} (12 V output) setting. If one of these currents exceeds the I_{ocp} (12 V output) setting, the system will enter the Protection mode.The system supposes the extra series resistance to be half the value of the inductor series resistance. The I_{ocp} (12 V output) has a default setting of −100 μA, corresponding to 180 mV for 12V1, and 90 mV for 12V2.

Applying a series resistance of 5 mΩ and an inductor series resistance of 10 mΩ, the default OCP levels of the 12 V outputs are set at 18 A. The OCP levels of the 12 V outputs can be increased by a resistor from pin OCP_12V to ground and decreased by a resistor from pin VDD to pin OCP_12V.

The 3.3 V and 5 V OCP can be adjusted externally, whereas the system assumes identical 3.3 V and 5 V OCP levels, see Figure 16. The output currents are measured via an RC network across the output inductor, making use of the inductor series resistance. If either the 5 V or 3.3 V output exceeds its OCP setting, the system enters the Protection mode.

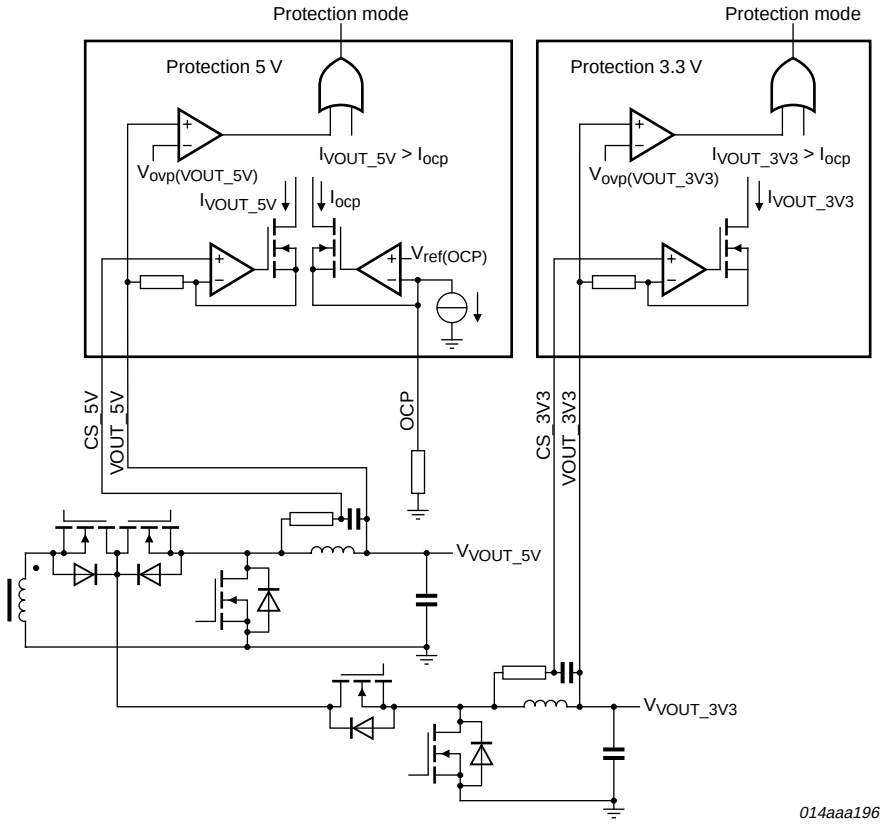


Fig 16. 3.3 V / 5 V output overcurrent protection

The I_{ocp} has a default setting of –100 µA. Applying an inductor series resistance of 10 mΩ, the default OCP level is set at 19.5 A. The OCP levels of 3.3 V and 5 V can be increased by a resistor from pin OCP to ground and decreased by a resistor from pin VDD to pin OCP.

The 5 V standby OCP level is set to approximately 2.5 A, assuming an inductors series resistance of 70 mΩ. The OCP_STB level can be increased by a resistor from pin OCP_STB to ground and decreased by a resistor from pin VDD to pin OCP_STB.

Besides changing the OCP level by a resistor connected to the OCP pin, this level can be changed by choosing a different series resistance of the output coil.

Whereas an OCP on one of the main outputs results in a latched Protection mode, a 5 V standby OCP also disables the output but resumes switching at the next cycle when the output current drops below the OCP level. When the 5 V standby output voltage drops below its minimum level, because the output current is limited, the system switches to Standby mode.

7.12.5 Overtemperature protection

The system will enter the Protection mode at an initialized temperature level via an external NTC network connected to the VNTC pin of the TEA1781T. In this way the system can be protected against overtemperature.

If an OTP is detected all main outputs will be switched off, but the 5 V standby output remains on.

7.12.6 System restart

If an OCP, OVP, or OTP is detected on one of the main outputs, all these outputs are switched off and latched. A OCP or OVP detection on the 5 V standby will switch off its output but it will be resumed again at the next cycle.

All outputs can be disabled individually by disabling the bidirectional switch (SR / SB). Disabling an output will resolve the reason why Protection mode was entered, which can be an OVP, OCP or OTP.

If a certain time after entering Protection mode ($t_{d(restart)}$ (≈ 500 µs)) the system still detects an OCP or OVP, the secondary side enters the system restart mode. In this mode the primary side is switched off via the opto coupler, followed by a safe restart. A continuous error could be caused by a shorted SB switch, for example.

If a small increase of temperature is detected because of an OTP after entering Protection mode, the system will also turn off the primary side.

So normally, an OCP, OVP or OTP will switch off the secondary outputs. Only when an OCP, OVP or OTP remains after the outputs are switched off, will the primary side be switched off. In that case the 5 V standby output will also drop.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
TEA1781T					
V_{DF_5V}	voltage on pin DF_5V		–7	+40	V
$V_{VSTARTUP}$	voltage on pin VSTARTUP		–0.4	+75	V
I_{ocp}	overcurrent protection current		–250	+80	µA
V_{CS_5V}	voltage on pin CS_5V		–0.4	+7	V
V_{VOUT_5V}	voltage on pin VOUT_5V		–0.4	+7	V
V_{VSENSE_5V}	voltage on pin VSENSE_5V		–0.4	+7	V
V_{VNTC}	voltage on pin VNTC		–0.4	+7	V
V_{ENABLE}	voltage on pin ENABLE		–0.4	+13	V
V_{PGND_5V}	voltage on pin PGND_5V		-0.8	+0.8	V
V_{DD}	supply voltage		–0.4	+13	V
V_{PGND_3V3}	voltage on pin PGND_3V3		–0.8	+0.8	V
V_{PWROK}	voltage on pin PWROK		–0.4	+13	V

Table 5. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{VSENSE_3V3}	voltage on pin VSENSE_3V3		–0.4	+7	V
V_{VOUT_3V3}	voltage on pin VOUT_3V3		–0.4	+7	V
V_{CS_3V3}	voltage on pin CS_3V3		–0.4	+7	V
V_{PGOOD}	voltage on pin PGOOD		–0.4	+7	V
V_{DF_3V3}	voltage on pin DF_3V3		–7	+40	V
$V_{WND\_SEC\_2}$	voltage on pin WND_SEC_2		–40	+40	V
General					
P_{tot}	total power dissipation	T_{amb} < 45 °C	-	<tbd>	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–20	+145	°C
V_{esd}	electrostatic discharge voltage	human body model:[1]			
		all pins	–2000	+2000	V
		machine model:[2]			
		all pins	–200	+200	V
		charged device model	-	500	V
TEA1782T					
V_{DF_12V}	voltage on pin DF_12V		-7	+73	V
I_{OCP_12V}	current on pin OCP_12V		–250	+80	µA
V_{CS_12V}	voltage on pin CS_12V	with respect to V_{VOUT_12V1}	–0.4	+0.8	V
V_{VOUT_12V1}	voltage on pin VOUT_12V1	with respect to V_{VOUT_12V2}	–0.4	+0.4	V
V_{VOUT_12V2}	voltage on pin VOUT_12V2		–0.4	+13.4	V
V_{EN_NM}	voltage on pin EN_NM		–0.4	+13	V
V_{PS_OFF}	voltage on pin PS_OFF		–0.4	+13	V
V_{PGND_12V}	voltage on pin PGND_12V		–0.8	+0.8	V
V_{DD}	supply voltage		–0.4	+13	V
V_{PGND_STB}	voltage on pin PGND_STB		–0.8	+0.8	V
V_{PGOOD}	voltage on pin PGOOD		–0.4	+13	V
V_{VOUT_STB}	voltage on pin VOUT_STB		–0.4	+7	V
V_{CS_STB}	voltage on pin CS_STB		–0.4	+7	V
I_{OCP_STB}	current on pin OCP_STB		–250	+80	µA

Table 5. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DF_STB}	voltage on pin DF_STB		–0.8	+73	V
$V_{WND\_SEC\_1}$	voltage on pin WND_SEC_1		–73	+73	V
General					
P_{tot}	total power dissipation	T_{amb} < 45 °C	-	<tbd>	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–20	+145	°C
V_{esd}	electrostatic discharge voltage	human body model:[1]			
		all pins	–1500	+1500	V
		machine model:[2]			
		all pins	–150	+150	V
		charged device model		+500	V

[1] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω series resistor.

[3] Peak voltages up to the OVP level are allowed.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	<tbd>	K/W

[1] Thermal resistance $R_{th(j-a)}$ can be lower when pin GND is connected to sufficient copper area on the printed-circuit board. See the TEA1771T application notes for details.

10. Characteristics

Table 7. TEA1781T characteristics

T_{amb} = 25 °C; no over temperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
$V_{reg(VDD)}$	regulation voltage on pin VDD	$V_{startup}$ = 14 V to 90 V	9.0	9.5	10.1	V
I_{VDD}	current on pin VDD	Standby mode	-	1.2	-	mA
		Normal mode	-	1.9	-	mA
Drivers						
R_{pu}	pull-up resistance	SR / SB drivers; $V_{WND(SEC)\_2} = V_{DF\_3V3} = V_{DF\_5V}$ = 40 V; $V_{FSR} = V_{FSB\_3V3} = V_{FSB\_5V}$ = 52 V; $V_{GSB\_3V3} = V_{GSB\_5V} = V_{GSR}$ = 51.5 V	13	17	21	Ω
		SF drivers; $V_{DF\_3V3} = V_{DF\_5V}$ = –1 V; $V_{VDD} - V_{GSF\_3V3}$ (or V_{GSF_5V}) = 0.5 V	-	30	-	Ω
R_{pd}	pull-down resistance	SR / SB drivers; $V_{WND(SEC)\_2} = V_{DF\_3V3} = V_{DF\_5V}$ = 40 V; $V_{FSR} = V_{FSB\_3V3} = V_{FSB\_5V}$ = 52 V; $V_{GSB\_3V3} = V_{GSB\_5V} = V_{GSR}$ = 40.5 V	3.5	4.5	5.5	Ω
		SF driver; $V_{DF\_3V3} = V_{DF\_5V}$ = 0 V; $V_{GSF\_3V3} = V_{GSF\_5V}$ = 0.5 V	3.5	4.5	5.5	Ω
$V_{float(UVLO)}$	undervoltage lockout floating voltage	SR/SB driver	5.0	5.4	5.8	V
Control						
$V_{trip(L)}$	LOW-level trip voltage	enable GSB; voltage on pin WND_SEC_2	–4.7	–4.1	–3.5	V
		enable GSR; voltage on pin DF (3.3 V and 5 V)	3.4	4.5	5.6	V
$V_{trip(H)}$	HIGH-level trip voltage	enable GSB; voltage on pin WND_SEC_2	–2.2	–1.9	–1.6	V
		enable GSR; voltage on pin DF (3.3 V and 5 V)	5.8	7.0	8.2	V
t_d	delay time	enable GSB	-	0.9	-	µs
I-Control 3.3 V						
$V_{ref(3V3)}$	reference voltage (3.3 V)	$V_{CS\_3V3} = V_{VOUT}$	3.25	3.35	3.45	V
		$V_{CS\_3V3} = V_{VOUT}$ + 100 mV	3.19	3.29	3.39	V
I-Control 5 V						
$V_{ref(5V)}$	reference voltage (5 V)	$V_{CS\_5V} = V_{VOUT}$	4.95	5.10	5.25	V
		$V_{CS\_5V} = V_{VOUT}$ + 100 mV	4.85	5.00	5.15	V
Pins VOUT_3V3 and VOUT_5V						
I_{pd}	pull-down current	Standby mode; $V_{VOUT\_3V3} = V_{VOUT\_5V}$ = 0.4 V	2	4	6	mA
Enable						
$V_{trip(ENABLE)}$	trip voltage on pin ENABLE		7.0	8.0	9.0	V

Table 7. TEA1781T characteristics *...continued*

T_{amb} = 25 °C; no over temperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{ENABLE}	current on pin ENABLE	current pulled out of the pin ENABLE to disable, to move to Protection mode		1.0	-	-	mA
Soft start							
$t_{start(soft)}$	soft start time			10	15	20	ms
PGOOD and PWROK							
$I_{sink(PGOOD)}$	sink current on pin PGOOD	V_{PGOOD} = 0.4 V		6.0	-	-	mA
$V_{trip(H)(PGOOD)}$	HIGH-level trip voltage on pin PGOOD			2.5	2.7	3.0	V
$V_{trip(L)(PGOOD)}$	LOW-level trip voltage on pin PGOOD	LOW		2.2	2.4	2.7	V
$I_{sink(PWROK)}$	sink current on pin PWROK	V_{PWROK} = 0.4 V		16	-	-	mA
Overcurrent protection							
$V_{ref(OCP)}$	reference voltage on pin OCP	OCP = n.c.		1.21	1.25	1.29	V
V_{ocp}	overcurrent protection voltage	$V_{CS\_x} - V_{VOUT}$ activating current protection; OCP = n.c.	[1]	155	180	205	mV
		$V_{CS\_x} - V_{VOUT}$ activating current protection; I_{ocp} = –100 µA	[1]	320	380	440	mV
		$V_{CS\_x} - V_{VOUT}$ activating current protection; I_{ocp} = 50 µA	[1]	60	80	105	mV
		$V_{CS\_x} - V_{VOUT}$ activating current protection during soft start; OCP = n.c.	[1]	310	360	410	mV
Undervoltage/overvoltage protection							
$V_{uvp(VOUT\_3V3)}$	undervoltage protection voltage on pin VOUT_3V3			2.60	2.80	3.00	V
$V_{uvp(VOUT\_5V)}$	undervoltage protection voltage on pin VOUT_5V			4.00	4.25	4.50	V
$V_{ovp(VOUT\_3V3)}$	overvoltage protection voltage on pin VOUT_3V3			3.76	4.00	4.25	V
$V_{ovp(VOUT\_5V)}$	overvoltage protection voltage on pin VOUT_5V			6.00	6.40	6.80	V
Temperature protection							
$V_{otp(H)}$	HIGH-level overtemperature protection voltage	V_{ENABLE} = 12 V		450	505	560	mV
$V_{otp(L)}$	LOW-level overtemperature protection voltage	V_{ENABLE} = 0 V		320	375	430	mV

[1] V_{CS_x}: the “x” stand for either “3V3” or ”5V”.

Table 8. TEA1782T characteristics

T_{amb} = 25 °C; no over temperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
$V_{startup(VDD)}$	start-up voltage on pin VDD		8.0	8.5	9.0	V
$V_{stop(VDD)}$	stop voltage on pin VDD		6.9	7.4	7.9	V
I_{VDD}	current on pin VDD		-	3.0	-	mA
$t_{d(startup)}$	start-up delay time		5	7	9	ms
Driver SF standby						
R_{pu}	pull-up resistance	SF driver; $V_{DF\_12V} = V_{DF\_STB} = -1$ V; $V_{VDD} - V_{GSF\_12V}$ (or V_{GSF_STB}) = 0.5 V	-	35	-	Ω
R_{pd}	pull-down resistance	SF driver; $V_{DF\_12V} = V_{DF\_STB} = 0$ V; $V_{GSF\_12V} = V_{GSF\_STB}$ = 0.5 V	5.0	6.5	8.0	Ω
Drivers (12 V and SB standby)						
R_{pu}	pull-up resistance	SR / SB drivers; $V_{WND(SEC)\_1} = V_{DF\_12V} = V_{DF\_STB}$ = 73 V; $V_{FSR} = V_{FSB\_12V} = V_{FSB\_STB}$ = 85 V; $V_{GSR} = V_{GSB\_12V} = V_{GSB\_STB}$ = 84.5 V	13	17	21	Ω
		SF driver; $V_{DF\_12V} = V_{DF\_STB} = -1$ V; $V_{VDD} - V_{GSF\_12V}$ (or V_{GSF_STB}) = 0.5 V	-	30	-	Ω
R_{pd}	pull-down resistance	SR / SB drivers; $V_{WND(SEC)\_1} = V_{DF\_12V} = V_{DF\_STB}$ = 73 V; $V_{FSR} = V_{FSB\_12V} = V_{FSB\_STB}$ = 85 V; $V_{GSR} = V_{GSF\_12V} = V_{GSF\_STB}$ = 73.5 V	3.5	4.5	5.5	Ω
		$V_{DF\_12V} = V_{DF\_STB} = 0$ V; $V_{GSF\_12V} = V_{GSF\_STB}$ = 0.5 V	3.5	4.5	5.5	Ω
$V_{float(UVLO)}$	undervoltage lockout floating voltage		5.0	5.4	5.8	V
Control standby						
$V_{trip(L)}$	LOW-level trip voltage	enable GSB standby; voltage on pin WND_SEC_1	1.0	2.0	3.0	V
$V_{trip(H)}$	HIGH-level trip voltage	enable GSB standby; voltage on pin WND_SEC_1	8.0	9.0	10.0	V
Control 12 V						
$V_{trip(L)}$	LOW-level trip voltage	enable GSB 12 V; voltage on pin WND_SEC_1	−12.5	−11	−9.5	V
		enable GSR; voltage on pin DF	3.8	4.6	5.4	V
$V_{trip(H)}$	HIGH-level trip voltage	enable GSB 12 V; voltage on pin WND_SEC_1	−5.5	−5.0	−4.5	V
		enable GSR; voltage on pin DF	6.4	7.2	8.0	V
t_d	delay time	enable GSB 12 V	0.7	0.9	1.1	µs
I-control standby						
$V_{ref(stb)}$	standby reference voltage		4.85	5.00	5.15	V
		$V_{CS\_x} = V_{VOUT}$ + 100 mV [1]	4.7	4.9	5.1	V

Table 8. TEA1782T characteristics *...continued*

T_{amb} = 25 °C; no over temperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I-Control 12 V							
$V_{ref(12V)}$	reference voltage (12 V)			11.7	12.1	12.4	V
		$V_{CS\_x} = V_{VOUT}$ + 100 mV	[1]	11.5	11.9	12.3	V
Pins VOUT_12V and VOUT_STB							
I_{pd}	pull-down current	Standby mode; $V_{OUT\_12V} = V_{OUT\_STB}$ = 0.4 V		4	6	8	mA
Enable Normal mode							
V_{EN_NM}	voltage on pin EN_NM			1.14	1.20	1.26	V
		system to Standby mode		0.66	0.70	0.74	V
Digital control pin PS_OFF							
V_{trip}	trip voltage	Normal mode		1.0	1.2	1.4	V
		Standby mode		1.4	1.7	2.0	V
Enable							
V_{ENABLE}	voltage on pin ENABLE	Normal mode		10.5	11.0	11.5	V
		Standby mode		3.8	4.2	4.6	V
$I_{prot(ENABLE)}$	protection current on pin ENABLE	Normal mode; Protection mode		–600	–450	–300	µA
Soft start							
$t_{start(soft)}$	soft start time			10	15	20	ms
PowerGood and PowerOK							
$I_{sink(PGOOD)}$	sink current on pin PGOOD	V_{PGOOD} = 0.4 V		6.0	-	-	mA
OPTO control							
I_{OPTO}	current on pin OPTO	V_{OPTO} = 5 V					
		Standby mode		0	-	I_{OPTO} (Normal mode)	mA
		Normal mode		–4.5	–3.5	–2.5	mA
		system restart		–40	–30	–20	mA
Overcurrent protection (OCP levels for 12 V2 are half the values given below)							
$V_{ref(OCP\_12V)}$	reference voltage on pin OCP_12V			1.18	1.23	1.28	V
$V_{ref(OCP\_STB)}$	reference voltage on pin OCP_STB						

Table 8. TEA1782T characteristics *...continued*

T_{amb} = 25 °C; no over temperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{ocp}	overcurrent protection voltage	V_{CS_x} - V_{VOUT} activating current protection; OCP = n.c. (Can V_{CS} be changed to e.g. VCS_12V or VCS_STB here. If so, then that is preferred here.)	[1]	155	180	205	mV
		V_{CS_x} – V_{VOUT} activating current protection; I_{OCP} = –100 mA (Can V_{CS} be changed to e.g. VCS_12V or VCS_STB here. If so, then that is preferred here.)	[1]	320	380	440	mV
		V_{CS_x} – V_{OUT} activating current protection; I_{OCP} = +50 mA (Can V_{CS} be changed to e.g. VCS_12V or VCS_STB here. If so, then that is preferred here.)	[1]	60	80	105	mV
		V_{CS_STB} – V_{VOUT_STB} activating current protection during soft start; OCP_STB = n.c.		230	270	310	mV
		V_{CS_12V} – V_{VOUT_12V} activating current protection during soft start; OCP_12V = n.c.		310	360	410	mV
Undervoltage protection/overvoltage protection							
$V_{uvp(VOUT\_STB)}$	undervoltage protection voltage on pin VOUT_STB			3.90	4.25	4.60	V
$V_{uvp(VOUT\_12V1)}$	undervoltage protection voltage on pin VOUT_12V1			9.70	10.20	10.70	V
$V_{ovp(VOUT\_STB)}$	overvoltage protection voltage on pin VOUT_STB			5.70	6.10	6.50	V
$V_{ovp(VOUT\_12V1)}$	overvoltage protection voltage on pin VOUT_12V1			13.7	14.5	15.2	V
Protection							
$t_{d(prot)}$	protection delay time			9	18	27	µs
System restart							
$t_{d(restart)}$	restart delay time			275	550	825	µs

[1] V_{CS_x}: The “x” stands for either “12V” or “STB”

11. Application information

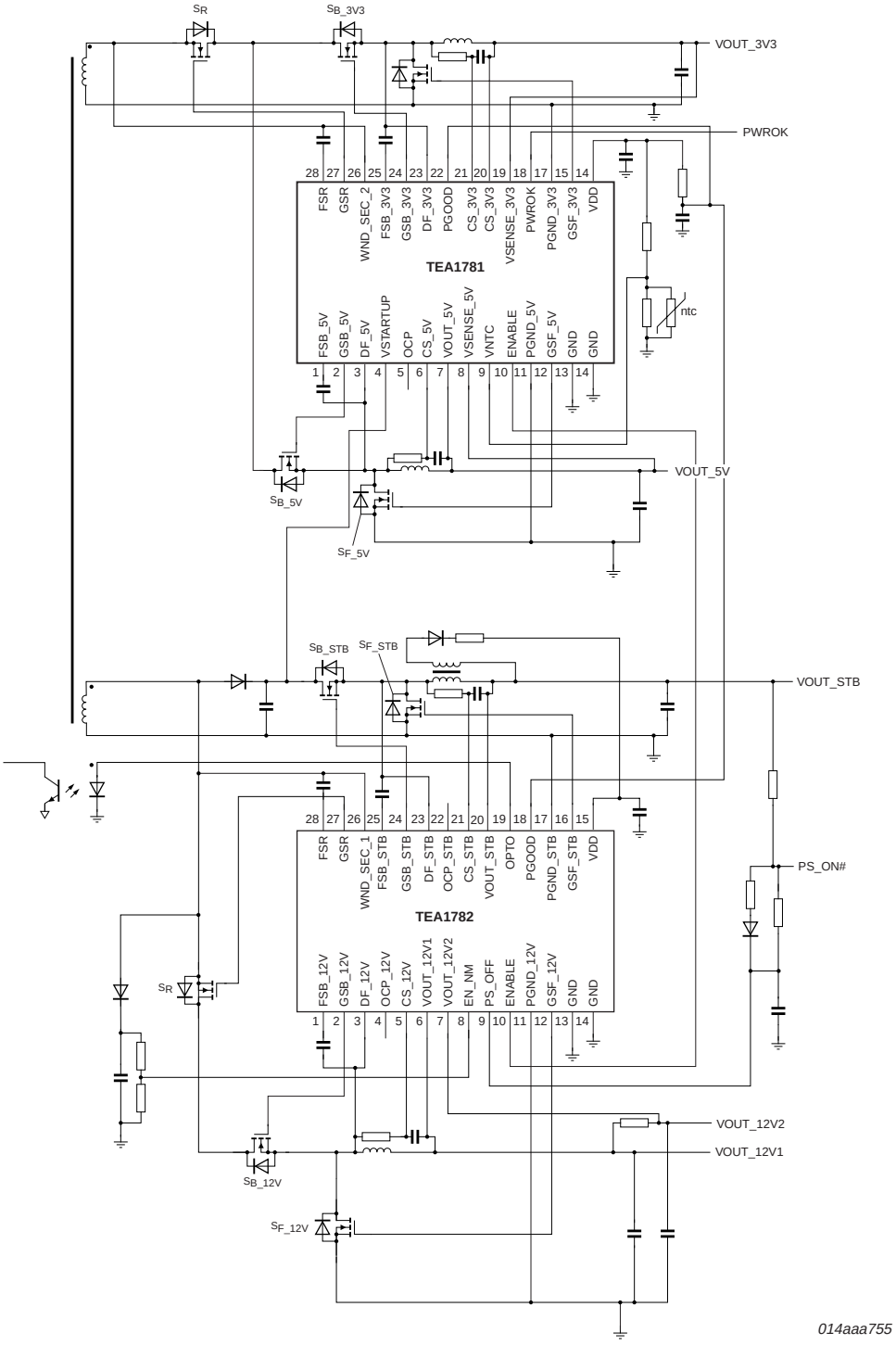
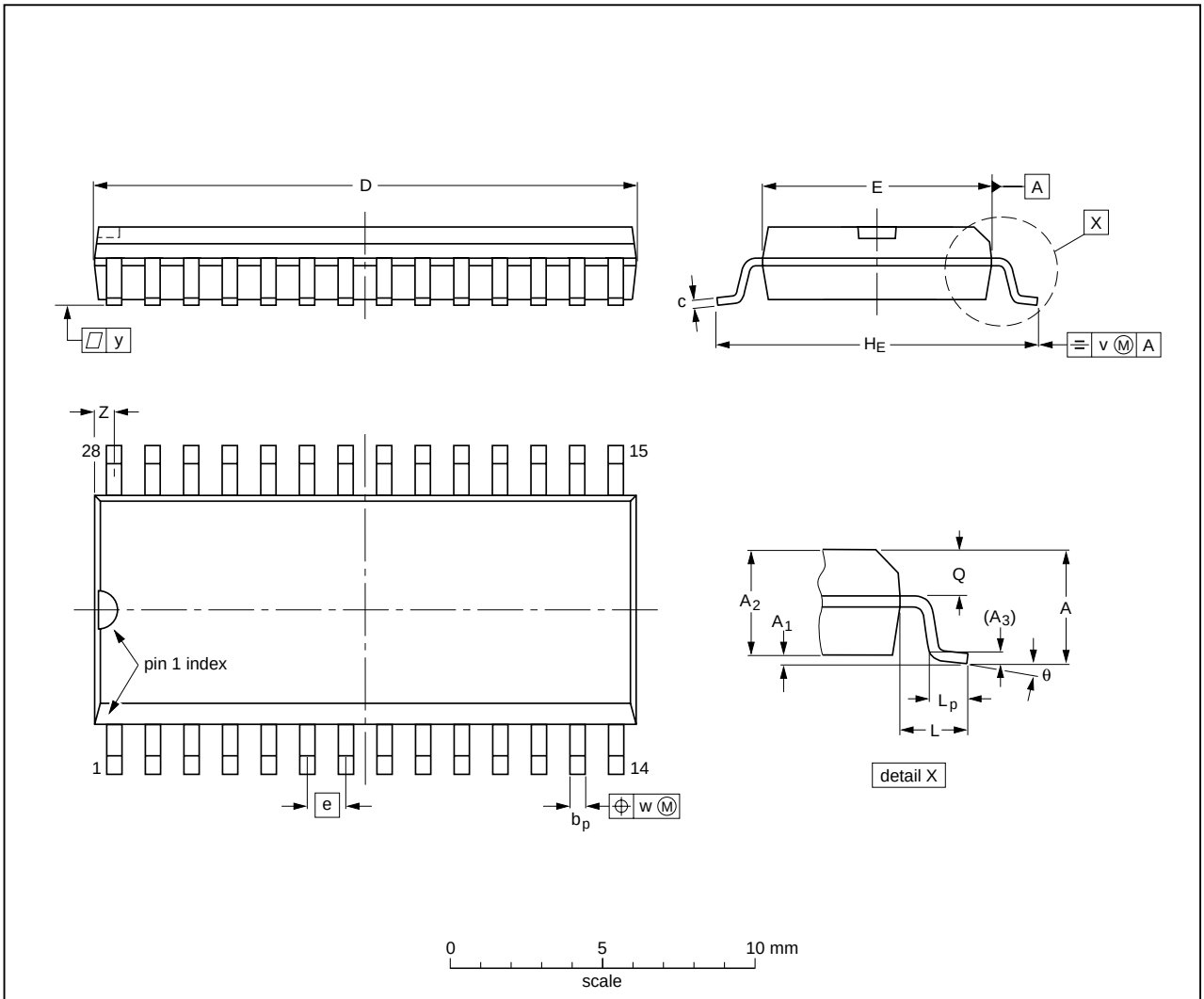


Fig 17. Application diagram

12. Package outline

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT136-1	075E06	MS-013				~~99-12-27~~ 03-02-19

Fig 18. Package outline SOT136-1 (SO28)

13. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1781_82_1	20090213	Preliminary data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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