Smart Battery Charger Controller

FEATURES

- **Single Chip Smart Battery Charger Controller**
- **100% Compliant (Rev. 1.1) SMBus Support Allows for Operation with or without Host**
- **Up to 4A Charging Current Capability**
- **High Efficiency Synchronous Buck Charger**
- **V_{BAT} Optimized 3V to 5.5V**
- SMBus Accelerator Improves SMBus Timing
- Hardware Interrupt and SMBAlert Response Eliminate Interrupt Polling
- 0.5V Dropout Voltage; Maximum Duty Cycle > 98%
- AC Adapter Current Limit Maximizes Charge Rate
- ±0.8% Voltage Accuracy; ±4% Current Accuracy
- 10-Bit DAC for Charge Current Programming
- 11-Bit DAC for Charger Voltage Programming
- User-Selectable Overvoltage and Overcurrent Limits
- High Noise Immunity SafetySignal Sensor
- Available in a 24-Pin SSOP Package

APPLICATIONS

- Portable Instruments and Computers
- Data Storage Systems and Battery Backup Servers

DESCRIPTION

The LTC®4101 Smart Battery Charger is a single chip charging solution that dramatically simplifies construction of an SBS compliant system. The LTC4101 implements a Level 2 charger function whereby the charger can be programmed by the battery or by the host. A SafetySignal on the battery being charged is monitored for temperature, connectivity and battery type information. The SMBus interface remains alive when the AC power adapter is removed and responds to all SMBus activity directed to it, including SafetySignal status (via the ChargerStatus command). The charger also provides an interrupt to the host whenever a status change is detected (e.g., battery removal, AC adapter connection).

Charging current and voltage are restricted to chemistry-specific limits for improved system safety and reliability. Limits are programmable by two external resistors. Additionally, the maximum average current from the AC adapter is programmable to avoid overloading the adapter when simultaneously supplying load current and charging current. When supplying system load current, charging current is automatically reduced to prevent adapter overload.

TYPICAL APPLICATION

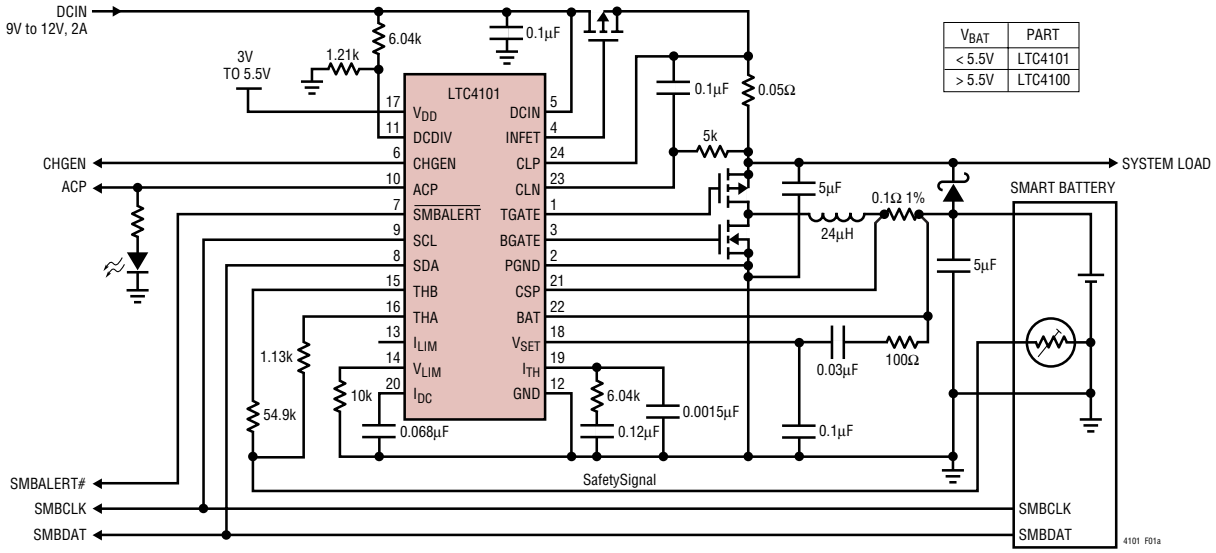


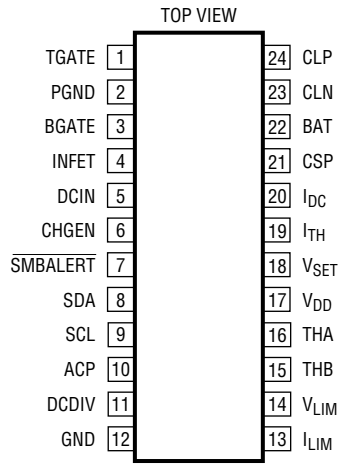
Figure 1. 1A Smart Battery Charger

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Voltage from V_{DD} to GND 7V/–0.3V
Voltage from CHGEN, DCDIV, SDA, SCL and $\overline{\text{SMBALERT}}$ to GND 7V/–0.3V
Voltage from DCIN, CLP, CLN to GND 32V/–0.3V
Voltage from CLP to CLN ..... ±0.3V
PGND wrt. GND ..... ±0.3V
CSP, BAT to GND 28V/–5V
Operating Ambient Temperature Range (Note 4) ..... –40°C to 85°C
Junction Temperature Range ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
24-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 90°C/W

ORDER PART NUMBER
LTC4101EG

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DCIN} = 20V, V_{DD} = 3.3V, V_{BAT} = 4V unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	DCIN Operating Range		●	6		28	V
I_{DCIN}	DCIN Operating Current	Charging, Sum of Currents on DCIN, CLP and CLN			3	5	mA
V_{TOL}	Charge Voltage Accuracy	(Note 2)	 ●	–1.1 –1.3		1.1 1.3	% %
I_{TOL}	Charge Current Accuracy (Note 3)	$V_{CSP} – V_{BAT}$ Target = 102.3mV I_{DAC} = 0xFFFF	 ●	–2 –3		6 7	% %
V_{DD}	V_{DD} Operating Voltage	0V ≤ V_{DCIN} ≤ 28V	●	3		5.5	V
Shutdown							
	Battery Leakage Current	DCIN = 0V, $V_{CLP} = V_{CLN} = V_{CSP} = V_{BAT}$	●		15	35	µA
UVLO	Undervoltage Lockout Threshold	DCIN Rising, V_{BAT} = 0V	●	4.2	4.7	5.5	V
	V_{DD} Power-Fail	Part Held in Reset Until this V_{DD} Present	●			3	V
	DCIN Current in Shutdown	V_{CHGEN} = 0V			2	3	mA
Current Sense Amplifier, CA1							
	Input Bias Current into BAT Pin				11.66		µA
CMSL	CA1/I_1 Input Common Mode Low		●	0			V
CMSH	CA1/I_1 Input Common Mode High	V_{DCIN} ≤ 28V	●			V_{CLN}-0.2	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Comparators I_{REV}							
I_{TREV}	Reverse Current Threshold (V_{CSP}-V_{BAT})				–30		mV
Current Sense Amplifier, CA2							
	Transconductance				1		mmho
	Source Current	Measured at I_{TH}, V_{ITH} = 1.4V			–40		µA
	Sink Current	Measured at I_{TH}, V_{ITH} = 1.4V			40		µA
Current Limit Amplifier							
	Transconductance				1.5		mmho
V_{CLP}	Current Limit Threshold		●	93	100	107	mV
I_{CLN}	CLN Input Bias Current				50		nA
Voltage Error Amplifier, EA							
	Transconductance				1		mmho
	Sink Current	Measured at I_{TH}, V_{ITH} = 1.4V			36		µA
OVSD	Overvoltage Shutdown Threshold as a Percent of Programmed Charger Voltage		●	102	107	110	%
Input P-Channel FET Driver (INFET)							
	DCIN Detection Threshold (V_{DCIN}-V_{CLP})	DCIN Voltage Ramping Up from V_{CLP}-0.05V	●	0	0.17	0.25	V
	Forward Regulation Voltage (V_{DCIN}-V_{CLP})		●		25	50	mV
	Reverse Voltage Turn-Off Voltage (V_{DCIN}-V_{CLP})		●	–60	–25		mV
	INFET “ON” Clamping Voltage (V_{DCIN}-V_{INFET})	I_{INFET} = 1µA	●	5	5.8	6.5	V
	INFET “OFF” Clamping Voltage (V_{DCIN}-V_{INFET})	I_{INFET} = –25µA				0.25	V
Oscillator							
f_{OSC}	Regulator Switching Frequency			255	300	345	kHz
f_{MIN}	Regulator Switching Frequency in Drop Out	Duty Cycle ≥ 98%		20	25		kHz
DC_{MAX}	Regulator Maximum Duty Cycle	V_{CSP} = V_{BAT}		98	99		%
Gate Drivers (TGATE, BGATE)							
	V_{TGATE} High (V_{CLP}-V_{TGATE})	I_{TGATE} = –1mA				50	mV
	V_{BGATE} High	C_{LOAD} = 3000pF		4.5	5.6	10	V
	V_{TGATE} Low (V_{CLP}-V_{TGATE})	C_{LOAD} = 3000pF		4.5	5.6	10	V
	V_{BGATE} Low	I_{BGATE} = 1mA				50	mV
TGTR TGTF	TGATE Transition Time TGATE Rise Time TGATE Fall Time	 C_{LOAD} = 3000pF, 10% to 90% C_{LOAD} = 3000pF, 10% to 90%			 50 50	 110 100	 ns ns
BGTR BGTF	BGATE Transition Time BGATE Rise Time BGATE Fall Time	 C_{LOAD} = 3000pF, 10% to 90% C_{LOAD} = 3000pF, 10% to 90%			 40 40	 90 80	 ns ns
	V_{TGATE} at Shutdown (V_{CLN}-V_{TGATE})	I_{TGATE} = –1µA				100	mV
	V_{BGATE} at Shutdown	I_{TGATE} = 1µA				100	mV

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Present Comparator							
V_{ACP}	DCDIV Threshold	V_{DCDIV} Rising from 1V to 1.4V	●	1.14	1.20	1.26	V
	DCDIV Hysteresis				25		mV
	DCDIV Input Bias Current	V_{DCDIV} = 1.2V		–1		1	µA
	ACP V_{OH}	I_{ACP} = –2mA		2			V
	ACP V_{OL}	I_{ACP} = 1mA				0.5	V
	DCDIV to ACP Delay	V_{DCDIV} = 1.3V				10	µs
SafetySignal Decoder							
	SafetySignal Trip (RES_COLD/RES_OR)	R_{THA} = 1130Ω ±1%, C_{TH} = 1nF (Note 6) R_{THB} = 54.9Ω ±1%	●	95	100	105	kΩ
	SafetySignal Trip (RES_IDEAL/RES_COLD)	R_{THA} = 1130Ω ±1%, C_{TH} = 1nF (Note 6) R_{THB} = 54.9Ω ±1%	●	28.5	30	31.5	kΩ
	SafetySignal Trip (RES_HOT/RES_IDEAL)	R_{THA} = 1130Ω ±1%, C_{TH} = 1nF (Note 6) R_{THB} = 54.9Ω ±1%	●	2.85	3	3.15	kΩ
	SafetySignal Trip (RES_UR/RES_HOT)	R_{THA} = 1130Ω ±1%, C_{TH} = 1nF (Note 6) R_{THB} = 54.9Ω ±1%	●	425	500	575	Ω
	Time Between SafetySignal Measurements	DCDIV = 1.3V DCDIV = 1V			32	 250	ms ms
DACs							
	Charging Current Resolution	Guaranteed Monotonic Above I_{MAX}/16		10			Bits
	Charging Current Granularity	R_{ILIM} = 0 R_{ILIM} = 10k ±1% R_{ILIM} = 33k ±1% R_{ILIM} = Open (or Short to V_{DD})			1 2 4 4		mA mA mA mA
	Wake-Up Charging Current ($I_{WAKE-UP}$)	All Values of R_{ILIM} All Values of R_{VLIM}			80 (Note 5)		mA
	Charging Current Limit CSP – BAT	R_{ILIM} = 0 (0-1A) Charging Current = 0x03FF (0x0400 Note 7)		97.3		107.3	mV
		R_{ILIM} = 10k ±1% (0-2A) Charging Current = 0x07FE (0x0800 Note 7)		97.3		107.3	mV
		R_{ILIM} = 33k ±1% (0-3A) Charging Current = 0x0BFC (0x0C00 Note 7)		72.3		82.3	mV
		R_{ILIM} = 0pen (or Short to V_{DD}) (0-4A) Charging Current = 0x0FFC (0x1000 Note 7)	●	97.3		107.3	mV
	Charging Voltage Resolution	Guaranteed Monotonic (2.9V ≤ V_{BAT} ≤ 5.6V)		11			Bits
	Charging Voltage Granularity				16		mV
	Charging Voltage Limit	R_{VLIM} = 0 Charging Voltage = 0x1090 (Note 7)		4.206	4.240	4.274	V
		R_{VLIM} = 10k ±1% Charging Voltage = 0x10D0 (Note 7)		4.270	4.304	4.338	V
		R_{VLIM} = 33k ±1% Charging Voltage = 0x1150 (Note 7)		4.397	4.432	4.467	V
		R_{VLIM} = 100k ±1% Charging Voltage = 0x11A0 (Note 7)		4.476	4.512	4.548	V
		R_{VLIM} = 0pen (or Short to V_{DD}) Charging Voltage = 0x1580 (Note 7)		5.460	5.504	5.548	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Levels							
V_{IL}	SCL/SDA Input Low Voltage	V_{DD} = 3V and V_{DD} = 5.5V	●			0.8	V
V_{IH}	SCL/SDA Input High Voltage	V_{DD} = 3V and V_{DD} = 5.5V	●	2.1			V
V_{OL}	SDA Output Low Voltage	$I_{PULL-UP}$ = 350µA	●			0.4	V
I_{IL}	SCL/SDA Input Current	V_{SDA}, V_{SCL} = V_{IL}		–1		1	µA
I_{IH}	SCL/SDA Input Current	V_{SDA}, V_{SCL} = V_{IH}		–1		1	µA
V_{OL}	$\overline{\text{SMBALERT}}$ Output Low Voltage	$I_{PULL-UP}$ = 500µA	●			0.4	V
	$\overline{\text{SMBALERT}}$ Output Pull-Up Current	$V_{\overline{\text{SMBALERT}}}$ = V_{OL}		–17.5	–10	–3.5	µA
I_{LEAK}	SDA/SCL/$\overline{\text{SMBALERT}}$ Power Down Leakage	V_{SDA}, V_{SCL}, $V_{\overline{\text{SMBALERT}}}$ = 5.5V, V_{DD} = 0V	●	–2		2	µA
V_{OL}	CHGEN Output Low Voltage	I_{OL} = 100µA	●			0.5	V
	CHGEN Output Pull-Up Current	V_{CHGEN} = V_{OL}		–17.5	–10	–3.5	µA
V_{IL}	CHGEN Input Low Voltage		●			0.9	V
V_{IH}	CHGEN Input High Voltage	V_{DD} = 3V V_{DD} = 5.5V	●	2.5	 3.9		V V
	Power-On Reset Duration	V_{DD} Ramp from 0V to >3V in <5µs			100		µs
SMBus Timing (Refer to System Management Bus Specification, Revision 1.1, Section 2.1 for Timing Diagrams)							
t_{HIGH}	SCL Serial Clock High Period	$I_{PULL-UP}$ = 350µA, C_{LOAD} = 250pF, R_{PU} = 9.31k, V_{DD} = 3V and V_{DD} = 5.5V	●	4			µs
t_{LOW}	SCL Serial Clock Low Period	$I_{PULL-UP}$ = 350µA, C_{LOAD} = 250pF, R_{PU} = 9.31k, V_{DD} = 3V and V_{DD} = 5.5V	●	4.7		15000	µs
t_R	SDA/SCL Rise Time	C_{LOAD} = 250pF, R_{PU} = 9.31k, V_{DD} = 3V and V_{DD} = 5.5V	●			1000	ns
t_F	SDA/SCL Fall Time	C_{LOAD} = 250pF, R_{PU} = 9.31k, V_{DD} = 3V and V_{DD} = 5.5V	●			300	ns
$t_{SU:STA}$	Start Condition Setup Time	V_{DD} = 3V and V_{DD} = 5.5V	●	4.7			µs
$t_{HD:STA}$	Start Condition Hold Time	V_{DD} = 3V and V_{DD} = 5.5V	●	4			µs
$t_{HD:DAT}$	SDA to SCL Falling-Edge Hold Time, Slave Clocking in Data	V_{DD} = 3V and V_{DD} = 5.5V	●	300			ns
$t_{TIMEOUT}$	Time Between Receiving Valid ChargingCurrent() and ChargingVoltage() Commands	V_{DD} = 3V and V_{DD} = 5.5V	●	140	175	210	sec

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliabilty and lifetime.

Note 2: See Test Circuit.

Note 3: Does not include tolerance of current sense resistor.

Note 4: The LTC4101E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

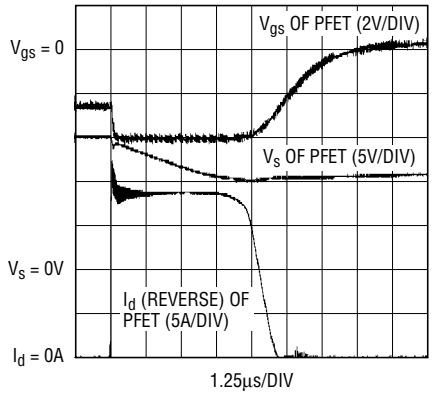
Note 5: Current accuracy dependent upon circuit compensation and sense resistor.

Note 6: C_{TH} is defined as the sum of capacitance on THA, THB and SafetySignal.

Note 7: The corresponding overrange bit will be set when a HEX value greater than or equal to this value is used.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

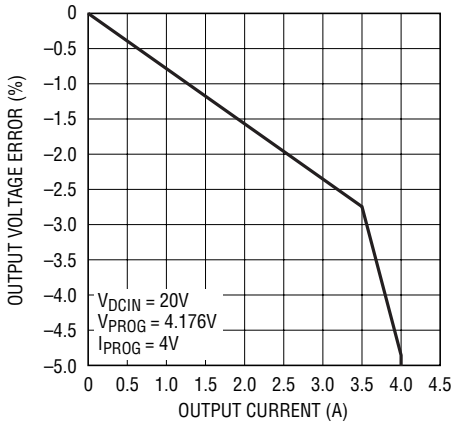
INFET Response Time to Reverse Current



TEST PERFORMED ON DEMOBOARD
V_{IN} = 15V_{DC} V_{CHARGE} = 4.2V
CHARGER = ON INFET = 1/2 Si4925DY
I_{CHARGE} = <10mA

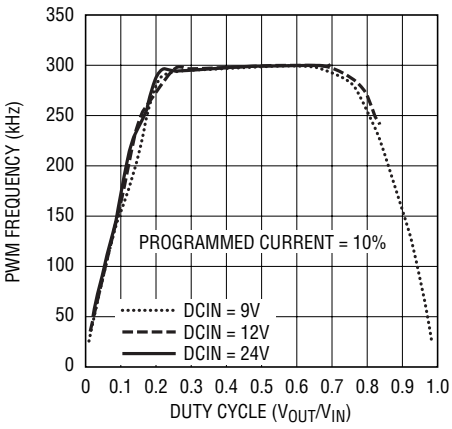
4101 G01

Output Voltage vs Output Current



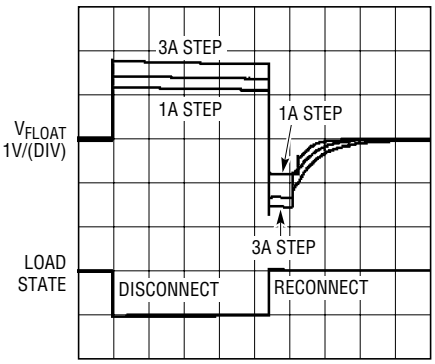
4101 G02

PWM Frequency vs Duty Cycle



4101 G03

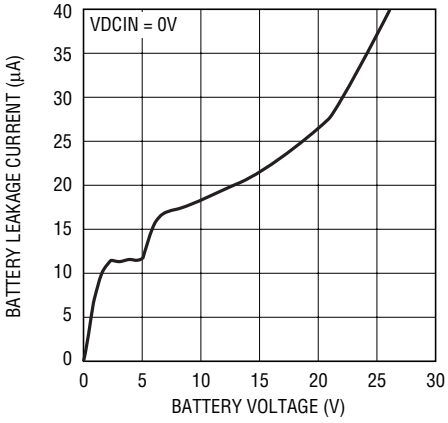
Disconnect/Reconnect Battery (Load Dump)



LOAD CURRENT = 1A, 2A, 3A
DCIN = 12V
V_{FLOAT} = 4.2V

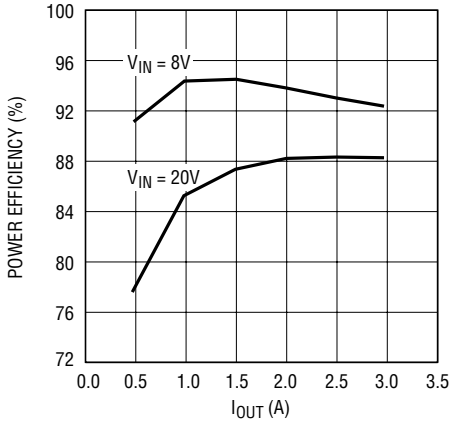
4101 G04

Battery Leakage Current vs Battery Voltage



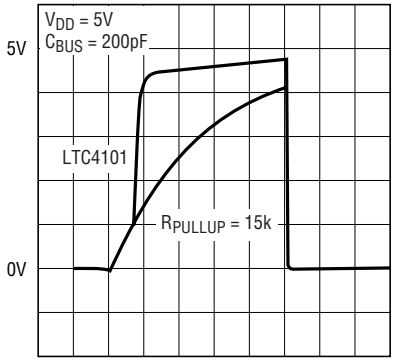
4101 G05

Efficiency at V_{PROG} = 4.208V



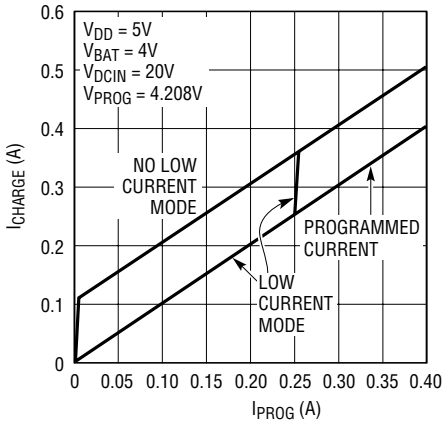
4101 G07

SMBus Accelerator Operation



4101 G09

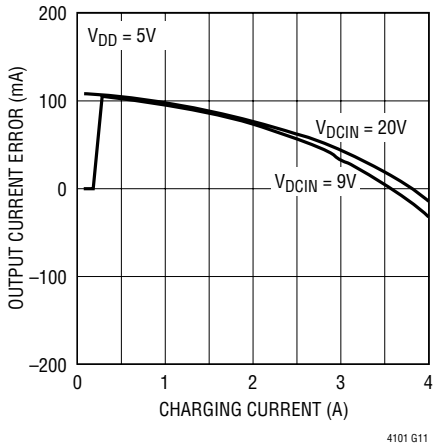
Low Current Operation



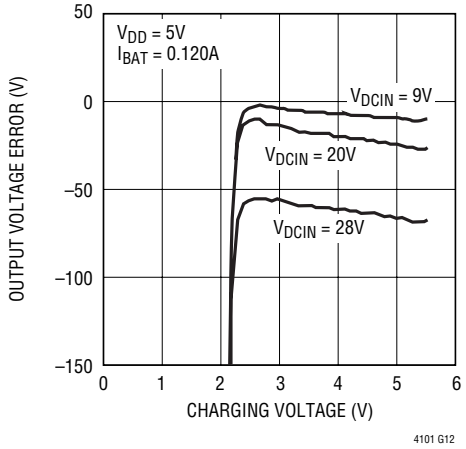
4101 G10

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Charging Current Error



Transfer Function of Charger



PIN FUNCTIONS

TGATE (Pin 1): Drives the Top External P-MOSFET of the Battery Charger Buck Converter.

PGND (Pin 2): High Current Ground Return for BGATE Driver.

BGATE (Pin 3): Drives the Bottom External N-MOSFET of the Battery Charger Buck Converter.

INFET (Pin 4): Drives the Gate of the External Input P-MOSFET.

DCIN (Pin 5): External DC Power Source Input. Bypass to ground with a 0.1µF capacitor.

CHGEN (Pin 6): Digital Bidirectional Pin to Enable Charger Function. This pin is connected as a wired AND bus.

The following events will cause the POWER_FAIL bit in the ChargerStatus register to become set:

1. An external device pulling the CHGEN signal to within 0.9V to GND;

2. The AC adapter voltage is not above the battery voltage.

$\overline{\text{SMBALERT}}$ (Pin 7): Active Low Interrupt Output to Host (referred to as the $\overline{\text{SMBALERT}}$ signal in the SMBus Revision 1.1 specification). Signals host that there has been a change of status in the charger registers and that the host should read the LTC4101 status registers to determine if any action on its part is required. This signal can be connected to the optional $\overline{\text{SMBALERT}}$ line of the SMBus. Open drain with weak current source pull-up to V_{DD} (with Schottky to allow it to be pulled to 5V externally).

SDA (Pin 8): SMBus Data Signal from Main (host-controlled) SMBus. External pull-up resistor is required.

SCL (Pin 9): SMBus Clock Signal from Main (host-controlled) SMBus. External pull-up resistor is required.

ACP (Pin 10): This Output Indicates the Value of the DCDIV Comparator. It can be used to indicate whether AC is present or not.

DCDIV (Pin 11): Supply Divider Input. This is a high impedance comparator input with a 1.2V threshold (rising edge) and hysteresis.

GND (Pin 12): Ground for Digital and Analog Circuitry.

I_{LIM} (Pin 13): An external resistor is connected between this pin and GND. The value of the external resistor programs the range and resolution of the programmed charger current.

V_{LIM} (Pin 14): An external resistor is connected between this pin and GND. The value of the external resistor programs the range and resolution of the charging voltage.

PIN FUNCTIONS

THB (Pin 15): SafetySignal Force/Sense Pin to Smart Battery. See description of operation for more detail. The maximum allowed combined capacitance on THA, THB and SafetySignal is 1nF (see Figure 4). A series resistor 54.9k needs to be connected between this pin and the battery's SafetySignal for this circuit to work correctly.

THA (Pin 16): SafetySignal Force/Sense Pin to Smart Battery. See description of operation for more detail. The maximum allowed combined capacitance on THA, THB and SafetySignal is 1nF (see Figure 4). A series resistor 1130Ω needs to be connected between this pin and the battery's SafetySignal for this circuit to work correctly.

V_{DD} (Pin 17): Power Supply Input for the LTC4101 Digital Circuitry. Bypass this pin with 0.1µF. Typically between 3.3V and $5V_{DC}$.

V_{SET} (Pin 18): Tap Point of the Programmable Resistor Divider, which Provides Battery Voltage Feedback to the Charger.

I_{TH} (Pin 19): Control Signal of the Inner Loop of the Current Mode PWM. Higher I_{TH} corresponds to higher charging current in normal operation. A 0.0015µF capacitor to GND filters out PWM ripple. Typical full-scale output current is 40µA. Nominal voltage range for this pin is 0V to 3V.

I_{DC} (Pin 20): Bypass to GND with a 0.068µF Capacitor.

CSP (Pin 21): Current Amplifier CA1 Input. This pin and the BAT pin measure the voltage across the sense resistor, R_{SENSE}, to provide the instantaneous current signals required for both peak and average current mode operation.

BAT (Pin 22): Battery Sense Input and the Negative Reference for the Current Sense Resistor. A bypass capacitor of at least 10µF is required.

CLN (Pin 23): Negative Input to the Input Current Limiting Circuit Block. If no current limit function is desired, connect this pin to CLP. The threshold is set at 100mV below the voltage at the CLP pin. When used to limit supply current, a filter is needed to filter out the switching noise.

CLP (Pin 24): Positive Input to the Input Current Limiting Circuit Block. This pin also serves as a power supply for the IC.

BLOCK DIAGRAM

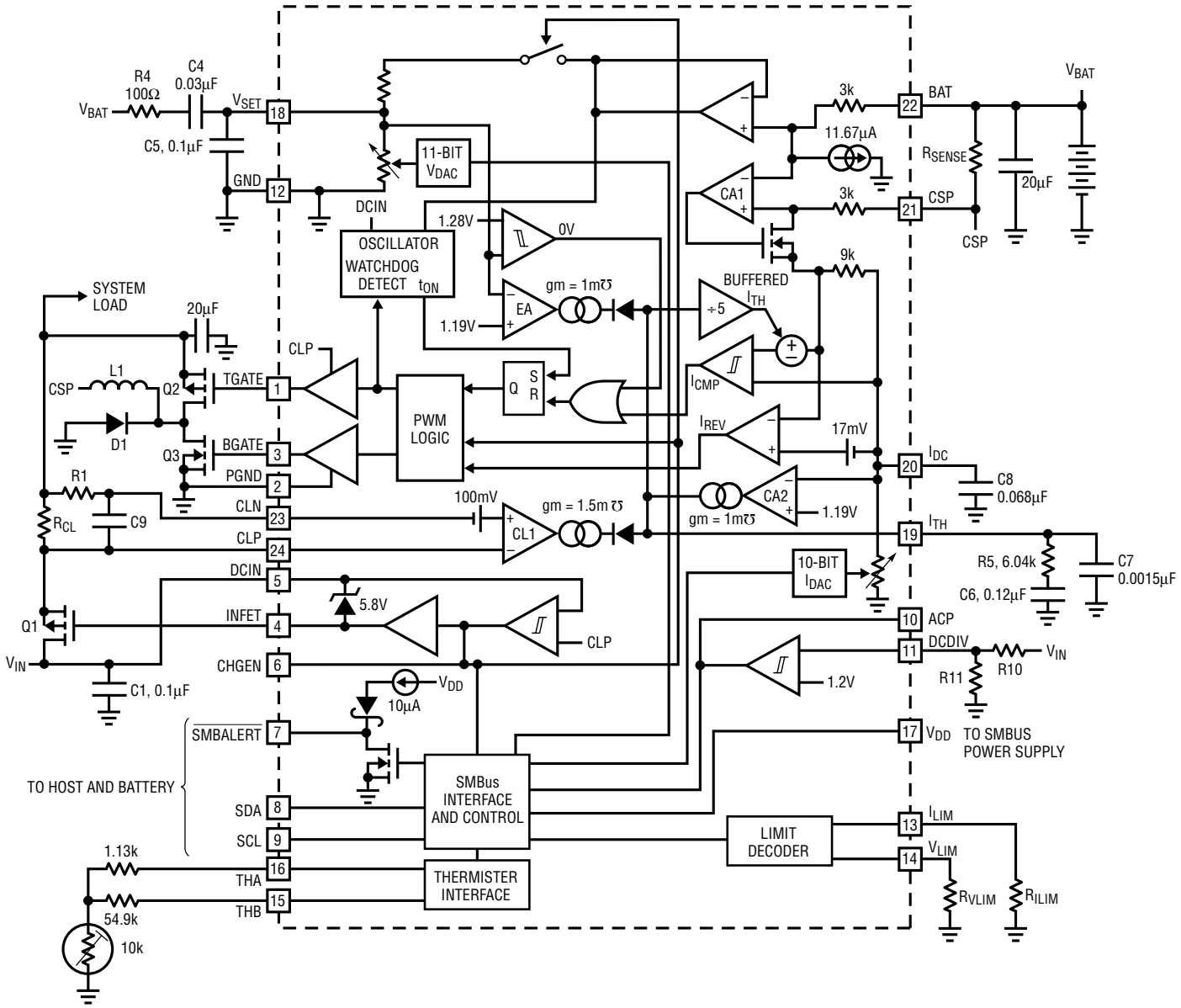
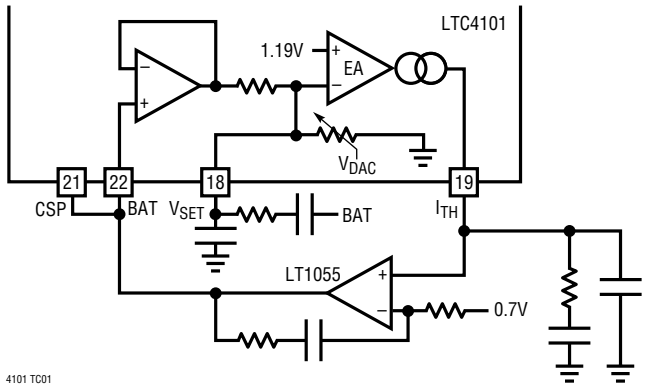


Figure 2.

TEST CIRCUIT



$$V_{TOL} = \frac{V_{BAT} - V_{VDAC}}{V_{VDAC}} \bullet 100$$

FOR $V_{VDAC} = 4.176V (0x1050)$

DCIN = 21V

CLN = CLP = 20V

$V_{DD} = 3.3V$

OPERATION

Overview (Refer to Block Diagram)

The LTC4101 is composed of a battery charger section, a charger controller, a 10-bit DAC to control charger current, an 11-bit DAC to control charger voltage, a SafetySignal decoder, limit decoder and an SMBus controller block. If no battery is present, the SafetySignal decoder indicates a RES_OR condition and charging is disabled by the charger controller (CHGEN = Low). Charging will also be disabled if DCDIV is low, or the SafetySignal is decoded as RES_HOT. If a battery is inserted and AC power is connected, the battery will be charged with an 80mA "wake-up" current. The wake-up current is discontinued after $t_{TIMEOUT}$ if the SafetySignal is decoded as RES_UR or RES_COLD, and the battery or host doesn't transmit charging commands.

The SMBus interface and control block receives ChargingCurrent() and ChargingVoltage() commands via the SMBus. If ChargingCurrent() and ChargingVoltage() command pairs are received within a $t_{TIMEOUT}$ interval, the values are stored in the current and voltage DACs and the charger controller asserts the CHGEN line if the decoded SafetySignal value will allow charging to commence. ChargingCurrent() and ChargingVoltage() values are compared against limits programmed by the limit decoder block; if the commands exceed the programmed limits these limits are substituted and overrange flags are set.

The charger controller will assert $\overline{\text{SMBALERT}}$ whenever a status change is detected, namely: AC_PRESENT, BATTERY_PRESENT, ALARM_INHIBITED, or V_{DD} power-fail. The host may query the charger, via the SMBus, to obtain ChargerStatus() information. $\overline{\text{SMBALERT}}$ will be deasserted upon a successful read of ChargerStatus() or a successful Alert Response Address (ARA) request.

Battery Charger Controller

The LTC4101 charger controller uses a constant off-time, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the SR latch and turned off when the main current comparator I_{CMP} resets the SR latch. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current trips the current comparator I_{REV}, or the beginning of the next cycle. The oscillator uses the equation,

$$t_{OFF} = \frac{(V_{DCIN} - V_{BAT})}{(V_{DCIN} \bullet f_{OSC})}$$

OPERATION

to set the bottom MOSFET on time. The result is quasi-constant frequency operation: the converter frequency remains nearly constant over a wide range of output voltages. This activity is diagrammed in Figure 3.

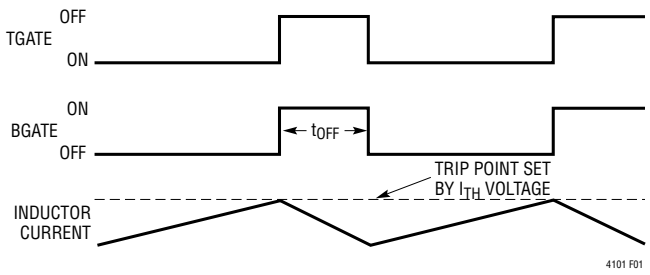


Figure 3.

The peak inductor current, at which I_{CMP} resets the SR latch, is controlled by the voltage on I_{TH}. I_{TH} is in turn controlled by several loops, depending upon the situation at hand. The average current control loop converts the voltage between CSP and BAT to a representative current. Error amp CA2 compares this current against the desired current programmed by the I_{DAC} at the I_{DC} pin and adjusts I_{TH} for the desired voltage across R_{SENSE}.

The voltage at BAT is divided down by an internal resistor divider set by the V_{DAC} and is used by error amp EA to decrease I_{TH} if the divider voltage is above the 1.19V reference.

The amplifier CL1 monitors and limits the input current, normally from the AC adapter, to a preset level (100mV/R_{CL}). At input current limit, CL1 will decrease the I_{TH} voltage to reduce charging current.

An overvoltage comparator, OV, guards against transient overshoots (>7%). In this case, the top MOSFET is turned off until the overvoltage condition is cleared. This feature is useful for batteries that "load dump" themselves by opening their protection switch to perform functions such as calibration or pulse mode charging.

PWM Watchdog Timer

There is a watchdog timer that observes the activity on the TGATE pin. If TGATE stops switching for more than 40µs, the watchdog activates and turns off the top MOSFET for about 400ns. The watchdog engages to prevent very low frequency operation in dropout – a potential source of audible noise when using ceramic input and output capacitors.

Charger Start-Up

When the charger is enabled, it will not begin switching until the I_{TH} voltage exceeds a threshold that assures initial current will be positive. This threshold is 5% to 15% of the maximum programmed current. After the charger begins switching, the various loops will control the current at a level that is higher or lower than the initial current. The duration of this transient condition depends upon the loop compensation, but is typically less than 1ms.

SMBus Interface

All communications over the SMBus are interpreted by the SMBus interface block. The SMBus interface is a SMBus slave device. All internal LTC4101 registers may be updated and accessed through the SMBus interface, and charger controller as required. The SMBus protocol is a derivative of the I²C™ bus (Reference *"I²C-Bus and How to Use It, V1.0"* by Philips, and "System Management Bus Specification," Version 1.1, from the SBS Implementers Forum, for a complete description of the bus protocol requirements.)

All data is clocked into the shift register on the rising edge of SCL. All data is clocked out of the shift register on the falling edge of SCL. Detection of an SMBus Stop condition, or power-on reset via the V_{DD} power-fail, will reset the SMBus interface to an initial state at any time.

The LTC4101 command set is interpreted by the SMBus interface and passed onto the charger controller block as control signals or updates to internal registers.

Description of Supported Battery Charger Functions

The functions are described as follows (see Table 1 also):

FunctionName() 'hnn (command code)

Description: A brief description of the function.

Purpose: The purpose of the function, and an example where appropriate.

- **SMBus Protocol:** Refer to Section 5 of the Smart Battery Charger specification for more details.

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*http://www. SBS-FORUM.org

OPERATION

Input, Output or Input/Output: A description of the data supplied to or returned by the function.

ChargerSpecInfo() ('h11)

Description: The SMBus Host uses this command to read the LTC4101's extended status bits.

Purpose: Allows the System Host to determine the specification revision the charger supports as well as other extended status information.

- **SMBus Protocol:** Read Word.

Output: The CHARGER_SPEC indicates that the LTC4101 supports Version 1.1 of the Smart Battery Charger Specification. The SELECTOR_SUPPORT indicates that the LTC4101 does not support the optional Smart Battery Selector Commands.

ChargerMode() ('h12)

Description: The SMBus Host uses this command to set the various charger modes. The default values are set to allow a Smart Battery and the LTC4101 to work in concert without requiring an SMBus Host.

Purpose: Allows the SMBus Host to configure the charger and change the default modes. This is a write only function, but the value of the "mode" bit, INHIBIT_CHARGE may be determined using the ChargerStatus() function.

- **SMBus Protocol:** Write Word.

Input: The INHIBIT_CHARGE bit allows charging to be inhibited without changing the ChargingCurrent() and ChargingVoltage() values. The charging may be resumed by clearing this bit. This bit is automatically cleared when power is reapplied or when a battery is reinserted.

The ENABLE_POLLING bit is not supported by the LTC4101. Values written to this bit are ignored.

The POR_RESET bit sets the LTC4101 to its power-on default condition.

The RESET_TO_ZERO bit sets the ChargingCurrent()and ChargingVoltage() values to zero. This function ALWAYS clears the ChargingVoltage() and ChargingCurrent() values to zero even if the INHIBIT_CHARGE bit is set.

ChargerStatus() ('h13)

Description: The SMBus Host uses this command to read the LTC4101's status bits.

Purpose: Allows the SMBus Host to determine the status and level of the LTC4101.

- **SMBus Protocol:** Read Word.

Output: The CHARGE_INHIBITED bit reflects the status of the LTC4101 set by the INHIBIT_CHARGE bit in the ChargerMode() function.

The POLLING_ENABLED, VOLTAGE_NOTREG, and CURRENT_NOTREG are not supported by the LTC4101.

The LTC4101 always reports itself as a Level 2 Smart Battery Charger.

CURRENT_OR bit is set only when ChargingCurrent() is set to a value outside the current regulation range of the LTC4101. This bit may be used in conjunction with the INHIBIT_CHARGE bit of the ChargerMode() and ChargingCurrent() to determine the current capability of the LTC4101. When ChargingCurrent() is set to the programmatic maximum current + 1, the CURRENT_OR bit will be set.

VOLTAGE_OR bit is set only when ChargingVoltage() is set to a value outside the voltage regulation range of the LTC4101. This bit may be used in conjunction with the INHIBIT_CHARGE bit of the ChargerMode() and ChargingVoltage() to determine the voltage capability of the LTC4101. When ChargingVoltage() is set to the programmatic maximum voltage, the VOLTAGE_OR bit will be set.

The RES_OR bit is set only when the SafetySignal resistance value is greater than 95kΩ. This indicates that the SafetySignal is to be considered as an open circuit.

The RES_COLD bit is set only when the SafetySignal resistance value is greater than 28.5kΩ. The SafetySignal indicates a cold battery. The RES_COLD bit will be set whenever the RES_OR bit is set.

The RES_HOT bit is set only when the SafetySignal resistance is less than 3150Ω, which indicates a hot battery. The RES_HOT bit will be set whenever the RES_UR bit is set.

OPERATION

Table 1: Summary of Supported Charger Functions

Function	Access	SMBus Address	Command Code	Data Type	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ChargerSpecInfo()		7'b0001_001	8'h11	Info	Reserved											SELECTOR_SUPPORT	CHARGER_SPEC			
	Read			Return Values	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
ChargerMode()		7'b0001_001	8'h12	Control	Reserved												RESET_TO_ZERO	POR_RESET	ENABLE_POLLING	INHIBIT_CHARGE
	Write			Permitted Values	Ignored												1/0	1/0	Ign	1/0
ChargerStatus()		7'b0001_001	8'h13	Status	AC_PRESENT	BATTERY_PRESENT	POWER_FAIL	ALARM_INHIBITED	RES_UR	RES_HOT	RES_COLD	RES_OR	VOLTAGE_OR	CURRENT_OR	LEVEL:3/LEVEL:2		CURRENT_NOTREG	VOLTAGE_NOTREG	POLLING_ENABLED	CHARGE_INHIBITED
	Read			Return Values	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	0	1	0	0	0	1/0
ChargingCurrent()		7'b0001_001	8'h14	Value	CHARGING_CURRENT[15:0]															
	Write			Permitted Values	Unsigned integer representing current in mA															
ChargingVoltage()		7'b0001_001	8'h15	Value	CHARGING_VOLTAGE[15:0]															
	Write			Permitted Values	Unsigned integer representing voltage in mV															
AlarmWarning()		7'b0001_001	8'h16	Control	OVER_CHARGED_ALARM	TERMINATE_CHARGE_ALARM	RESERVED_ALARM	OVER_TEMP_ALARM	TERMINATE_DISCHARGE_ALARM	Reserved	REMAINING_CAPACITY_ALARM	REMAINING_TIME_ALARM	INITIALIZED	DISCHARGING	FULLY_CHARGED	FULLY DISCHARGED	ERROR			
	Write			Permitted Values	1/0	1/0	1/0	1/0	Ignored											
LTC0() □□		7'b0001_001	8'h3C	Register	Reserved			NO_LOWI	LTC4101's Version Identification											
	Write			Permitted Values	Ignored			1/0	Ignored											
	Read			Return Values	0	1	0	1/0	0	0	0	0	0	1	0	0	0	0	0	0
Alert Response Address		7'b0001_100	N/A	Status	Not Supported								LTC4101's Address							Undefined
	Read Byte			Return Values									0	0	0	1	0	0	1	X

OPERATION

The RES_UR bit is set only when the SafetySignal resistance value is less than 575Ω.

ALARM_INHIBITED bit is set if a valid AlarmWarning() message has been received and charging is inhibited as a result. This bit is cleared if both ChargingVoltage() and ChargingCurrent() are rewritten to the LTC4101, power is removed (DCDIV < V_{ACP}), or if a battery is removed. The setting of the ALARM_INHIBITED will activate the LTC4101 SMBALERT pull-down.

POWER_FAIL bit is set if the LTC4101 does not have sufficient DCIN voltage to charge the battery or if an external device is pulling the CHGEN input signal low. Charging is disabled whenever this bit is set. The setting of this bit does not clear the values in the ChargingVoltage() and ChargingCurrent() function values, nor does it necessarily affect the charging modes of the LTC4101.

BATTERY_PRESENT is set if a battery is present otherwise it is cleared. The LTC4101 uses the SafetySignal in order to determine battery presence. If the LTC4101 detects a RES_OR condition, the BATTERY_PRESENT bit is cleared immediately. The LTC4101 will not set the BATTERY_PRESENT bit until it successfully samples the SafetySignal twice and does not detect a RES_OR condition on either sampling. If AC is not present (e.g. DCDIV < V_{ACP}), this bit may not be set for up to one-half second after the battery is connected to the SafetySignal. The ChargingCurrent() and ChargingVoltage() function values are immediately cleared whenever this bit is cleared. Charging will never be allowed if this bit is cleared. A change in BATTERY_PRESENT will activate the LTC4101 SMBALERT pull-down.

AC_PRESENT is set if the voltage on DCDIV is greater than V_{ACP}. This does not necessarily indicate that the voltage on DCIN is sufficient to charge the battery. A change in AC_PRESENT will activate the LTC4101 SMBALERT pull-down.

ChargingCurrent() ('h14)

Description: The Battery, System Host or other master device sends the desired charging current (mA) to the LTC4101.

Purpose: The LTC4101 uses R_{ILIM}, the granularity of the I_{DAC}, and the value of the ChargingCurrent() function to determine its charging current supplied to the battery. The charging current will never exceed the maximum current permitted by R_{ILIM}. The ChargingCurrent() value will be truncated to the granularity of the I_{DAC}. The charging current will also be reduced if the battery voltage exceeds the programmed charging voltage.

- **SMBus Protocol:** Write Word.

Input: The CHARGING_CURRENT is an unsigned 16 bit integer specifying the requested charging current in mA. The following table defines the maximum permissible value of CHARGING_CURRENT that will not set the CURRENT_OR in the ChargerStatus() function for a given value of the R_{ILIM}:

R_{ILIM}	ChargingCurrent()	Current
Short to GND	0x0000 through 0x03FF	0mA through 1023mA
10kΩ ±1%	0x0000 through 0x07FF	0mA through 2047mA
33kΩ ±1%	0x0000 through 0x0BFF	0mA through 3071mA
Open (or short to V_{DD})	0x0000 through 0x0FFF	0mA through 4095mA

ChargingVoltage() ('h15)

Description: The Battery, SMBus Host or other master device sends the desired charging voltage (mV) to the LTC4101.

Purpose: The LTC4101 uses R_{VLIM}, the granularity of the V_{DAC}, and the value of the ChargingVoltage() function to determine its charging voltage supplied to the battery. The charging voltage will never be forced beyond the voltage permitted by R_{VLIM}. The ChargingVoltage() value will be truncated to the granularity of the V_{DAC}. The charging voltage will also be reduced if the battery current exceeds the programmed charging current.

- **SMBus Protocol:** Write Word.

Input: The CHARGING_VOLTAGE is an unsigned 16-bit integer specifying the requested charging voltage in mV. The LTC4101 considers any value from 0x0001 through 0x044F the same as writing 0x0000. The following

OPERATION

table defines the maximum permissible value of CHARGING_VOLTAGE that will not set the VOLTAGE_OR in the ChargerStatus() function for a given value of R_{VLIM}:

R_{VLIM}	Maximum ChargingVoltage()
Short to GND	0x1090 (4240mV)
10kΩ ± 1%	0x10D0 (4304mV)
33kΩ ± 1%	0x1150 (4432mV)
100kΩ ± 1%	0x11A0 (4512mV)
Open (or short to V_{DD})	0x1580 (5504mV)

AlarmWarning() ('h16)

Description: The Smart Battery, acting as a bus master device, sends the AlarmWarning() message to the LTC4101 to notify it that one or more alarm conditions exist. Alarm indications are encoded as bit fields in the Battery's Status register, which is then sent to the LTC4101 by this function.

Purpose: The LTC4101 will use the information sent by this function to properly charge the battery. The LTC4101 will only respond to certain alarm bits. Writing to this function does not necessarily cause an alarm condition that inhibits battery charging.

- **SMBus Protocol:** Write Word.

Input: Only the OVER_CHARGED_ALARM, TERMINATE_CHARGE_ALARM, reserved (0x2000), and OVER_TEMP_ALARM bits are supported by the LTC4101. Writing a one to any of these specified bits will inhibit the charging by the LTC4101 and will set the ALARM_INHIBITED bit in the ChargerStatus() function. The TERMINATE_DISCHARGE_ALARM, REMAINING_CAPACITY_ALARM, REMAINING_TIME_ALARM, and the ERROR bits are ignored by the LTC4101.

LTC0() ('h3C)

Description: The SMBus Host uses this command to determine the version number of the LTC4101 and set extended operation modes not defined by the Smart Battery Charger Specification.

Purpose: This function allows the SMBus Host to determine if the battery charger is an LTC4101. Identifying the manufacturer and version of the Smart Battery Charger permits software to perform tasks specific to a given charger. The LTC4101 also provides a means of disabling the LOWI current mode of the I_{DAC}.

- **SMBus Protocol:** Write Word.

Input: The NO_LOWI is the only bit recognized by this function. The default value of NO_LOWI is zero. The LTC4101 LOWI current mode provides a more accurate average charge current when the charge current is less than 1/16 of the full scale I_{DAC} value. When the NO_LOWI is set, a less accurate I_{DAC} algorithm is used to generate the charging current, but because the charger is not pulsed on and off, it may be preferred.

- **SMBus Protocol:** Read Word.

Output: The NO_LOWI indicates the I_{DAC} mode of operation. If clear, then the LOWI current mode will be used when the charging current is less than 1/16 of the full-scale I_{DAC} value.

The LTC Version Identification will always be 0x4040 for the LTC4101.

Alert Response Address (ARA)

Description: The SMBus system host uses the Alert Response Address to quickly identify the generator of an SMBALERT# event.

Purpose: The LTC4101 will respond to an ARA if the $\overline{\text{SMBALERT}}$ signal is actively pulling down the SMBALERT# bus. The LTC4101 will follow the prioritization reporting as defined in the System Management Bus Specification, Version 1.1, from the SBS Implementers Forum.

- **SMBus Protocol:** A 7-bit Addressable Device Responds to an ARA.

Output: The Device Address will be sent to the SMBus system host. The LTC4101 Device address is 0x12 (or 0x09 if just looking at the 7-bit address field).

The following events will cause the LTC4101 to pull-down the SMBALERT# bus through the $\overline{\text{SMBALERT}}$ pin:

- Change of AC_PRESENT in the ChargerStatus() function.
- Change of BATTERY_PRESENT in the ChargerStatus() function.
- Setting ALARM_INHIBITED in the ChargerStatus() function.
- Internal power-on reset condition.

OPERATION

SMBus Accelerator Pull-Ups

Both SCL and SDA have SMBus accelerator circuits which reduce the rise time on systems with significant capacitance on the two SMBus signals. The dynamic pull-up circuitry detects a rising edge on SDA or SCL and applies 1mA to 10mA pull-up to V_{DD} when $V_{IN} > 0.8V$ until $V_{IN} < V_{DD} – 0.8V$ (external pull-up resistors are still required to supply DC current). This action allows the bus to meet SMBus rise time requirements with as much as 250pF on each SMBus signal. The improved rise time will benefit all of the devices which use the SMBus, especially those devices that use the I^2C logic levels. Note that the dynamic pull-up circuits only pull to V_{DD}, so some SMBus devices that are not compliant to the SMBus specifications may still have rise time compliance problems if the SMBus pull-up resistors are terminated with voltages higher than V_{DD}.

The Control Block

The LTC4101 charger operations are handled by the control block. This block is capable of charging the selected battery autonomously or under SMBus Host control. The control block can request communications with the system management host (SMBus Host) by asserting SMBALERT = 0; this will cause the SMBus Host, if present, to poll the LTC4101.

The control block receives SMBus slave commands from the SMBus interface block.

The control block allows the LTC4101 to meet the following Smart Battery-controlled (Level 2) charger requirements:

1. Implements the Smart Battery's critical warning messages over the SMBus.
2. Operates as an SMBus slave device that responds to ChargingVoltage() and ChargingCurrent() commands and adjusts the charger output parameters accordingly.
3. The host may control charging by disabling the Smart Battery's ability to transmit ChargingCurrent() and ChargingVoltage() request functions and broadcasting the charging commands to the LTC4101 over the SMBus.
4. The LTC4101 will still respond to Smart Battery critical warning messages without host intervention.

Wake-up Charging Mode

The following conditions must be met in order to allow wake-up charging of the battery:

1. The SafetySignal must be RES_COLD, RES_IDEAL, or RES_UR.
2. AC must be present. This is qualified by DCDIV > V_{ACP}.

Wake-up charging initiates when a newly inserted battery does not send ChargingCurrent() and ChargingVoltage() functions to the LTC4101.

The following conditions will terminate the Wake-up Charging Mode.

1. A $T_{TIMEOUT}$ period is reached when the SafetySignal is RES_COLD or RES_UR.
2. The SafetySignal is registering RES_OR.
3. The successful writing of the ChargingCurrent() AND ChargingVoltage() function. The LTC4101 will proceed to the controlled charging mode after these two functions are written.
4. The SafetySignal is registering RES_HOT.
5. The AC power is no longer present. (DCDIV < V_{ACP})
6. The ALARM_INHIBITED becomes set in the ChargerStatus() function.
7. The INHIBIT_CHARGE is set in the ChargerMode() function.
8. The CHGEN pin is pulled low by an external device. The LTC4101 will resume wake-up charging, if the CHGEN pin is released by the external device. Toggling the CHGEN pin will not reset the $T_{TIMEOUT}$ timer.
9. There is insufficient DCIN voltage to charge the battery. The LTC4101 will resume wake-up charging when there is sufficient DCIN voltage to charge the battery. This condition will not reset the $T_{TIMEOUT}$ timer.

OPERATION

Controlled Charging Algorithm Overview

The following conditions must be met in order to allow controlled charging to start on the LTC4101:

1. The ChargingVoltage() AND ChargingCurrent() function must be written to non-zero values.
2. The SafetySignal must be RES_COLD, RES_IDEAL, or RES_UR.
3. AC must be present. This is qualified by DCDIV > V_{ACP}.

The following conditions will stop the Controlled Charging Algorithm and will cause the Battery Charger Controller to stop charging:

1. The ChargingCurrent() AND ChargingVoltage() functions have not been written for $T_{TIMEOUT}$.
2. The SafetySignal is registering RES_OR.
3. The SafetySignal is registering RES_HOT.
4. The AC power is no longer present. (DCDIV < V_{ACP})
5. ALARM_INHIBITED is set in the ChargerStatus() function.
6. INHIBIT_CHARGE is set in the ChargerMode() function. Clearing INHIBIT_CHARGE will cause the LTC4101 to resume charging using the previous ChargingVoltage() AND ChargingCurrent() function values.
7. RESET_TO_ZERO is set in the ChargerMode() function.
8. CHGEN pin is pulled low by an external device. The LTC4101 will resume charging using the previous ChargingVoltage() AND ChargingCurrent() function values, if the CHGEN pin is released by the external device.
9. Insufficient DCIN voltage to charge the battery. The LTC4101 will resume charging using the previous ChargingVoltage() AND ChargingCurrent() function values, when there is sufficient DCIN voltage to charge the battery.
10. Writing a zero value to ChargingVoltage() function.
11. Writing a zero value to ChargingCurrent() function.

The SafetySignal Decoder Block

This block measures the resistance of the SafetySignal and features high noise immunity at critical trip points. The low power standby mode supports only battery presence SMB charger reporting requirements when AC is not present. The SafetySignal decoder is shown in Figure 4. The value of R_{THA} is 1.13k and R_{THB} is 54.9k.

SafetySignal sensing is accomplished by a state machine that reconfigures the switches of Figure 4 using THA_SELB and THB_SELB, a selectable reference generator, and two comparators. This circuit has two modes of operation based upon whether AC is present.

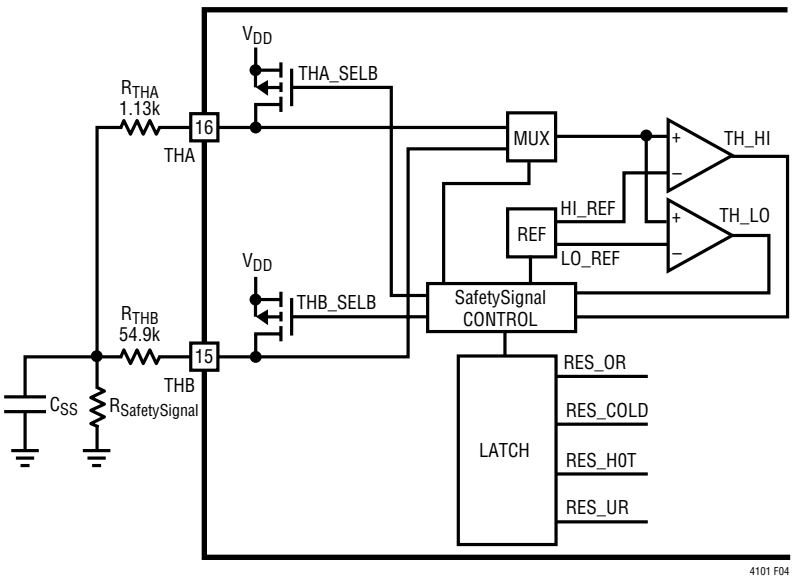


Figure 4. SafetySignal Decoder Block

OPERATION

When AC is present, the LTC4101 samples the value of the SafetySignal and updates the ChargerStatus register approximately every 32ms. The state machine successively samples the SafetySignal value starting with the RES_OR ≥ RES_COLD threshold, then RES_COLD ≥ RES_IDEAL threshold, RES_IDEAL ≥ RES_HOT threshold, and finally the RES_HOT ≥ RES_UR threshold. Once the SafetySignal range is determined, the lower value thresholds are not sampled. The SafetySignal decoder block uses the previously determined SafetySignal value to provide the appropriate adjustment in threshold to add hysteresis. The R_{THB} resistor value is used to measure the RES_OR ≥ RES_COLD and RES_COLD ≥ RES_IDEAL thresholds by connecting the THB pin to V_{DD} and measuring the voltage resultant on the THA pin. The R_{THA} resistor value is used to measure the RES_IDEAL ≥ RES_HOT and RES_HOT ≥ RES_UR thresholds by connecting the THA pin to V_{DD} and measuring the voltage resultant on the THB pin.

The SafetySignal decoder block uses a voltage divider network between V_{DD} and GND to determine SafetySignal range thresholds. Since the THA and THB inputs are sequentially connected to V_{DD}, this provides V_{DD} noise immunity during SafetySignal measurement.

When AC power is not available the SafetySignal block supports the following low power operating features:

1. The SafetySignal is sampled every 250ms or less, instead of 32ms.
2. A full SafetySignal status is sampled every 30s or less, instead of every 32ms.

The SafetySignal impedance is interpreted according to Table 4.

Table 4. SafetySignal State Ranges

SafetySignal RESISTANCE	CHARGE STATUS BITS	DESCRIPTION
0Ω to 500Ω	RES_UR, RES_HOT BATTERY_PRESENT	Underrange
500Ω to 3kΩ	RES_HOT BATTERY_PRESENT	Hot
3kΩ to 30kΩ	BATTERY_PRESENT	Ideal
30kΩ to 100kΩ	RES_COLD BATTERY_PRESENT	Cold
Above 100kΩ	RES_OR RES_COLD	Overrange

Note: The underrange detection scheme is a very important feature of the LTC4101. The $R_{THA}/R_{SafetySignal}$ divider trip point of 0.333 • V_{DD} (1V) is well above the 0.047 • V_{DD} (140mV) threshold of a system using a 10k pull-up. A system using a 10k pull-up would not be able to resolve the important underrange to hot transition point with a modest 100mV of ground offset between battery and SafetySignal detection circuitry. Such offsets are anticipated when charging at normal current levels.

The required values for R_{THA} and R_{THB} are shown in Table 5.

Table 5. SafetySignal External Resistor Values

EXTERNAL RESISTOR	VALUE (Ω)
R_{THA}	1130 ±1%
R_{THB}	54.9k ±1%

C_{SS} represents the capacitance between the SafetySignal and GND. C_{SS} may be added to provide additional noise immunity from transients in the application. C_{SS} cannot exceed 1nF if the LTC4101 is to properly sense the value of $R_{SafetySignal}$.

OPERATION

The I_{LIM} Decoder Block

The value of an external resistor connected from this pin to GND determines one of four current limits that are used for maximum charging current value. These limits provide a measure of safety with a hardware restriction on charging current which cannot be overridden by software.

Table 6. I_{LIM} Trip Points and Ranges

EXTERNAL RESISTOR (R_{ILIM})	I_{LIM} VOLTAGE	CONTROLLED CHARGING CURRENT RANGE	GRANULARITY
Short to GND	$V_{ILIM} < 0.09V_{DD}$	0 < I < 1023mA	1mA
10k ±1%	$0.17V_{VDD} < V_{ILIM} < 0.34V_{VDD}$	0 < I < 2046mA	2mA
33k ±1%	$0.42V_{VDD} < V_{ILIM} < 0.59V$	0 < I < 3068mA	4mA
Open (>250k, or Short to V_{DD})	$0.66V_{VDD} < V_{ILIM}$	0 < I < 4092mA	4mA

The V_{LIM} Decoder Block

The value of an external resistor connected from this pin to GND determines one of five voltage limits that are applied to the charger output value. These limits provide a measure of safety with a hardware restriction on charging voltage which cannot be overridden by software.

Table 7. V_{LIM} Trip Points and Ranges (See Figure 5)

EXTERNAL RESISTOR (R_{VLIM})	V_{LIM} VOLTAGE	CONTROLLED CHARGING VOLTAGE (V_{OUT}) RANGE	GRANULARITY
Short to GND	$V_{VLIM} < 0.09V_{VCCP}$	2900mV < V_{OUT} < 4240mV	16mV
10k ±1%	$0.17V_{VDD} < V_{VLIM} < 0.34V_{VDD}$	2900mV < V_{OUT} < 4304mV	16mV
33k ±1%	$0.42V_{VCCP} < V_{VLIM} < 0.59V_{VDD}$	2900mV < V_{OUT} < 4432mV	16mV
100k ±1%	$0.66V_{VDD} < V_{VLIM} < 0.84V_{VDD}$	2900mV < V_{OUT} < 4512mV	16mV
Open or Tied to V_{DD}	$0.91V_{VDD} < V_{VLIM}$	2900mV < V_{OUT} < 5504mV	16mV

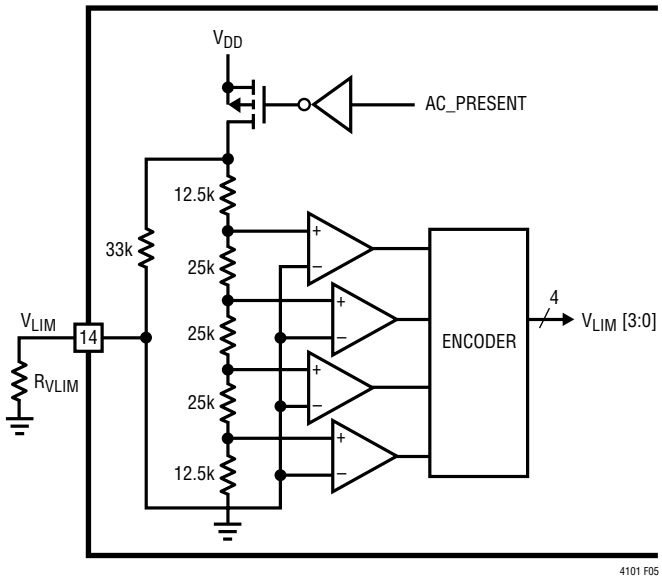
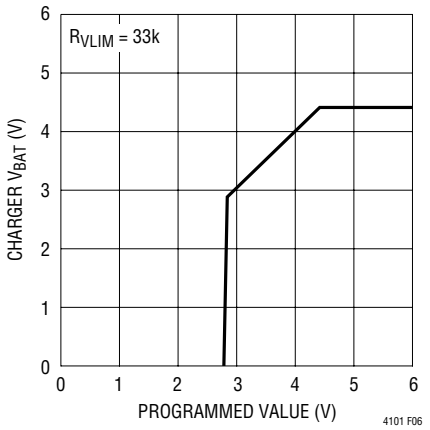


Figure 5. Simplified V_{LIM} Circuit Concept (I_{LIM} is Similar)

OPERATION

The Voltage DAC Block

Note that the charger output voltage is offset by V_{REF}. Therefore, the value of V_{REF} is subtracted from the SMBus ChargingVoltage() value in order for the output voltage to be programmed properly (without offset). If the ChargingVoltage() value is below the nominal reference voltage of the charger, nominally 1.104V, the charger output voltage is programmed to zero. In addition, if the ChargingVoltage() value is above the limit set by the V_{LIM} pin, then the charger output voltage is set to the value determined by the V_{LIM} resistor and the VOLTAGE_OR bit is set. These limits are demonstrated in Figure 6.



NOTE: THE LTC4101 CAN BE PROGRAMMED WITH ChargingVoltage() FUNCTION VALUES BETWEEN 1.104V AND 2.9V, HOWEVER, THE BATTERY CHARGER CONTROLLER OUTPUT VOLTAGE MAY BE ZERO WITH PROGRAMMED VALUES BELOW 2.9V.

Figure 6. Transfer Function of Charger

The Current DAC Block

The current DAC is a delta-sigma modulator which controls the effective value of an external resistor, R_{SET}, used to set the current limit of the charger. Figure 7 is a simplified diagram of the DAC operation. The delta-sigma modulator and switch convert the ChargingCurrent() value, received via the SMBus, to a variable resistance equal to:

$$1.25R_{SET}/[ChargingCurrent()/I_{LIM[X]}] = R_{IDC}$$

Therefore, programmed current is equal to:

$$I_{CHARGE} = (102.3mV/R_{SENSE})\ (ChargingCurrent()/I_{LIM[X]}),$$
for ChargingCurrent() < $I_{LIM[X]}$.

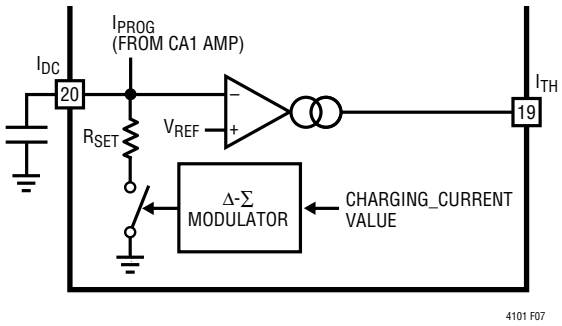


Figure 7. Current DAC Operation

When a value less than 1/16th of the maximum current allowed by I_{LIM} is applied to the current DAC input, the current DAC enters a different mode of operation called LOWI. The current DAC output is pulse width modulated with a high frequency clock having a duty cycle value of 1/8. Therefore, the maximum output current provided by the charger is $I_{MAX}/8$. The delta-sigma output gates this low duty cycle signal on and off. The delta-sigma shift registers are then clocked at a slower rate, about 45ms/bit, so that the charger has time to settle to the $I_{MAX}/8$ value. The resulting average charging current is equal to that requested by the ChargingCurrent() value.

Note: The LOWI mode can be disabled by setting the NO_LOWI bit in the LTC0() function.

When wake-up is asserted to the current DAC block, the delta-sigma is then fixed at a value equal to 80mA, independent of the I_{LIM} setting.

Input FET

The input FET circuit performs two functions. It enables the charger if the input voltage is higher than the CLP pin, and provides an indication of this condition at both the CHGEN pin and the PWR_FAIL bit in the ChargerStatus() register. It also controls the gate of the input FET to keep a low forward voltage drop when charging and prevents reverse current flow through the input FET.

If the input voltage is less than V_{CLP}, it must go at least 130mV higher than V_{CLP} to activate the charger. The CHGEN pin is forced low unless this condition is met. The gate of the input FET is driven to a voltage sufficient to keep a low forward voltage drop from drain to source. If the voltage between DCIN and CLP drops to less than 25mV,

OPERATION

the input FET is turned off slowly. If the voltage between DCIN and CLP is ever less than –25mV, then the input FET is turned off quickly to prevent significant reverse current from flowing in the input FET. In this condition the CHGEN pin is driven low and the charger is disabled.

The AC Present Block (AC_PRESENT)

The DCDIV pin is used to determine AC presence. If the DCDIV voltage is above the DCDIV comparator threshold (V_{ACP}), then the ACP output pin will be switched to V_{DD} and the AC_PRESENT bit in the ChargerStatus() function will be set. If the DCDIV voltage is below the DCDIV comparator threshold minus the DCDIV comparator hysteresis, then the ACP output pin is switched to GND and the AC_PRESENT bit in the ChargerStatus() function is cleared. The ACP output pin is designed to drive 2mA continuously.

Adapter Limiting

An important feature of the LTC4101 is the ability to automatically adjust charging current to a level which avoids overloading the wall adapter. This allows the product to operate at the same time that batteries are being charged without complex load management algorithms. Additionally, batteries will automatically be charged at the maximum possible rate of which the adapter is capable.

This feature is created by sensing total adapter output current and adjusting charging current downward if a preset adapter current limit is exceeded. True analog control is used, with closed loop feedback ensuring that adapter load current remains within limits. Amplifier CL1 in Figure 9 senses the voltage across R_{CL}, connected between the CLP and CLN pins. When this voltage exceeds 100mV, the amplifier will override programmed charging current to limit adapter current to $100mV/R_{CL}$. A lowpass filter formed by 4.99k and 0.1µF is required to eliminate switching noise. If the current limit is not used, CLP should be connected to CLP, but leave CLN connected to power.

Setting Input Current Limit

To set the input current limit, you need to know the minimum wall adapter current rating. Subtract 7% for the input current limit tolerance and use that current to determine the resistor value.

$R_{CL} = 100mV/I_{LIM}$

I_{LIM} = Adapter Min Current –
(Adapter Min Current • 7%)

As is often the case, the wall adapter will usually have at least a +10% current limit margin and many times one can simply set the adapter current limit value to the actual adapter rating (see Figure 9).

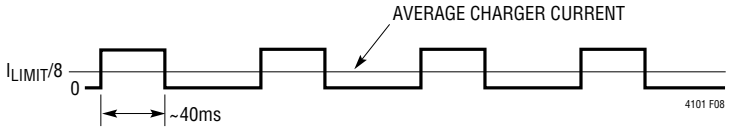


Figure 8. Charging Current Waveform in Low Current Mode

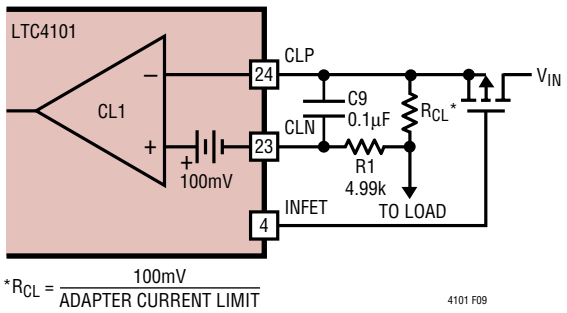


Figure 9. Adapter Current Limiting

APPLICATIONS INFORMATION

Charge Termination Issues

Batteries with constant current charging and voltage-based charger termination might experience problems with reductions of charger current caused by adapter limiting. It is recommended that input limiting feature be defeated in such cases. Consult the battery manufacturer for information on how your battery terminates charging.

Setting Output Current Limit (Refer to Figure 1)

The LTC4101 current DAC and the PWM analog circuitry must coordinate the setting of the charger current. Failure to do so will result in incorrect charge currents.

Table 9. Recommended Resistor Values

I_{MAX} (A)	R_{SENSE} (Ω) 1%	R_{SENSE} (W)	R_{ILIM} (Ω) 1%
1.023	0.100	0.25	0
2.046	0.05	0.25	10k
3.068	0.025	0.5	33k
4.092	0.025	0.5	Open

Warning

DO NOT CHANGE THE VALUE OF R_{ILIM} DURING OPERATION. The value must remain fixed and track the R_{SENSE} value at all times. Changing the current setting can result in currents that greatly exceed the requested value and potentially damage the battery or overload the wall adapter if no input current limiting is provided.

Inductor Selection

Higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition, the effect of inductor value on ripple current and low current operation must also be considered. The inductor ripple current ΔI_L decreases with higher frequency and increases with higher V_{IN}.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Table 8. Common R_{CL} Resistor Values

Adapter Rating (A)	–7% Adapter Rating (A)	R_{CL} Value* (Ω)1%	R_{CL} Limit (A)	R_{CL}Power Dissipation (W)	R_{CL} Power Rating(W)
1.5	1.40	0.068	1.47	0.15	0.25
1.8	1.67	0.062	1.61	0.16	0.25
2.0	1.86	0.051	1.96	0.20	0.25
2.3	2.14	0.047	2.13	0.21	0.25
2.5	2.33	0.043	2.33	0.23	0.50
2.7	2.51	0.039	2.56	0.26	0.50
3.0	2.79	0.036	2.79	0.28	0.50
3.3	3.07	0.033	3.07	0.31	0.50
3.6	3.35	0.030	3.35	0.33	0.50
4.0	3.72	0.027	3.72	0.37	0.50

* Rounded to nearest 5% standard step value. Many non standard values are popular.

APPLICATIONS INFORMATION

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{MAX})$. Remember the maximum ΔI_L occurs at the maximum input voltage. The inductor value also has an effect on low current operation. The transition to low current operation begins when the inductor current reaches zero while the bottom MOSFET is on. Lower inductor values (higher ΔI_L) will cause this to occur at higher load currents, which can cause a dip in efficiency in the upper range of low current operation.

Table 10. Recommended Inductor Values

Inductance	I_{MAX} (A)		
V_{IN} Range (V)	1	2	3* annd 4
≤ 7.5	16µH ± 20%	8µH ± 20%	4µH ± 20%
≤ 9.0	20µH ± 20%	10µH ± 20%	5µH ± 20%
≤ 12.0	24µH ± 20%	12µH ± 20%	6µH ± 20%
≤ 15.0	26µH ± 20%	13µH ± 20%	6.5µH ± 20%
≤ 28.0	30µH ± 20%	15µH ± 20%	7.5µH ± 20%
R_{SENSE}	0.1Ω	0.05Ω	0.025Ω

* 3 Amp uses the same R_{SENSE} that 4 amps uses. Thus the inductance can be the same.

Choose and inductor who's inductance value is equal to or greater than the value shown. Values assume:
1.–32% RSS result from –20% inductance tolerance and a –25% inductance loss at I_{MAX}.
2.Inductor ripple current ratio of 0.51 of I_{OUT} across R_{SENSE}.
3. V_{OUT} is at 4.2V

Charger Switching Power MOSFET and Diode Selection

Two external power MOSFETs must be selected for use with the charger: a P-channel MOSFET for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak gate drive levels are set internally. This voltage is typically 6V. Consequently, logic-level threshold MOSFETs must be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, total gate capacitance Q_G, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. The charger is operating in continuous mode so the duty cycles for the top and bottom MOSFETs are given by:

Main Switch Duty Cycle = V_{OUT}/V_{IN}

Synchronous Switch Duty Cycle = $(V_{IN} – V_{OUT})/V_{IN}$.

The MOSFET power dissipations at maximum output current are given by:

$$PMAIN = V_{OUT}/V_{IN}(I_{MAX})^2(1 + \delta\Delta T)R_{DS(ON)} + k(V_{IN})^2(I_{MAX})(C_{RSS})(f_{OSC})$$

$$PSYNC = (V_{IN} – V_{OUT})/V_{IN}(I_{MAX})^2(1 + \delta\Delta T)R_{DS(ON)}$$

Where $\delta\Delta T$ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current. Both MOSFETs have I^2R losses while the PMAIN equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short circuit when the duty cycle in this switch in nearly 100%. The term $(1 + \delta\Delta T)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs. $C_{RSS} = Q_{GD}/\Delta V_{DS}$ is usually specified in the MOSFET characteristics. The constant k = 2 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

If the charger is to operate in low dropout mode or with a high duty cycle less than 50%, then the bottomside N-Channel efficiency generally improves with a larger MOSFET. Using asymmetrical MOSFETs may achieve cost savings or efficiency gains.

Both of the LTC4101 MOSFET drivers are optimized to take advantage of MOSFETs Q_G values of less than 22nC and a TD-off delay specification of around 60ns or less. Larger FETs may work, but you must qualify them and monitor LTC4101 temperature rise.

APPLICATIONS INFORMATION

Using excessively large MOSFETs relative to the I_{MAX} charge current they are working with will actually reduce efficiency at lighter current levels with very limited gain at high currents. A good place to start looking for a suitable MOSFET in a datasheet is to look for a part with an I_D rating a little over 2 times the I_{MAX} charge current rating. For the LTC4101, the P-channel FET can typically be scaled down a bit to take advantage of the lower duty cycle limits. However make sure you never exceed the P_D rating of the device.

The Schottky diode D1, shown in the Typical Application on the back page, conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. A 1A Schottky is generally a good size for 4A regulators due to the relatively small average current. Larger diodes can result in additional transition losses due to their larger junction capacitance.

The diode may be omitted if the efficiency loss can be tolerated.

Calculating IC Power Dissipation

The power dissipation of the LTC4101 is dependent upon the gate charge of the top and bottom MOSFETs (Q2 & Q3 respectively) The gate charge (QG) is determined from the manufacturer's data sheet and is dependent upon both the gate voltage swing and the drain voltage swing of the MOSFET. Use 6V for the gate voltage swing and V_{DCIN} for the drain voltage swing.

$$P_D = V_{DCIN} \bullet (f_{OSC} (QG_{Q2} + QG_{Q3}) + I_{DCIN}) + V_{DD} \bullet I_{DD}$$

Example: V_{DCIN} = 12V, f_{OSC} = 345kHz, QG_{Q2} = 25nC, QG_{Q3} = 15nC, I_{DCIN} = 5mA, V_{DD} = 5.5V, I_{DD} = 1mA.

P_D = 231mW

Soft-Start and Undervoltage Lockout

The LTC4101 is soft-started by the 0.12µF capacitor on the I_{TH} pin. On start-up, I_{TH} pin voltage will rise quickly to 0.5V, then ramp up at a rate set by the internal 30µA pull-up current and the external capacitor. Battery charging current starts ramping up when I_{TH} voltage reaches 0.8V and full current is achieved with I_{TH} at 2V. With a 0.12µF capacitor, time to reach full charge current is about 2ms and it is assumed that input voltage to the charger will reach full value in less than 2ms. The capacitor can be increased up to 1µF if longer input start-up times are needed.

In any switching regulator, conventional timer-based soft-starting can be defeated if the input voltage rises much slower than the time out period. This happens because the switching regulators in the battery charger and the computer power supply are typically supplying a fixed amount of power to the load. If input voltage comes up slowly compared to the soft-start time, the regulators will try to deliver full power to the load when the input voltage is still well below its final value. If the adapter is current limited, it cannot deliver full power at reduced output voltages and the possibility exists for a quasi "latch" state where the adapter output stays in a current limited state at reduced output voltage. For instance, if maximum charger plus computer load power is 30W, a 15V adapter might be current limited at 2.5A. If adapter voltage is less than (30W/2.5A = 12V) when full power is drawn, the adapter voltage will be pulled down by the constant 30W load until it reaches a lower stable state where the switching regulators can no longer supply full load. This situation can be prevented by utilizing the DCDIV resistor divider, set higher than the minimum adapter voltage where full power can be achieved.

APPLICATIONS INFORMATION

Input and Output Capacitors

In the 4A Lithium Battery Charger (Typical Application on back page), the input capacitor (C2) is assumed to absorb all input switching ripple current in the converter, so it must have adequate ripple current rating. Worst-case RMS ripple current will be equal to one half of output charging current. Actual capacitance value is not critical. Solid tantalum low ESR capacitors have high ripple current rating in a relatively small surface mount package, *but caution must be used when tantalum capacitors are used for input or output bypass*. High input surge currents can be created when the adapter is hot-plugged to the charger or when a battery is connected to the charger. Solid tantalum capacitors have a known failure mechanism when subjected to very high turn-on surge currents. Only Kemet T495 series of "Surge Robust" low ESR tantalums are rated for high surge conditions such as battery to ground.

The relatively high ESR of an aluminum electrolytic for C1, located at the AC adapter input terminal, is helpful in reducing ringing during the hot-plug event. Refer to AN88 for more information.

The highest possible voltage rating on the capacitor will minimize problems. Consult with the manufacturer before use. Alternatives include new high capacity ceramic (at least 20µF) from Tokin, United Chemi-Con/Marcon, et al. Other alternative capacitors include OSCON capacitors from Sanyo.

The output capacitor (C3) is also assumed to absorb output switching current ripple. The general formula for capacitor current is:

$$I_{RMS} = \frac{0.29(V_{BAT})\left(1-\frac{V_{BAT}}{V_{DCIN}}\right)}{(L1)(f)}$$

For example, V_{DCIN} = 12V, V_{BAT} = 4.2V, L1 = 10µH, and f = 300kHz, I_{RMS} = 0.26A.

EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the300kHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance. If the ESR of C3 is 0.2Ω and the battery impedance is raised to 4Ω with a bead or inductor, only 5% of the current ripple will flow in the battery.

Protecting SMBus Inputs

The SMBus inputs, SCL and SDA, are exposed to uncontrolled transient signals whenever a battery is connected to the system. If the battery contains a static charge, the SMBus inputs are subjected to transients which can cause damage after repeated exposure. Also, if the battery's positive terminal makes contact to the connector before the negative terminal, the SMBus inputs can be forced below ground with the full battery potential, causing a potential for latch-up in any of the devices connected to the SMBus inputs. Therefore it is good design practice to protect the SMBus inputs as shown in Figure 10.

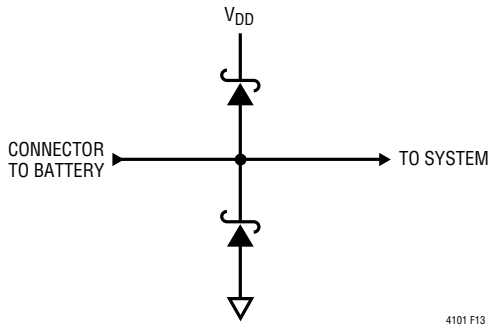


Figure 10. Recommended SMBus Transient Protection

APPLICATIONS INFORMATION

PCB Layout Considerations

For maximum efficiency, the switch node rise and fall times should be minimized. To prevent magnetic and electrical field radiation and high frequency resonant problems, proper layout of the components connected to the IC is essential. (See Figure 11.) Here is a PCB layout priority list for proper layout. Layout the PCB using this specific order.

1. Input capacitors need to be placed as close as possible to switching FET's supply and ground connections. Shortest copper trace connections possible. These parts must be on the same layer of copper. Vias must not be used to make this connection.
2. The control IC needs to be close to the switching FET's gate terminals. Keep the gate drive signals short for a clean FET drive. This includes IC supply pins that connect to the switching FET source pins. The IC can be placed on the opposite side of the PCB relative to above.
3. Place inductor input as close as possible to switching FET's output connection. Minimize the surface area of this trace. Make the trace width the minimum amount needed to support current—no copper fills or pours. Avoid running the connection using multiple layers in parallel. Minimize capacitance from this node to any other trace or plane.
4. Place the output current sense resistor right next to the inductor output but oriented such that the IC's current sense feedback traces going to resistor are not long. The feedback traces need to be routed together as a single pair on the same layer at any given time with smallest trace spacing possible. Locate any filter component on these traces next to the IC and not at the sense resistor location.
5. Place output capacitors next to the sense resistor output and ground.
6. Output capacitor ground connections need to feed into same copper that connects to the input capacitor ground before tying back into system ground.

Interfacing with a Selector

The LTC4101 is designed to be used with a true analog multiplexer for the SafetySignal sensing path. Some selector ICs from various manufacturers may not implement this. Consult LTC applications department for more information.

Electronic Loads

The LTC4101 is designed to work with a real battery. Electronic loads will create instability within the LTC4101 preventing accurate programming currents and voltages. Consult LTC applications department for more information.

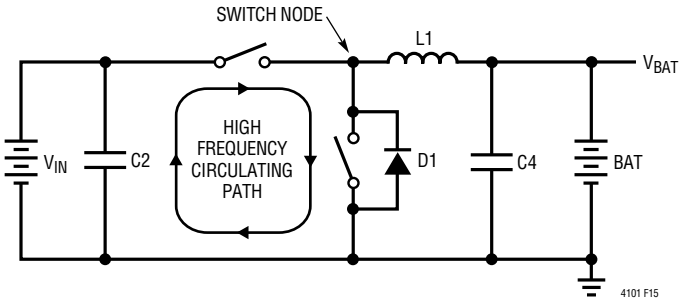


Figure 11. High Speed Switching Path

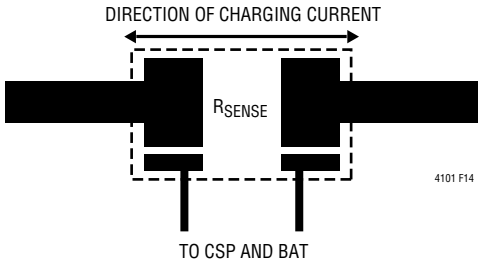
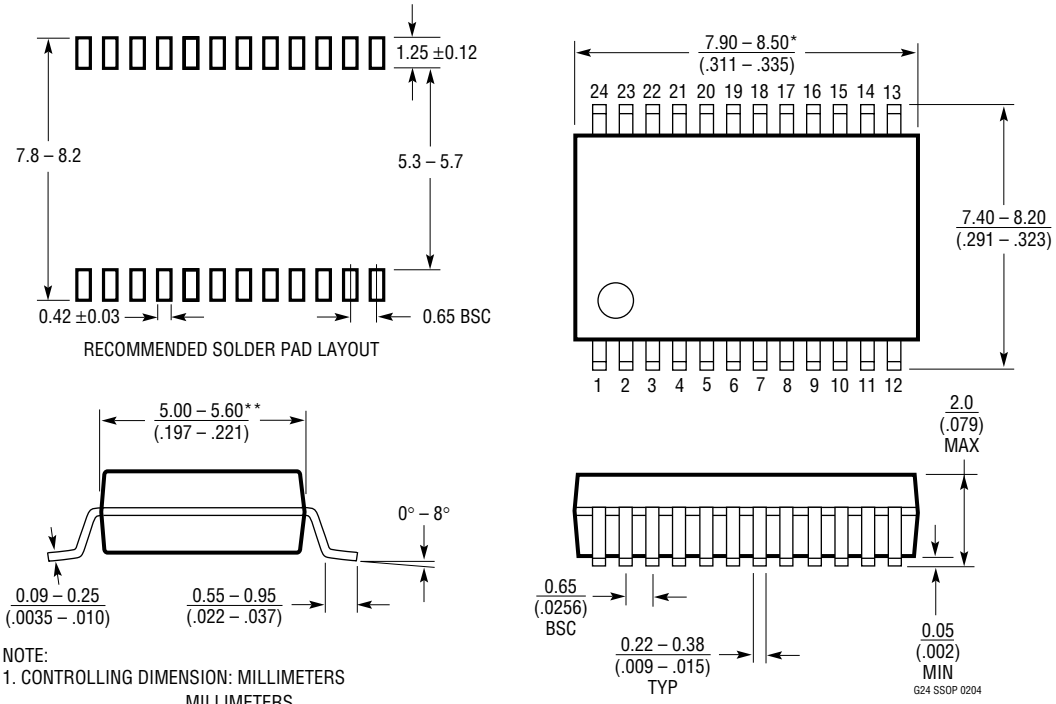


Figure 12. Kelvin Sensing of Charging Current

PACKAGE DESCRIPTION

G Package
24-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



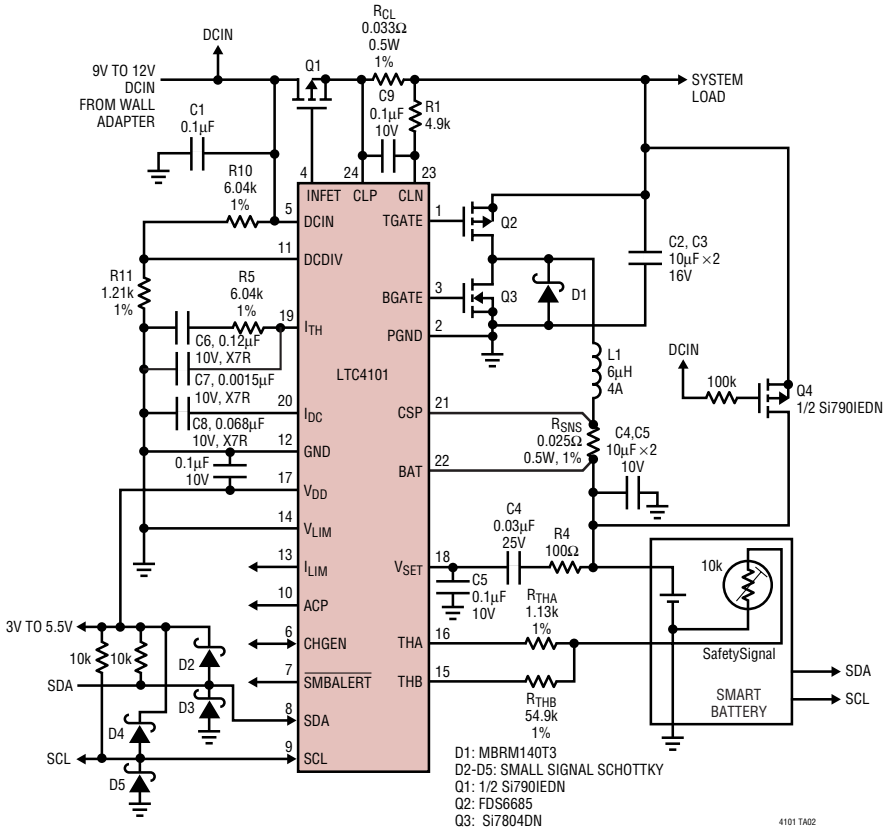
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

TYPICAL APPLICATION

LTC4101 Li-Ion Battery Charger I_{LIM} = 4A/V_{LIM} = 4.240V, Adapter Rating = 2.7A



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1760	Smart Battery System Manager	Autonomous Power Management and Battery Charging for Two Smart Batteries, SMBus Rev 1.1 Compliant
LTC4006	Small, High Efficiency, Fixed Voltage, Lithium-Ion Battery Charger	Constant Current/Constant Voltage Switching Regulator with Termination Timer, AC Adapter Current Limit and SafetySignal Sensor in a Small 16-Pin Package
LTC4007	High Efficiency, Programmable Voltage Battery Charger with Termination	Complete Charger for 3- or 4-Cell Li-Ion Batteries, AC Adapter Current Limit, SafetySignal Sensor and Indicator Outputs
LTC4008	High Efficiency, Programmable Voltage/Current Battery Charger	Constant Current/Constant Voltage Switching Regulator; Resistor Voltage/ Current Programming, AC Adapter Current Limit and SafetySignal Sensor
LTC4010	High Efficiency Standalone Nickel Battery Charger	Complete NiMH/NiCd Charger in a 16-Pin TSSOP Package, Constant-Current Switching Regulator
LTC4011	High Efficiency Standalone Nickel Battery Charger	Complete NiMH/NiCd Charger in a 20-Pin TSSOP Package, PowerPath™ Control. Constant-Current Switching Regulator
LTC4060	Standalone Linear NiMH/NiCd Fast Charger	Complete NiMH/NiCd Charger in a Small Leaded or Leadless 16-Pin Package, No Sense Resistor or Blocking Diode Required
LTC4100	Smart Battery Charger Controller	For Smart Batteries with Voltages Above 5.5V
LTC4412	Low Loss PowerPath Controller	Very Low Loss Replacement for Power Supply OR'ing Diodes Using Minimal External Components

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