

# M62281P/FP

## General Purpose Current Mode PWM Control IC

REJ03D0840-0201  
Rev.2.01  
Nov 14, 2007

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### Description

M62281P/FP is designed as a high speed current mode PWM control IC.

This small 10 pin package contains many functions and protection circuits allowing simpler peripheral circuit and compact set design.

This IC can operate high speed switching (700 kHz Max.) with high speed current sense comparator and current limiting circuit.

### Features

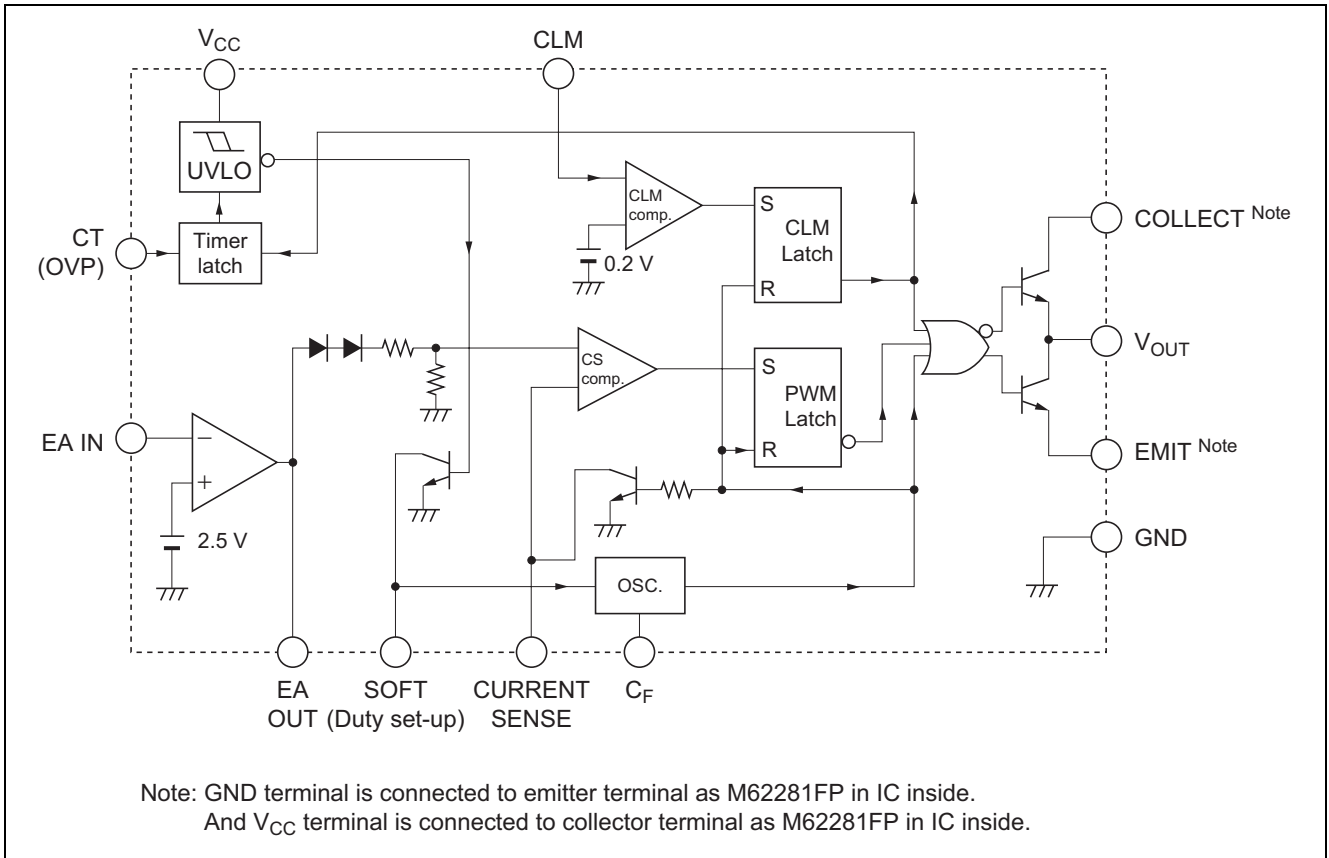
- 700 kHz applicable to MOS-FET
  - Output current  $I_o(\text{peak}) = \pm 1 \text{ A}$
  - Totem-pole output
- CURRENT SENSE terminal separate from CLM terminal makes SMPS strong in noise.
- High speed pulse-by-pulse current limiting
- Timer type latch protection circuit with OVP (external reset is possible)
- Soft start operation is possible (with dead time control)
- Built-in OP Amp for feedback control (photo coupler can be driven)
- Small start-up current 180  $\mu\text{A}$
- Start-up voltage 12.5 V, Stop voltage 8.3 V

### Application

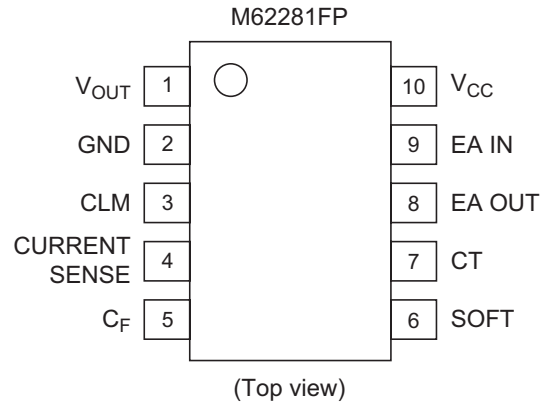
Switching Regulator

DC/DC converter

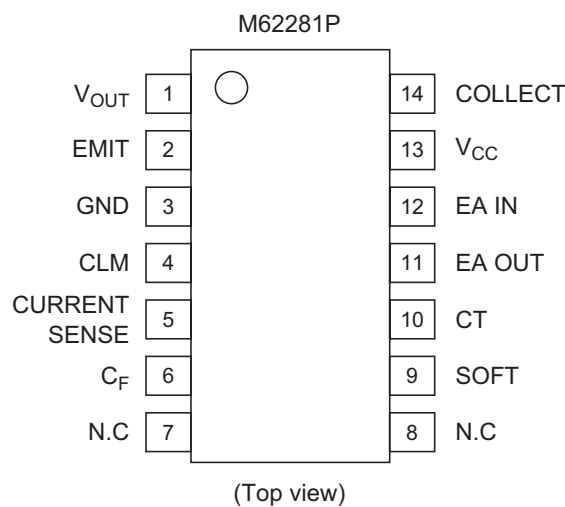
Block Diagram



## Pin Arrangement



Outline: PRSP0010DB-A (10P2N-A)



Outline: PRDP0014AA-A (14P4)

## Absolute Maximum Ratings

(T<sub>a</sub> = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V <sub>CC</sub>	36	V	
Output terminal current	I <sub>OUT</sub>	150	mA	Continuous
		1.0	A	Peak
CT terminal supply voltage	V <sub>CT</sub>	36	V	
EA IN terminal supply voltage	V <sub>EA IN</sub>	10	V	
CLM terminal supply voltage	V <sub>CLM</sub>	-0.3 to +4.0	V	
CURRENT SENSE terminal supply voltage	V <sub>CS</sub>	-0.3 to +5.8	V	
Power dissipation	P <sub>d</sub>	1500	mW	P
		440		FP
Thermal derating	K <sub>θ</sub>	12	mW/°C	T <sub>a</sub> ≥ 25°C
		3.52		FP
Operating temperature	T <sub>opr</sub>	-20 to +85	°C	
Storage temperature	T <sub>stg</sub>	-40 to +150	°C	

## Electrical Characteristics

(Ta = 25°C, V<sub>CC</sub> = 14 V, unless otherwise noted)

Block	Item	Symbol	Limits			Unit	Test Conditions
			Min.	Typ.	Max.		
All device	Supply voltage range	V <sub>CC</sub>	V <sub>CC(STOP)</sub>	—	35	V	
	Operation start-up voltage	V <sub>CC(START)</sub>	11.5	12.5	13.5	V	
	Operation stop voltage	V <sub>CC(STOP)</sub>	7.6	8.3	9.0	V	
	Start-up and stop Voltage difference	ΔV <sub>CC</sub>	3.5	4.2	5.1	V	
	Stand-by current	I <sub>CCL</sub>	90	180	270	μA	V <sub>CC</sub> = V <sub>CC(START)</sub> – 0.5 V
	Operating current	I <sub>CCO</sub>	7.5	13	19	mA	
	Timer latch circuit current	I <sub>CCOFF</sub>	0.9	2.0	3.0	mA	V <sub>CC</sub> = 14 V
0.8			1.8	2.7	mA	V <sub>CC</sub> = V <sub>CC(STOP)</sub> + 0.2 V	
CT	CT term. "H" threshold voltage	V <sub>THCTH</sub>	3.5	4.0	4.5	V	
	CT term. "L" threshold voltage	V <sub>THCTL</sub>	0.4	0.7	1.0	V	
	CT term. discharge current	I <sub>CTDCHG</sub>	70	110	165	μA	In normal operation
	CT term. charge current	I <sub>CTCHG</sub>	–33	–14	–5	μA	In CLM actuating
Error Amp	Reference voltage	V <sub>B</sub>	2.4	2.5	2.6	V	
	Input bias current	I <sub>B</sub>	–300	–100	0	nA	
	Open loop gain	A <sub>v</sub>	—	70	—	dB	
	Unity gain bandwidth	f <sub>r</sub>	—	1	—	MHz	
	Output source current	I <sub>OS</sub>	–460	–370	–240	μA	V <sub>EAIN</sub> = 0 V
	Output voltage (High)	V <sub>Om+</sub>	5.3	5.8	6.25	V	
	Output voltage (Low)	V <sub>Om-</sub>	0	0.2	0.35	V	
Current sense	CS term. input voltage gain	A <sub>vCS</sub>	—	3.0	—	V/V	
	Input bias current	I <sub>B</sub>	–5	–1	—	μA	
	CS term. delay time	T <sub>PDCS</sub>	—	150	—	ns	Delay time to output
CLM	CLM term. threshold voltage	V <sub>THCLM</sub>	180	200	220	mV	
	CLM term. output current	I <sub>OUTCLM</sub>	–270	–200	–140	μA	V <sub>CLM</sub> = 0 V
	CLM term. delay time	T <sub>PDCLM</sub>	—	100	—	ns	Delay time to output
SOFT	Input voltage range at 0% duty	V <sub>SOFT(0%)</sub>	0	—	1.0	V	Soft term. voltage range to set 0% duty
	Input voltage at 50% duty	V <sub>SOFT(50%)</sub>	—	2.7	—	V	Soft term. voltage at 50% duty
	Maximum duty	Duty Max	83	90	97	%	
	Soft term. input current	I <sub>SOFT</sub>	–50	–43	–36		
OSC	Maximum oscillation frequency	f <sub>OSCMAX</sub>	—	—	700	kHz	
	Oscillation frequency	f <sub>OSC</sub>	130	180	230	kHz	C <sub>F</sub> = 270 pF
	Oscillation upper limit voltage	V <sub>OSCH</sub>	3.2	3.6	4.0	V	C <sub>F</sub> = 270 pF
	Oscillation lower limit voltage	V <sub>OSCL</sub>	1.2	1.4	1.6	V	C <sub>F</sub> = 270 pF
	Oscillation voltage	ΔV <sub>OSC</sub>	1.9	2.2	2.5	V	C <sub>F</sub> = 270 pF

(Ta = 25°C, V<sub>CC</sub> = 14 V, unless otherwise noted)

Block	Item	Symbol	Limits			Unit	Test Conditions
			Min.	Typ.	Max.		
Output	Output low voltage	V <sub>OL1</sub>	—	0.04	0.4	V	V <sub>CC</sub> = 14 V, I <sub>O</sub> = 10 mA
		V <sub>OL2</sub>	—	0.3	1.4	V	V <sub>CC</sub> = 14 V, I <sub>O</sub> = 100 mA
	Output high voltage	V <sub>OH1</sub>	12.0	12.7	—	V	V <sub>CC</sub> = 14 V, I <sub>O</sub> = -10 mA
		V <sub>OH2</sub>	11.5	12.5	—	V	V <sub>CC</sub> = 14 V, I <sub>O</sub> = -100 mA
	Output voltage rise time	T <sub>RISE</sub>	—	50	—	ns	No load
	Output voltage fall time	T <sub>FALL</sub>	—	35	—	ns	No load

## Function Description and Application

### EA IN, EA OUT Terminal

Circuit for EA OUT terminal is connected to constant current load (370 μA Typ.) shown in figure 1. Output voltage of error amp. is controlled by the output transistor to provide current-sense comp. with the controlled voltage.

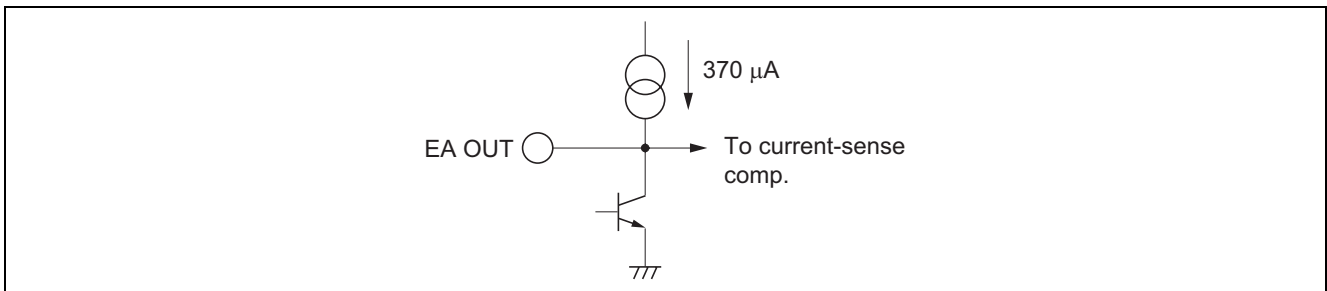


Figure 1 Circuit Diagram of EA OUT Terminal

#### 1. Peripheral circuit of Error Amp

Detected voltage divided by R1 and R2 is input to EA IN terminal in such case as fly-back system where V<sub>CC</sub> line voltage is proportional to output voltage, or in the case that the voltage detection is made on the primary side. In this case operating region is set by R1 and R2, and AC gain by R1//R2, R<sub>F</sub>.

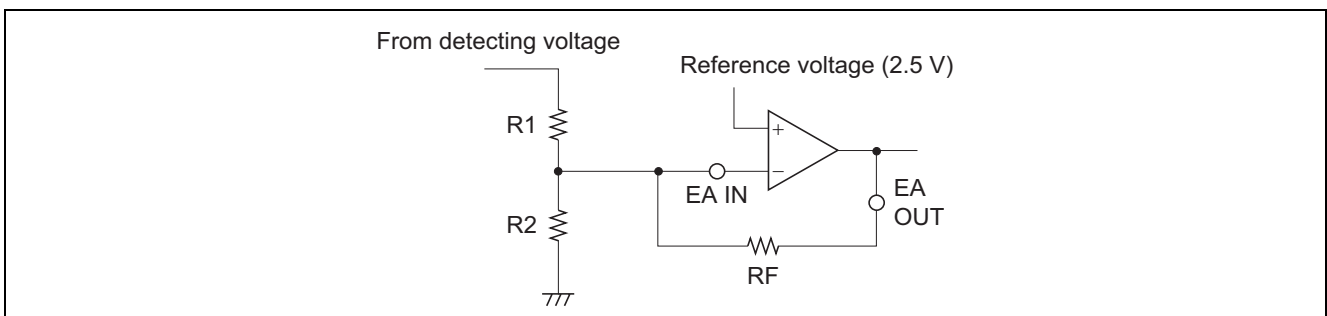
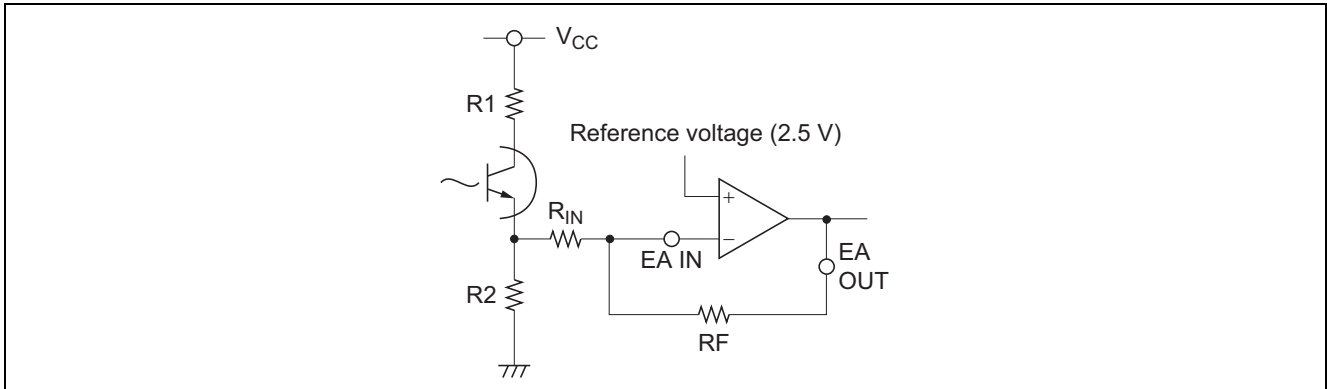


Figure 2 Method to Detect The Voltage on The Primary Side

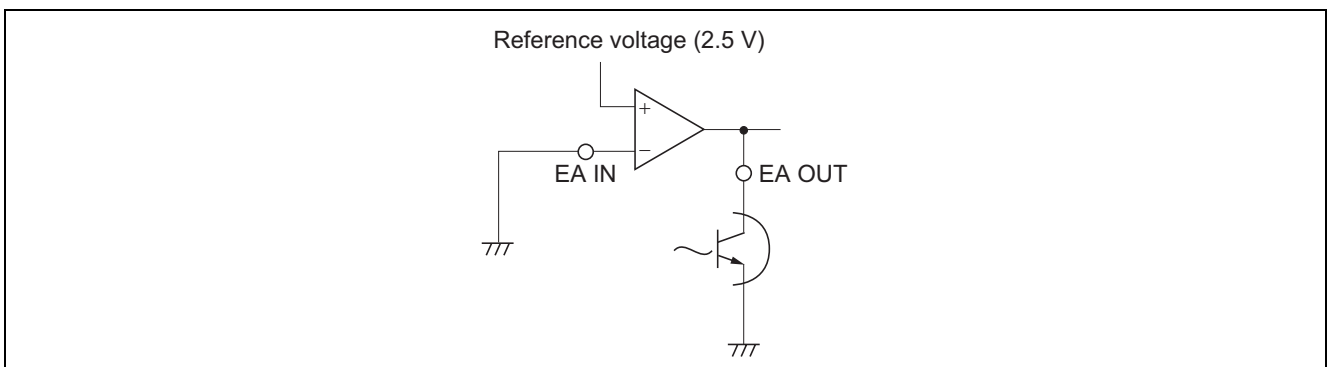
In the case that feed forward system by photo-coupler is applied, following two methods are available.

One is the method by error amp. as in figure 3-1, the other is by the direct connection to photo-coupler as in figure 3-2.

When photo-coupler is directly connected to EA OUT terminal, input terminal of error amp. is connected to GND, photo-coupler is connected directly to EA OUT terminal.



**Figure 3-1 Method to Use Photo-Coupler (1)**



**Figure 3-2 Method to Use Photo-Coupler (2)**

In figure 3-1, AC gain is represented as :

$$|A_V| = |R_F / R_{IN}|$$

Proper gain setting is about 40 dB.

$R_F$  should be 52 k $\Omega$  or more due to the current source capability of error amp.

$R_1$ ,  $R_2$  should meet the condition as below so that the voltage of EA IN terminal should not be over 5 V.

$$R_2 \cdot V_{CC} / (R_1 + R_2) \leq 5 \text{ V}$$

Due to the input impedance of EA IN terminal, the current in  $R_1$ ,  $R_2$  should be less than several mA.

### CT (OVP) Terminal

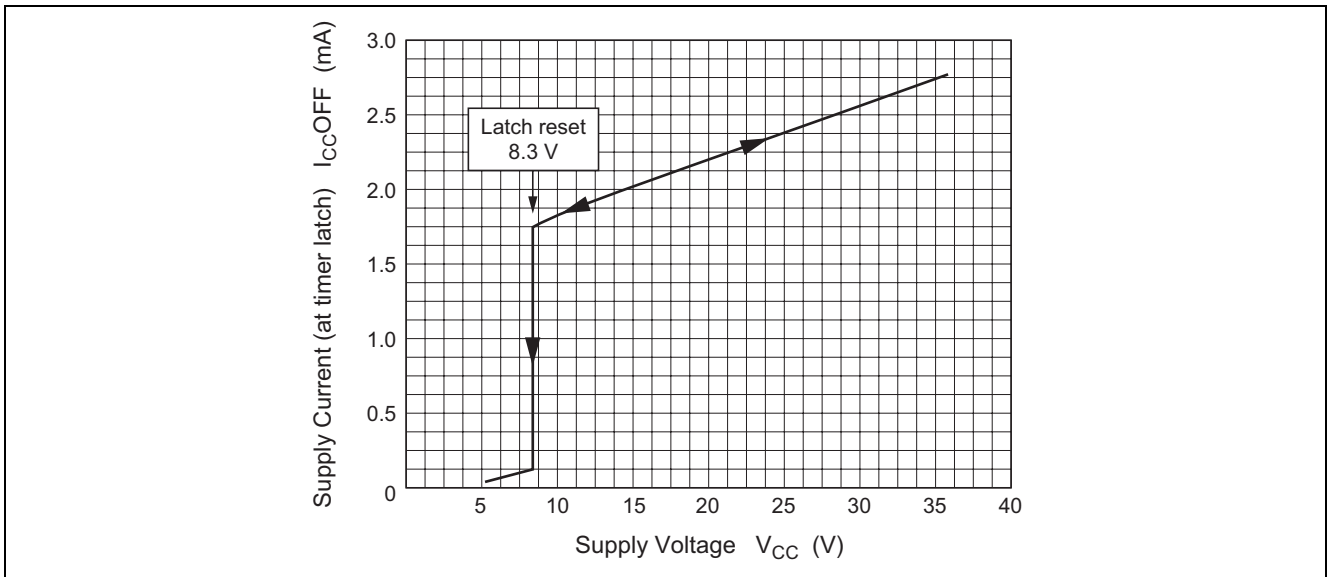
Timer type latch circuit works as follows.

Constant charge current flows out from CT terminal to the external capacitor when CLM is operative.

When the voltage of CT terminal rises up to over 4.0 V (Typ.), the latch circuit operates to make functions of this IC inoperative. Inoperative status is sustained until supply voltage becomes less than stop voltage. The value for start-up register has to be set so that the current over 1.8 mA (Typ.) can flow the resistor because the stop status has to be kept by the current in start-up resistor  $R_1$  shown in application circuit.

When timer latch circuit is operative, supply current increases at high voltage as shown in figure 4 to avoid the damage caused by unnecessarily increased supply voltage.

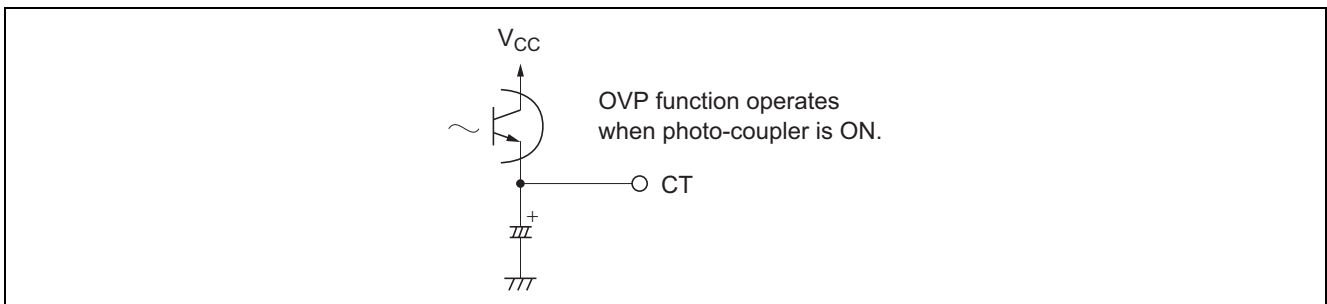
Inoperative status goes back to operation by forcibly decreasing the voltage of CT terminal to less than 0.7 V.



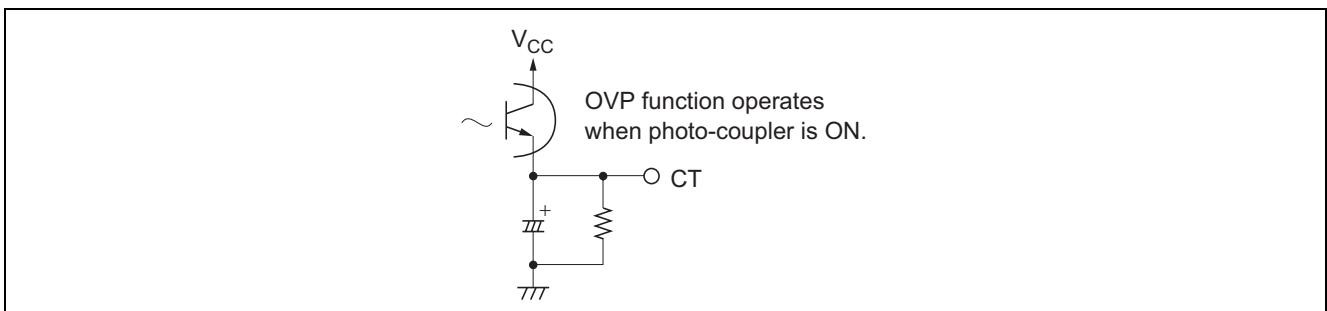
**Figure 4 Supply Current vs. Supply Voltage Characteristics (at Timer Latch)**

Even if the timer function is not needed, latch function operates, that is, IC becomes in operative when the voltage of CT terminal is forced to be high voltage. Therefore, CT terminal can also be used for OVP (over voltage protection).

When only OVP function is needed (timer latch function is not necessary), connect the resistor between CT terminal and GND. In this case, the above mentioned charge current cannot make the voltage of CT terminal rise up to “H” threshold, thus latch function does not operate. (Refer to figure 5-1, 5-2)



**Figure 5-1 Method to Use Timer Type Latch And OVP**



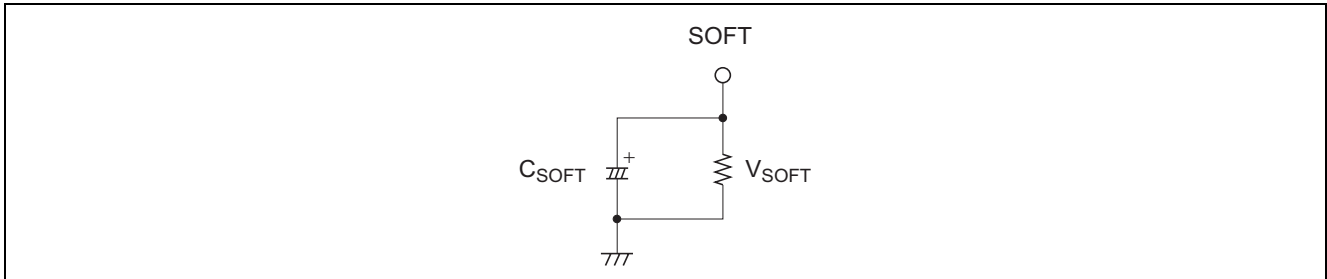
**Figure 5-2 Method to Use Only OVP**

## SOFT (Duty Set-Up) Terminal

The voltage of SOFT terminal determines the maximum duty.

Maximum duty can be set by connecting the resistor as in figure 6 because the constant current compensated for temperature flows out of this terminal.

And by connecting the capacitor between the terminal and GND, soft start function operates. That is, we can get the gradual increase of maximum duty at start-up.



**Figure 6 Method to Set Up Duty and SOFT Start Function**

Maximum duty is represented as :

$$\text{Duty (Max.)} \approx (42 \cdot V_{\text{SOFT}}) - 59 (\%)$$

$$\text{where } V_{\text{SOFT}} = I_{\text{SOFT}} \cdot R_{\text{SOFT}} (\text{V}), I_{\text{SOFT}} = 43 \mu\text{A (Typ.)}$$

If the voltage of SOFT terminal is higher than 3.53 V (Typ.) (upper limit voltage of the oscillation waveform), maximum duty is internally decided to be 90%.

Soft start time ( $T_{\text{SOFT}}$ ) is represented as :

$$T_{\text{SOFT}} \approx C_{\text{SOFT}} \cdot 31 \cdot 10^3 (\text{s})$$

$T_{\text{SOFT}}$  means the time from start-up until the voltage of SOFT terminal goes up to higher than 1.4 V (Typ.) (lower limit voltage of the oscillation waveform).

Discharging circuit operative before start-up at  $V_{\text{CC}}$  is internally equipped so that the soft start never fail to operate at the restart of voltage supply.

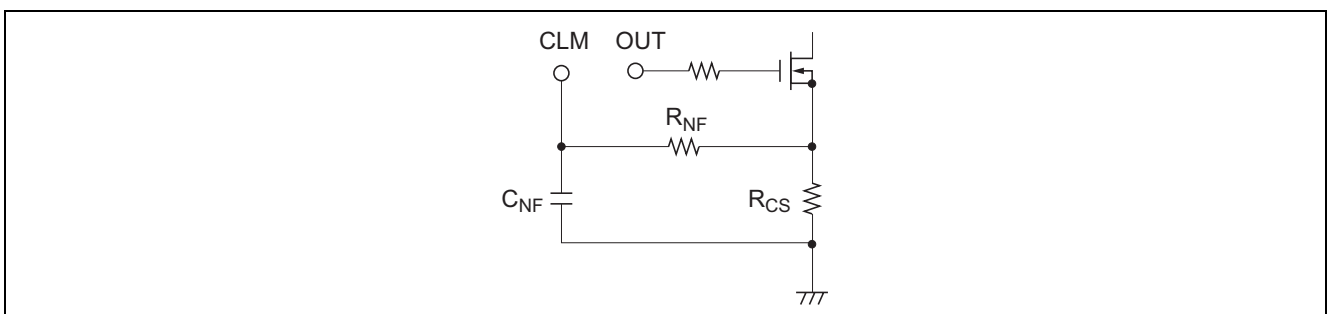
## CLM Terminal

This terminal is for pulse-by-pulse current limiting.

Current limiting circuit is almost the same as that of M51995.

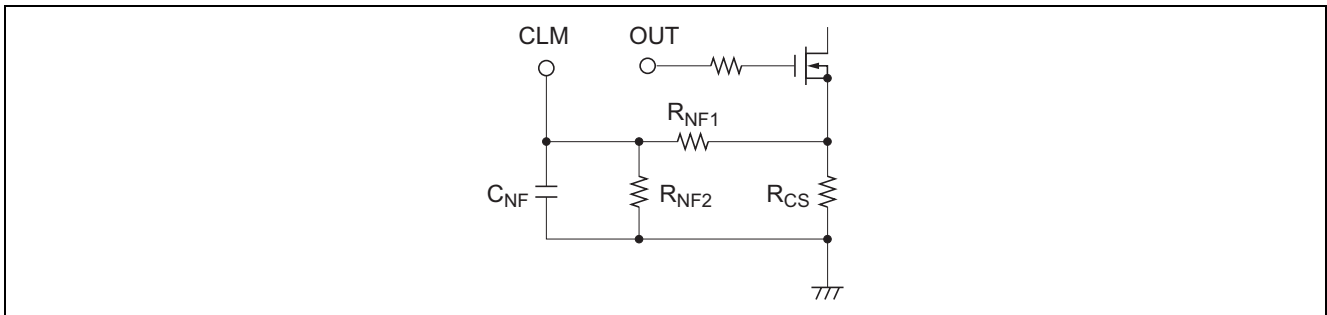
CLM terminal is separate from CURRENT SENSE terminal allowing the noise filter to be optimized and the high-speed over current protection.

The voltage detected by the current detecting resistor can be directly input as shown in figure 7-1, if the detected voltage is about the threshold voltage (200 mV (Typ.)), but if the voltage is larger than the threshold, the voltage has to be input divided by resistors as shown in figure 7-2.



**Figure 7-1 Peripheral Circuit of CLM**





**Figure 7-2 Peripheral Circuit of CLM When The Detected Voltage is High**

1000 pF to 22000 pF is recommended for  $C_{NF}$ . Be sure to use 100  $\Omega$  or less for  $R_{NF}$  and  $R_{NF1} // R_{NF2}$  (\*) so that the detection sensitivity is not influenced by the current flown out from CLM terminal.

Non-inductive resistor is recommended for current detecting resistor.

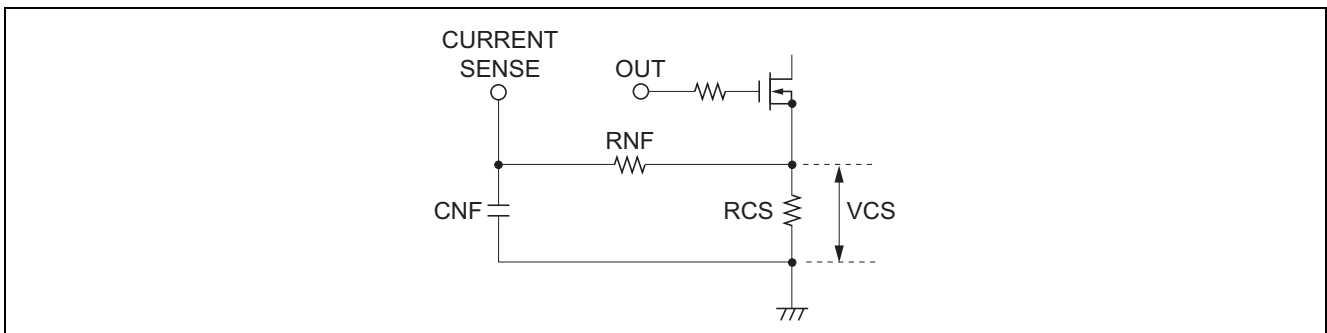
$$* R_{NF1} // R_{NF2} = (R_{NF1} \cdot R_{NF2}) / (R_{NF1} + R_{NF2})$$

### CURRENT SENSE Terminal

The voltage proportional to the switching current is supplied to this terminal.

Output duty is controlled by comparing this voltage with the output of error amp..

CLM and CURRENT SENSE terminal is separate from each other, so various settings are available depending upon the application.



**Figure 8 Peripheral Circuit of CURRENT SENSE**

$R_{CS}$  is determined by :

$$V_{CS} = (V_{EA\ OUT} - 1.3) / 3 \text{ (V)}, \text{ where } V_{EA\ OUT} \text{ represents the voltage of } E_{A\ OUT} \text{ terminal.}$$

### CF Terminal

Oscillation frequency is set by capacitor connected to CF terminal.

The waveform of CF terminal is triangular one with the ratio of 9 : 1 for charge-discharge period.

Oscillation frequency is represented as :

$$f_{OSC} = \frac{1}{(19.4 \times 10^3 \times C_{OSC}) + (0.4 \times 10^{-6})} \text{ (Hz)}$$

### Attention for heat generation

Although the absolute maximum rating of ambient temperature is spelled out as 85°C, it is always annoying to specify the location this temperature refers to because the power dissipation generated locally in switching regulator is fairly large and the temperature in the vicinity of the IC varies from place to place.

One of the recommendable ways to solve this problem is to check the temperature on the surface of the IC.

The difference in temperature between IC junction and the surface of IC package is 30°C or less when IC junction temperature is measured by utilizing the temperature characteristics of p-n junction forward voltage, and the surface temperature by "thermo-viewer" on the condition that the IC is mounted on the "phenol-base" PC board in normal atmosphere.

This concludes that maximum case temperature (surface temperature of IC package) rating is 100°C with adequate margin considering the absolute maximum rating of junction temperature is 150°C.





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