

Silicon PNP Power Transistors

BD910 BD912

DESCRIPTION

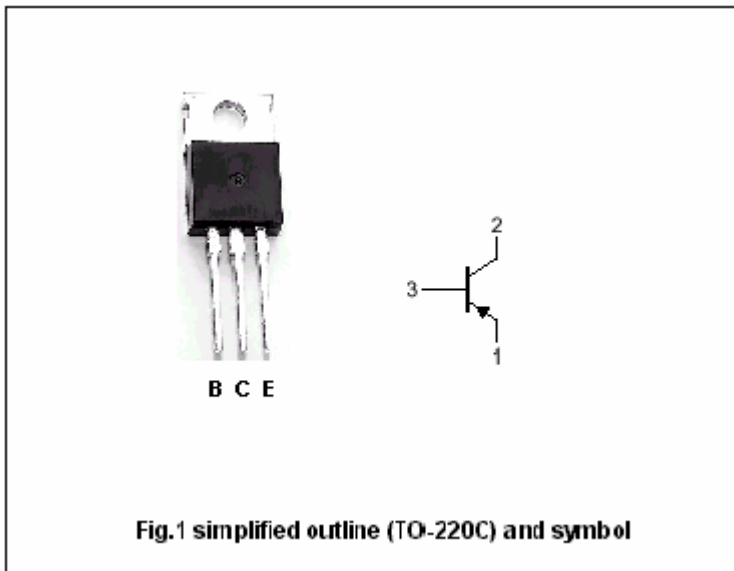
- With TO-220C package
- Complement to type BD909 BD911

APPLICATIONS

- Intended for use in power linear and switching applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base



Absolute maximum ratings (Ta=25)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	BD910	-80	V
		BD912	-100	
V _{CEO}	Collector-emitter voltage	BD910	-80	V
		BD912	-100	
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-15	A
I _B	Base current		-5	A
P _C	Collector power dissipation	T _C 25	90	W
T _j	Junction temperature		150	
T _{stg}	Storage temperature		-65~150	

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	MAX	UNIT
R _{th j-c}	Thermal resistance junction to case	1.4	/W

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CHARACTERISTICS

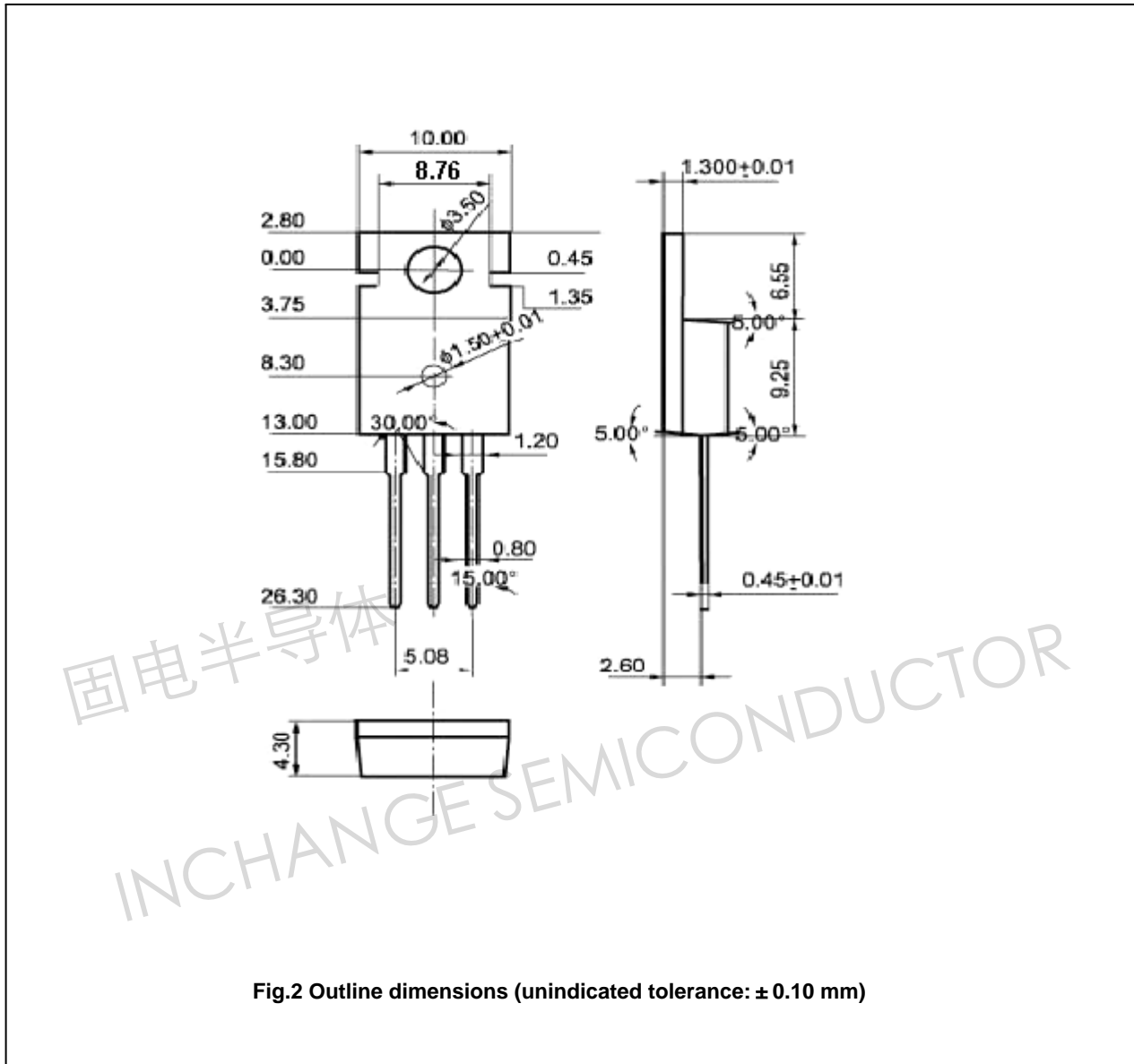
T_j=25 unless otherwise specified

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEO(SUS)}	Collector-emitter sustaining voltage	BD910	I _C =-0.1A; I _B =0	-80			V
		BD912		-100			
V _{CEsat-1}	Collector-emitter saturation voltage		I _C =-5 A; I _B =-0.5 A			-1.0	V
V _{CEsat-2}	Collector-emitter saturation voltage		I _C =-10A; I _B =-2.5 A			-3.0	V
V _{BEsat}	Base-emitter saturation voltage		I _C =-10A; I _B =-2.5 A			-2.5	V
V _{BE}	Base-emitter voltage		I _C =-5A ; V _{CE} =-4V			-1.5	V
I _{CBO}	Collector cut-off current	BD910	V _{CB} =-80V; I _E =0 T _C =150			-0.5 -5.0	mA
		BD912	V _{CB} =-100V; I _E =0 T _C =150			-0.5 -5.0	
I _{CEO}	Collector cut-off current	BD910	V _{CE} =-40V; I _B =0			-1.0	mA
		BD912	V _{CE} =-50V; I _B =0				
I _{EBO}	Emitter cut-off current		V _{EB} =-5V; I _C =0			-1.0	mA
h _{FE-1}	DC current gain		I _C =-0.5A ; V _{CE} =-4V	40		250	
h _{FE-2}	DC current gain		I _C =-5A ; V _{CE} =-4V	15		150	
h _{FE-3}	DC current gain		I _C =-10A ; V _{CE} =-4V	5			
f _T	Transition frequency		I _C =-0.5A ; V _{CE} =-4V	3			MHz

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PACKAGE OUTLINE



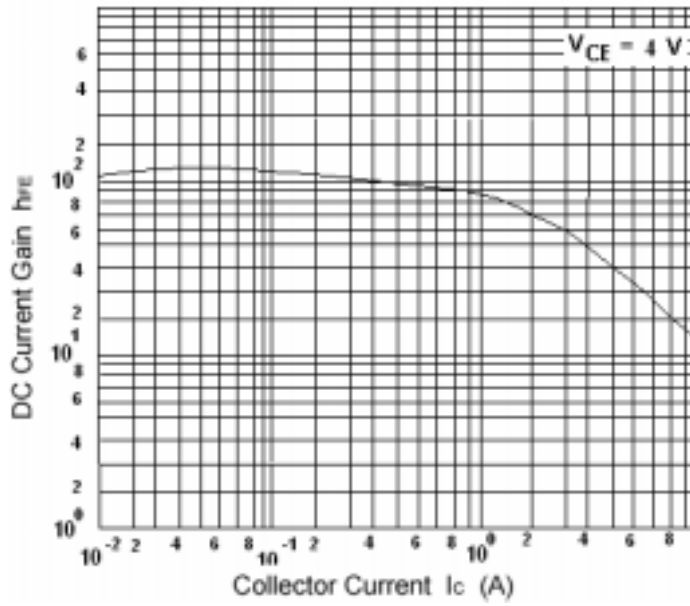


Fig.3 $h_{FE} - I_C$

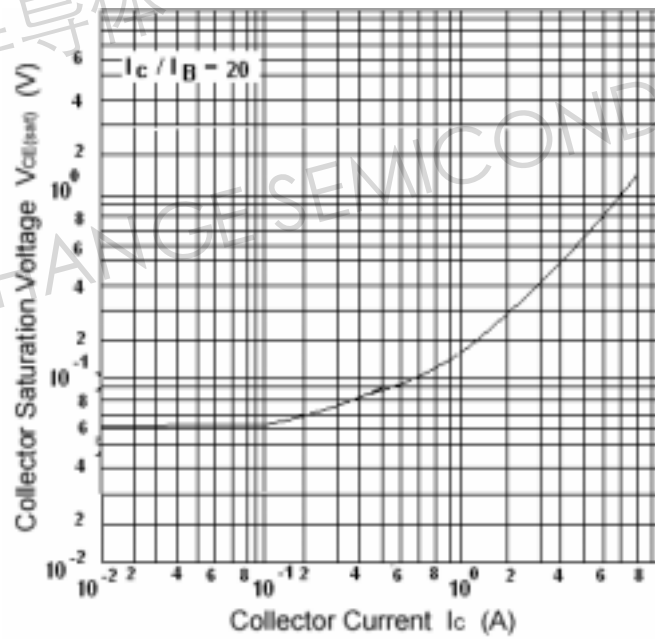


Fig.4 $V_{CE(sat)} - I_C$

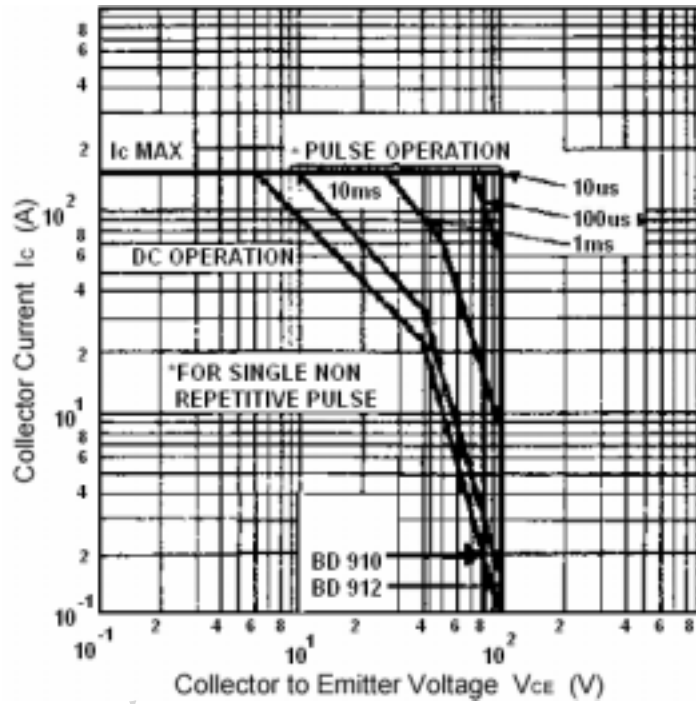


Fig.5 SAFE OPERATING AREA

固电半导体 INCHANGE SEMICONDUCTOR