

### **VIAS2-SIP Series DC-DC Converter**

Rev. 06-2006

### Description

Designed to convert fixed voltages into an isolated regulated voltage, the VIAS2-SIP series is well suited for providing boardmount local supplies in a wide range of applications, including mixed analog/digital circuits, test & measurement equip., process/machine controls, datacom/telecom fields, etc...

### **Features**

- -Isolated 2 W output
- Regulated
- High efficiency to 74%
- ·Dual voltage output ·Small footprint
- ·SIP package style
- ·Industry standard pinout
- ·UL94-V0 package
- •No heatsink required
- -1K VDC isolation
- •Temperature range: -40°C~+85°C
- •No external component required
- ·Low cost



mpar	Voltage	Output	Output (	Jurrent		Package
Nominal	Range	Voltage	Max.	Min.	Efficiency	Style
5 Vdc	4.75~5.25 Vdc	±5 Vdc	±150 mA	±15 mA	70%	SIP
5 Vdc	4.75~5.25 Vdc	±9 Vdc	±100 mA	±10 mA	72%	SIP
5 Vdc	4.75~5.25 Vdc	±12 Vdc	±83 mA	±9 mA	72%	SIP
5 Vdc	4.75~5.25 Vdc	±15 Vdc	±67 mA	±7 mA	73%	SIP
12 Vdc	11.4~12.4 Vdc	±5 Vdc	±150 mA	±15 mA	70%	SIP
12 Vdc	11.4~12.4 Vdc	±9 Vdc	±100 mA	±10 mA	71%	SIP
12 Vdc	11.4~12.4 Vdc	±12 Vdc	±83 mA	±9 mA	72%	SIP
12 Vdc	11.4~12.4 Vdc	±15 Vdc	±67 mA	±7 mA	74%	SIP
24 Vdc	22.8~25.2 Vdc	±5 Vdc	±150 mA	±15 mA	71%	SIP
24 Vdc	22.8~25.2 Vdc	±9 Vdc	±100 mA	±10 mA	72%	SIP
24 Vdc	22.8~25.2 Vdc	±12 Vdc	±83 mA	±9 mA	73%	SIP
24 Vdc	22.8~25.2 Vdc	±15 Vdc	±67 mA	±7 mA	73%	SIP
	5 Vdc 5 Vdc 5 Vdc 12 Vdc 12 Vdc 12 Vdc 12 Vdc 12 Vdc 24 Vdc 24 Vdc 24 Vdc	5 Vdc   4.75~5.25 Vdc     12 Vdc   11.4~12.4 Vdc     12 Vdc   11.4~2.4 Vdc     24 Vdc   22.8~25.2 Vdc     24 Vdc   22.8~25.2 Vdc     24 Vdc   22.8~25.2 Vdc	5   Vdc   4.75~5.25   Vdc   ±5   Vdc     5   Vdc   4.75~5.25   Vdc   ±9   Vdc     5   Vdc   4.75~5.25   Vdc   ±12   Vdc     5   Vdc   4.75~5.25   Vdc   ±12   Vdc     5   Vdc   4.75~5.25   Vdc   ±12   Vdc     12   Vdc   11.4~12.4   Vdc   ±5   Vdc     12   Vdc   11.4~12.4   Vdc   ±9   Vdc     12   Vdc   11.4~12.4   Vdc   ±12   Vdc     12   Vdc   11.4~12.4   Vdc   ±12   Vdc     12   Vdc   11.4~12.4   Vdc   ±12   Vdc     12   Vdc   11.4~12.4   Vdc   ±15   Vdc     24   Vdc   22.8~25.2   Vdc   ±5   Vdc     24   Vdc   22.8~25.2   Vdc   ±9   Vdc     24   Vdc   22.8~25.2   Vdc	5 Vdc 4.75~5.25 Vdc ±5 Vdc ±150 mA   5 Vdc 4.75~5.25 Vdc ±9 Vdc ±100 mA   5 Vdc 4.75~5.25 Vdc ±12 Vdc ±83 mA   5 Vdc 4.75~5.25 Vdc ±12 Vdc ±83 mA   5 Vdc 4.75~5.25 Vdc ±12 Vdc ±67 mA   12 Vdc 11.4~12.4 Vdc ±5 Vdc ±100 mA   12 Vdc 11.4~12.4 Vdc ±9 Vdc ±100 mA   12 Vdc 11.4~12.4 Vdc ±12 Vdc ±83 mA   12 Vdc 11.4~12.4 Vdc ±12 Vdc ±83 mA   12 Vdc 11.4~12.4 Vdc ±12 Vdc ±83 mA   12 Vdc 11.4~12.4 Vdc ±15 Vdc ±67 mA   24 Vdc 22.8~25.2 Vdc ±5 Vdc ±150 mA   24 Vdc 22.8~25.2 Vdc ±5 Vdc ±100 mA   24 Vdc 22.8~25.2 Vdc ±12 Vdc ±83 mA	5 Vdc 4.75~5.25 Vdc ±5 Vdc ±150 mA ±15 mA   5 Vdc 4.75~5.25 Vdc ±9 Vdc ±100 mA ±10 mA   5 Vdc 4.75~5.25 Vdc ±12 Vdc ±83 mA ±9 mA   5 Vdc 4.75~5.25 Vdc ±12 Vdc ±83 mA ±9 mA   5 Vdc 4.75~5.25 Vdc ±15 Vdc ±67 mA ±7 mA   12 Vdc 11.4~12.4 Vdc ±5 Vdc ±100 mA ±10 mA   12 Vdc 11.4~12.4 Vdc ±9 Vdc ±100 mA ±10 mA   12 Vdc 11.4~12.4 Vdc ±12 Vdc ±83 mA ±9 mA   12 Vdc 11.4~12.4 Vdc ±12 Vdc ±83 mA ±9 mA   12 Vdc 11.4~12.4 Vdc ±12 Vdc ±83 mA ±9 mA   12 Vdc 11.4~12.4 Vdc ±12 Vdc ±83 mA ±9 mA   12 Vdc 11.4~12.4 Vdc ±15 Vdc ±67 mA ±7 mA   24 Vdc 22.8~25.2 Vdc ±5 Vdc ±150 mA ±15 mA   24 Vdc 22.8~25.2 Vdc ±9 Vdc ±100 mA ±10 mA   24 Vdc 22.8~25.2 Vdc ±12 Vdc ±83 mA ±9 mA	5 Vdc 4.75~5.25 Vdc ±5 Vdc ±150 mA ±15 mA 70%   5 Vdc 4.75~5.25 Vdc ±9 Vdc ±100 mA ±10 mA 72%   5 Vdc 4.75~5.25 Vdc ±12 Vdc ±83 mA ±9 mA 72%   5 Vdc 4.75~5.25 Vdc ±12 Vdc ±83 mA ±9 mA 72%   5 Vdc 4.75~5.25 Vdc ±12 Vdc ±67 mA ±7 mA 73%   12 Vdc 11.4~12.4 Vdc ±5 Vdc ±100 mA ±10 mA 71%   12 Vdc 11.4~12.4 Vdc ±9 Vdc ±100 mA ±10 mA 71%   12 Vdc 11.4~12.4 Vdc ±12 Vdc ±83 mA ±9 mA 72%   12 Vdc 11.4~12.4 Vdc ±12 Vdc ±83 mA ±9 mA 72%   12 Vdc 11.4~12.4 Vdc ±12 Vdc ±83 mA ±9 mA 72%   12 Vdc 11.4~12.4 Vdc ±15 Vdc ±67 mA ±7 mA 74%   24 Vdc 22.8~25.2 Vdc ±5 Vdc ±100 mA ±10 mA 71%   24 Vdc 22.8~25.2 Vdc ±9 Vdc ±100 mA ±10 mA 72% <td< td=""></td<>

#### Note:

1. All specifications measured at TA=25°C, humidity <75%, nominal input voltage and rated output load unless otherwise specified.

### **Output Specifications**

Item	Test conditions	Min.	Тур.	Max.	Units
Output power		0.2		2	W
Line Regulation	For Vin change of 1%			0.25	%
Load Regulation	10% to 100% full load			1	%
Output voltage accuracy	100% full load			±3	%
Temperature drift	100% full load			0.03	%/°C
Output ripple	20 MHz Bandwidth		20	30	mVp-p
Output noise	20 MHz Bandwidth		75	150	mVp-p
Switching frequency	Full load, nominal input		75		KHz



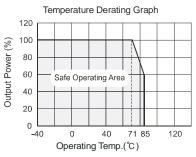
# **General Specifications**

Short circuit protection	1 second
Temperature rise at full load	25°C Max, 15°C Typ.
Cooling	Free air convection
Operating temperature range	-40°C to +85°C
Storage temperature range	-55°C to +125°C
Soldering temperature	300°C (1.5mm from case for 10 sec.)
Storage humidity range	<95%
Case material	Plastic (UL94-V0)
MTBF	>3,500,000 hrs.
Burn-in	At +85°C, for 4 hours at no-load and 4 hours at full load.

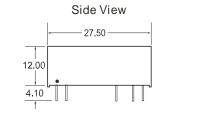
## **Isolation Specifications**

Item	Test Conditions	Min.	Тур.	Max.	Units
Isolation Voltage	Tested for 1 min.	1000			Vdc
Insulation Resistance	Test at 500 Vdc	1000			MΩ

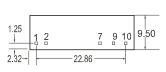
# **Typical Characteristics**

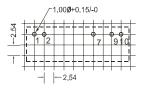


## Outline Dimensions & Recommended Layout Pattern



**Bottom View** 





1	+Vin
2	-Vin
7	+Vout
9	-Vout
10	COM

Note: All Pins on a 2.54mm pitch; all pin diameters are 0.50mm; all dimensions in mm.



### **Application Notes:**

#### - Input filtering

To reduce the reflected ripple current and minimize EMI, especially when the converter input is more than 2" away from the DC source, it is recommended to connect a low ESR electrolytic capacitor between Vin and Gnd. The values suggested are as shown in Table 1. If additional filtering is required, the capacitance may be increased, or expanded to an LC network as shown in Figure 1.

### Table 1

Input Voltage	External Input Capacitance
5 V	4.7 µF
12 V	2.2 µF
24 V	1.0 µF

- Output filtering

An output capacitor as shown in Table 2 may be used to reduce output ripples and noise.

requirements as shown in Table 2.

Output capacitance may be increased for additional filtering, but should not exced  $10\mu F$ . It can also be expanded to an LC network as in Figure 1.

### Table 2

Vout	External Ouput Capacitance
5 V	4.7 µF
9 V	2.2 μF
12 V	1.0 µF
15 V	0.47 µF

#### - Minimum loading

The converter needs a minimum of 10% loading to maintain output regulation. Operation under no-load conditions will not cause immediate damages but may reduce reliability, and cause performance not to meet specifications.

#### - Protection

The converter has minimal protection against input over-voltage or output over-load, and may be permanently damaged if exposed to these conditions. An input clamping device can be used for input voltage limiting. An input fuse or an output fuse can also be used to protect against over-loading.

#### - Unregulated input

As fixed input converters, this series can accept voltages within a limited range of the nominal input. Otherwise the converter may not function properly or may be damaged.

