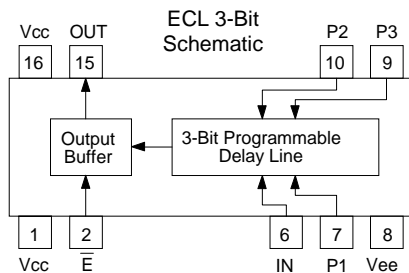


3-Bit Programmable Delay Modules

PECL3 Series 10K ECL Logic

3PECLH Series 10KH ECL Logic

Available in Surface Mount



ENABLE input \bar{E} , Pin 2, is active low.
Output is disabled (low) when Pin 2 is logic high.

Electrical Specifications at 25°C

3Bit 10K ECL DIP Part Number	3-Bit 10KH ECL DIP Part Number	Delay per Step (ns)	Error ref. to "000" (ns)	Referenced to "000" - Delay (ns) per Program Setting (P3*P2*P1)									
				000	001	010	011	100	101	110	111		
"000"=3±0.5ns **	"000"=1.5±.5ns **												
PECL3-0.5	3PECLH-0.5	0.5 ± .25	± .30	0.0	0.5	1.0	1.5	2.0	2.5	3.0	3.5		
PECL3-0.75	3PECLH0.75	0.75 ± .3	± .50	0.0	0.75	1.50	2.25	3.00	3.75	4.50	5.25		
PECL3-1	3PECLH-1	1.0 ± .4	± .50	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0		
PECL3-1.25	3PECLH1.25	1.25 ± .5	± .70	0.0	1.25	2.50	3.75	5.00	6.25	7.50	8.75		
PECL3-1.5	3PECLH-1.5	1.5 ± .5	± .70	0.0	1.5	3.0	4.5	6.0	7.5	9.0	10.5		
PECL3-2	3PECLH-2	2.0 ± .7	± .80	0.0	2.0	4.0	6.0	8.0	10.0	12.0	14.0		
PECL3-2.5	3PECLH-2.5	2.5 ± .7	± .90	0.0	2.5	5.0	7.5	10.0	12.5	15.0	17.5		
PECL3-3	3PECLH-3	3.0 ± .7	± 1.0	0.0	3.0	6.0	9.0	12.0	15.0	18.0	21.0		
PECL3-5	3PECLH-5	5.0 ± 1.0	± 1.5	0.0	5.0	10.0	15.0	20.0	25.0	30.0	35.0		
PECL3-10	3PECLH-10	10.0 ± 1.5	± 3.0	0.0	10.0	20.0	30.0	40.0	50.0	60.0	70.0		

**** INITIAL DELAY & CUMULATIVE TOLERANCES:** "Error" Tolerance is for Programmed Delays Referenced to Initial Delay, Setting "000."
For example, the setting "111" delay of PECL3-2 is 14.0 ± 0.8 ns ref. to "000," and 17.0 ± 1.3 ns referenced to the input,
and the setting "111" delay of 3PECLH-2 is 14.0 ± 0.8 ns ref. to "000," and 15.5 ± 1.3 ns referenced to the input.

INPUT LOADING: Input, Pin 6, internally connected to eight ECL gate inputs terminated by Thevenin equivalent of 100 Ohms to -2V.

OPERATING SPECIFICATIONS (10K, PECL3)

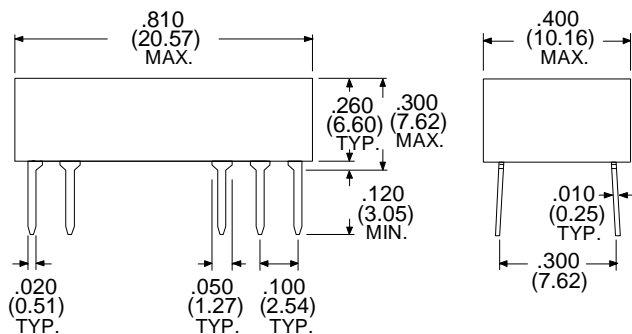
V_{EE} Supply Voltage	-5.20 ± 0.25VDC
I_{EE} Supply Current	60 mA typical
Logic "1" Input: V_{IH}	-0.98V min.
I_{IH}	265 μ A max.
I_{IH} (Pin 6) *	-11mA typ.
Logic "0" Input: V_{IL}	-1.63V max.
I_{IL}	0.5 μ A min.
I_{IL} (Pin 6) *	-2mA typ.
V_{OH} Logic "1" Voltage Out	-0.96V min.
V_{OL} Logic "0" Voltage Out	-1.65V max.
P_{WI} Input Pulse Width	40% of Max. Delay min.
Operating Temp. Range (10K, PECL3)	-30 to +85°C
Storage Temperature Range	-65 to +150°C

OPERATING SPECIFICATIONS (10KH, 3PECLH)

V_{EE} Supply Voltage	-5.20 ± 0.25VDC
I_{EE} Supply Current	75 mA typical
Logic "1" Input: V_{IH}	-0.98V min.
I_{IH}	320 μ A max.
I_{IH} (Pin 6) *	-11mA typ.
Logic "0" Input: V_{IL}	-1.63V max.
I_{IL}	0.7 μ A min.
I_{IL} (Pin 6) *	-2mA typ.
V_{OH} Logic "1" Voltage Out	-0.96V min.
V_{OL} Logic "0" Voltage Out	-1.65V max.
P_{WI} Input Pulse Width	40% of Max. Delay min.
Operating Temp. Range (10KH, 3PECLH)	-0 to +75°C
Storage Temperature Range	-65 to +150°C

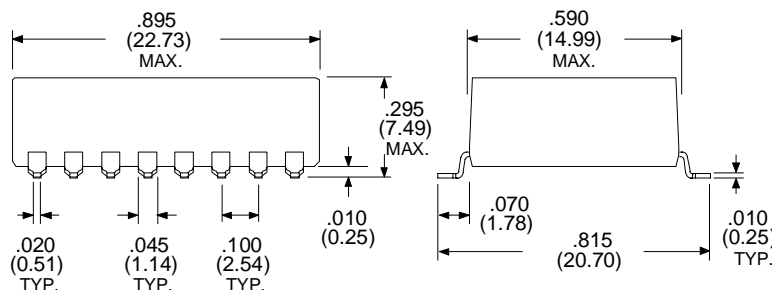
* Refer to Input (Pin 6) Loading note above.

Dimensions in Inches (mm)



16-Pin SMD Pkg. Unused leads are NOT removed.

To Specify SMD Package, Add "H" Suffix to P/N
Examples: PECL3-1.25H, 3PECLH-2H



Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

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