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ML5805

5.8GHz Variable Data Rate FSK Transceiver with Integrated PA

Preliminary Data Sheet

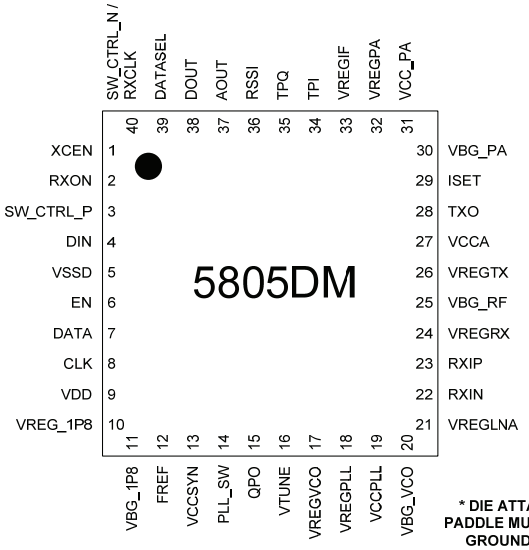
GENERAL DESCRIPTION

The ML5805 is a single chip fully integrated Frequency Shift Keyed (FSK) transceiver developed for a variety of applications operating in the 5.725GHz to 5.850GHz unlicensed ISM band. The ML5805 is mode selectable for operation with digital cordless phones (DSSS or DECT) and higher data rate streaming applications like wireless audio and video.

The ML5805 contains a dual-conversion low-IF receiver with all channel selectivity on chip. IF filtering, IF gain, and demodulation are performed on-chip, eliminating the need for any external IF filters or production tuning. A post detection filter and a data slicer are integrated to complete the receiver.

The ML5805 transmitter uses an adjustment-free closed loop modulator, which modulates the on-chip VCO with filtered data. The ML5805 includes an upconversion mixer, a buffer/predriver, and a power amplifier to produce a typical output power of +21dBm. A fully integrated fractional synthesizer is used in both receive and transmit modes. Power supply regulation is included in the ML5805, providing circuit isolation and consistent performance over supply voltages between 2.8V-3.6V.

PIN CONFIGURATION (TOP VIEW)



*** DIE ATTACH PADDLE MUST BE GROUNDED**

ORDERING INFORMATION

PART NUMBER	TEMP RANGE	PACKAGE	PACK (QTY)
ML5805DM	-10°C to +60°C	40 QFN 6x6 mm	Antistatic Tray (490)
ML5805DM-T	-10°C to +60°C	40 QFN 6x6 mm	Tape & Reel (2500)

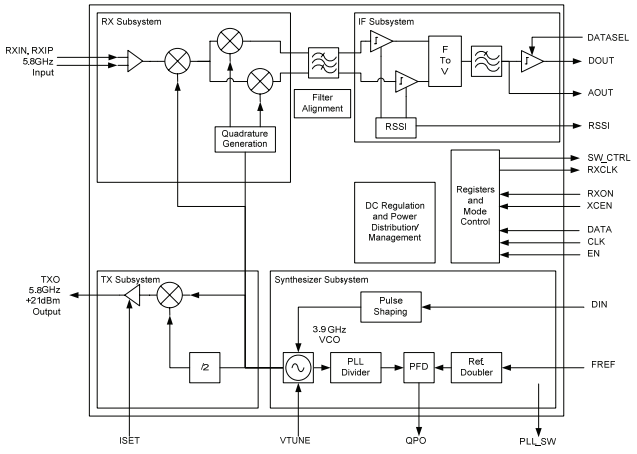
FEATURES

- Highly integrated 5.8GHz FSK Transceiver with selectable data rates; 576kbps, 1.152Mbps, 1.536Mbps, 1.755Mpbs, 2.048Mbps
- Fractional-N synthesizer with 30 Hz resolution
- Low-IF receiver eliminates external IF filters
- Fully integrated digital FIR Tx data filter, IF filters, FM discriminator, and Rx data filter.
- Self-calibrating VCO and filters eliminate tuning.
- Operating Modes include DSSS-DCT, DECT, and high rate (2.048Mbps) for wireless audio and video
- -97dBm sensitivity (0.1%BER) with Integrated LNA
- +21dBm typical output power from Integrated PA
- Includes **FastWave™** embedded wireless microcontroller technology
- Simple 3-wire control interface
- TR PIN diode or FET switch driver outputs
- Analog RSSI output: 35mV/dB
- Selectable Rx clock recovery output
- 40 QFN package (6mm x 6mm)

APPLICATIONS

- Digital Cordless Telephones DSSS & DECT
- Wireless Streaming Audio and Video
- Wireless Data Links

BLOCK DIAGRAM



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Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied. Operating the device for any length of time beyond the operating conditions may degrade device performance and/or shorten operating lifetime.

VCC ..... VSS-0.3 to 3.6 V
VCC_PA ..... VSS-0.3 to 4.5 V
Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10s) ..... 260°C

OPERATING CONDITIONS

Ambient Temperature Range (T_A) ..... -10°C to 60°C
VCC Range [VDD (pin 9), VCCSYN (pin 13), VCCPLL (pin 19), VCCA (pin27)] ..... 2.8V to 3.6V
VCC_PA Range [VCC_PA (pin31)] ..... 3.0V to 4.5V
Thermal Resistance (θ_{JA}) ..... 36°C/W

ELECTRICAL CHARACTERISTICS

Unless otherwise specified T_A = 25°C and the supply voltage is VCC=3.3V, VCC_PA=3.6V, R_{ISET}=381 Ohm, FREF=12.288MHz, DATA RATE=1.536Mbps, all measurements are normalized to the IC pins.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
I_{STBY}	Supply current, STANDBY mode	DC supply connected, XCEN low, RXON high		2		µA
I_{RX}	Supply current, RECEIVE mode	RX chain active, data being received		69		mA
I_{TX}	Transmit supply current at VCC pins			77		mA
I_{TXPA}	VCC_PA pin	P_{OUT}=+21dBm		100		mA
		P_{OUT}=+18dBm[1]		78		mA
SYNTHESIZER						
I_P	Charge Pump sink/source current			±0.2		mA
V_{TUNE}	VCO input voltage		0.3		2.5	V
t_{FH}	Lock time for any in band frequency change	From EN asserted to RX valid data (RX) or PAON high (TX)		110		µsec
		NOIVCOC = 1 (no incremental VCO cal)		55		µsec
PN	Phase noise	@ 100 kHz @ 1 MHz @ 2 MHz @ 10 MHz		-85 -116 -122 -134		dBc/Hz

[1] Contact factory for configuration settings for this power setting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f_{FREF}	Reference signal frequency	Data Rate=1.5360, 1.7554, and 2.0480Mbps		12.288		MHz
		Data Rate=576, 1,152Kbps		13.824		MHz
V_{FREF}	Reference signal input level	Clipped sine, AC coupled	0.5			V_{P-P}
RECEIVER						
F_{RXI}	Receive input frequency range		5.725		5.850	GHz
Z_{RX}	Input Impedance			100 Ohm Differential		Ω
F_{STEP}	Channel Spacing	Data Rate=1.1520Mbps Data Rate=1.5360Mbps Data Rate=1.7554Mbps Data Rate=2.0480Mbps		1.728 2.048 4.096 4.096		MHz
S_{RXI}	Input Sensitivity	<0.1%BER@1.1520Mbps <0.1%BER@1.5360Mbps <0.1%BER@1.7554Mbps <0.1%BER@2.0480Mbps		-97 -97 -97 -96		dBm
P_{IN}	RF Input Power	<0.1%BER@ 1.1520Mbps, 1.5360Mbps, 1.7554Mbps, and 2.0480Mbps			+10	dBm
T_{SLICE}	Data Slicer Time Constant	DATASEL= V_{IH} DATASEL= V_{IL}		6 300		uS uS
P_{RXI}	RX conducted emissions at RXI	RXI terminated in 50 ohms			-50	dBm
IRR	RX Chain Image rejection ratio			28		dB
ACR	RX adjacent channel(s) rejection Wanted signal = -80dBm, PN20, CW Interfering signal, 0.1% BER	±1 channel offset ±2 channels offset ±3 or more channels offset		15 40 45		dB dB dB
CCR	Co-Channel rejection, 0.1% BER	Wanted signal = -80dBm, Unwanted signal is GFSK modulated with 1.536Mbps PRBS data, BT=0.9		-9		dB
RSSI						
t_{R_RSSI}	RSSI rise time, 20% to 80%	20pF loading on RSSI pin RF off to -15dBm		5	10	µsec
t_{F_RSSI}	RSSI fall time, 80% to 20%	20pF loading on RSSI pin –15dBm to RF off		5	10	µsec
V_{RSMX}	RSSI maximum voltage	-10 dBm into RXI		2.7		V
V_{RSMD}	RSSI midrange voltage	-40 dBm into RXI		2.5		V
V_{RSMN}	RSSI minimum voltage	No signal applied		0.2		V
G_{RSSI}	RSSI sensitivity	$(V_{-40dBm} – V_{-50dBm})/10dB$		35		mV/dB
	RSSI accuracy	Deviation from best fit straight line		±3		dB
TRANSMITTER						
F_{TXO}	Transmit input frequency range		5.725		5.850	GHz
P_{TXO}	TX output power at 5.8GHz	Matched into 50 ohms		21		dBm

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
F_{DEV}	Transmit Modulation Deviation	Data Rate=1.1520Mbps Data Rate=1.5360Mbps Data Rate=1.7554Mbps Data Rate=2.0480Mbps		±400 ±512 ±596 ±680		kHz
Z_{TXO}	Output Impedance	at TXO pin		TBD		Ω
BT	Transmit Filter Bandwidth / Symbol Rate Ratio	Data Rate=1.1520Mbps Data Rate=1.5360Mbps Data Rate=1.7554Mbps Data Rate=2.0480Mbps		0.5 0.9 0.8 0.7		
P_{SPUR}	PLL reference spurious	V_{FREF} < 2 Vp-p clip-sine		-70		dBc
P_{LO}	TX LO feed through, LO harmonics and sub-harmonics[2]	P_{TXO} =+21dBm, F_{SPUR} =1/3, 2/3, 4/3, and 5/3 F_{TXO}		-40		dBc
P_{Harm}	TX Harmonics, P_{TXO} =+21dBm	2nd Harmonic		-45		dBc
		3rd Harmonic		-25		dBc
INTERFACE LOGIC LEVELS						
CMOS DIGITAL INPUT PINS (XCEN, RXON, DIN, DATASEL)						
V_{IH}	Input high voltage		VDD*0.7		VDD	V
V_{IL}	Input low voltage		0		VDD*0.3	V
I_B	Input bias current	All states	-5		5	µA
C_{IN}	Input capacitance	1MHz test frequency		4		pF
CMOS DIGITAL OUTPUT PINS (SW_CTRL, RXCLK, DOUT)						
V_{OH}	SW_CTRL output high voltage	Sourcing 5.0mA	VDD-0.4			V
V_{OL}	SW_CTRL output low voltage	Sinking 5.0mA			0.4	V
I_o	SW_CTRL source/sink current		±5.0	±8.0		mA
V_{OH}	RXCLK (recovered clock) output high voltage	Sourcing 0.1mA	VDD–0.4			V
V_{OL}	RXCLK (recovered clock) output low voltage	Sinking 0.1mA			0.4	V
V_{OH}	DOUT (data output) output high voltage	Sourcing 0.1mA	VDD–0.4			V
V_{OL}	DOUT (data output) output low voltage	Sinking 0.1mA			0.4	V
ANALOG OUTPUT PINS (AOUT)						
V_{ODC}	Quiescent output voltage @ AOUT			1.15		V
V_{OPK}	Output voltage swing @ AOUT			0.8		V_{P-P}
3 WIRE SERIAL BUS TIMING						
t_r	CLK input rise time (note 1)				15	ns
t_f	CLK input fall time (note 1)				15	ns
t_{ck}	CLK period		50			ns
t_{ew}	EN pulse width		200			ns
t_l	Delay from last clock rising edge to rise of EN		15			ns

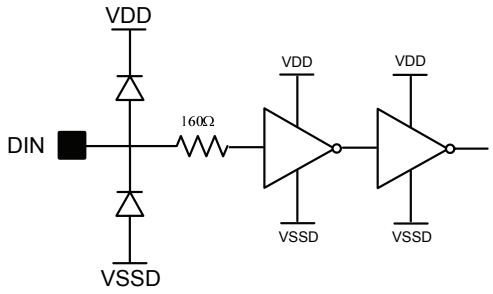
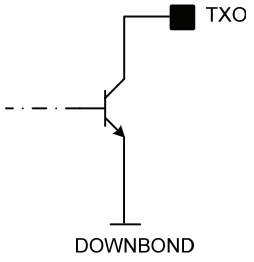
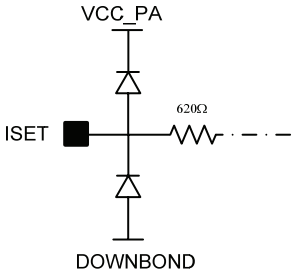
[2] TX frequency = F_{TXO}, TX power = P_{TXO}

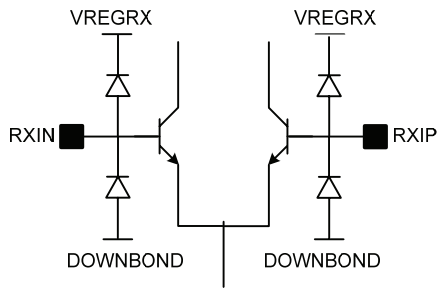
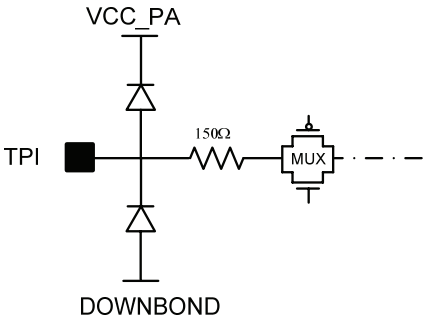
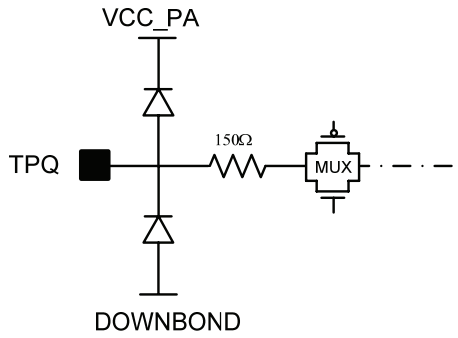
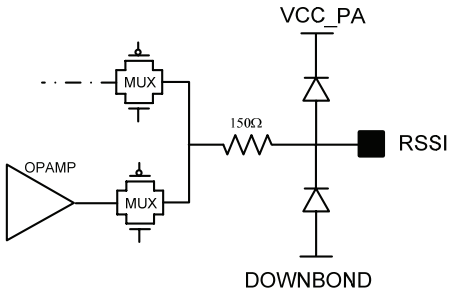
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{se}	EN setup time to ignore next rising CLK		15			ns
t_s	DATA-to-CLK setup time		15			ns
t_h	DATA-to-CLK hold time		15			ns

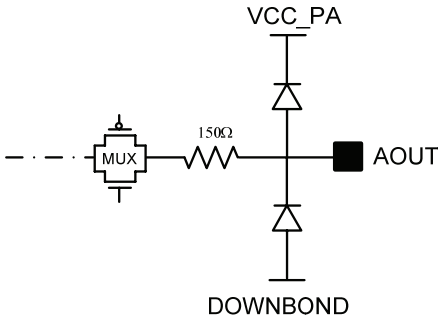
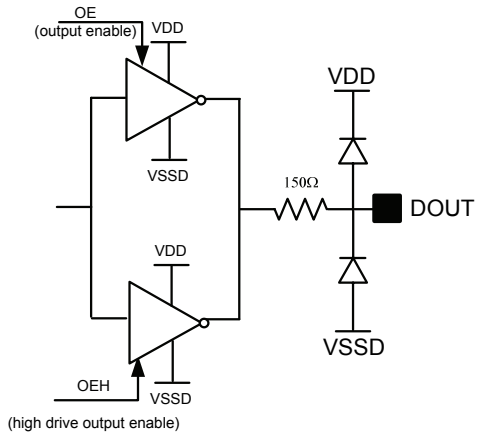
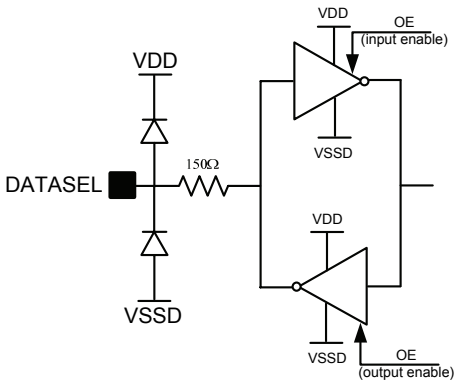
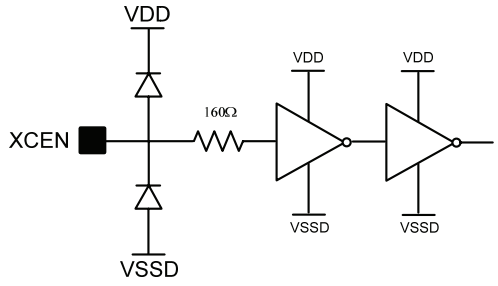
Note 1: Serial I/O clock maximum rise and fall times are based on the minimum clock period. Longer rise and fall times can be accommodated for slower clocks provided the rise and fall times remain less than 20% of the clock period and all set up and hold time minimums are met with respect to the CMOS switching points (V_{IL} MAX and V_{IH} MIN). The serial I/O clock rise and fall times are limited to an absolute maximum of 100ns.

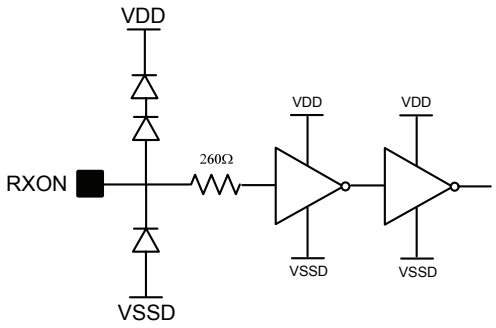
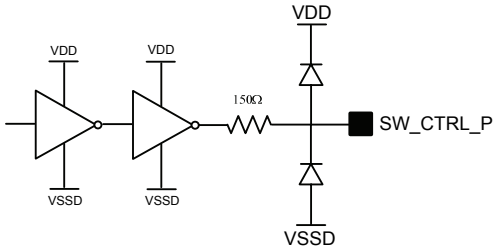
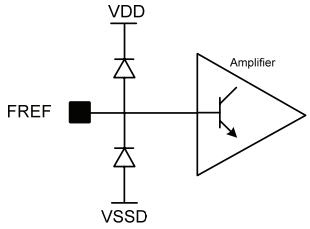
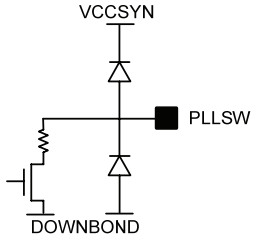
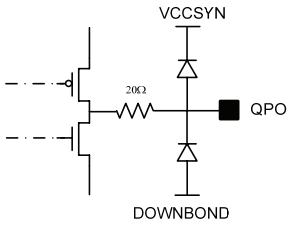
PIN DESCRIPTIONS

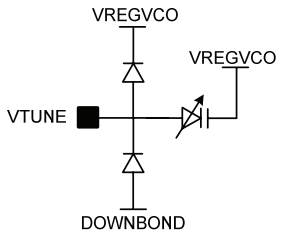
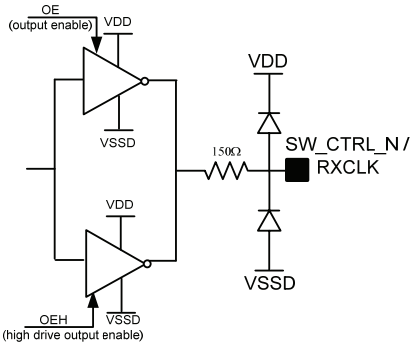
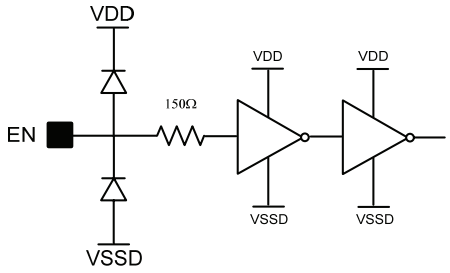
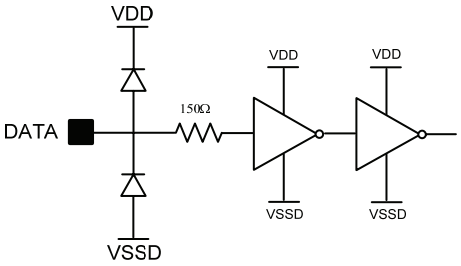
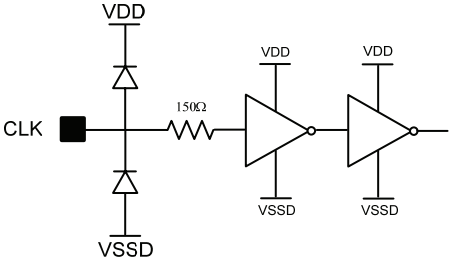
PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
POWER & GROUND				
5	VSSD	GND	Digital ground for all digital I/O circuits and control logic.	**N/A**
9	VDD	PWR/I	3.3VDC power supply input	**N/A**
10	VREG_1P8	PWR/O (Decouple)	1.8VDC regulator output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	**N/A**
11	VBG_1P8	PWR/O (Decouple)	1.13VDC bandgap voltage output. Place capacitor between this pin and ground to decouple (bypass) noise.	**N/A**
13	VCCSYN	PWR/I	2.7VDC power supply input. **Must be connected to VREGPLL pin externally.**	**N/A**
17	VREGVCO	PWR/O (Decouple)	2.5VDC regulator output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	**N/A**
18	VREGPLL	PWR/O (Decouple)	2.7VDC power supply output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	**N/A**
19	VCCPLL	PWR/I (Decouple)	3.3VDC power supply input. Place capacitor between this pin and ground to decouple (bypass) noise.	**N/A**
20	VBG_VCO	PWR/O (Decouple)	1.13VDC bandgap voltage output. Place capacitor between this pin and ground to decouple (bypass) noise	**N/A**
21	VREGLNA	PWR/O (Decouple)	2.7VDC regulator output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	**N/A**
24	VREGRX	PWR/O (Decouple)	2.7VDC regulator output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	**N/A**
25	VBG_RF	PWR/O (Decouple)	Bandgap 1.24V decouple voltage. Decoupled to ground with a capacitor.	**N/A**
26	VREGTX	PWR/I (Decouple)	2.7VDC power supply input. **Must be connected to VREGRX pin externally.**	**N/A**

PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
27	VCCA	PWR/I	3.3VDC power supply input	**N/A**
30	VBG_PA	PWR/O (Decouple)	1.13VDC bandgap voltage output. Place capacitor between this pin and ground to decouple (bypass) noise	**N/A**
31	VCC_PA	PWR/I	Unregulated Battery DC Power Supply Input	**N/A**
32	VREGPA	PWR/O (Decouple)	Programmable 3.6VDC/3.4VDC/3.3VDC regulator output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	**N/A**
33	VREGIF	PWR/O (Decouple)	2.7VDC regulator output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	**N/A**
TRANSMIT PINS				
4	DIN	I (CMOS)	Transmit Data Input.	
28	TXO	O (analog)	TX RF open-collector output. Connect this pin to VREGPA using an (RF blocking) inductor	
29	ISET	I (analog)	TX I_{SET} resistor.	

RECEIVE PINS				
22	RXIN	I (analog)	Differential receive RF Input.	
23	RXIP	I (analog)	Differential receive RF Input.	
34	TPI	I/O (analog)	RX/TX test port. Used to test or apply test signals to both RX and TX sections.	
35	TPQ	I/O (analog)	RX/TX test port. Used to test or apply test signals to both RX and TX sections.	
36	RSSI	I/O (analog)	Receive Signal Strength Indicator. Also used as RX/TX test port.	

37	AOUT	O (analog)	Analog data output.	
38	DOUT	O (CMOS)	Serial digital output after demodulation, bit rate filtering and center data slicing. CMOS levels with controlled slew rates.	
39	DATASEL -or- PLL_Lock	I/O (CMOS)	When TCMOD = 4 or 5, this pin becomes an input and it controls the time constant of the data slicer. When TCMOD = 4 or 5; DATASEL= V_{IH} selects 6uS time constant DATASEL= V_{IL} selects 300uS time constant -else- When TCMOD is not set to value 4 or 5, this pin becomes the PLL Lock/Unlock *output* PLL_Lock = V_{OH} indicates PLL is locked PLL_Lock = V_{OL} indicates PLL is not locked	
MODE CONTROL AND INTERFACE LINES				
1	XCEN	I (CMOS)	Transceiver Enable input. Enables the bandgap reference and voltage regulators when high, enabling normal control functions. Consumes only leakage current in STANDBY mode when low. Operating mode = V_{IH} Standby mode = V_{IL}	

2	RXON	I (CMOS)	TX/RX Control Input. Switches the transceiver between TRANSMIT and RECEIVE mode. Receive mode = V_{IH} Transmit mode = V_{IL}	
3	SW_CTRL_P	O (CMOS)	TR switch control output, positive polarity. Logic high (V_{OH}) while transmitting Logic low (V_{OL}) while receiving	
12	FREF	I (analog)	Input reference frequency.	
14	PLL_SW	O (analog)	Loop filter control switch	
15	QPO	O (analog)	Charge pump output of the phase detector. This is connected to the external PLL loop filter.	

16	VTUNE	I (analog)	VCO Tuning Voltage input from the PLL loop filter. This pin is very sensitive to noise coupling and leakage currents.	
40	SW_CTRL_N -or- RXCLK	O (CMOS)	TR switch control output, negative polarity. V_{OL} while transmitting V_{OH} while receiving -or- Recovered RXCLK clock output is multiplexed in this pin. When configured for RXCLK output, clock pulses may be observed for 6 to 8uS after the falling edge of RXON before settling to logic high (V_{IH}).	
SERIAL BUS SIGNALS				
6	EN	I (CMOS)	Control Bus Enable. Enable pin for the three-wire serial control bus. The control registers are loaded on the rising edge of this signal. Serial control bus data is ignored when this signal is high (V_{IH}).	
7	DATA	I (CMOS)	Serial Control Bus Data.	
8	CLK	I (CMOS)	Serial control bus data is clocked in on the rising edge and only when EN is low.	

FUNCTIONAL DESCRIPTION

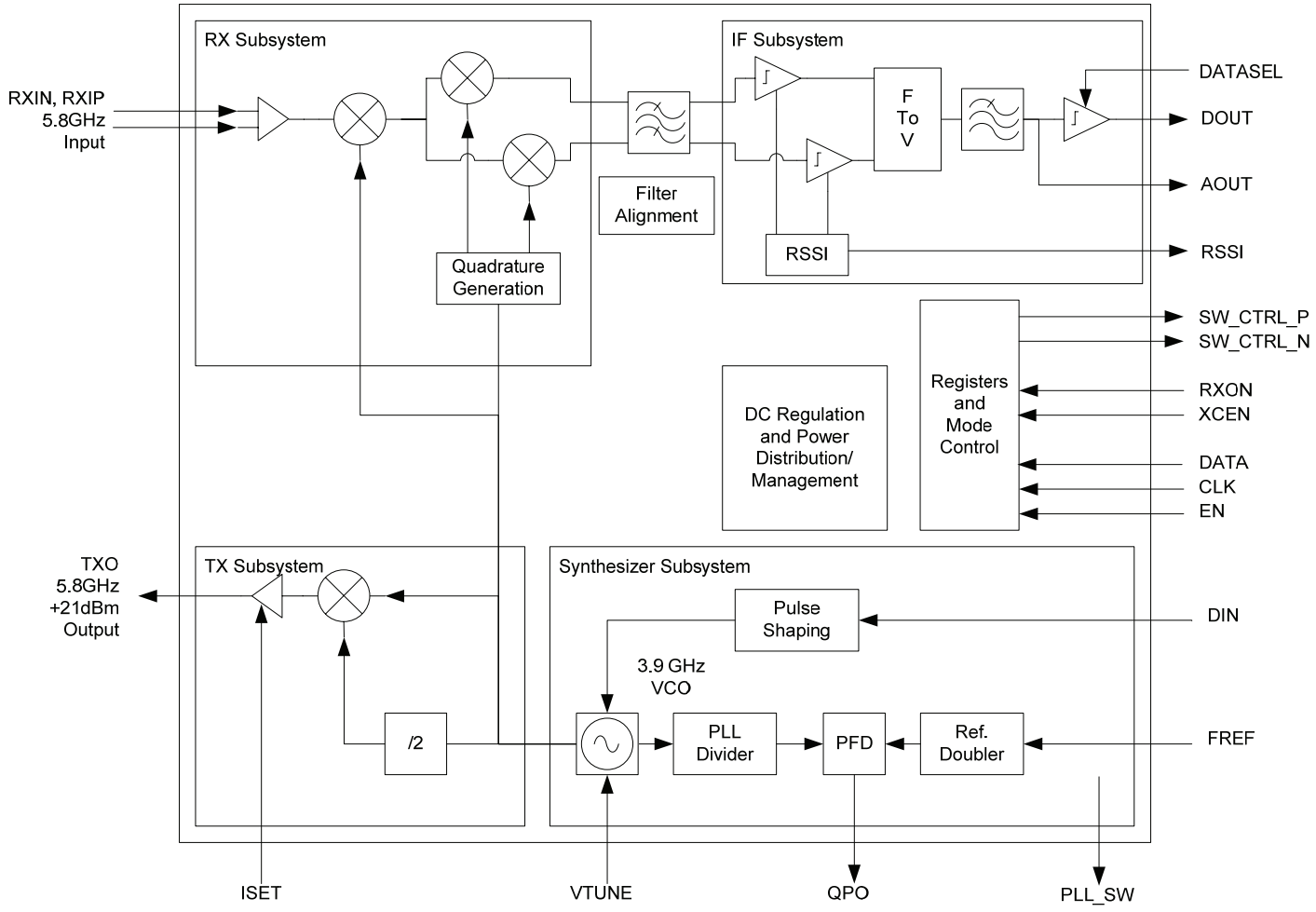


Figure 1: ML5805 Block Diagram

The ML5805 is a single chip wireless digital transceiver. The ML5805 integrates all the frequency generation, receiver and transmit functions requiring only a TR switch to form a complete 5.725 – 5.850GHz ISM band radio. The ML5805 is designed to transmit and receive 576kbps to 2.048Mbps signals using channels spaced from 1.728MHz to 4.096MHz over the 5.725 – 5.850GHz ISM band.

RECEIVER

The ML5805 contains a dual conversion, low-IF receiver with all channel selectivity on-chip. The signal enters through a differential LNA to the 1st mixer which down-converts the 5.8GHz input to a high 1st IF of 1.9GHz, followed by an image reject 2nd mixer that brings this IF signal down to a low IF frequency. On chip IF filtering, gain and demodulation are performed at; a 864KHz IF frequency for the 576kbps and 1.152Mbps data rate, a 1.024MHz IF frequency for the 1.536Mbps data rate or a 2.048MHz IF frequency for the 1.755Mbps and 2.048Mbps data rates.

No external filters or production tuning are required. A post detection filter and data slicer are also provided to complete the receiver. The DATASEL pin allows selection between two different time constants in the data slicer. Rx clock recovery is optionally performed for the 1.152Mbps, 1.536Mbps, 1.755Mpbs, 2.048Mbps data rate to aid those applications using a simple microcontroller based MODEM. A receive signal strength indication (RSSI) signal is also

provided. RSSI (an indication of field strength) can be used by the system to determine transmit power control (conserve battery life) and/or to determine if a given channel is occupied.

AUTOMATIC VCO AND FILTER ALIGNMENT

The VCO and IF filters are calibrated to remove process and temperature variation. IF filter and VCO calibration occurs when the chip is first powered on and at specified intervals during normal operation. This calibration is transparent to the normal operation of the ML5805 and is absorbed in the system timing shown in Figure 2 and Table 2. This self-calibration adjusts:

- VCO center frequency
- Discriminator center frequency
- IF filter center frequency and bandwidth
- Receiver data low-pass filter bandwidth

TRANSMITTER AND PA

The ML5805 transmitter consists of an up-conversion mixer followed by a programmable gain amplifier to allow factory calibration of the output power, and finally a power amplifier (PA). The input data is filtered before being sent to an adjustment free VCO modulator. An FIR Gaussian pulse shaping filter is used followed by DAC and interpolation filter for clock rejection. The output of modulator is up-converted by a mixer and amplified with a PA to deliver 21dBm output power. A complementary T/R switch control output with adjustable timing is provided to control the external T/R switch.

PLL/SYNTHESIZER

A single, on-chip 3.9GHz fractional-N synthesizer is used to generate the receiver LO and transmit carrier. The VCO has an on chip resonator, active devices and tuning circuitry for a completely integrated VCO function. All required DC voltage regulation is within the IC. The PLL center frequency is programmed with a 23 bit word written via the SPI port during either standby or active operation.

A lock detect circuit monitors the state of the PLL loop allowing the PA to be disabled prior to the PLL achieving lock in TRANSMIT mode. In RECEIVE mode, the synthesizer produces a low side LO frequency offset (compared to TX mode) to produce the required IF frequency.

MODES OF OPERATION

The ML5805 has three key modes of operation:

- **STANDBY:** All circuits powered down, except the control interface (static CMOS)
- **RECEIVE:** Receiver circuits active
- **TRANSMIT:** Transmitter circuits active

MODE CONTROL

The two operational modes controlled by RXON are RECEIVE and TRANSMIT. XCEN is the chip enable/disable control pin, which sets the device to either operational or STANDBY modes. The relationship between the parallel control lines and the mode of operation of the IC is summarized in Table 1.

XCEN	RXON	MODE NAME	FUNCTION
0	X	STANDBY	Control interfaces active, all other circuits powered down
1	1	RECEIVE	Receiver time slot
1	0	TRANSMIT	Transmit time slot

Table 1: Modes of Operation

STANDBY MODE

In STANDBY mode, the ML5805 transceiver is powered down. The only active circuits are the control interfaces, which are static CMOS to minimize power consumption. The serial control interface and control registers remain powered up and will accept and retain programming data as long as the VDD and VCCA are present.

RECEIVE MODE

In RECEIVE mode, the received signal at 5.8GHz is down converted, band pass filtered (IF filter), fed to the frequency-to-voltage converter, and then low-pass filtered. The output of the low-pass filter is available at both the AOUT pin and to the on-chip data slicer that produces NRZ digital data presented at the DOUT pin. An RSSI output voltage is also provided.

TRANSMIT MODE

In TRANSMIT mode, the PLL loop is closed to eliminate frequency drift. A closed loop FSK modulator modulates both the VCO and the fractional-N PLL. The VCO is directly modulated with filtered FSK transmit data. The PLL is driven by a sigma-delta modulator, which ensures that the PLL follows the mean frequency of the modulated VCO.

CONTROL INTERFACE

There are two types of Input/output (I/O) signals to control and monitor the ML5805; Discrete I/O and Serial input.

- **Discrete I/O**: XCEN, RXON, SW_CTRL_P, SW_CTRL _N, DATASEL
- **Serial Control Bus**: EN, DATA, CLK

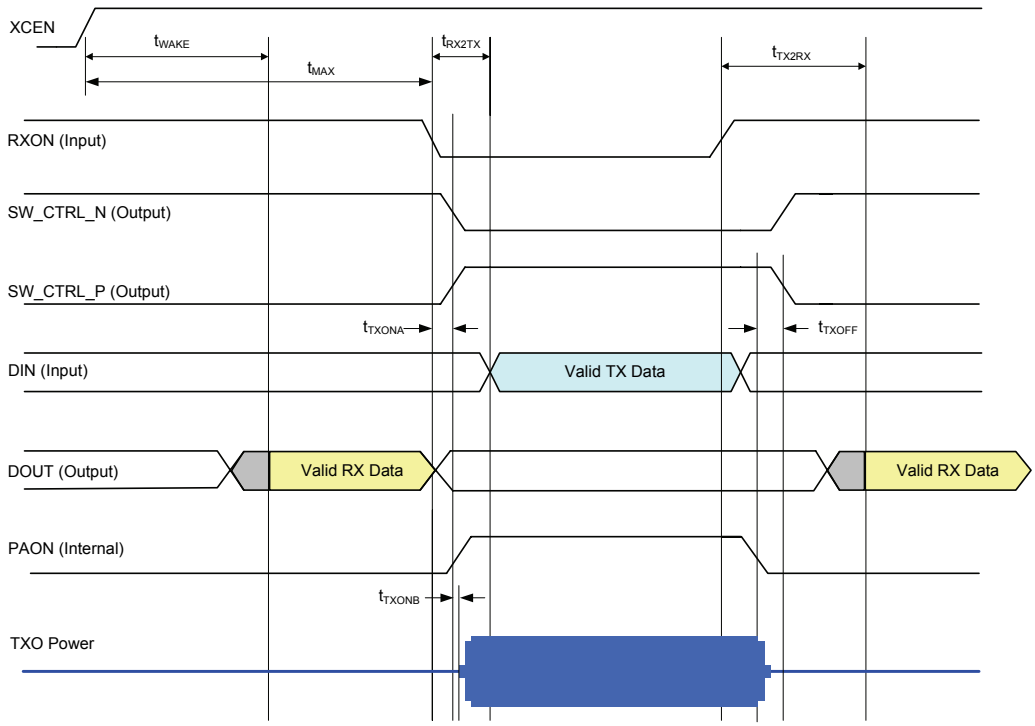
The ML5805 transceiver is used in time division duplex (TDD) mode, where the transceivers at each end of a radio link alternately transmit and receive. Prior to entering receive mode, the ML5805 goes through a 'self-calibration' sequence, where the VCO, IF and data filters are frequency aligned. This occurs in the time period just before the PLL settles to the LO frequency. These calibration cycles are triggered by logic transitions on the control interface. **Figure 2a and 2b** show the normal operating cycle for the ML5805. Figure 2a shows the timing when register variable `PAFIRST` is set to 0, causing the switch control signals to change state before the PA is enabled. Figure 2b shows the timing when register variable `PAFIRST` is set to 1, causing the switch control signals to change state after the PA is enabled.

RF CONTROL: XCEN, RXON, SW_CTRL

The **XCEN** pin enables/disables the ML5805 and places the device in either STANDBY or ACTIVE modes.

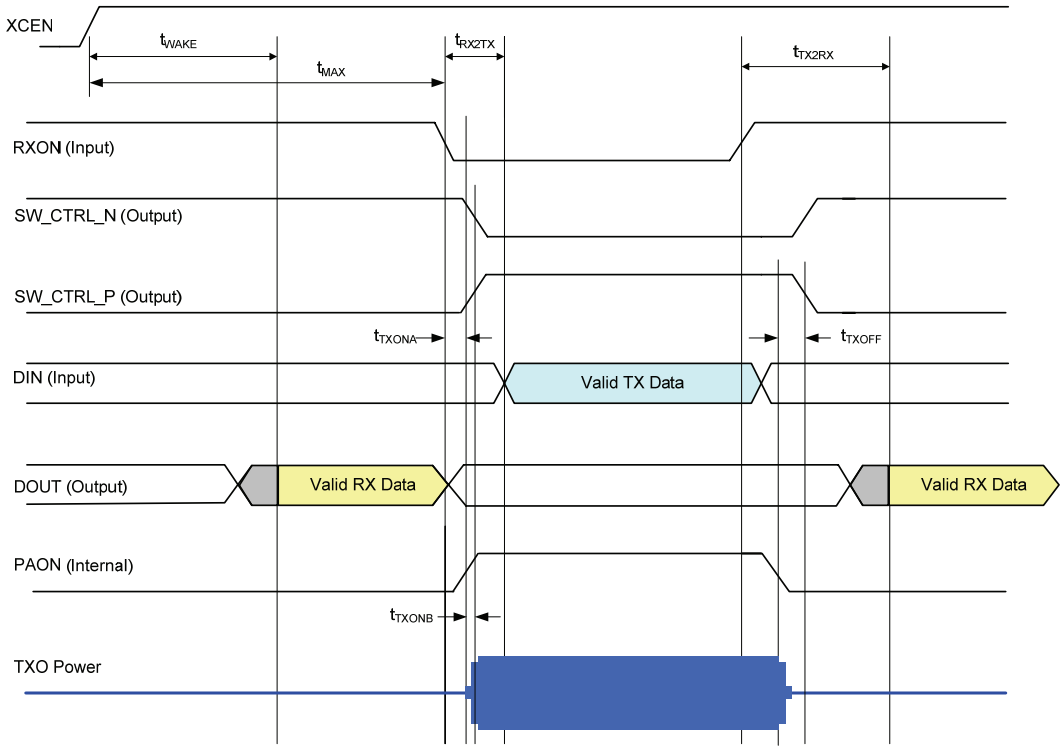
The **RXON** pin determines which active mode the ML5805 is in: RECEIVE or TRANSMIT.

SW_CTRL_P and SW_CTRL_N are complimentary CMOS outputs with 5mA drive capability that control an off-chip T/R switch. They can directly drive PIN diodes. **SW_CTRL_P** outputs a logic high when RXON is asserted low and a logic low at all other times. The time delays between RXON and SW_CTRL_P are programmable are shown in Figure 2 and Table 3. These outputs are inhibited when the PLL is not locked.



PAFIRST = 0 (The external switch controls SW_CTRL_P/N are switched before PA is turned on).

Figure 2a: Control Timing for TDD Operation, PAFIRST = 0



PAFIRST = 1 (PA turns on before external switch controls, SW_CTRL_P/N are switched.

Figure 2b: Control Timing for TDD Operation, PAFIRST = 1

Table 2 shows the minimum time required between control interface transitions.

SYMBOL	PARAMETER		WORST CASE TIMING	UNITS
t_{WAKE}	Time from XCEN asserted to valid RECEIVE data out		325	µsec
t_{FH}	Time from rising edge of Serial Bus EN to valid RECEIVE data out (channel scan mode, one channel hop, PLL re-locking triggered by rising EN).	NOIVCOC = 0	110	µsec
		NOIVCOC = 1	55	
t_{TX2RX}	Time from rising edge of RXON to valid RECEIVE data out	NOIVCOC = 0	90	µsec
		NOIVCOC = 1	80	
t_{RX2TX}	Time from falling edge on RXON to start of valid data on DIN pin. Some RF energy will be present on TXO during this period but PAON will be unasserted		70	µsec
t_{TXONA}	For the case where PAFIRST = 0: t_{TXONA} defines the time between falling edge of RXON and rising edge of RF output power For the case where PAFIRST = 1: t_{TXONA} defines the time between falling edge of RXON and rising edge of SW_CTRL_P t_{TXONA} = 44µS + TTXONA * 8 / f_{ref} where TTXONA is an integer with range from 0 to 63		44 to 85	µsec
t_{TXONB}	For the case where PAFIRST = 0: t_{TXONB} defines the time between rising edge of SW_CTRL_P and rising edge of RF output power For the case where PAFIRST = 1: t_{TXONB} defines the time between rising edge of RF output power and rising edge of SW_CTRL_P t_{TXONB} = 4.2µS + TTXONB * 8 / f_{ref} where TTXONB is an integer with range from 0 to 31		4.2 to 24.2	µsec
t_{TXOFF}	Time between falling edge of RF output power and falling edge of SW_CTRL_P signal t_{TXOFF} = 3.5µS + TTXOFF * 40 / f_{ref} where TTXOFF is an integer with range from 0 to 3		3.5 to 13.5	µsec

Table 2: Transceiver Control Interface Timing (using default register values)

Channel Scan Timing in Receive Mode

To implement channel scanning, the ML5805 is kept in RECEIVE mode (XCEN and RXON high) and the PLL is reprogrammed to select a different RF channel. A VCO and filter calibration cycle is initiated periodically after the serial bus writes to the register controlling the PLL. Any serial bus writes to the other registers (while XCEN = V_{IL} (0)) will trigger a complete calibration cycle. Non-PLL register writes (R0 to R4) are only performed when XCEN = V_{IL} (0). Otherwise, unstable operation will occur. Signal diagram for channel scanning is shown in **Figure 3.**

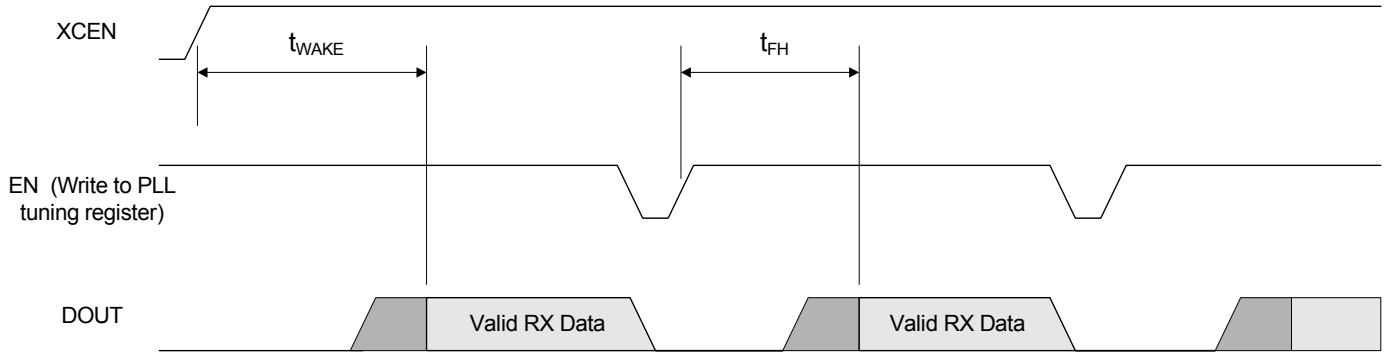


Figure 3: Control Timing when Channel Scanning

TRANSMIT & RECEIVE DATA INTERFACES

There are two sets of transmit and receive data interfaces for the ML5805:

- **Baseband Data:** DIN, DOUT, AOUT, RXCLK, FREF, RSSI
- **RF Data:** RXIN, RXIP, TXO

Please refer to application schematic in **Figure 4** for recommended component values.

BASEBAND DATA: DIN, DOUT, AOUT, RXCLK

The **DIN** pin is a CMOS logic level serial data input for 2-FSK modulation on the radio channel. This DIN pin drives data bits into the transmit modulator. There is no re-timing of the chips, so the transmitted 2-FSK chips take their timing from the DIN pin.

The **DOUT** pin is a corresponding CMOS level digital data output. In DS-FSK mode the ML5805 is designed to operate as a Direct Sequence Spread Spectrum FSK transceiver in the 5.725 – 5.850GHz ISM band. The chip rate, bit rate and spreading code are determined in the baseband processor, and the FM deviation and transmit filtering are determined in the ML5805 transceiver.

Setting the **AOUT** bit in the serial register turns the **AOUT** pin into a buffered, single ended output from the data filter. This can be used to drive an off chip data slicer, or an ADC input for a DSP data slicer.

When using the digital output DOUT, FM demodulation, data filtering and center slicing take place in the ML5805 receiver. A clock recovery circuit at the data slicer output extracts the receiver clock **RXCLK** for those applications that do not have access to clock recovery circuitry.

The **FREF** pin is the master reference frequency (f_{ref}) input for the transceiver. It supplies the frequency reference for the RF channel frequency and the on-chip filter tuning. The FREF pin is a clipped sine input with on-chip biasing resistors. It can be driven by an AC coupled sine-wave or a CMOS[3] logic source. FREF is used as a calibration frequency and as a timing reference in the control circuits. The reference source must be accurate to 20 PPM.

The **RSSI** (Received Signal Strength Indicator) pin supplies a voltage that indicates the amplitude of the received RF signal. The **RSSI** voltage is proportional to the logarithm of the received power level. It can be connected to the input of an ADC on the baseband IC, and is used during channel scanning to detect clear channels on which the radio can transmit.

RF DATA: RXIN, RXIP, TXO

The **RXIN** and **RXIP** receive input and the **TXO** transmit output are the only RF I/O pins. The RXIN and RXIP pins requires a single-ended to differential conversion from a 50Ω input impedance and a matching network for best input noise figure, and the TXO pin also requires a matching network for maximum power output into 50Ω (see **Figure 4**).

[3] For $V(f_{ref})$ > 1.5Vp-p, the level of the reference spurious response (f_{TX} +/- f_{ref}) to increases in proportion to $V(f_{ref})$. $V(f_{ref})$ levels that exceed 2.0Vp-p will cause the typical reference spur to be greater than -70dBc.

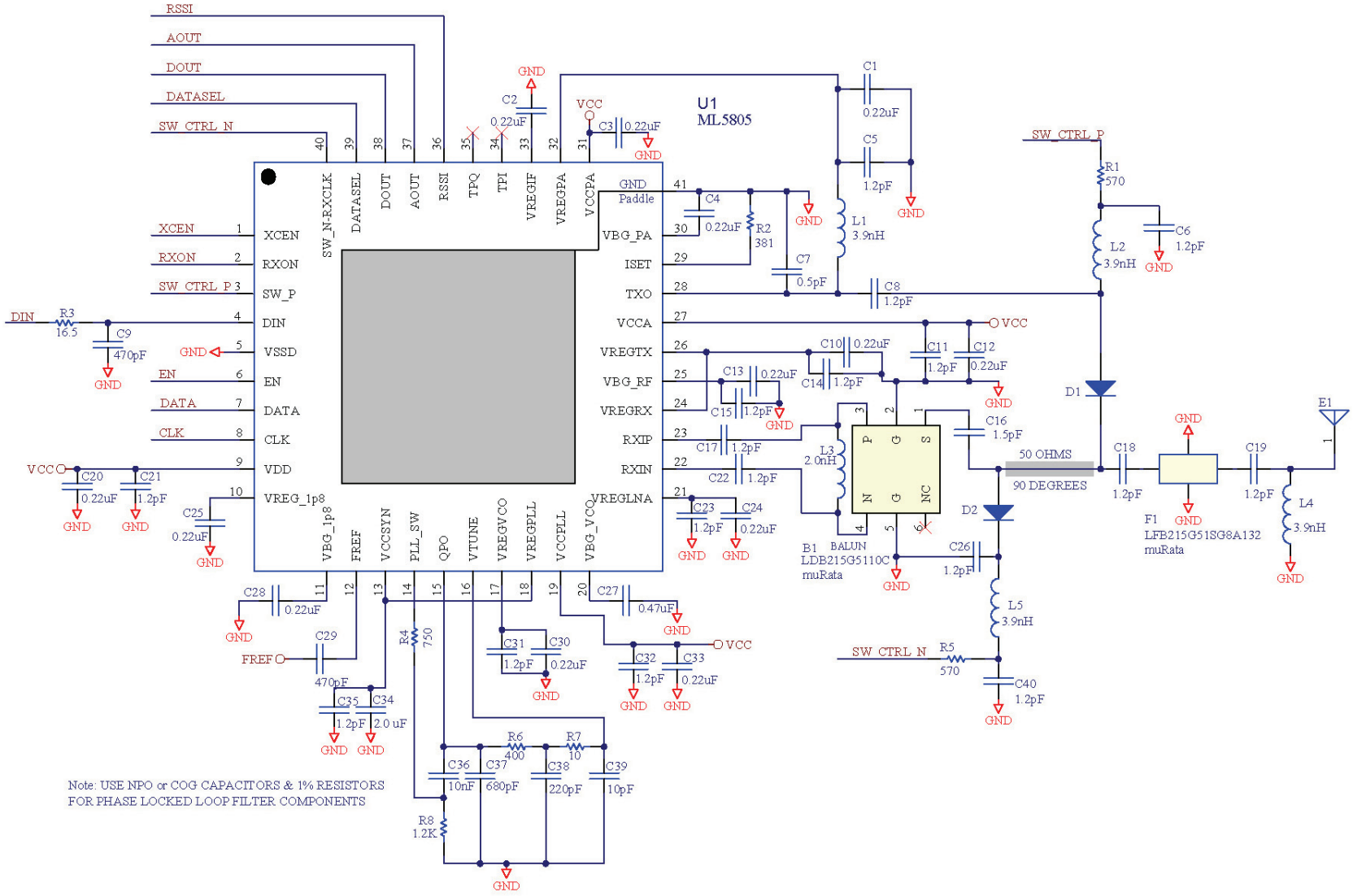


Figure 4 ML5805 Application Schematic

SERIAL BUS CONTROL: EN, DATA, CLK

A 3-wire serial interface is used for programming the ML5805 configuration registers, which control device mode of operation, pin functions, PLL and reference dividers, internal test modes and filter alignment. Data words are entered beginning with the MSB. The 24 bit configuration register word consists of 5 bit address and 16 bit data fields.. When the address field has been decoded the destination register is loaded on the rising edge of EN. **Note: Providing less than 24 bits of data will result in unpredictable behavior when EN goes high.**

Data and clock signals are ignored when EN is high. When EN is low, data on the DATA pin is clocked into a shift register by rising edges on the CLK pin. The information is loaded into the addressed latch when EN returns high. This serial interface bus is an industry standard bus commonly found on PLL devices. It can be efficiently programmed by either byte or 24-bit word oriented serial bus hardware. The data latches are implemented in CMOS and use minimal power when the bus is inactive (see **Figure 5** and **Table 3**).

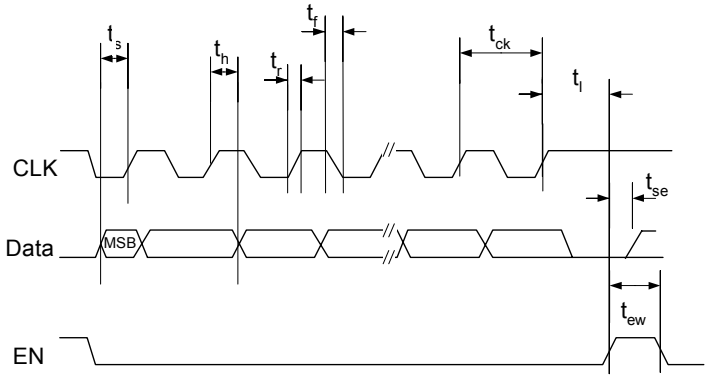


Figure 5: Serial Bus Timing Diagram

SYMBOL	PARAMETER	MIN	MAX	UNITS
BUS CLOCK (CLK)				
t_r	Clock input rise time (Note 1)		15	ns
t_f	Clock input fall time (Note 1)		15	ns
t_{ck}	Clock period	50		ns
ENABLE (EN)				
t_{ew}	Minimum pulse width	200		ns
t_l	Delay from last clock rising edge to rise of EN	15		ns
t_{se}	Enable set up time to ignore next rising clock	15		ns
BUS DATA (DATA)				
t_s	Data to clock set up time	15		ns
t_h	Data to clock hold time	15		ns

Table 3: Serial Bus Timing Specifications

Note 1: Serial I/O clock maximum rise and fall times are based on the minimum clock period. Longer rise and fall times can be accommodated for slower clocks provided the rise and fall times remain less than 20% of the clock period and all set up and hold time minimums are met with respect to the CMOS switching points (V_{IL} MAX and V_{IH} MIN). The serial I/O clock rise and fall times are limited to an absolute maximum of 100ns.

SERIAL FREQUENCY WORD AND CONFIGURATION REGISTERS

SERIAL WORD TRANSACTION TYPES AND CONFIGURATION REGISTER MAP

Table 4: Serial Word Format (Frequency or Configuration)

Bit				
23	**22**	**21**	**20:16**	**15:0**
0	PLL FREQUENCY WORD			
1	RESET	WEN	ADDRESS	CDATA (see Table 5)

Table 5: Configuration Register Map showing ROM Default Values *

Register	BIT															
(default)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	TCMOD			RATE			UWD POL	PLLUL ACT	RESERVED	RESERVED	RESERVED		RESERVED			
(0x010E)	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0
R1	CDRDLY				CDR EN	TXPADRV			RSSI DLY	PA FIRST	TXFILT EDGE	TXFILT POL	NOI VCOC	UW1 ERR	IFREGSEL	
(0x8080)	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R2	RESERVED		AOUT EN	TTXONB					TTXOFF		TTXONA					
(0x4080)	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R3	RESERVED								DIVBASEOFFS				RESERVED		RESERVED	
(0x8886)	1	0	0	0	1	0	0	0	1	0	0	0	0	1	1	0
R4	MDCALV								RESERVED							
(0XC008)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

* Grey **items are reserved.**

SERIAL WORD DEFINITIONS

There are two types of serial words used, specified by the state of Bit 23. Bit 23=0 sets the serial word type to 'frequency' and Bit 23=1 specifies the serial transaction type as a 'configuration word'.

Bit	Definition
23	Specifies whether this serial transaction is type PLL frequency or type configuration register. Value: 0 — PLL frequency specification word Value: 1 — Configuration register specification word
22:0	Data

PLL Frequency Word

The PLL Frequency Word may be sent during standby (XCEN=0) or operation (XCEN=1).

Bit	Value	Definition
23	0	Specifies PLL frequency word
22:20	IPART	Integer part of the PLL programming variable
19:0	FPART	Fractional part of the PLL programming variable

The frequency of the channel is controlled by the configuration PLL Frequency Word defined above and the input reference frequency. The expression for the channel frequency is

$$f_{ch} = 3 f_{ref} \left[H + I + \frac{N}{2^{20}} \right] \text{ MHz,}$$

where;

N = FPART (the fractional part of the DSM programming value),

I = IPART (the integer part of the DSM programming value),

H = DIVBASEOFFS + 147 for f_{ref} = 12.288MHz (RATE = 2, 3, or 4),

DIVBASEOFFS + 130 for f_{ref} = 13.824MHz (RATE = 0 or 1),

DIVBASEOFFS = a variable defined in Register 3 (default = 8),

RATE = a variable defined in Register 0 (default = 0),

f_{ref} = 12.288MHz or 13.824MHz.

Configuration Register Serial Word

The configuration registers are written only during standby mode (XCEN=0). These data registers are volatile and will erase when VCC is removed. The format is shown below.

Bit	Value	Definition
23	1	This is a configuration register transaction.
22	RESET	<table><tr><th>Value</th><th>Definition</th></tr><tr><td>0</td><td>Normal operation</td></tr><tr><td>1</td><td>Perform reset operation. *Must be asserted on first serial transfer.*</td></tr></table>
21	1	Must be set to write to register.
20:16	ADDRESS	Register address (value = 0, 1, 2, 3, or 4)
15:0	CDATA	Configuration Register data.

All registers (R0, R1, R2, R3, and R4) will be loaded with default values and need to be initialized by the system base band hardware for the data rate used. See **Table 6** following this section.

REGISTER 0

Register 0 is a special register because some of the hardware is controlled *directly* from this register. Since those specific bits are connected physically to active hardware, they must always be written *first* after power on. If Register 0 is not initialized first by the base band hardware, the ML5805 will not operate correctly.

<table>
<tr><th>Bit</th><th>Variable</th><th>Default</th><th>Definition</th></tr>
<tr><td>15:13</td><td>TCMOD</td><td>0</td><td>Selects one of eight possible data slicer time constant combinations.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0</td><td>Forces 300µs</td></tr>
<tr><td>1</td><td>Forces 6µs</td></tr>
<tr><td>2</td><td>Forces 3µs</td></tr>
<tr><td>3</td><td>Forces 2µs</td></tr>
<tr><td>4</td><td>External selection between 300µs and 6µs</td></tr>
<tr><td>5</td><td>External selection between 300µs and 3µs</td></tr>
<tr><td>6</td><td>Use Unique Word Detect mode and forces 6µs</td></tr>
<tr><td>7</td><td>Use Unique Word Detect mode and forces 3µs</td></tr>
</table></td></tr>
<tr><td>12:10</td><td>RATE</td><td>0</td><td>Selects one of eight possible bit rate combinations. Selected bit rates are dependent on external crystal frequency supplied
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0</td><td>576kbps (@13.824MHz)</td></tr>
<tr><td>1</td><td>1,152kbps (@13.824MHz)</td></tr>
<tr><td>2</td><td>1,536kbps (@12.288MHz)</td></tr>
<tr><td>3</td><td>1,755kbps (@12.288MHz)</td></tr>
<tr><td>4</td><td>2,048kbps (@12.288MHz)</td></tr>
<tr><td>5</td><td>Not defined.</td></tr>
<tr><td>6</td><td>Not defined.</td></tr>
<tr><td>7</td><td>Not defined.</td></tr>
</table></td></tr>
<tr><td>9</td><td>UWDPOL</td><td>0</td><td>1: invert the default DECT Unique Word (UWD) pattern
0: use the default DECT Unique Word (UWD) pattern</td></tr>
<tr><td>8</td><td>PLLULACT</td><td>1</td><td>
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0</td><td>PA will always turn on</td></tr>
<tr><td>1</td><td>If the PLL does not lock, the PA does not turn on</td></tr>
</table></td></tr>
<tr><td>7</td><td>(spare)</td><td>0</td><td>Spare bit</td></tr>
<tr><td>6</td><td>RESERVED</td><td>0</td><td>RESERVED</td></tr>
<tr><td>5:4</td><td>RESERVED</td><td>0</td><td>RESERVED</td></tr>
<tr><td>3:0</td><td>RESERVED</td><td>0xE</td><td>RESERVED</td></tr>
</table>

REGISTER 1

Bit	Variable	Default	Definition
15:12	CDRDLY	8	Recovered Data Clock Delay (RDC_{delay}) is the delay between the rising edge of RX data and the rising edge of the recovered RX data clock. The CDRDLY variable sets this delay as follows; RDC_{delay} = CDRDLY / (2 x f_{ref}) [default RDC_{delay} = 325 ns]
11	CDREN	0	1: enable RDC_{delay} 0: RDC_{delay} is not used
10:8	TXPADRV	0	Current Setting for PA. Value / Definition 0 / Bias current setting = 63uA 1 / Bias current setting = 280uA 2 / Bias current setting = 368uA 3 / Bias current setting = 605uA 4 / Bias current setting = 605uA 5 / Bias current setting = 822uA 6 / Bias current setting = 930uA 7 / Bias current setting = 1177uA
7	RSSIDLY	1	1: RSSI output is masked until the PLL finished tuning 0: RSSI will function during the PLL tuning change time
6	PAFIRST	0	1: the PA turns on before the external switch controls change 0: the external switch controls change before the PA is turned on
5	TXFILTEDGE	0	1: clock TX data on the falling edge of the reference clock 0: clock TX data on the rising edge of the reference clock
4	TXFILTPOL	0	1: invert the TX data before filtering 0: no data inversion applied
3	NOIVCOC	0	1: no incremental VCO calibration, only incremental IF calibration 0: perform both VCO and IF incremental calibrations
2	UW1ERR	0	1: one error is allowed for the DECT unique word detection 0: zero errors are allowed for the DECT unique word detection
1:0	IFREGSEL	0	IF and PA Circuit Regulator Voltages Value / Definition 0 / Regulator output = 3.3V 1 / Not valid 2 / Regulator output = 3.44V 3 / Regulator output = 3.67V

REGISTER 2

Bit	Variable	Default	Definition
15:14	RESERVED	1	RESERVED
13	AOUTEN	0	1: use the analog output 0: use the digital output
12:8	TTXONB	0	PA on to T/R switch delay (see Table 2)
7:6	TTXOFF	2	PA off to T/R switch delay (see Table 2)
5:0	TTXONA	0	RX to TX delay time (see Table 2)

REGISTER 3

Bit	Variable	Default	Definition
15:12	RESERVED	0	RESERVED
11:8	RESERVED	0	RESERVED
7:4	DIVBASEOFFS	8	Offset to integer portion of PLL programming
3:2	RESERVED	1	RESERVED
1:0	RESERVED	2	RESERVED

REGISTER 4

Bit	Variable	Power-on Default	Rate Variable	Definition
15:8	MDCALV	0x38 0x45 0x5D 0x60 0x50 0x00 0x00 0x00	0 1 2 3 4 5 6 7	Frequency Modulation Deviation value. Small adjustments to MDCALV will tune the modulation spectrum. Note: At power-on, the MDCALV default value corresponding to the RATE variable of Register0 is written to this register. Factory optimized values for MDCALV are shown in Table 6.
7:0	RESERVED	0		RESERVED

RECOMMENDED CONFIGURATION REGISTER VALUES

Register	Data Rate (kbps)				
	576	1152	1536	1755	2048
R0	0x017A	0x057A	0x097A	0x0D7A	0x117A
R1	0xF482	0xF482	0xC482	0x8482	0x8482
R2	0xC000	0xC000	0xC000	0xC000	0xC000
R3	0x0080	0x0080	0x0080	0x0080	0x0080
R4	0x3600	0x4800	0x5D00	0x6400	0x5200

Table 6 Recommended register values for each data rate

Please consult with RFMD application engineering for updates to these values or if you have special configuration requirements. The recommended register settings in Table 6 initialize the ML5805 as follows;

- **DOUT enabled (AOUT disabled),**
- **force 300μs data slicer time constant,**
- **CDR disabled,**
- **RSSI muting while PLL is not locked,**
- **3.44V PA regulator,**
- **minimum RX to TX delay,**
- **minimum PA on to T/R switch delay and,**
- **minimum PA off to T/R switch delay.**

TYPICAL PERFORMANCE DATA

Unless otherwise specified T_A = 25°C and the supply voltage is VCC=3.3V, VCC_PA=3.6V, R_{ISET}=381 Ohm, FREF=12.288MHz, DATA RATE=1.536Mbps, all measurements are normalized to the IC pins.

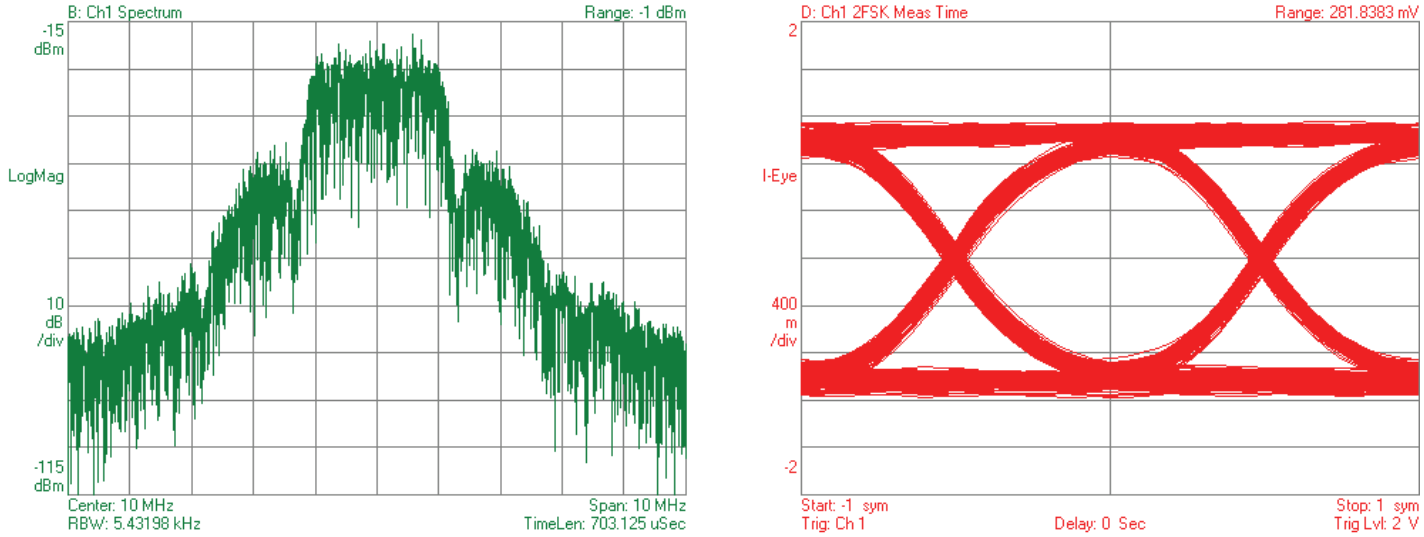


Figure 3 TX output spectrum and eye diagram for 2.048Mbps, PN20 digital mode.

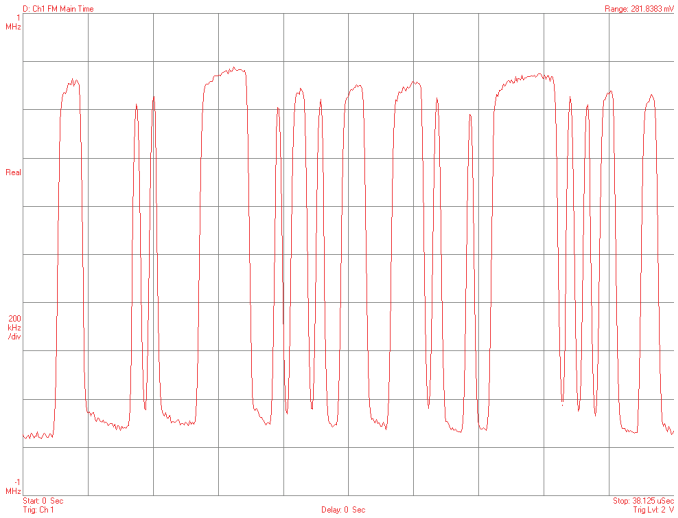


Figure 4 Measured frequency deviation in the time domain for 2.048Mbps, PN20 digital mode.

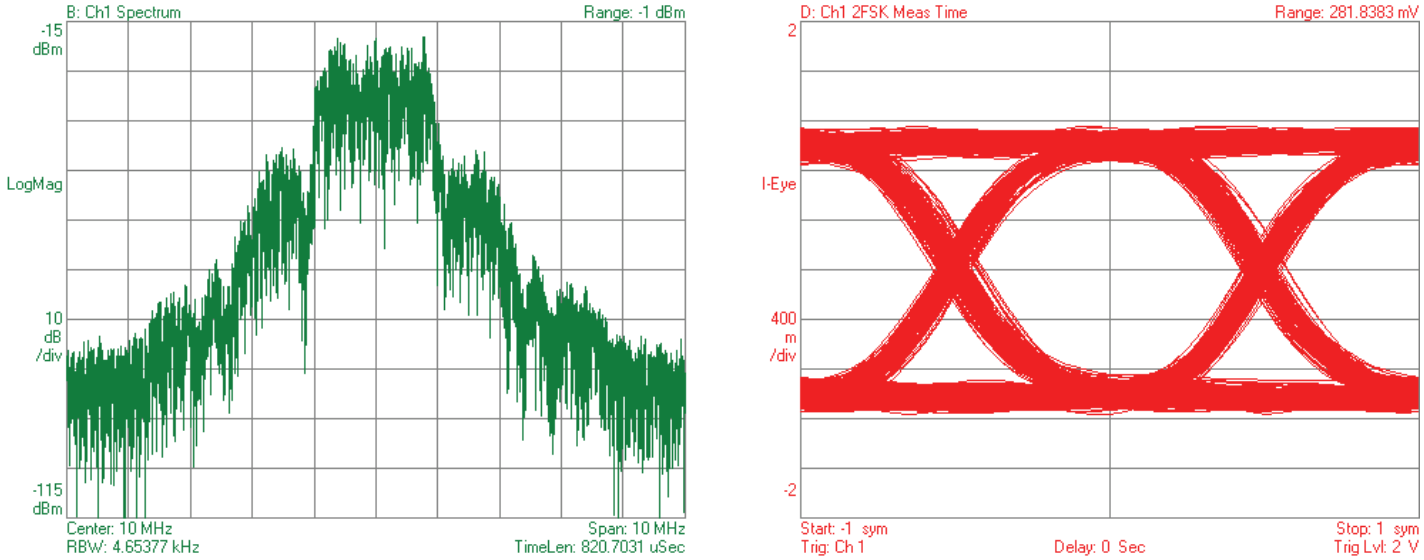


Figure 5 TX output spectrum and eye diagram for 1.755Mbps, PN20 digital mode.

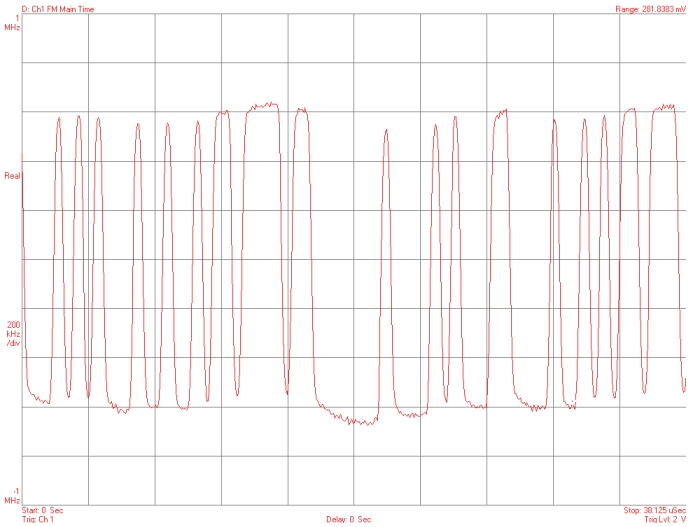


Figure 6 Measured frequency deviation in the time domain for 1.755Mbps, PN20 digital mode.

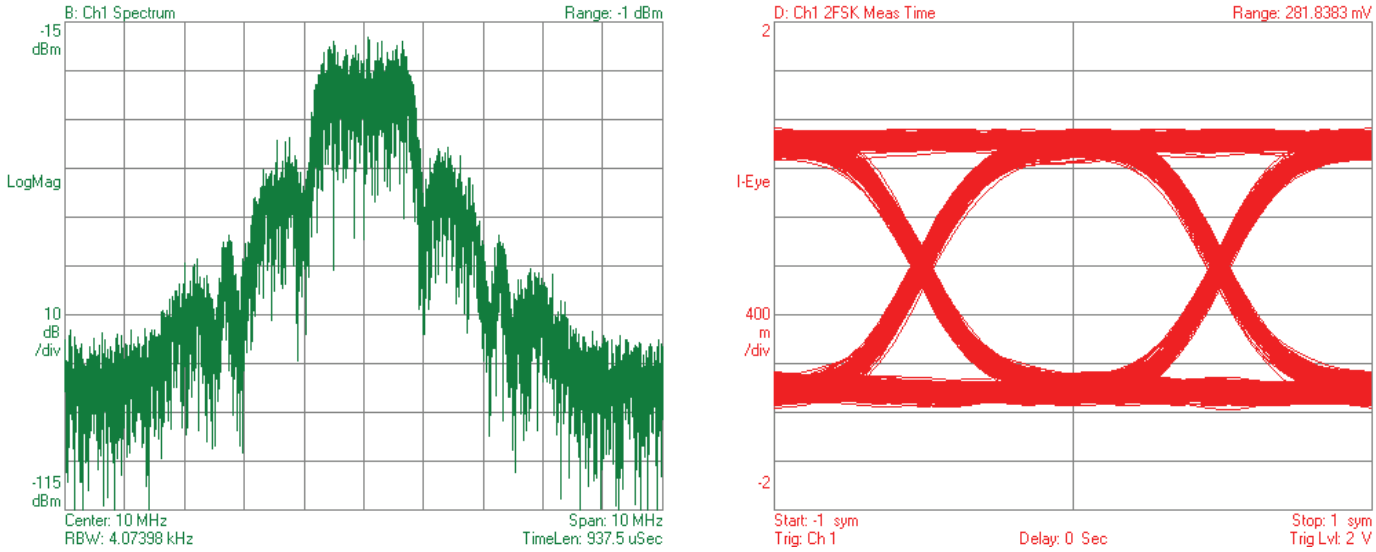


Figure 7 TX output spectrum and eye diagram for 1.536Mbps, PN20 digital mode.

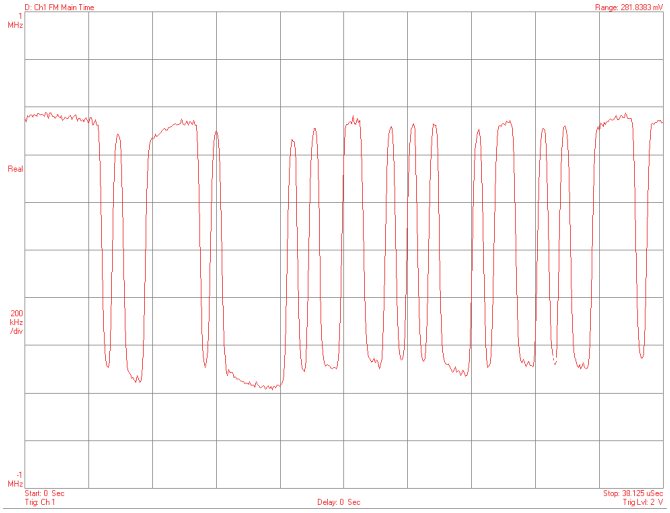


Figure 8 Measured frequency deviation in the time domain for 1.536Mbps, PN20 digital mode.

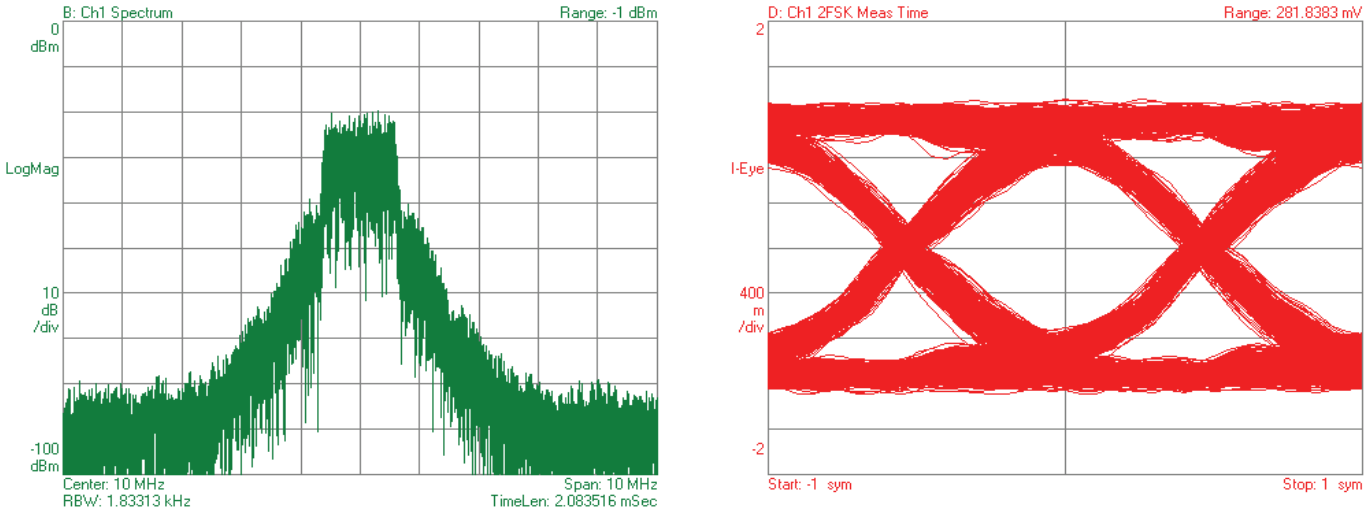


Figure 9 TX output spectrum and eye diagram for 1.152Mbps, PN20 digital mode.

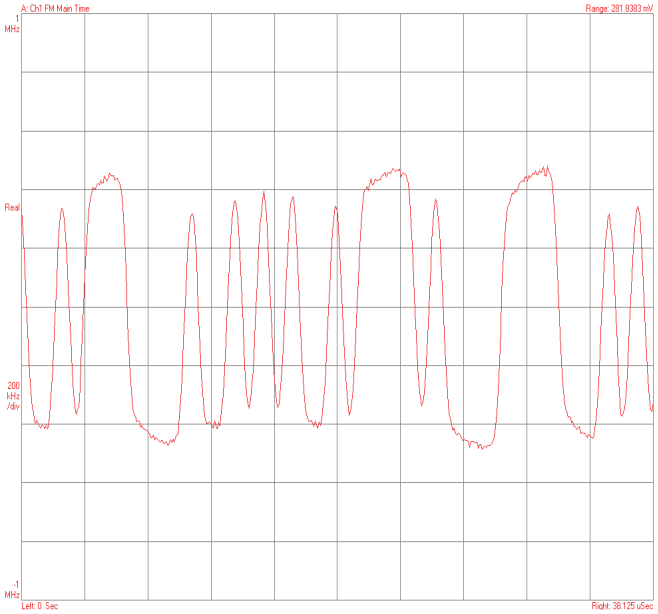


Figure 10 Measured frequency deviation in the time domain for 1.152Mbps, PN20 digital mod

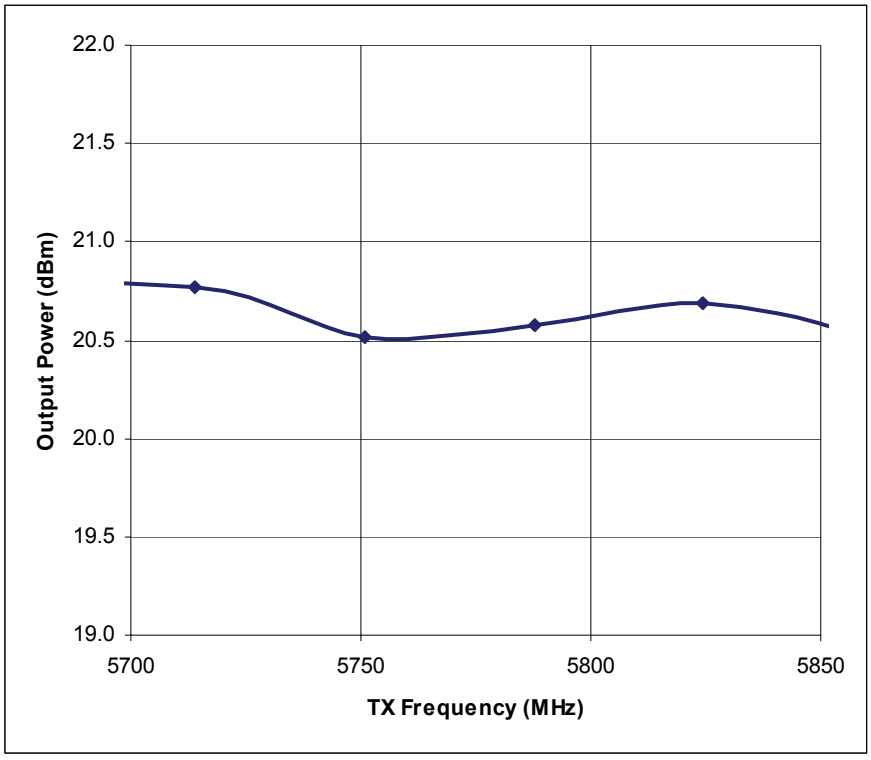


Figure 11 Transmit Power .vs. Frequency

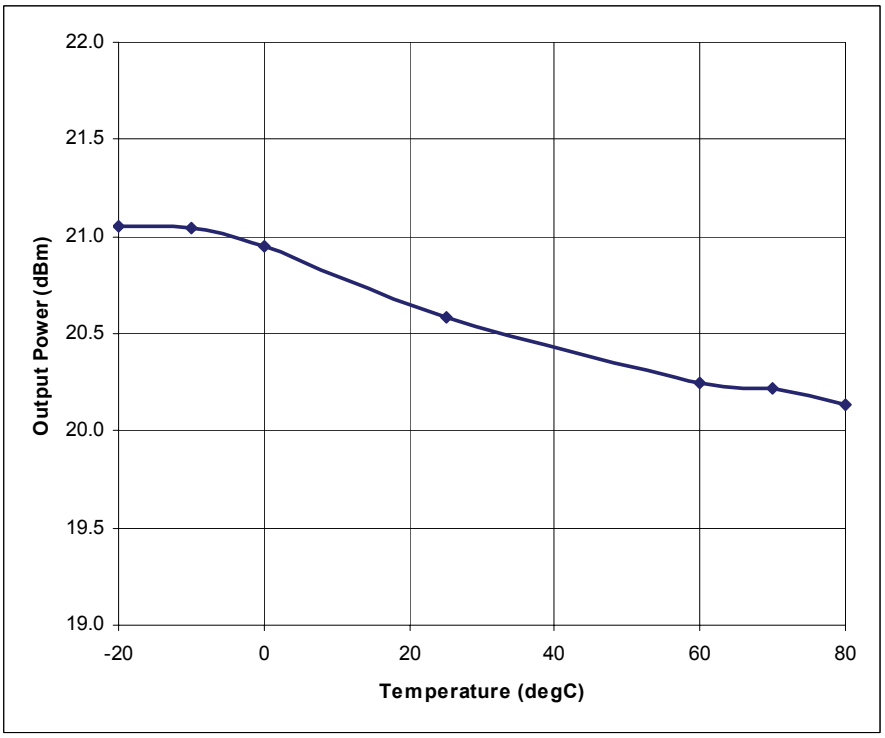


Figure 12 Transmit Power .vs. Temperature

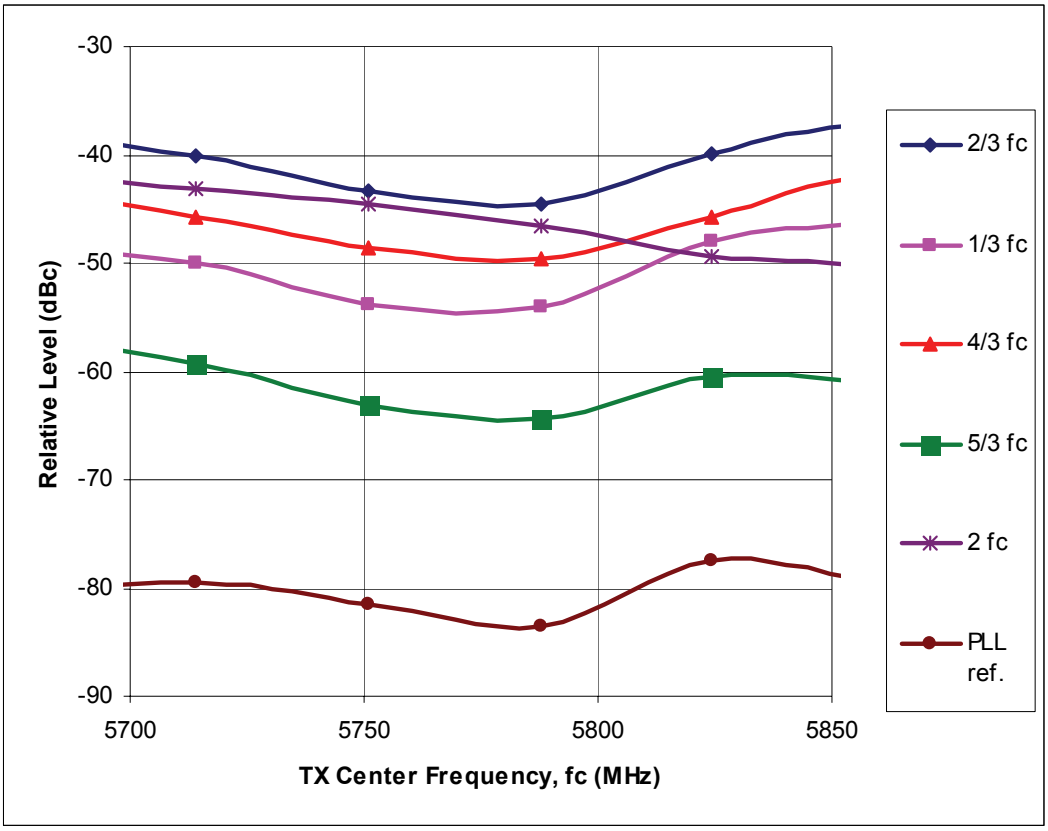


Figure 13 Tx Harmonics and Sub-Harmonics .vs. Frequency

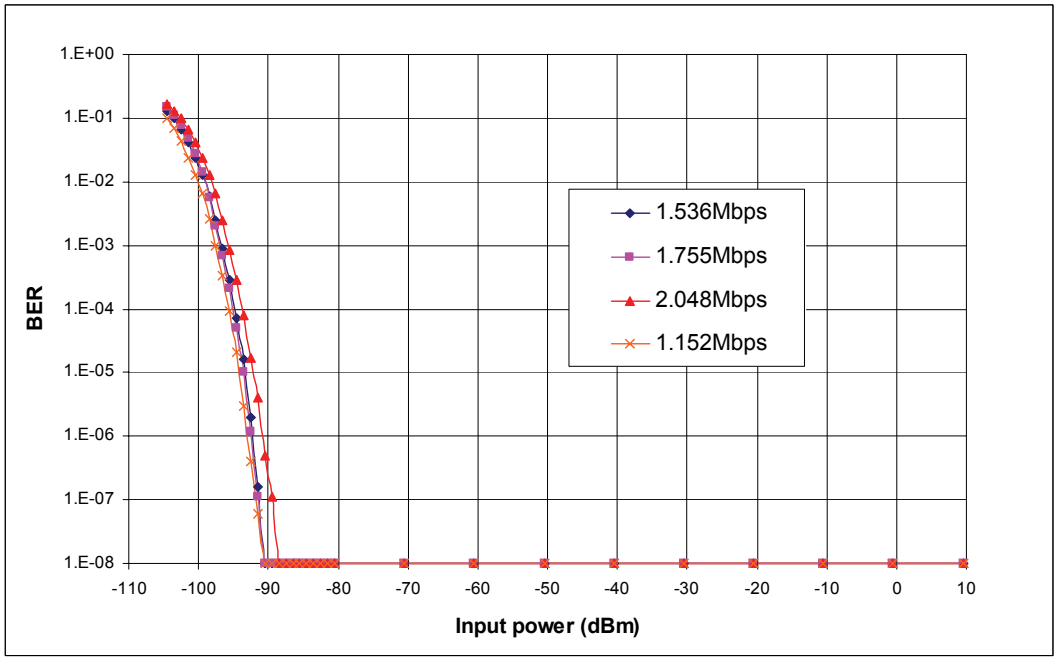


Figure 14 Bit Error Rate .vs. Data Rate

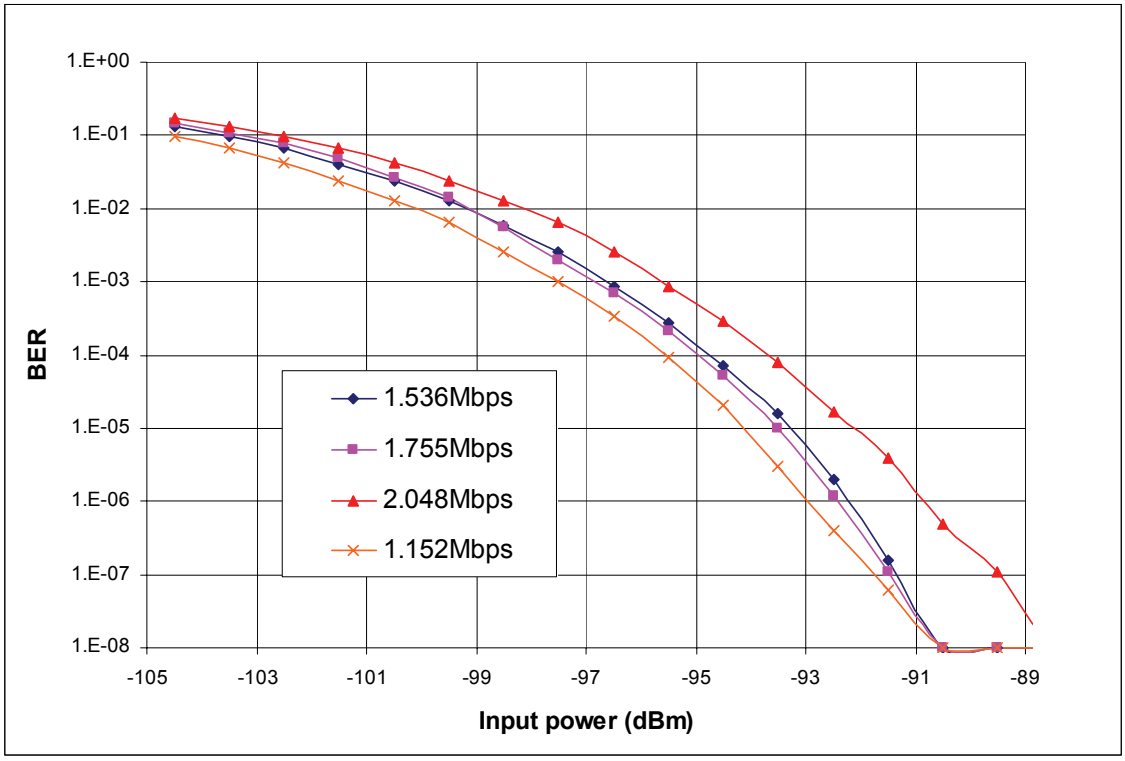


Figure 15 Bit Error Rate .vs. Data Rate

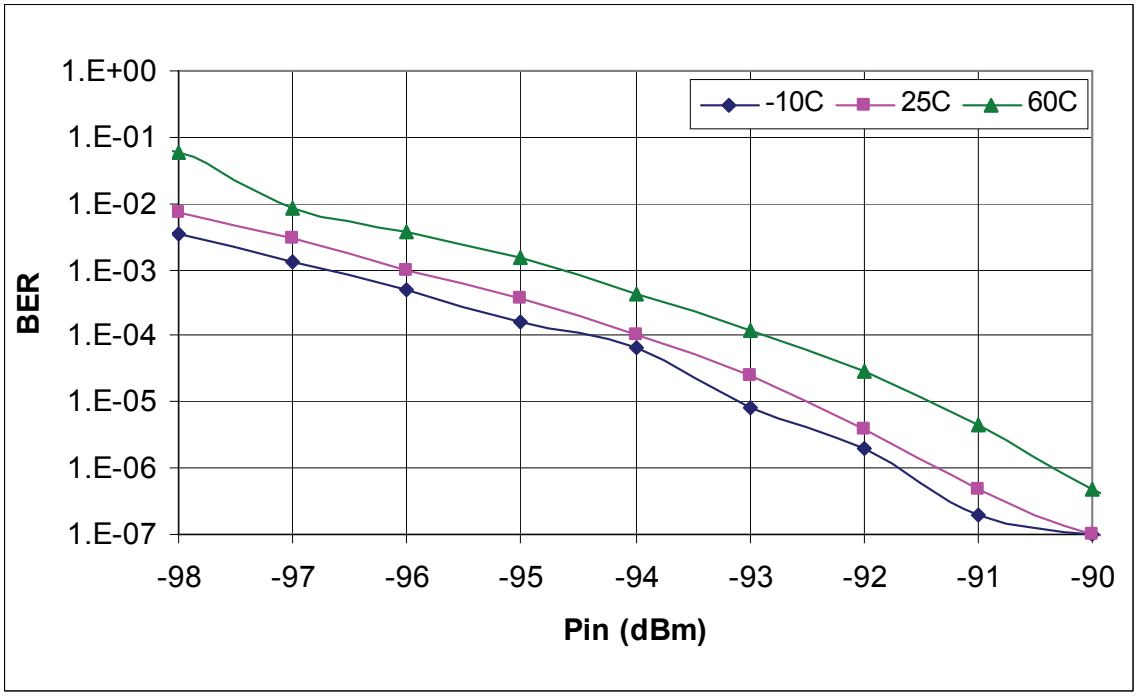


Figure 16 Bit Error Rate .vs. Temperature (2.048Mbps)

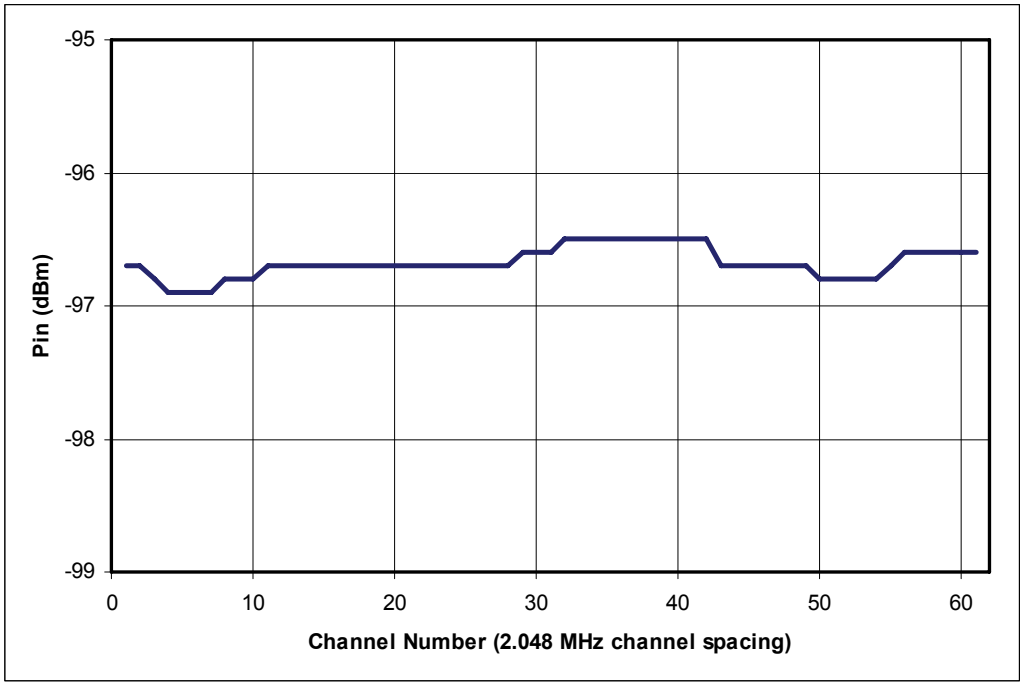


Figure 17 0.10% Bit Error Rate .vs. Channel (1.536Mbps)

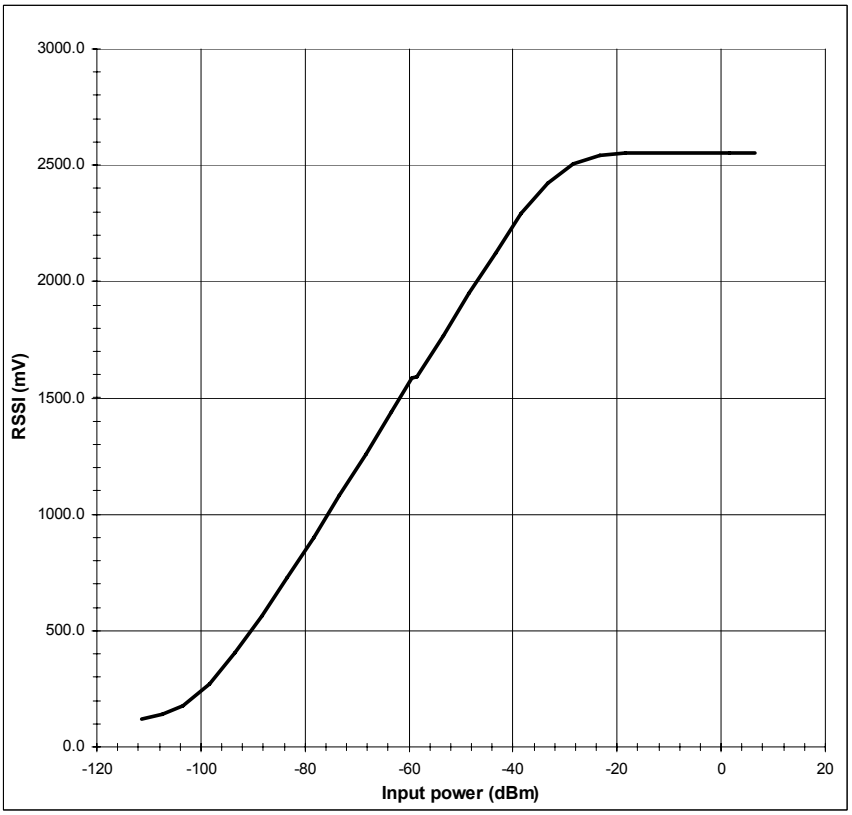
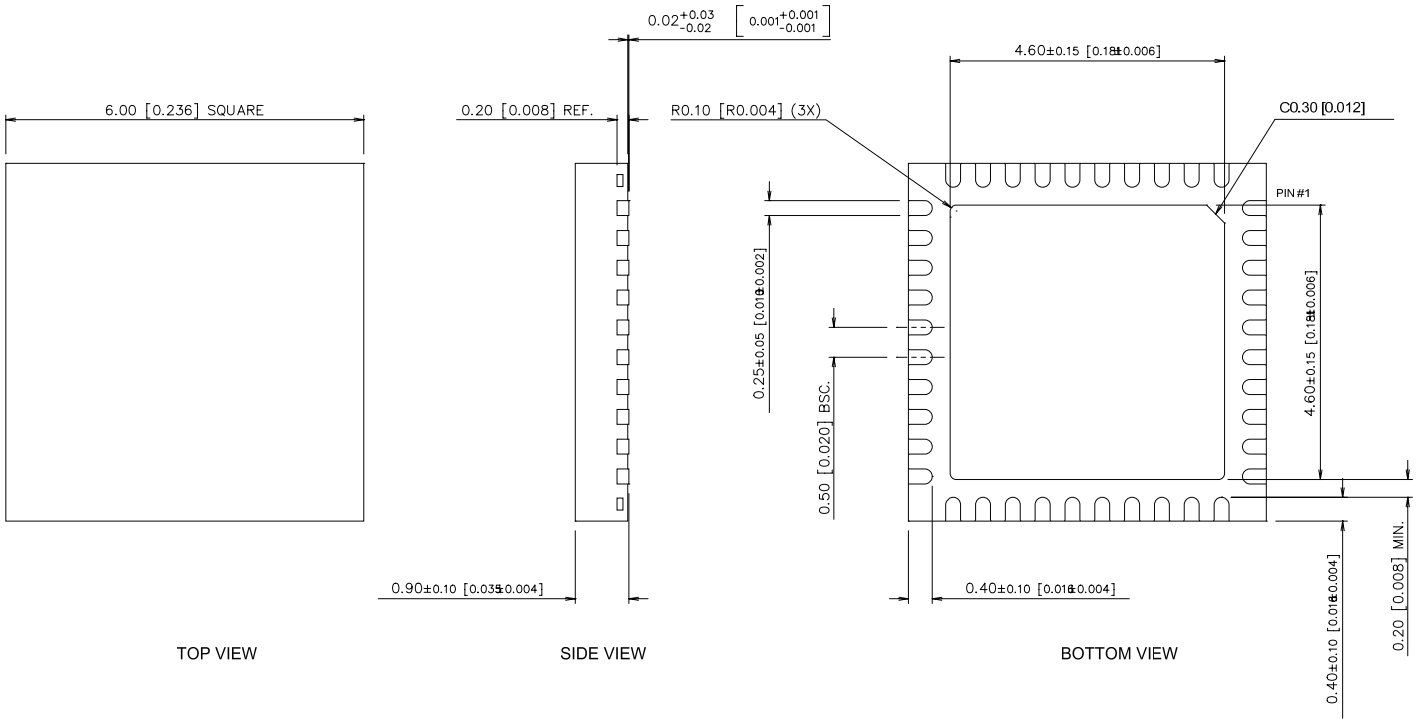


Figure 18 RSSI .vs. Input Power

PHYSICAL DIMENSIONS



NOTES:
1. JEDEC REFERENCE: MO-220 (VJJD-4)
2. ALL DIMENSIONS ARE IN MM [INCHES].
3. GENERAL TOLERANCE: ±0.05 [±0.002]

Figure 19: 40 Pin QFN Package Dimensions

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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5.844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714; 7,076,217. Other patents are pending.

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