FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11440-2E

MEMORY

CMOS

128 M-BIT (4-BANK × 1 M-WORD × 32-BIT) SINGLE DATA RATE I/F FCRAM™

Consumer/Embedded Application Specific Memory for SiP

MB81ES123245-10

■ DESCRIPTION

The Fujitsu MB81ES123245 is a Single Data Rate Interface Fast Cycle Random Access Memory (FCRAM*) containing 134,217,728 memory cells accessible in a 32-bit format. The MB81ES123245 features a fully synchronous operation referenced to a positive clock edge whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence.

The MB81ES123245 is utilized using a Fujitsu advanced FCRAM core technology and designed for low power consumption and low voltage operation than regular synchronous DRAM (SDRAM) .

The MB81ES123245 is dedicated for SiP (System in a Package) , and ideally suited for various embedded/ consumer applications including digital AVs and image processing where a large band width and low power consumption memory is needed.

* : FCRAM is a trademark of Fujitsu Limited, Japan.

■ PRODUCT LINEUP

Parameter		MB81ES123245-10
Clock Frequency (Max)	CL = 2	54 MHz
	CL = 3	108 MHz
Burst Mode Cycle Time (Min)	CL = 2	18.5 ns
	CL = 3	9.2 ns
Access Time from CLK (Max)	CL = 2	9 ns
	CL = 3	7 ns
Operating Current (Max) (64 page length)		35 mA
Power Down Mode Current (Max) (I_{DD2PS})		0.5 mA
Self-Refresh Current (Max)	Tj = +35 °C Max	200 µA

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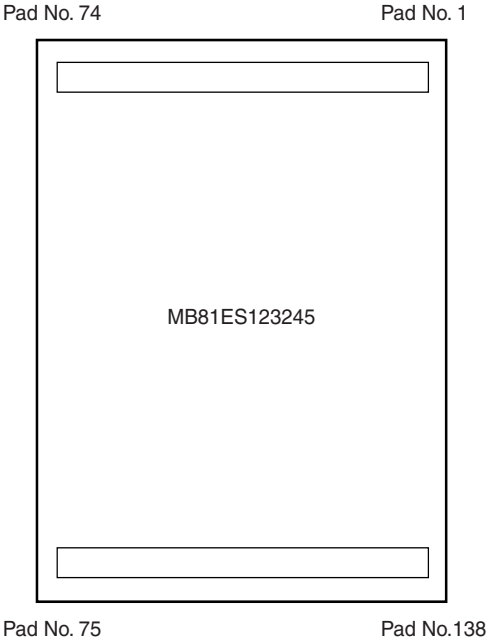
■ FEATURES

- 1 M word × 32 bit × 4 banks organization
- Low power supply
  - V_{DD} : +1.7 V to +1.9 V
  - V_{DDQ} : +1.7 V to +1.9 V
- 1.8V CMOS I/O interface
- 4 K refresh cycles every 64 ms
- Auto- and Self-refresh
- Four banks operation
- Programmable burst type, burst length, and CAS Latency
- Burst read/write operation and burst read/single write operation capability
- Programmable page length function
- Programmable Partial Array Self-Refresh (PASR)
- Programmable Driver Strength (DS)
- Deep power down mode
- Junction temperature (Tj) : −25 °C to +95 °C
- CKE power down mode
- Output enable and input data mask
- Self burn-in function for TEST
- Built In Self Test (BIST) function for TEST

■ PAD LAYOUT

Pad No.		Pad No.	
1	V_{DD}	75	V_{DD}
2	V_{SS}	76	V_{SS}
3	—	77	—
4	V_{SS}	78	—
5	—	79	—
6	—	80	—
7	—	81	—
8	DQ_{15}	82	—
9	—	83	—
10	DQ_{14}	84	—
11	—	85	—
12	—	86	DQ_{23}
13	DQ_{12}	87	—
14	—	88	DQ_{22}
15	DQ_{13}	89	—
16	—	90	—
17	—	91	DQ_{20}
18	DQ_{11}	92	—
19	—	93	DQ_{21}
20	DQ_{10}	94	—
21	V_{DDQ}	95	—
22	V_{SSQ}	96	DQ_{19}
23	DQ_8	97	—
24	—	98	DQ_{18}
25	DQ_9	99	V_{DDQ}
26	—	100	V_{SSQ}
27	A_0	101	DQ_{16}
28	A_1	102	—
29	A_2	103	DQ_{17}
30	A_3	104	—
31	A_4	105	—
32	A_5	106	DQM_1
33	A_6	107	—
34	A_7	108	DQM_0
35	A_8	109	V_{DD}
36	A_9	110	V_{SS}
37	A_{10}	111	DQM_2
38	V_{SS}	112	—
39	V_{DD}	113	DQM_3
40	CKE	114	—
41	CLK	115	—
42	CSB	116	DQ_{25}
43	RASB	117	—
44	CASB	118	DQ_{24}
45	WEB	119	V_{SSQ}
46	BA_0	120	V_{DDQ}
47	BA_1	121	DQ_{26}
48	A_{11}	122	—
49	A_{12}	123	DQ_{27}
50	A_{13}	124	—
51	V_{SS}	125	—
52	—	126	DQ_{29}
53	DQ_1	127	—
54	—	128	DQ_{28}
55	DQ_0	129	—
56	V_{SSQ}	130	—
57	V_{DDQ}	131	DQ_{30}
58	DQ_2	132	—
59	—	133	DQ_{31}
60	DQ_3	134	—
61	—	135	—
62	—	136	—
63	DQ_5	137	V_{SS}
64	—	138	V_{DD}
65	DQ_4		
66	—		
67	—		
68	DQ_8		
69	—		
70	DQ_7		
71	—		
72	V_{SS}		
73	V_{SS}		
74	V_{DD}		

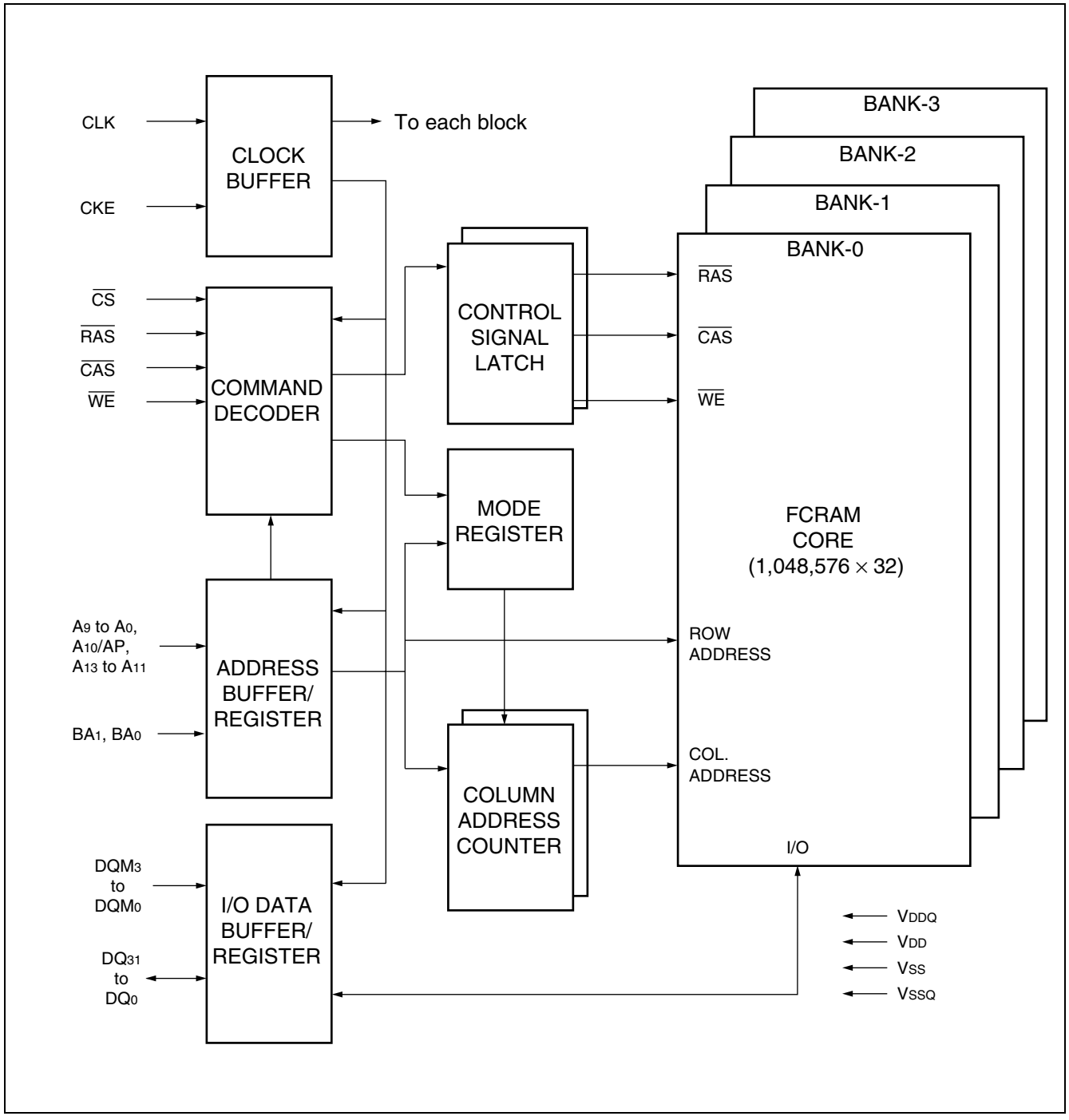


■ PAD DESCRIPTIONS

Symbol	Function			
V_{DDQ}, V_{DD}	Supply Voltage			
DQ_{31} to DQ_0	Data I/O			
V_{SSQ}, V_{SS}	Ground			
$\overline{WE}$ (WEB)	Write Enable			
$\overline{CAS}$ (CASB)	Column Address Strobe			
$\overline{RAS}$ (RASB)	Row Address Strobe			
$\overline{CS}$ (CSB)	Chip Select			
BA_1, BA_0	Bank Select (Bank Address)			
AP	Auto Precharge Enable			
A_{13} to A_0 *	Address Input		Row	Column
		256 page	A_{11} to A_0	A_7 to A_0
		128 page	A_{12} to A_0	A_6 to A_0
		64 page	A_{13} to A_0	A_5 to A_0
CKE	Clock Enable			
CLK	Clock Input			
DQM_3 to DQM_0	Input Mask/Output Enable			
—	Don't Bond			

* : A_{12} must be connected to V_{SS} in 256 page length mode. A_{13} must be connected to V_{SS} in 256 page length mode and 128 page length mode.

■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE *1

1. COMMAND TRUTH TABLE *2, *3, *4

Function	Command	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A_{10} (AP)	Address (Except for A_{10})
		n-1	n							
Device Deselect *5	DESL	H	X	H	X	X	X	X	X	X
No Operation *5	NOP	H	X	L	H	H	H	X	X	X
Burst Stop *6, *7	BST	H	X	L	H	H	L	X	X	X
Read *7	READ	H	X	L	H	L	H	V	L	Column Address
Read with Auto-precharge *7	READA	H	X	L	H	L	H	V	H	Column Address
Write *7	WRIT	H	X	L	H	L	L	V	L	Column Address
Write with Auto-precharge *7	WRITA	H	X	L	H	L	L	V	H	Column Address
Bank Active *8	ACTV	H	X	L	L	H	H	V	Row Address	
Precharge Single Bank	PRE	H	X	L	L	H	L	V	L	X
Precharge All Banks	PALL	H	X	L	L	H	L	X	H	X
Mode Register Set *9, *10	MRS	H	X	L	L	L	L	V	V	V

*1 : V = Valid, L = V_{IL}, H = V_{IH}, X = either V_{IL} or V_{IH}.
Row Address
256 page length : A_{11} to A_0
128 page length : A_{12} to A_0
64 page length : A_{13} to A_0
Column Address
256 page length : A_7 to A_0
128 page length : A_6 to A_0
64 page length : A_5 to A_0

*2 : All commands assume no CSUS command on previous rising edge of clock.

*3 : All commands are assumed to be valid state transitions.

*4 : All inputs are latched on the rising edge of clock.

*5 : NOP and DESL commands have the same effect. Unless specifically noted, NOP will represent both NOP and DESL command in later description.

*6 : When the current state is idle and CKE = L, BST command will represent Deep Power Down command. Refer to “1. COMMAND TRUTH TABLE” and “3. CKE TRUTH TABLE”.

*7 : READ, READA, WRIT, WRITA and BST commands should only be issued after the corresponding bank has been activated (ACTV command) . Refer to “■STATE DIAGRAM”.

*8 : ACTV command should only be issued after corresponding bank has been precharged (PRE or PALL command) .

*9 : Required after power up. Refer to “22. POWER-UP INITIALIZATION” in section “■FUNCTIONAL DESCRIPTION”.

*10 : MRS command should only be issued after all banks have been precharged (PRE or PALL command) . Refer to “■STATE DIAGRAM”.

2. DQM TRUTH TABLE

Function	Symbol	CKE		DQMi *1, *2
		n-1	n	
Data Write/Output Enable	ENBi *1	H	X	L
Data Mask/Output Disable	MASKi *1	H	X	H

*1 : i = 0, 1, 2, 3

*2 : DQM_0, DQM_1, DQM_2 and DQM_3 controls DQ_7 to DQ_0, DQ_{15} to DQ_8, DQ_{23} to DQ_{16}, and DQ_{31} to DQ_{24}, respectively.

3. CKE TRUTH TABLE *1

Current State	Function	Command	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A_{10} (AP)	Address (Except for A_{10})
			n-1	n							
Bank Active	Clock Suspend Mode Entry *2	CSUS	H	L	X	X	X	X	X	X	X
Any (Except Idle)	Clock Suspend Continue *2	—	L	L	X	X	X	X	X	X	X
Clock Suspend	Clock Suspend Mode Exit	—	L	H	X	X	X	X	X	X	X
Idle	Auto-refresh Command *3	REF	H	H	L	L	L	H	X	X	X
Idle	Self-refresh Entry *3, *4	SELF	H	L	L	L	L	H	X	X	X
Self Refresh	Self-refresh Exit *5	SELFX	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X
Idle	Power Down Entry *3, *4	PD	H	L	L	H	H	H	X	X	X
			H	L	H	X	X	X	X	X	X
Power Down	Power Down Exit	PDX	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X
Idle	Deep Power Down Entry *3, *4	DPD	H	L	L	H	H	L	X	X	X
Deep Power Down	Deep Power Down Exit	DPDX	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X

*1 : Address : A_{11} to A_0 @256 page length mode
: A_{12} to A_0 @128 page length mode
: A_{13} to A_0 @64 page length mode

*2 : The CSUS command requires that at least one bank is active. Refer to "■STATE DIAGRAM".

*3 : REF, SELF, PD and DPD commands should only be issued after all banks have been precharged (PRE or PALL command) . Refer to "■STATE DIAGRAM".

*4 : SELF, PD and DPD commands should only be issued after the last read data have been appeared on DQ.

*5 : CKE should be held High during t_{REFC} period after t_{CKSP}.

4. OPERATION COMMAND TABLE (single bank operation) *1

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	Bank Active after t_{RCD}
	L	L	H	L	BA, AP	PRE/PALL	NOP *5
	L	L	L	H	X	REF/SELF	Auto-refresh or Self-refresh *3, *6
	L	L	L	L	MODE	MRS	Mode Register Set (Idle after t_{RSC}) *3, *7
Bank Active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Begin Read; Determine AP
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Begin Write; Determine AP
	L	L	H	H	BA, RA	ACTV	Illegal *2
	L	L	H	L	BA, AP	PRE/PALL	Begin Precharge; Determine Precharge Type
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Read	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst Stop → Bank Active
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, New Read; Determine AP
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, Start Write; Determine AP *4
	L	L	H	H	BA, RA	ACTV	Illegal *2
	L	L	H	L	BA, AP	PRE/PALL	Terminate Burst, Precharge → Idle
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	

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Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
Write	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst Stop → Bank Active
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, Start Read; Determine AP *4
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, New Write; Determine AP
	L	L	H	H	BA, RA	ACTV	Illegal *2
	L	L	H	L	BA, AP	PRE/PALL	Terminate Burst, Precharge → Idle
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Read with Auto-precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge → Idle)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Write with Auto-precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge → Idle)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	

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Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
Precharging	H	X	X	X	X	DESL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	NOP (Idle after t_{RP}) *8
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE/PALL	NOP (PALL may affect other bank) *5
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Bank Activating	H	X	X	X	X	DESL	NOP (Bank Active after t_{RCD})
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Refreshing	H	X	X	X	X	DESL	NOP (Idle after t_{RC})
	L	H	H	X	X	NOP/BST	NOP (Idle after t_{RC}) *8
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal
	L	L	H	X	X	ACTV/ PRE/PALL	
	L	L	L	X	X	REF/SELF/ MRS	
Mode Register Setting	H	X	X	X	X	DESL	NOP (Idle after t_{RSC})
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	X	X	READ/READA/ WRIT/WRITA	
	L	L	X	X	X	ACTV/PRE/ PALL/REF/ SELF/MRS	

RA = Row Address BA = Bank Address
CA = Column Address AP = Auto Precharge

*1 : When a command is input, CKE should be held High from the preceding clock cycle. If any illegal command is asserted, following command operation and data cannot be guaranteed. If the illegal command is input, the power-up initialization is needed again.

*2 : Illegal to bank in the specified state; entry may be legal in the bank specified by BA, depending on the state of that bank.

*3 : Illegal if any bank is not idle.

*4 : Must satisfy bus contention, bus turn around, and/or write recovery requirements.
Refer to “7. READ INTERRUPTED BY PRECHARGE (EXAMPLE @ BL = 4) ” and “12. WRITE TO READ TIMING (EXAMPLE @ CL = 3, BL = 4) ” in section “■TIMING DIAGRAMS”.

*5 : NOP to bank precharging or in idle state. May precharge bank specified by BA (and AP) .

*6 : SELF command should only be issued after the last read data have been appeared on DQ.

*7 : MRS command should only be issued on condition that all DQ are in High-Z.

*8 : BST command should only be issued with CKE = High.

5. COMMAND TRUTH TABLE FOR CKE *1

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function
Self-refresh	H	X	X	X	X	X	X	Invalid
	L	H	H	X	X	X	X	Exit Self-refresh (Self-refresh Recovery → Idle after t_{RC})
	L	H	L	H	H	H	X	
	L	H	L	H	H	L	X	Illegal
	L	H	L	H	L	X	X	
	L	H	L	L	X	X	X	
	L	L	X	X	X	X	X	NOP (Maintain Self-refresh)
Self-refresh Recovery	L	X	X	X	X	X	X	Invalid
	H	H	H	X	X	X	X	Idle after t_{RC}
	H	H	L	H	H	H	X	
	H	H	L	H	H	L	X	Illegal
	H	H	L	H	L	X	X	
	H	H	L	L	X	X	X	
	H	H	X	X	X	X	X	
	H	L	X	X	X	X	X	Illegal *2
Power Down	H	X	X	X	X	X	X	Invalid
	L	H	H	X	X	X	X	Exit Power Down Mode → Idle
	L	H	L	H	H	H	X	
	L	L	X	X	X	X	X	NOP (Maintain Power Down Mode)
	L	H	L	L	X	X	X	Illegal
	L	H	L	H	L	X	X	
Deep Power Down	H	X	X	X	X	X	X	Invalid
	L	H	H	X	X	X	X	Exit Deep Power Down Mode → Idle *3
	L	H	L	H	H	H	X	
	L	L	X	X	X	X	X	NOP (Maintain Deep Power Down Mode)
	L	H	L	L	X	X	X	Illegal
	L	H	L	H	L	X	X	

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Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function
Bank Active Bank Activating Read/Write All Banks Idle	H	H	X	X	X	X	X	Refer to “4. Operation Command Table”.
	H	L	X	X	X	X	X	Refer to “4. Operation Command Table”. Start Clock Suspend next cycle
	L	X	X	X	X	X	X	Invalid
Precharging Refreshing	H	H	X	X	X	X	X	Refer to “4. Operation Command Table”.
	H	L	H	X	X	X	X	
	H	L	L	H	X	X	X	
	H	L	L	H	L	X	X	
	H	L	L	L	H	H	X	
	L	X	X	X	X	X	X	Invalid
Clock Suspend	H	X	X	X	X	X	X	Invalid
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle
	L	L	X	X	X	X	X	Maintain Clock Suspend
Any State Other Than Listed Above	L	X	X	X	X	X	X	Invalid
	H	H	X	X	X	X	X	Refer to “4. Operation Command Table”.
	H	L	X	X	X	X	X	Illegal

*1 : All entries are specified at CKE (n) state. CKE input must satisfy corresponding set up and hold time for CKE.

*2 : CKE should be held High during t_{REFC} period.

*3 : After deep power down exit, it requires “19. DEEP POWER DOWN EXIT” procedure in section “■TIMING DIAGRAMS”.

■ FUNCTIONAL DESCRIPTION

1. SDR I/F FCRAM BASIC FUNCTION

This SDR I/F FCRAMs have major three features of which are the same functions as conventional SDRAMs : “synchronized operation”, “burst mode”, and “mode register” for setting the operation mode. The MB81ES123245 are compatible with conventional SDRAMs regarding the basic electrical function and interface.
The synchronized operation is the fundamental function. An MB81ES123245 requires an external clock input (CLK) for the synchronization. Each operation of MB81ES123245 is determined by commands and all operations function synchronizing with the rising edge of the clock.
The burst mode is a very high speed access mode utilizing an internal column address generator. Once a column addresses for the first access is set, following addresses are automatically generated by the internal column address counter.
The mode register is to justify the MB81ES123245 operation and function into desired system conditions. Refer to “■MODE REGISTER TABLE”.

2. FCRAM

The MB81ES123245 utilizes FCRAM core technology. The FCRAM is an acronym of Fast Cycle Random Access Memory, which provides very fast random cycle time, low latency and low power consumption than conventional SDRAMs.

3. CLOCK INPUT (CLK) and CLOCK ENABLE (CKE)

All input and output signals of MB81ES123245 use register type buffers. A CLK is used as a trigger for the registers and internal burst counter increment. All inputs are latched by a rising edge of CLK. All outputs are validated by the CLK. CKE is a high active clock enable signal, and controls an internal clock generator. CKE is latched at the rising edge of CLK. It is required to set High one clock cycle before the command input cycle. When CKE = Low is latched at a clock input during active cycle, the next clock will be internally masked. During idle state (all banks have been precharged) , the Power Down mode is entered with CKE = Low and this will make low standby current. The standby current of the Deep Power Down mode is lower than that of the Power Down mode. This mode is entered with CKE = Low, $\overline{RAS}$ = $\overline{CAS}$ = High and $\overline{WE}$ = Low.

4. CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ enables all commands inputs, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and address input. When $\overline{CS}$ is High, command signals are negated but internal operation such as burst cycle are not stopped. If such a control isn’t needed, $\overline{CS}$ can be tied to ground level.

5. COMMAND INPUT ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$)

Unlike a conventional DRAM, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ do not directly imply MB81ES123245 operation, such as Row address strobe by $\overline{RAS}$. Instead, a combination of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ input referring $\overline{CS}$ input at a rising edge of the CLK determines MB81ES123245 operation. Refer to “1. COMMAND TRUTH TABLE” in section “■FUNCTIONAL TRUTH TABLE.”

6. ADDRESS INPUT (A_{13} to A_0)

Address input selects an arbitrary location of a total of 1,048,576 words of each memory cell matrix. Row address field defined by selected page length is as follows : 256 page length = A_{11} to A_0, 128 page length = A_{12} to A_0, 64 page length = A_{13} to A_0. Total twenty address input signals by a combination of row address and column address are required to decode a matrix. MB81ES123245 adopts an address multiplexer in order to reduce the pin count of the address line. The row address is first latched by the Bank Active command (ACTV) , and the column address is then latched by a column address strobe command of either the Read command (READ or READA) or the Write command (WRIT or WRITA) .

7. BANK SELECT (BA_1, BA_0)

This MB81ES123245 has four banks and each bank is organized as 1 M words by 32-bit. Bank selection by BA occurs at Bank Active command (ACTV) followed by read (READ or READA) , write (WRIT or WRITA) , and precharge command (PRE) .

8. DATA I/O (DQ_{31} to DQ_0)

Input data is latched and written into the memory at the clock following the write command input. Data output is obtained by the following conditions followed by a read command input :

t_{RAC} ; Time from the bank active command when t_{RCD} (Min) is satisfied. (This parameter is reference only.)
t_{CAC} ; Time from the read command when t_{RCD} is greater than t_{RCD} (Min) . (This parameter is reference only.)
t_{AC} ; Time from the rising clock edge after t_{RAC} and t_{CAC}.

The polarity of the output data is identical to that of the input data. Data valid period is between access time (determined by the three conditions above) and the next rising clock edge plus output hold time (t_{OH}) .

9. INPUT MASK/OUTPUT ENABLE (DQM_3 to DQM_0)

DQM is an active high enable input and has an output disable and input mask function. When DQM = High is latched during burst cycle, input is masked at the same clock and output will be masked at the second clock later while internal burst counter will increment by one or will go to the next stage depending on burst type. DQM_0, DQM_1, DQM_2, DQM_3, controls DQ_7 to DQ_0, DQ_{15} to DQ_8, DQ_{23} to DQ_{16}, DQ_{31} to DQ_{24}, respectively.

10. BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access. The burst mode is implemented by keeping the same row address and by automatic strobing column address. Access time and cycle time of burst mode is specified as t_{AC} and t_{CK}, respectively. The internal column address counter operation is determined by a mode register which defines burst type and burst count length of 1, 2, 4 or 8 bits of boundary or full column. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 1, the following combinations will be required.

Current Stage	Next Stage	Method (Assert the following command)	
Burst Read	Burst Read	Read Command	
Burst Read	Burst Write	1st Step	Mask Command (Normally 3 clock cycles)
		2nd Step	Write Command after l_{OWD}
Burst Write	Burst Write	Write Command	
Burst Write	Burst Read	Read Command	
Burst Read	Precharge	Precharge Command	
Burst Write	Precharge	Precharge Command	

The burst type can be selected either sequential or interleave mode if burst length is 2, 4 or 8. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns + 1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least significant address (= 0) . The interleave mode is a scrambled decoding scheme for A_2 and A_0. If the first access of column address is even (the least significant bit is 0) , the next address will be odd (the least significant bit is 1) , or vice-versa. When the full column burst operation is executed at single write mode, Auto-precharge command is valid only at write operation.

Burst Length	Starting Column Address A_2 A_1 A_0	Sequential Mode	Interleave Mode
2	X X 0	0 – 1	0 – 1
	X X 1	1 – 0	1 – 0
4	X 0 0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
	X 0 1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
	X 1 0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
	X 1 1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8	0 0 0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0 0 1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
	0 1 0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
	0 1 1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
	1 0 0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1 0 1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
	1 1 0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
	1 1 1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0

11. FULL COLUMN BURST AND BURST STOP COMMAND (BST)

The full column burst is an option of burst length and available only at sequential mode of burst type. This full column burst mode executes by automatically strobing the column address while keeping the same row address. If burst mode reaches the end of column address, then it wraps around to the first column address (= 0) and continues to count until interrupted by the new read (READ) /write (WRIT) , precharge (PRE) , or burst stop (BST) commands. The selection of Auto-precharge option is illegal during the full column burst operation.
The BST command is applicable to terminate the burst operation. If the BST command is asserted during the burst mode, its operation is terminated immediately and the internal state moves to Bank Active.
When a read mode is interrupted by the BST command, the output will be in High-Z. For the detailed rule, please refer to “8. READ INTERRUPTED BY BURST STOP (EXAMPLE @CL = 3, BL = Full Column” in section “■TIMING DIAGRAMS”. When a write mode is interrupted by the BST command, the data to be input at the same time with the BST command will be ignored.

12. BURST READ & SINGLE WRITE

The burst read and single write mode provides single word write operation regardless of its burst length. In this mode, burst read operation does not be affected by this mode.

13. PROGRAMMABLE PAGE LENGTH FUNCTION

The programmable page length function provides lower operation current than regular SDRAM. Page length is selected by Mode Register Set, and the composition of the row address field and column address field are defined for selected page length as below.

	Row address	Column address
256 page length	A_{11} to A_0	A_7 to A_0
128 page length	A_{12} to A_0	A_6 to A_0
64 page length	A_{13} to A_0	A_5 to A_0

Row/column address allocation at each page length is shown as the following table. For example, A_{13} (row address) at 64 page length mode is corresponded to A_6 (column address) at 128 page length mode.

64 page length	Row : A_{13} to A_0														Column : A_5 to A_0				
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	5	4	3	2	1	0
128 page length	Row : A_{12} to A_0													Column : A_6 to A_0						
	0	1	2	3	4	5	6	7	8	9	10	11	12	6	5	4	3	2	1	0
256 page length	Row : A_{11} to A_0												Column : A_7 to A_0							
	0	1	2	3	4	5	6	7	8	9	10	11	7	6	5	4	3	2	1	0

14. PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

The MB81ES123245 memory core is the same as conventional SDRAMs, requiring precharge and refresh operations. Precharge rewrites the bit line and resets the internal row address line. With the Precharge command (PRE) , MB81ES123245 will automatically be in a standby state after precharge time (t_{RP}) . The precharged bank is selected by combination of AP and BA when Precharge command is asserted. If AP = High, all banks are precharged regardless of BA (PALL command) . If AP = Low, a bank to be selected by BA is precharged (PRE command) . The Auto-precharge enters precharge mode at the end of burst mode of read or write without Precharge command assertion. This Auto-precharge is entered by setting AP = High when a read or write command is asserted. Refer to “1. COMMAND TRUTH TABLE” in section “■FUNCTIONAL TRUTH TABLE”.

15. AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The MB81ES123245 Auto-refresh command (REF) generates Precharge command internally. All banks of MB81ES123245 should be precharged prior to asserting the Auto-refresh command. The Auto-refresh command should also be asserted every 15.6 μs or a total 4,096 refresh commands within every 64 ms period to ensure data stored.

16. SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh function until cancelled by the Self-refresh Exit command (SELFX) . The Self-refresh is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF) . Once MB81ES123245 enters the Self-refresh mode, all inputs except for CKE will be in a “don’t care” state (High or Low) and all outputs will be in a High-Z state.

During the Self-refresh mode, CKE = Low should be maintained. SELF command should only be issued after last read data has been appeared on DQ.

Note : When the burst refresh method is used, a total of 4,096 Auto-refresh commands within 2 ms must be asserted prior to the Self-refresh mode entry.

17. SELF-REFRESH EXIT (SELFX)

To exit Self-refresh mode, apply the Self-refresh Exit command (SELFX) after minimum t_{CKSP} from CKE brought High. After SELFX, the No Operation command (NOP) or the Deselect command (DESL) should be asserted during t_{REFC} period. CKE should be held High during t_{REFC} period after t_{CKSP}. Refer to “16. SELF-REFRESH ENTRY AND EXIT” in section “■TIMING DIAGRAMS” for the detail. It is recommended to assert the Auto-refresh command just after the t_{REFC} period to prevent row addresses not to be refreshed.

Note : When the burst refresh method is used, a total of 4,096 Auto-refresh commands within 2 ms must be asserted after the Self-refresh Exit.

18. MODE REGISTER SET (MRS)

The mode register of MB81ES123245 provides a variety of different operations. The register consists of five operation fields : Burst Length, Burst Type, CAS Latency, Operation Code and Page Length. Refer to "■MODE REGISTER TABLE". The mode register can be programmed by the Mode Register Set command (MRS) . Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command. MRS command should only be issued on condition that all DQ is in High-Z. The condition of the mode register is undefined after the power-up stage. Set each field after initialization of this device. Refer to "22. POWER-UP INITIALIZATION".

19. EXTENDED MODE REGISTER SET (EMRS)

The extended mode register consists of two operation fields : Partial Array Self Refresh (PASR) and Driver Strength (DS) . Refer to "■MODE REGISTER TABLE". The state of the extended mode register is undefined after the Power-up stage. Set each field after initialization. Refer to "22. POWER-UP INITIALIZATION".

20. PARTIAL ARRAY SELF-REFRESH (PASR)

Partial Array Self-Refresh is a function that limits the memory array size to be refreshed during self-refresh in order to reduce the self-refresh current. Data outside the defined area will not be retained.

21. DRIVER STRENGTH (DS)

This function is to adjust the driver strength of the data output.

22. POWER-UP INITIALIZATION

The state of MB81ES123245 internal conditions after power-up will be undefined. Follow the following Power On Sequence to execute read or write operation.

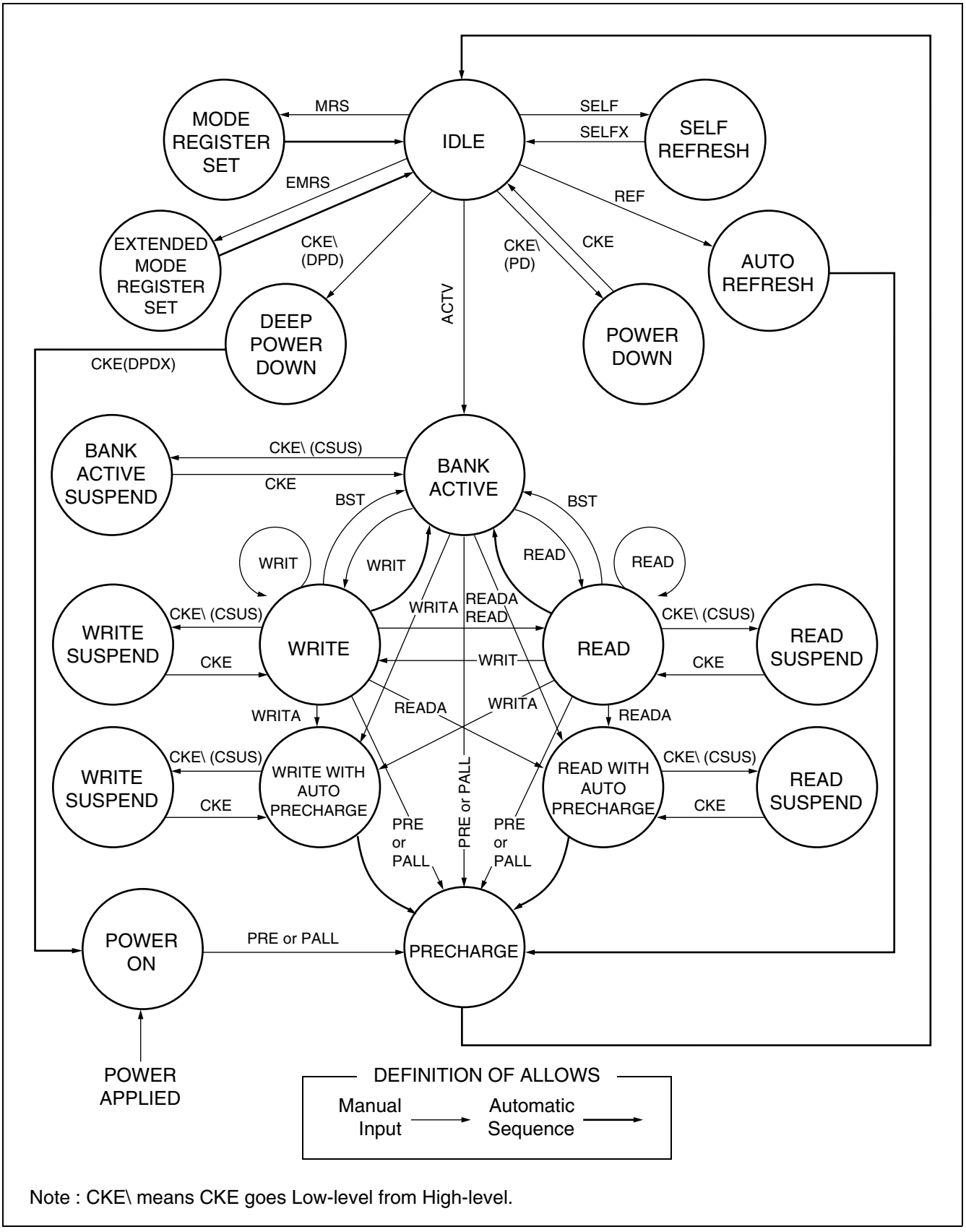
1. Apply power (V_{DD} should be applied before or in parallel with V_{DDQ}) and start clock. Attempt to maintain either NOP or DESL command at the input.
2. Maintain stable power, stable clock, and NOP condition for a minimum of 300 μs.
3. Precharge all banks by single bank precharge command (PRE) or all banks precharge command (PALL) .
4. Assert minimum of 2 Auto-refresh commands (REF) .
5. Program the mode register by Mode Register Set command (MRS) .
6. Program the extended mode register by Extended Mode Register Set command (EMRS) .

In addition, it is recommended DQM and CKE track V_{DD} to insure that output is High-Z state. The Mode Register Set command (MRS) and Extended Mode Register Set command (EMRS) can also be set before 2 Auto-refresh commands (REF) .

23. AUTOMATIC TEMPERATURE COMPENSATED SELF-REFRESH (ATCSR)

The MB81ES123245 has an ATCSR feature for low-power self-refresh current at room temperature.

■ STATE DIAGRAM



Note : CKE\ means CKE goes Low-level from High-level.

■ BANK OPERATION COMMAND TABLE

MINIMUM CLOCK LATENCY OR DELAY TIME FOR SINGLE BANK OPERATION

Second command (same bank) / First command	MRS	ACTV	READ	*4 READA	WRIT	*4 WRITA	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}	—	—	—	—	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV	—	—	t_{RCD}	t_{RCD}	t_{RCD}	t_{RCD}	t_{RAS}	t_{RAS}	—	—	1
READ	—	—	1	1	*5 1	*5 1	*4 1	*4 1	—	—	1
READA	*1, *2 BL + t_{RP}	BL + t_{RP}	—	—	—	—	*4 BL + t_{RP}	*4 BL + t_{RP}	*2 BL + t_{RP}	*2, *7 BL + t_{RP}	—
WRIT	—	—	t_{WR}	t_{WR}	1	1	*4 t_{DPL}	*4 t_{DPL}	—	—	1
WRITA	*2 BL–1 + t_{DAL}	BL–1 + t_{DAL}	—	—	—	—	*4 BL–1 + t_{DAL}	*4 BL–1 + t_{DAL}	*2 BL–1 + t_{DAL}	*2 BL–1 + t_{DAL}	—
PRE	*2, *3 t_{RP}	t_{RP}	—	—	—	—	1	*4 1	*2 t_{RP}	*2, *6 t_{RP}	1
PALL	*3 t_{RP}	t_{RP}	—	—	—	—	1	1	t_{RP}	*6 t_{RP}	1
REF	t_{RC}	t_{RC}	—	—	—	—	t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}
SELFX	t_{RC}	t_{RC}	—	—	—	—	t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}

— : Illegal Command

*1 : If t_{RP} (Min) < CL × t_{CK}, minimum latency is a sum of (BL + CL) × t_{CK}.

*2 : Assume all banks are in Idle state.

*3 : Assume output is in High-Z state.

*4 : Assume t_{RAS} (Min) is satisfied.

*5 : Assume no I/O conflict.

*6 : Assume after the last data have been appeared on DQ.

*7 : If t_{RP} (Min) < (CL – 1) × t_{CK}, minimum latency is a sum of (BL + CL – 1) × t_{CK}.

MINIMUM CLOCK LATENCY OR DELAY TIME FOR MULTI BANK OPERATION

Second command (other bank) / First command	MRS	ACTV	READ *5	READA *5,*6	WRIT *5	WRITA *5, *6	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}	—	—	—	—	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV	—	*2 t_{RRD}	*7 1	*7 1	*7 1	*7 1	*6, *7 1	*7 t_{RAS}	—	—	1
READ	—	*2, *4 1	1	1	*10 1	*10 1	*6 1	*6 1	—	—	1
READA	*1, *2 BL + t_{RP}	*2, *4 1	*6 1	*6 1	*6, *10 1	*6, *10 1	*6 1	*6 BL + t_{RP}	*2 BL + t_{RP}	*2, *9 BL + t_{RP}	—
WRIT	—	*2, *4 1	1	1	1	1	*6 1	*6 t_{DPL}	—	—	1
WRITA	*2 BL–1 + t_{DAL}	*2, *4 1	*6 1	*6 1	*6 1	*6 1	*6 1	*6 BL–1 + t_{DAL}	*2 BL–1 + t_{DAL}	*2 BL–1 + t_{DAL}	—
PRE	*2, *3 t_{RP}	*2, *4 1	*7 1	*7 1	*7 1	*7 1	*6, *7 1	*7 1	*2 t_{RP}	*2, *8 t_{RP}	1
PALL	*3 t_{RP}	t_{RP}	—	—	—	—	1	1	t_{RP}	*8 t_{RP}	1
REF	t_{RC}	t_{RC}	—	—	—	—	t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}
SELFX	t_{RC}	t_{RC}	—	—	—	—	t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}

— : Illegal Command

*1 : If t_{RP} (Min) < CL × t_{CK}, minimum latency is a sum of (BL + CL) × t_{CK}.

*2 : Assume bank of the object is in Idle state.

*3 : Assume output is in High-Z state.

*4 : t_{RRD} (Min) of other bank (second command will be asserted) is satisfied.

*5 : Assume other bank is in active, read or write state.

*6 : Assume t_{RAS} (Min) is satisfied.

*7 : Assume other banks are not in READA/WRITA state.

*8 : Assume after the last data have been appeared on DQ.

*9 : If t_{RP} (Min) < (CL – 1) × t_{CK}, minimum latency is a sum of (BL + CL – 1) × t_{CK}.

*10 : Assume no I/O conflict.

■ MODE REGISTER TABLE

• MODE REGISTER SET

BA_1	BA_0	A_{13}*5	A_{12}*4	A_{11}	A_{10}	A_9	A_8*3	A_7*3	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
0	0	PL		0	0	Opcode	0	0	CL			BT	BL			MODE REGISTER

A_{13}	A_{12}	PAGE LENGTH
GND	GND	256 page
GND	1	128 page
1	0	64 page
1	1	Reserved

A_6	A_5	A_4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Length	
			BT = 0	BT = 1*2
0	0	0	1	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Column	Reserved

A_9	Operation Code
0	Burst Read & Burst Write
1	Burst Read & Single Write*1

A_3	Burst Type
0	Sequential (Wrap round, Binary-up)
1	Interleave (Wrap round, Binary-up)

• EXTENDED MODE REGISTER

BA_1	BA_0	A_{13}*5	A_{12}*4	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
1	0	0	0	0	0	0	0	0	DS		0	0	PASR			EXTENDED MODE REGISTER

A_6	A_5	Driver Strength
0	0	100% (Normal)
0	1	70%
1	0	60%
1	1	30%

A_2	A_1	A_0	SELF REFRESH AREA
0	0	0	128 M bit
0	0	1	64 M bit (BA_1 = 0)
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

*1. When A_9 = 1, burst length at Write is always one regardless of BL value.
*2. BL = 1 and Full column are not applicable to the interleave mode.
*3. A_7 = 1 and A_8 = 1 are reserved for vendor test.
*4. A_{12} should be connected to GND at 256 page length mode.
*5. A_{13} should be connected to GND at 128 and 256 page length mode.

■ ABSOLUTE MAXIMUM RATINGS

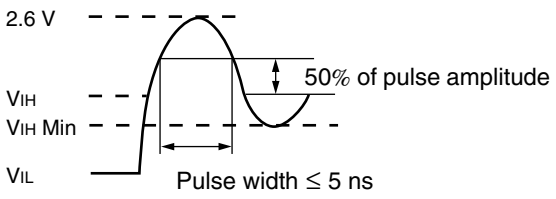
Parameter	Symbol	Rating		Unit
		Min	Max	
Supply Voltage*	V_{DD}, V_{DDQ}	− 0.5	+ 2.6	V
Input/Output Voltage*	V_{IN}, V_{OUT}	− 0.5	+ 2.6	V
Short Circuit Output Current	I_{OUT}	− 50	+ 50	mA
Power Dissipation	P_D	—	1.0	W
Storage Temperature	T_{STG}	− 55	+ 125	°C

* : All voltages are referenced to V_{SS}.

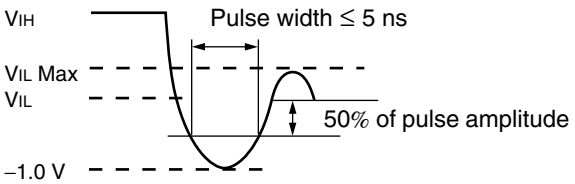
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{DD}, V_{DDQ}	1.7	1.8	1.9	V
	V_{SS}, V_{SSQ}	0	0	0	V
Input High Voltage *1	V_{IH}	$V_{DDQ} \times 0.8$	—	$V_{DDQ} + 0.3$	V
Input Low Voltage *2	V_{IL}	− 0.3	—	$V_{DDQ} \times 0.2$	V
Junction Temperature *3	Tj	− 25	—	+ 95	°C



*1 : Overshoot limit :
V_{IH} (Max) = 2.6 V for pulse width ≤ 5 ns,
pulse width measured at 50% of pulse amplitude.



*2 : Undershoot limit :
V_{IL} (Min) = V_{SSQ} − 1.0 V for pulse width ≤ 5 ns,
pulse width measured at 50% of pulse amplitude.

*3 : The maximum junction temperature of FCRAM (Tj) should not be more than +95 °C.
Tj is represented by the power consumption of FCRAM (P_{FCRAM}) and Logic LSI (P_D) , the thermal resistance of the package (θ ja) , and the maximum ambient temperature of the SiP (Tamax) .

Σ pmax[W] = $P_{FCRAM} + P_D$
Tjmax[°C] = Tamax[°C] + θ ja[°C/W] × Σ pmax[W]

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ CAPACITANCE

(T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance, Except for CLK	C_{IN1}	1.5	—	3.0	pF
Input Capacitance for CLK	C_{IN2}	1.5	—	3.0	pF
I/O Capacitance	$C_{I/O}$	2.0	—	4.0	pF

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) *1, *2, *3

Parameter	Symbol	Condition		Value		Unit
				Min	Max	
Output High Voltage	V_{OH} (DC)	I_{OH} = –0.1 mA		V_{DDQ} – 0.2	—	V
Output Low Voltage	V_{OL} (DC)	I_{OL} = 0.1 mA		—	0.2	V
Input Leakage Current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DDQ}, All other pins not under test = 0 V		–5	+ 5	µA
Output Leakage Current	I_{LO}	0 V ≤ V_{IN} ≤ V_{DDQ}, Data out disabled		–5	+ 5	µA
Operating Current (Average Power Supply Current)	I_{DD1}	Burst Length = 1, t_{RC} = Min, t_{CK} = Min, One bank active, Output pin open, Address changed up to 1 time during t_{RC} (Min) , 0 V ≤ V_{IN} ≤ V_{IL} (Max) , V_{IH} (Min) ≤ V_{IN} ≤ V_{DD}	256 page length	—	60	mA
			128 page length	—	45	
			64 page length	—	35	
Precharge Standby Current (Power Supply Current)	I_{DD2P}	CKE = V_{IL}, All banks idle, t_{CK} = Min, Power down mode, 0 V ≤ V_{IN} ≤ V_{IL} (Max) , V_{IH} (Min) ≤ V_{IN} ≤ V_{DD}		—	0.8	mA
	I_{DD2PS}	CKE = V_{IL}, All banks idle, CLK = V_{IH} or V_{IL}, Power down mode, 0 V ≤ V_{IN} ≤ V_{IL} (Max) , V_{IH} (Min) ≤ V_{IN} ≤ V_{DD}		—	0.5	mA
	I_{DD2N}	CKE = V_{IH}, All banks idle, t_{CK} = 20 ns, NOP commands only, Input signals (except for commands) are changed 1 time during 2 clocks, 0 V ≤ V_{IN} ≤ V_{IL} (Max) , V_{IH} (Min) ≤ V_{IN} ≤ V_{DD}		—	10	mA
	I_{DD2NS}	CKE = V_{IH}, All banks idle, CLK = V_{IH} or V_{IL}, Input signals are stable, 0 V ≤ V_{IN} ≤ V_{IL} (Max) , V_{IH} (Min) ≤ V_{IN} ≤ V_{DD}		—	1	mA
Burst mode Current (Average Power Supply Current)	I_{DD4}	t_{CK} = Min, Burst Length = 4, Output pin open, All-banks active, Gapless data, 0 V ≤ V_{IN} ≤ V_{IL} (Max) , V_{IH} (Min) ≤ V_{IN} ≤ V_{DD}	CL = 2	—	40	mA
			CL = 3	—	70	
Refresh Current#1 (Average Power Supply Current)	I_{DD5}	Auto-refresh, t_{CK} = Min, t_{RC} = Min, 0 V ≤ V_{IN} ≤ V_{IL} (Max) , V_{IH} (Min) ≤ V_{IN} ≤ V_{DD}		—	150	mA

(Continued)

(Continued)

(At recommended operating conditions unless otherwise noted.) *1, *2, *3

Parameter	Symbol	Condition		Value		Unit
				Min	Max	
Refresh Current #2 (Average Power Supply Current)	I_{DD6}	Self-refresh (128M-bit) , t_{CK} = Min, CKE ≤ 0.2 V, 0 V ≤ V_{IN} ≤ V_{IL} (Max) , V_{IH} (Min) ≤ V_{IN} ≤ V_{DDQ}	Tj ≤ +35 °C	—	200	µA
			Tj ≤ +95 °C	—	800	
Precharge Standby Current in Deep Power Down mode	I_{DD7}	CKE ≤ 0.2 V, All banks idle, Deep Power Down mode, 0 V ≤ V_{IN} ≤ V_{IL} (Max) , V_{IH} (Min) ≤ V_{IN} ≤ V_{DD}		—	15	µA

*1 : All voltages are referenced to V_{SS}.

*2 : DC characteristics are measured after following the “22. POWER-UP INITIALIZATION” procedure in section “■FUNCTIONAL DESCRIPTION.”

*3 : I_{DD} depends on the output termination or load condition, clock cycle rate, signal clocking rate. The specified values are obtained with the output open and no termination resistor.

■ AC CHARACTERISTICS

1. BASIC AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) *1, *2, *3

Parameter		Symbol	Value		Unit
			Min	Max	
Clock Period	CL = 2	t_{CK2}	18.5	—	ns
	CL = 3	t_{CK3}	9.2	—	ns
Clock High Pulse Width *5		t_{CH}	3	—	ns
Clock Low Pulse Width *5		t_{CL}	3	—	ns
Input Setup Time *5		t_{SI}	2.5	—	ns
Input Hold Time *5		t_{HI}	1	—	ns
Access Time from CLK (t_{CK} = Min) *5, *6, *7	CL = 2	t_{AC2}	—	9	ns
	CL = 3	t_{AC3}	—	7	ns
CLK to Output in Low-Z Delay Time *5		t_{LZ}	0	—	ns
CLK to Output in High-Z Delay Time *5, *7, *8	CL = 2	t_{HZ2}	2.5	9	ns
	CL = 3	t_{HZ3}	2.5	7	ns
Output Hold Time *4		t_{OH}	2.5	—	ns
Time between Auto-Refresh Command Interval *9		t_{REFI}	—	15.6	µs
Time between Refresh		t_{REF}	—	64	ms
Refresh Cycle Time		t_{REFC}	82.8	—	ns
Transition Time		t_T	0.5	10	ns
CKE Setup Time for Power Down Exit *5		t_{CKSP}	2.5	—	ns

*1 : AC characteristics are measured after following the “22. POWER-UP INITIALIZATION” procedure in section “■FUNCTIONAL DESCRIPTION”.

*2 : AC characteristics assume t_T = 1 ns, 50Ω of termination resistor. Refer to “5. MEASUREMENT CONDITION OF AC CHARACTERISTICS”.

*3 : 0.9 V is the reference level for 1.8 V I/O for measuring timing of input/output signals. Transition times are measured between V_{IH} (Min) and V_{IL} (Max) .

*4 : This value is for reference only.

*5 : If input signal transition time (t_T) is longer than 1 ns : [(t_T/2) – 0.5] ns should be added to t_{AC} (Max) , t_{HZ} (Max) , and t_{CKSP} (Min) spec values, [(t_T/2) – 0.5] ns should be subtracted from t_{LZ} (Min) , t_{HZ} (Min) , and t_{OH} (Min) spec values, and (t_T – 1.0) ns should be added to t_{CH} (Min) , t_{CL} (Min) , t_{SI} (Min) , and t_{HI} (Min) spec values.

*6 : t_{AC} also specifies the access time at burst mode.

*7 : t_{AC} and t_{OH} are measured under output load circuit shown in “5. MEASUREMENT CONDITION OF AC CHARACTERISTICS”.

*8 : Specified where output buffer is no longer driven.

*9 : Auto refresh command is allowed to input maximum 32 times a t_{REFI} (Max) period.

2. BASE VALUES FOR CLOCK COUNT/LATENCY

Parameter		Symbol	Value		Unit
			Min	Max	
$\overline{RAS}$ Cycle Time *		t_{RC}	82.8	—	ns
$\overline{RAS}$ Precharge Time		t_{RP}	24	—	ns
$\overline{RAS}$ Active Time		t_{RAS}	55.2	110000	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	24	—	ns
Write Recovery Time		t_{WR}	9.2	—	ns
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time		t_{RRD}	16	—	ns
Data-in to Precharge Lead Time		t_{DPL}	18.4	—	ns
Data-in to Active/Refresh Command Period	CL = 2	t_{DAL2}	1 cyc + t_{RP}	—	ns
	CL = 3	t_{DAL3}	2 cyc + t_{RP}	—	ns
Mode Register Set Cycle Time		t_{RSC}	16	—	ns

* : Actual clock count of t_{RC} (I_{RC}) will be sum of clock count of t_{RAS} (I_{RAS}) and t_{RP} (I_{RP}) .

3. CLOCK COUNT FORMULA

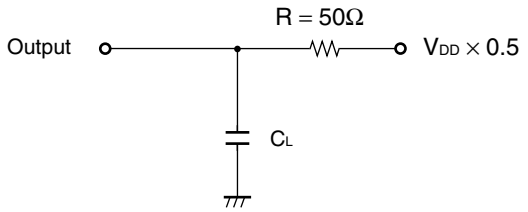
$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad \text{(Round up a whole number)}$$

Note : All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by above formula.

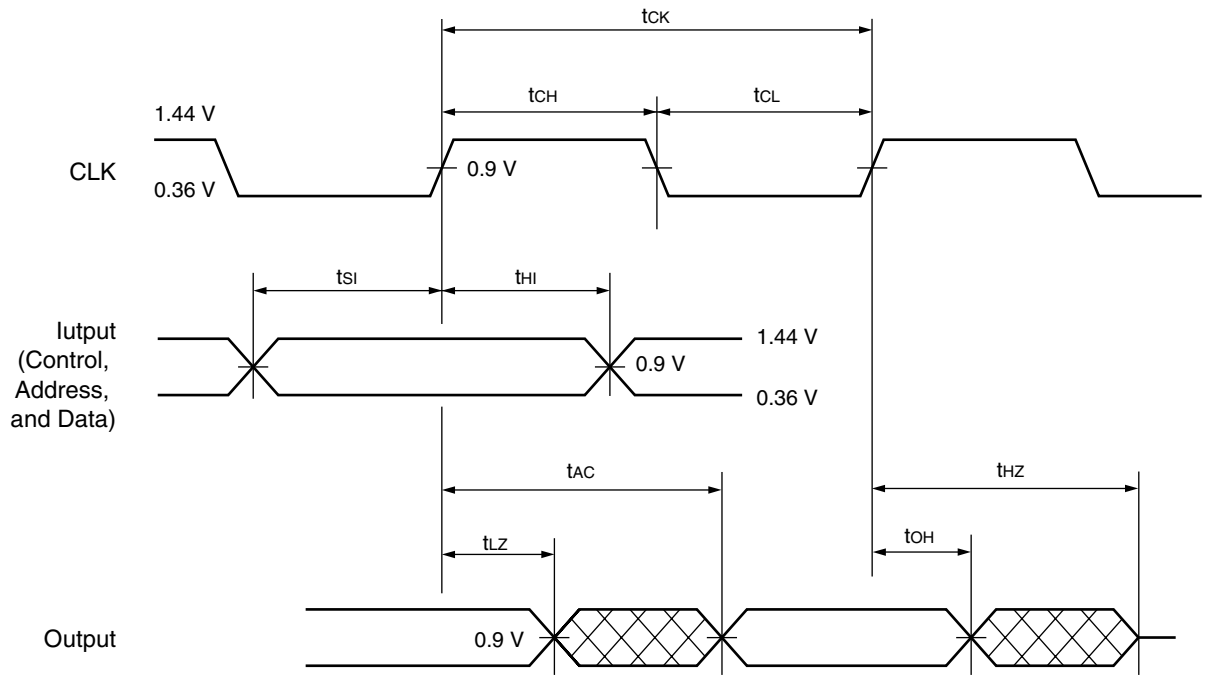
4. LATENCY (The latency values on these parameters are fixed regardless of clock period.)

Parameter		Symbol	Value	Unit
CKE to Clock Disable		I_{CKE}	1	cycle
DQM to Output in High-Z		I_{DQZ}	2	cycle
DQM to Input Data Delay		I_{DQD}	0	cycle
Last Output to Write Command Delay		I_{OWD}	2	cycle
Write Command to Input Data Delay		I_{DWD}	0	cycle
Precharge to Output in High-Z Delay	CL = 2	I_{ROH2}	2	cycle
	CL = 3	I_{ROH3}	3	cycle
Burst Stop Command to Output in High-Z Delay	CL = 2	I_{BSH2}	2	cycle
	CL = 3	I_{BSH3}	3	cycle
$\overline{CAS}$ to $\overline{CAS}$ Delay (Min)		I_{CCD}	1	cycle
$\overline{CAS}$ Bank Delay (Min)		I_{CBD}	1	cycle

5. MEASUREMENT CONDITION OF AC CHARACTERISTICS

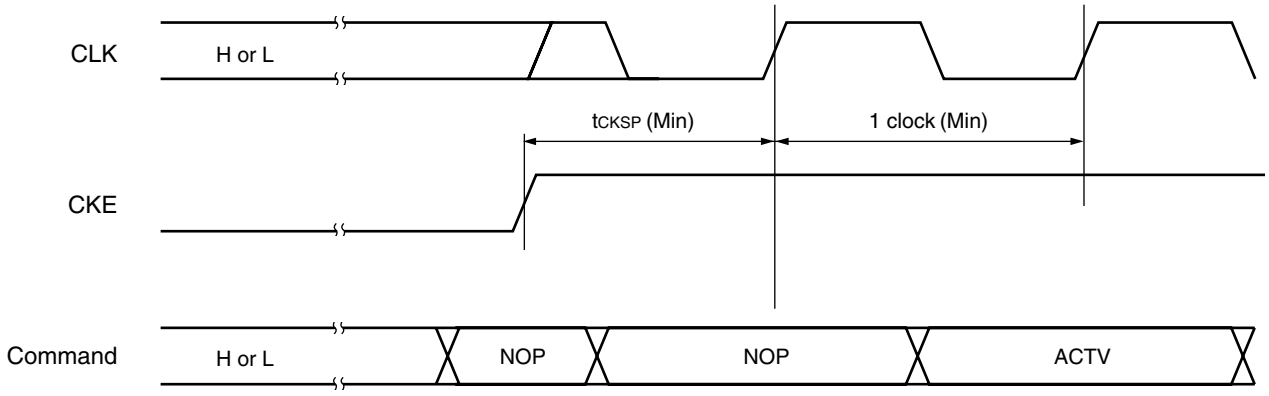


6. SETUP, HOLD AND DELAY TIME

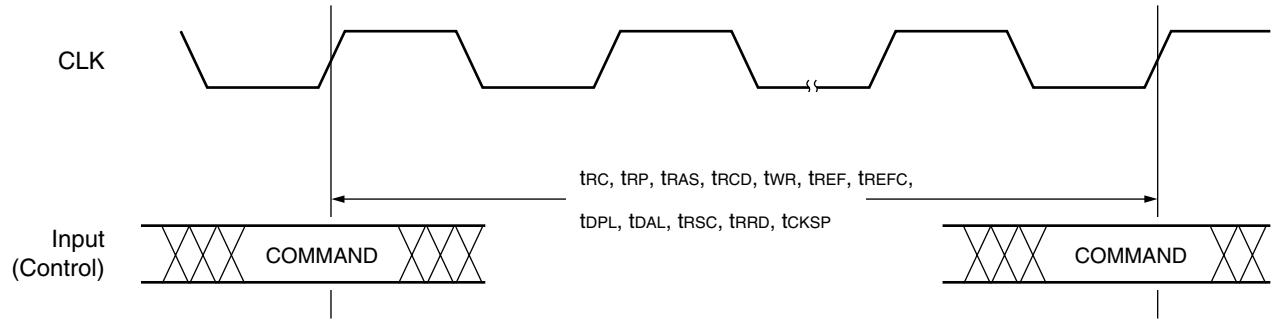


Note : Reference level of input signal is 0.9 V.
Access time is measured at 0.9 V.
AC characteristics are also measured in this condition.

7. DELAY TIME FOR POWER DOWN EXIT

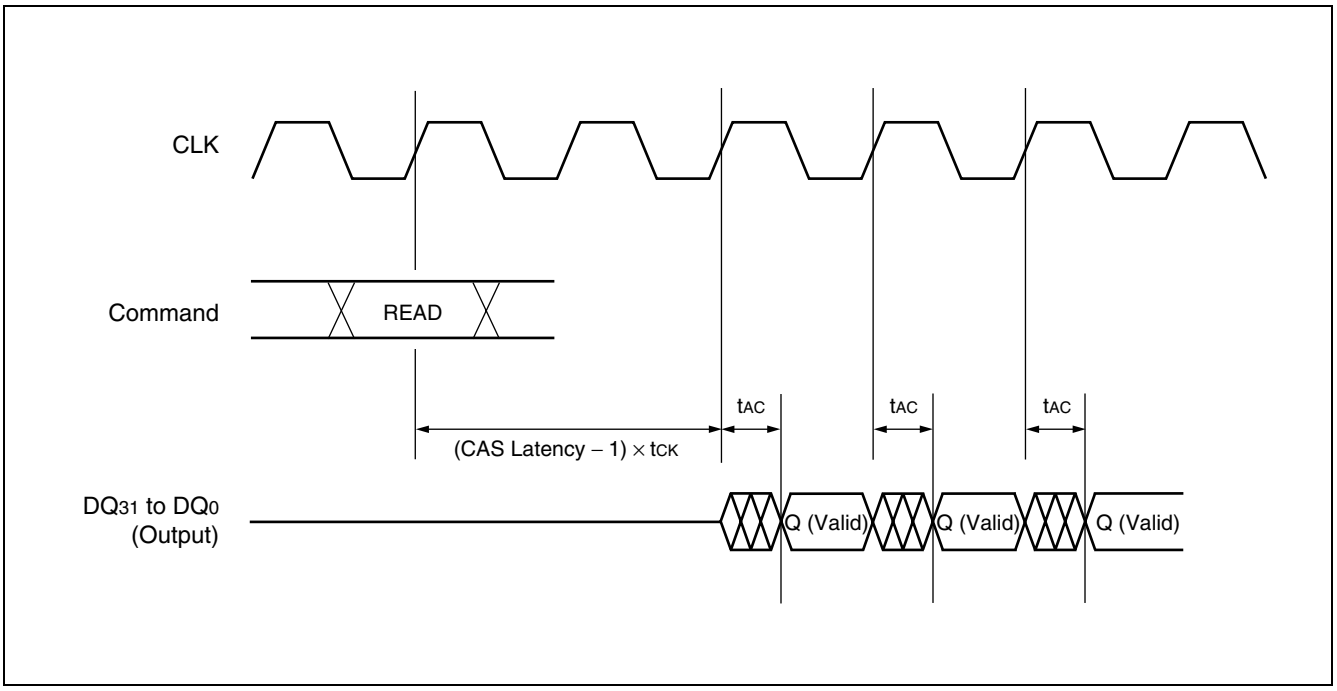


8. PULSE WIDTH



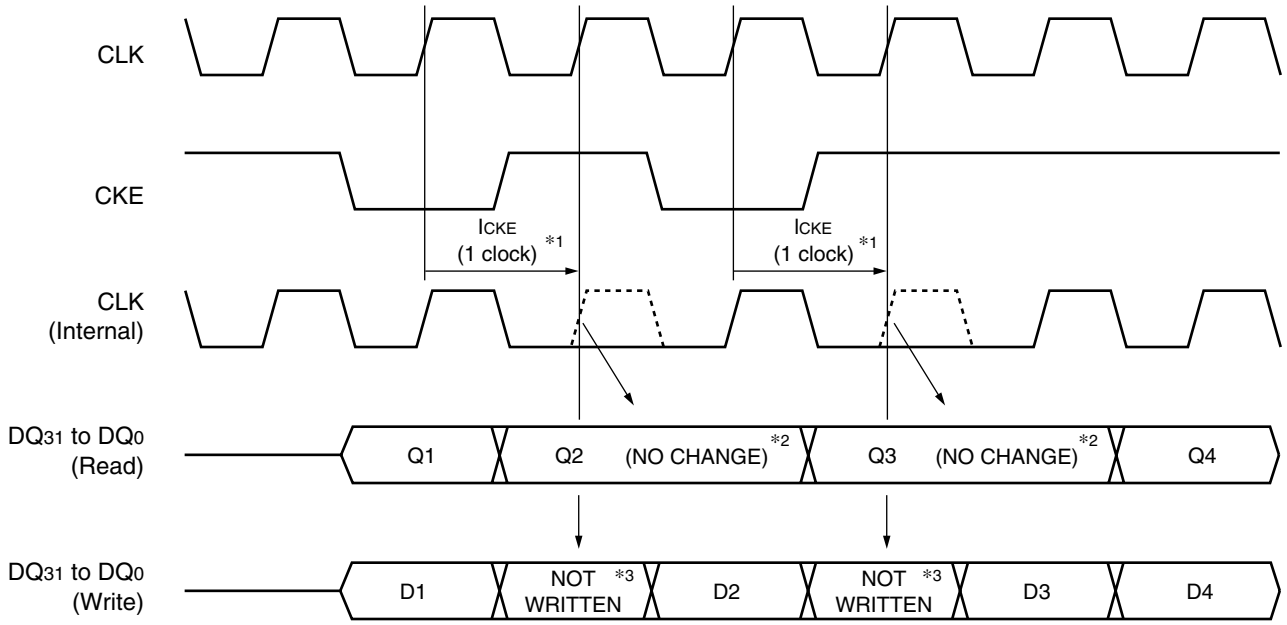
Note : These parameters are a limit value of the rising edge of the clock from one command input to next input.
t_{CKSP} is the latency value from the rising edge of CKE.
Measurement reference voltage is 0.9 V.

9. ACCESS TIME



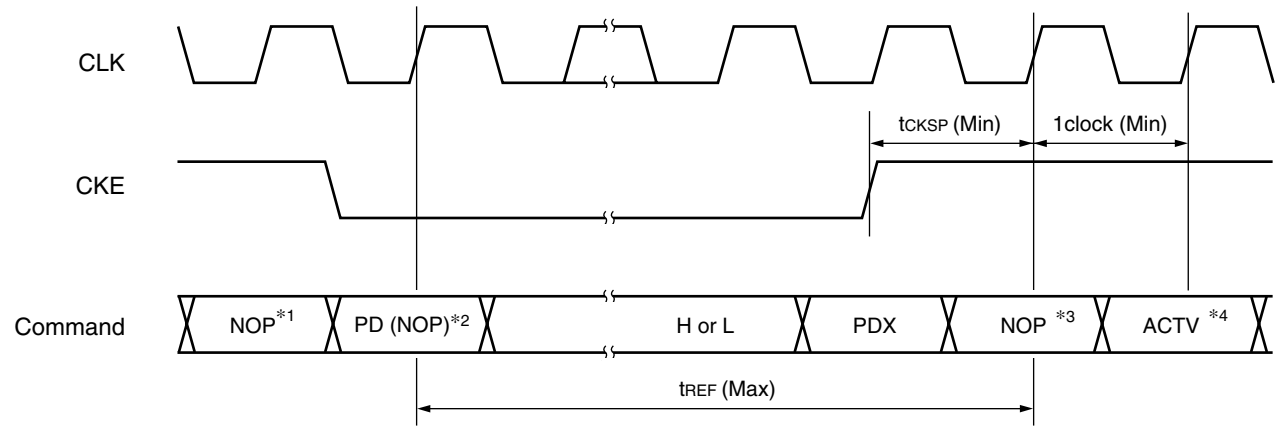
■ TIMING DIAGRAMS

1. CLOCK ENABLE READ AND WRITE SUSPEND (@ BL = 4)



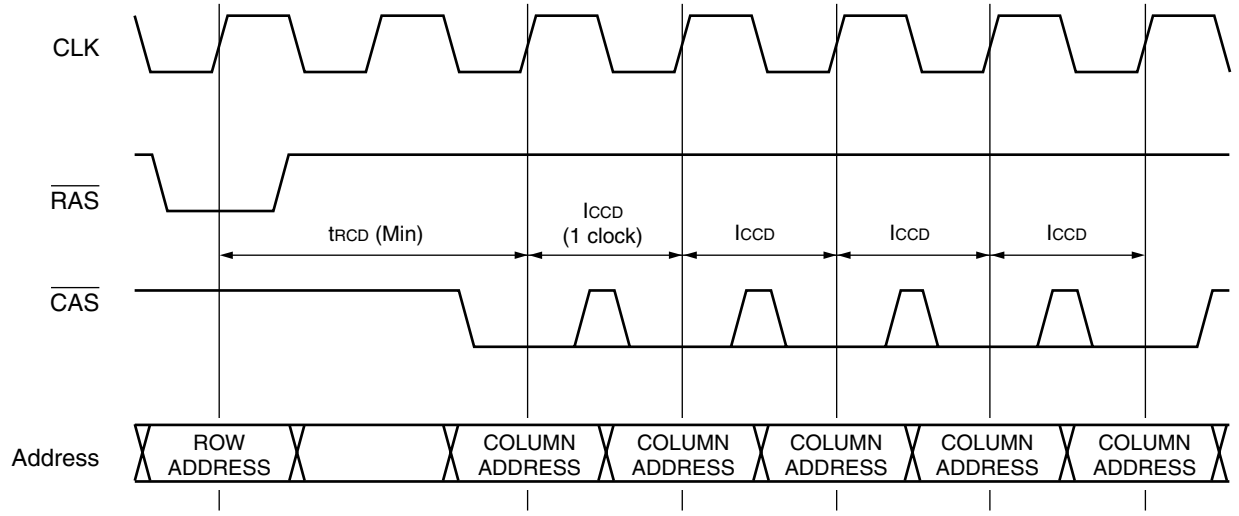
*1 : The latency of CKE (I_{CKE}) is one clock.
*2 : During read mode, the burst counter is not be incremented at the following clock of CSUS command. The output data remain the same.
*3 : During write mode, the data at the following clock of CSUS command is ignored.

2. POWER DOWN ENTRY AND EXIT



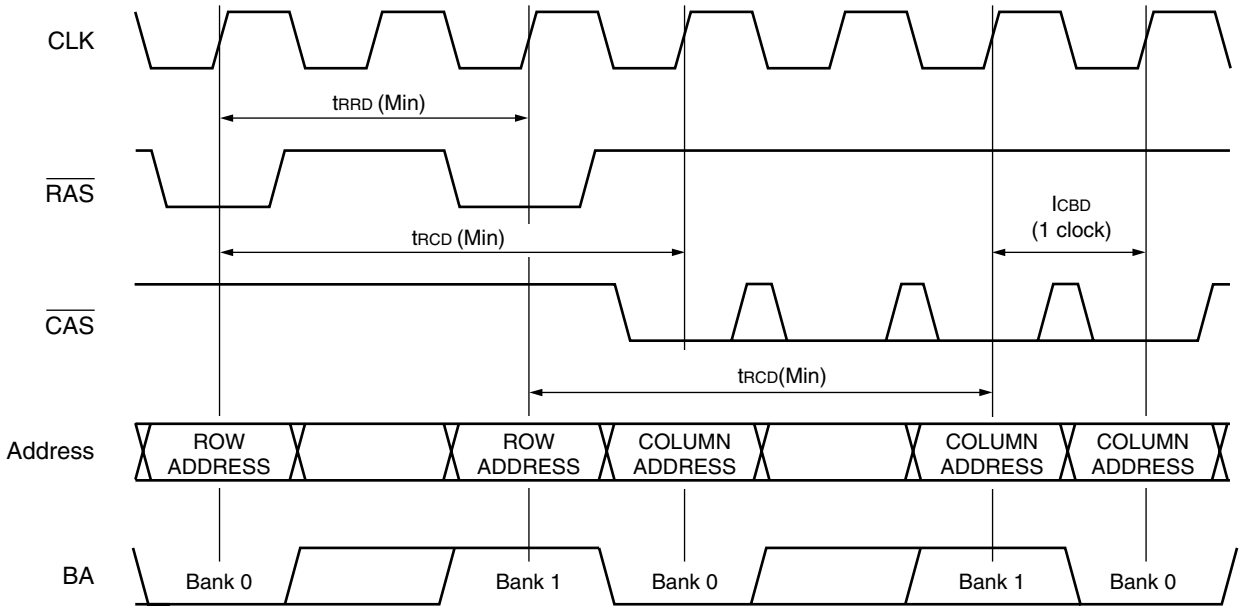
*1 : Precharge command (PRE or PALL) should be asserted if any bank is active and in the burst mode.
*2 : Precharge command can be posted in conjunction with CKE after the last read data have been appeared on DQ.
*3 : It is recommended to apply NOP command in conjunction with CKE.
*4 : The ACTV command can be latched after t_{CKSP} (Min) + 1 clock (Min) .

3. COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY



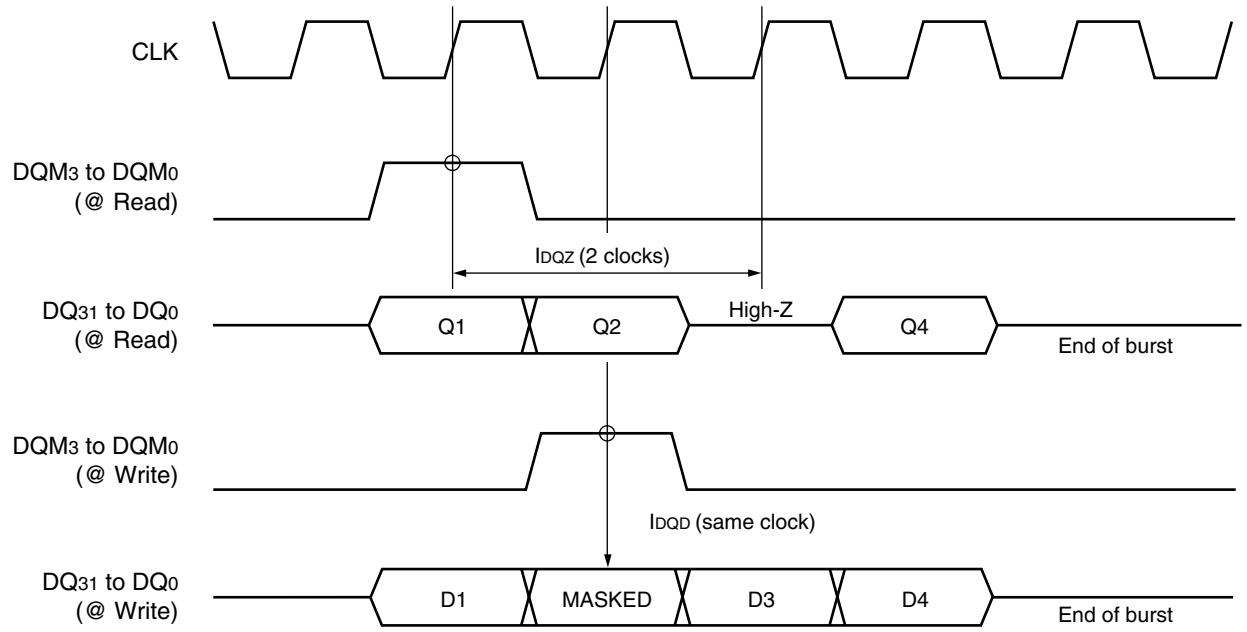
Note : $\overline{CAS}$ to $\overline{CAS}$ delay (t_{CCD}) can be one or more clock period.

4. DIFFERENT BANK ADDRESS INPUT DELAY

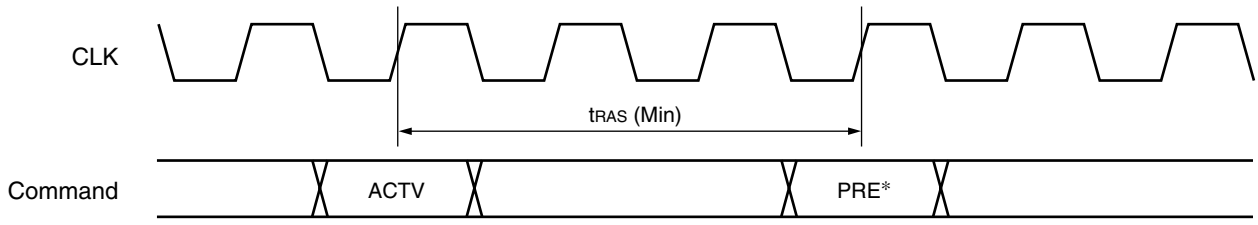


Note : $\overline{CAS}$ Bank delay (t_{CBD}) can be one or more clock period.

5. INPUT MASK AND OUTPUT DISABLE (@ BL = 4)

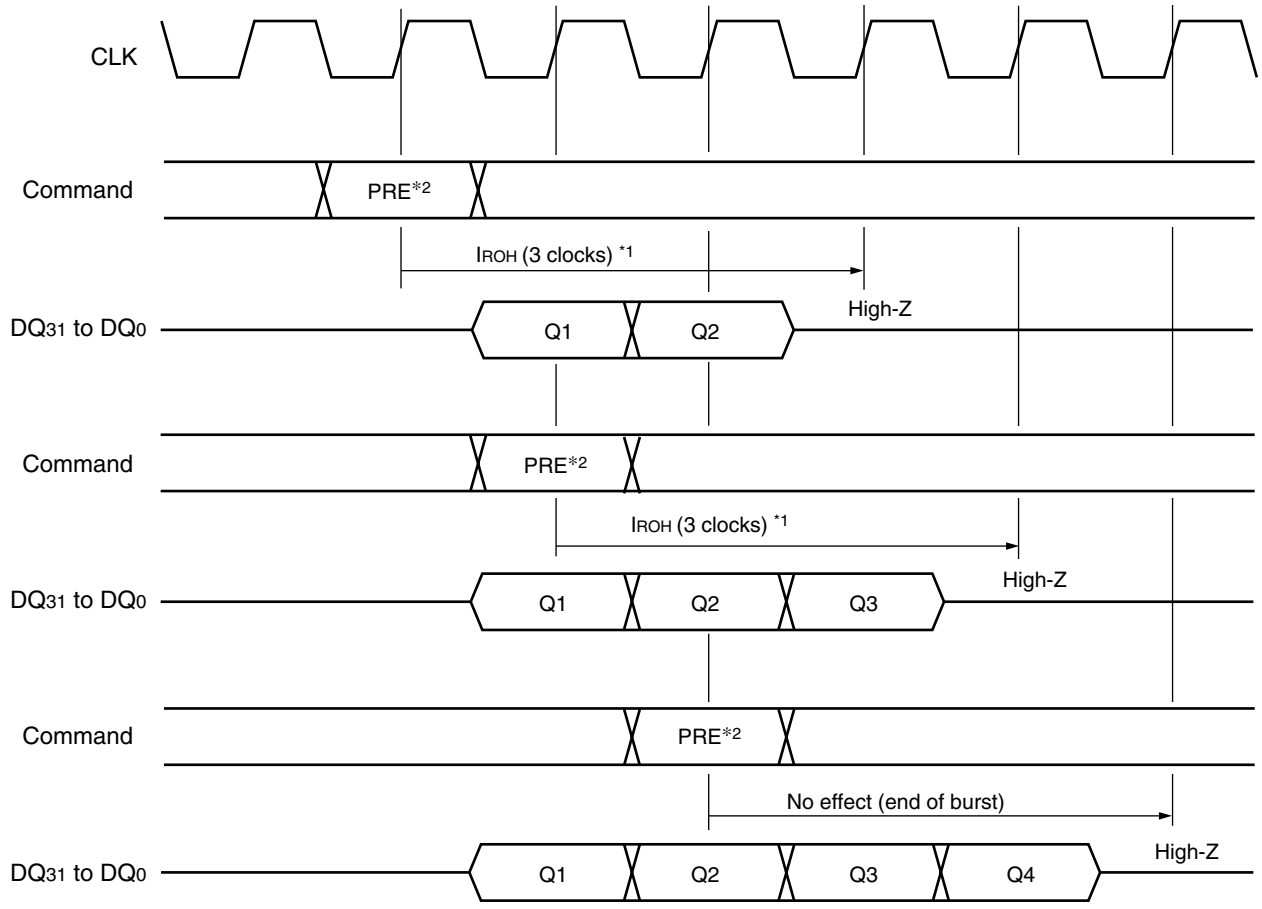


6. PRECHARGE TIMING (APPLIED TO THE SAME BANK)



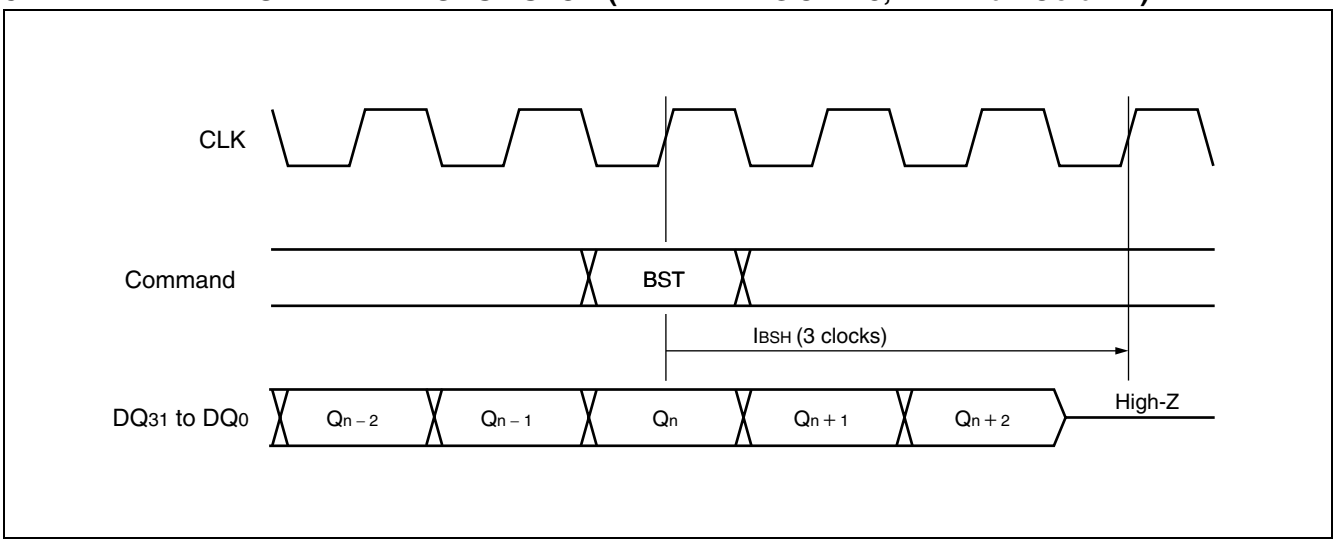
* : PRE means 'PRE' or 'PALL'.

7. READ INTERRUPTED BY PRECHARGE (EXAMPLE @ BL = 4)

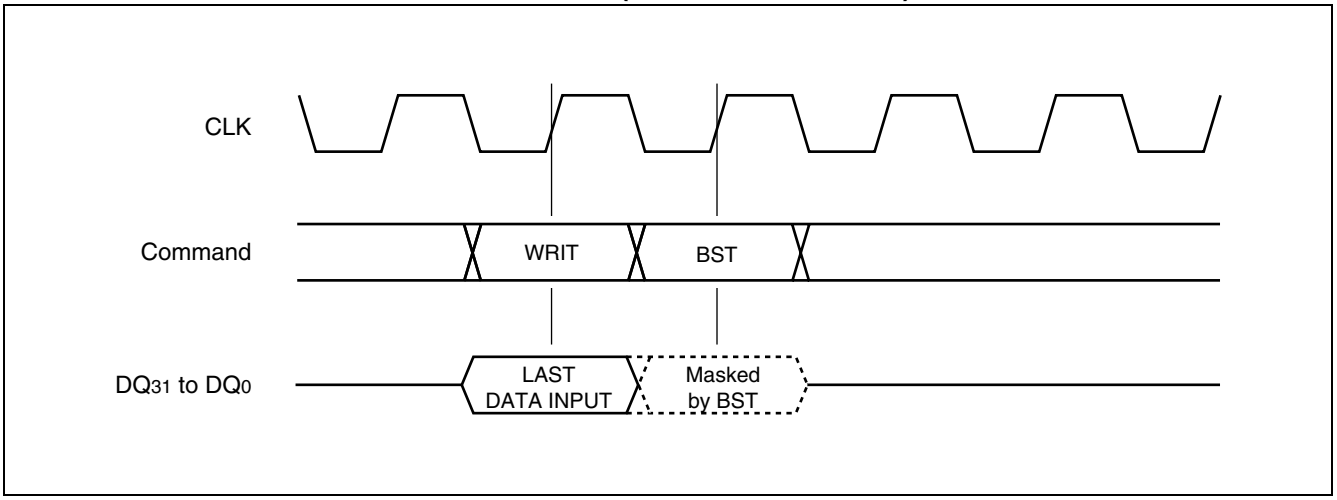


*1 : In case of CL = 3, the latency from the Precharge command (PRE) to output in High-Z (I_{ROH}) is 3 clocks.
*2 : PRE means 'PRE' or 'PALL'.

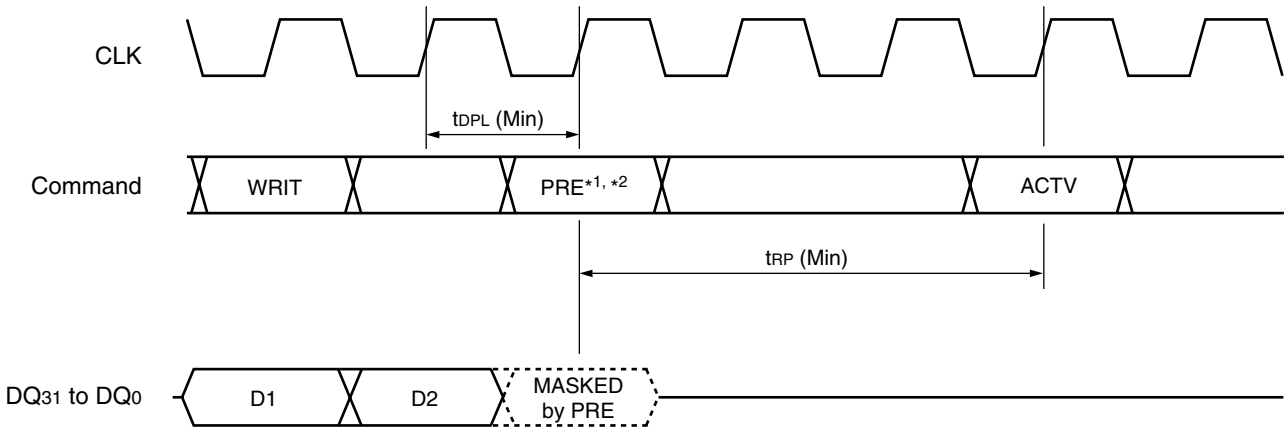
8. READ INTERRUPTED BY BURST STOP (EXAMPLE @CL = 3, BL = Full Column)



9. WRITE INTERRUPTED BY BURST STOP (EXAMPLE @ BL = 2)



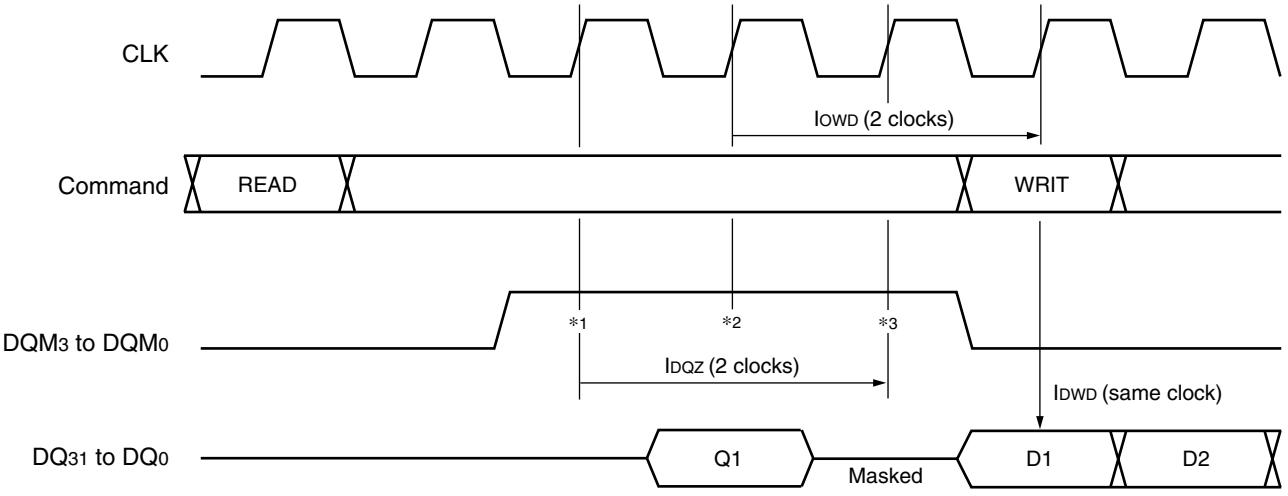
10. WRITE INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 3, BL = 4)



*1 : The precharge command (PRE) should only be issued after the t_{DPL} of final data input is satisfied.

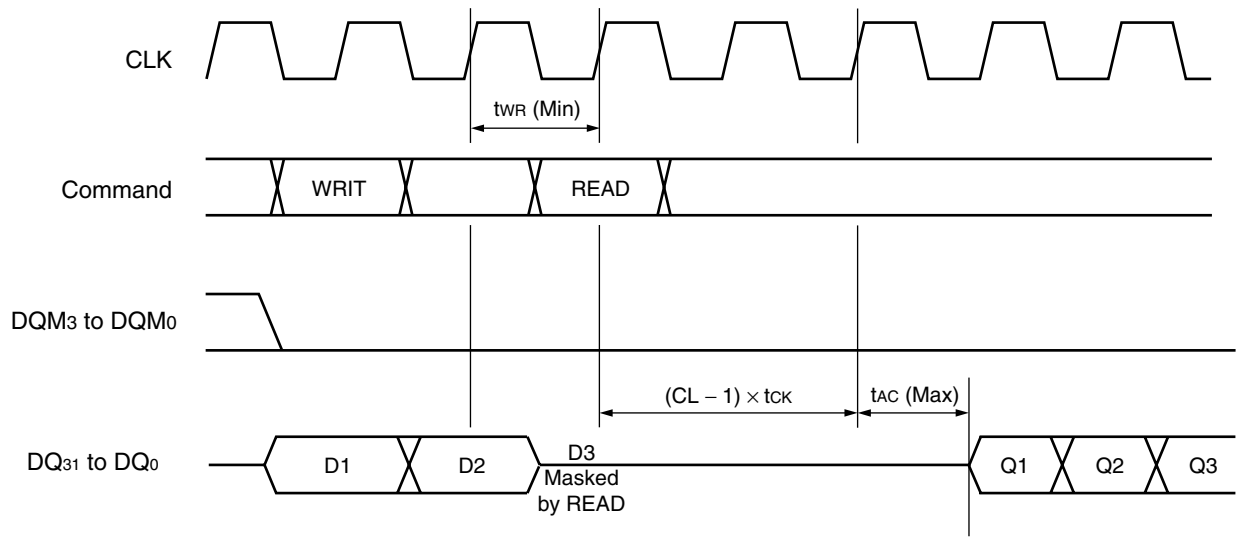
*2 : PRE means “PRE” or “PALL”.

11. READ INTERRUPTED BY WRITE (EXAMPLE @ CL = 3, BL = 4)



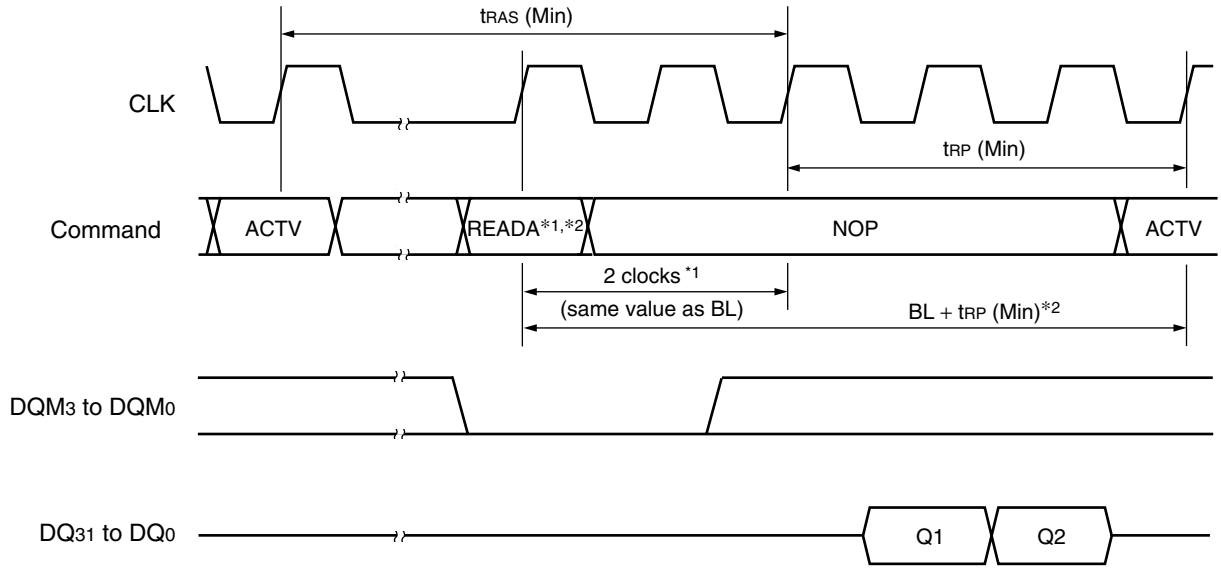
*1 : First DQM makes High-Z state between last output and first input data.
*2 : Second DQM makes internal output data mask to avoid bus contention.
*3 : Third DQM also makes internal output data mask. If burst read ends (final data output) at or after the second clock of burst write, this third DQM is required to avoid internal bus contention.

12. WRITE TO READ TIMING (EXAMPLE @ CL = 3, BL = 4)



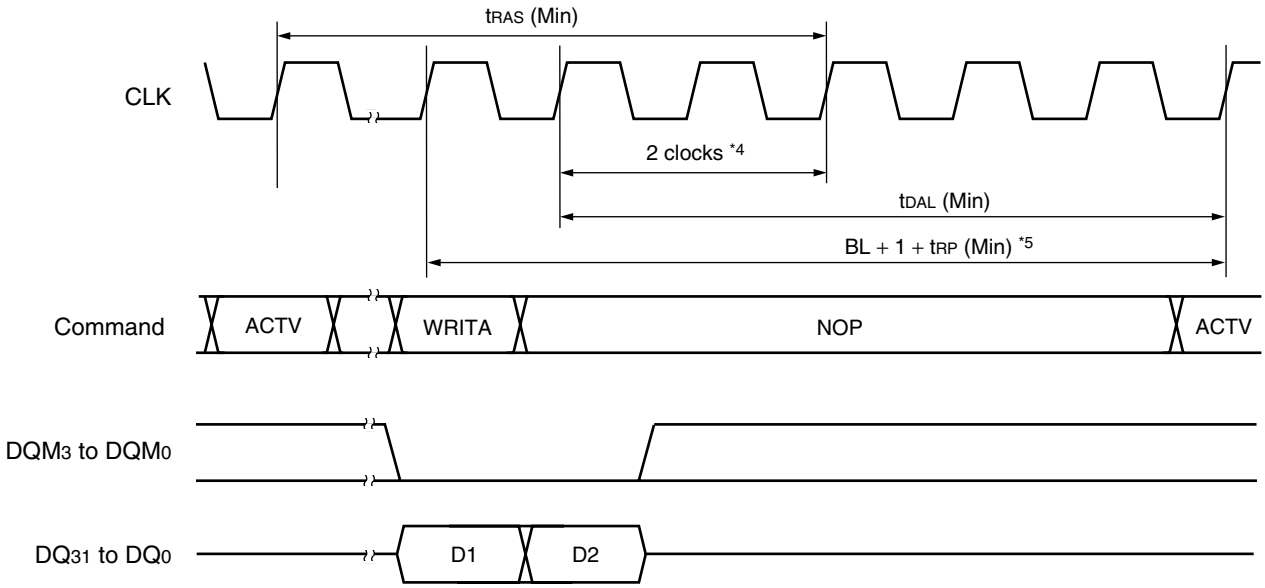
Note : Read command should be issued after t_{WR} of final data input is satisfied.

13. READ WITH AUTO-PRECHARGE (EXAPLE @ CL = 3, BL = 2, Applied to same bank)



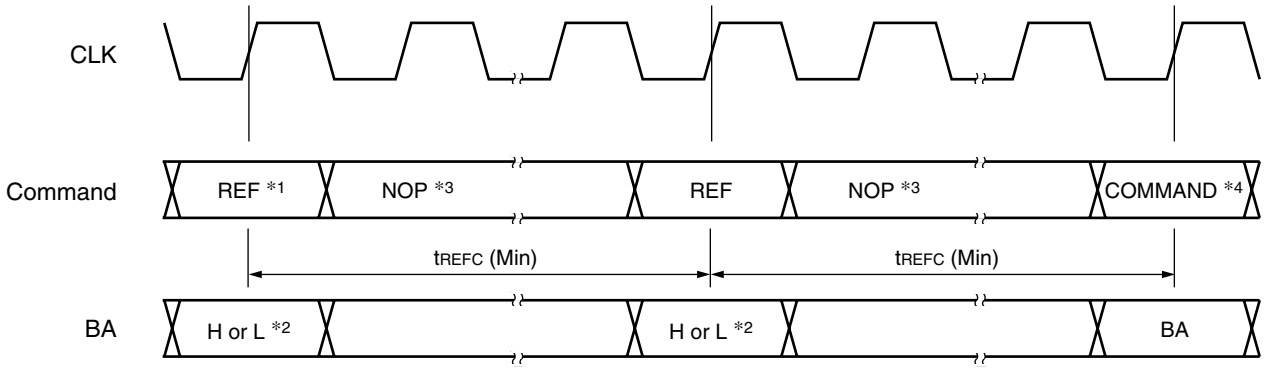
*1 : Precharge at read with Auto-precharge command (READA) is started from number of clocks that is the same as Burst Length (BL) after the READA command is asserted.
*2 : Next ACTV command should be issued after BL + t_{RP} (Min) from READA command.

14. WRITE WITH AUTO-PRECHARGE (EXAMPLE @ CL = 3, BL = 2, Applied to same bank) *1, *2, *3



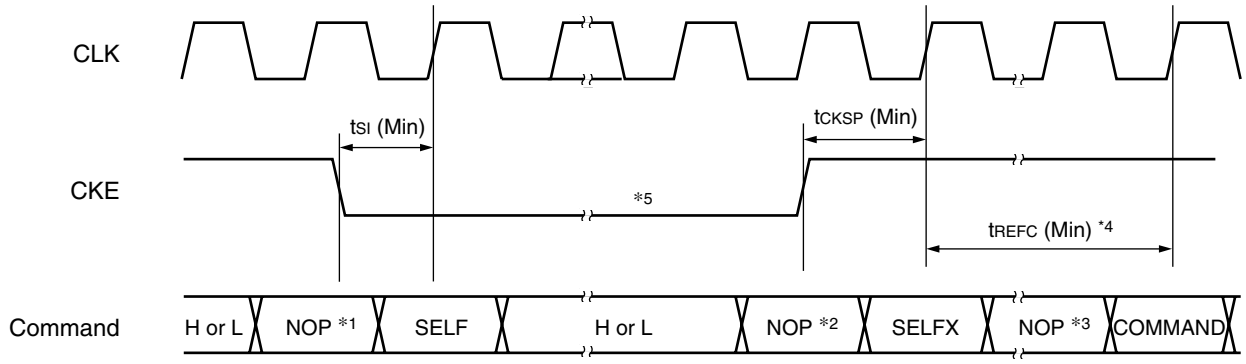
*1 : Even if the final input data are masked by DQM, the precharge is started at same timing as the case final data are not masked.
*2 : Once auto precharge command is asserted, no new command within the same bank can be issued.
*3 : Auto-precharge command doesn't affect at full column burst operation except Burst Read & Single Write.
*4 : Precharge at write with Auto-precharge is started after 1 clock at CL = 2, 2 clocks at CL = 3 from the end of burst.
*5 : Next command should be issued after BL + t_{RP} (Min) at CL = 2, BL + 1 + t_{RP} (Min) at CL = 3 from WRITA command.

15. AUTO-REFRESH



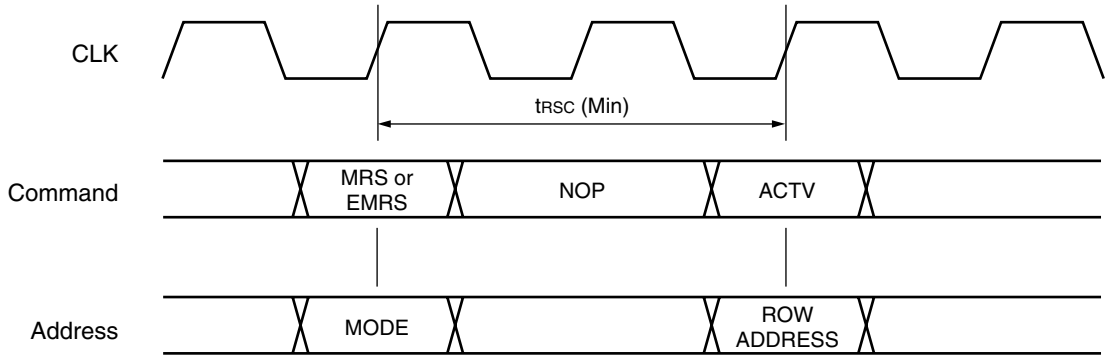
*1 : All banks should be precharged prior to the first Auto-refresh command (REF) .
*2 : Bank select is ignored at REF command. The refresh address and bank select are selected by internal refresh counter.
*3 : Either NOP or DESL command should be asserted during t_{REFC} period while Auto-refresh mode.
*4 : Any activation command such as ACTV or MRS command other than REF command should be asserted after t_{REFC} from the last REF command.

16. SELF-REFRESH ENTRY AND EXIT



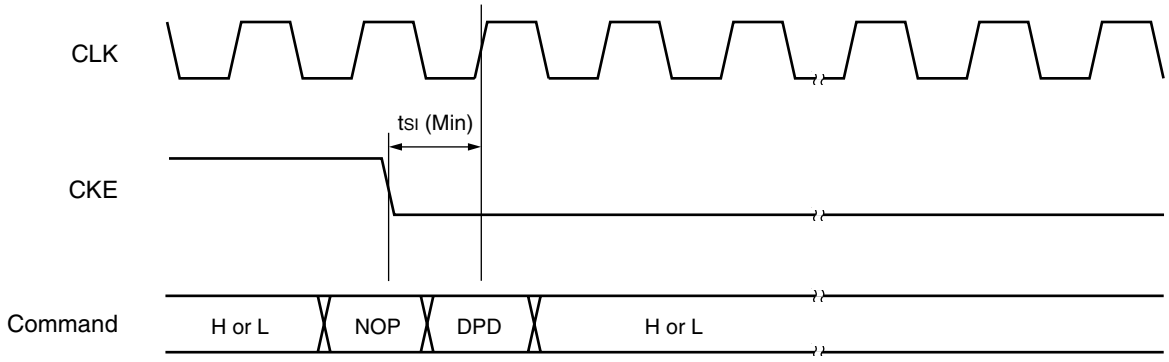
*1 : Precharge command (PRE or PALL) should be asserted if any bank is active prior to Self-refresh Entry command (SELF) .
*2 : The Self-refresh Exit command (SELFX) is latched after t_{CKSP} (Min) . It is recommended to apply NOP command on the rising edge of CKE.
*3 : Either NOP or DESL command can be asserted during t_{REFC} period.
*4 : CKE should be held High during t_{REFC} period after t_{CKSP}.
*5 : CKE level should be held less than 0.2 V during self-refresh mode.

17. MODE REGISTER SET



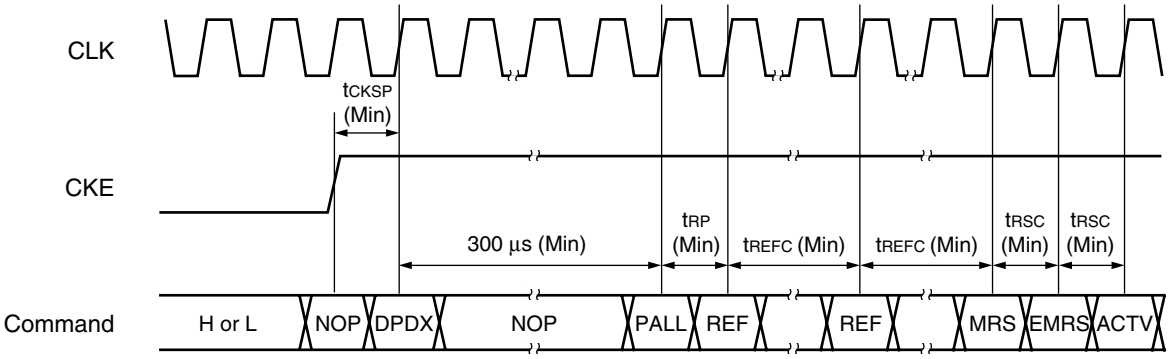
Note : The Mode Register Set command (MRS) or Extended Mode Register Set command (EMRS) should only be asserted after all banks have been precharged.

18. DEEP POWER DOWN ENTRY



Note : Deep Power Down Entry command (DPD) should only be asserted if all banks have been precharged and all outputs are in High-Z.

19. DEEP POWER DOWN EXIT



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