Features

- **13.56 MHz RFID Chip for Cards or Tags**
- **2048-bit Read/Write RFID EEPROM**
- **ISO 14443-2 Type B Compliant**
- **Full ISO 14443-3 Compliant Anticollision**
- **100,000 Write Cycle Reliability**
- **3 ms Write Time**
- **Password and Lockwrite Protection**
- **82 pF Tuning Capacitor**
- **0 – 70°C Operation**

Description

The AT88RF020 is a low-end 13.56 MHz RFID (Radio Frequency IDentification) device that includes an on-chip EEPROM-based (nonvolatile) memory. The wireless interface complies with Type B operation of ISO/IEC 14443. The specific sections of compliance are 14443-1, as well as 14443-2:1999(E) (dated 5/2/00) and 14443-3:2000(E) (dated 7/13/00).

This device is designed to be used in applications where one or more RFID devices will be simultaneously placed within an intelligent reader/writer RF field. Communication between the RF reader/writer and this device will take place through the use of the featured anticollision command set supported by this device.

The memory contains a total of 2048 bits, organized as 32 64-bit pages. Write operations are designed to complete in less than three milliseconds (ms). The endurance rating for the memory is 100,000 write cycles per byte.

This device supports these security features: password checking, data locking, a one-way counter and a guaranteed unique serial number.

The AT88RF020 includes an on-chip internal tuning capacitor that enables it to operate with a single external coil antenna. This antenna completes the RFID channel.

Figure 1. Block Diagram
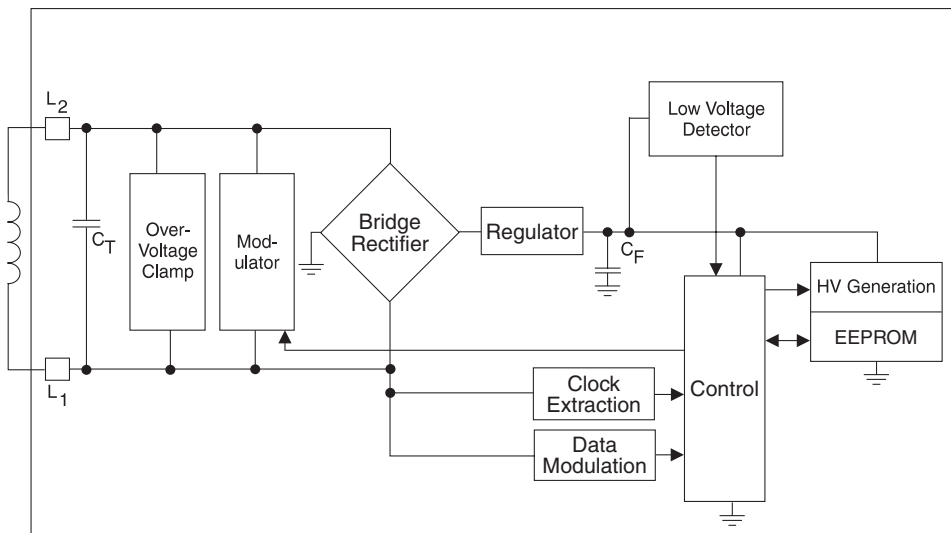
13.56 MHz, 2048-bit RFID EEPROM

AT88RF020

All bits are sent to or read from the chip least significant bit first. Bit fields listed in this document are listed with the LSB on the left and the MSB on the right. Multibyte information is sent to the chip least significant byte first.

The first byte sent to the chip is stored in memory at the lowest address, and the internal address is incremented for subsequent bytes. Information is read from the memory and transmitted by the chip in exactly the same order in which it was written: the first bit written is the first bit read.

This specification follows the nomenclature found within the ISO/IEC 14443 document. Proximity Coupling Device (PCD) is the reader/writer, and Proximity Integrated Circuit Card (PICC) is the tag/card. ETU refers to Elementary Time Unit, which is the time required to transmit or receive one bit. One ETU is equal to 128 carrier cycles (9.439 µs). RFU refers to any feature, item, bit field or bit that is held as Reserved for Future Use. When the reader/writer sends data to this device, RFU bits should always be "0". When this device sends data to the reader/writer, RFU bits are undefined.

Memory Map

The memory array within this device is organized as shown in Table 1.

Table 1. Memory Map

	Byte 0	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**
Page 0	Pseudo Unique PICC ID				LockBits			
Page 1	Application Data				Reserved			
Page 2	Signature						Counter	
Page 3	Password							
Page 4	—	—	—	—	—	—	—	—
...								
...								
...								
Page 31	—	—	—	—	—	—	—	—

Bytes marked "–" in Table 1 are user-defined and will be set to 0x00 upon shipment from Atmel. The chip accesses these bytes using specific commands described later in this document.

A total of 1904 bits (238 bytes) are available for user-defined purposes, including the Reserved and Signature fields but excluding the PUPI, LockBits, Counter and Password fields in the above memory map.

The fields named above are defined as follows:

Pseudo Unique PICC Identifier: This PUPI field is a unique serial number permanently written into the device's nonvolatile memory at the Atmel factory during wafer probe/test. It cannot be modified and is guaranteed to be unique for all AT88RF020 devices. Customers desiring serial numbers longer than 32 bits are expected to use other locations within the memory, including the Reserved field within Page 1.

Application Data: This field is transmitted unmodified from the card to the reader/writer as part of the ATQB command response.

Counter: This field is automatically incremented by the device whenever the COUNT instruction is executed. It is factory set to the value of zero upon shipment from Atmel.

Signature: This field is written unmodified into the first six bytes of Page 2 via the COUNT instruction. It is expected that this value will be related to the count and may be encrypted by the reader/writer. In this manner, the Counter and Signature fields together can provide an additional level of security from tampering.

Pages 0, 1 and 2 can always be read by the system; Page 3 may never be read by the system; and all remaining pages can be read only after the proper password has been sent to the chip. The LockBits field within Page 0 can be modified only through the use of the LOCK command and only after the proper password has been sent to the chip. The contents of Page 2 can only be modified using the COUNT command—again, only after the proper password has been sent to the chip.

All other pages (1 and 3 through 31) can be written to only after the proper password has been validated by the chip. The first four bytes of Page 0 comprise the serial number (PUPI) and, although the adjacent LockBits field is updateable, the serial number can never be changed during any kind of operation.

Communications

The electrical signaling of the chip is fully compatible with ISO 14443-2, "Radio Frequency Power and Signal Interface," version 1999(e) for Type B only. Anticollision operation and frame formatting is compatible with ISO 14443-3 Type B, "Initialization and Anticollision," version 2000(e), Type B only.

Command/Data Transmission Frame

All data sent between the PICC and PCD is sent as characters (see ISO 14443-3, section 7.1.1). The character is composed of a start bit (logic "0"), 8 bits of data and a stop bit (logic "1").

Between characters is an extra guard time (EGT) that must not exceed 6 ETUs (~57 microseconds (µs)) for data sent to the PICC and will be two ETUs for data sent to the PCD (see ISO 14443-3, section 7.1.2).

The PICC will automatically resynchronize character reception (internal clocks) with the start bit of each incoming character.

Groups of characters exchanged between the PCD and PICC comprise a frame, which is delimited by a Start of Frame (SOF) and an End of Frame (EOF) signal protocol (see ISO 14443-3, sections 7.1.3–7.1.5).

After the READ command has been received by the PICC, the PICC will respond with the data frame following a delay of 8 ETUs (~75.5 µs) and transmit a sub carrier for a period of 10 ETUs (~94.4 µs) with no phase changes (see ISO 14443-3, section 7.1.6, and ISO 14443-2, section 9.2.5.).

Note: This device ignores attempts to reduce the minimum TR0 and TR1 values from the ISO 14443-2 defaults as may be specified by the PCD in the ATTRIB command (see ISO 14443-3, sections 7.10.3.1 and 7.10.3.2.).

CRC

A 2-byte CRC code is included in all frame transmissions. The CRC polynomials are defined as:

$$x^{16} + x^{12} + x^5 + x^0$$

This is a hex polynomial of 1021. The CRC register is initialized to 0xFFFF. When receiving information from the system, the device computes the CRC on the incoming command, data and CRC bytes (start/stop bits, SOT, EOT and EGT are ignored). When the last bit of the CRC has been received, the value in the CRC register should be 0x0000. When the device transmits data, the CRC is computed based on all outgoing data bits.

Anticollision

Anticollision is implemented as per ISO 14443-3, Type B (see ISO 14443-3, sections 7.3 and 7.4). There are four primitive commands that support the anticollision scheme: REQB/WUPB, SlotMARKER, ATTRIB and HLTB.

REQB/WUPB Command

This 5-byte command (see ISO 14443-3, section 7.7) is used for the PCD to probe the field for PICCs or to wake up PICCs that are in the HALT state. The first byte must be a fixed 0x05. This chip will respond only to values of 0x00 or 0x01 in the second (AFI) byte. Bit 3 of the third byte is used to select between REQB and WUPB commands, while Bits 0–2 are used to set N, which is used for the command response (ATQB). If the PICC receives a WUPB command with an invalid AFI code, then it will remain in the HALT state.

When the PICC receives one of these commands properly encoded, it will generate a random number (R) of up to four bits, according to the value of N passed by the PCD and specified in Table 13 of ISO 14443-3 and in Table 2 on page 4. If N = 1 or the random number generator selects R = 1, then the PICC will send an ATQB and listen for REQB/WUPB, ATTRIB and HLTB commands. Otherwise, it will wait for the Slot-MARKER command that matches the value R selected by the random number generator.

Table 2. Command Codes

Binary Code (in cmd)	N	Size of R (in bits)
000	1	–
100	2	1
010	4	2
110	8	3
001	16	4

The response to both of these commands is an ATQB packet. This format is as specified in ISO 14443-3, section 7.9.1, with the following values:

PUPI:	As stored in memory (unique serial number)
Application Data:	As stored in memory
Protocol Info:	0x00, 0x00, 0x41
	(Bit_rate_capability: 106 Kbps only)
	(Max_frame_size: 16)
	(Protocol type: not compliant with 14443-4)
	(FWI: Frame Waiting Time minimal, 4.8 ms)
	(ADC: Application Data Coding is proprietary)
	(FO: Only CID (Card Identifier) supported by PICC)

ATTRIB Command

The ATTRIB command is used to select among all the chips that may have responded to a given REQB/WUPB command. The chip will respond to ATTRIB commands from 11 to 16 bytes in length where the 2nd, 3rd, 4th and 5th bytes exactly match the PUPI stored in the memory. If the chip responds to the ATTRIB command, it enters the ACTIVE state where the data transfer commands described above will be honored.

The PICC ignores all the PARAM bytes with the exception of the least significant four bits of PARAM4, which are stored within the chip as the CID for future responses. Any higher layer INF command is also ignored.

The PICC response to a valid ATTRIB command is always three bytes long. The first byte contains the CID in the lower nibble and 0x0 in the upper nibble. The next two bytes are the CRC.
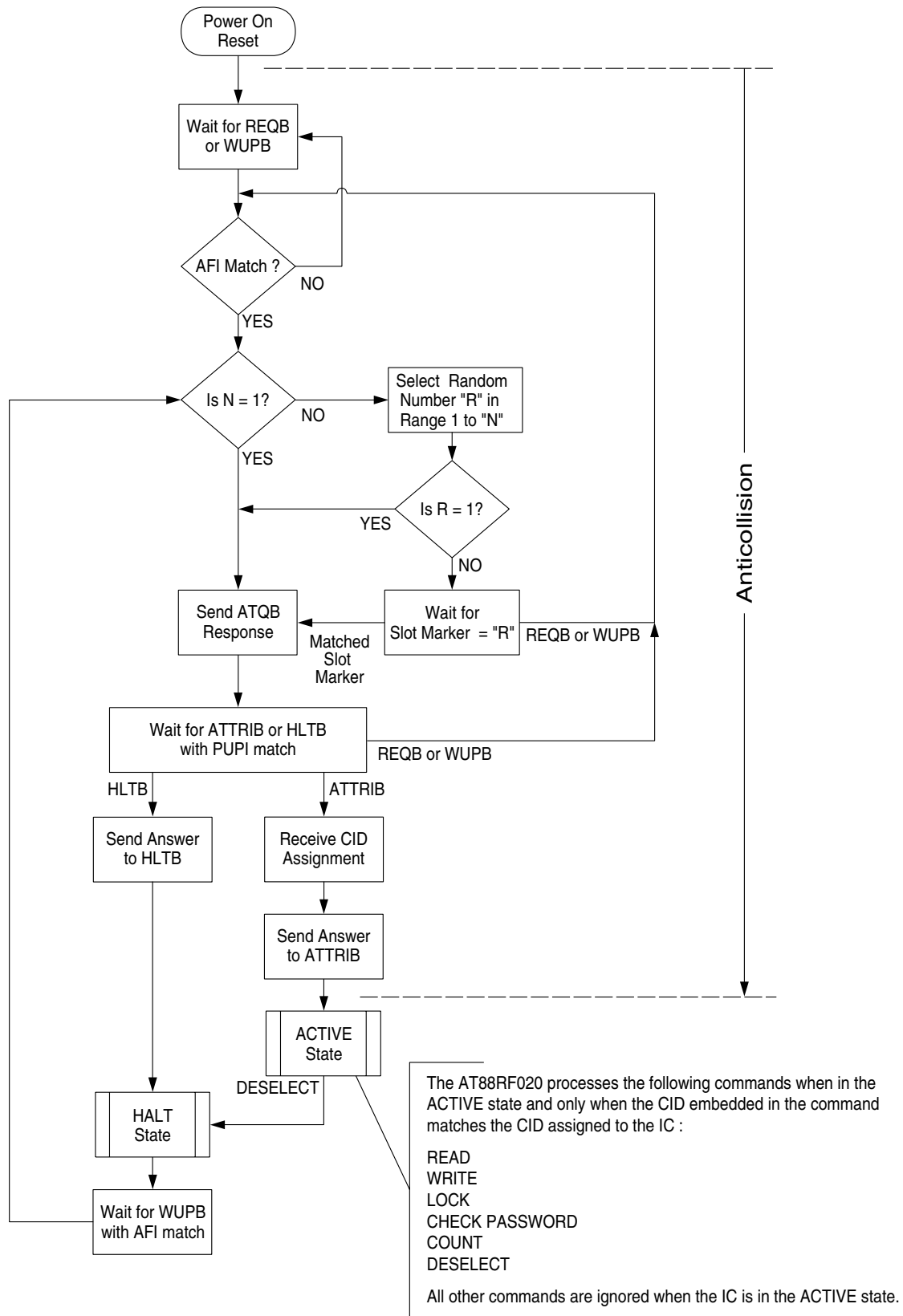
HLTB Command

The HLTB command is used to set the PICC to the HALT state, after which only the WUPB command will be acknowledged. The format of this 7-byte command is 0x50, PUPI (4 bytes), CRC (2 bytes). The chip always responds to a valid HLTB command with the 3-byte sequence: 0x00, CRC_0 and CRC_1. The HLTB command is not valid if the PICC is in the ACTIVE state (see ISO 14443-3 sections 7.4.7 and 7.12 for additional information).

SlotMARKER Command

The SlotMARKER command provides a way for the reader to query those cards for which the generated random number R is greater than 1. It is a 3-byte command, the last two of which are the CRC bytes. The least significant nibble of the first byte is the slot number, and if this matches the generated random number, then the ATQB response is generated. The chip will truncate the slot number field to match the value of N provided in the REQB command. The most significant nibble of this command is fixed at 0xA.

Figure 2. AT88RF020 Anticollision and State Transition Flow Chart


```
                    ┌─────────────┐
                    │  Power On   │
                    │   Reset     │
                    └──────┬──────┘
                           │
                    ┌──────▼──────┐
                    │ Wait for REQB│◄────┐
                    │   or WUPB    │     │
                    └──────┬───────┘     │
                           │             │
                      ◇ AFI Match ? ──NO─┘
                           │
                          YES
                           │
                      ◇ Is N = 1? ──NO──► Select Random Number "R" in Range 1 to "N"
                           │                         │
                          YES                   ◇ Is R = 1? ──YES──
                           │                         │
                           │                        NO
                           ▼                         ▼
                    Send ATQB Response ◄── Wait for Slot Marker = "R" ──REQB or WUPB
                           │         Matched Slot Marker
                           ▼
                    Wait for ATTRIB or HLTB with PUPI match ── REQB or WUPB
                     │HLTB                    │ATTRIB
                     ▼                        ▼
              Send Answer to HLTB      Receive CID Assignment
                                              │
                                              ▼
                                       Send Answer to ATTRIB
                                              │
                                              ▼
                                       ACTIVE State
                     ┌───DESELECT───────┘
                     ▼
              HALT State
                     │
                     ▼
              Wait for WUPB with AFI match
```

Anticollision

The AT88RF020 processes the following commands when in the ACTIVE state and only when the CID embedded in the command matches the CID assigned to the IC :

READ
WRITE
LOCK
CHECK PASSWORD
COUNT
DESELECT

All other commands are ignored when the IC is in the ACTIVE state.

Data Transfer Commands

The following commands are supported for data transfer when the chip is in the ACTIVE state (see ISO 14443-3, section 7.4.7). If the command is properly received (CRC correct, legal opcode and address, etc.), the chip will respond either with a NACK command, an ACK command or data. Otherwise, the chip will silently wait for a proper command. The chip supports additional commands as part of the anticollision sequencing; these commands are documented elsewhere in this data sheet. On-chip password checking is required for most operations. The coding of these commands is described in Table 3 and Table 4 on page 9.

Below is a description of the individual commands supported.

READ Command

The addressed 64-bit page referenced in the READ command is returned to the PCD. The PICC will respond with the data if the address is correct, the page is readable and the password has been sent; otherwise, it will respond with a NACK. Password checking is not required to read Pages 0, 1 and 2, but all other pages require a previously executed valid password check to read the chip. There is no byte read capability. Page 3 (the actual password) can never be read directly and is only accessed internally during the PASSWORD command. The chip will NACK any attempt to read Page 3.

WRITE Command

The 64-bit memory page referenced in the WRITE command is written with the data that follows the command byte. The chip ignores the upper 3 bits of the byte-wide memory address and the lower five bits from the memory address.

If the target page cannot be written to because the page is read only or is locked, or if the chip has not been properly opened to access with a valid password, then a NACK command will be issued by the PICC. Otherwise, an ACK command will be transmitted *after* the memory write operation has been completed.

Reader/writer modulation is prohibited during the memory write time, which is the time period between the PCD's EOF and the issuance of the PICC's ACK command. This period is less than 3 ms and is considered to be an extended TR0 wait interval, as per ISO 14443.

Memory is never modified if a NACK command is issued. Pages 0 and 2 (PUPI, Lock-Bits, Signature and Counter) cannot be written with this command. Addressing either Page 0 or Page 2 within the WRITE command will result in a NACK command being issued by the device.

LOCK Command

The LOCK command can be executed only after proper password validation has been performed. The LOCK command locks the addressed memory location from future changes. The memory location can still be read with proper password validation. The last 31 bits of data within the LOCK command are logically ORed within the device with the 31-bit value stored within the LockBits field of Page 0 (see *Memory Map,* Table 1 on page 2). The result is then written back into the memory. After the memory has been written, an ACK command will be transmitted. A NACK command is issued if the LOCK command is attempted without previous password validation.

If power is interrupted during this write, all bits within LockBits may be set to "1", and the chip may be disabled. The first 33 bits of data sent within the command to the PICC are ignored.

The bits within the LockBits field correspond to the pages within the memory and, if set to "1", prevent all future writes to the corresponding page; i.e., LockBits field bit 6 locks Page 6 when it is set to a "1". There is no mechanism to ever "unlock" a page, so once a page is locked, it can never be unlocked and, as such, can never be modified. The 31-bit LockBits field is set to all "0"s upon shipment from the factory. Bit 0 of the LockBits

field is ignored for obvious reasons, since it would normally point to memory Page 0, which contains the embedded PUPI (serial number) and the actual LockBits field.

A command to lock Page 0 with password access will result in an ACK command being issued with no other effects, since Page 0 can never be locked. Attempting to lock Page 0 is not viewed as an error, so the command will be executed in the normal manner.

CHECK PASSWORD Command

The 64-bit value embedded within the CHECK PASSWORD command is compared to the password stored within Page 3 of the memory (See *Memory Map,* Table 1 on page 2). If the input password matches the stored password, then the chip will reply with an ACK command, and the device will be open to access. If the input password does not match the internally stored password, then the chip will reply with a NACK command.

This command must be executed (and the proper password sent) before most device accesses are allowed (some accesses are permitted without password validation). The chip will remain accessible until power is removed or an incorrect password is sent to the chip. If a subsequent password check fails, the chip will become inaccessible until a valid password check is again executed.

Once the password has been properly acknowledged and device access opened, the current password can be changed using the WRITE command. The device will remain ACTIVE after the new password has been written until power is removed or until a subsequent invalid password check occurs.

The only password that is not allowed is the "all ones" password. If the CHECK PASSWORD command is attempted for an "all ones" password, the device will respond with a NACK command. If the "all ones" password is validly programmed into this device using the WRITE command, the device will forever be locked out of future password validated accesses.

It is strongly suggested that the "all zeroes" password be avoided since this password is considered too simplistic and could represent a security risk. The device is delivered with all zeros in the password page.

DESELECT Command

If the DESELECT command is properly received and the PICC is in the ACTIVE state, the PICC will issue an ACK command and enter the HALT state. Its functionality is identical to HLTB as described in the anticollision section. A NACK response is never issued following this command (see ISO 14443-3, section 7.4.7).

COUNT Command

The COUNT command is used to write Page 2. The first six bytes sent by the PCD (referred to as the Signature) are written to the first six bytes of Page 2 unmodified. The last two bytes of data sent by the PCD in the COUNT command are only placeholders and will be ignored.

The 16-bit value stored in the counter field of Page 2 is incremented by one each time COUNT is executed. Once the value of the counter reaches 0x8000, no further count operations will be executed, and Page 2 will be effectively locked against further modification. Password validation must occur before the COUNT command is permitted.

The chip will compute the new incremented count that will be written into the last two bytes of Page 2 immediately following the incoming 6-byte data field. It is expected that at least part of the 6-byte value will be the result of an externally computed cryptographic operation on the new Counter value, thus permitting some degree of transaction validation.

If the write cannot take place (because Counter has a value of 0x8000, Page 2 is locked or no password has been sent), then a NACK command will be issued by the PICC; otherwise, an ACK command will be transmitted after the write has completed.

Data Transfer Command Formats

The first byte of each command includes the CID as the least significant nibble followed by the command opcode (COP) as the most significant nibble. COP is encoded according to Table 3.

Table 3. Command Summary

LSB		MSB		Command	Description
0	0	1	0	READ	64-bit page from memory
1	1	0	0	WRITE	64-bit page to memory
0	1	0	0	LOCK	Data is ORed with existing LockBits value
0	1	1	0	CHECK PASSWORD	
0	1	0	1	DESELECT	
0	1	1	1	COUNT	

All these commands consist of 12 bytes to be sent to the PICC by the PCD. CID is the card ID byte as received by the PICC during the anticollision sequence. The address field in the following chart is a 5-bit value, and the device ignores the most significant three bits of the byte. Therefore, the device will interpret a value of 0xFF as 0x1F.

The command bytes are shown in Table 4.

Table 4. Command Bytes

Commands	1st Byte	2nd Byte	3rd–10th Bytes	11th Byte	12th Byte
READ	CID | 0x4	Address	Ignored	CRC_0	CRC_1
WRITE	CID | 0x3	Address	64 bits data	CRC_0	CRC_1
LOCK	CID | 0x2	Ignored	32 bits ignored, 32 bits data	CRC_0	CRC_1
CHECK PASSWORD	CID | 0x6	Ignored	64 bits data	CRC_0	CRC_1
DESELECT	CID | 0xA	Ignored	Ignored	CRC_0	CRC_1
COUNT	CID | 0xE	Ignored	16 bits ignored, 48 bits data	CRC_0	CRC_1

A valid READ command response is a 12-byte frame sent from the PICC to the PCD and is formatted as shown in Table 5.

Table 5. PICC Frame Format

Commands	1st Byte	2nd Byte	3rd–10th Bytes	11th Byte	12th Byte
READ	CID	0x4	Address	64 bits data	CRC_0	CRC_1

Both the ACK and NACK responses consist of a 4-byte frame sent from the PICC to the PCD and are formatted as shown in Table 6.

Table 6. ACK and NACK

Description	1st Byte	2nd Byte	3rd Byte	4th Byte
ACK	CID	COP	0xX0	CRC_0	CRC_1
NACK	CID	COP	0xX1	CRC_0	CRC_1

There are two parts to the second byte of the ACK and NACK response commands (see Table 6): the most significant nibble and the least significant nibble.

For each command, the most significant nibble is not guaranteed, and therefore the reader/writer should mask this field when assessing whether an ACK or a NACK has been issued by the PICC. As indicated in Table 6, the least significant nibble of the second byte will always be a "0" for an ACK and a "1" for a NACK.

For an ACK, the most significant nibble of the second byte will be undefined. For a NACK, the most significant nibble of the second byte contains an error feedback code. This error code represents the error that caused the NACK response command.

Table 7. Error Codes

ACK/NACK 2nd Byte								Command Decode
X	X	X	X	0	0	0	0	ACK, no errors detected
0	0	0	1	0	0	0	1	NACK, attempted write to locked page
X	X	1	0	0	0	0	1	NACK, terminal count reached or attempted operation to invalid address
0	1	0	0	0	0	0	1	NACK, invalid password attempted
1	0	0	0	0	0	0	1	NACK, low-voltage condition detected

Electrical

This device includes a voltage reference to ensure that the chip operates only when the power supply voltage on the chip is above a required level of 1.8 – 2.0 volts. Memory writes are guaranteed above this voltage level. The on-chip regulator will ensure that the VDD voltage will be within the range of 2.1 – 2.5 volts.

The chip is specified to operate over the temperature range of 0°C to 70°C (junction temperature). The coil pads (*ac1* and *ac2*) offer ESD protection at levels greater than 2 kV.
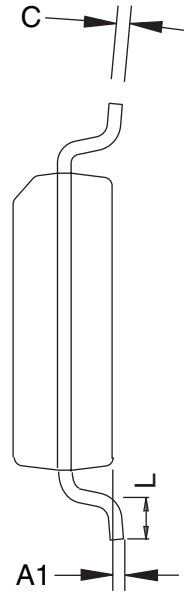
The input capacitance of the coil pins will be 82 pf and may vary by ±10% over process, temperature, voltage and frequency. Internal power supply bypass capacitance is integrated on the chip.
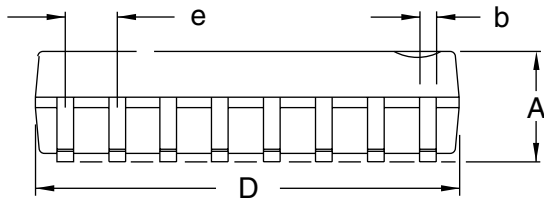
Package Drawing

16S2 – SOIC
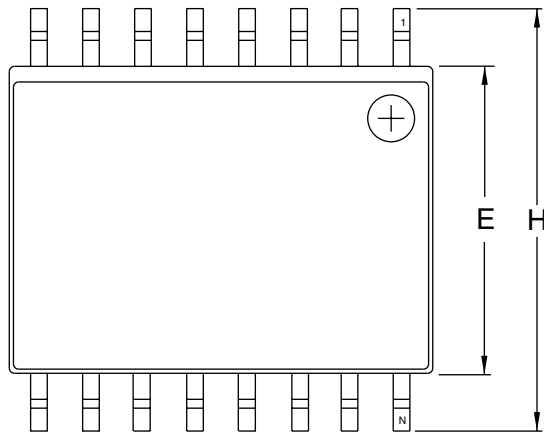
Top View

End View

Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.0926	–	0.1043	
A1	0.0040	–	0.0118	
b	0.0130	–	0.0200	5
C	0.0091	–	0.0125	
D	0.3977	–	0.4133	2
E	0.2914	–	0.2992	3
H	0.3940	–	0.4190	
L	0.0160	–	0.050	4
e	0.050 BSC			

Notes: 1. This drawing is for general information only; refer to JEDEC drawing MS-013, Variation AA for additional information.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006") per side.
3. Dimension E does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010") per side.
4. L is the length of the terminal for soldering to a substrate.
5. The lead width B, as measured 0.36 mm (0.014") or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024") per side.

1/9/02

	TITLE	**DRAWING NO.**	**REV.**
2325 Orchard Parkway San Jose, CA 95131	**16S2**, 16-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	16S2	A

Mechanical

Package Sample Pinout

Pin 1 = AC1

Pin 16 = AC2

All other pins should float.

Pad Information

The layout of the die is shown in Figure 3 on page 13. The antenna coil contact pads (*ac1* and *ac2*) and the test 5, 6 and 7 pad passivation openings are 90x90 microns. The antenna coil and test 5, 6 and 7 pads are designed to be compatible with current factory production bump mounting processes.

Ordering Information

Ordering Code	Package	Operation Range
AT88RF020-WA1	Die on Wafer, 82 pf	Commercial
AT88RF020-MR1	RF Module R (XOA2), 82 pf, Green	(0°C to 70°C)

Die Layout

Figure 3. Die Layout
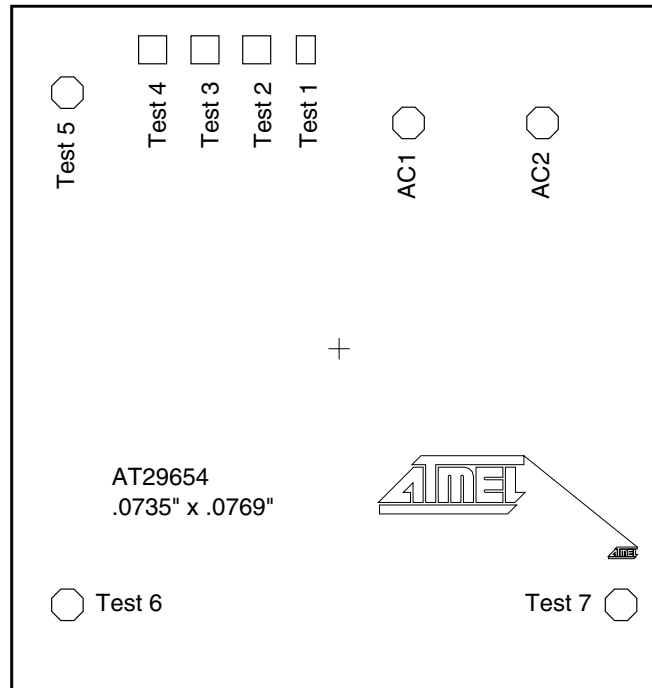
Overall Die Size:	1.866 mm x 1.953 mm	73.5 mils x 76.9 mils
Pad Size:	80 μm (square pad)	3.1 mils
	90 μm (octagon pad)	3.5 mils

Pad Location

AC1	X=	198.44 μm	X=	7.813 mils
	Y=	645.44 μm	Y=	25.411 mils
AC2	X=	581.40 μm	X=	22.890 mils
	Y=	645.44 μm	Y=	25.411 mils
Test 1	X=	−102.54 μm	X=	−4.037 mils
	Y=	854.48 μm	Y=	33.641 mils
Test 2	X=	−235.68 μm	X=	−9.279 mils
	Y=	854.48 μm	Y=	33.641 mils
Test 3	X=	−383.44 μm	X=	−15.096 mils
	Y=	854.48 μm	Y=	33.641 mils
Test 4	X=	−533.20 μm	X=	−20.992 mils
	Y=	854.48 μm	Y=	33.641 mils
Test 5	X=	−776.80 μm	X=	−30.583 mils
	Y=	732.00 μm	Y=	28.819 mils
Test 6	X=	−776.80 μm	X=	−30.583 mils
	Y=	−732.00 μm	Y=	−28.819 mils
Test 7	X=	805.84 μm	X=	31.726 mils
	Y=	−732.00 μm	Y=	28.819 mils

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
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