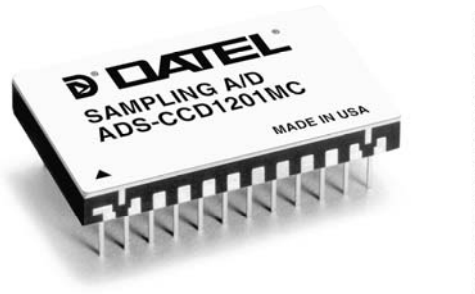
INNOVATION and EXCELLENCE

ADS-CCD1201

12-Bit, 1.2MHz, Sampling A/D's Optimized for CCD Applications

FEATURES

- **Unipolar input range (0 to +10V)**
- **1.2MHz sampling rate**
- **4096-to-1 dynamic range (72.2dB)**
- **Low noise, 400µVrms (1/6 of an LSB)**
- **Outstanding differential nonlinearity error (±0.35 LSB max.)**
- **Small, 24-pin ceramic DDIP**
- **Low power, 1.7 Watts**
- **Operates from ±12V or ±15V supplies**
- **Edge-triggered, no pipeline delay**



GENERAL DESCRIPTION

The functionally complete, easy-to-use ADS-CCD1201 is a 12-bit, 1.2MHz Sampling A/D Converter whose performance and production testing have been optimized for use in electronic imaging applications, particularly those employing charge coupled devices (CCD's) as their photodetectors. The ADS-CCD1201 delivers the lowest noise (400µVrms) and the best differential nonlinearity error (±0.35LSB max.) of any commercially available 12-bit A/D in its speed class. It can respond to full scale input steps (from empty to full well) with less than a single count of error, and its input is immune to overvoltages that may occur due to blooming.

Packaged in an industry-standard, 24-pin, ceramic DDIP, the ADS-CCD1201 requires ±15V (or ±12V) and +5V supplies and typically consumes 1.7 (1.4) Watts. The device is 100% production tested for all critical performance parameters and is fully specified over both the 0 to +70°C and –55 to +125°C operating temperature ranges.

For those applications using correlated double sampling, the ADS-CCD1201 can be supplied without its internal sample-hold amplifier. DATEL will also entertain discussions about including the CDS circuit internal to the ADS-CCD1201. Please contact us for more details.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	24	–12V/–15V SUPPLY
2	BIT 11	23	GROUND
3	BIT 10	22	+12V/+15V SUPPLY
4	BIT 9	21	+10V REFERENCE OUT
5	BIT 8	20	ANALOG INPUT
6	BIT7	19	GROUND
7	BIT 6	18	NO CONNECT
8	BIT 5	17	NO CONNECT
9	BIT 4	16	START CONVERT
10	BIT 3	15	$\overline{\text{EOC}}$
11	BIT 2	14	GROUND
12	BIT 1 (MSB)	13	+5V SUPPLY

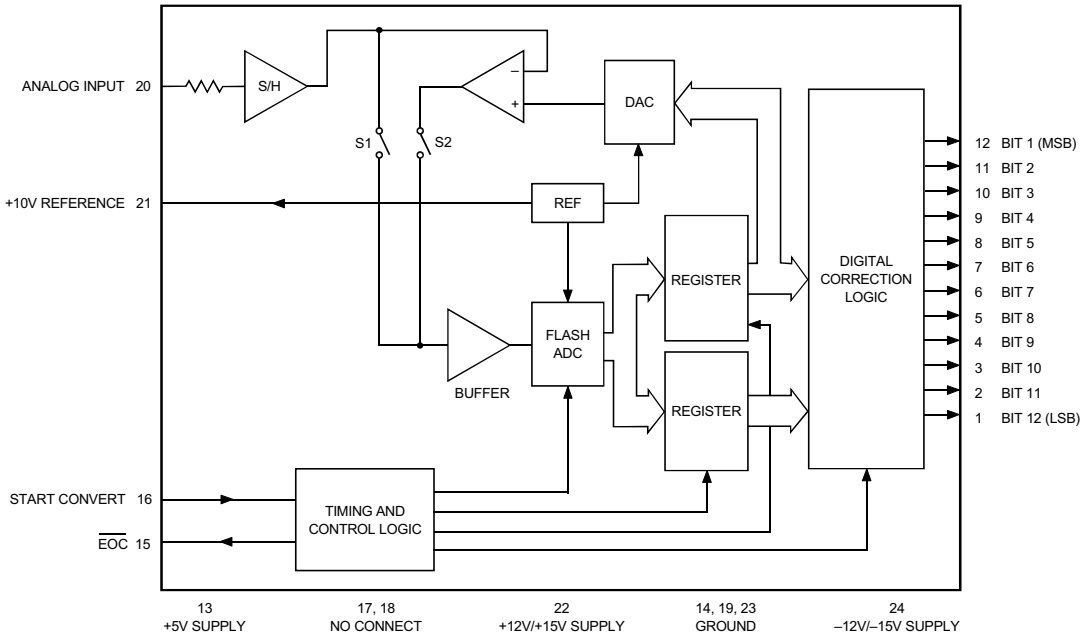


Figure 1. ADS-CCD1201 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+12V/+15V Supply (Pin 22)	0 to +16	Volts
–12V/–15V Supply (Pin 24)	0 to –16	Volts
+5V Supply (Pin 13)	0 to +6	Volts
Digital Input (Pin 16)	–0.3 to +V_{DD} +0.3	Volts
Analog Input (Pin 20)	–4 to +17	Volts
Lead Temp. (10 seconds)	+300	℃

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
ADS-CCD1201MC	0	—	+70	℃
ADS-CCD1201MM	–55	—	+125	℃
Thermal Impedance				
θ_{jc}	—	5	—	°C/Watt
θ_{ca}	—	24	—	°C/Watt
Storage Temperature Range	–65	–	+150	℃
Package Type	24-pin, metal-sealed ceramic DDIP			
Weight	0.42 ounces (12 grams)			

FUNCTIONAL SPECIFICATIONS

(T_A = +25°C, ±Vcc = ±15V (or ±12V), +V_{DD} = +5V, 1.2MHz sampling rate, and a minimum 1 minute warmup① unless otherwise specified.)

	+25°C			0 to +70°C			–55 to +125° C			
ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage Range ②	—	0 to +10	—	—	0 to +10	—	—	0 to +10	—	Volts
Input Resistance	—	1	—	—	1	—	—	1	—	kΩ
Input Capacitance	—	7	15	—	7	15	—	7	15	pF
DIGITAL INPUTS										
Logic Levels										
Logic "1"	+2.0	—	—	+2.0	—	—	+2.0	—	—	Volts
Logic "0"	—	—	+0.8	—	—	+0.8	—	—	+0.8	Volts
Logic Loading "1"	—	—	+20	—	—	+20	—	—	+20	µA
Logic Loading "0"	—	—	–20	—	—	–20	—	—	–20	µA
Start Convert Positive Pulse Width ③	—	100	—	—	100	—	—	100	—	ns
STATIC PERFORMANCE										
Resolution	—	12	—	—	12	—	—	12	—	Bits
Integral Nonlinearity (fin = 10kHz)	—	±0.5	—	—	±0.5	—	—	±1	—	LSB
Differential Nonlinearity (fin = 10kHz)	—	+0.25	±0.35	—	±0.25	±0.35	—	±0.35	±0.75	LSB
Full Scale Absolute Accuracy	—	+0.1	±0.3	—	±0.2	±0.5	—	±0.3	±0.5	%FSR
Offset Error (Tech Note 2)	—	±0.05	±0.15	—	±0.1	±0.15	—	±0.15	±0.4	%FSR
Gain Error (Tech Note 2)	—	±0.1	±0.3	—	±0.2	±0.5	—	±0.3	±0.5	%
No Missing Codes (fin = 10kHz)	12	—	—	12	—	—	12	—	—	Bits
DYNAMIC PERFORMANCE										
Peak Harmonics (–0.5dB)										
dc to 100kHz	—	–86	–80	—	–86	–80	—	–82	–76	dB
100kHz to 500kHz	—	–84	–78	—	–84	–78	—	–81	–75	dB
Total Harmonic Distortion (–0.5dB)										
dc to 100kHz	—	–84	–79	—	–84	–79	—	–77	–71	dB
100kHz to 500kHz	—	–82	–77	—	–82	–77	—	–76	–70	dB
Signal-to-Noise Ratio (w/o distortion, –0.5dB)										
dc to 100kHz	72	73	—	72	73	—	70	72	—	dB
100kHz to 500kHz	71	72	—	71	72	—	70	72	—	dB
Signal-to-Noise Ratio ④ (8 distortion, –0.5dB)										
dc to 100kHz	71	73	—	71	73	—	68	71	—	dB
100kHz to 500kHz	71	72	—	71	72	—	68	71	—	dB
Two-tone Intermodulation Distortion (fin = 100kHz, 240kHz fs = 1.2MHz, –0.5dB)	—	–85	—	—	–84	—	—	–83	—	dB
Noise	—	400	—	—	500	—	—	700	—	µVrms
Input Bandwidth (–3dB)										
Small Signal (–20dB input)	—	7.5	—	—	7.5	—	—	7.5	—	MHz
Large Signal(–0.5dB input)	—	6	—	—	6	—	—	6	—	MHz
Feedthrough Rejection (fin = 500kHz)	—	84	—	—	84	—	—	84	—	dB
Slew Rate	—	±60	—	—	±60	—	—	±60	—	V/µs
Aperture Delay Time	—	±20	—	—	±20	—	—	±20	—	ns
Aperture Uncertainty	—	5	—	—	5	—	—	5	—	ps rms
S/H Acquisition Time (to ±0.01%FSR, 10V step)	360	400	440	360	400	440	360	400	440	ns
Overvoltage Recovery Time ⑤	—	400	833	—	400	833	—	400	833	ns
A/D Conversion Rate	1.2	—	—	1.2	—	—	1.2	—	—	MHz

	+25°C			0 to +70°C			–55 to +125°C			
ANALOG OUTPUT	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Internal Reference										
Voltage	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	+9.95	+10.0	+10.05	Volts
Drift	—	±5	—	—	±5	—	—	±5	—	ppm/ºC
External Current	—	—	1.5	—	—	1.5	—	—	1.5	mA
DIGITAL OUTPUTS										
Logic Levels										
Logic "1"	+2.4	—	—	+2.4	—	—	+2.4	—	—	Volts
Logic "0"	—	—	+0.4	—	—	+0.4	—	—	+0.4	Volts
Logic Loading "1"	—	—	–4	—	—	–4	—	—	–4	mA
Logic Loading "0"	—	—	+4	—	—	+4	—	—	+4	mA
Delay, Falling Edge of EOC to Output Data Valid	—	—	35	—	—	35	—	—	35	ns
Output Coding	Straight Binary									
POWER REQUIREMENTS, ±15V										
Power Supply Range										
+15V Supply	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	Volts
–15V Supply	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	–14.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+15V Supply	—	+50	+65	—	+50	+65	—	+50	+65	mA
–15V Supply	—	–40	–50	—	–40	–50	—	–40	–50	mA
+5V Supply	—	+70	+85	—	+70	+85	—	+70	+85	mA
Power Dissipation	—	1.7	1.9	—	1.7	1.9	—	1.7	1.9	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V
POWER REQUIREMENTS, ±12V										
Power Supply Range										
+12V Supply	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	+11.5	+12.0	+12.5	Volts
–12V Supply	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	–11.5	–12.0	–12.5	Volts
+5V Supply	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	Volts
Power Supply Current										
+12V Supply	—	+50	+65	—	+50	+65	—	+50	+65	mA
–12V Supply	—	–40	–48	—	–40	–48	—	–40	–48	mA
+5V Supply	—	+70	+80	—	+70	+80	—	+70	+80	mA
Power Dissipation	—	1.4	1.6	—	1.4	1.6	—	1.4	1.6	Watts
Power Supply Rejection	—	—	±0.01	—	—	±0.01	—	—	±0.01	%FSR/%V

Footnotes:

① All power supplies must be on before applying a start convert pulse. All supplies and the clock (START CONVERT) must be present during warmup periods. The device must be continuously converting during this time. There is a slight degradation in performance when using ±12V supplies.

② Contact DATEL for availability of other input voltage ranges.

③ A 100ns wide start convert pulse is used for all production testing.

④ Effective bits is equal to:

$$\frac{(\text{SNR + Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}\right]}{6.02}$$

⑤ This is the time required before the A/D output data is valid after the analog input is back within the specified range.

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-CCD1201 requires careful attention to pc-card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19, and 23) directly to a large ***analog*** ground plane beneath the package.

   Bypass all power supplies, as well as the REFERENCE OUTPUT (pin 21), to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible. If the user-installed offset and gain adjusting circuit shown in Figure 2 is used, also locate it as close to the ADS-CCD1201 as possible.

2. ADS-CCD1201 achieves its specified accuracies without external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the input circuit of Figure 2. When using this circuit, or any similar offset and gain-calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

3. When operating the ADS-CCD1201 from ±12V supplies, do not drive external circuitry with the REFERENCE OUTPUT (pin 21). The reference's accuracy and drift specifications may not be met, and loading the circuit may cause accuracy errors within the converter.

4. A passive bandpass filter is used at the input of the A/D for all production testing.

5. Applying a start pulse while a conversion is in progress ($\overline{EOC}$ = logic "1") initiates a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.

Table 1. Zero and Gain Adjust

Input Voltage Range	Zero Adjust +1/2 LSB	Gain Adjust +FS – 1 1/2 LSB
0 to +10V	+1.2207mV	+9.99634V

CALIBRATION PROCEDURE

(Refer to Figures 2 and 3)

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuit of Figure 2 are guaranteed to compensate for the ADS-CCD1201's initial accuracy errors and may not be able to compensate for additional system errors.

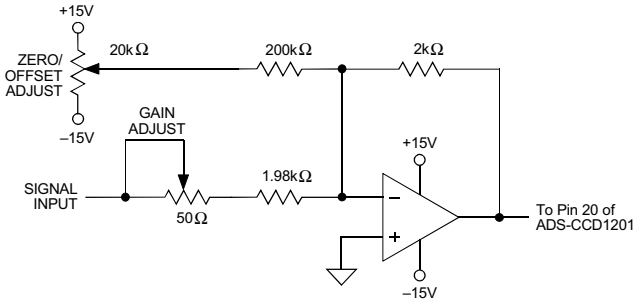


Figure 2. ADS-CCD1201 Calibration Circuit

All fixed resistors in Figure 2 should be metal-film types, and multi-turn potentiometers should have TCR's of 100ppm/°C or less to minimize drift with temperature. In many applications, the CCD will require an offset-adjust (black balance) circuit near its output and also a gain stage, presumably with adjust capabilities, to match the output voltage of the CCD to the input range of the AID. If one is performing a "system I/O calibration" (from light in to digital out), these circuits can be used to compensate for the relatively small initial offset and gain errors of the A/D. This would eliminate the need for the circuit shown in Figure 2.

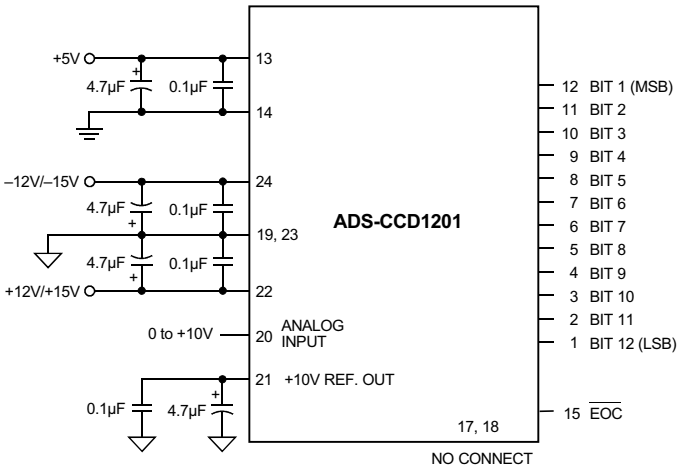


Figure 3. Typical ADS-CCD1201 Connection Diagram

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

For the ADS-CCD1201, offset adjusting is normally accomplished at the point where all output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is +1/2LSB (+1.2207mV).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus 1 1/2 LSB's (+9.99634V).

Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 16) so the converter is continuously converting. If using LED's on the outputs, a 200kHz conversion rate will reduce flicker.
2. Apply +1.2207mV to the ANALOG INPUT (pin 20).
3. Adjust the offset potentiometer until the output bits are 0000 0000 00000 and the LSB flickers between 0 and 1.

Gain Adjust Procedure

1. Apply +9.99634V to the ANALOG INPUT (pin 20).
2. Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.

Table 2. ADS-CCD1201 Output Coding

Input Voltage (0 to +10V)	Unipolar Scale	Digital Output MSB LSB
+9.9976	+FS – 1LSB	1111 1111 1111
+7.5000	+3/4 FS	1100 0000 0000
+5.0000	+1/2 FS	1000 0000 0000
+2.5000	+1/4 FS	0100 0000 0000
+0.0024	+1LSB	0000 0000 0001
0	0	0000 0000 0000

Coding is straight binary; 1LSB = 2.44mV

THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and – 55 to +125°C. All room-temperature (T_A = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package. Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than "socketed," and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters,"or contact DATEL directly, for additional information.

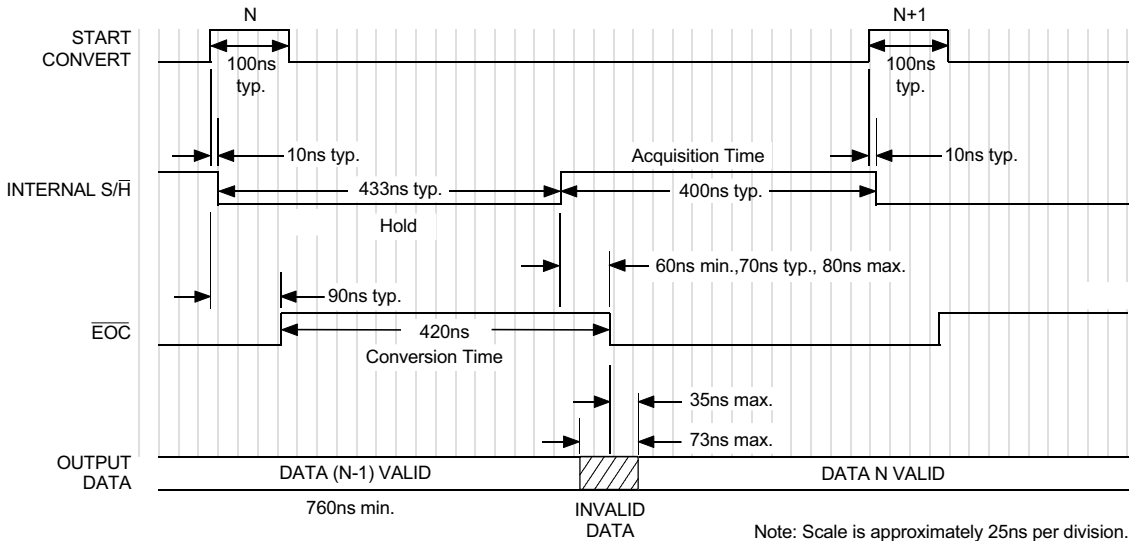


Figure 4. ADS-CCD1201 Timing Diagram

TIMING

The ADSCCD-1201 is an edge triggered device. A conversion is initiated by the rising edge of the start convert pulse and no additional external timing signals are required. The device does not employ "pipeline" delays to increase its throughput rate. It does not require multiple start convert pulses to bring valid digital data to its output pins.

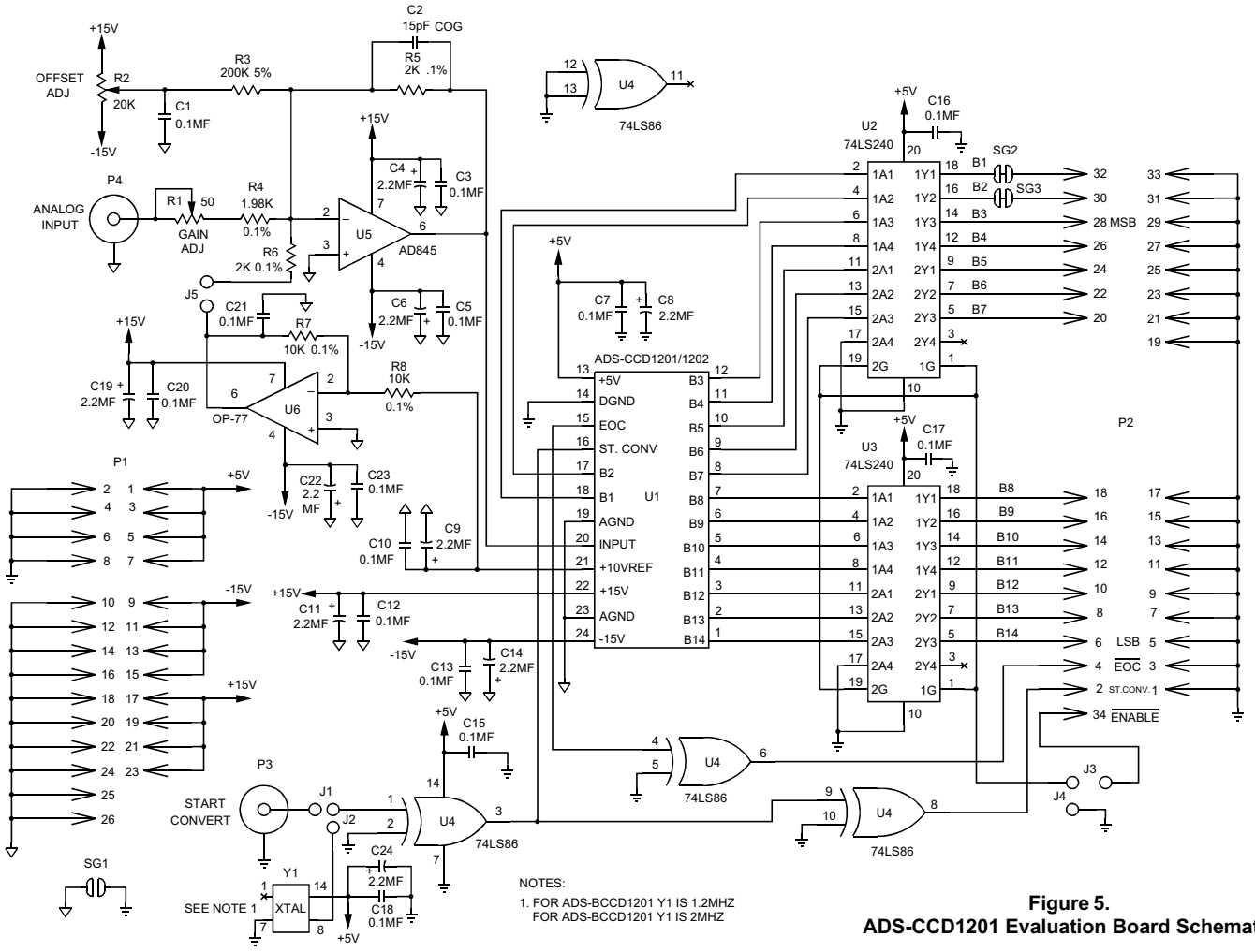


Figure 5.
ADS-CCD1201 Evaluation Board Schematic

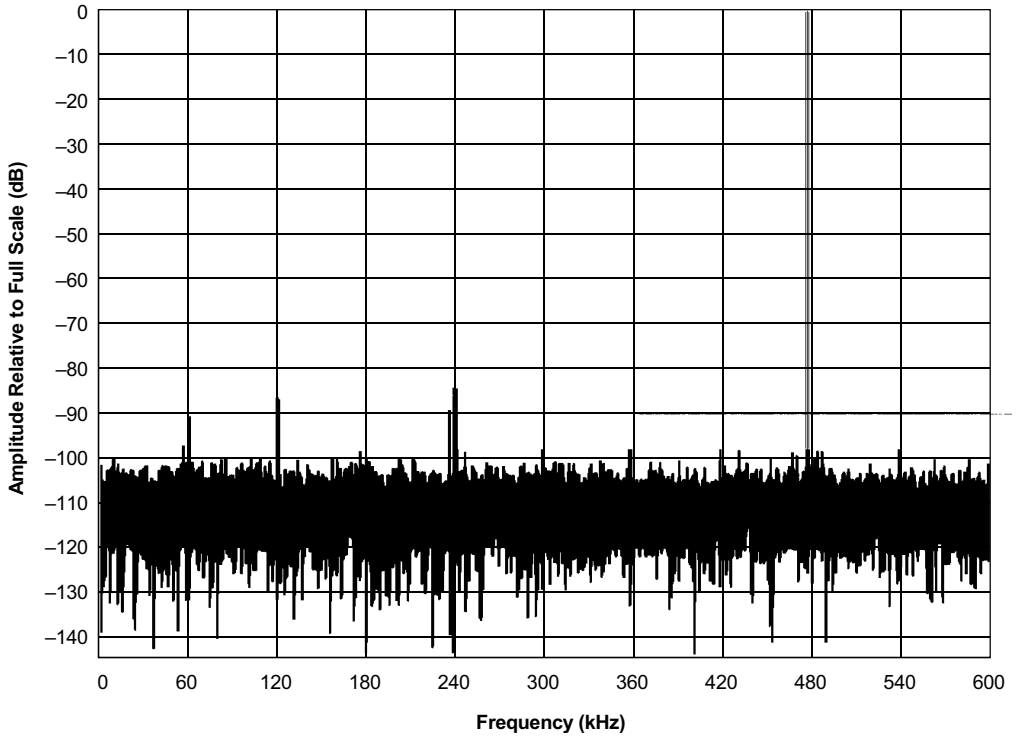


Figure 6. ADS-CCD1201 FFT
(f_{in} = 480kHz, f_s = 1.2MHz, V_{in} = –0.5dB, 16,384 points)

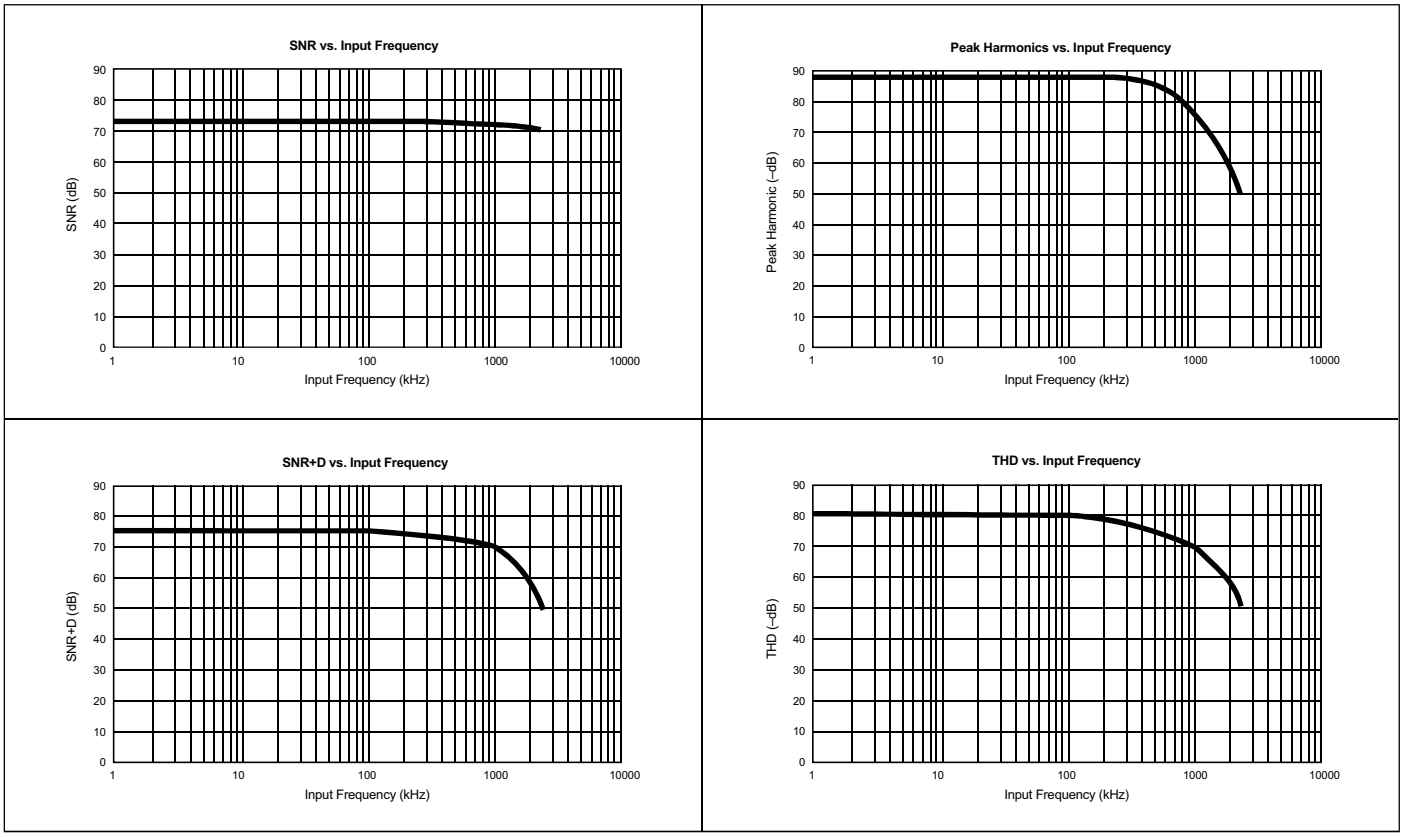
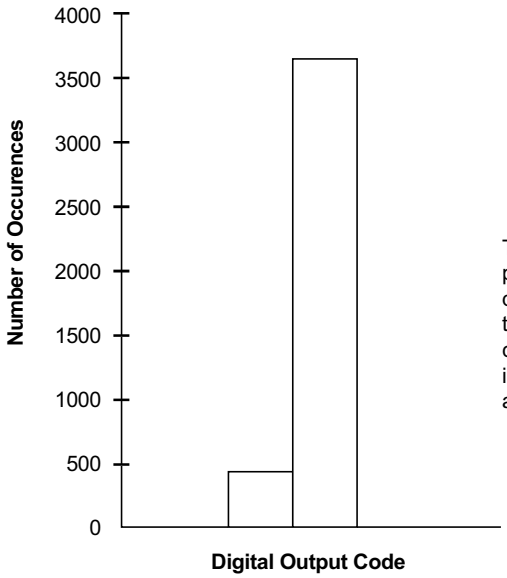


Figure 7. Typical ADS-CCD1201 Dynamic Performance vs. Input Frequency at +25°C (Vin = –0.5dB, fs = 1.2MHz)



This histogram represents the typical peak-to-peak noise (including quantization noise) associated with the ADS-CCD1201. 4,096 conversions were processed with the input to the ADS-CCD1201 tied to analog ground.

Figure 8. ADS-CCD1201 Grounded Input Histogram

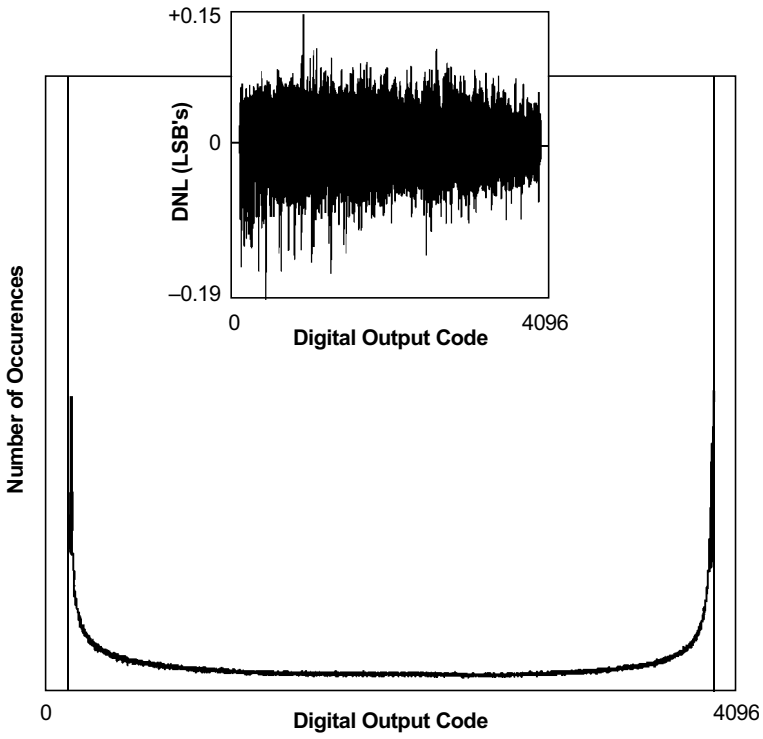
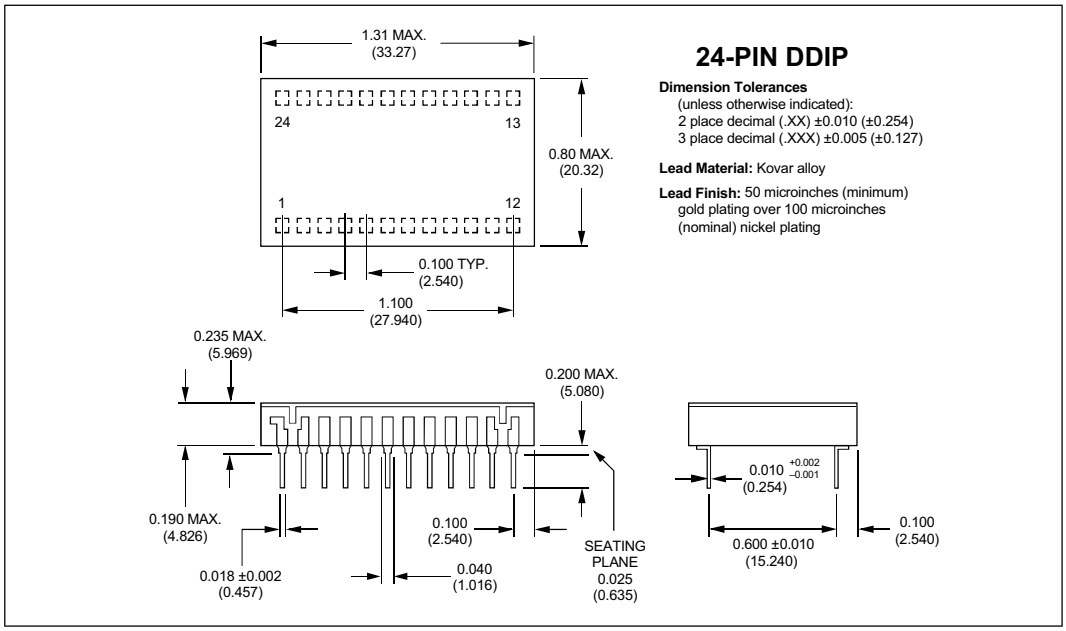


Figure 9. ADS-CCD1201 Histogram and Differential Nonlinearity

MECHANICAL DIMENSIONS INCHES (mm)

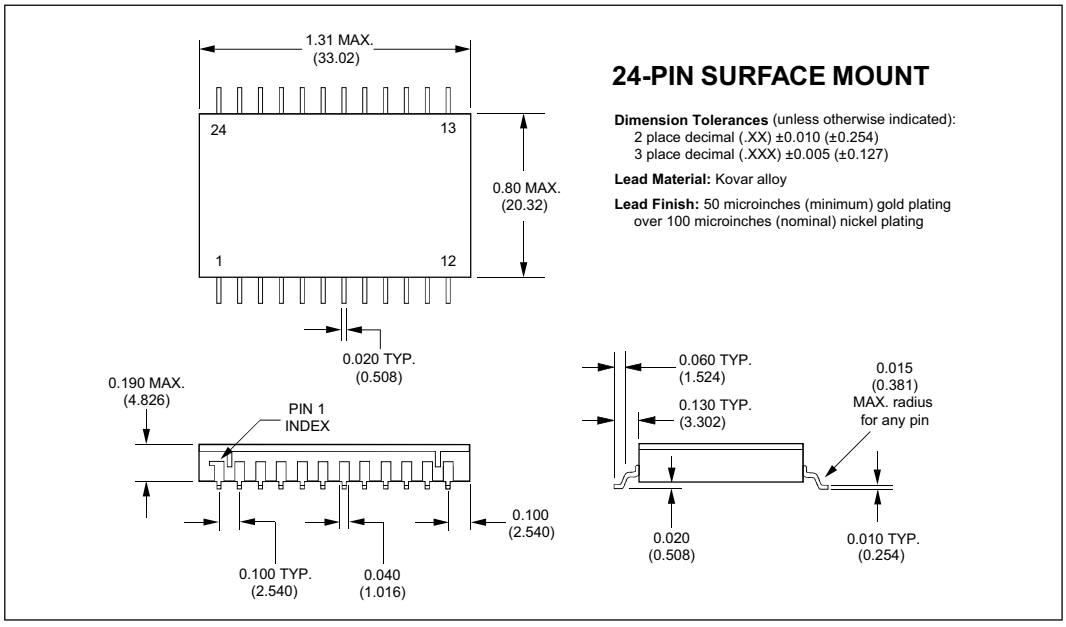


24-PIN DDIP

Dimension Tolerances
(unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating



24-PIN SURFACE MOUNT

Dimension Tolerances (unless otherwise indicated):
2 place decimal (.XX) ±0.010 (±0.254)
3 place decimal (.XXX) ±0.005 (±0.127)

Lead Material: Kovar alloy

Lead Finish: 50 microinches (minimum) gold plating over 100 microinches (nominal) nickel plating

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	ANALOG INPUT
ADS-CCD1201MC	0 to +70°C	Unipolar (0 to +10V)
ADS-CCD1201MM	–55 to +125°C	Unipolar (0 to +10V)

Contact DATEL for availability of surface-mount packaging or high-reliability screening.

Accessories

ADS-BCCD1201	Evaluation Board (without ADS-CCD1201)
HS-24	Heat Sink for ADS-CCD1201 models

Receptacles for pc board mounting can be ordered through Amp Inc., part number 3-331272-8 (component lead socket), 24 required.

INNOVATION and EXCELLENCE

ISO 9001 REGISTERED

DS-0274C 10/96

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