PAM8606

6W Stereo Class-D Audio Power Amplifier with DC Volume Control

Key Features

- 6W@10%THD / Channel Output into a 8Ω Load at 10V
- Low Noise: –80dB
- Over 90% Efficiency
- 32Step DC Volume Control from -75dB to 32dB
- With Shutdown/Mute/Fade Function
- Over Current , Thermal and Short-Circuit Protection
- Low THD+N
- Low Quiescent Current
- Pop Noise suppression
- Small Package Outlines: 48pinTQFP(E-PAD) 7mm*7mm Package
- Pb-Free Package (RoHS Compliant)

Applications

- Flat Monitor /LCD TVS
- Multi-media Speaker System
- DVD Players, Game Machines
- Boom Box
- Music Instruments

General Description

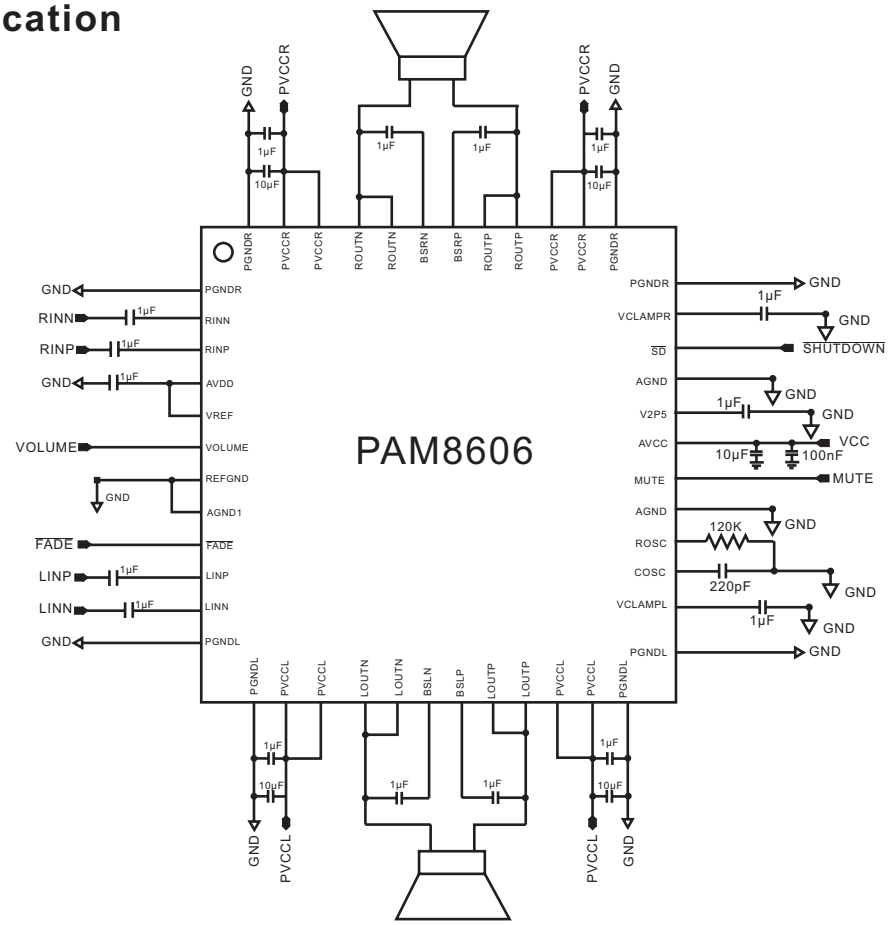
The PAM8606 is 6W (per channel), stereo class-D audio amplifier with DC Volume Control which offers low THD+N (0.1%), low EMI, and good PSRR, allowing it to produce high-quality sound reproduction. The 32 steps DC volume control has a +32dB to -75dB range.

The PAM8606 runs off of a 7.0V to 13.5V supply at much higher efficiency than class-AB amplifier.

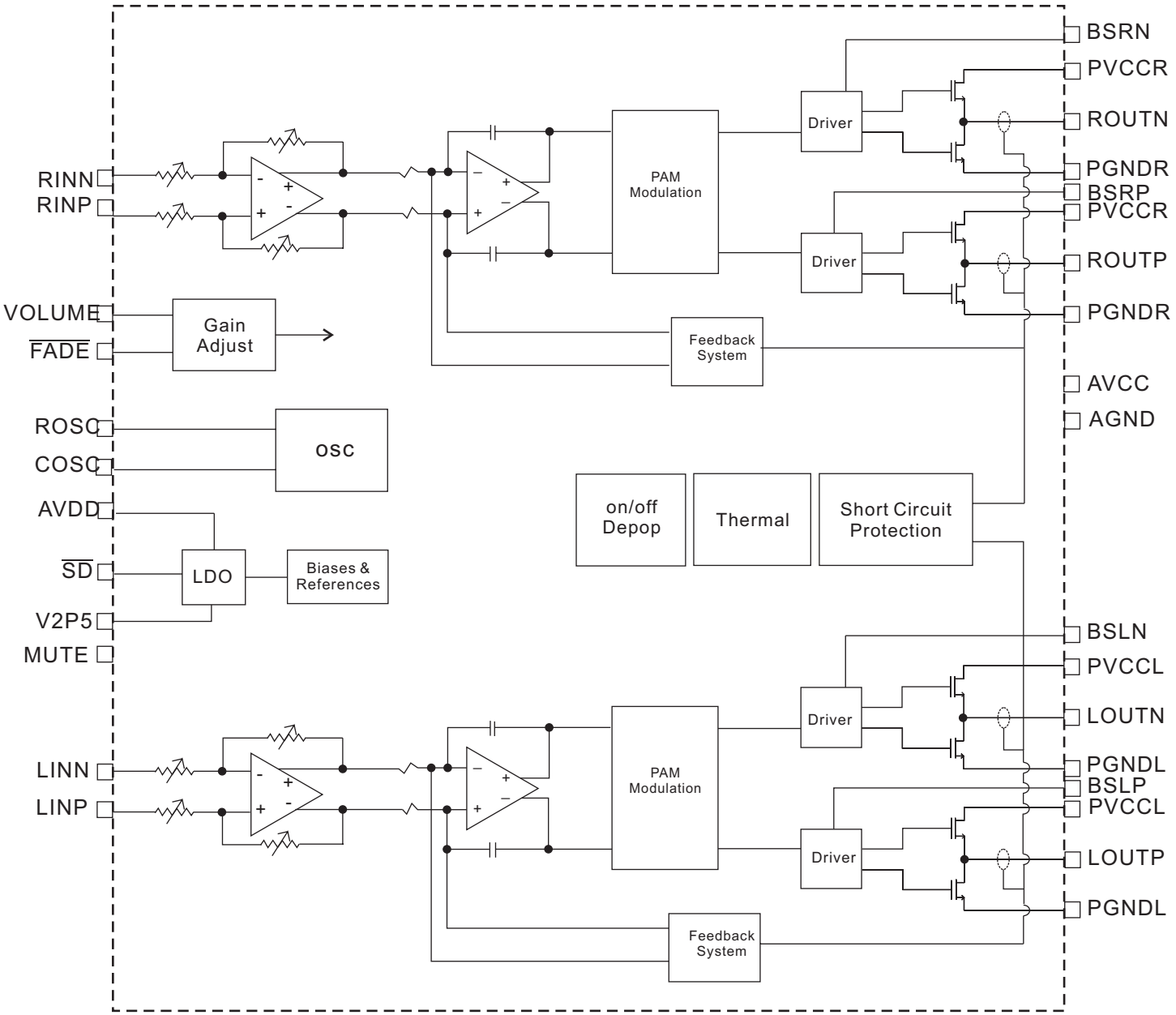
The PAM8606 only requires minimal number of external components, resulting in significant cost and board space savings.

The PAM8606 is available in a 48pin TQFP(E-PAD) 7mm*7mm package.

Typical Application

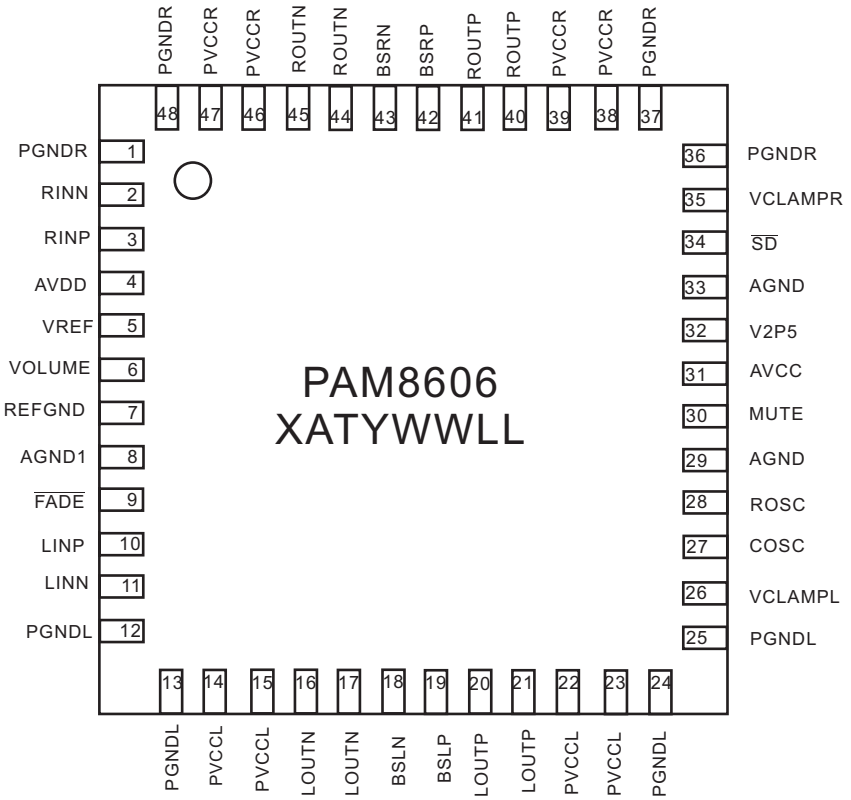


Block Diagram



Pin Configuration & Marking Information

Top View
7mm*7mm TQFP



X: Internal Code
A: Assembly Code
T: Testing Code
Y: Year
WW: Week
LL: Internal Code

Pin Descriptions

Number	Name	Function
2	RINN	Negative differential audio input for right channel
3	RINP	Positive differential audio input for right channel
4	AVDD	5V Analog VDD
5	VREF	Analog reference for gain control section
6	VOLUME	DC voltage that sets the gain of the amplifier
7	REFGND	Ground for gain control circuitry. Connect to AGND. If using a DAC to control the volume, connect the DAC ground to this terminal.
8	AGND1	Analog GND
9	$\overline{\text{FADE}}$	Input for controlling volume ramp rate when cycling SD or during power-up. A logic low on this pin places the amplifier in fade mode. A logic high on this pin allows a quick transition to the desired volume setting.
10	LINP	Positive differential audio input for left channel
11	LINN	Negative differential audio input for left channel
12,13,24,25	PGNDL	Power ground for left channel H-bridge
14,15,22,23	PVCCL	Power supply for left channel H-bridge, not connected to PVCCR or AVCC.
16,17	LOUTN	Class-D 1/2-H-bridge negative output for left channel
18	BSLN	Bootstrap I/O for left channel, negative high-side FET
19	BSLP	Bootstrap I/O for left channel, positive high-side FET
20,21	LOUTP	Class-D 1/2-H-bridge positive output for left channel
26	VCLAMPL	Internally generated voltage supply for left channel bootstrap capacitors.
27	COSC	I/O for charge/discharging currents onto capacitor for ramp generator triangle wave biased at V2P5
28	ROSC	Current setting resistor for ramp generator.
29,33	AGND	Analog GND
30	MUTE	A logic high on this pin disables the outputs and a logic low enables the outputs.
31	AVCC	High-voltage analog power supply (7.0 V to 13.5V)
32	V2P5	2.5V Reference for analog cells, as well as reference for unused audio input when using single-ended inputs.
34	$\overline{\text{SD}}$	Shutdown signal for IC (low= shutdown, high =operational). TTL logic levels with compliance to AVCC.
35	VCLAMPR	Internally generated voltage supply for right channel bootstrap capacitors.
1,36,37,48	PGNDR	Power ground for right channel H-bridge
38,39,46,47	PVCCR	Power supply for right channel H-bridge, not connected to PVCCL or AVCC.
40,41	ROUTP	Class-D 1/2-H-bridge positive output for right channel
42	BSRP	Bootstrap I/O for right channel, positive high-side FET
43	BSRN	Bootstrap I/O for right channel, negative high-side FET
44,45	ROUTN	Class-D 1/2-H-bridge negative output for right channel

Absolute Maximum Ratings

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Supply Voltage V_{DD}.....-0.3V to15.0V
Input Voltage Range V_I:
MUTE,VREF,VOLUME,$\overline{FADE}$.....0V to 6.0V
$\overline{SD}$.....-0.3V to V_{DD}
RINN,RINP,LINN,LINP.....-0.3V to 6.0V

Junction Temperature Range,T_J.....-40°C to 125°C
Storage Temperature.....-65°C to150°C
Lead Temperature1,6mm (1/16 inch) from case for 5 seconds.....260°C

Recommended Operating Conditions

Supply Voltage.....7.0V to 13.5V
Maximum Volume Control Pins, Input Pins Voltage.....0V to 5.0V
High Level Input Voltage: $\overline{SD}$.....2.0V
MUTE, $\overline{FADE}$.....2.0V

Low Level Input Voltage: $\overline{SD}$.....0.3V
MUTE, $\overline{FADE}$.....0.3V
Ambient Operating Temperature.....-20°C to 85°C

Thermal Information

Parameter	Package	Symbol	Maximum	Unit
Thermal Resistance (Junction to Case)	TQFP 7mm*7mm	θ_{JC}	8.7	°C/W
Thermal Resistance* (Junction to Ambient)	TQFP 7mm*7mm	θ_{JA}	48	

*4-layer PCB with the Exposed PAD soldered to a thermal land on the PCB and vias on PCB for heat dissipation (refer to Application Information hereinafter).

Electrical Characteristic

T_A=25°C, V_{DD}=9V, R_L=8Ω (unless otherwise noted)

Parameter	Symbol	condition		MIN	TYP	MAX	Units
Supply Voltage	V_{DD}			7.0	9	13.5	V
Continuous Output Power	Po	THD+N=0.1%,f=1kHz,R_L=8Ω			4		W
		THD+N=1.0%,f=1kHz,R_L=8Ω			4.5		
		THD+N=10%,f=1kHz,R_L=8Ω, V_{DD}=10V			6		
Total Harmonic Distortion plus Noise	THD+N	P_O=4W, f=1kHz, R_L =8Ω			0.1		%
Quiescent Current	I_{DD}	(no load)			20	30	mA
Supply Quiescent Current in shutdown mode	I_{SD}	SHUTDOWN=0V			4	10	μA
Drain-source on-state resistance	$r_{ds(on)}$	V_{CC}=12V I_O=1A T_J=25℃	High side		200		mΩ
			Low side		200		
			Total		400		
Power Supply Ripple Rejection Ratio	PSRR	$1V_{PP}$ ripple, f=1kHz, Inputs ac-coupled to ground			-60		dB
Oscillator Frequency	f_{OSC}	R_{OSC}=120kΩ, C_{OSC}=220pF			250		kHz
Output Integrated Noise Floor	Vn	20Hz to 22 kHz, A-weighted			-90		dB
Crosstalk	CS	P_O=3W, R_L=8Ω, f=1kHz			-80		dB
Signal to Noise Ratio	SNR	Maximum output at THD+N < 0.5%, f=1 kHz			80		dB
Output offset voltage (measured differentially)	$\|V_{OS}\|$	INN and INP connected together			30		mV
2.5V Bias voltage	V2P5	No Load			2.5		V
Internal Analog supply Voltage	AV_{DD}	V_{DD}=7V to 13.5V			5	5.5	V
Over Temperature Shutdown	OTS				150		°C
Thermal Hysteresis	OTH				40		°C

Table 1. DC Volume Control

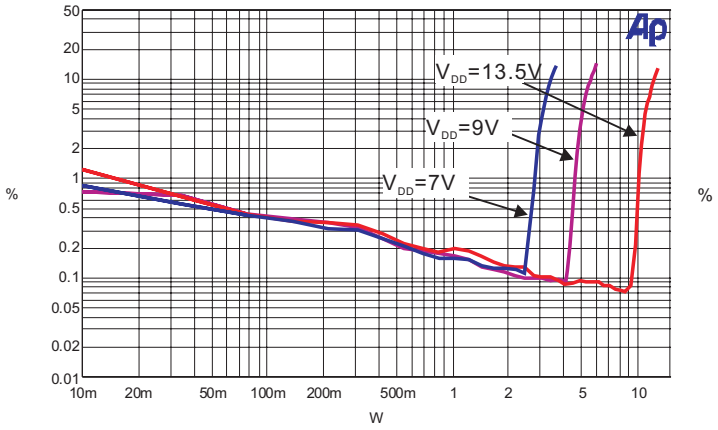
Step	Volume	Gain (dB)	Rf (kΩ)	Ri (kΩ)
1	0.0	-75	0.40	200.00
2	0.1	-40	1.26	199.60
3	0.2	-30	3.92	198.74
4	0.3	-20	11.90	196.08
5	0.4	-10	20.22	188.10
6	0.5	-5	33.33	179.78
7	0.6	0	52.47	166.67
8	0.7	5	77.49	147.53
9	0.8	10	83.02	122.51
10	0.9	11	88.65	116.98
11	1.0	12	94.37	111.35
12	1.1	13	100.12	105.63
13	1.2	14	105.87	99.88
14	1.3	15	111.58	94.13
15	1.4	16	117.21	88.42
16	1.5	17	122.74	82.79
17	1.6	18	128.12	77.26
18	1.7	19	133.33	71.88
19	1.8	20	138.35	66.67
20	1.9	21	143.15	61.65
21	2.0	22	147.71	56.85
22	2.1	23	152.04	52.29
23	2.2	24	156.11	47.96
24	2.3	25	159.92	43.89
25	2.4	26	163.49	40.08
26	2.5	27	166.80	36.51
27	2.6	28	169.86	33.20
28	2.7	29	172.69	30.14
29	2.8	30	175.30	27.31
30	2.9	31	177.68	24.70
31	3.0	32	179.87	22.32
32	3.1	33	200.00	20.13

Note:
Volume: DC voltage on Volume pin
Rf: Internal pre-amplifier feedback resistance
Ri: Internal pre-amplifier input resistance
Calculation Gain=20log(5XRf/Ri),there is one dB tolerance from device to device.

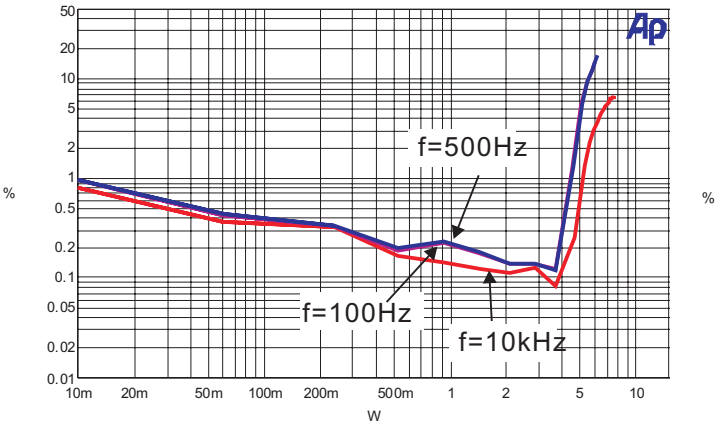
Typical Performance Characteristics

V_{DD}=9V,R_L=8Ω,T_A=25°C (unless otherwise noted).

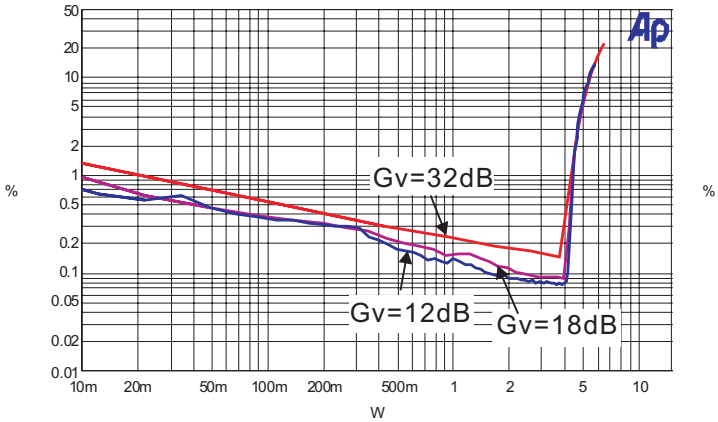
1. THD vs. Power



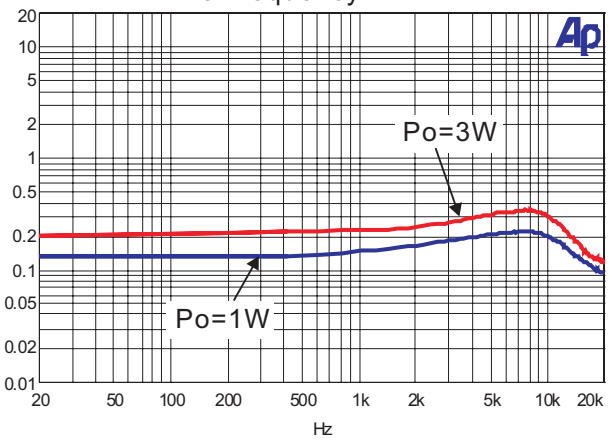
2. THD vs. Power



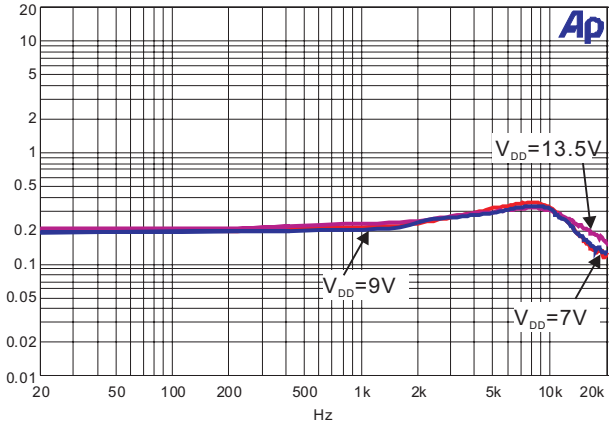
3. THD vs. Power



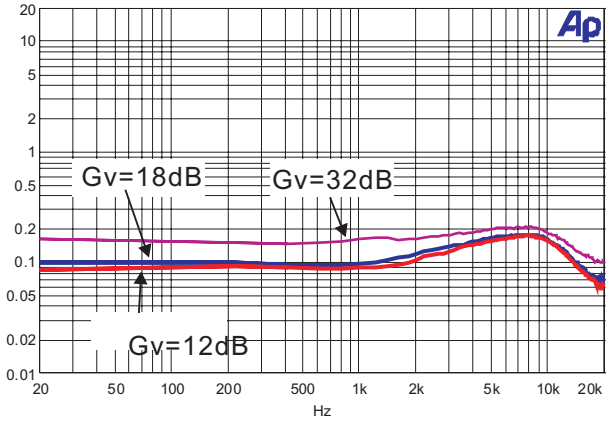
4. THD+N vs Frequency



5. THD+N vs Frequency (Po=1W)



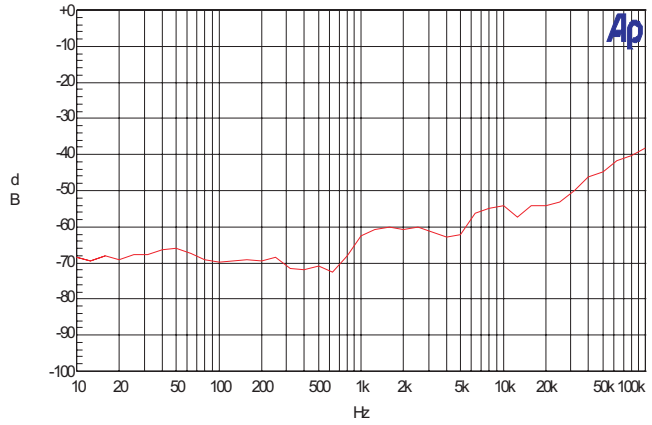
6. THD+N vs Frequency (Po=3W)



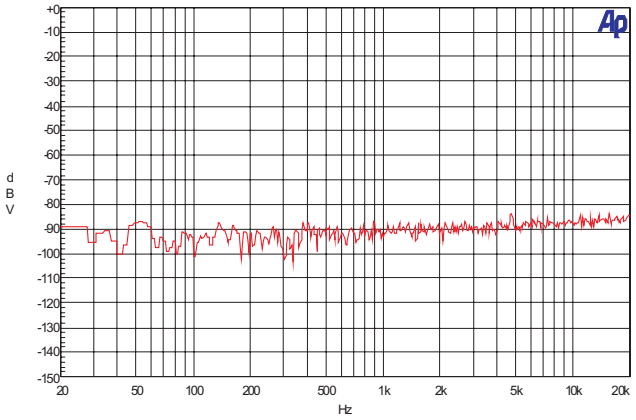
Typical Performance Characteristics

V_{DD}=9V,R_L=8Ω,T_A=25°C (unless otherwise noted).

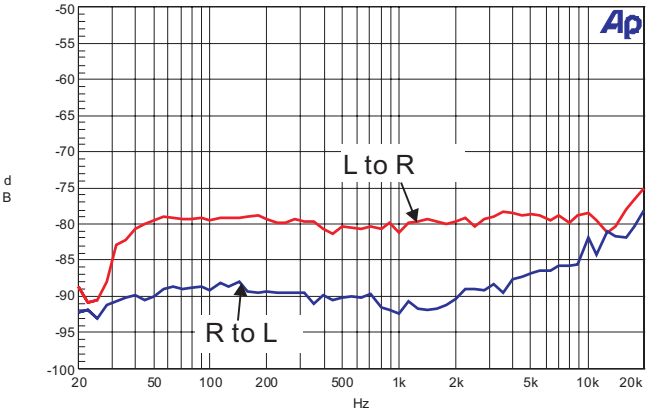
7. Power Supply Ripple Rejection



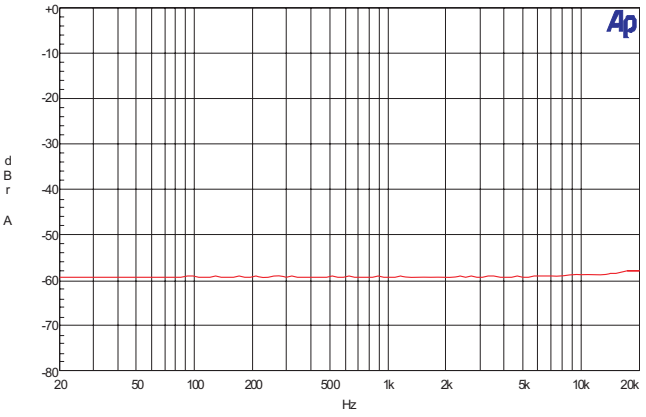
10. Noise Floor



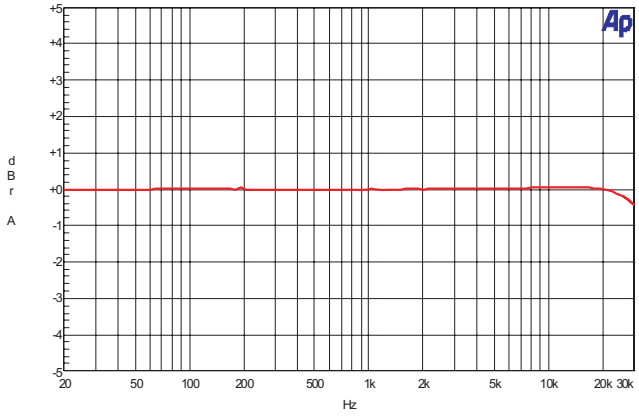
8. Crosstalk



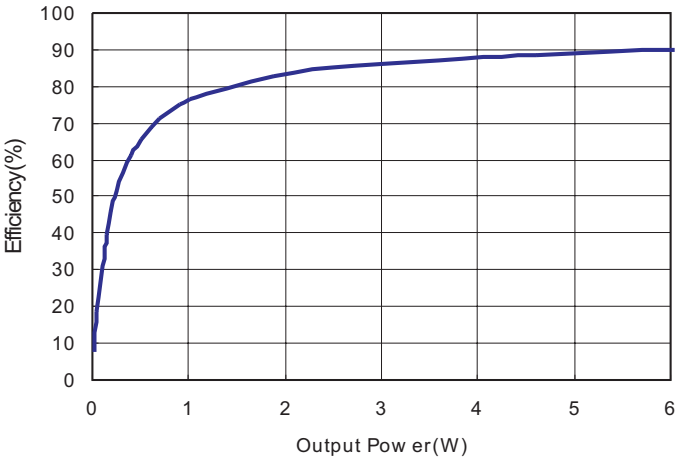
11. CMRR



9. Frequency Response (Vo=1.0Vrms)



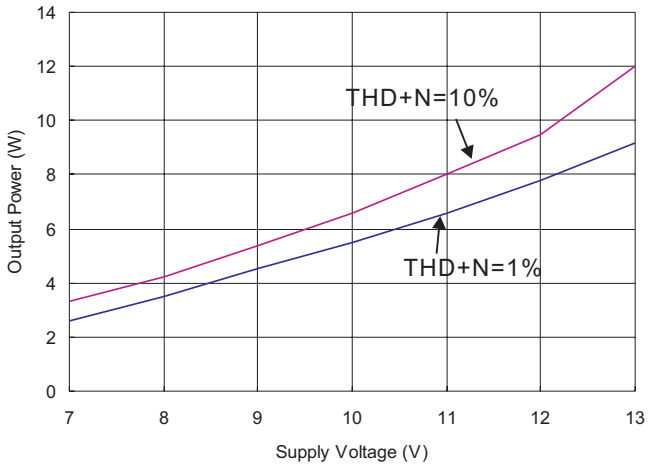
12. Efficiency vs Power



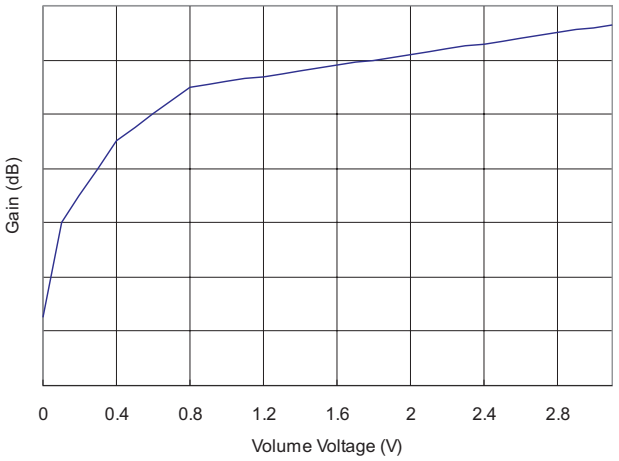
Typical Performance Characteristics

V_{DD}=9V,R_L=8Ω,T_A=25°C (unless otherwise noted).

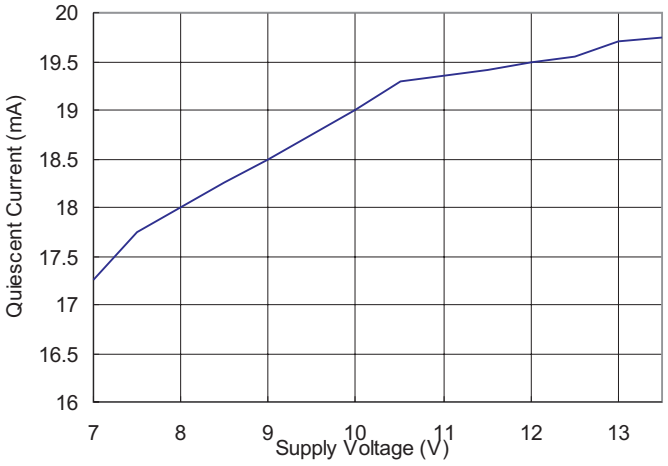
13. Output Power vs Supply Voltage



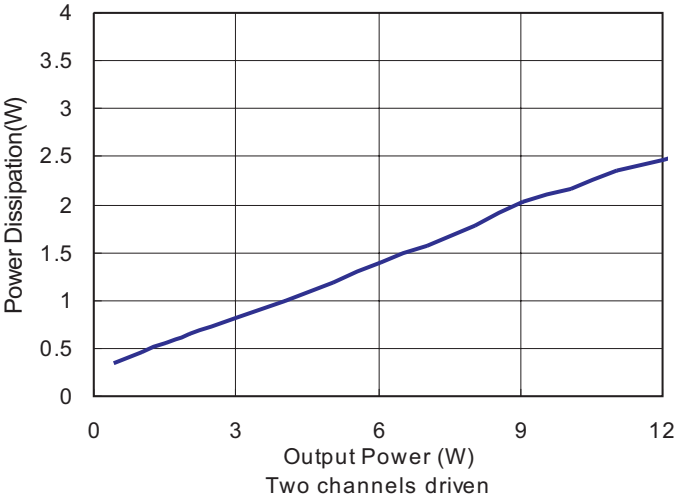
15.Gain vs DC voltage



14. Quesicent Current vs Supply Voltage

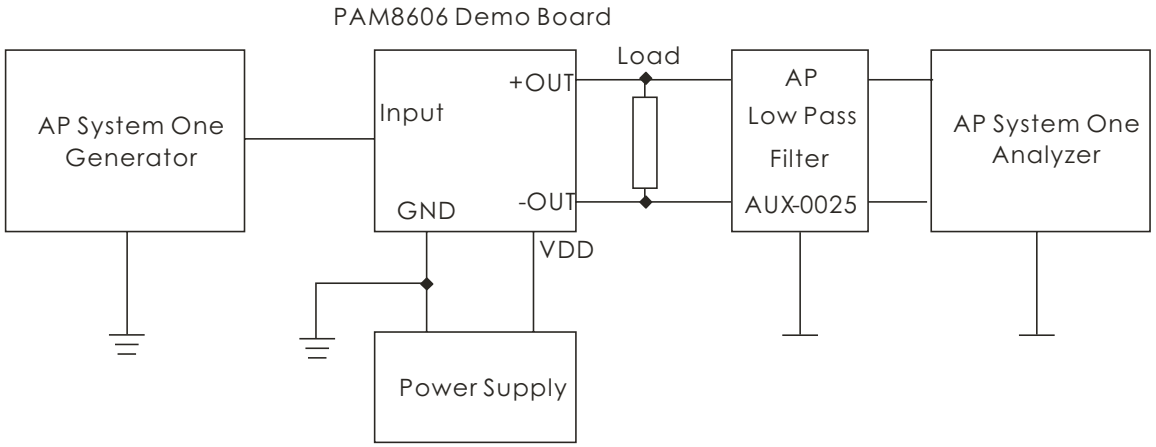


16.Power Dissipation vs. Output Power



Note:
PCB information for power dissipation measurement.
1. The PCB size is 74mm∗68mm with 1.2mm thickness, two layers and Fr4.
2. 16 vias at the thermal land on the PCB with 0.5mm diameter.
3. The size of exposed copper is 10mm*10mm with 3oz thickness.

Test Setup for Performance Testing



Notes

1. The AP AUX-0025 low pass filter is necessary for every class-D amplifier measurement with AP analyzer.

2. Two 22μH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

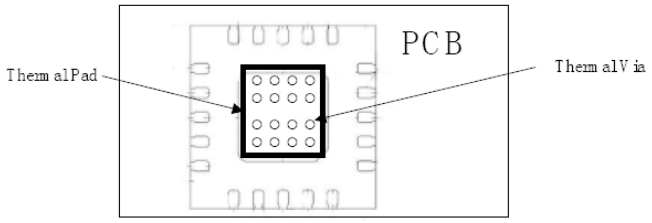
Application Information

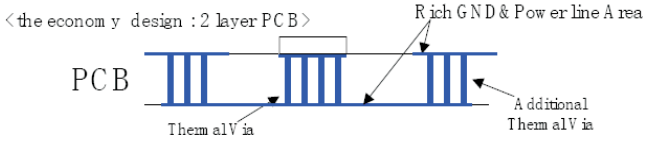
Heat Dissipation in PCB Design

Generally, class-D amplifiers are high efficiency and need no heat sink. For high power ones that has high dissipation power, the heat sink may also not necessary if the PCB is carefully designed to achieve good heat dissipation by the PCB itself.

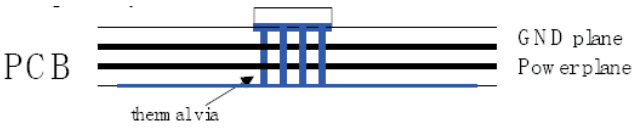
Dual-Side PCB
To achieve good heat dissipation, the PCB's copper plate should be thicker than 0.035mm and the copper plate on both sides of the PCB should be utilized as heat sink.

The thermal pad on the bottom of the device should be soldered to the plate of the PCB, and via holes, usually 9 to 16, should be drilled in the PCB area under the device and deposited copper on the vias should be thick enough so that the heat can be dissipated to the other side of the plate. There should be no insulation mask on the other side of the copper plate. It is better to drill more vias on the PCB around the device if possible.



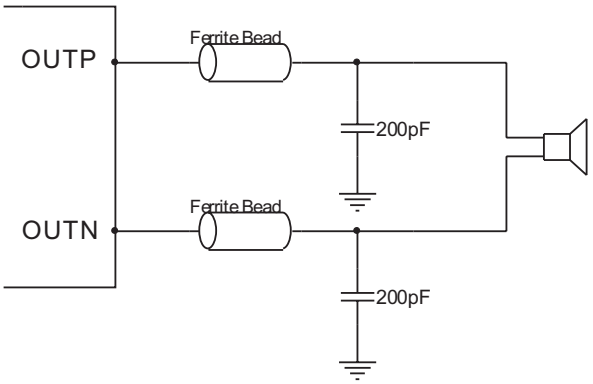


4-layer PCB
If it is 4-layer PCB, the two middle layers of grounding and power can be employed as heat sink, isolating them into serval islands to avoid short between ground and power.



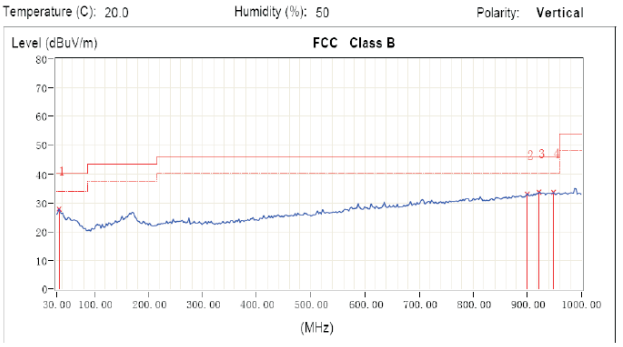
Consideration for EMI

Filters are not required if the traces from the amplifier to the speakers are short (<20cm). But most applications require a ferrite bead filter as shown in below figure. The ferrite bead filter reduces EMI of around 1MHz and higher to meet the FCC and CE's requirements. It is recommended to use a ferrite bead with very low impedances at low frequencies and high impedance at high frequencies (above 1MHz).

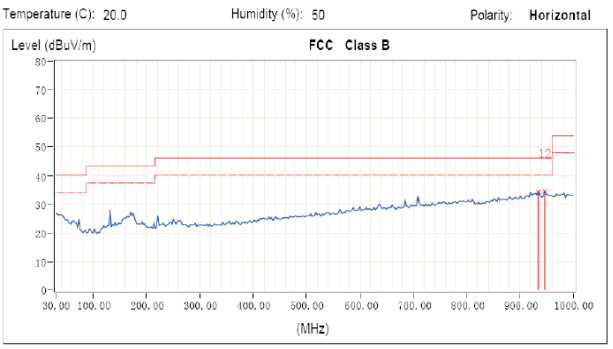


The EMI characteristics are as follows after employing the ferrite bead.

Vertical Polarization



Horizontal Polarization



Volume Control

A DC volume control section is integrated in PAM8606, controlling via VREF, VOLUME and VREFGND terminals. The voltage on VOLUME pin, without exceeding VREF, determines internal amplifier gain as listed in Table 1.

If a resistor divider is used to fix gain of the amplifier, the VREF terminal can be directly connected to AVDD and the resistor divider connected across VREF and REFGND. For fixed gain, the resistor divider values are calculated to center the voltage given in the Table 1.

FADE Operation

The $\overline{\text{FADE}}$ terminal is a logic input that controls the operation of the volume control circuitry during transitions to and from the shutdown state and during power-up.

A logic low on this terminal will set the amplifier in fade mode. During power-up or recovery from the shutdown state (a logic high is applied to the $\overline{\text{SD}}$ terminal), the volume is smoothly ramped up from the mute state, -75dB, to the desired volume set by the voltage on the volume control terminal. Conversely, the volume is smoothly ramped down from the current state to the mute state when a logic low is applied to the $\overline{\text{SD}}$ terminal. A logic high on this pin disables the volume fade effect during transitions to and from the shutdown state and during power-up. During power-up or recovery from the shutdown state (a logic high is applied to the $\overline{\text{SD}}$ terminal), the transition from the mute state, -75dB, to the desired volume setting is less than 1ms. Conversely, the volume ramps down from current state to the mute state within 1ms when a logic low is applied to the $\overline{\text{SD}}$ terminal.

MUTE Operation

The MUTE pin is an input for controlling the output state of the PAM8606. A logic high on this pin disables the outputs and low enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade.

For power saving, the $\overline{\text{SD}}$ pin should be used to reduce the quiescent current to the absolute minimum level. The volume will fade, increasing or decreasing slowly, when leaving or entering the shutdown state if the $\overline{\text{FADE}}$ terminal is held low. If the $\overline{\text{FADE}}$ terminal is held high, the outputs will transit very quickly. Refer to the $\overline{\text{FADE}}$ operation section.

Shutdown Operation

The PAM8606 employs a shutdown operation mode to reduce supply current to the absolute minimum level during periods of non-use to save power. The $\overline{\text{SD}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SD}}$ low causes the outputs to mute and the amplifier to enter a low-current state. $\overline{\text{SD}}$ should never be left unconnected to prevent the amplifier from unpredictable operation.

For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

Internal 2.5V Bias Generator Capacitor Selection

The internal 2.5V bias generator (V2P5) provides the internal bias for the preamplifier stage. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the V2P5 terminal is critical for achieving the best device performance. During startup or recovery from shutdown state, the V2P5 capacitor determines the rate at which the amplifier starts up. When the voltage on the V2P5 capacitor equals 0.75 x V2P5, or 75% of its final value, the device turns on and the class-D outputs start switching. The startup time is not critical for the best de-pop performance since any heard pop sound is the result of the class-D output switching-on other than that of the startup time. However, at least a 0.47µF capacitor is recommended for the V2P5 capacitor.

Another function of the V2P5 capacitor is to filter high frequency noise on the internal 2.5V bias generator.

Power Supply Decoupling, C_s

The PAM8606 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents oscillations caused by long lead between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series

-resistance (ESR) ceramic capacitor, typically 1µF, is recommended, placing as close as possible to the device's VCC lead. To filter lower-frequency noises, a large aluminum electrolytic capacitor of 10µF or greater is recommended, placing near the audio power amplifier. The 10µF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

Selection of C_{osc} and R_{osc}

The switching frequency is determined by the values of components connected to ROSC (pin 23) and COSC (pin 22) and calculated as follows:

$$f_{osc} = 2\pi / (R_{osc} * C_{osc})$$

The frequency may varies from 225kHz to 275kHz by adjusting the values of R_{osc} and C_{osc}. The recommended values are C_{osc} = 220pF, R_{osc}=120kΩ for a switching frequency of 250kHz.

BSN and BSP Capacitors

The full H-bridge output stages use NMOS transistors only. They therefore require bootstrap capacitors for the high side of each output to turn on correctly. A at least 220nF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from xOUTP to xBSP, and another 220nF capacitor from xOUTN to xBSN. It is recommended to use 1µF BST capacitor to replace 220nF (pin18, pin19, pin42 and pin43) for lower than 100Hz applications.

VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors not exceeded, two internal regulators are used to clamp the gate voltage. Two 1µF capacitors must be connected from VCLAMPL and VCLAMPR to ground and must be rated for at least 25V. The voltages at the VCLAMP terminals vary with V_{CC} and may not be used to power any other circuitry.

Internal Regulated 5-V Supply (AVDD)

The AVDD terminal is the output of an internally-generated 5V supply, used for the oscillator, preamplifier, and volume control circuitry. It requires a 0.1µF to 1µF capacitor, placed very close to the pin to Ground to keep the regulator stable. The regulator may not be used to power any external circuitry.

Differential Input

The differential input stage of the amplifier eliminates noises that appear on the two input lines of the channel. To use the PAM8606 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the PAM8606 with a single-ended source, ac-ground the INP input through a capacitor equal in value to the input capacitor on INN and apply the audio source to the INN input. In a single-ended input application, the INP input should be ac-grounded at the audio source other than at the device input for best noise performance.

Using low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (with respect to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves as an ideal capacitor.

Short-circuit Protection

The PAM8606 has short circuit protection circuitry on the outputs to prevent damage to the device when output-to-output shorts, output-to-GND shorts, or output-to-VCC shorts occur. Once a short-circuit is detected on the outputs, the output drive is immediately disabled. This is a latched fault and must be reset by cycling the voltage on the $\overline{SD}$ pin to a logic low and back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

Thermal Protection

Thermal protection on the PAM8606 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the set thermal point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 40°C. The device begins normal operation at this point without external system intervention.

Ordering Information

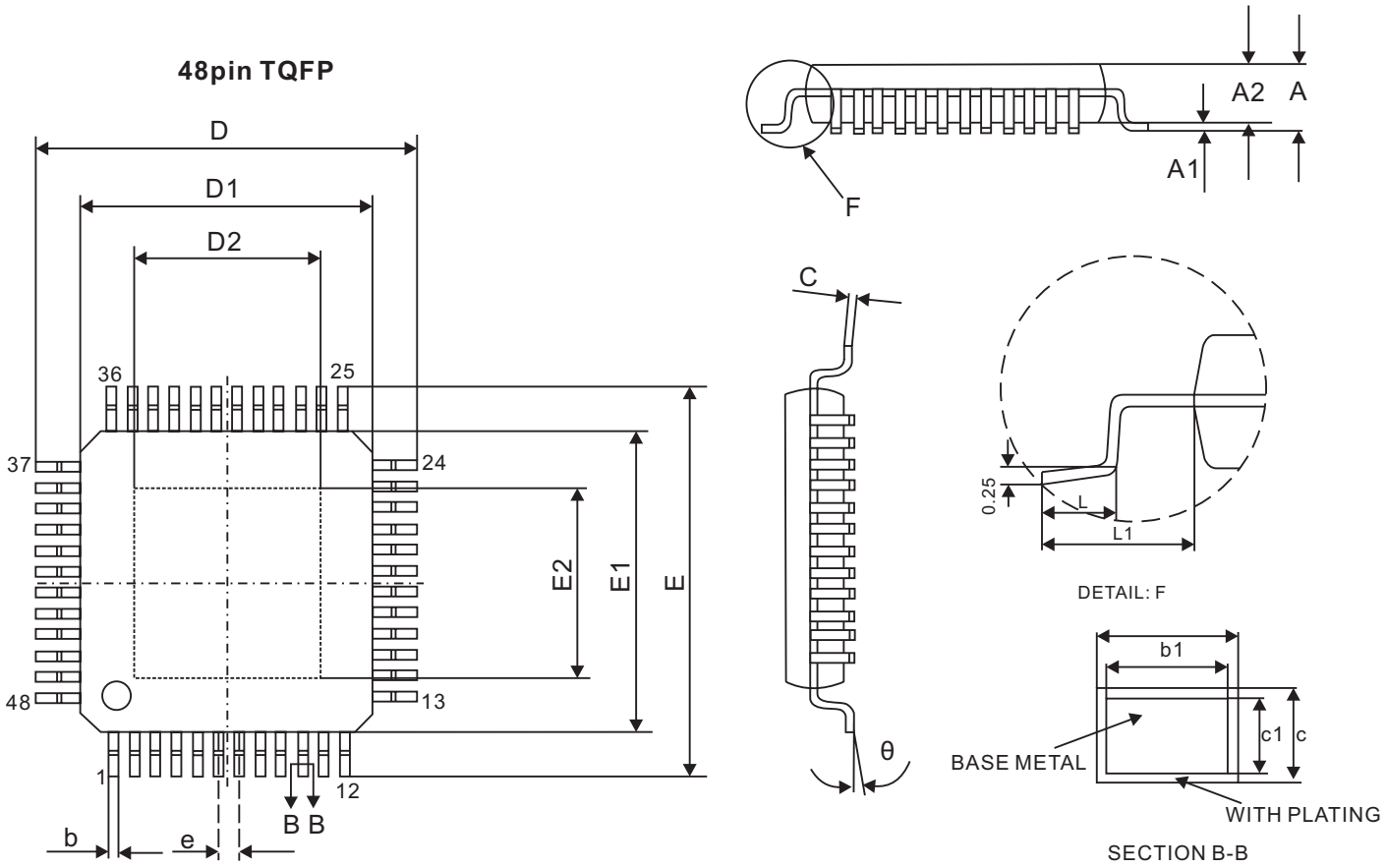
PAM8606 X X

- Shipping(B:Tray)
- Package Type(X:TQFP)

Part Number	Marking	Package Type	Shipping
PAM8606XB	PAM8606 XATYWWLL	TQFP 7mm*7mm	250 Units/ Tray

Outline Dimension

48pin TQFP



SYMBOL	MILLIMETER			SYMBOL	MILLIMETER		
	MIN	NOM	MAX		MIN	NOM	MAX
A	-	-	1.60	E	8.80	9.00	9.20
A1	0.05	0.15	0.25	E1	6.80	7.00	7.20
A2	0.9		1.50	E2	5.00REF		
B	0.19	-	0.27	e	0.50BSC		
b1	0.18	0.20	0.23	L	0.35	0.50	0.65
c	0.13	-	0.18	L1	1.00BSC		
c1	0.12	0.13	0.14	θ	0	-	8
D	8.80	9.00	9.20				
D1	6.80	7.00	7.20				
D2	5.00REF						