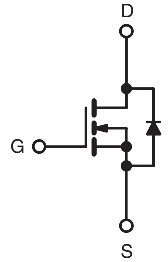
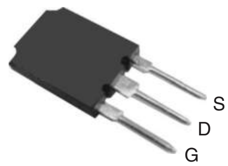
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.175
Q_g (Max.) (nC)	220	
Q_{gs} (nC)	67	
Q_{gd} (nC)	96	
Configuration	Single	



N-Channel MOSFET

SUPER-247™



FEATURES

- Super Fast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhances dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offer Improved Noise Immunity
- Lead (Pb)-free Available

Pb Available

RoHS* COMPLIANT

APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

ORDERING INFORMATION	
Package	SUPER-247™
Lead (Pb)-free	IRFPS29N60LPbF
	SiHFPS29N60L-E3
SnPb	IRFPS29N60L
	SiHFPS29N60L

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	600	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	29	A
		T_C = 100 °C		18	
Pulsed Drain Current[a]			I_{DM}	110	
Linear Derating Factor				3.8	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	570	mJ
Repetitive Avalanche Current[a]			I_{AR}	29	A
Repetitive Avalanche Energy[a]			E_{AR}	48	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	480	W
Peak Diode Recovery dV/dt[c]			dV/dt	15	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

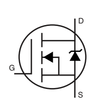
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting T_J = 25 °C, L = 1.5 mH, R_G = 25 Ω, I_{AS} = 29 A (see fig.12a).
c. $I_{SD} \leq 29$ A, dI/dt ≤ 830 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient[a]	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)[a]	R_{thJC}	-	0.26	

Note
a. R_{th} is measured at T_J approximately 90 °C.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.53	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V		-	-	50	µA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125 °C		-	-	2.0	mA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 17 A[b]	-	0.175	0.21	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 17 A[b]		15	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5[b]		-	6160	-	pF
Output Capacitance	C_{oss}			-	530	-	
Reverse Transfer Capacitance	C_{rss}			-	44	-	
Effective Output Capacitance	C_{oss} eff.	V_{DS} = 0 V to 480 V[c]		-	250	-	
Effective Output Capacitance (Energy Related)	C_{oss} eff. (ER)			-	190	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 29 A, V_{DS} = 480 V, see fig. 7 and 15[b]	-	-	220	nC
Gate-Source Charge	Q_{gs}			-	-	67	
Gate-Drain Charge	Q_{gd}			-	-	96	
Internal Gate Resistance	R_G	f = 1 MHz, open drain		-	0.86	-	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} =300 V, I_D = 29 A, R_G = 4.3 Ω, V_{GS} = 10 V, see fig. 11a and 11b[b]		-	34	-	ns
Rise Time	t_r			-	100	-	
Turn-Off Delay Time	$t_{d(off)}$			-	66	-	
Fall Time	t_f			-	54	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	29	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	110	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 29 A, V_{GS} = 0 V[b]		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 29 A T_J = 125 °C, dI/dt = 100 A/µs[b]		-	130	190	ns
				-	240	360	
Body Diode Reverse Recovery Charge	Q_{rr}			-	630	950	µC
				-	1820	2720	
Body Diode Recovery Current	I_{RRM}	T_J = 25 °C		-	9.4	14	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominatred by L_S and L_D)					

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.
c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS}.
C_{oss} eff. (ER) is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS}.

Document Number: 91255
S-81359-Rev. A, 07-Jul-08

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

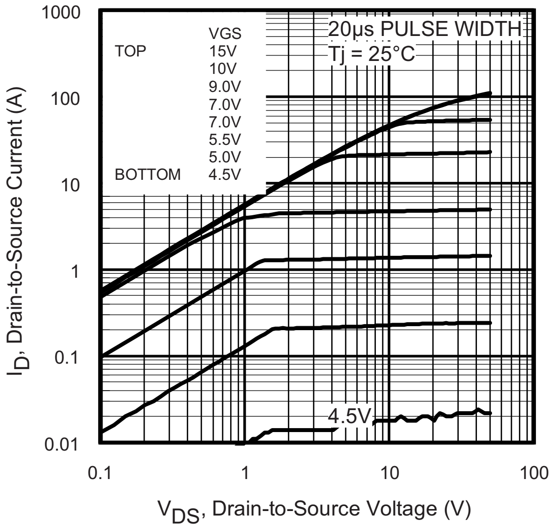


Fig. 1 - Typical Output Characteristics

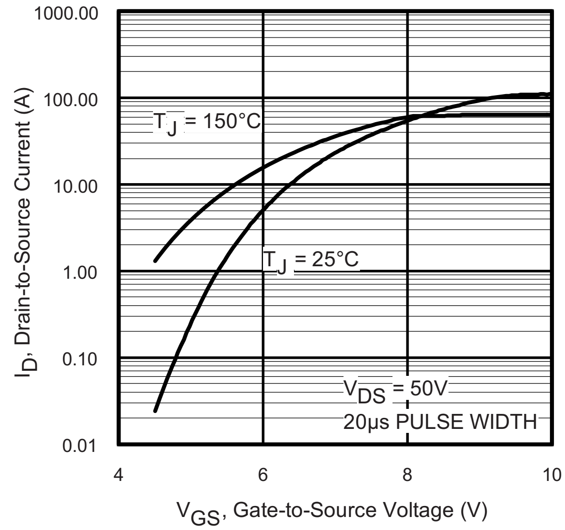


Fig. 3 - Typical Transfer Characteristics

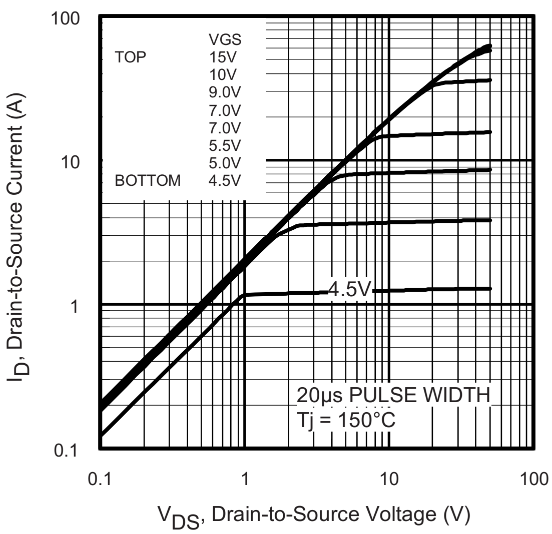


Fig. 2 - Typical Output Characteristics

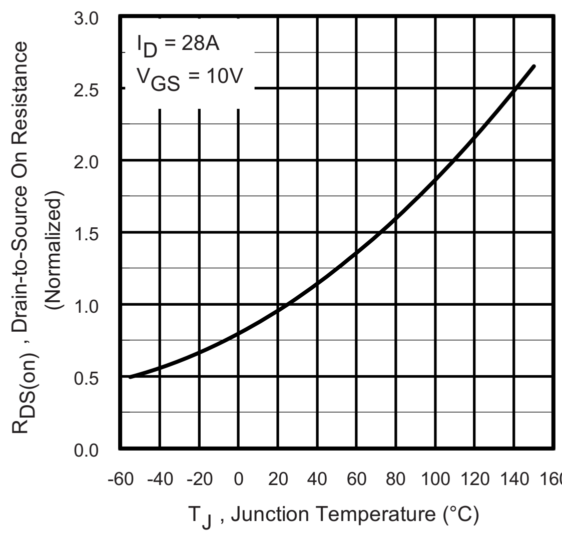


Fig. 4 - Normalized On-Resistance vs. Temperature

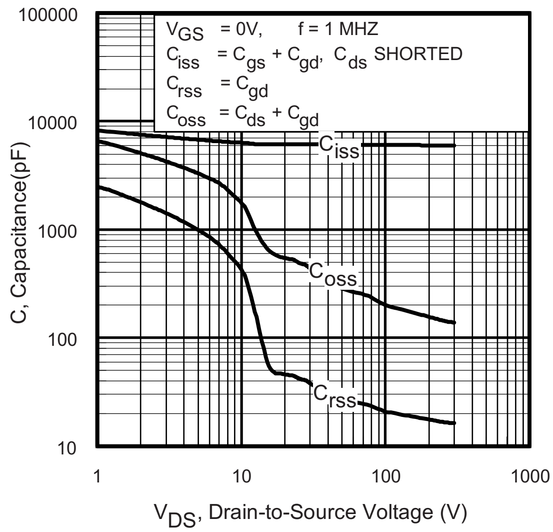


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

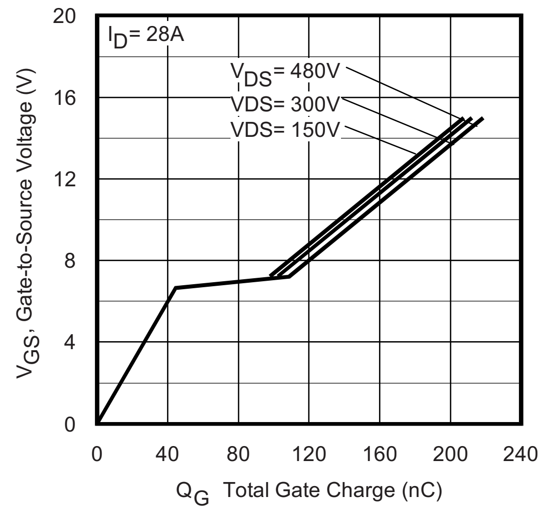


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

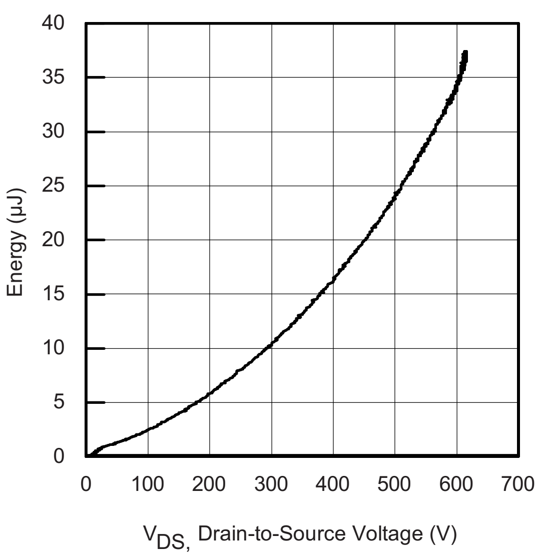


Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

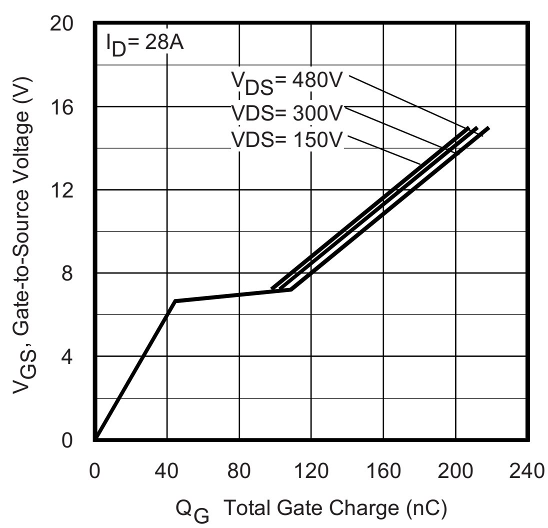


Fig. 8 - Typical Source-Drain Diode Forward Voltage

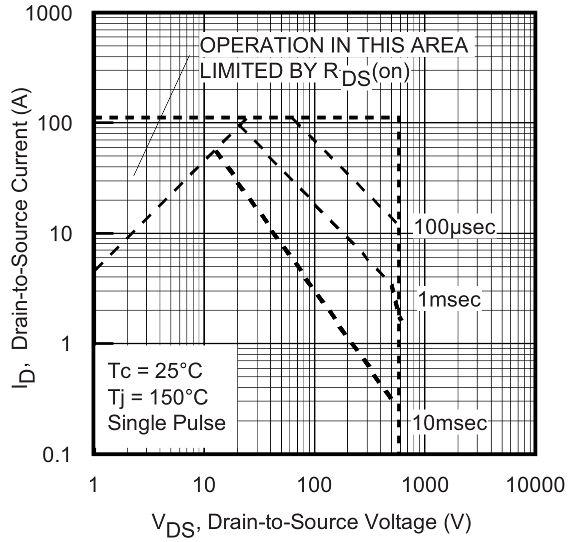


Fig. 9 - Maximum Safe Operating Area

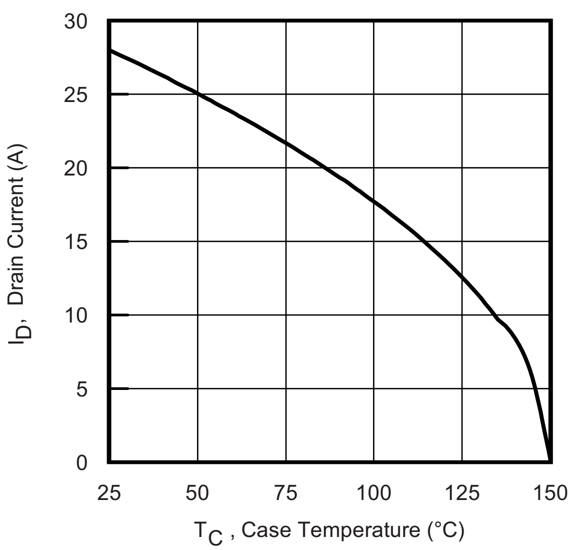


Fig. 10 - Maximum Drain Current vs. Case Temperature

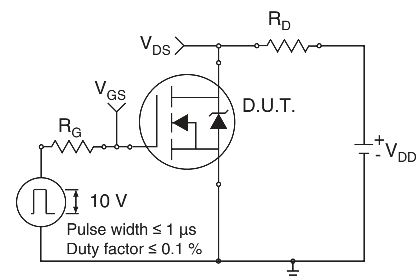


Fig. 11a - Switching Time Test Circuit

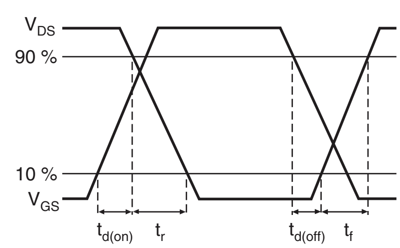


Fig. 11b - Switching Time Waveforms

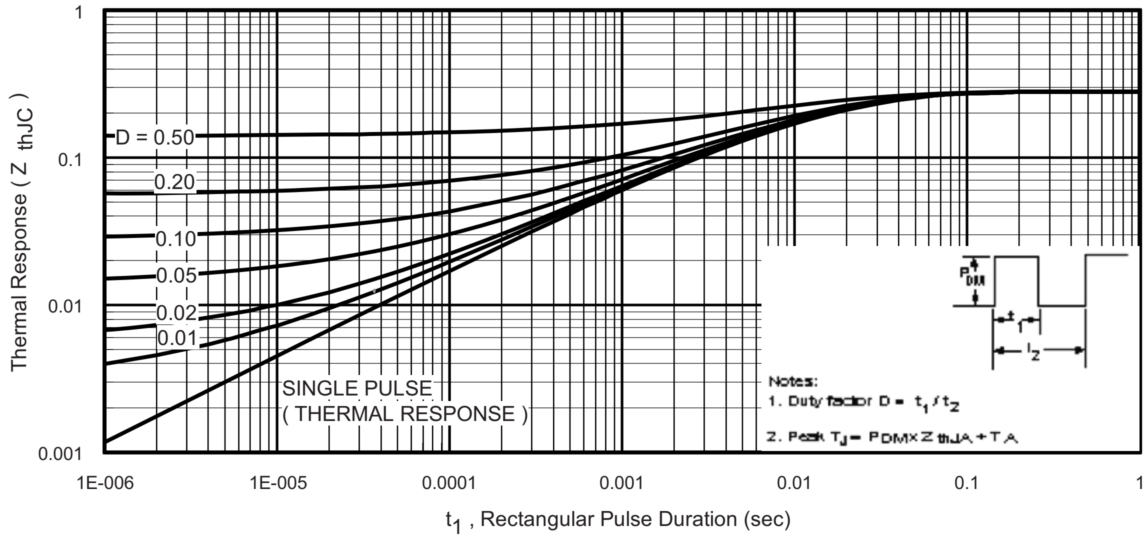


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

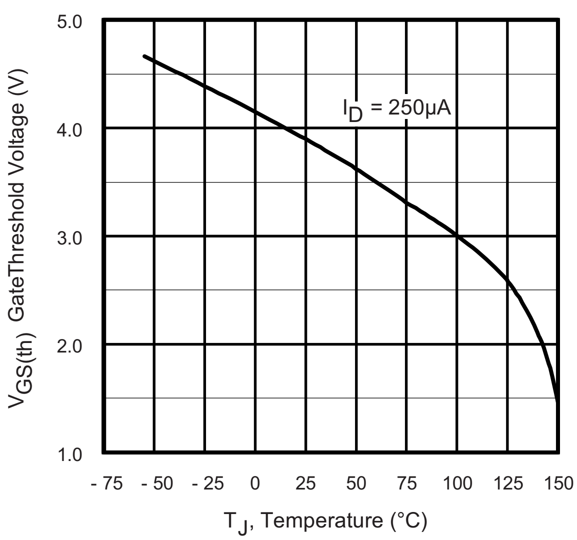


Fig. 13 - Threshold Voltage vs. Temperature

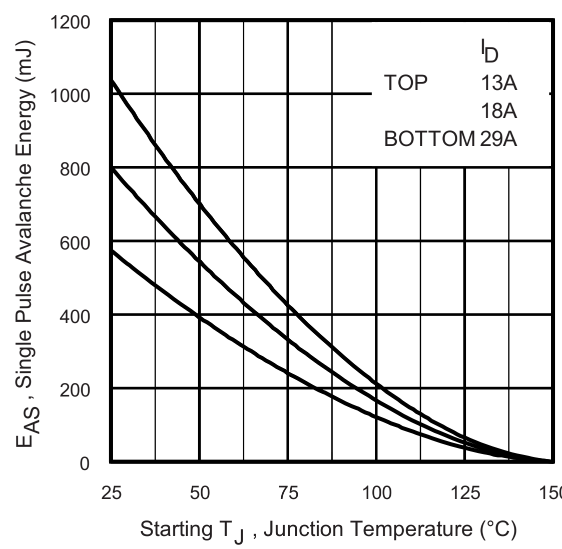


Fig. 14a - Maximum Avalanche Energy vs. Drain Current

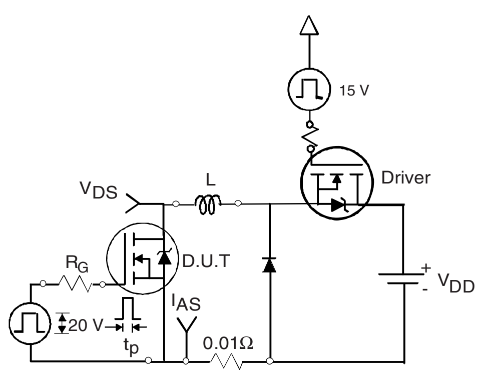


Fig. 14b - Unclamped Inductive Test Circuit

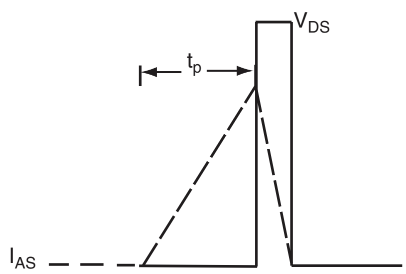


Fig. 14c - Unclamped Inductive Waveforms

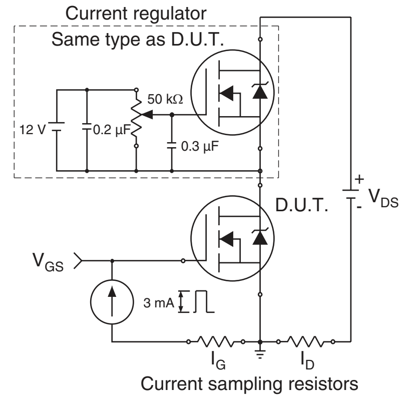


Fig. 15a - Gate Charge Test Circuit

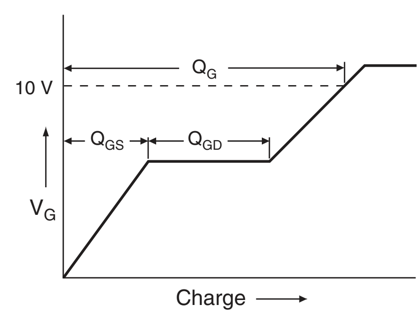
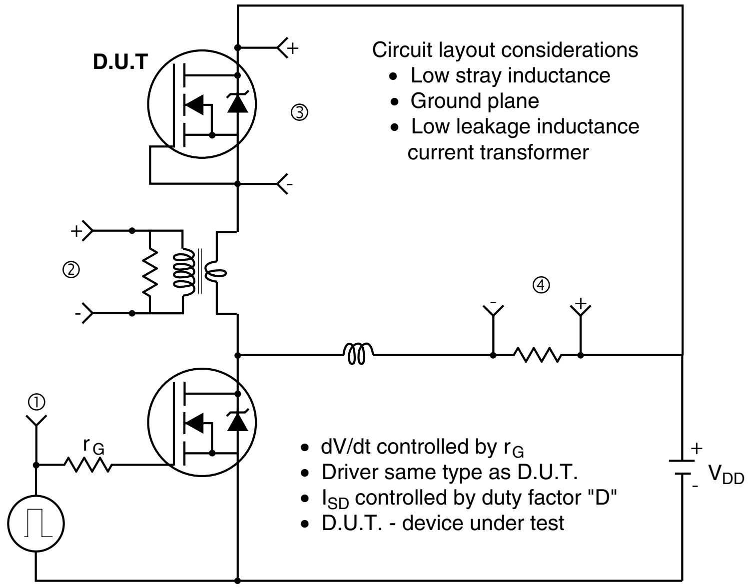
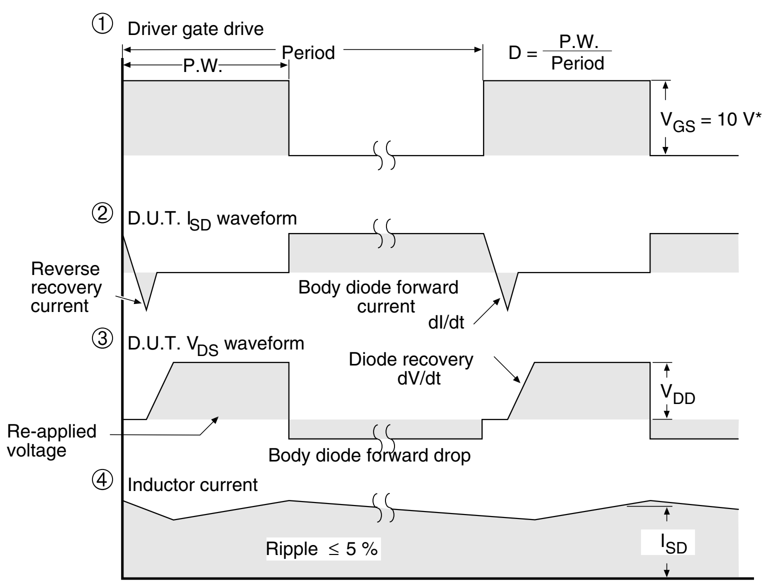


Fig. 15b - Basic Gate Charge Waveform

Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = 5 V for logic level devices

Fig. 16 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?91255.

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.