Silicon PNP Power Transistors 2SB689

DESCRIPTION

- ·With TO-220C package
- ·Low collector saturation voltage
- ·High power dissipation

APPLICATIONS

- ·For low frequency power amplifier, TV vertical deflection ouptut applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base

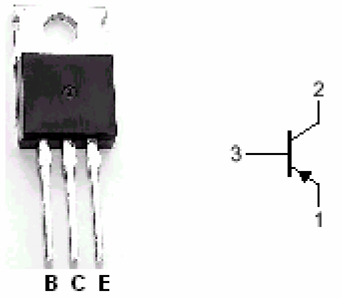

Fig.1 simplified outline (TO-220) and symbol

Absolute maximum ratings (Ta=25℃)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-100	V
V_{CEO}	Collector-emitter voltage	Open base	-100	V
V_{EBO}	Emitter-base voltage	Open collector	-4	V
I_C	Collector current		-4	A
I_{CM}	Collector current-peak		-5	A
P_C	Collector power dissipation	T_C=25℃	40	W
		T_a=25℃	1.8	
T_j	Junction temperature		150	℃
T_{stg}	Storage temperature		-45~150	℃

CHARACTERISTICS

Tj=25℃ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=-10mA; $R_{BE}=\infty$	-100			V
$V_{(BR)EBO}$	Emitter-base breakdown votage	I_E=-1mA; I_C=0	-4			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=-1A;I_B=-0.1 A			-1.0	V
I_{CEO}	Collector cut-off current	V_{CE}=-80V; $R_{BE}=\infty$			-100	μA
I_{EBO}	Emitter cut-off current	V_{EB}=-3.5V; I_C=0			-50	μA
h_{FE-1}	DC current gain	I_C=-0.5A ; V_{CE}=-4V	50		250	
h_{FE-2}	DC current gain	I_C=-50mA ; V_{CE}=-4V	25		350	

PACKAGE OUTLINE

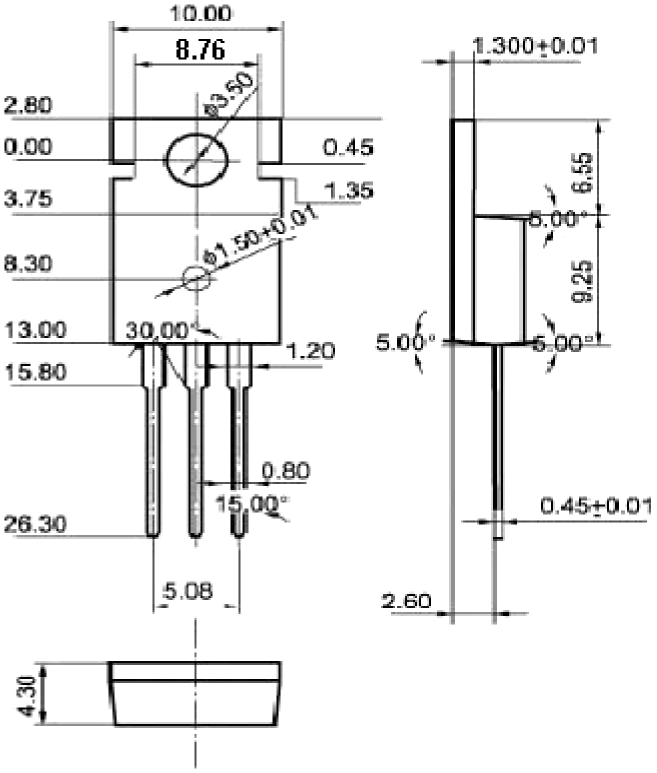

Fig.2 Outline dimensions (unindicated tolerance:±0.10 mm)