

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCXR164245FT

16-Bit Dual Supply Bus Transceiver with Series Resistor

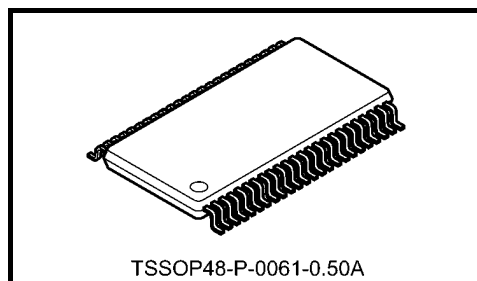
The TC74LCXR164245FT is a dual supply, advanced high-speed CMOS 16-bit dual supply voltage interface bus transceiver fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 5-V bus and a 3.3-V or 2.5-V bus in mixed 5-V/3.3-V or 2.5-V supply systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is intended for 2 way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input. The enable input (\overline{OE}) can be used to disable the device so that the buses are effectively isolated. The B-port interfaces with the 5-V bus, the A-port with the 3.3-V or 2.5-V-bus.

The 26- Ω series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



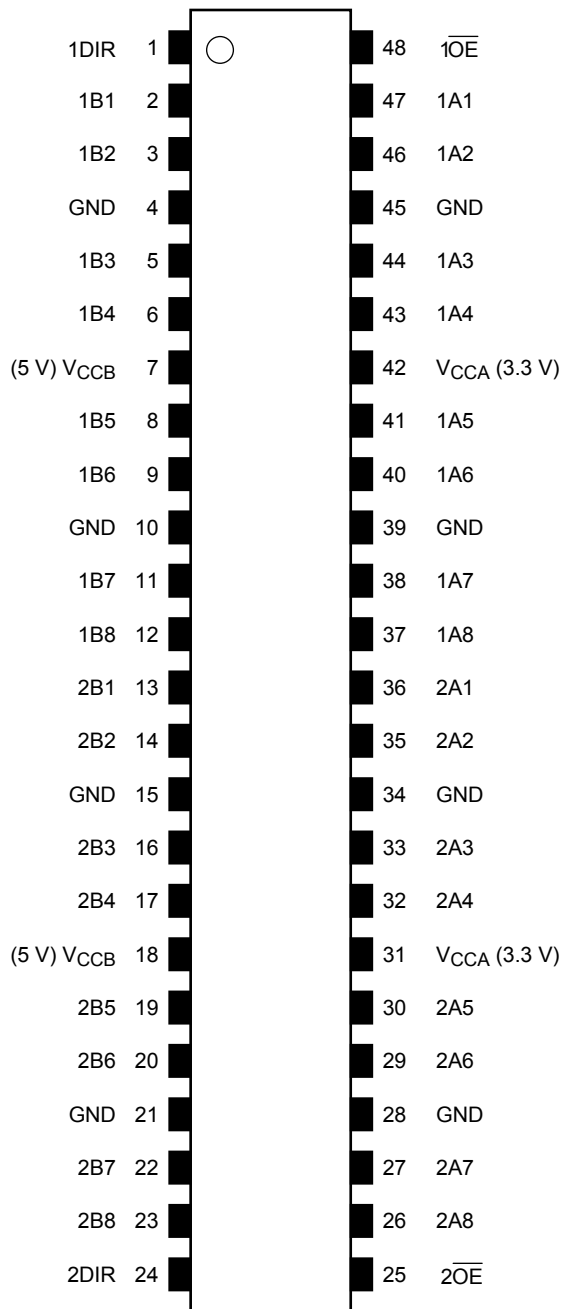
Weight: 0.25 g (typ.)

Features (Note)

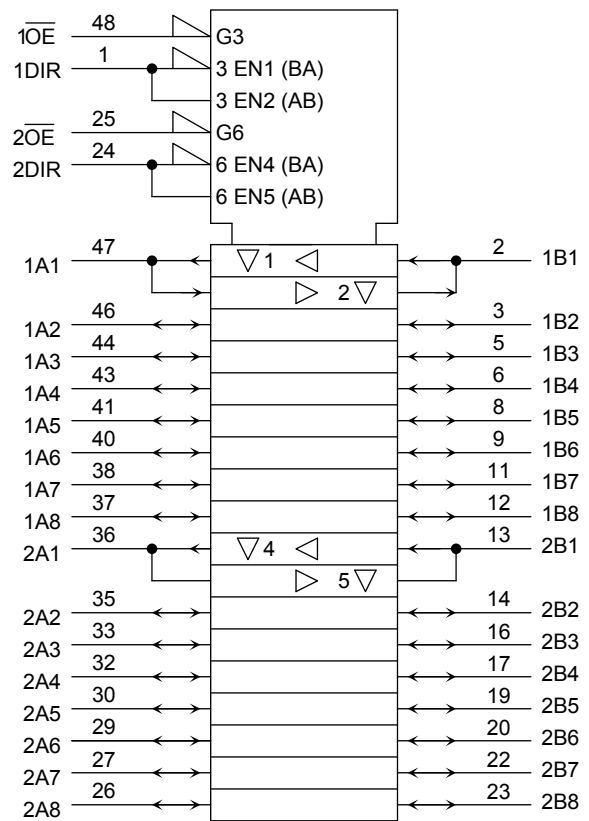
- Bidirectional interface between 5 V and 3.3 V or 2.5 V buses
- 26- Ω series resistors on outputs
- High-speed: $t_{pd} = 6.8$ ns (max)
($V_{CCB} = 5.0 \pm 0.5$ V/ $V_{CCA} = 3.3 \pm 0.3$ V, $T_a = -40$ to 85°C)
- Low power dissipation: $I_{CC} = 80$ μA (max) ($T_a = -40$ to 85°C)
- Symmetrical output impedance: $I_{OUTB} = \pm 12$ mA (min)
 $I_{OUTA} = \pm 12$ mA (min)
($V_{CCB} = 4.5$ V/ $V_{CCA} = 3.0$ V)
- Power-down protection is provided on all inputs and outputs.
- Allows A port and V_{CCA} to float simultaneously when \overline{OE} is "H"
- Latch-up performance: -500 mA
- Package: TSSOP

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pins must have their input fixed by means of pull-up or pull-down resistors.

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

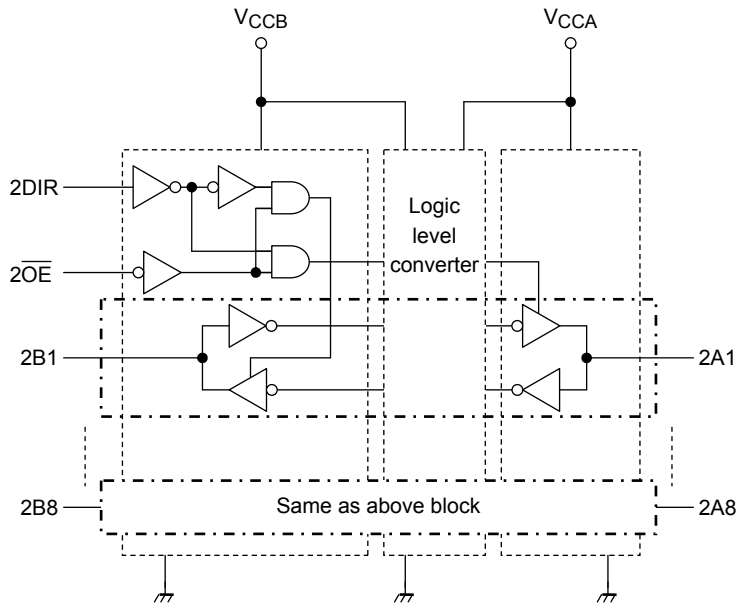
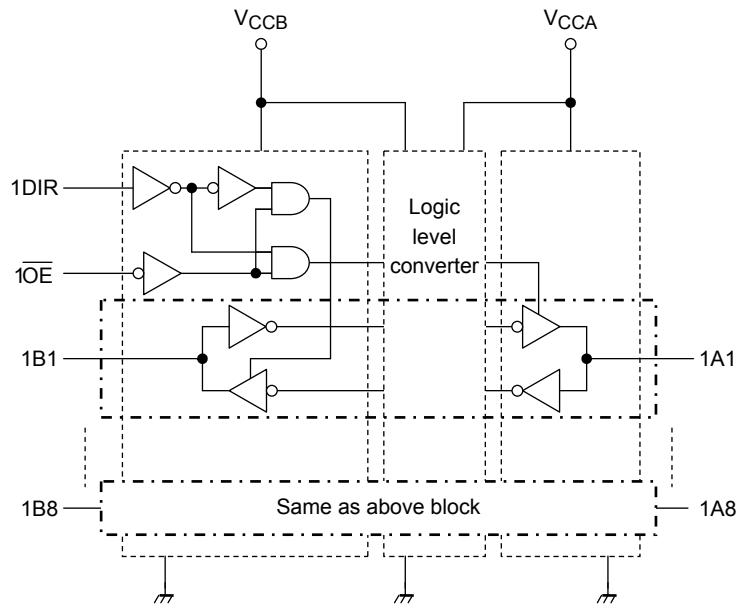
Inputs		Function		Outputs
$\overline{1OE}$	1DIR	Bus 1A1-1A8	Bus 1B1-1B8	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

Inputs		Function		Outputs
$\overline{2OE}$	2DIR	Bus 2A1-2A8	Bus 2B1-2B8	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

X: Don't care

Z: High impedance

Block Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 2)	V_{CCB}	-0.5 to 7.0	V
	V_{CCA}	-0.5 to $V_{CCB} + 0.5$	
DC input voltage (DIR, \overline{OE})	V_{IN}	-0.5 to 7.0	V
DC bus I/O voltage	$V_{I/OB}$	-0.5 to 7.0 (Note 3)	V
		-0.5 to $V_{CCB} + 0.5$ (Note 4)	
	$V_{I/OA}$	-0.5 to 7.0 (Note 3)	
		-0.5 to $V_{CCA} + 0.5$ (Note 4)	
Input diode current	I_{IK}	-50	mA
Output diode current	$I_{I/OK}$	± 50 (Note 5)	mA
DC output current	I_{OUTB}	± 50	mA
	I_{OUTA}	± 50	
DC V_{CC} /ground current per supply pin	I_{CCB}	± 100	mA
	I_{CCA}	± 100	
Power dissipation	P_D	400	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: $V_{CCB} > V_{CCA}$

Don't supply a voltage to V_{CCA} terminal when V_{CCB} is in the off-state.

Note 3: OFF state

Note 4: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 5: $V_{OUT} < GND, V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CCB}	4.5 to 5.5	V
	V_{CCA}	2.3 to 3.6	
Input voltage (DIR, \overline{OE})	V_{IN}	0 to 5.5	V
Bus I/O voltage	$V_{I/OB}$	0 to 5.5 (Note 2)	V
		0 to V_{CCB} (Note 3)	
	$V_{I/OA}$	0 to 5.5 (Note 2)	
		0 to V_{CCA} (Note 3)	
Output current	I_{OUTB}	± 12 (Note 4)	mA
		± 12 (Note 5)	
	I_{OUTA}	± 4 (Note 6)	
Operating temperature	T_{opr}	-40 to 85	$^{\circ}\text{C}$
Input rise and fall time	dt/dv	0 to 10 (Note 7)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND. Please connect both bus inputs and the bus outputs with VCC or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 2: OFF state

Note 3: High or low state

Note 4: $V_{CCB} = 4.5$ to 5.5 V

Note 5: $V_{CCA} = 3.0$ to 3.6 V

Note 6: $V_{CCA} = 2.3$ to 2.7 V

Note 7: $V_{INB} = 0.8$ to 2.0 V, $V_{CCB} = 5.0$ V
 $V_{INA} = 0.8$ to 2.0 V, $V_{CCA} = 3.0$ V

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	V _{CCB} (V)	V _{CCA} (V)	Ta = -40 to 85°C		Unit	
					Min	Max		
H-level input voltage	V _{IHB}	DIR, \overline{OE} , Bn	5.0 ± 0.5	2.3 to 3.6	2.0	—	V	
	V _{IHA}	An	5.0 ± 0.5	2.5 ± 0.2	1.7	—		
				5.0 ± 0.5	3.3 ± 0.3	2.0	—	
L-level input voltage	V _{ILB}	DIR, \overline{OE} , Bn	5.0 ± 0.5	2.3 to 3.6	—	0.8	V	
	V _{IHA}	An	5.0 ± 0.5	2.5 ± 0.2	—	0.7		
				5.0 ± 0.5	3.3 ± 0.3	—	0.8	
H-level output voltage	V _{OHB}	V _{IHA} = V _{IHA} or V _{IHA}	I _{OHB} = -100 μA	5.0 ± 0.5	2.3 to 3.6	V _{CCB} - 0.2	—	V
			I _{OHB} = -12 mA	4.5	2.3 to 3.6	3.8	—	
	V _{OHA}	V _{IHB} = V _{IHB} or V _{IHB}	I _{OHA} = -100 μA	5.0 ± 0.5	2.3 to 3.6	V _{CCA} - 0.2	—	
			I _{OHA} = -12 mA	5.0 ± 0.5	3.0	2.2	—	
		I _{OHA} = -4 mA	5.0 ± 0.5	2.3	1.8	—		
L-level output voltage	V _{OLB}	V _{IHA} = V _{IHA} or V _{IHA}	I _{OLB} = 100 μA	5.0 ± 0.5	2.3 to 3.6	—	0.2	V
			I _{OLB} = 12 mA	4.5	2.3 to 3.6	—	0.7	
	V _{OLA}	V _{IHB} = V _{IHB} or V _{IHB}	I _{OLA} = 100 μA	5.0 ± 0.5	2.3 to 3.6	—	0.2	
			I _{OLA} = 12 mA	5.0 ± 0.5	3.0	—	0.8	
		I _{OLA} = 4 mA	5.0 ± 0.5	2.3	—	0.6		
3-state output OFF state current	I _{OZB}	V _{IN} = V _{IHB} or V _{IHB} V _{I/OB} = 0 to 5.5 V	5.0 ± 0.5	2.3 to 3.6	—	±5.0	μA	
	I _{OZA}	V _{IN} = V _{IHB} or V _{IHB} V _{I/OA} = 0 to 5.5 V	5.0 ± 0.5	2.3 to 3.6	—	±5.0		
Input leakage current	I _{IN}	V _{IN} (DIR, \overline{OE}) = 0 to 5.5 V	5.5	3.6	—	±5.0	μA	
Power-off leakage current	I _{OFF}	V _{IHA} /V _{IHB} = 5.5 V	0	0	—	10	μA	
Quiescent supply current	I _{CCB1}	V _{I/OA} = Open, V _{CCA} = Open V \overline{OE} = V _{CCB} , DIR = GND	5.5	Open	—	80	μA	
	I _{CCB2}	V _{IHA} = V _{CCA} or GND V _{IHB} = V _{CCB} or GND	5.5	3.6	—	80		
	I _{CCA}	V _{IHA} = V _{CCA} or GND V _{IHB} = V _{CCB} or GND	5.5	3.6	—	50		
	I _{CCTB}	V _{IHB} = 3.4 V per input	5.5	2.3 to 3.6	—	2.0	mA	
	I _{CCTA}	V _{IHA} = V _{CCA} - 0.6 V per input	5.0 ± 0.5	3.6	—	500	μA	

AC Characteristics (input: $t_r = t_f = 2.5 \text{ ns}$, $R_L = 500 \Omega$)

$V_{CCA} = 3.3 \pm 0.3 \text{ V}$

Characteristics	Symbol	Test Condition	CL (pF)	V_{CCB} (V)	Ta = -40 to 85°C		Unit
					Min	Max	
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Input: Bn Output: An (DIR = "L")	50	5.0 ± 0.5	1.0	6.8	ns
3-state output enable time (\overline{OE} → An)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	10.0	
3-state output disable time (\overline{OE} → An)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	9.5	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Input: An Output: Bn (DIR = "H")	50	5.0 ± 0.5	1.0	6.8	ns
3-state output enable time (\overline{OE} → Bn)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	10.0	
3-state output disable time (\overline{OE} → Bn)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	9.5	
Output to output skew	t_{osLH} t_{osHL}	(Note)	50	5.0 ± 0.5	—	1.0	ns

Note: Parameter guaranteed by design.
 $(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$

$V_{CCA} = 2.5 \pm 0.2 \text{ V}$

Characteristics	Symbol	Test Condition	CL (pF)	V_{CCB} (V)	Ta = -40 to 85°C		Unit
					Min	Max	
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Input: Bn Output: An (DIR = "L")	30	5.0 ± 0.5	1.0	9.0	ns
3-state output enable time (\overline{OE} → An)	t_{pZL} t_{pZH}		30	5.0 ± 0.5	1.0	12.5	
3-state output disable time (\overline{OE} → An)	t_{pLZ} t_{pHZ}		30	5.0 ± 0.5	1.0	11.5	
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Input: An Output: Bn (DIR = "H")	50	5.0 ± 0.5	1.0	10.0	ns
3-state output enable time (\overline{OE} → Bn)	t_{pZL} t_{pZH}		50	5.0 ± 0.5	1.0	12.5	
3-state output disable time (\overline{OE} → Bn)	t_{pLZ} t_{pHZ}		50	5.0 ± 0.5	1.0	11.5	
Output to output skew	t_{osLH} t_{osHL}	(Note)	30 or 50	5.0 ± 0.5	—	1.0	ns

Note: Parameter guaranteed by design.
 $(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$

Capacitive Characteristics (Ta = 25°C)

V_{CCB} = 5.0 V

Characteristics	Symbol	Test Circuit	Test Condition	V _{CCA} (V)	Typ.	Unit
Input capacitance	C _{IN}	—	DIR, \overline{OE}	2.5, 3.3	7	pF
Output capacitance	C _{I/O}	—	An, Bn	2.5, 3.3	8	pF
Power dissipation capacitance (Note)	C _{PD} A	—	A ⇒ B (DIR = "H")	2.5, 3.3	2	pF
			B ⇒ A (DIR = "L")	2.5, 3.3	26	
	C _{PD} B	—	A ⇒ B (DIR = "H")	2.5, 3.3	36	pF
			B ⇒ A (DIR = "L")	2.5, 3.3	4	

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

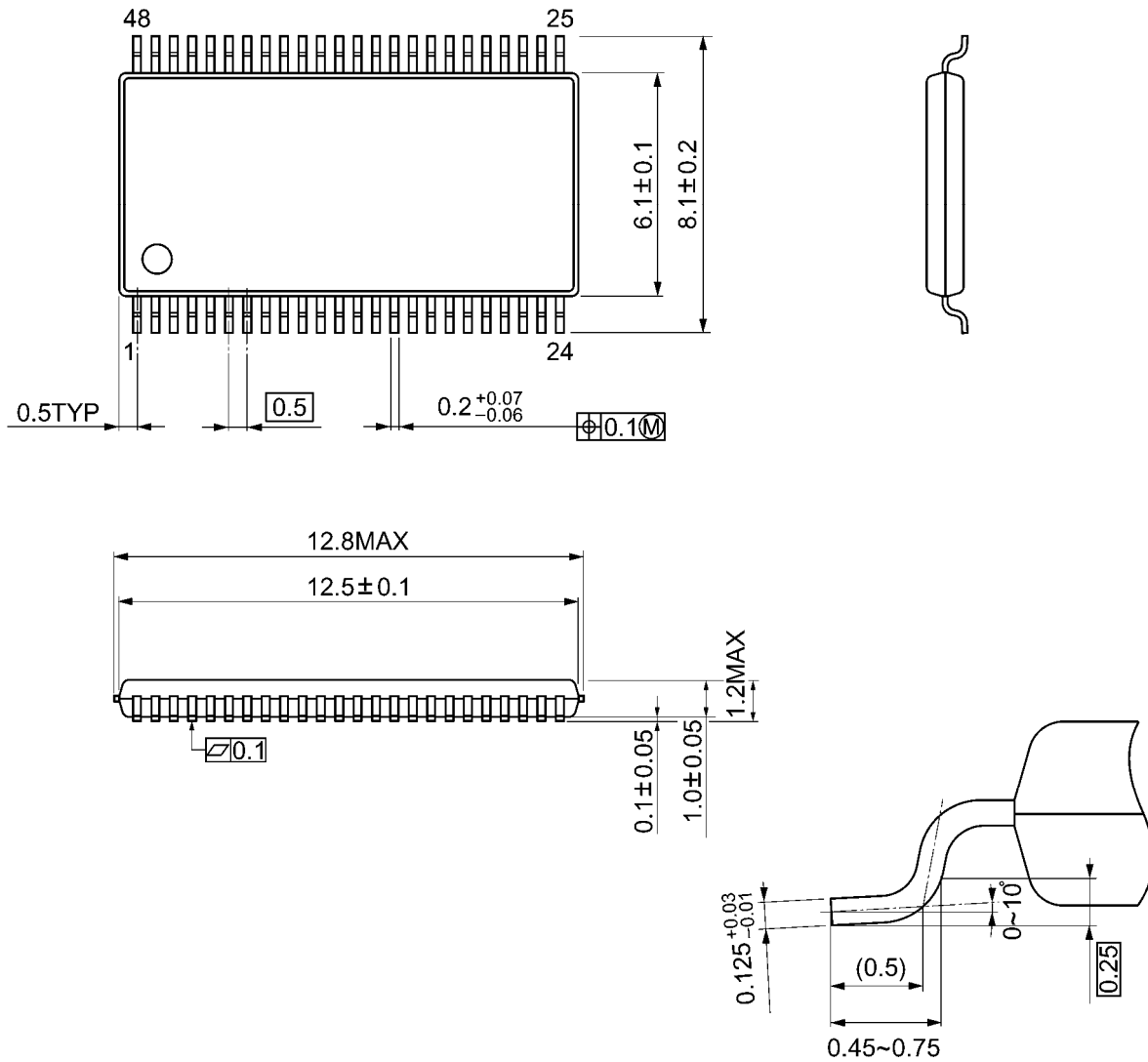
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16 \text{ (per bit)}$$

Package Dimensions

TSSOP48-P-0061-0.50A

Unit: mm



Weight: 0.25 g (typ.)

RESTRICTIONS ON PRODUCT USE

20070701-EN

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