

## 1. DESCRIPTION

The M3727GM6/M8-XXXSP/FP are single-chip microcomputers designed with CMOS silicon gate technology. They have a OSD, data slicer, and I<sup>2</sup>C-BUS interface, so it is useful for a channel selection system for TV with a closed caption decoder.

The features of the M37272E8SP/FP are similar to those of the M3727GM6/M8-XXXSP/FP except that these chips have a built-in PROM which can be written electrically. The difference between M3727GM6-XXXSP/FP and M3727GM8-XXXSP/FP are the ROM size and RAM size. Accordingly, the following descriptions will be for the M3727GM6-XXXSP/FP.

## 2. FEATURES

- Number of basic instructions ..... 71
- Memory size
  - ROM ..... 24K bytes  
(M3727GM6-XXXSP/FP)
  - 32K bytes  
(M3727GM8-XXXSP/FP, M37272E8SP/FP)
  - RAM ..... 1024 bytes  
(M3727GM6-XXXSP/FP)
  - 1152 bytes  
(M3727GM8-XXXSP/FP, M37272E8SP/FP)
 (\*ROM correction memory included)
- Minimum instruction execution time  
..... 0.5  $\mu$ s (at 8 MHz oscillation frequency)
- Power source voltage ..... 5 V  $\pm$  10 %
- Subroutine nesting ..... 128 levels (Max.)
- Interrupts ..... 17 types, 16 vectors
- 8-bit timers ..... 6
- Programmable I/O ports (Ports P0, P1, P2, P30, P31) ..... 26
- Input ports (Ports P50, P51) ..... 2
- Output ports (Ports P52-P55) ..... 4
- LED drive ports ..... 4
- Serial I/O ..... 8-bit X 1 channel
- Multi-master I<sup>2</sup>C-BUS interface ..... 1 (2 systems)
- A-D comparator (6-bit resolution) ..... 6 channels
- PWM output circuit ..... 8-bit X 6
- Power dissipation
  - In high-speed mode ..... 137.5 mW  
(at V<sub>CC</sub> = 5.5V, 8 MHz oscillation frequency, OSD on, and Data slicer on)
  - In low-speed mode ..... 0.33 mW  
(at V<sub>CC</sub> = 5.5V, 32 kHz oscillation frequency)
- ROM correction function ..... 2 vectors
- Closed caption data slicer

- OSD function
  - Display characters ..... 32 characters X 2 lines  
(It is possible to display 3 lines or more by software)
  - Kinds of characters ..... 254 kinds
  - Character display area ..... CC mode: 16 X 26 dots  
OSD mode: 16 X 20 dots
  - Kinds of character sizes ..... CC mode: 1 kind  
OSD mode: 8 kinds
  - Kinds of character colors ..... 8 colors (R, G, B)
  - Coloring unit ..... character, character background, raster
  - Display position
    - Horizontal: 128 levels      Vertical: 512 levels
  - Attribute .....
    - CC mode: smooth italic, underline, flash, automatic solid space
    - OSD mode: border
  - Smooth roll-up
  - Window function

## 3. APPLICATION

TV with a closed caption decoder

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### 4. PIN CONFIGURATION

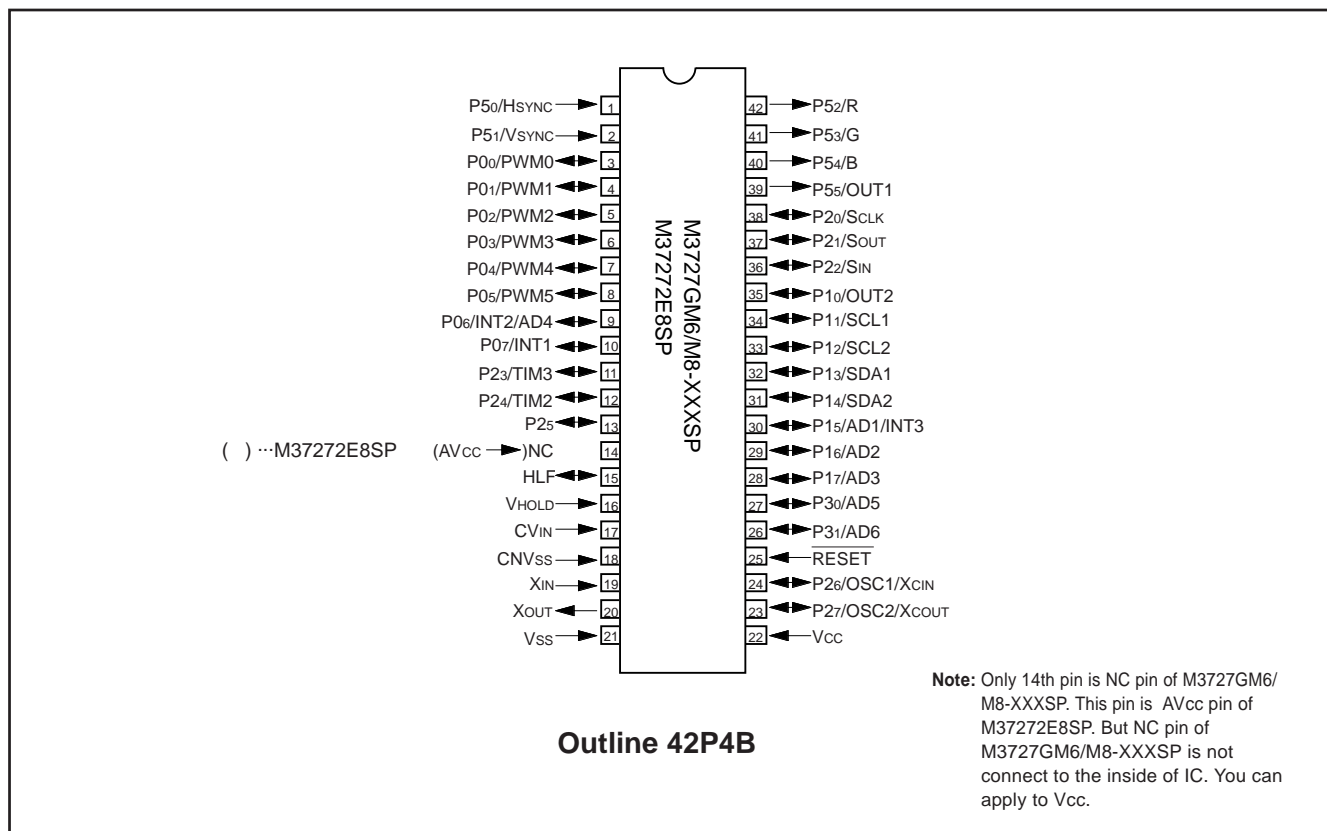


Fig. 4.1 Pin Configuration (1) (Top View)

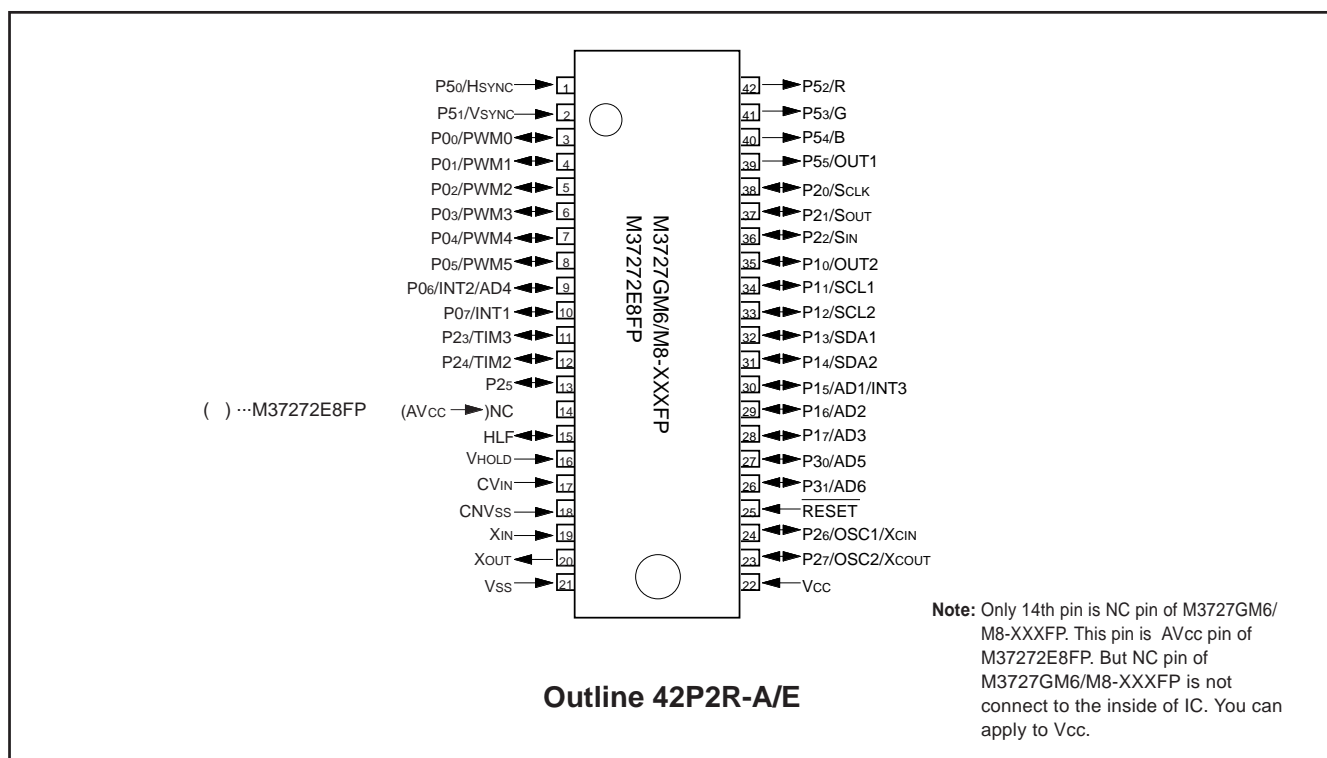


Fig. 4.2 Pin Configuration (2) (Top View)

### 5. FUNCTIONAL BLOCK DIAGRAM

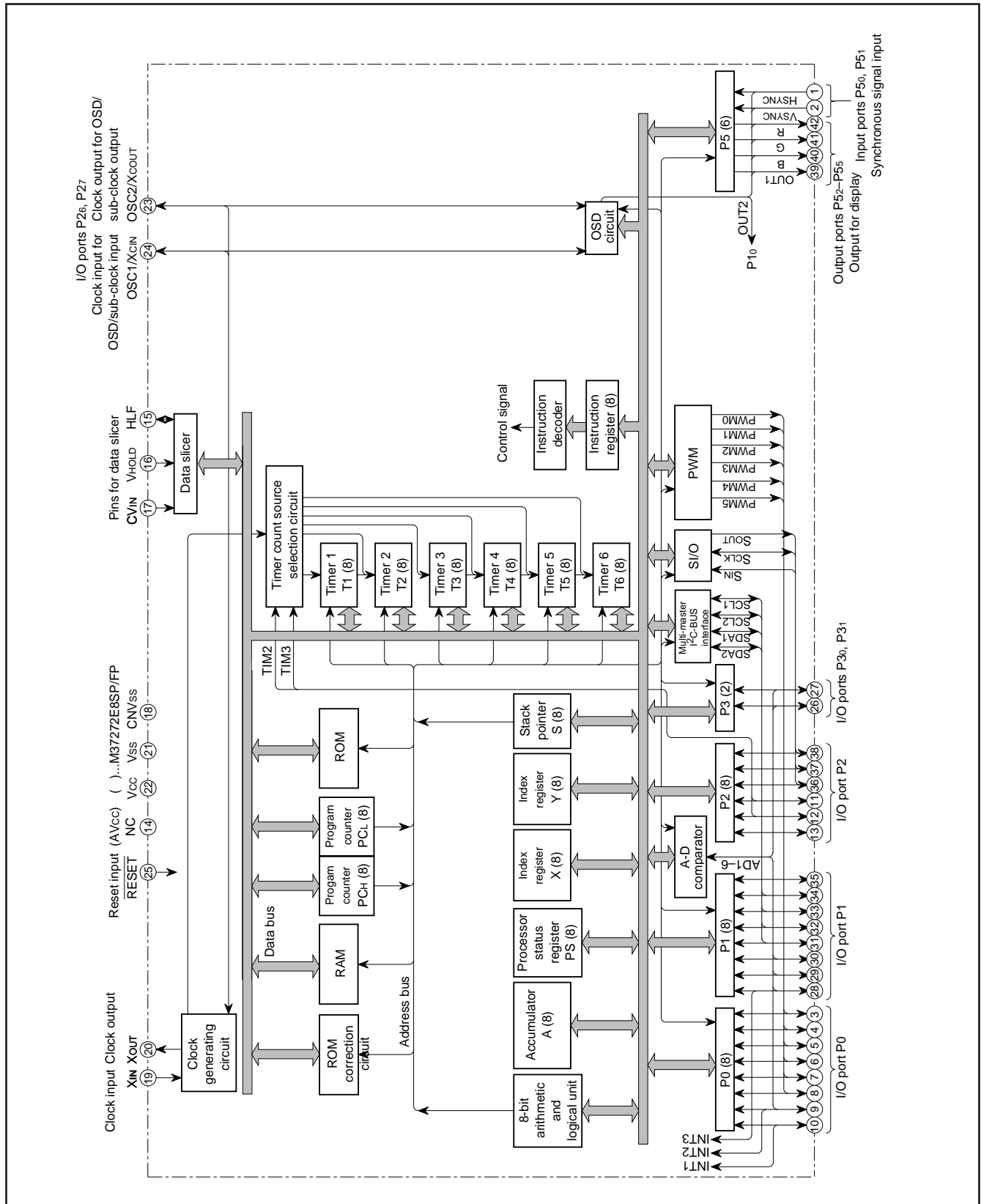


Fig. 5.1 Functional Block Diagram of M3727G

## 6. PERFORMANCE OVERVIEW

Table 6.1 Performance Overview

Parameter			Functions
Number of basic instructions			71
Instruction execution time			0.5 $\mu$ s (the minimum instruction execution time, at 8 MHz oscillation frequency)
Clock frequency			8 MHz (maximum)
Memory size	ROM	M3727GM6-XXXSP/FP	24K bytes
		M3727GM8-XXXSP/FP, M37272E8SP/FP	32K bytes
	RAM	M3727GM6-XXXSP/FP	1024 bytes (ROM correction memory included)
		M3727GM8-XXXSP/FP, M37272E8SP/FP	1152 bytes (ROM correction memory included)
	OSD ROM		10K bytes
	OSD RAM		128 bytes
Input/Output ports	P0	I/O	8-bit X 1 (N-channel open-drain output structure, can be used as PWM output pins, INT input pins, A-D input pin)
	P10–P17	I/O	8-bit X 1 (CMOS input/output structure, however, N-channel open-drain output structure, when P11–P14 are used as multi-master I <sup>2</sup> C-BUS interface, can be used as OSD output pin, A-D input pins, INT input pin, multi-master I <sup>2</sup> C-BUS interface)
	P20–P27	I/O	8-bit X 1 (P2 is CMOS input/output structure, however, N-channel open-drain output structure when P20 and 21 are used as serial output, can be used as serial input/output pins, timer external clock input pins, OSD clock input/output pin, sub-clock input/output pins)
	P30, P31	I/O	2-bit X 1 (CMOS input/output or N-channel open-drain output structure, can be used as A-D input pins)
	P50, P51	Input	2-bit X 1 (can be used as OSD input pins)
	P52–P55	Output	4-bit X 1 (CMOS output structure, can be used as OSD output pins)
Serial I/O			8-bit X 1
Multi-master I <sup>2</sup> C-BUS interface			1 (2 systems)
A-D comparator			6 channels (6-bit resolution)
PWM output circuit			8-bit X 6
Timers			8-bit timer X 6
ROM correction function			2 vectors
Subroutine nesting			128 levels (maximum)
Interrupt			<17 types> INT external interrupt X 3, Internal timer interrupt X 6, Serial I/O interrupt X 1, OSD interrupt X 1, Multi-master I <sup>2</sup> C-BUS interface interrupt X 1, Data slicer interrupt X 1, f(XIN)/4096 interrupt X 1, Vsync interrupt X 1, BRK instruction interrupt X 1, reset X 1
Clock generating circuit			2 built-in circuits (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Data slicer			Built-in

Table 6.2 Performance Overview (Continued)

Parameter			Functions
OSD function	Number of display characters		32 characters X 2 lines
	Dot structure		CC mode: 16 X 26 dots (character display area : 16 X 20 dots) OSD mode: 16 X 20 dots
	Kinds of characters		254 kinds
	Kinds of character sizes 1 screen : 8		CC mode: 1 kinds OSD mode: 8 kinds
	Character font coloring		1 screen: 8 kinds (per character unit)
	Display position		Horizontal: 128 levels, Vertical: 512 levels
Power source voltage			5V ± 10%
Power dissipation	In high-speed mode	OSD ON    Data slicer ON	137.5mW typ. ( at oscillation frequency f(XIN) = 8 MHz, fosc = 27 MHz) <165mW typ. >    < > ..When use M37272E8SP/FP
		OSD OFF    Data slicer OFF	55mW typ. ( at oscillation frequency f(XIN) = 8 MHz) <82.5mW typ. >    < > ..When use M37272E8SP/FP
	In low-speed mode	OSD OFF    Data slicer OFF	0.33 mW typ. ( at oscillation frequency f(XCIN) = 32 kHz, f(XIN) = stopped)
	In stop mode		0.055 mW ( maximum )
Operating temperature range			-10 °C to 70 °C
Device structure			CMOS silicon gate process
Package	M3727GM6/M8-XXXSP, M37272E8FP		42-pin plastic molded DIP
	M3727GM6/M8-XXXSP, M37272E8FP		42-pin plastic molded SSOP

## 7. PIN DESCRIPTION

Table 7.1 Pin Description

Pin	Name	Input/ Output	Functions
VCC, (AVCC) VSS	Power source		Apply voltage of $5\text{ V} \pm 10\%$ to (typical) VCC (AVCC), and 0 V to VSS. ( ).. Only M37272E8SP/FP
CNVSS	CNVSS		This is connected to VSS.
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a LOW for 2 $\mu\text{s}$ or more (under normal VCC conditions). If more time is needed for the quartz-crystal oscillator to stabilize, this LOW condition should be maintained for the required time.
XIN	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between pins XIN and XOUT. If an external clock is used, the clock source should be connected to the XIN pin and the XOUT pin should be left open.
XOUT	Clock output	Output	
P00/PWM0– P05/PWM5, P06/INT2/AD4, P07/INT1	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open-drain output. (See note 1)
	PWM output	Output	Pins P00–P05 are also used as PWM output pins PWM0–PWM5 respectively. The output structure is N-channel open-drain output.
	External interrupt input	Input	Pins P06 and P07 are also used as INT external interrupt input pins INT2 and INT1 respectively.
	Analog input	Input	P06 pin is also used as analog input pin AD4.
P10/OUT2, P11/SCL1, P12/SCL2, P13/SDA1, P14/SDA2, P15/AD1/INT3, P16/AD2, P17/AD3	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output. (See note 1)
	OSD output	Output	Pins P10 is also used as OSD output pin OUT2. The output structure is CMOS output.
	Multi-master I <sup>2</sup> C-BUS interface	I/O	Pins P11–P14 are used as SCL1, SCL2, SDA1 and SDA2 respectively, when multi-master I <sup>2</sup> C-BUS interface is used. The output structure is N-channel open-drain output.
	Analog input	Input	Pins P10, P15–P17 are also used as analog input pin AD8, AD1–AD3 respectively.
	External interrupt input	Input	P15 pin is also used as INT external interrupt input pin INT3.
P20/SCLK, P21/SOUT, P22/SIN, P23/TIM3, P24/TIM2, P25, P26/OSC1/ XCIN, P27/OSC2/ XCOUT	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output. (See note 1)
	Serial I/O synchronous clock input/output port	I/O	P20 pin is also used as serial I/O synchronous clock input/output pin SCLK. The output structure is N-channel open-drain output.
	Serial I/O data output	I/O	P21 pin is also used as serial I/O data output pin SOUT. The output structure is open-drain output.
	Serial I/O data input	Input	P22 pin is also used as serial I/O data input pin SIN.
	External clock input for timer	Input	Pins P23 and P24 are also used as timer external clock input pins TIM3 and TIM2 respectively.
	Clock input for OSD	Input	P26 pin is also used as OSD clock input pin OSC1. (See note 2)
	Clock output for OSD	Output	P27 pin is also used as OSD clock input pin OSC2. The output structure is CMOS output. (See note 2)
	Sub-clock input	Input	P26 pin is also used as sub-clock input pin XCIN.
Sub-clock output	Output	P27 pin is also used as sub-clock output pin XCOUT.	

Table 7.2 Pin Description (continued)

Pin	Name	Input/ Output	Functions
P30/AD5, P31/AD6	I/O port P3	I/O	Ports P30 and P31 are a 2-bit I/O port and has basically the same functions as port 0. The output structure can be selected either CMOS output or N-channel open-drain output structure. (See notes 1, 3)
	Analog input	Input	Pins P30 and P31 are also used as analog input pins AD5 and AD6 respectively.
P50/HSYNC, P51/VSYNC	Input port P5	Input	Pin P50 and P51 are 2-bit input ports.
	HSYNC input	Input	Pin P50 is also used as HSYNC input. This is a horizontal synchronous signal input for OSD.
	VSYNC input	Input	Pin P51 is also used as VSYNC input. This is a vertical synchronous signal input for OSD.
P52/R, P53/G, P54/B, P55/OUT1	Output port P5	Output	Ports P52–P55 are a 4-bit output port. The output structure is CMOS output.
	OSD output	Output	Pins P52–P55 are also used as OSD output pins R, G, B, OUT1 respectively. The output structure is CMOS output.
CVIN	I/O for data slicer	Input	Input composite video signal through a capacitor.
VHOLD		Input	Connect a capacitor between VHOLD and Vss.
HLF		I/O	Connect a filter using of a capacitor and a resistor between HLF and Vss.

**Notes 1:** Port Pi (i = 0 to 3) has the port Pi direction register which can be used to program each bit as an input ("0") or an output ("1"). The pins programmed as "1" in the direction register are output pins. When pins are programmed as "0," they are input pins. When pins are programmed as output pins, the output data are written into the port latch and then output. When data is read from the output pins, the output pin level is not read but the data of the port latch is read. This allows a previously-output value to be read correctly even if the output LOW voltage has risen, for example, because a light emitting diode was directly driven. The input pins are in the floating state, so the values of the pins can be read. When data is written into the input pin, it is written only into the port latch, while the pin remains in the floating state.

**2:** To switch output functions, set the raster color register and OSD control register. When pins P26 and P27 are used as the OSD clock input/output pins, set the corresponding bits of the port P2 direction register to "0" (input mode).

**3:** To switch output structures, set bits 2 and 3 of the port P3 direction register, When "0," CMOS output ; when "1," N-channel open-drain output.



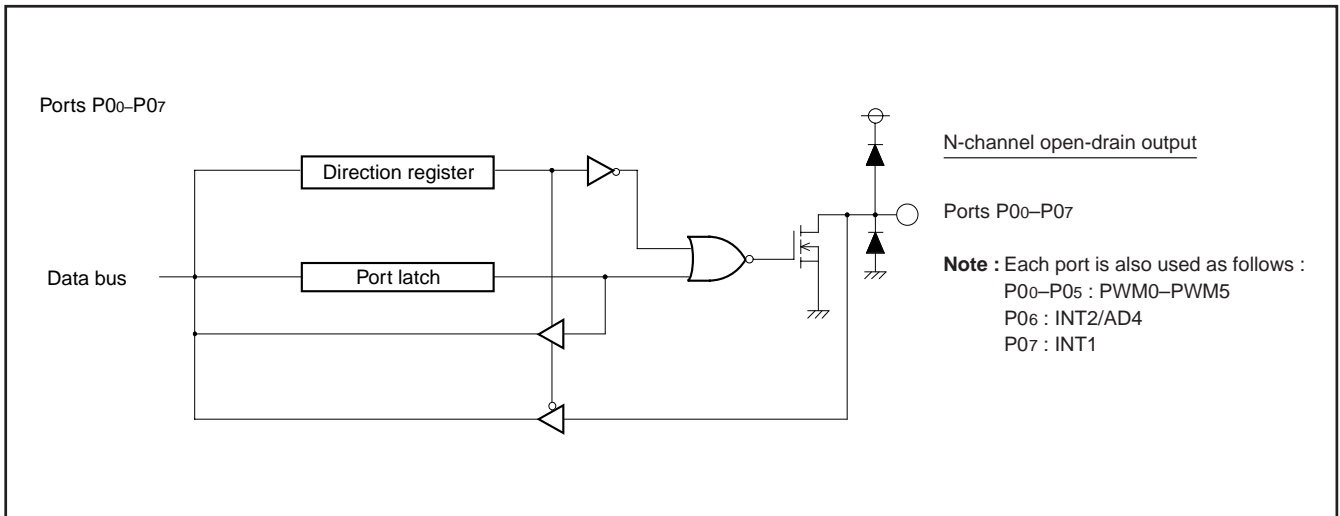


Fig. 7.1 I/O Pin Block Diagram (1)

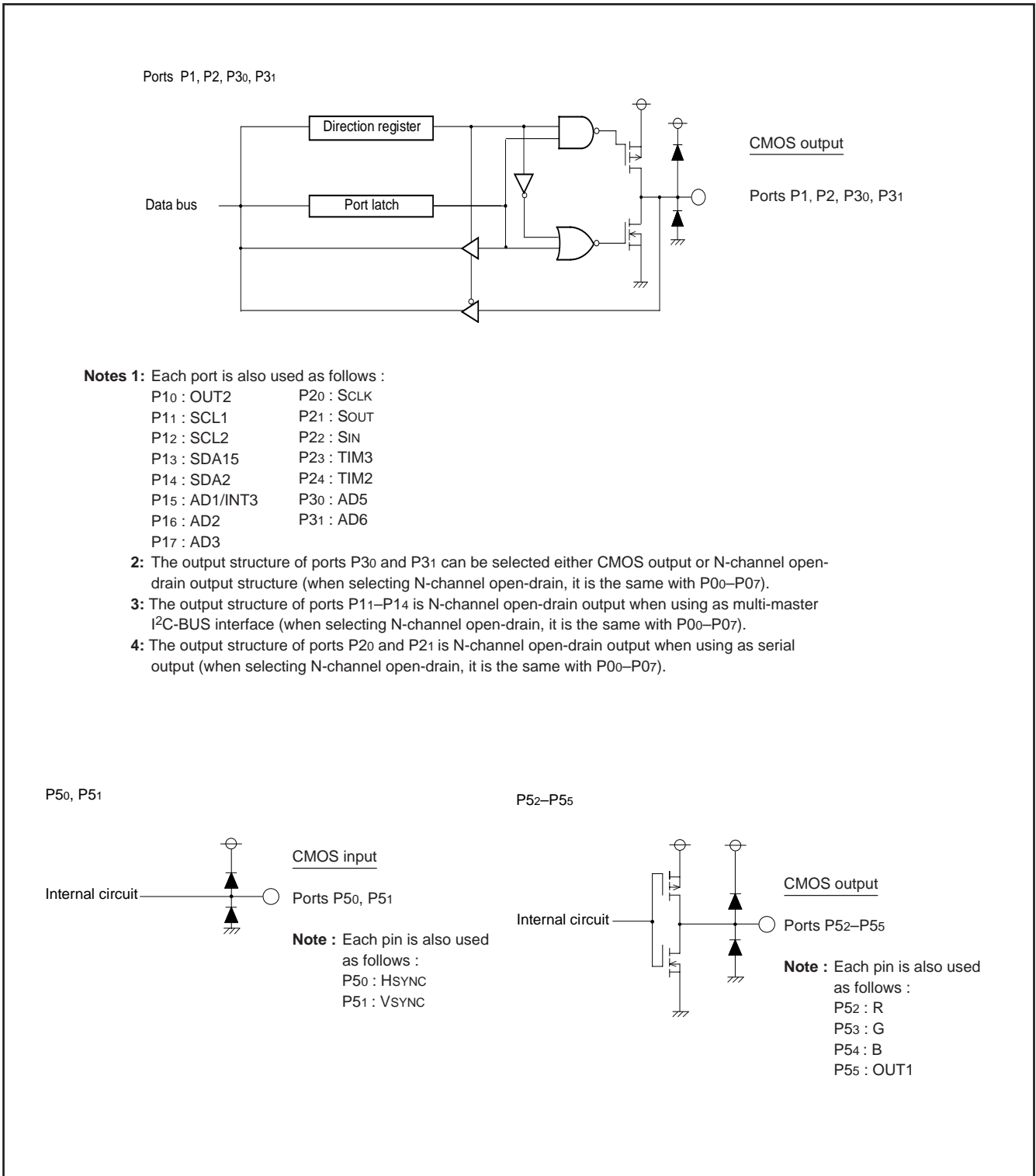


Fig. 7.2 I/O Pin Block Diagram (2)

## 8. FUNCTIONAL DESCRIPTION

### 8.1 CENTRAL PROCESSING UNIT (CPU)

This microcomputer uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instructions can be used.

#### 8.1.1 CPU Mode Register

The CPU mode register contains the stack page selection bit and internal system clock selection bit. The CPU mode register is allocated at address 00FB16.

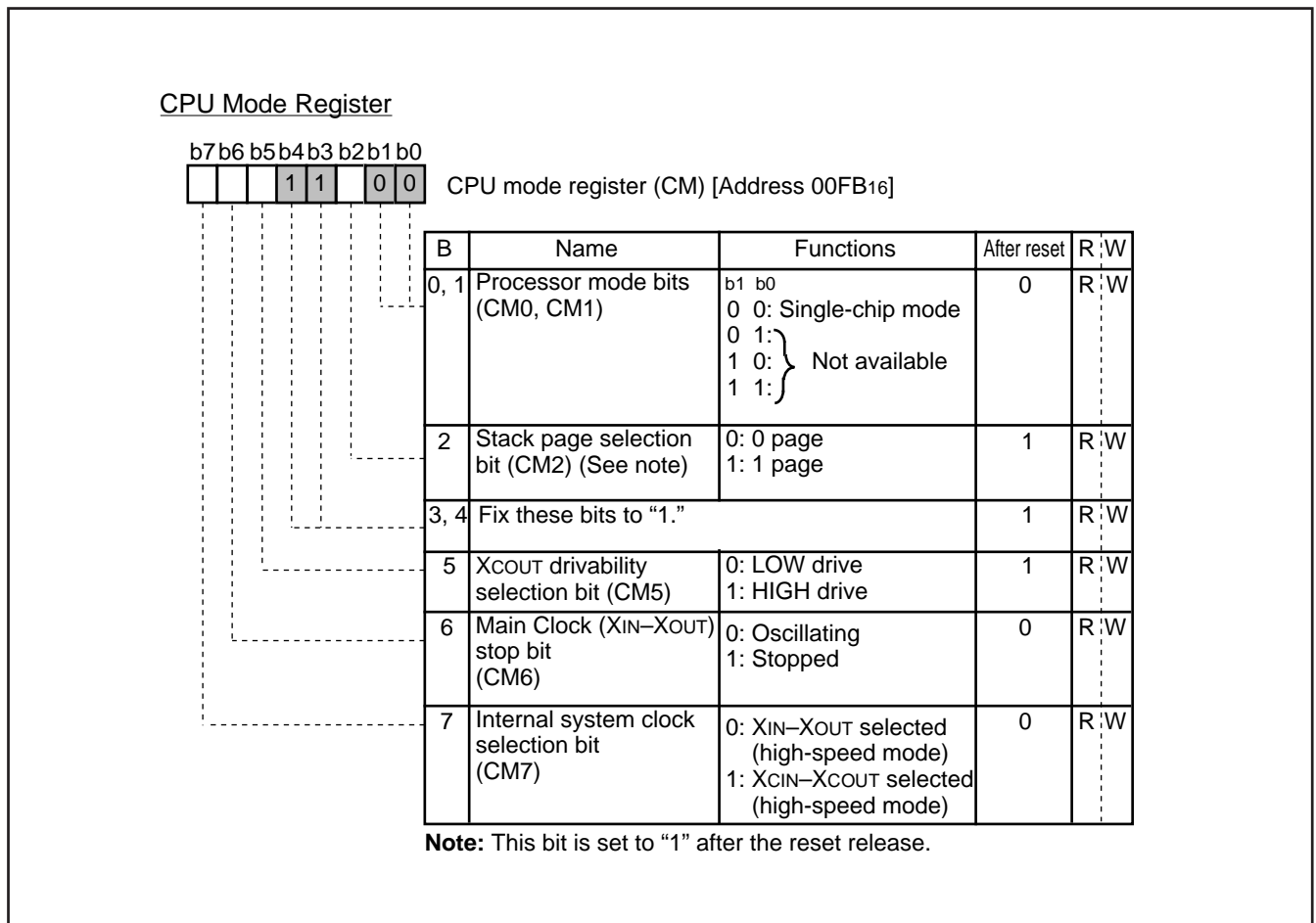


Fig. 8.1.1 CPU Mode Register

## 8.2 MEMORY

### 8.2.1 Special Function Register (SFR) Area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

### 8.2.2 RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

### 8.2.3 ROM

ROM is used for storing user programs as well as the interrupt vector area.

### 8.2.4 OSD RAM

RAM for display is used for specifying the character codes and colors to display.

### 8.2.5 OSD ROM

ROM for display is used for storing character data.

### 8.2.6 Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

### 8.2.7 Zero Page

The 256 bytes from addresses 0000<sub>16</sub> to 00FF<sub>16</sub> are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

### 8.2.8 Special Page

The 256 bytes from addresses FF00<sub>16</sub> to FFFF<sub>16</sub> are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

### 8.2.9 ROM Correction Vector

This is used as the program jump destination addresses for ROM correction.

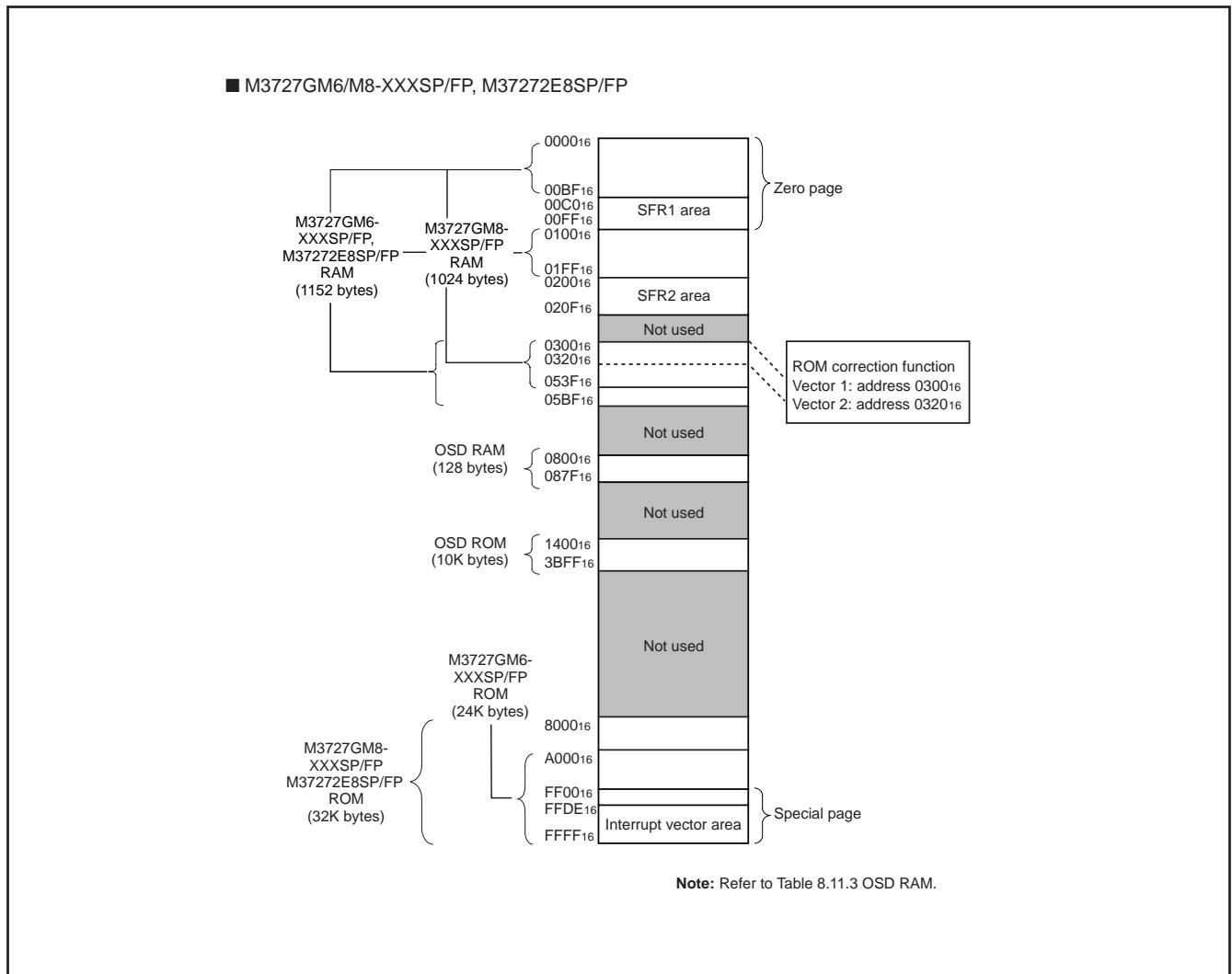


Fig. 8.2.1 Memory Map (M3727GM6/M8-XXXSP/FP, M37272E8SP/FP)

■ SFR1 Area (addresses C0<sub>16</sub> to DF<sub>16</sub>)

<Bit allocation>

- : } Function bit  
Name : }
- : No function bit
- 0 : Fix this bit to "0"  
(do not write "1")
- 1 : Fix this bit to "1"  
(do not write "0")

<State immediately after reset>

- 0 : "0" immediately after reset
- 1 : "1" immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	Bit allocation								State immediately after reset							
		b7						b0		b7						b0	
C0 <sub>16</sub>	Port P0 (P0)																
C1 <sub>16</sub>	Port P0 direction register (D0)									0	0	0	0	0	0	0	?
C2 <sub>16</sub>	Port P1 (P1)																
C3 <sub>16</sub>	Port P1 direction register (D1)									0	0	0	0	0	0	0	?
C4 <sub>16</sub>	Port P2 (P2)																
C5 <sub>16</sub>	Port P2 direction register (D2)									0	0	0	0	0	0	0	?
C6 <sub>16</sub>	Port P3 (P3)							P31	P30	0	0	0	0	0	0	0	?
C7 <sub>16</sub>	Port P3 direction register (D3)		T3SC					P31CP30C	P31DP30D								
C8 <sub>16</sub>																	
C9 <sub>16</sub>																	
CA <sub>16</sub>	Port P5 (P5)																
CB <sub>16</sub>	OSD port control register (PF)		PF7		PF5	PF4	PF3	PF2	0	0							
CC <sub>16</sub>											0	0	0	0	0	0	0
CD <sub>16</sub>																	
CE <sub>16</sub>	Caption data register 3 (CD3)	CDL27	CDL26	CDL25	CDL24	CDL23	CDL22	CDL21	CDL20								
CF <sub>16</sub>	Caption data register 4 (CD4)	CDH27	CDH26	CDH25	CDH24	CDH23	CDH22	CDH21	CDH20								
D0 <sub>16</sub>	OSD control register (OC)	0	OC6	OC5	OC4	OC3	OC2	OC1	OC0								
D1 <sub>16</sub>	Horizontal position register (HP)		HP6	HP5	HP4	HP3	HP2	HP1	HP0								
D2 <sub>16</sub>	Block control register 1 (BC1)	BC17	BC16	BC15	BC14	BC13	BC12	BC11	BC10								
D3 <sub>16</sub>	Block control register 2 (BC2)	BC27	BC26	BC25	BC24	BC23	BC22	BC21	BC20								
D4 <sub>16</sub>	Vertical position register 1 (VP1)	VP17	VP16	VP15	VP14	VP13	VP12	VP11	VP10								
D5 <sub>16</sub>	Vertical position register 2 (VP2)	VP27	VP26	VP25	VP24	VP23	VP22	VP21	VP20								
D6 <sub>16</sub>	Window register 1 (WN1)	WN17	WN16	WN15	WN14	WN13	WN12	WN11	WN10								
D7 <sub>16</sub>	Window register 2 (WN2)	WN27	WN26	WN25	WN24	WN23	WN22	WN21	WN20								
D8 <sub>16</sub>	I/O polarity control register (PC)	0	PC6	PC5	PC4	PC3	PC2	PC1	PC0								
D9 <sub>16</sub>	Raster color register (RC)	RC7	0	0	RC4	RC3	RC2	RC1	RC0								
DA <sub>16</sub>																	
DB <sub>16</sub>																	
DC <sub>16</sub>	Interrupt input polarity control register (RE)							INT3	INT2	INT1							
DD <sub>16</sub>										0	0	0	0	0	0	0	0
DE <sub>16</sub>										0	0	0	0	0	0	0	0
DF <sub>16</sub>										0	0	0	0	0	0	0	0

Fig. 8.2.2 Memory Map of Special Function Register 1 (SFR1) (1)

■ SFR1 Area (addresses E0<sub>16</sub> to FF<sub>16</sub>)

<Bit allocation>

- : } Function bit  
Name : }
- : No function bit
- 0 : Fix this bit to "0"  
(do not write "1")
- 1 : Fix this bit to "1"  
(do not write "0")

<State immediately after reset>

- 0 : "0" immediately after reset
- 1 : "1" immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	Bit allocation								State immediately after reset										
		b7						b0						b7						b0
E0 <sub>16</sub>	Data slicer control register 1 (DSC1)	0	1	1	0	0	DSC12	DSC11	DSC10											00 <sub>16</sub>
E1 <sub>16</sub>	Data slicer control register 2 (DSC2)		0	DSC25	DSC24	DSC23		1	DSC20										? 0 ? 0 ? ? 0 ?	
E2 <sub>16</sub>	Caption data register 1 (CD1)	CDL17	CDL16	CDL15	CDL14	CDL13	CDL12	CDL11	CDL10										00 <sub>16</sub>	
E3 <sub>16</sub>	Caption data register 2 (CD2)	CDH17	CDH16	CDH15	CDH14	CDH13	CDH12	CDH11	CDH10										00 <sub>16</sub>	
E4 <sub>16</sub>	Clock run-in detect register (CRD)	CRD7	CRD6	CRD5	CRD4	CRD3													00 <sub>16</sub>	
E5 <sub>16</sub>	Data clock position register (DPS)	DPS7	DPS6	DPS5	DPS4	DPS3	0	1	0										09 <sub>16</sub>	
E6 <sub>16</sub>	Caption position register (CPS)	CPS7	CPS6	CPS5	CPS4	CPS3	CPS2	CPS1	CPS0										0 0 ? 0 0 0 0 0	
E7 <sub>16</sub>	Data slicer test register 2																		00 <sub>16</sub>	
E8 <sub>16</sub>	Data slicer test register 1																		00 <sub>16</sub>	
E9 <sub>16</sub>	Synchronous signal counter register			HC5	HC4	HC3	HC2	HC1	HC0										00 <sub>16</sub>	
EA <sub>16</sub>	Serial I/O register (SIO)																		?	
EB <sub>16</sub>	Serial I/O mode register (SM)	0	SM6	SM5	0	SM3	SM2	SM1	SM0										00 <sub>16</sub>	
EC <sub>16</sub>	A-D control register 1 (AD1)				ADC14	ADC12	ADC11	ADC10											0 0 0 ? 0 0 0 0	
ED <sub>16</sub>	A-D control register 2 (AD2)				ADC25	ADC24	ADC23	ADC22	ADC21	ADC20										00 <sub>16</sub>
EE <sub>16</sub>	Timer 5 (T5)																		07 <sub>16</sub>	
EF <sub>16</sub>	Timer 6 (T6)																		FF <sub>16</sub>	
F0 <sub>16</sub>	Timer 1 (T1)																		FF <sub>16</sub>	
F1 <sub>16</sub>	Timer 2 (T2)																		07 <sub>16</sub>	
F2 <sub>16</sub>	Timer 3 (T3)																		FF <sub>16</sub>	
F3 <sub>16</sub>	Timer 4 (T4)																		07 <sub>16</sub>	
F4 <sub>16</sub>	Timer mode register 1 (TM1)	TM17	TM16	TM15	TM14	TM13	TM12	TM11	TM10										00 <sub>16</sub>	
F5 <sub>16</sub>	Timer mode register 2 (TM2)	TM27	TM26	TM25	TM24	TM23	TM22	TM21	TM20										00 <sub>16</sub>	
F6 <sub>16</sub>	I <sup>2</sup> C data shift register (S0)	D7	D6	D5	D4	D3	D2	D1	D0										?	
F7 <sub>16</sub>	I <sup>2</sup> C address register (S0D)	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	RBW										00 <sub>16</sub>	
F8 <sub>16</sub>	I <sup>2</sup> C status register (S1)	MST	TRX	BB	PIN	AL	AAS	AD0	LRB										0 0 0 1 0 0 0 ?	
F9 <sub>16</sub>	I <sup>2</sup> C control register (S1D)	BSEL1	BSEL0	10BIT SAD	ALS	ESO	BC2	BC1	BC0										00 <sub>16</sub>	
FA <sub>16</sub>	I <sup>2</sup> C clock control register (S2)	ACK	ACK BIT	FAST MODE	CCR4	CCR3	CCR2	CCR1	CCR0										00 <sub>16</sub>	
FB <sub>16</sub>	CPU mode register (CPUM)	CM7	CM6	CM5	1	1	CM2	0	0										3C <sub>16</sub>	
FC <sub>16</sub>	Interrupt request register 1 (IREQ1)		IN3R	VSCR	OSDR	TM4R	TM3R	TM2R	TM1R										00 <sub>16</sub>	
FD <sub>16</sub>	Interrupt request register 2 (IREQ2)	0	TM56R	ICR	IN2R	CKR	S1R	DSR	IN1R										00 <sub>16</sub>	
FE <sub>16</sub>	Interrupt control register 1 (ICON1)		IN3E	VSCOE	OSDE	TM4E	TM3E	TM2E	TM1E										00 <sub>16</sub>	
FF <sub>16</sub>	Interrupt control register 2 (ICON2)	TM56C	TM56E	IICE	IN2E	CKE	S1E	DSE	IN1E										00 <sub>16</sub>	

Fig. 8.2.3 Memory Map of Special Function Register 1 (SFR1) (2)

■ SFR2 Area (addresses 200<sub>16</sub> to 20F<sub>16</sub>)

<Bit allocation>

- : } Function bit
- Name : }
- : No function bit
- 0 : Fix this bit to 0 (do not write 1)
- 1 : Fix this bit to 1 (do not write 0)

<State immediately after reset>

- 0 : 0 immediately after reset
- 1 : 1 immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	Bit allocation								State immediately after reset							
		b7							b0	b7							b0
200 <sub>16</sub>	PWM0 register (PWM0)																?
201 <sub>16</sub>	PWM1 register (PWM1)																?
202 <sub>16</sub>	PWM2 register (PWM2)																?
203 <sub>16</sub>	PWM3 register (PWM3)																?
204 <sub>16</sub>	PWM4 register (PWM4)																?
205 <sub>16</sub>	PWM5 register (PWM5)																?
206 <sub>16</sub>		00 <sub>16</sub>															?
207 <sub>16</sub>		00 <sub>16</sub>															?
208 <sub>16</sub>	PWM mode register 1 (PM1)							PM13									?
209 <sub>16</sub>	PWM mode register 2 (PM2)	0		PM25	M24	M23			PM10								0
20A <sub>16</sub>	ROM correction address 1 (high-order)																00 <sub>16</sub>
20B <sub>16</sub>	ROM correction address 1 (low-order)																00 <sub>16</sub>
20C <sub>16</sub>	ROM correction address 2 (high-order)																00 <sub>16</sub>
20D <sub>16</sub>	ROM correction address 2 (low-order)																00 <sub>16</sub>
20E <sub>16</sub>	ROM correction enable register (RCR)								RCR1								00 <sub>16</sub>
20F <sub>16</sub>																	?

Fig. 8.2.4 Memory Map of Special Function Register 2 (SFR2)

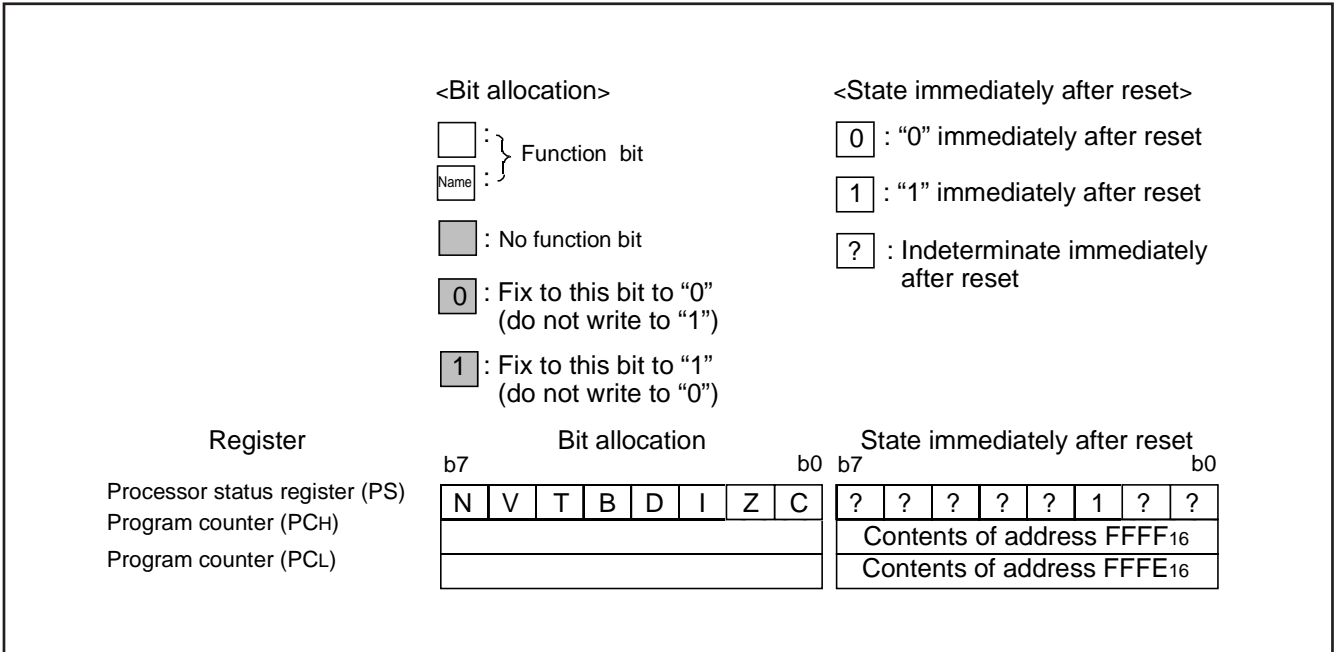


Fig. 8.2.5 Internal State of Processor Status Register and Program Counter at Reset



## 8.3 INTERRUPTS

Interrupts can be caused by 17 different sources consisting of 4 external, 11 internal, 1 software, and reset. Interrupts are vectored interrupts with priorities as shown in Table 8.3.1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted,

- ① The contents of the program counter and processor status register are automatically stored into the stack.
- ② The interrupt disable flag I is set to "1" and the corresponding interrupt request bit is set to "0."
- ③ The jump destination address stored in the vector address enters the program counter.

Other interrupts are disabled when the interrupt disable flag is set to "1."

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figures 8.3.2 to 8.3.6 show the interrupt-related registers.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1," interrupt request bit is "1," and the interrupt disable flag is "0." The interrupt request bit can be set to "0" by a program, but not set to "1." The interrupt enable bit can be set to "0" and "1" by a program.

Reset is treated as a non-maskable interrupt with the highest priority.

Figure 8.3.1 shows interrupt control.

### 8.3.1 Interrupt Causes

#### (1) VSYNC, OSD interrupts

The VSYNC interrupt is an interrupt request synchronized with the vertical sync signal.

The OSD interrupt occurs after character block display to the CRT is completed.

#### (2) INT1 to INT3 external interrupts

The INT1 to INT3 interrupts are external interrupt inputs, the system detects that the level of a pin changes from LOW to HIGH or from HIGH to LOW, and generates an interrupt request. The input active edge can be selected by bits 3 to 5 of the interrupt input polarity register (address 00DC16) : when this bit is "0," a change from LOW to HIGH is detected; when it is "1," a change from HIGH to LOW is detected. Note that both bits are cleared to "0" at reset.

#### (3) Timers 1 to 4 interrupts

An interrupt is generated by an overflow of timers 1 to 4.

**Table 8.3.1 Interrupt Vector Addresses and Priority**

Priority	Interrupt Source	Vector Addresses	Remarks
1	Reset	FFFF <sub>16</sub> , FFFE <sub>16</sub>	Non-maskable
2	OSD interrupt	FFFD <sub>16</sub> , FFFC <sub>16</sub>	
3	INT1 external interrupt	FFFB <sub>16</sub> , FFFA <sub>16</sub>	Active edge selectable
4	Data slicer interrupt	FFF9 <sub>16</sub> , FFF8 <sub>16</sub>	
5	Serial I/O interrupt	FFF7 <sub>16</sub> , FFF6 <sub>16</sub>	
6	Timer 4 interrupt	FFF5 <sub>16</sub> , FFF4 <sub>16</sub>	
7	f(XIN)/4096 interrupt	FFF3 <sub>16</sub> , FFF2 <sub>16</sub>	
8	VSYNC interrupt	FFF1 <sub>16</sub> , FFF0 <sub>16</sub>	
9	Timer 3 interrupt	FFEF <sub>16</sub> , FFEE <sub>16</sub>	
10	Timer 2 interrupt	FFED <sub>16</sub> , FFEC <sub>16</sub>	
11	Timer 1 interrupt	FFEB <sub>16</sub> , FFEA <sub>16</sub>	
12	INT3 external interrupt	FFE9 <sub>16</sub> , FFE8 <sub>16</sub>	Active edge selectable
13	INT2 external interrupt	FFE7 <sub>16</sub> , FFE6 <sub>16</sub>	Active edge selectable
14	Multi-master I <sup>2</sup> C-BUS interface interrupt	FFE5 <sub>16</sub> , FFE4 <sub>16</sub>	
15	Timer 5 • 6 interrupt	FFE3 <sub>16</sub> , FFE2 <sub>16</sub>	Source switch by software (see note)
16	BRK instruction interrupt	FFDF <sub>16</sub> , FFDE <sub>16</sub>	Non-maskable

**Note:** Switching a source during a program causes an unnecessary interrupt. Therefore, set a source at initializing of program.

**(4) Serial I/O interrupt**

This is an interrupt request from the clock synchronous serial I/O function.

**(5)  $f(X_{IN})/4096$  interrupt**

The  $f(X_{IN})/4096$  interrupt occurs regularly with a  $f(X_{IN})/4096$  period. Set bit 0 of the PWM mode register 1 to "0."

**(6) Data slicer interrupt**

An interrupt occurs when slicing data is completed.

**(7) Multi-master I<sup>2</sup>C-BUS interface interrupt**

This is an interrupt request related to the multi-master I<sup>2</sup>C-BUS interface.

**(8) Timer 5 • 6 interrupt**

An interrupt is generated by an overflow of timer 5 or 6. Their priorities are same, and can be switched by software.

**(9) BRK instruction interrupt**

This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag I (non-maskable).

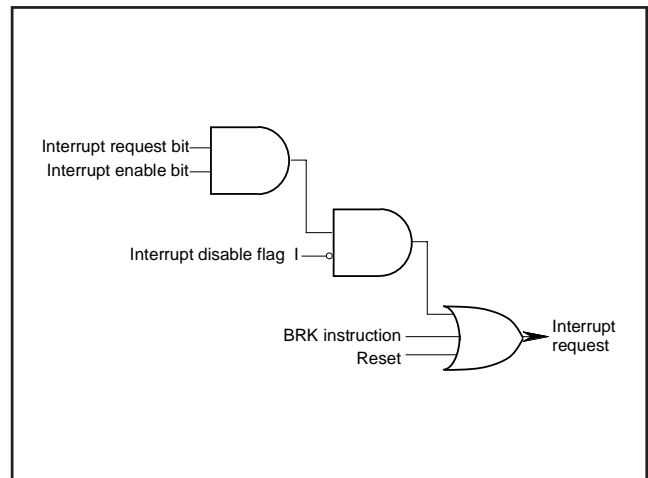
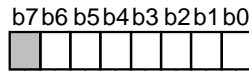


Fig. 8.3.1 Interrupt Control

**Interrupt Request Register 1**



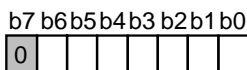
Interrupt request register 1 (IREQ1) [Address 00FC16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	OSD interrupt request bit (OSDR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	VSNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	INT3 external interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

\*: "0" can be set by software, but "1" cannot be set.

Fig. 8.3.2 Interrupt Request Register 1

**Interrupt Request Register 2**



Interrupt request register 2 (IREQ2) [Address 00FD16]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt request bit (INIR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Data slicer interrupt request bit (DSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Serial I/O interrupt request bit (S1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	f(XIN)/4096 interrupt request bit (CKR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	INT2 external interrupt request bit (IN2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	Multi-master I <sup>2</sup> C-BUS interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	Timer 5 • 6 interrupt request bit (TM56R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Fix this bit to "0."		0	R	W

\*: "0" can be set by software, but "1" cannot be set.

Fig. 8.3.3 Interrupt Request Register 2

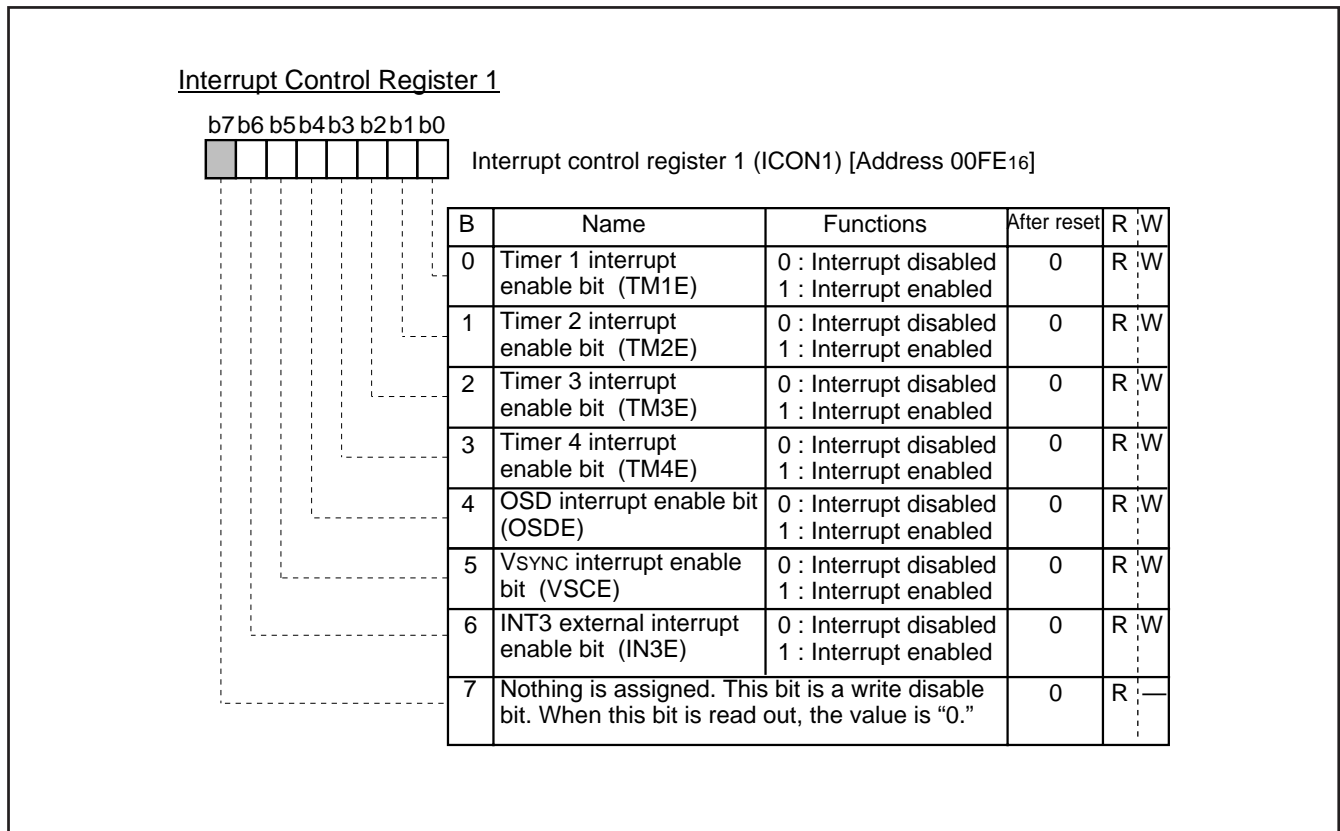


Fig. 8.3.4 Interrupt Control Register 1

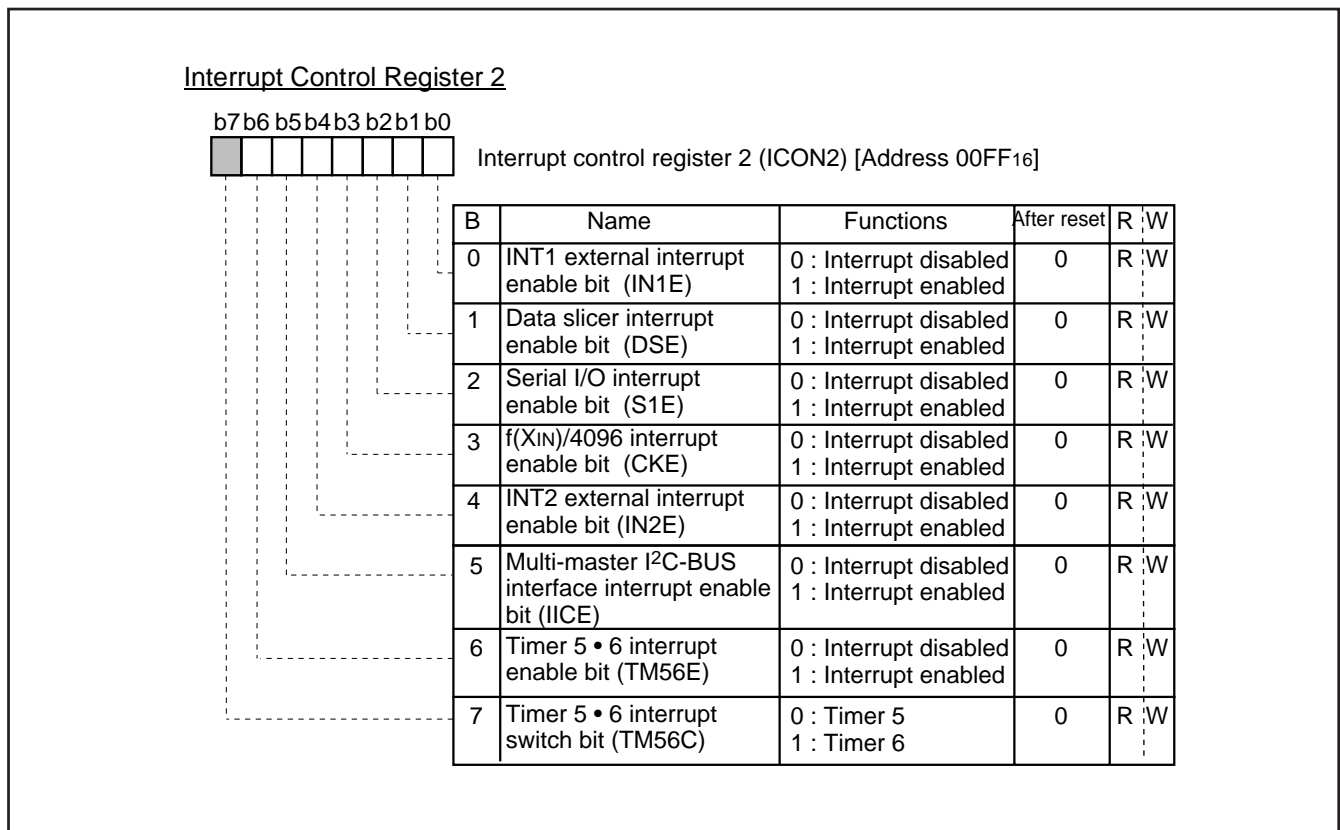


Fig. 8.3.5 Interrupt Control Register 2

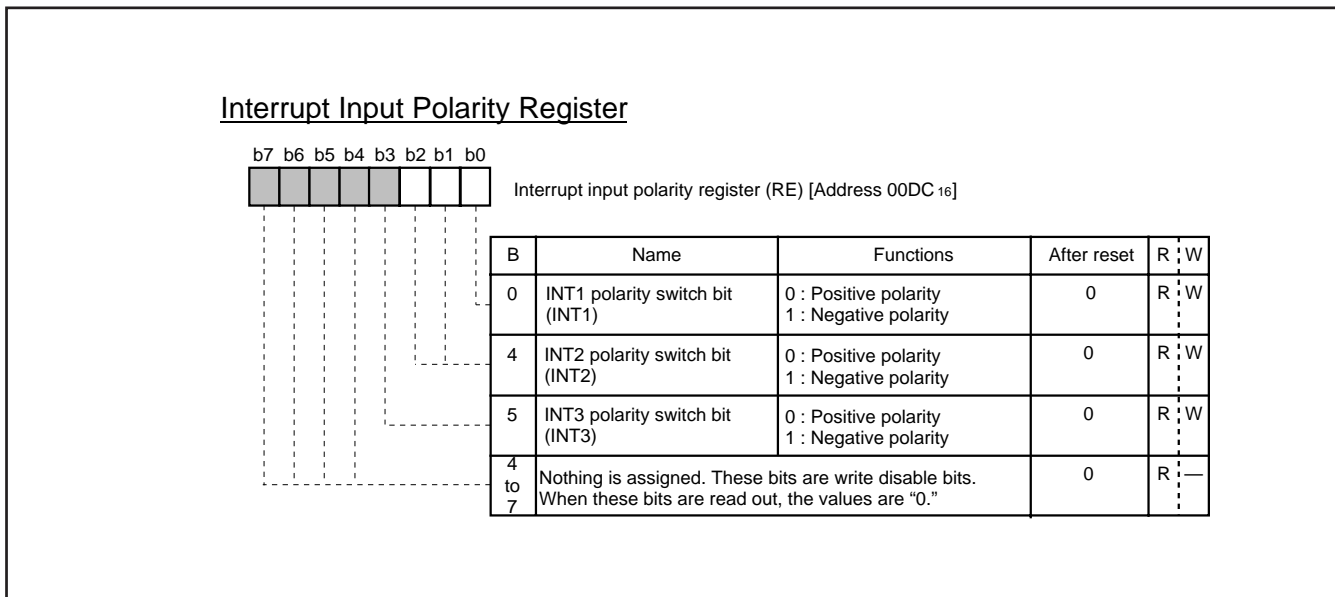


Fig. 8.3.6 Interrupt Input Polarity Register

## 8.4 TIMERS

This microcomputer has 6 timers: timer 1, timer 2, timer 3, timer 4, timer 5, and timer 6. All timers are 8-bit timers with the 8-bit timer latch. The timer block diagram is shown in Figure 8.4.3.

All of the timers count down and their divide ratio is  $1/(n+1)$ , where  $n$  is the value of timer latch. By writing a count value to the corresponding timer latch (addresses 00F0<sub>16</sub> to 00F3<sub>16</sub>: timers 1 to 4, addresses 00EE<sub>16</sub> and 00EF<sub>16</sub>: timers 5 and 6), the value is also set to a timer, simultaneously.

The count value is decremented by 1. The timer interrupt request bit is set to "1" by a timer overflow at the next count pulse, after the count value reaches "00<sub>16</sub>".

### 8.4.1 Timer 1

Timer 1 can select one of the following count sources:

- $f(XIN)/16$  or  $f(XCIN)/16$
- $f(XIN)/4096$  or  $f(XCIN)/4096$
- External clock from the TIM2 pin

The count source of timer 1 is selected by setting bits 5 and 0 of timer mode register 1 (address 00F4<sub>16</sub>). Either  $f(XIN)$  or  $f(XCIN)$  is selected by bit 7 of the CPU mode register.

Timer 1 interrupt request occurs at timer 1 overflow.

### 8.4.2 Timer 2

Timer 2 can select one of the following count sources:

- $f(XIN)/16$  or  $f(XCIN)/16$
- Timer 1 overflow signal
- External clock from the TIM2 pin

The count source of timer 2 is selected by setting bits 4 and 1 of timer mode register 1 (address 00F4<sub>16</sub>). Either  $f(XIN)$  or  $f(XCIN)$  is selected by bit 7 of the CPU mode register. When timer 1 overflow signal is a count source for the timer 2, the timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

### 8.4.3 Timer 3

Timer 3 can select one of the following count sources:

- $f(XIN)/16$  or  $f(XCIN)/16$
- $f(XCIN)$
- External clock from the TIM3 pin

The count source of timer 3 is selected by setting bit 0 of timer mode register 2 (address 00F5<sub>16</sub>) and bit 6 at address 00C7<sub>16</sub>. Either  $f(XIN)$  or  $f(XCIN)$  is selected by bit 7 of the CPU mode register.

Timer 3 interrupt request occurs at timer 3 overflow.

### 8.4.4 Timer 4

Timer 4 can select one of the following count sources:

- $f(XIN)/16$  or  $f(XCIN)/16$
- $f(XIN)/2$  or  $f(XCIN)/2$
- $f(XCIN)$

The count source of timer 3 is selected by setting bits 1 and 4 of the timer mode register 2 (address 00F5<sub>16</sub>). Either  $f(XIN)$  or  $f(XCIN)$  is selected by bit 7 of the CPU mode register. When timer 3 overflow signal is a count source for the timer 4, the timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow.

### 8.4.5 Timer 5

Timer 5 can select one of the following count sources:

- $f(XIN)/16$  or  $f(XCIN)/16$
- Timer 2 overflow signal
- Timer 4 overflow signal

The count source of timer 3 is selected by setting bit 6 of timer mode register 1 (address 00F4<sub>16</sub>) and bit 7 of the timer mode register 2 (address 00F5<sub>16</sub>). When overflow of timer 2 or 4 is a count source for timer 5, either timer 2 or 4 functions as an 8-bit prescaler. Either  $f(XIN)$  or  $f(XCIN)$  is selected by bit 7 of the CPU mode register.

Timer 5 interrupt request occurs at timer 5 overflow.

### 8.4.6 Timer 6

Timer 6 can select one of the following count sources:

- $f(XIN)/16$  or  $f(XCIN)/16$
- Timer 5 overflow signal

The count source of timer 6 is selected by setting bit 7 of the timer mode register 1 (address 00F4<sub>16</sub>). Either  $f(XIN)$  or  $f(XCIN)$  is selected by bit 7 of the CPU mode register. When timer 5 overflow signal is a count source for timer 6, the timer 5 functions as an 8-bit prescaler. Timer 6 interrupt request occurs at timer 6 overflow.

At reset, timers 3 and 4 are connected by hardware and "FF<sub>16</sub>" is automatically set in timer 3; "07<sub>16</sub>" in timer 4. The  $f(XIN) * /16$  is selected as the timer 3 count source. The internal reset is released by timer 4 overflow in this state and the internal clock is connected.

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF<sub>16</sub>" is automatically set in timer 3; "07<sub>16</sub>" in timer 4. However, the  $f(XIN) * /16$  is not selected as the timer 3 count source. So set both bit 0 of timer mode register 2 (address 00F5<sub>16</sub>) and bit 6 at address 00C7<sub>16</sub> to "0" before the execution of the STP instruction ( $f(XIN) * /16$  is selected as timer 3 count source). The internal STP state is released by timer 4 overflow in this state and the internal clock is connected.

As a result of the above procedure, the program can start under a stable clock.

\*: When bit 7 of the CPU mode register (CM7) is "1,"  $f(XIN)$  becomes  $f(XCIN)$ .

The timer-related registers is shown in Figures 8.4.1 and 8.4.2.

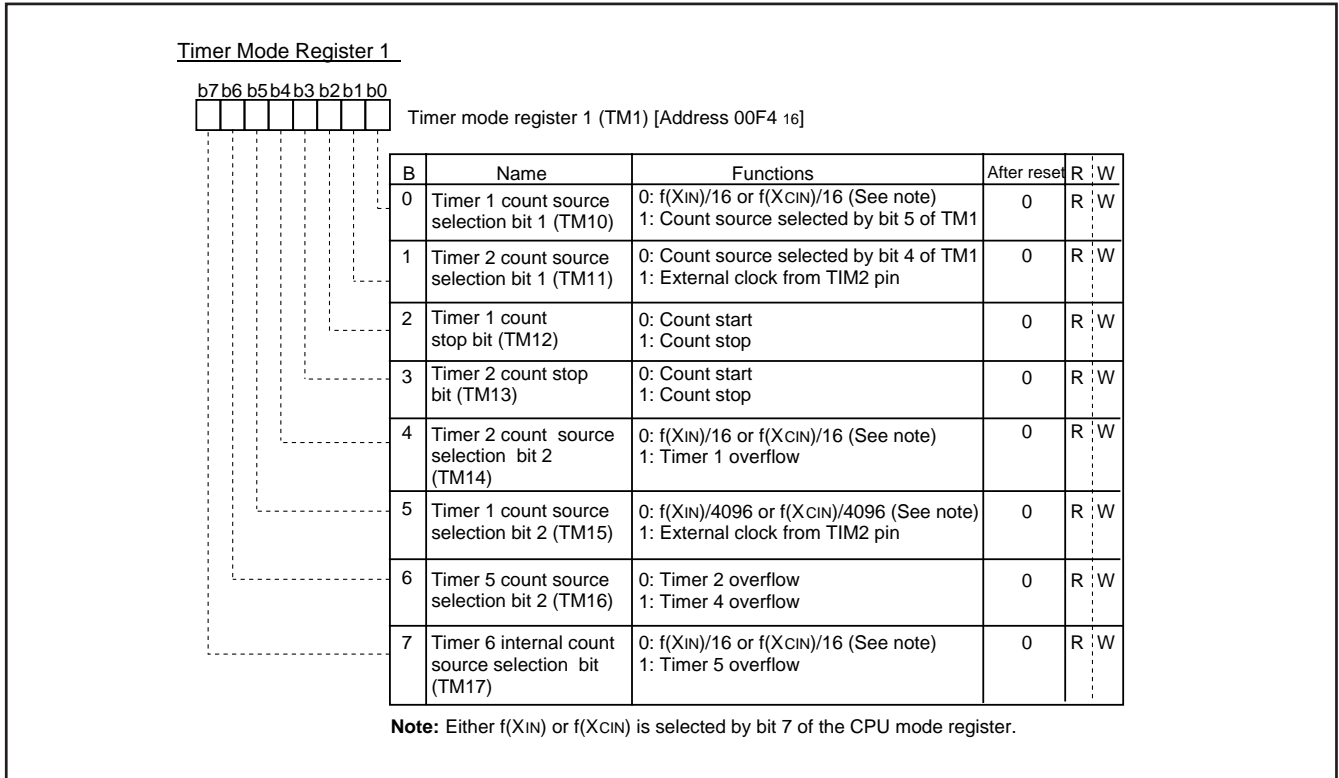


Fig. 8.4.1 Timer Mode Register 1

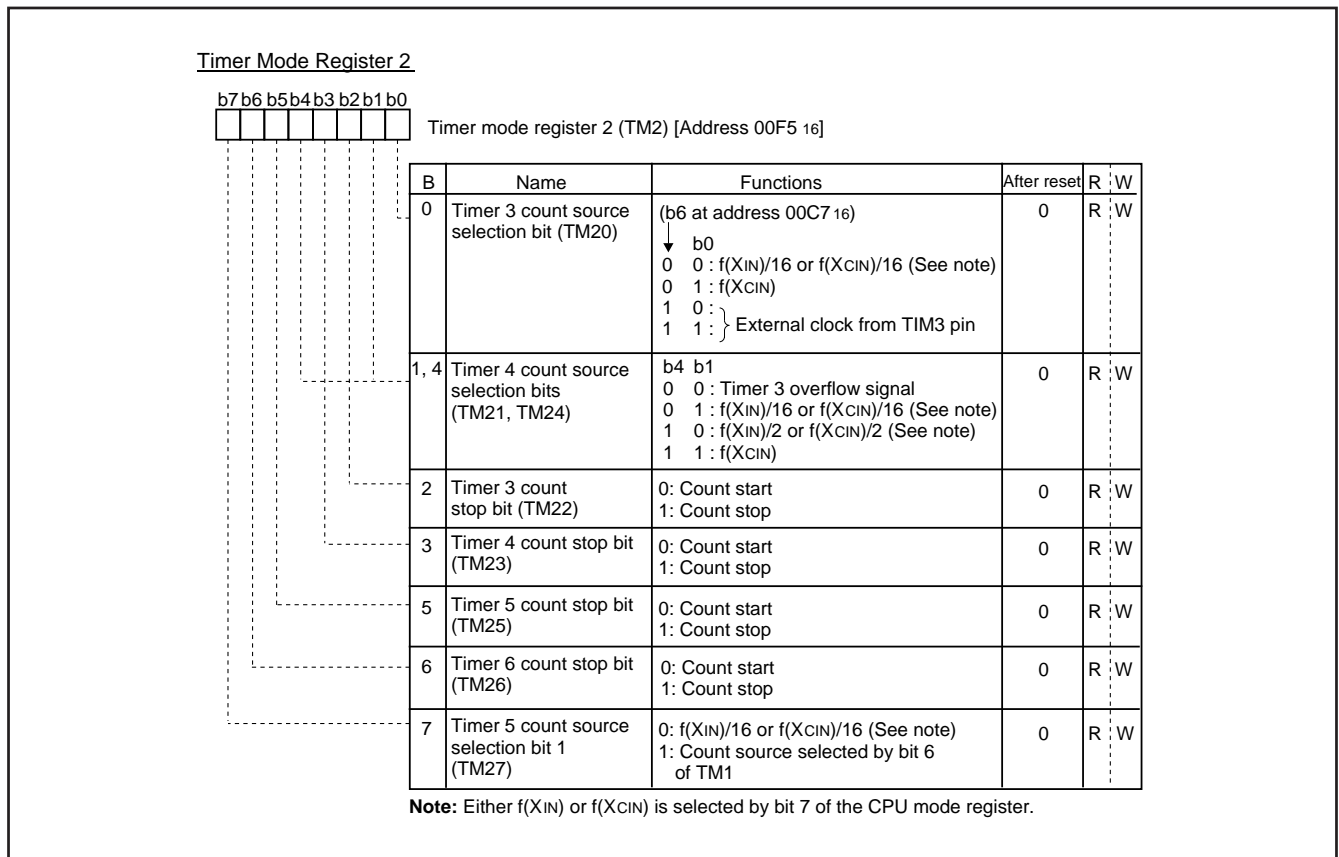


Fig. 8.4.2 Timer Mode Register 2

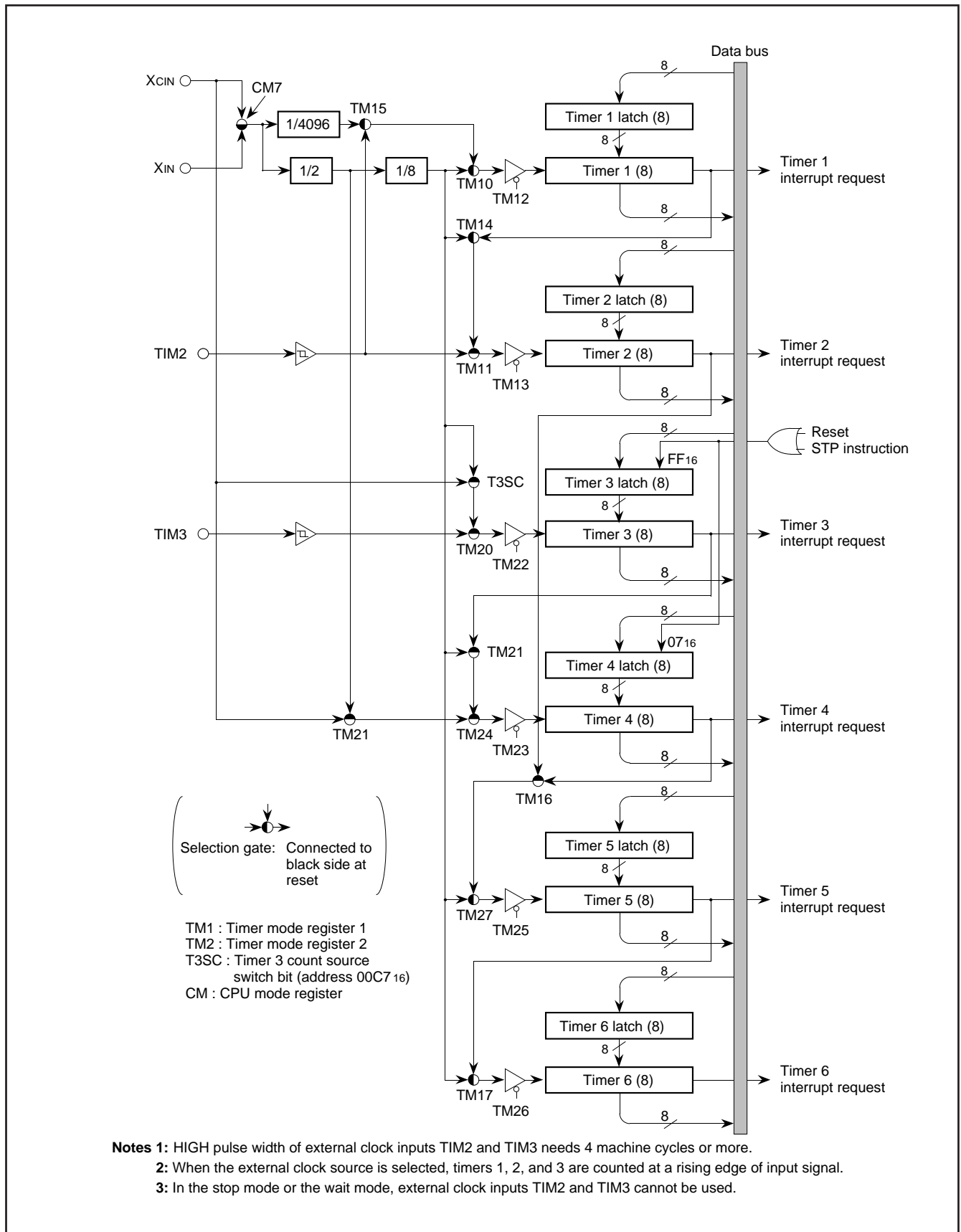


Fig. 8.4.3 Timer Block Diagram



### 8.5 SERIAL I/O

This microcomputer has a built-in serial I/O which can either transmit or receive 8-bit data serially in the clock synchronous mode.

The serial I/O block diagram is shown in Figure 8.5.1. The synchronous clock I/O pin (SCLK), and data output pin (SOUT) also function as port P4, data input pin (SIN) also functions as port P20-P22.

Bit 3 of the serial I/O mode register (address 00EB16) selects whether the synchronous clock is supplied internally or externally (from the SCLK pin). When an internal clock is selected, bits 1 and 0 select whether  $f(XIN)$  or  $f(XCIN)$  is divided by 8, 16, 32, or 64. To use the SIN pin for serial I/O, set the corresponding bit of the port P2 direction register (address 00C516) to "0."

The operation of the serial I/O is described below. The operation of the serial I/O differs depending on the clock source; external clock or internal clock.

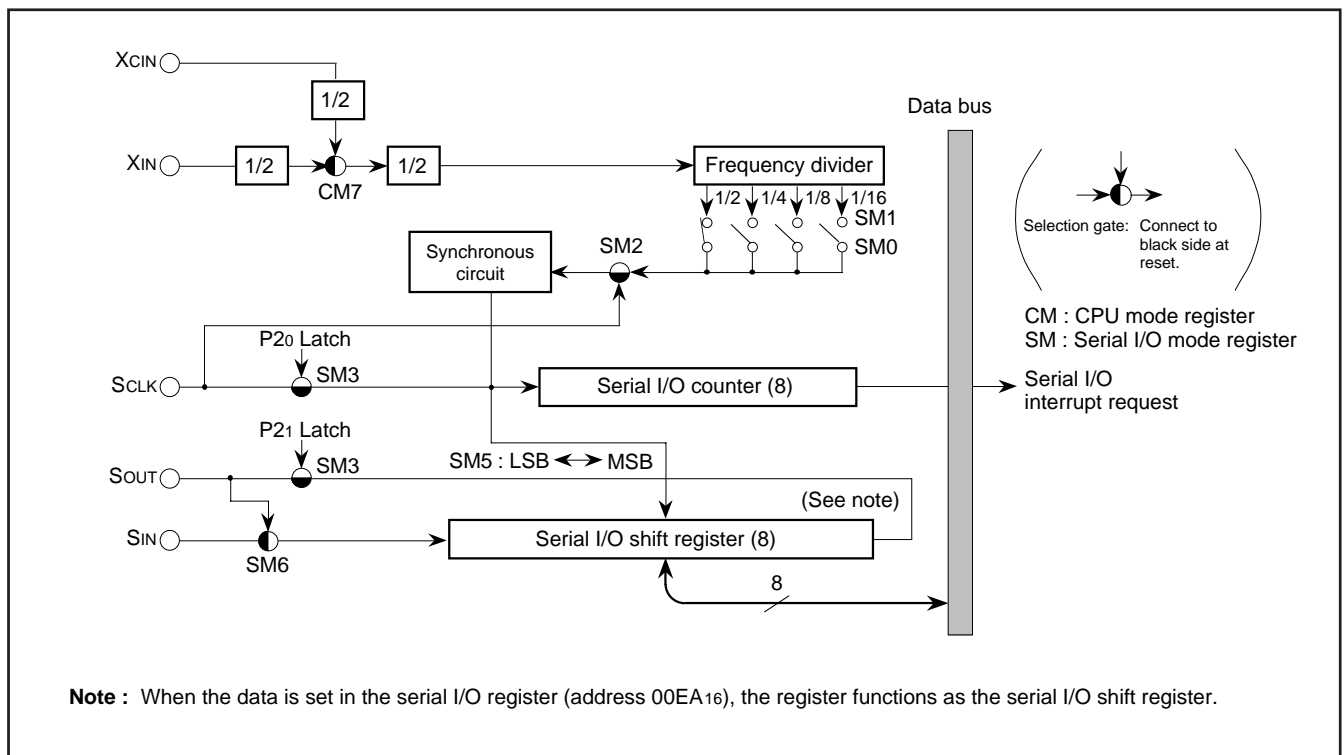


Fig. 8.5.1 Serial I/O Block Diagram

**Internal clock :** The serial I/O counter is set to “7” during the write cycle into the serial I/O register (address 00EA16), and the transfer clock goes HIGH forcibly. At each falling edge of the transfer clock after the write cycle, serial data is output from the SOUT pin. Transfer direction can be selected by bit 5 of the serial I/O mode register. At each rising edge of the transfer clock, data is input from the SIN pin and data in the serial I/O register is shifted 1 bit. After the transfer clock has counted 8 times, the serial I/O counter becomes “0” and the transfer clock stops at HIGH. At this time the interrupt request bit is set to “1.”

**External clock :** The an external clock is selected as the clock source, the interrupt request is set to “1” after the transfer clock has been counted 8 counts. However, transfer operation does not stop, so the clock should be controlled externally. Use the external clock of 1 MHz or less with a duty cycle of 50%. The serial I/O timing is shown in Figure 8.5.2. When using an external clock for transfer, the external clock must be held at HIGH for initializing the serial I/O counter. When switching between an internal clock and an external clock, do not switch during transfer. Also, be sure to initialize the serial I/O counter after switching.

- Notes 1:** On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions, such as SEB and CLB.
- 2:** When an external clock is used as the synchronous clock, write transmit data to the serial I/O register when the transfer clock input level is HIGH.

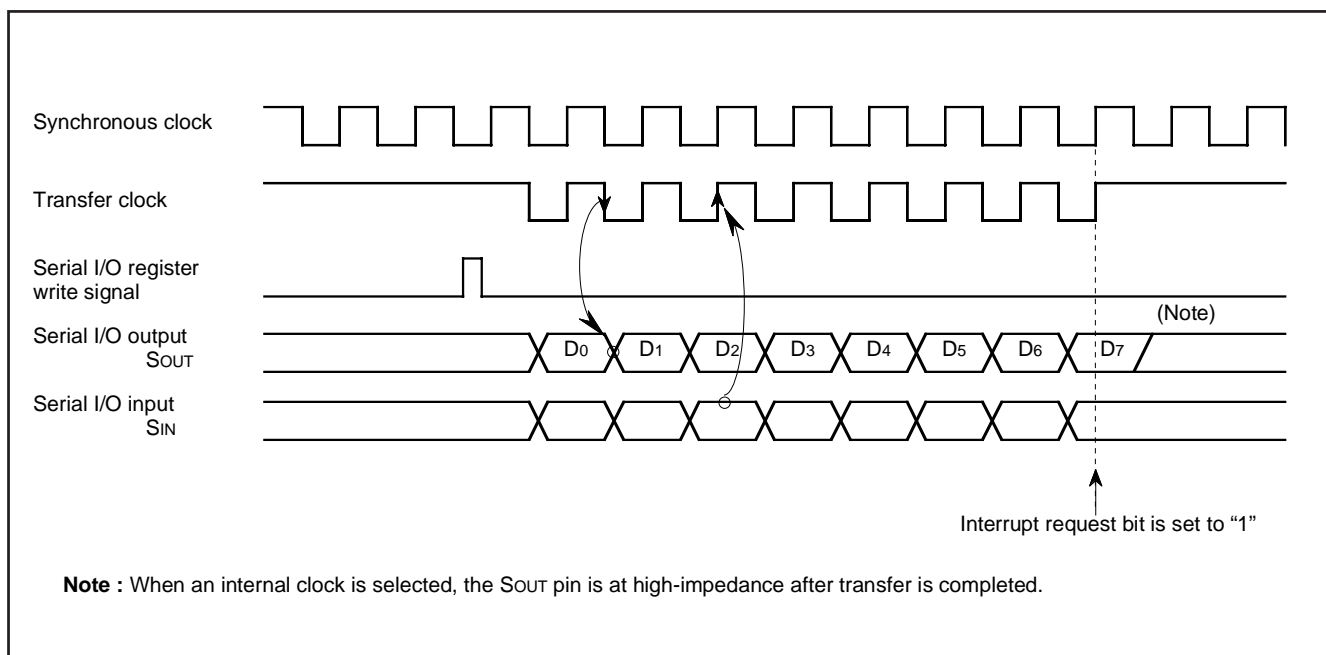


Fig. 8.5.2 Serial I/O Timing (for LSB first)

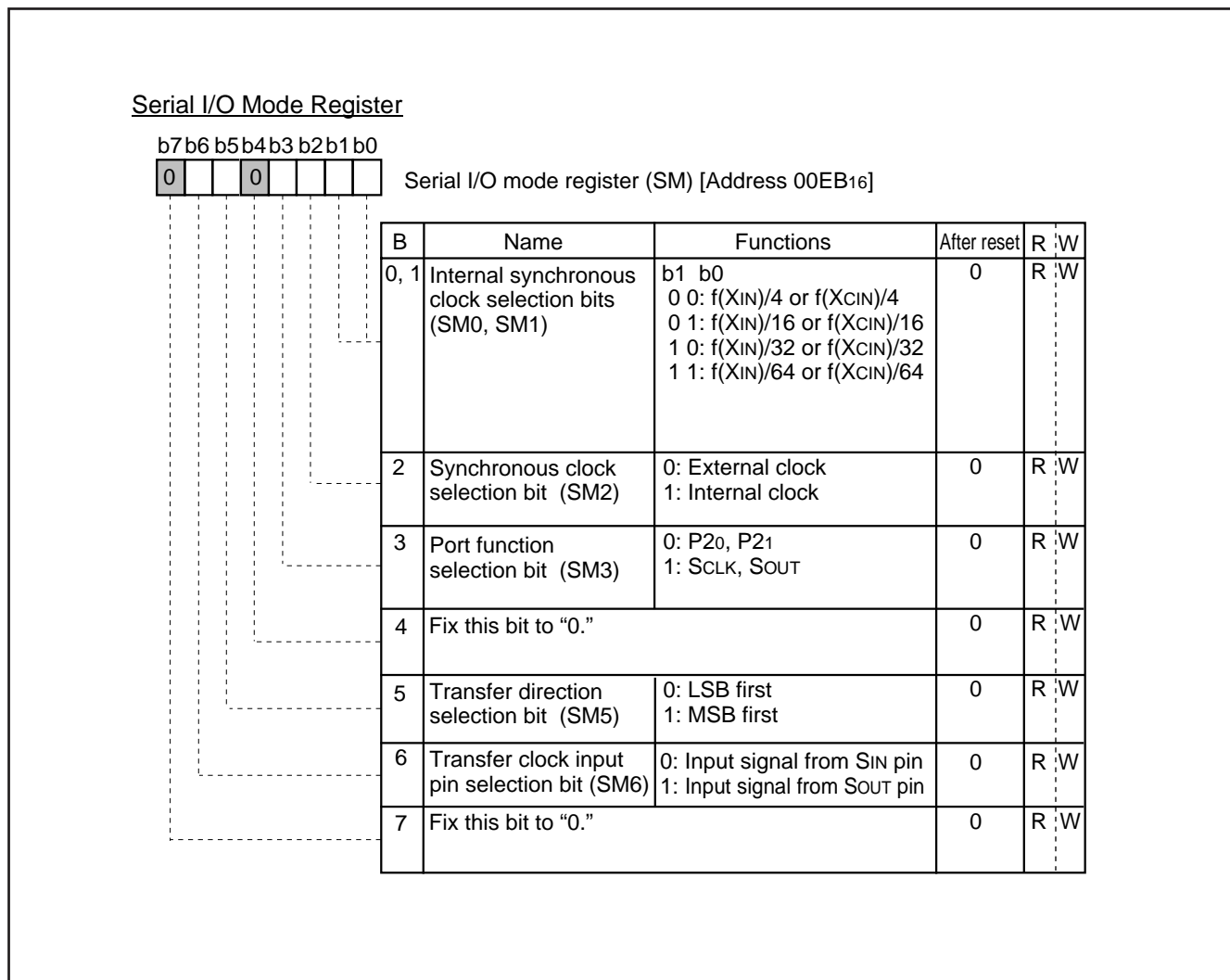


Fig. 8.5.3 Serial I/O Mode Register

### 8.6 MULTI-MASTER I<sup>2</sup>C-BUS INTERFACE

The multi-master I<sup>2</sup>C-BUS interface is a serial communications circuit, conforming to the Philips I<sup>2</sup>C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications. Figure 8.6.1 shows a block diagram of the multi-master I<sup>2</sup>C-BUS interface and Table 8.6.1 shows multi-master I<sup>2</sup>C-BUS interface functions.

This multi-master I<sup>2</sup>C-BUS interface consists of the I<sup>2</sup>C address register, the I<sup>2</sup>C data shift register, the I<sup>2</sup>C clock control register, the I<sup>2</sup>C control register, the I<sup>2</sup>C status register and other control circuits.

Table 8.6.1 Multi-master I<sup>2</sup>C-BUS Interface Functions

Item	Function
Format	In conformity with Philips I <sup>2</sup> C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I <sup>2</sup> C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at $\phi = 4$ MHz)

$\phi$  : System clock =  $f(XIN)/2$

**Note** : We are not responsible for any third party's infringement of patent rights or other rights attributable to the use of the control function (bits 6 and 7 of the I<sup>2</sup>C control register at address 00F916) for connections between the I<sup>2</sup>C-BUS interface and ports (SCL1, SCL2, SDA1, SDA2).

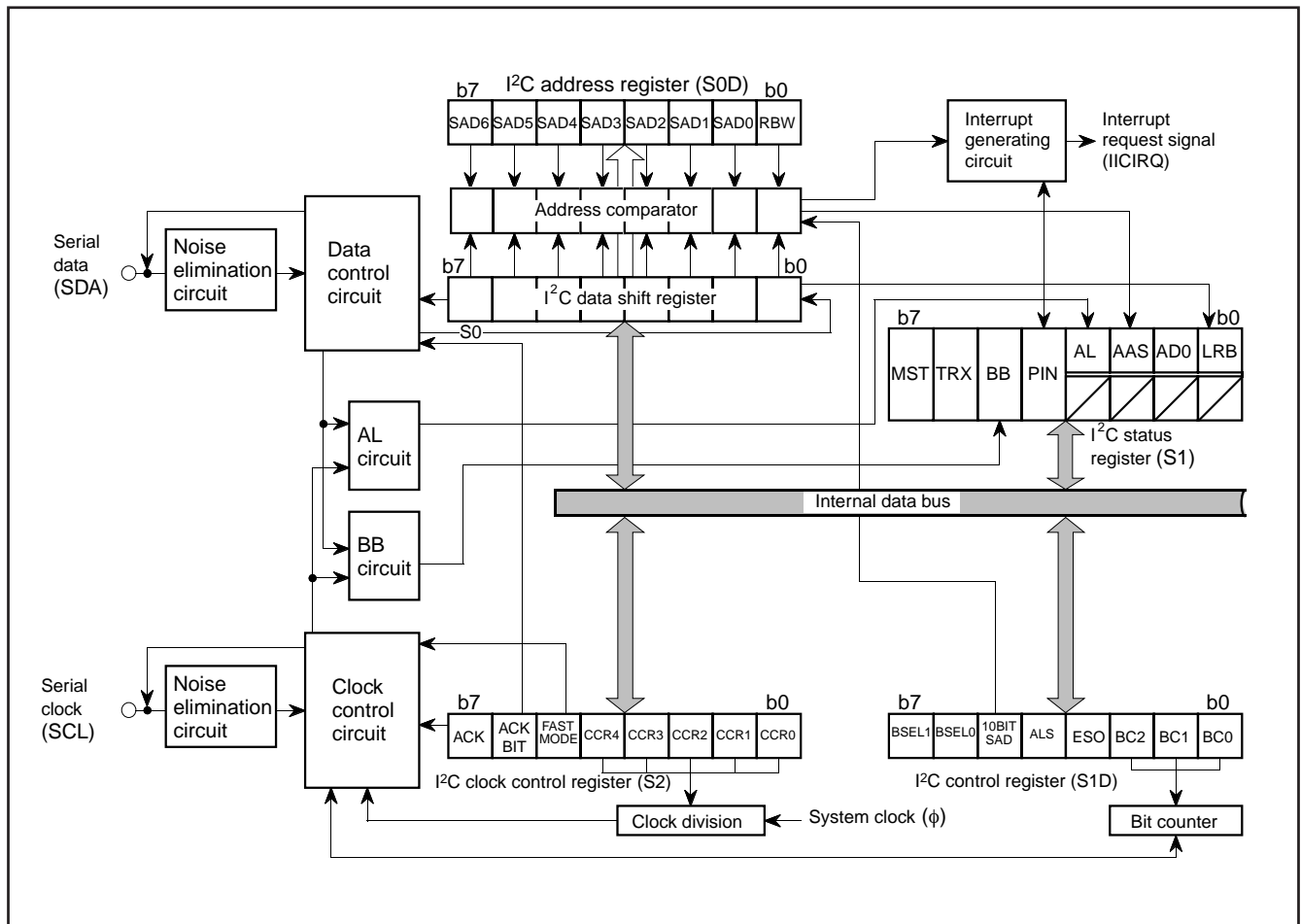


Fig. 8.6.1 Block Diagram of Multi-master I<sup>2</sup>C-BUS Interface

### 8.6.1 I<sup>2</sup>C Data Shift Register

The I<sup>2</sup>C data shift register (S0 : address 00F6<sub>16</sub>) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted one bit to the left.

The I<sup>2</sup>C data shift register is in a write enable status only when the ESO bit of the I<sup>2</sup>C control register (address 00F9<sub>16</sub>) is "1." The bit counter is reset by a write instruction to the I<sup>2</sup>C data shift register. When both the ESO bit and the MST bit of the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) are "1," the SCL is output by a write instruction to the I<sup>2</sup>C data shift register. Reading data from the I<sup>2</sup>C data shift register is always enabled regardless of the ESO bit value.

**Note:** To write data into the I<sup>2</sup>C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

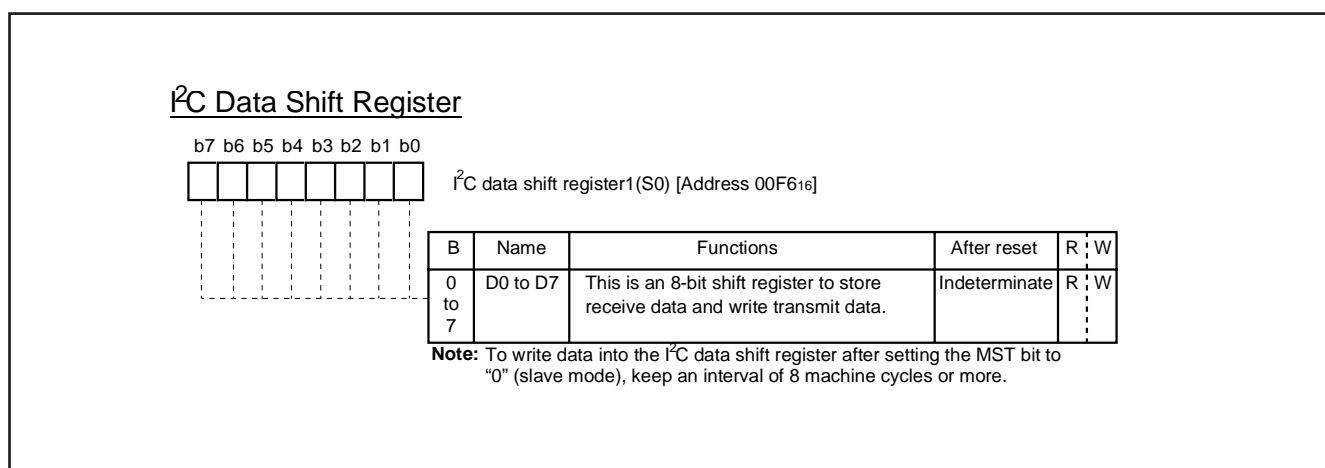


Fig. 8.6.2 Data Shift Register

### 8.6.2 I<sup>2</sup>C Address Register

The I<sup>2</sup>C address register (address 00F7<sub>16</sub>) consists of a 7-bit slave address and a read/write bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition are detected.

#### (1) Bit 0: read/write bit (RBW)

Not used when comparing addresses, in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD<sub>6</sub> to SAD<sub>0</sub> + RBW) of the I<sup>2</sup>C address register.

The RBW bit is cleared to "0" automatically when the stop condition is detected.

#### (2) Bits 1 to 7: slave address (SAD<sub>0</sub>–SAD<sub>6</sub>)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.

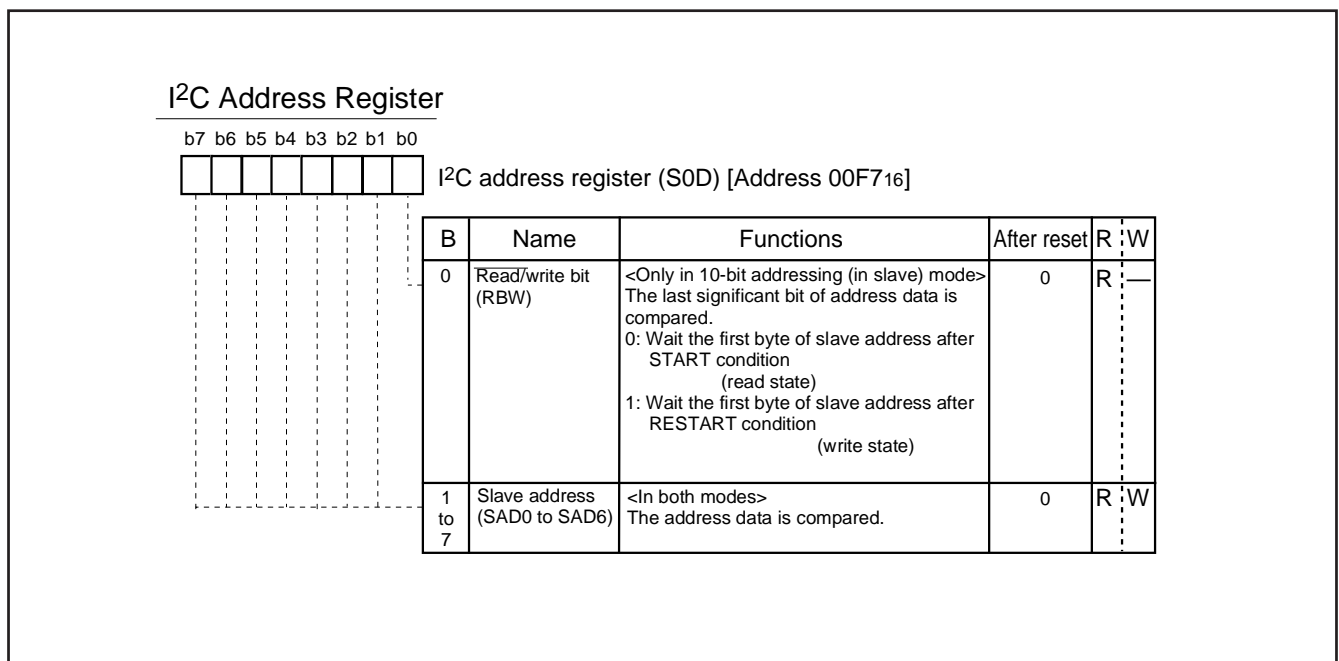


Fig. 8.6.3 I<sup>2</sup>C Address Register

### 8.6.3 I<sup>2</sup>C Clock Control Register

The I<sup>2</sup>C clock control register (address 00FA16) is used to set ACK control, SCL mode and SCL frequency.

#### (1) Bits 0 to 4: SCL frequency control bits (CCR0-CCR4)

These bits control the SCL frequency.

#### (2) Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to "0," the standard clock mode is set. When the bit is set to "1," the high-speed clock mode is set.

#### (3) Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock\* is generated. When this bit is set to "0," the ACK return mode is set and SDA goes to LOW at the occurrence of an ACK clock. When the bit is set to "1," the ACK non-return mode is set. The SDA is held in the HIGH status at the occurrence of an ACK clock.

However, when the slave address matches the address data in the reception of address data at ACK BIT = "0," the SDA is automatically made LOW (ACK is returned). If there is a mismatch between the slave address and the address data, the SDA is automatically made HIGH (ACK is not returned).

#### (4) Bit 7: ACK clock bit (ACK)

This bit specifies a mode of acknowledgment which is an acknowledgment response of data transmission. When this bit is set to "0," the no ACK clock mode is set. In this case, no ACK clock occurs after data transmission. When the bit is set to "1," the ACK clock mode is set and the master generates an ACK clock upon completion of each 1-byte data transmission. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (make SDA HIGH) and receives the ACK bit generated by the data receiving device.

**Note:** Do not write data into the I<sup>2</sup>C clock control register during transmission. If data is written during transmission, the I<sup>2</sup>C clock generator is reset, so that data cannot be transmitted normally.

\*ACK clock: Clock for acknowledgement

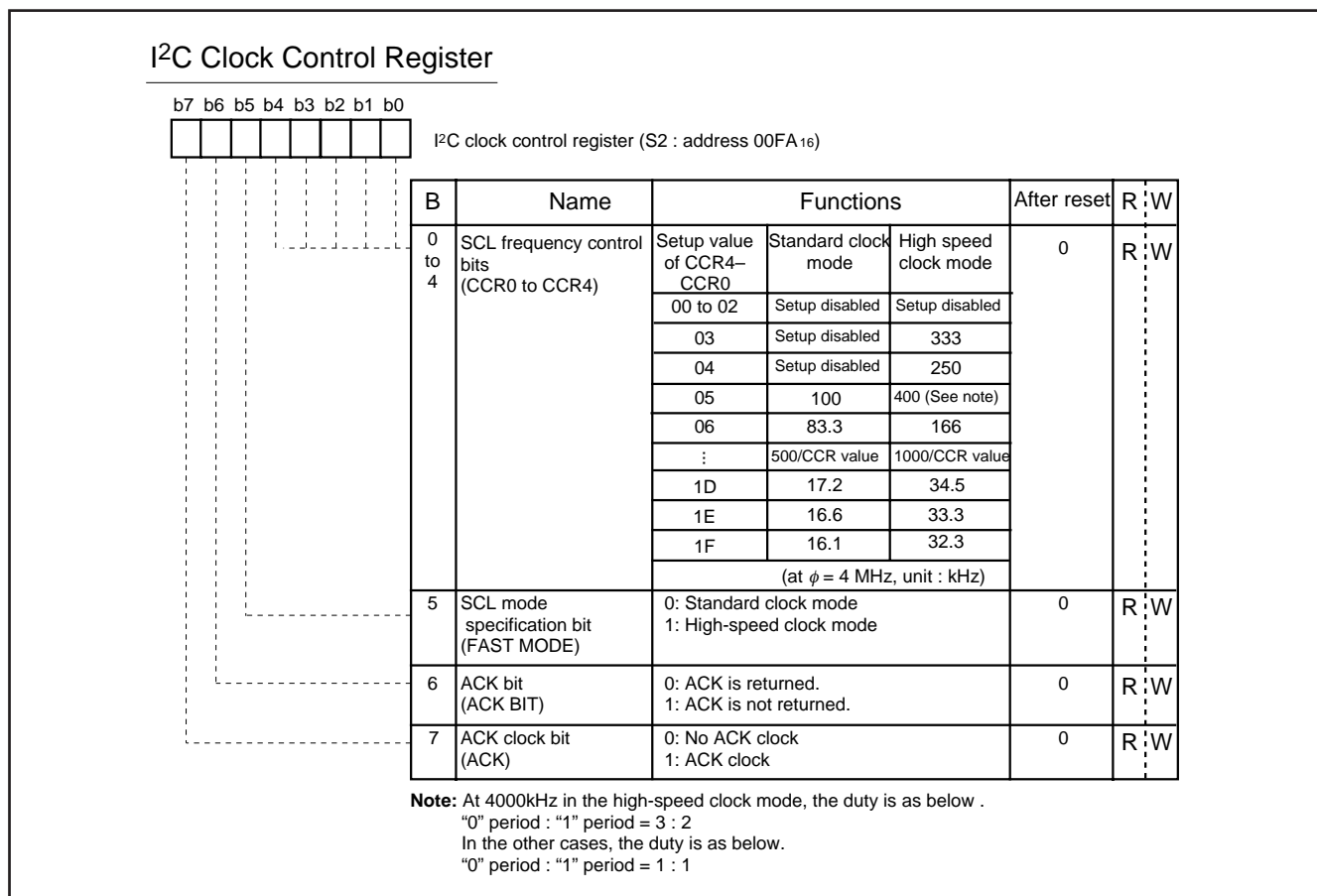


Fig. 8.6.4 I<sup>2</sup>C Address Register

### 8.6.4 I<sup>2</sup>C Control Register

The I<sup>2</sup>C control register (address 00F916) controls the data communication format.

#### (1) Bits 0 to 2: bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. An interrupt request signal occurs immediately after the number of bits specified with these bits are transmitted. When a START condition is received, these bits become “0002” and the address data is always transmitted and received in 8 bits.

#### (2) Bit 3: I<sup>2</sup>C interface use enable bit (ESO)

This bit enables usage of the multimaster I<sup>2</sup>C BUS interface. When this bit is set to “0,” the use disable status is provided, so the SDA and the SCL become high-impedance. When the bit is set to “1,” use of the interface is enabled.

When ESO = “0,” the following is performed.

- PIN = “1,” BB = “0” and AL = “0” are set (they are bits of the I<sup>2</sup>C status register at address 00F816).
- Writing data to the I<sup>2</sup>C data shift register (address 00F616) is disabled.

#### (3) Bit 4: data format selection bit (ALS)

This bit decides whether or not to recognize slave addresses. When this bit is set to “0,” the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to “8.6.5 I<sup>2</sup>C Status Register,” bit 1) is received, transmission processing can be performed. When this bit is set to “1,” the free data format is selected, so that slave addresses are not recognized.

#### (4) Bit 5: addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to “0,” the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I<sup>2</sup>C address register (address 00F716) are compared with address data. When this bit is set to “1,” the 10-bit addressing format is selected, all the bits of the I<sup>2</sup>C address register are compared with address data.

#### (5) Bits 6 and 7: connection control bits between I<sup>2</sup>C-BUS interface and ports (BSEL0, BSEL1)

These bits control the connection between SCL and ports or SDA and ports (refer to Figure 8.6.5).

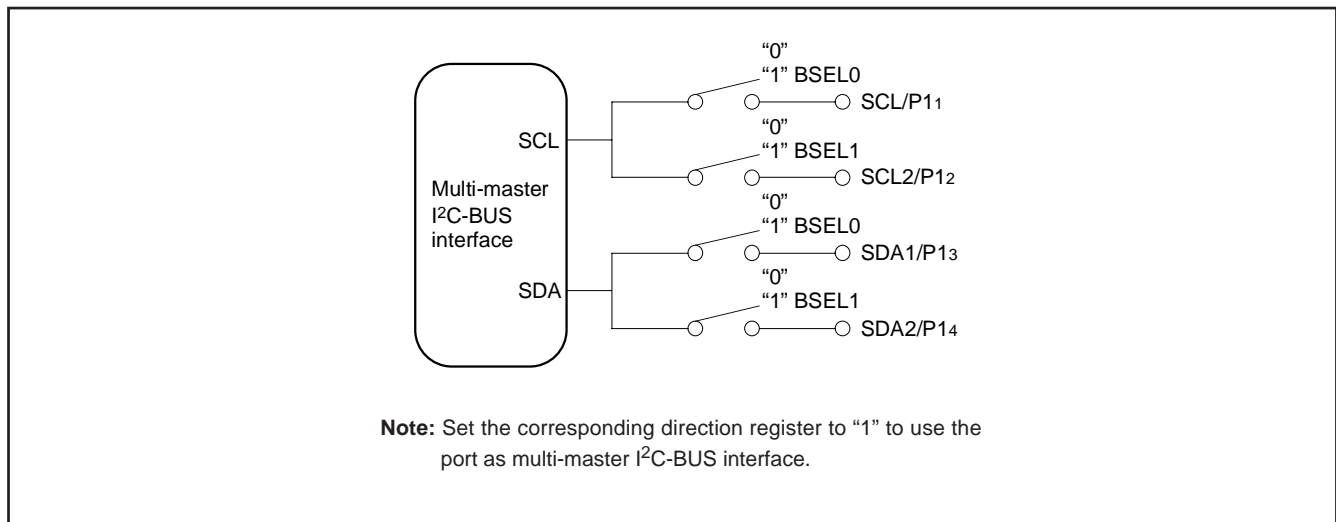
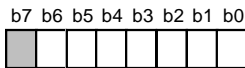


Fig. 8.6.5 Connection Port Control by BSEL0 and BSEL1



### I<sup>2</sup>C Control Register



I<sup>2</sup>C control register (S1D address 00F9<sub>16</sub>)

B	Name	Functions	After reset	R : W
0 to 2	Bit counter (Number of transmit/recieve bits) (BC0 to BC2)	b2 b1 b0 0 0 0 : 8 0 0 1 : 7 0 1 0 : 6 0 1 1 : 5 1 0 0 : 4 1 0 1 : 3 1 1 0 : 2 1 1 1 : 1	0	R : W
3	I <sup>2</sup> C-BUS interface use enable bit (ESO)	0 : Disabled 1 : Enabled	0	R : W
4	Data format selection bit(ALS)	0 : Addressing mode 1 : Free data format	0	R : W
5	Addressing format selection bit (10BIT SAD)	0 : 7-bit addressing format 1 : 10-bit addressing format	0	R : W
6, 7	Connection control bits between I <sup>2</sup> C-BUS interface and ports	b7 b6 Connection port (See note) 0 0 : None 0 1 : SCL1, SDA1 1 0 : SCL2, SDA2 1 1 : SCL1, SDA1 SCL2, SDA2	0	R : W

**Note:** When using ports P11-P14 as I<sup>2</sup>C-BUS interface, the output structure changes automatically from CMOS output to N-channel open-drain output.

Fig. 8.6.6 I<sup>2</sup>C Control Register

## 8.6.5 I<sup>2</sup>C Status Register

The I<sup>2</sup>C status register (address 00F816) controls the I<sup>2</sup>C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

### (1) Bit 0: last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I<sup>2</sup>C data shift register (address 00F616).

### (2) Bit 1: general call detecting flag (AD0)

This bit is set to "1" when a general call\* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition.

\*General call: The master transmits the general call address "0016" to all slaves.

### (3) Bit 2: slave address comparison flag (AAS)

This flag indicates a comparison result of address data.

- In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions.
  - The address data immediately after occurrence of a START condition matches the slave address stored in the high-order 7 bits of the I<sup>2</sup>C address register (address 00F716).
  - A general call is received.
- In the slave reception mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition.
  - When the address data is compared with the I<sup>2</sup>C address register (8 bits consists of slave address and RBW), the first bytes match.
- The state of this bit is changed from "1" to "0" by executing a write instruction to the I<sup>2</sup>C data shift register (address 00F616).

### (4) Bit 3: arbitration lost\* detecting flag (AL)

In the master transmission mode, when a device other than the microcomputer sets the SDA to "L", arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to receive and recognize its own slave address transmitted by another master device.

\*Arbitration lost: The status in which communication as a master is disabled.

### (5) Bit 4: I<sup>2</sup>C-BUS interface interrupt request bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the state of the PIN bit changes from "1" to "0." At the same time, an interrupt request signal is sent to the CPU. The PIN bit is set to "0" in synchronization with a falling edge of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling edge of the PIN bit. When detecting the STOP condition in slave, the multi-master I<sup>2</sup>C-BUS interface interrupt request bit (IR) is set "0" to "1" (interrupt request) regardless of falling of PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 8.6.8 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in any one of the following conditions.

- Writing "1" to the PIN bit
- Executing a write instruction to the I<sup>2</sup>C data shift register (address 00F616). (See note)
- When the ESO bit is "0"
- At reset

**Note:** It takes 8 BCLK cycles or more until PIN bit become "1" after write instructions are executed to these registers.

The conditions in which the PIN bit is set to "0" are shown below:

- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

### (6) Bit 5: bus busy flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. When this bit is set to "1," this bus system is busy and the occurrence of a START condition is disabled by the START condition duplication prevention function (See note).

This flag can be written by software only in the master transmission mode. In the other modes, this bit is set to "1" by detecting a START condition and set to "0" by detecting a STOP condition. When the ESO bit of the I<sup>2</sup>C control register (address 00F916) is "0" and at reset, the BB flag is kept in the "0" state.

### (7) Bit 6: communication mode specification bit (transfer direction specification bit: TRX)

This bit decides the direction of transfer for data communication. When this bit is "0," the reception mode is selected and the data of a transmitting device is received. When the bit is "1," the transmission mode is selected and address data and control data are output into the SDA in synchronization with the clock generated on the SCL.

When the ALS bit of the I<sup>2</sup>C control register (address 00F916) is "0" in the slave reception mode is selected, the TRX bit is set to "1" (transmit) if the least significant bit (R/W bit) of the address data transmitted by the master is "1." When the ALS bit is "0" and the R/W bit is "0," the TRX bit is cleared to "0" (receive).

The TRX bit is cleared to "0" in one of the following conditions.

- When arbitration lost is detected.
- When a STOP condition is detected.
- When occurrence of a START condition is disabled by the START condition duplication prevention function (Note).
- With MST = "0" and when a START condition is detected.
- With MST = "0" and when ACK non-return is detected.
- At reset

### (8) Bit 7: Communication mode specification bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is “0,” the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is “1,” the master is specified and a START condition and a STOP condition are generated, and also the clocks required for data communication are generated on the SCL.

The MST bit is cleared to “0” in one of the following conditions.

- Immediately after completion of 1-byte data transmission when arbitration lost is detected
- When a STOP condition is detected.
- When occurrence of a START condition is disabled by the START condition duplication preventing function (Note).
- At reset

**Note:** The START condition duplication prevention function disables the START condition generation, reset of bit counter reset, and SCL output, when the following condition is satisfied:  
a START condition is set by another master device.

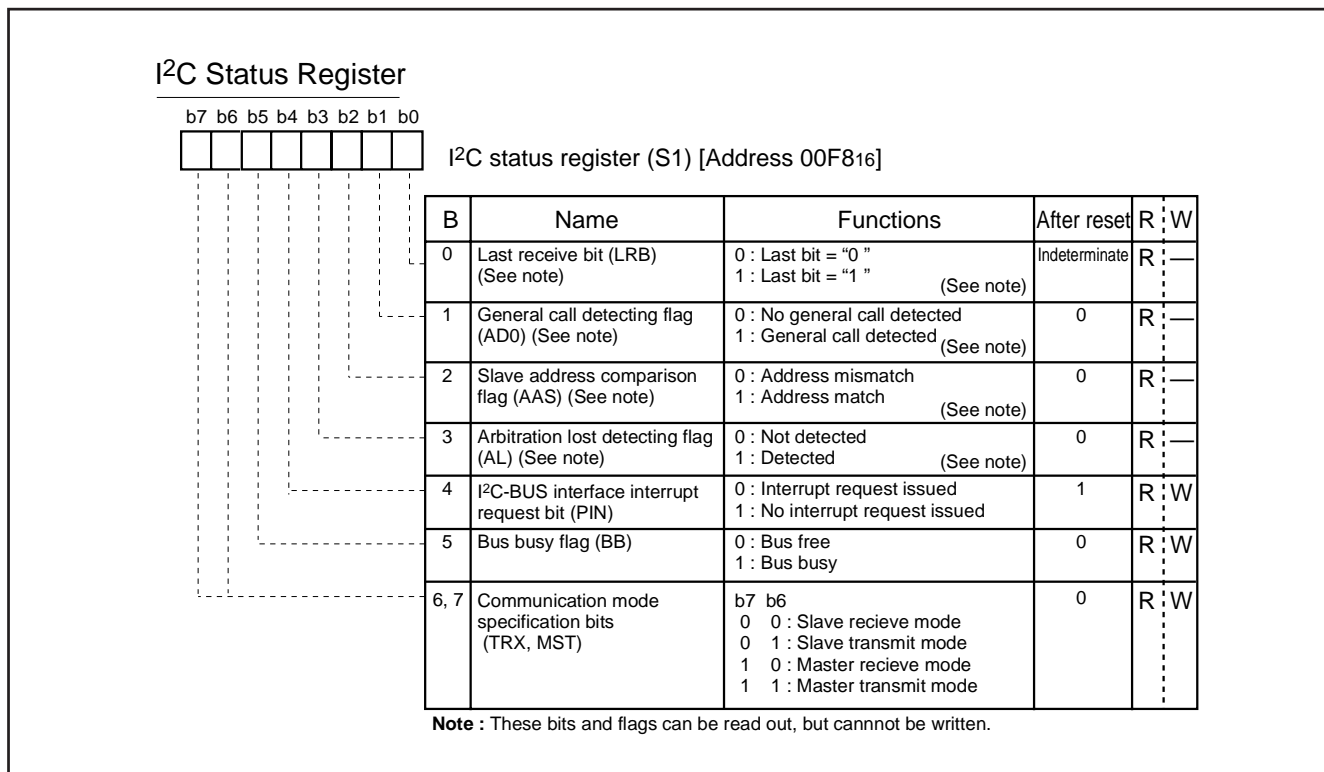


Fig. 8.6.7 I<sup>2</sup>C Status Register

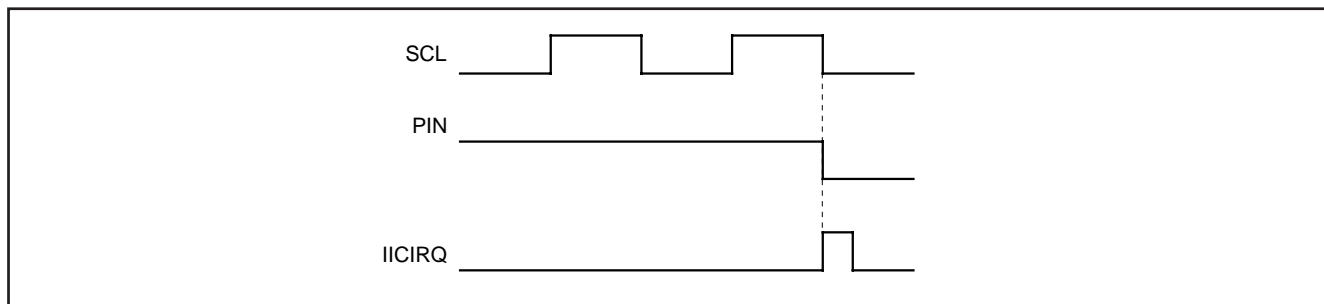


Fig. 8.6.8 Interrupt Request Signal Generation Timing

### 8.6.6 START Condition Generation Method

When the ESO bit of the I<sup>2</sup>C control register (address 00F9<sub>16</sub>) is “1,” execute a write instruction to the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) to set the MST, TRX and BB bits to “1.” A START condition will then be generated. After that, the bit counter becomes “000<sub>2</sub>” and an SCL for 1 byte is output. The START condition generation timing and BB bit set timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 8.6.9 for the START condition generation timing diagram, and Table 8.6.2 for the START condition/STOP condition generation timing table.

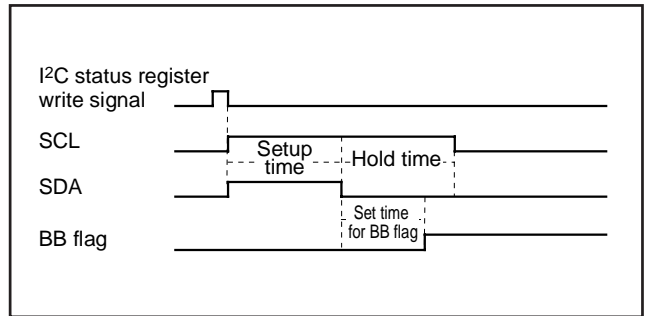


Fig. 8.6.9 START Condition Generation Timing Diagram

### 8.6.7 STOP Condition Generation Method

When the ESO bit of the I<sup>2</sup>C control register (address 00F9<sub>16</sub>) is “1,” execute a write instruction to the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) for setting the MST bit and the TRX bit to “1” and the BB bit to “0.” A STOP condition will then be generated. The STOP condition generation timing and the BB flag reset timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 8.6.10 for the STOP condition generation timing diagram, and Table 8.6.2 for the START condition/STOP condition generation timing table.

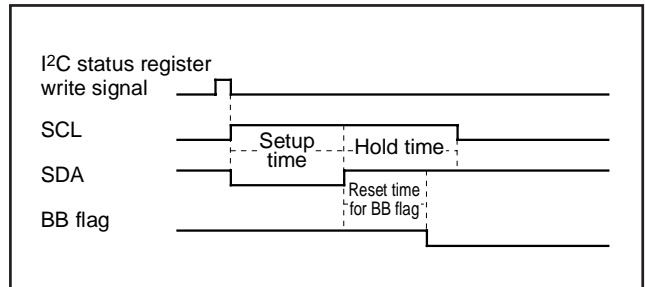


Fig. 8.6.10 STOP Condition Generation Timing Diagram

Table 8.6.2 START Condition/STOP Condition Generation Timing Table

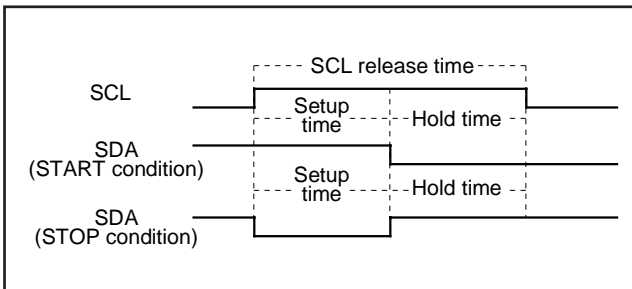
Item	Standard Clock Mode	High-speed Clock Mode
Setup time (START condition)	5.0 μs (20 cycles)	2.5 μs (10 cycles)
Setup time (STOP condition)	4.25 μs (17 cycles)	1.75 μs (7 cycles)
Hold time	5.0 μs (20 cycles)	2.5 μs (10 cycles)
Set/reset time for BB flag	3.0 μs (12 cycles)	1.5 μs (6 cycles)

Note: Absolute time at φ = 4 MHz. The value in parentheses denotes the number of φ cycles.

### 8.6.8 START/STOP Condition Detect Conditions

The START/STOP condition detect conditions are shown in Figure 8.6.11 and Table 8.6.3. Only when the 3 conditions of Table 8.6.3 are satisfied, a START/STOP condition can be detected.

**Note:** When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "IICIRQ" is generated to the CPU.



**Fig. 8.6.11 START Condition/STOP Condition Detect Timing Diagram**

**Table 8.6.3 START Condition/STOP Condition Detect Conditions**

Standard Clock Mode	High-speed Clock Mode
6.5 μs (26 cycles) < SCL release time	1.0 μs (4 cycles) < SCL release time
3.25 μs (13 cycles) < Setup time	0.5 μs (2 cycles) < Setup time
3.25 μs (13 cycles) < Hold time	0.5 μs (2 cycles) < Hold time

**Note:** Absolute time at φ = 4 MHz. The value in parentheses denotes the number of φ cycles.

### 8.6.9 Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats is described below.

#### (1) 7-bit addressing format

To meet the 7-bit addressing format, set the 10BIT SAD bit of the I<sup>2</sup>C control register (address 00F9<sub>16</sub>) to "0." The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I<sup>2</sup>C address register (address 00F7<sub>16</sub>). At the time of this comparison, address comparison of the RBW bit of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>) is not made. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 8.6.12, (1) and (2).

#### (2) 10-bit addressing format

To meet the 10-bit addressing format, set the 10BIT SAD bit of the I<sup>2</sup>C control register (address 00F9<sub>16</sub>) to "1." An address comparison is made between the first-byte address data transmitted from the master and the 7-bit slave address stored in the I<sup>2</sup>C address register (address 00F7<sub>16</sub>). At the time of this comparison, an address comparison between the RBW bit of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>) and the R/W bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the R/W bit which is the last bit of the address data not only specifies the direction of communication for control data but also is processed as an address data bit.

When the first-byte address data matches the slave address, the AAS bit of the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) is set to "1." After the second-byte address data is stored into the I<sup>2</sup>C data shift register (address 00F6<sub>16</sub>), make an address comparison between the second-byte data and the slave address by software. When the address data of the 2nd bytes matches the slave address, set the RBW bit of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>) to "1" by software. This processing can match the 7-bit slave address and R/W data, which are received after a RESTART condition is detected, with the value of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 8.6.12, (3) and (4).

### 8.6.10 Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

- ① Set a slave address in the high-order 7 bits of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>) and “0” in the RBW bit.
- ② Set the ACK return mode and SCL = 100 kHz by setting “85<sub>16</sub>” in the I<sup>2</sup>C clock control register (address 00FA<sub>16</sub>).
- ③ Set “10<sub>16</sub>” in the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) and hold the SCL at the HIGH.
- ④ Set a communication enable status by setting “48<sub>16</sub>” in the I<sup>2</sup>C control register (address 00F9<sub>16</sub>).
- ⑤ Set the address data of the destination of transmission in the high-order 7 bits of the I<sup>2</sup>C data shift register (address 00F6<sub>16</sub>) and set “0” in the least significant bit.
- ⑥ Set “F0<sub>16</sub>” in the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occurs.
- ⑦ Set transmit data in the I<sup>2</sup>C data shift register (address 00F6<sub>16</sub>). At this time, an SCL and an ACK clock automatically occurs.
- ⑧ When transmitting control data of more than 1 byte, repeat step ⑦.
- ⑨ Set “D0<sub>16</sub>” in the I<sup>2</sup>C status register (address 00F8<sub>16</sub>). After this, if ACK is not returned or transmission ends, a STOP condition will be generated.

### 8.6.11 Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode, using the addressing format, is shown below.

- ① Set a slave address in the high-order 7 bits of the I<sup>2</sup>C address register (address 00F7<sub>16</sub>) and “0” in the RBW bit.
- ② Set the no ACK clock mode and SCL = 400 kHz by setting “25<sub>16</sub>” in the I<sup>2</sup>C clock control register (address 00FA<sub>16</sub>).
- ③ Set “10<sub>16</sub>” in the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) and hold the SCL at the HIGH.
- ④ Set a communication enable status by setting “48<sub>16</sub>” in the I<sup>2</sup>C control register (address 00F9<sub>16</sub>).
- ⑤ When a START condition is received, an address comparison is made.
- ⑥ •When all transmitted address are “0” (general call):  
 ADO of the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) is set to “1” and an interrupt request signal occurs.  
 •When the transmitted addresses match the address set in ①:  
 ASS of the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) is set to “1” and an interrupt request signal occurs.  
 •In the cases other than the above:  
 ADO and AAS of the I<sup>2</sup>C status register (address 00F8<sub>16</sub>) are set to “0” and no interrupt request signal occurs.
- ⑦ Set dummy data in the I<sup>2</sup>C data shift register (address 00F6<sub>16</sub>).
- ⑧ When receiving control data of more than 1 byte, repeat step ⑦.
- ⑨ When a STOP condition is detected, the communication ends.

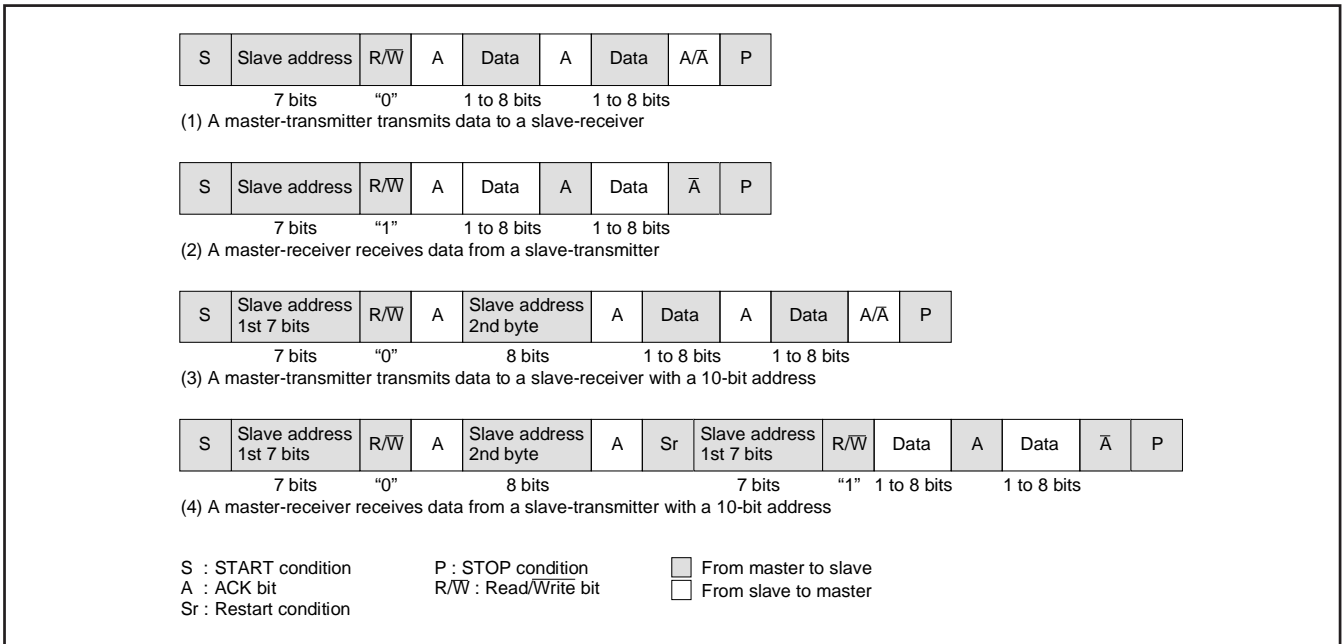


Fig. 8.6.12 Address Data Communication Format

### 8.6.12 Precautions when using multi-master I<sup>2</sup>C-BUS interface

#### (1) Read-modify-write instruction

The precautions when the read-modify-write instruction such as SEB, CLB etc. is executed for each register of the multi-master I<sup>2</sup>C-BUS interface are described below.

- I<sup>2</sup>C data shift register (S0)  
When executing the read-modify-write instruction for this register during transfer, data may become a value not intended.
- I<sup>2</sup>C address register (S0D)  
When the read-modify-write instruction is executed for this register at detecting the STOP condition, data may become a value not intended. It is because hardware changes the read/write bit (RBW) at the above timing.
- I<sup>2</sup>C status register (S1)  
Do not execute the read-modify-write instruction for this register because all bits of this register are changed by hardware.
- I<sup>2</sup>C control register (S1D)  
When the read-modify-write instruction is executed for this register at detecting the START condition or at completing the byte transfer, data may become a value not intended. Because hardware changes the bit counter (BC0-BC2) at the above timing.
- I<sup>2</sup>C clock control register (S2)  
The read-modify-write instruction can be executed for this register.

#### (2) START condition generating procedure using multi-master

①Procedure example (The necessary conditions of the generating procedure are described as the following ② to ⑤).

```

•
•
LDA    —                (Taking out of slave address value)
SEI    (Interrupt disabled)
BBS    5,S1,BUSBUSY    (BB flag confirming and branch process)
BUSFREE:
STA    S0                (Writing of slave address value)
LDM    #$F0, S1        (Trigger of START condition generating)
CLI    (Interrupt enabled)
•
•
BUSBUSY:
CLI    (Interrupt enabled)
•
•

```

- ②Use "STA," "STX" or "STY" of the zero page addressing instruction for writing the slave address value to the I<sup>2</sup>C data shift register.
- ③Use "LDM" instruction for setting trigger of START condition generating.
- ④Write the slave address value of above ② and set trigger of START condition generating of above ③ continuously shown the above procedure example.
- ⑤Disable interrupts during the following three process steps:
  - BB flag confirming
  - Writing of slave address value
  - Trigger of START condition generating
When the condition of the BB flag is bus busy, enable interrupts immediately.

### (3) RESTART condition generating procedure

① Procedure example (The necessary conditions of the generating procedure are described as the following ② to ⑥.)

Execute the following procedure when the PIN bit is "0."

```

      •
      •
LDM  #$00, S1    (Select slave receive mode)
LDA  —           (Taking out of slave address value)
SEI  —           (Interrupt disabled)
STA  S0          (Writing of slave address value)
LDM  #$F0, S1   (Trigger of RESTART condition generating)
CLI  —           (Interrupt enabled)
      •
      •

```

② Select the slave receive mode when the PIN bit is "0." Do not write "1" to the PIN bit. Neither "0" nor "1" is specified for the writing to the BB bit.

The TRX bit becomes "0" and the SDA pin is released.

③ The SCL pin is released by writing the slave address value to the I<sup>2</sup>C data shift register. Use "STA," "STX" or "STY" of the zero page addressing instruction for writing.

④ Use "LDM" instruction for setting trigger of RESTART condition generating.

⑤ Write the slave address value of above ③ and set trigger of RESTART condition generating of above ④ continuously shown the above procedure example.

⑥ Disable interrupts during the following two process steps:

- Writing of slave address value
- Trigger of RESTART condition generating

### (4) STOP condition generating procedure

① Procedure example (The necessary conditions of the generating procedure are described as the following ② to ④.)

```

      •
      •
SEI  —           (Interrupt disabled)
LDM  #$C0, S1   (Select master transmit mode)
NOP  —           (Set NOP)
LDM  #$D0, S1   (Trigger of STOP condition generating)
CLI  —           (Interrupt enabled)
      •
      •

```

② Write "0" to the PIN bit when master transmit mode is select.

③ Execute "NOP" instruction after setting of master transmit mode.

Also, set trigger of STOP condition generating within 10 cycles after selecting of master transmit mode.

④ Disable interrupts during the following two process steps:

- Select of master transmit mode
- Trigger of STOP condition generating

### (5) Writing to I<sup>2</sup>C status register

Do not execute an instruction to set the PIN bit to "1" from "0" and an instruction to set the MST and TRX bits to "0" from "1" simultaneously. It is because it may enter the state that the SCL pin is released and the SDA pin is released after about one machine cycle. Do not execute an instruction to set the MST and TRX bits to "0" from "1" simultaneously when the PIN bit is "1." It is because it may become the same as above.

### (6) Process of after STOP condition generating

Do not write data in the I<sup>2</sup>C data shift register S0 and the I<sup>2</sup>C status register S1 until the bus busy flag BB becomes "0" after generating the STOP condition in the master mode. It is because the STOP condition waveform might not be normally generated. Reading to the above registers do not have the problem.



## 8.7 PWM OUTPUT FUNCTION

This microcomputer is equipped with six 8-bit PWMs (PWM0–PWM5). PWM0–PWM5 have the same circuit structure and an 8-bit resolution with minimum resolution bit width of  $4 \mu\text{s}$  (for  $f(\text{XIN}) = 8 \text{ MHz}$ ) and repeat period of  $1024 \mu\text{s}$  (for  $f(\text{XIN}) = 8 \text{ MHz}$ ).

Figure 8.7.1 shows the PWM block diagram. The PWM timing generating circuit applies individual control signals to PWM0–PWM5 using  $f(\text{XIN})$  divided by 2 as a reference signal.

### 8.7.1 Data Setting

When outputting PWM0–PWM5, set 8-bit output data to the PWM $i$  register ( $i$  means 0 to 5; addresses 020016 to 020516).

### 8.7.2 Transmitting Data from Register to PWM circuit

Data transfer from the 8-bit PWM register to the 8-bit PWM circuit is executed at writing data to the register.

The signal output from the 8-bit PWM output pin corresponds to the contents of this register.

### 8.7.3 Operating of 8-bit PWM

The following explains PWM operation.

First, set the bit 0 of PWM mode register 1 (address 020816) to “0” (at reset, bit 0 is already set to “0” automatically), so that the PWM count source is supplied.

PWM0–PWM5 are also used as pins P00–P05. Set the corresponding bits of the port P0 direction register to “1” (output mode). And select each output polarity by bit 3 of PWM mode register 1 (address 020816). Then, set bits 5 to 0 of PWM mode register 2 (address 020916) to “1” (PWM output).

The PWM waveform is output from the PWM output pins by setting these registers.

Figure 17 shows the 8-bit PWM timing. One cycle ( $T$ ) is composed of 256 ( $2^8$ ) segments. The 8 kinds of pulses relative to the weight of each bit (bits 0 to 7), are output inside the circuit during 1 cycle. Refer to Figure 17 (a). The 8-bit PWM outputs waveform which is the logical sum (OR) of pulses corresponding to the contents of bits 0 to 7 of the 8-bit PWM register. Several examples are shown in Figure 17 (b). 256 kinds of output (HIGH area: 0/256 to 255/256) are selected by changing the contents of the PWM register. A length of entirely HIGH cannot be output, i.e. 256/256.

### 8.7.4 Output after Reset

At reset, the output of ports P00–P05 is in the high-impedance state, and the contents of the PWM register and the PWM circuit are undefined. Note that after reset, the PWM output is undefined until setting the PWM register.

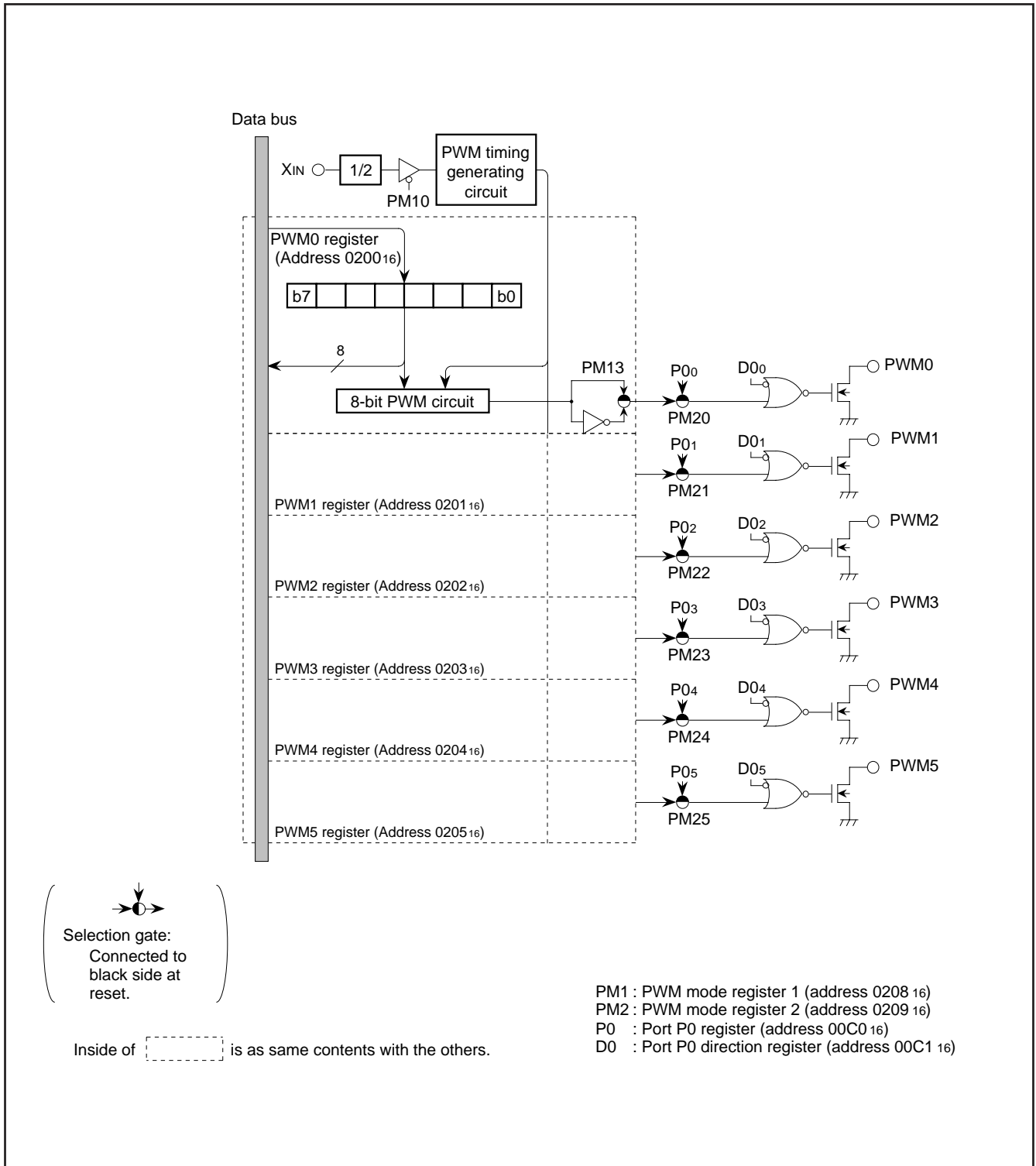


Fig. 8.7.1 PWM Block Diagram

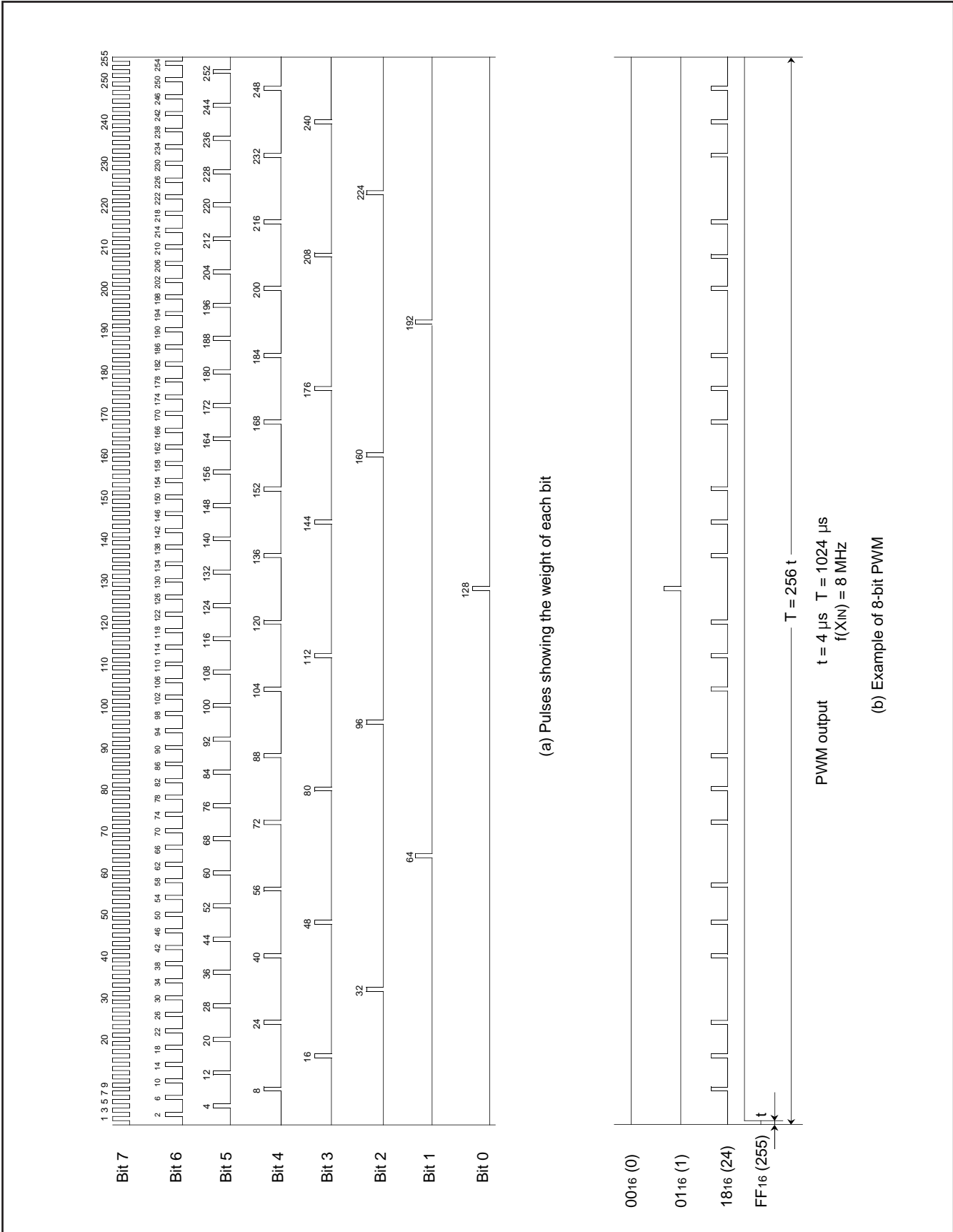


Fig. 8.7.2 PWM Timing

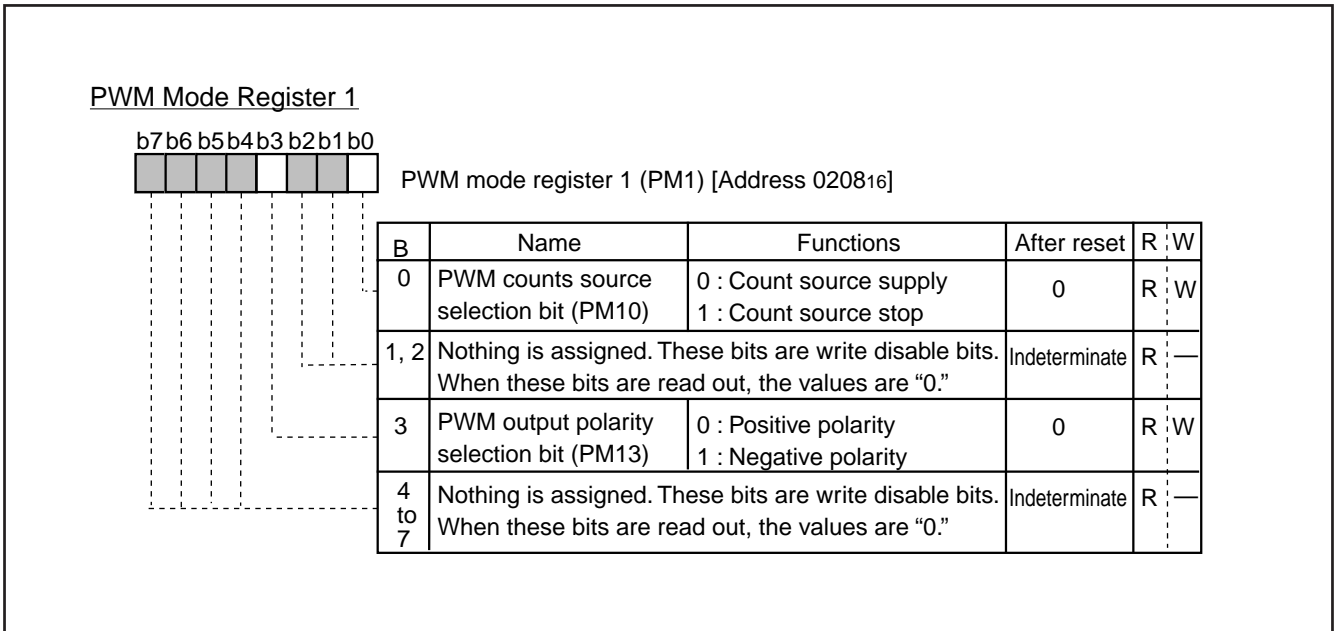


Fig. 8.7.3 PWM Mode Register 1

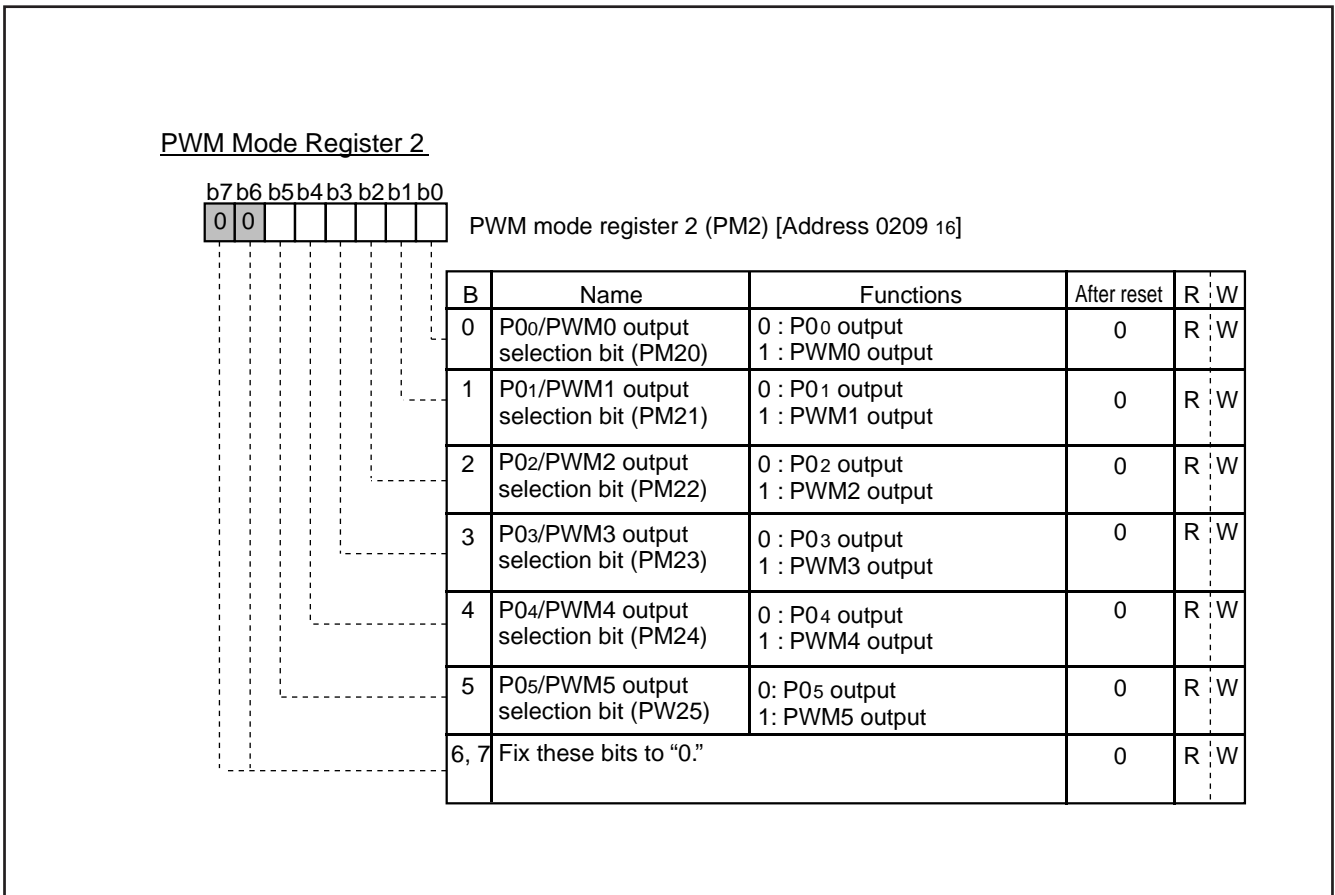


Fig. 8.7.4 PWM Mode Register 2

## 8.8 A-D COMPARATOR

A-D comparator consists of 6-bit D-A converter and comparator. A-D comparator block diagram is shown in Figure 8.8.1.

The reference voltage "V<sub>ref</sub>" for D-A conversion is set by bits 0 to 5 of A-D control register 2 (address 00ED16).

The comparison result of the analog input voltage and the reference voltage "V<sub>ref</sub>" is stored in bit 4 of A-D control register 1 (address 00EC16).

For A-D comparison, set "0" to corresponding bits of the direction register to use ports as analog input pins. Write the data for select of analog input pins to bits 0 to 2 of A-D control register 1 and write the digital value corresponding to V<sub>ref</sub> to be compared to the bits 0 to 5 of A-D control register 2. The voltage comparison starts by writing to A-D control register 2, and it is completed after 16 machine cycles (NOP instruction X 8).

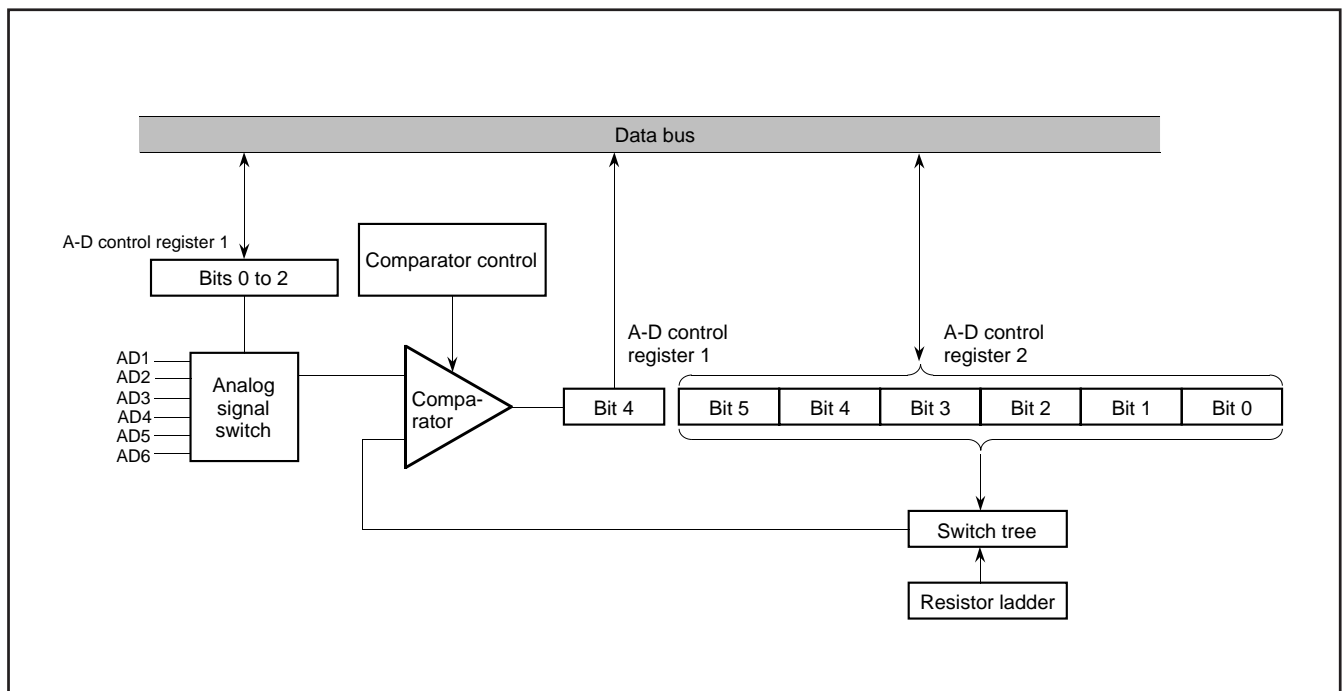


Fig. 8.8.1 A-D Comparator Block Diagram

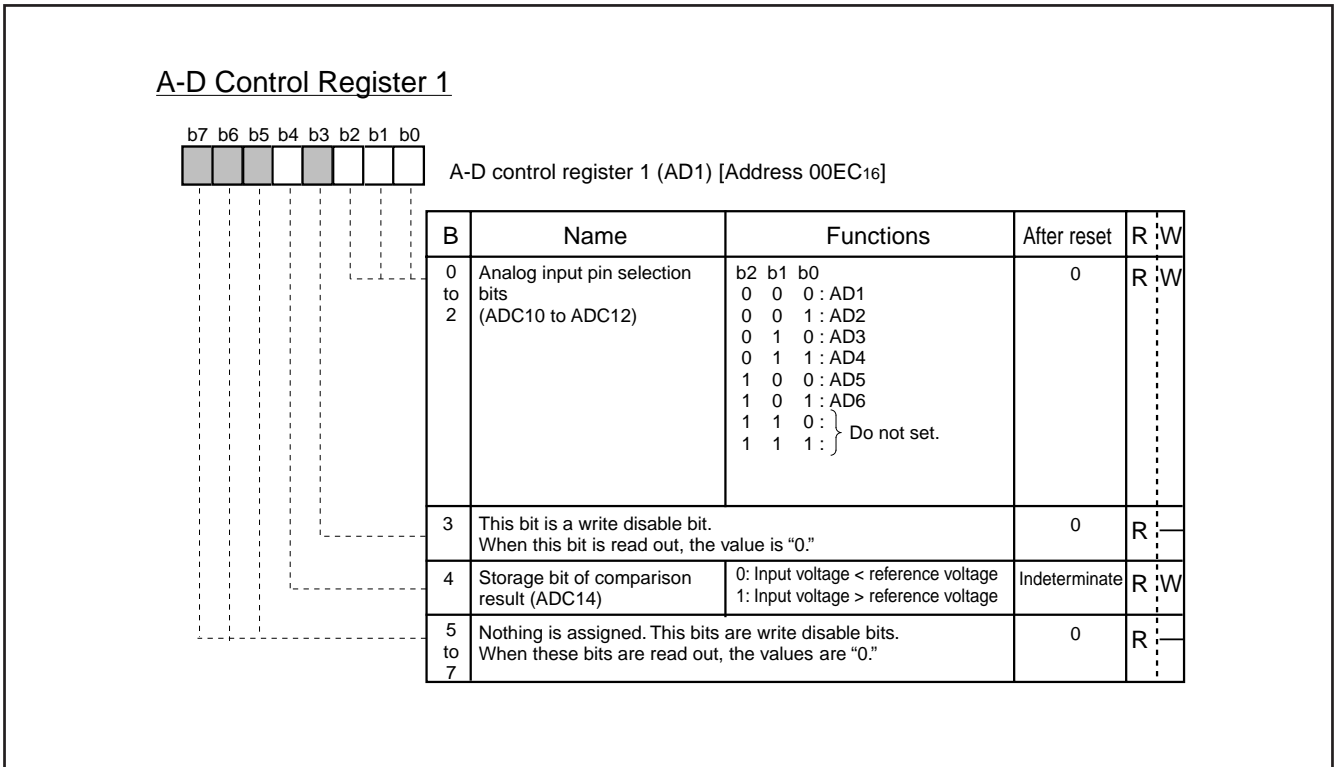


Fig. 8.8.2 A-D Control Register 1

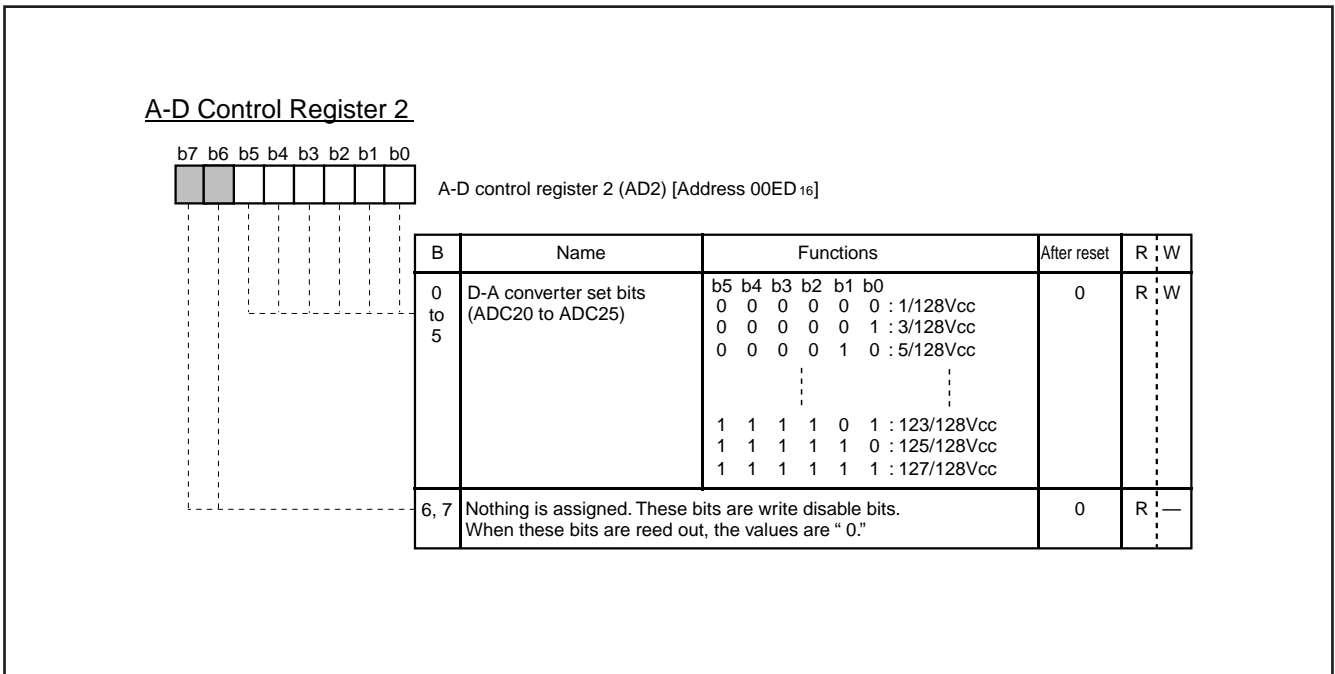


Fig. 8.8.3 A-D Control Register 2

### 8.9 ROM CORRECTION FUNCTION

This can correct program data in ROM. Up to 2 addresses can be corrected, a program for correction is stored in the ROM correction vector in RAM as the top address. The ROM correction vectors are 2 vectors.

Vector 1 : address 0300<sub>16</sub>

Vector 2 : address 0320<sub>16</sub>

Set the address of the ROM data to be corrected into the ROM correction address register. When the value of the counter matches the ROM data address in the ROM correction vector as the top address, the main program branches to the correction program stored in the ROM memory for correction. To return from the correction program to the main program, the op code and operand of the JMP instruction (total of 3 bytes) are necessary at the end of the correction program. The ROM correction function is controlled by the ROM correction enable register.

- Notes 1:** Specify the first address (op code address) of each instruction as the ROM correction address.  
**2:** Use the JMP instruction (total of 3 bytes) to return from the correction program to the main program.  
**3:** Do not set the same ROM correction address to vectors 1 and 2.

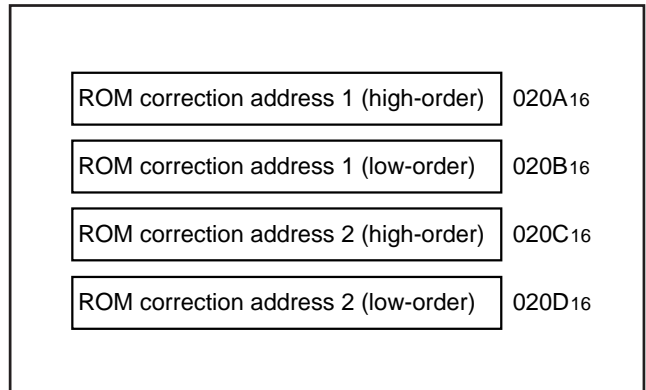


Fig. 8.9.1 ROM Correction Address Registers

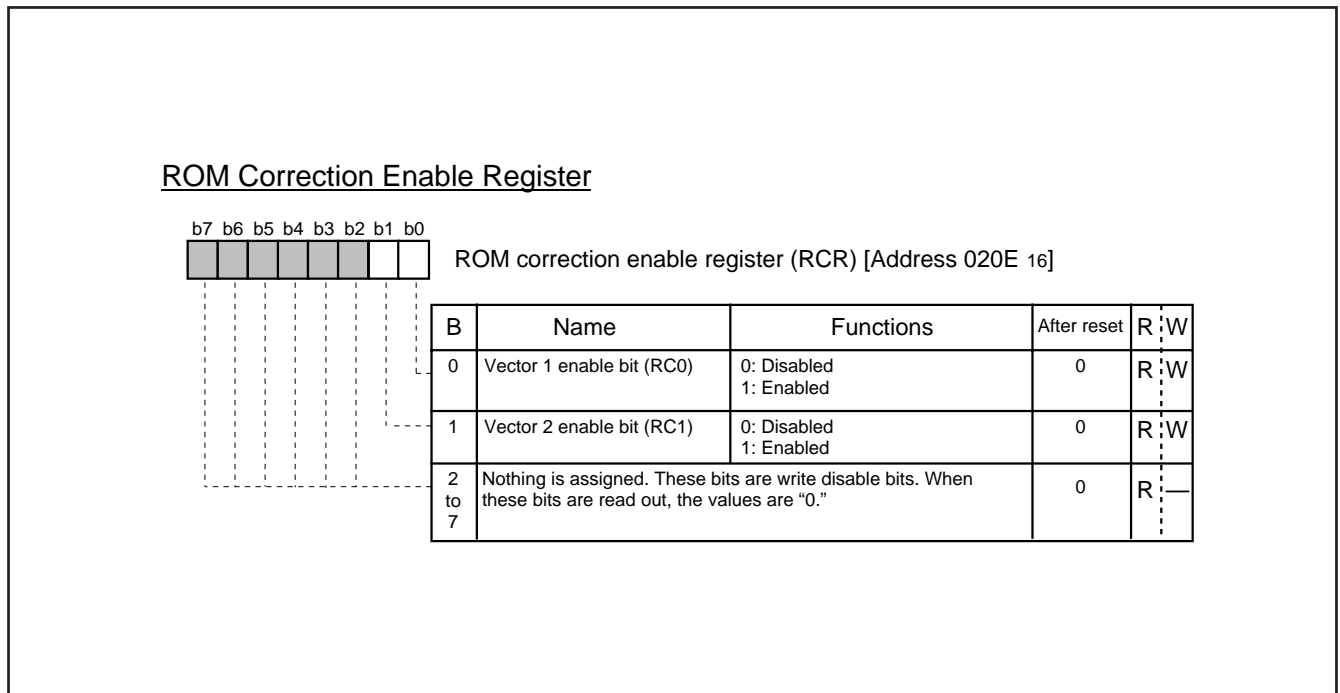


Fig. 8.9.2 ROM Correction Enable Register

### 8.10 DATA SLICER

This microcomputer includes the data slicer function for the closed caption decoder (referred to as the CCD). This function takes out the caption data superimposed in the vertical blanking interval of a composite video signal. A composite video signal which makes the sync chip's polarity negative is input to the CV<sub>IN</sub> pin.

When the data slicer function is not used, the data slicer circuit and the timing signal generating circuit can be cut off by setting bit 0 of the data slicer control register 1 (address 00E0<sub>16</sub>) to "0." These settings can realize the low-power dissipation.

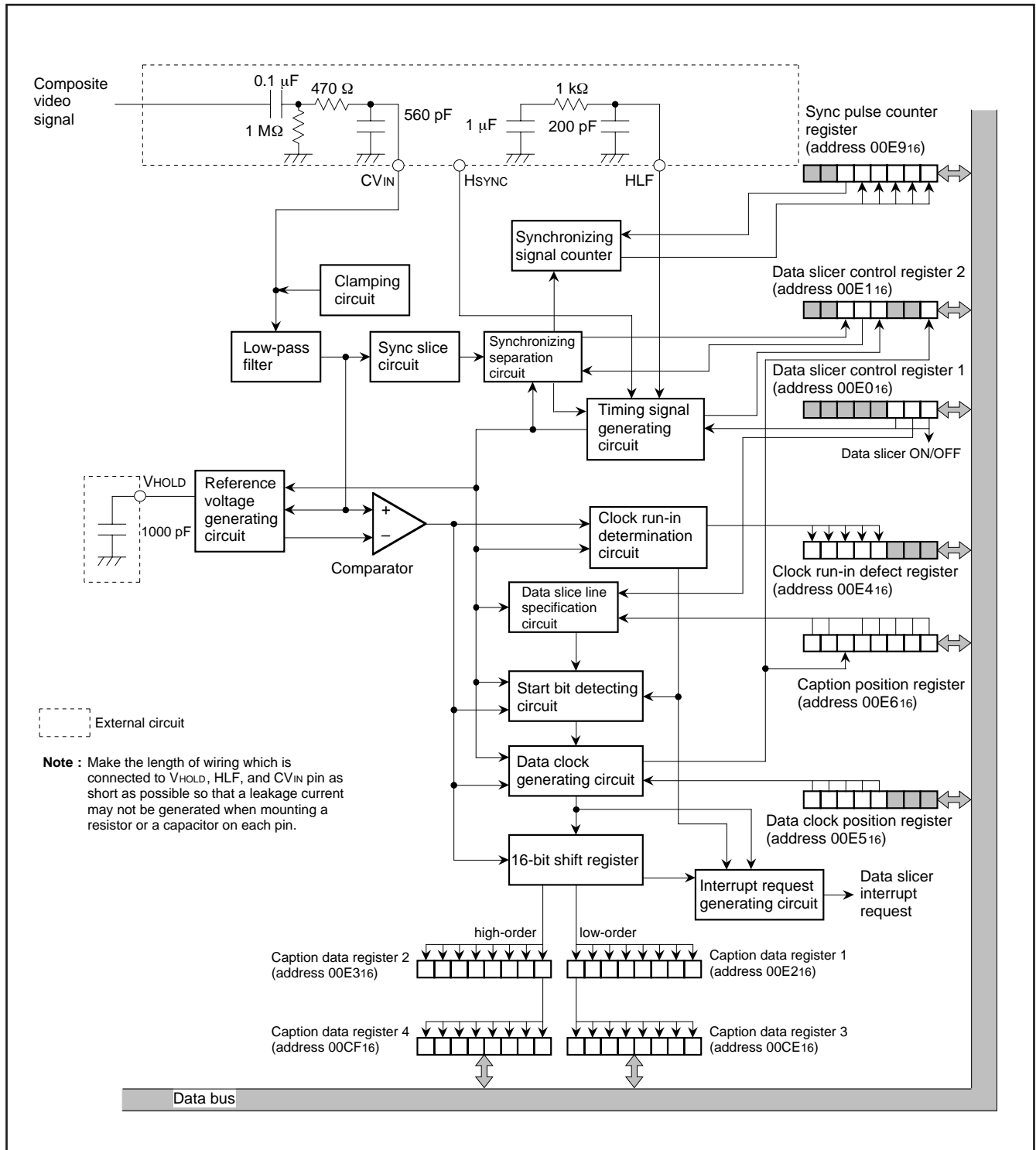


Fig. 8.10.1 Data Slicer Block Diagram



### 8.10.1 Notes When not Using Data Slicer

When bit 0 of data slicer control register 1 (address 00E016) is "0," terminate the pins as shown in Figure 8.10.2.

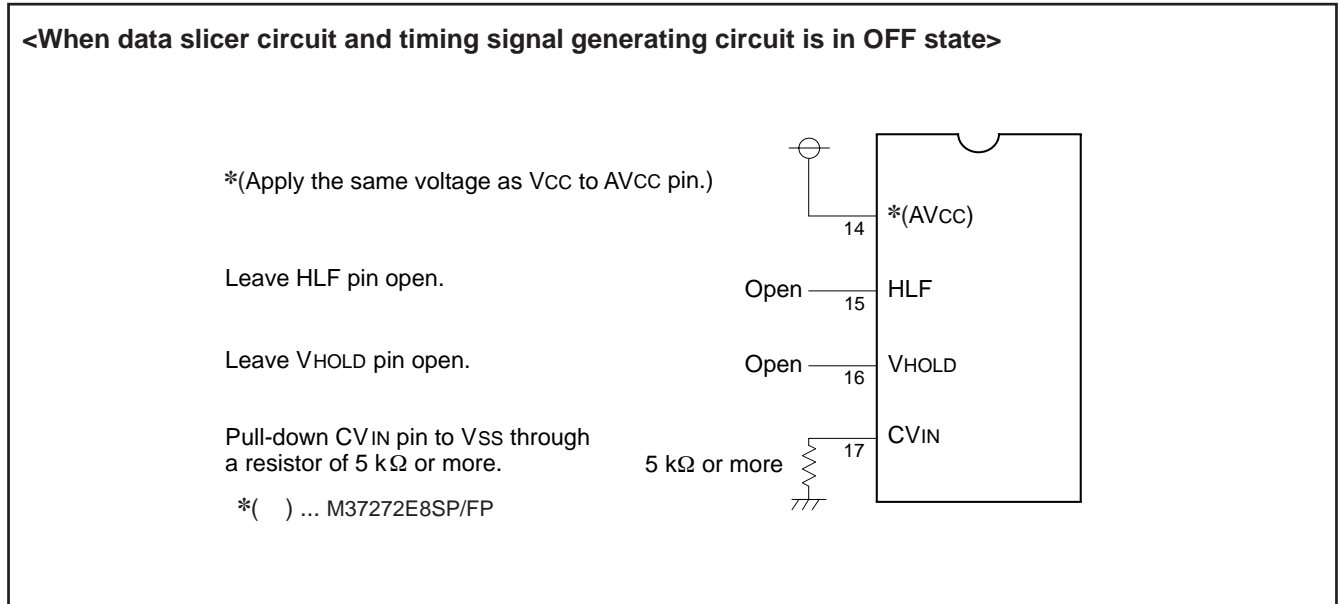


Fig. 8.10.2 Termination of Data Slicer Input/Output Pins when Data Slicer Circuit and Timing Generating Circuit Is in OFF State

When both bits 0 and 2 of data slicer control register 1 (address 00E016) are "1," terminate the pins as shown in Figure 8.10.3.

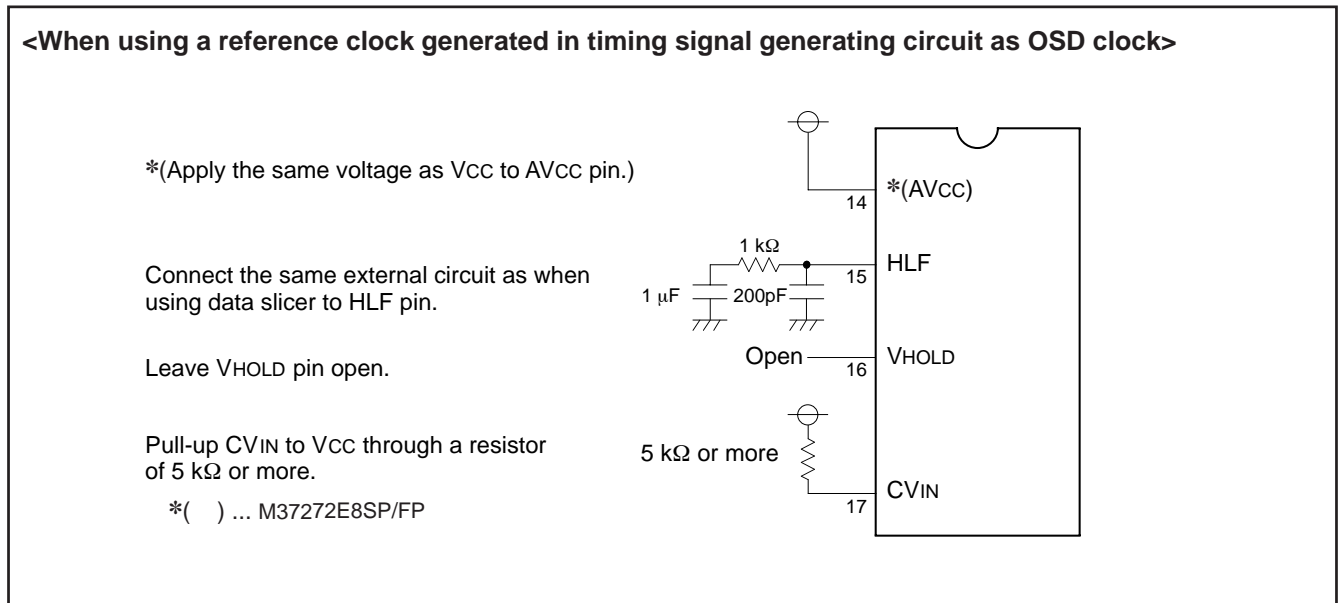


Fig. 8.10.3 Termination of Data Slicer Input/Output Pins when Timing Signal Generating Circuit Is in ON State

Figures 8.10.4 and 8.10.5 the data slicer control registers.

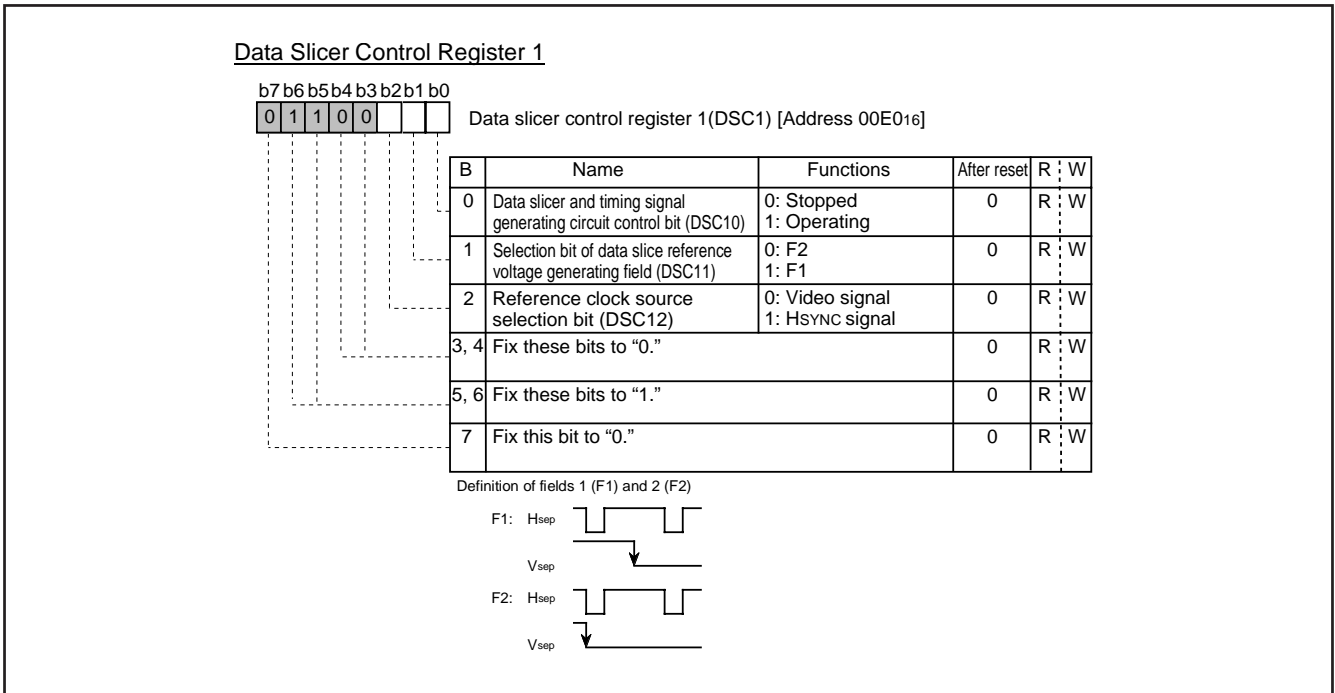


Fig. 8.10.4 Data Slicer Control Register 1

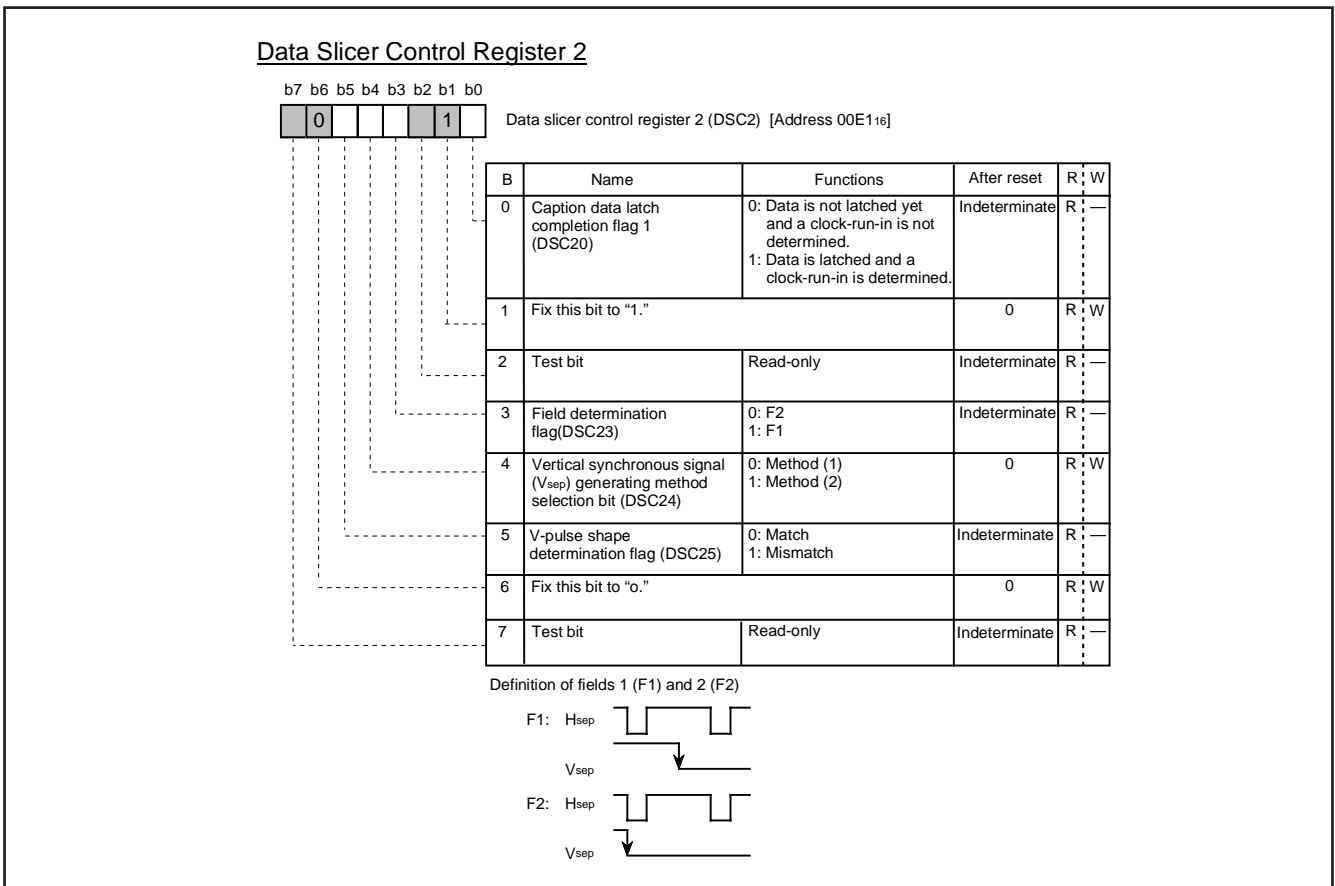


Fig. 8.10.5 Data Slicer Control Register 2

### 8.10.2 Clamping Circuit and Low-pass Filter

The clamp circuit clamps the sync chip part of the composite video signal input from the CVIN pin. The low-pass filter attenuates the noise of clamped composite video signal. The CVIN pin to which composite video signal is input requires a capacitor (0.1  $\mu$ F) coupling outside. Pull down the CVIN pin with a resistor of hundreds of kilohms to 1 M $\Omega$ . In addition, we recommend to install externally a simple low-pass filter using a resistor and a capacitor at the CVIN pin (refer to Figure 8.10.1).

### 8.10.3 Sync Slice Circuit

This circuit takes out a composite sync signal from the output signal of the low-pass filter.

### 8.10.4 Synchronous Signal Separation Circuit

This circuit separates a horizontal synchronous signal and a vertical synchronous signal from the composite sync signal taken out in the sync slice circuit.

#### (1) Horizontal Synchronous Signal (Hsep)

A one-shot horizontal synchronizing signal Hsep is generated at the falling edge of the composite sync signal.

#### (2) Vertical Synchronous Signal (Vsep)

As a Vsep signal generating method, it is possible to select one of the following 2 methods by using bit 4 of the data slicer control register 2 (address 00E116).

- Method 1 The LOW level width of the composite sync signal is measured. If this width exceeds a certain time, a Vsep signal is generated in synchronization with the rising of the timing signal immediately after this LOW level.
- Method 2 The LOW level width of the composite sync signal is measured. If this width exceeds a certain time, it is detected whether a falling of the composite sync signal exits or not in the LOW level period of the timing signal immediately after this LOW level. If a falling exists, a Vsep signal is generated in synchronization with the rising of the timing signal (refer to Figure 8.10.6).

Figure 8.10.6 shows a Vsep generating timing. The timing signal shown in the figure is generated from the reference clock which the timing generating circuit outputs.

Reading bit 5 of data slicer control register 2 permits determining the shape of the V-pulse portion of the composite sync signal. As shown in Figure 8.10.7, when the A level matches the B level, this bit is "0." In the case of a mismatch, the bit is "1."

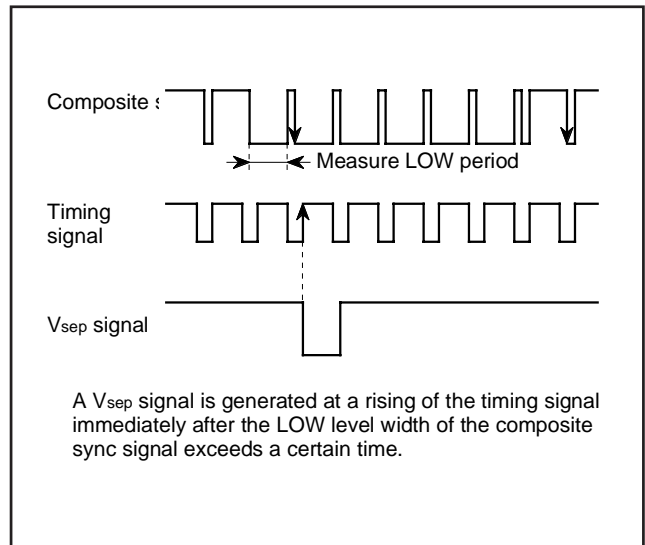


Fig. 8.10.6 Vsep Generating Timing (method 2)

### 8.10.5 Timing Signal Generating Circuit

This circuit generates a reference clock which is 832 times as large as the horizontal synchronous signal frequency. It also generates various timing signals on the basis of the reference clock, horizontal synchronous signal and vertical synchronizing signal. The circuit operates by setting bit 0 of data slicer control register 1 (address 00E016) to "1."

The reference clock can be used as a display clock for OSD function in addition to the data slicer. The HSYNC signal can be used as a count source instead of the composite sync signal. However, when the HSYNC signal is selected, the data slicer cannot be used. A count source of the reference clock can be selected by bit 2 of data slicer control register 1 (address 00E016).

For the pins HLF, connect a resistor and a capacitor as shown in Figure 8.10.1. Make the length of wiring which is connected to these pins as short as possible so that a leakage current may not be generated.

**Note:** It takes a few tens of milliseconds until the reference clock becomes stable after the data slicer and the timing signal generating circuit are started. In this period, various timing signals, H<sub>sep</sub> signals and V<sub>sep</sub> signals become unstable. For this reason, take stabilization time into consideration when programming.

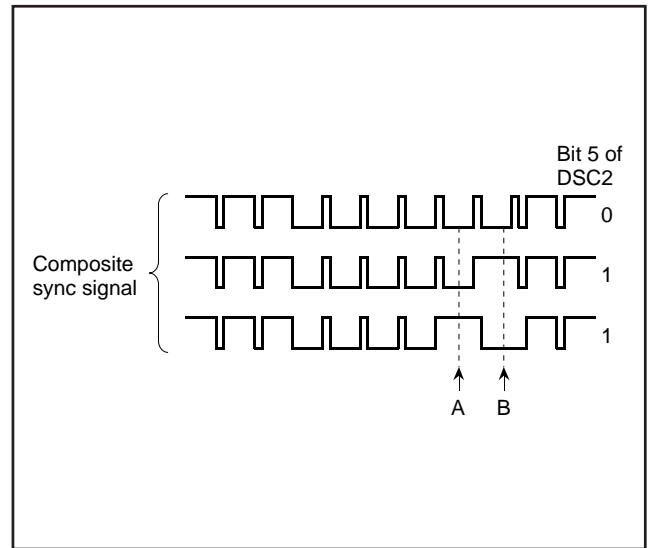


Fig. 8.10.7 Determination of V-pulse Waveform

## 8.10.6 Data Slice Line Specification Circuit

### (1) Specification of data slice line

This circuit decides a line on which caption data is superimposed. The line 21 (fixed), 1 appropriate line for a period of 1 field (total 2 line for a period of 1 field), and both fields (F1 and F2) are sliced their data. The caption position register (address 00E616) is used for each setting (refer to Table 8.10.1).

The counter is reset at the falling edge of  $V_{sep}$  and is incremented by 1 every  $H_{sep}$  pulse. When the counter value matched the value specified by bits 4 to 0 of the caption position register, this  $H_{sep}$  is sliced.

The values of "0016" to "1F16" can be set in the caption position register (at setting only 1 appropriate line). Figure 8.10.8 shows the signals in the vertical blanking interval. Figure 8.10.9 shows the structure of the caption position register.

### (2) Specification of line to set slice voltage

The reference voltage for slicing (slice voltage) is generated for the clock run-in pulse in the particular line (refer to Table 8.10.1). The field to generate slice voltage is specified by bit 1 of data slicer control register 1. The line to generate slice voltage 1 field is specified by bits 6, 7 of the caption position register (refer to Table 8.10.1).

### (3) Field determination

The field determination flag can be read out by bit 3 of data slicer control register 2. This flag charge at the falling edge of  $V_{sep}$ .

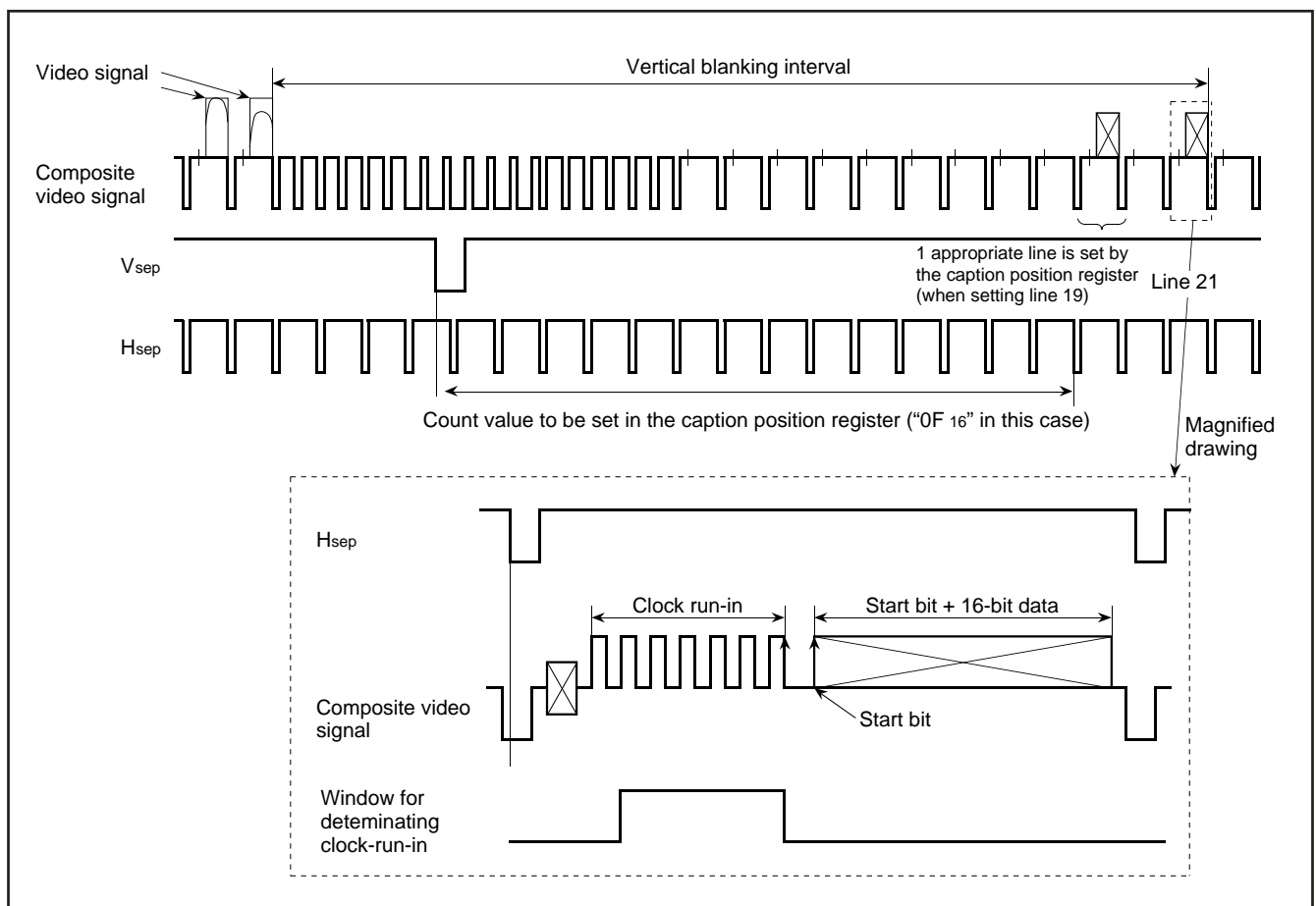


Fig. 8.10.8 Signals in Vertical Blanking Interval

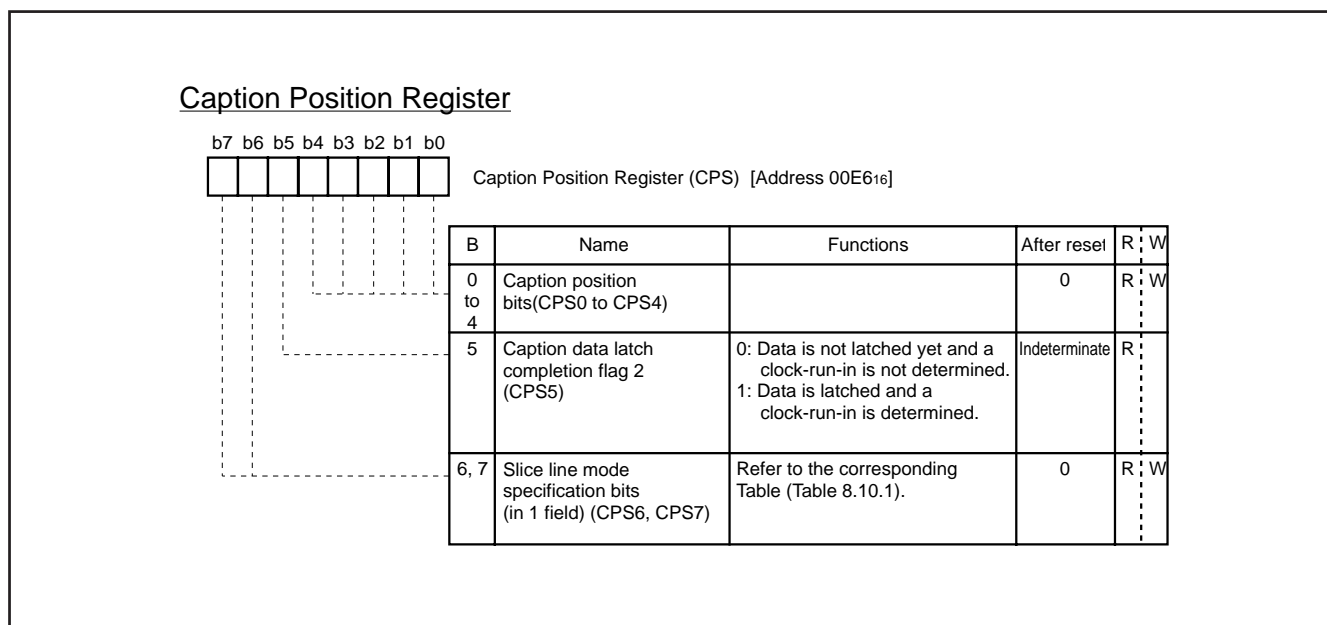


Fig. 8.10.9 Caption Position Register

Table 8.10.1 Specification of Data Slice Line

CPS		Field and Line to Be Sliced Data	Field and Line to Generate Slice Voltage
b7	b6		
0	0	<ul style="list-style-type: none"> <li>• Both fields of F1 and F2</li> <li>• Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2)</li> </ul>	<ul style="list-style-type: none"> <li>• Field specified by bit 1 of DSC1</li> <li>• Line 21 (total 1 line)</li> </ul>
0	1	<ul style="list-style-type: none"> <li>• Both fields of F1 and F2</li> <li>• A line specified by bits 4 to 0 of CPS (total 1 line) (See note 3)</li> </ul>	<ul style="list-style-type: none"> <li>• Field specified by bit 1 of DSC1</li> <li>• A line specified by bits 4 to 0 of CPS (total 1 line) (See note 3)</li> </ul>
1	0	<ul style="list-style-type: none"> <li>• Both fields of F1 and F2</li> <li>• Line 21 (total 1 line)</li> </ul>	<ul style="list-style-type: none"> <li>• Field specified by bit 1 of DSC1</li> <li>• Line 21 (total 1 line)</li> </ul>
1	1	<ul style="list-style-type: none"> <li>• Both fields of F1 and F2</li> <li>• Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2)</li> </ul>	<ul style="list-style-type: none"> <li>• Field specified by bit 1 of DSC1</li> <li>• Line 21 and a line specified by bits 4 to 0 of CPS (total 2 lines) (See note 2)</li> </ul>

**Notes 1:** DSC1 is data slicer control register 1.  
 CPS is caption position register.  
**2:** Set "0016" to "1016" to bits 4 to 0 of CPS.  
**3:** Set "0016" to "1F16" to bits 4 to 0 of CPS.

### 8.10.7 Reference Voltage Generating Circuit and Comparator

The composite video signal clamped by the clamping circuit is input to the reference voltage generating circuit and the comparator.

#### (1) Reference voltage generating circuit

This circuit generates a reference voltage (slice voltage) by using the amplitude of the clock run-in pulse in line specified by the data slice line specification circuit. Connect a capacitor between the VHOLD pin and the VSS pin, and make the length of wiring as short as possible so that a leakage current may not be generated.

#### (2) Comparator

The comparator compares the voltage of the composite video signal with the voltage (reference voltage) generated in the reference voltage generating circuit, and converts the composite video signal into a digital value.

### 8.10.8 Start Bit Detecting Circuit

This circuit detects a start bit at line decided in the data slice line specification circuit.

The detection of a start bit is described below.

- ① A sampling clock is generated by dividing the reference clock output by the timing signal.
- ② A clock run-in pulse is detected by the sampling clock.
- ③ After detection of the pulse, a start bit pattern is detected from the comparator output.

### 8.10.9 Clock Run-in Determination Circuit

This circuit determinates clock run-in by counting the number of pulses in a window of the composite video signal.

The reference clock count value in one pulse cycle is stored in bits 3 to 7 of the clock run-in detect register (address 00E4<sub>16</sub>). Read out these bits after the occurrence of a data slicer interrupt (refer to "8.10.12 Interrupt Request Generating Circuit").

Figure 8.10.10 shows the structure of clock run-in detect register.

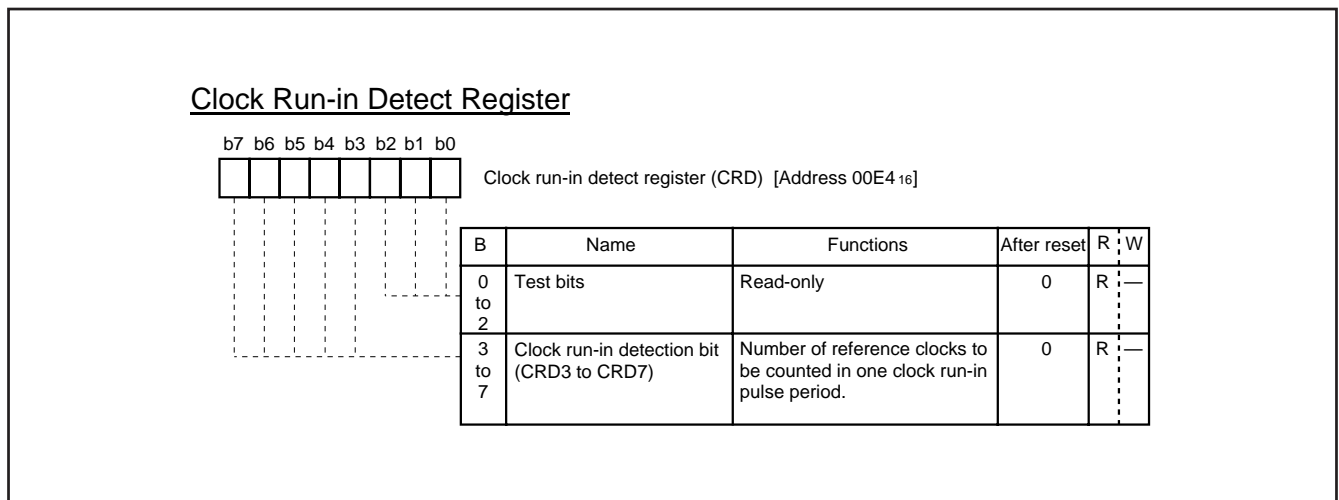


Fig. 8.10.10 Clock Run-in Detect Register

### 8.10.10 Data Clock Generating Circuit

This circuit generates a data clock synchronized with the start bit detected in the start bit detecting circuit. The data clock stores caption data to the 16-bit shift register. When the 16-bit data has been stored and the clock run-in determination circuit determines clock run-in, the caption data latch completion flag is set. This flag is reset at a falling of the vertical synchronous signal (Vsep).

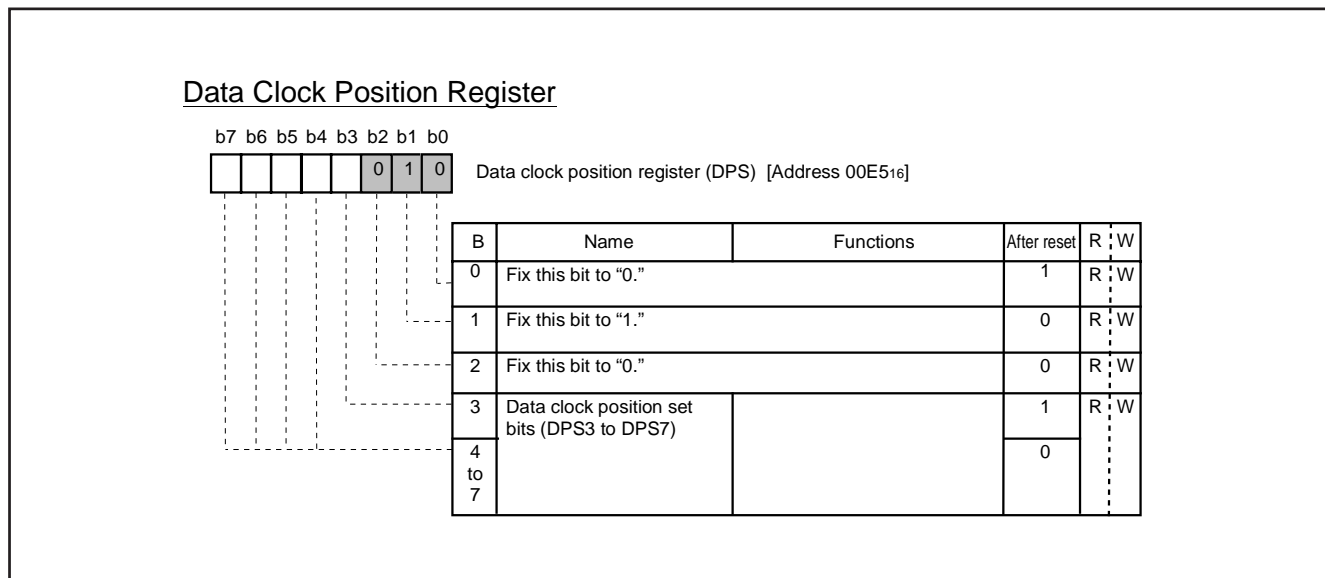


Fig. 8.10.11 Data Clock Position Register



### 8.10.11 16-bit Shift Register

The caption data converted into a digital value by the comparator is stored into the 16-bit shift register in synchronization with the data clock. The contents of the high-order 8 bits of the stored caption data can be obtained by reading out data register 2 (address 00E316) and data register 4 (address 00CF16). The contents of the low-order 8 bits can be obtained by reading out data register 1 (address 00E216) and data register 3 (address 00CE16), respectively. These registers are reset to “0” at a falling of  $V_{sep}$ . Read out data registers 1 and 2 after the occurrence of a data slicer interrupt (refer to “8.10.12 Interrupt Request Generating Circuit”).

### 8.10.12 Interrupt Request Generating Circuit

The interrupt requests as shown in Table 8.10.3 are generated by combination of the following bits; bits 6 and 7 of the caption position register (address 00E616). Read out the contents of data registers 1 to 4 and the contents of bits 3 to 7 of the clock run-in detect register after the occurrence of a data slicer interrupt request.

**Table 8.10.2 Contents of Caption Data Latch Completion Flag and 16-bit Shift Register**

Slice Line Specification Mode		Contents of Caption Data Latch Completion Flag		Contents of 16-bit Shift Register	
CPS		Completion Flag 1 (bit 0 of DSC2)	Completion Flag 2 (bit 5 of CPS)	Caption Data Registers 1, 2	Caption Data Registers 3, 4
bit 7	bit 6				
0	0	Line 21	A line specified by bits 4 to 0 of CPS	16-bit data of line 21	16-bit data of a line specified by bits 4 to 0 of CPS
0	1	A line specified by bits 4 to 0 of CPS	Invalid	16-bit data of a line specified by bits 4 to 0 of CPS	Invalid
1	0	Line 21	Invalid	16-bit data of line 21	Invalid
1	1	Line 21	A line specified by bits 4 to 0 of CPS	16-bit data of line 21	16-bit data of a line specified by bits 4 to 0 of CPS

CPS: Caption position register

DSC2: Data slicer control register 2

**Table 8.10.3 Occurrence Sources of Interrupt Request**

Caption position register		Occurrence Sources of Interrupt Request at End of Data Slice Line
b7	b6	
0	0	After slicing line 21
	1	After a line specified by bits 4 to 0 of CPS
1	0	After slicing line 21
	1	After slicing line 21

### 8.10.13 Synchronous Signal Counter

The synchronous signal counter counts the composite sync signal taken out from a video signal in the data slicer circuit or the vertical synchronous signal  $V_{sep}$  as a count source.

The count value in a certain time (T time) generated by  $f(X_{IN})/2^{13}$  or  $f(X_{IN})/2^{13}$  is stored into the 5-bit latch. Accordingly, the latch value changes in the cycle of T time. When the count value exceeds "1F<sub>16</sub>," "1F<sub>16</sub>" is stored into the latch.

The latch value can be obtained by reading out the sync pulse counter register (address 00E9<sub>16</sub>). A count source is selected by bit 5 of the sync pulse counter register.

The synchronous signal counter is used when bit 0 of PWM mode register 1 (address 0208<sub>16</sub>).

Figure 8.10.12 shows the structure of the sync pulse counter and Figure 8.10.13 shows the synchronous signal counter block diagram.

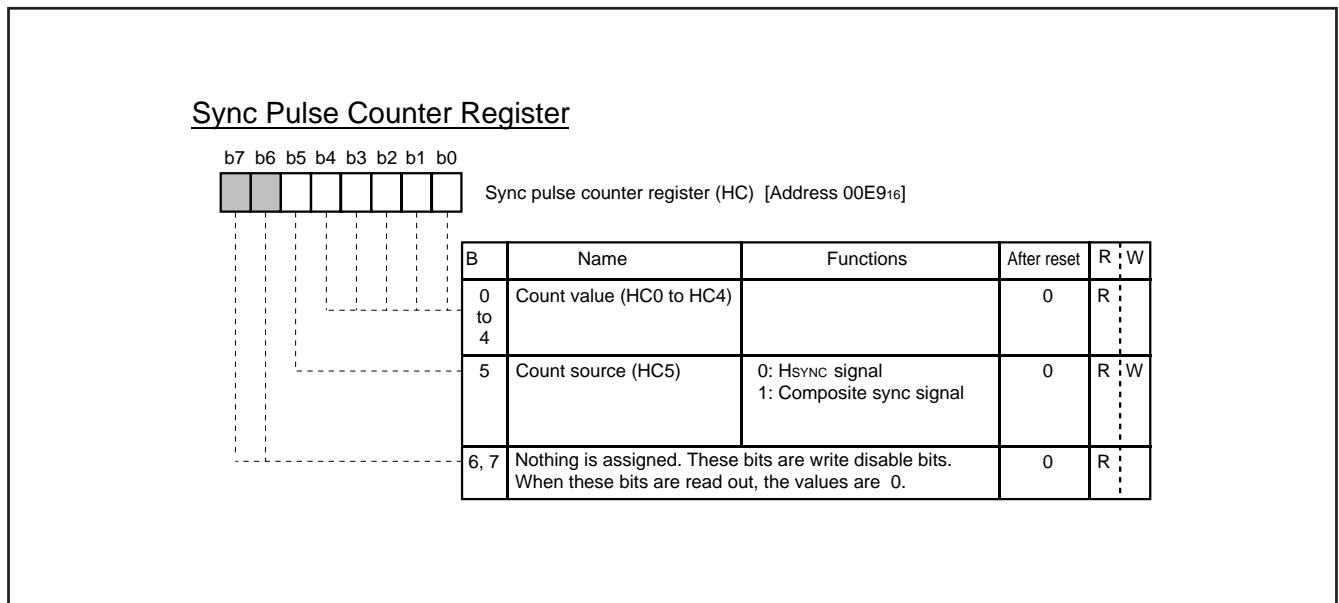


Fig. 8.10.12 Sync Pulse Counter Register

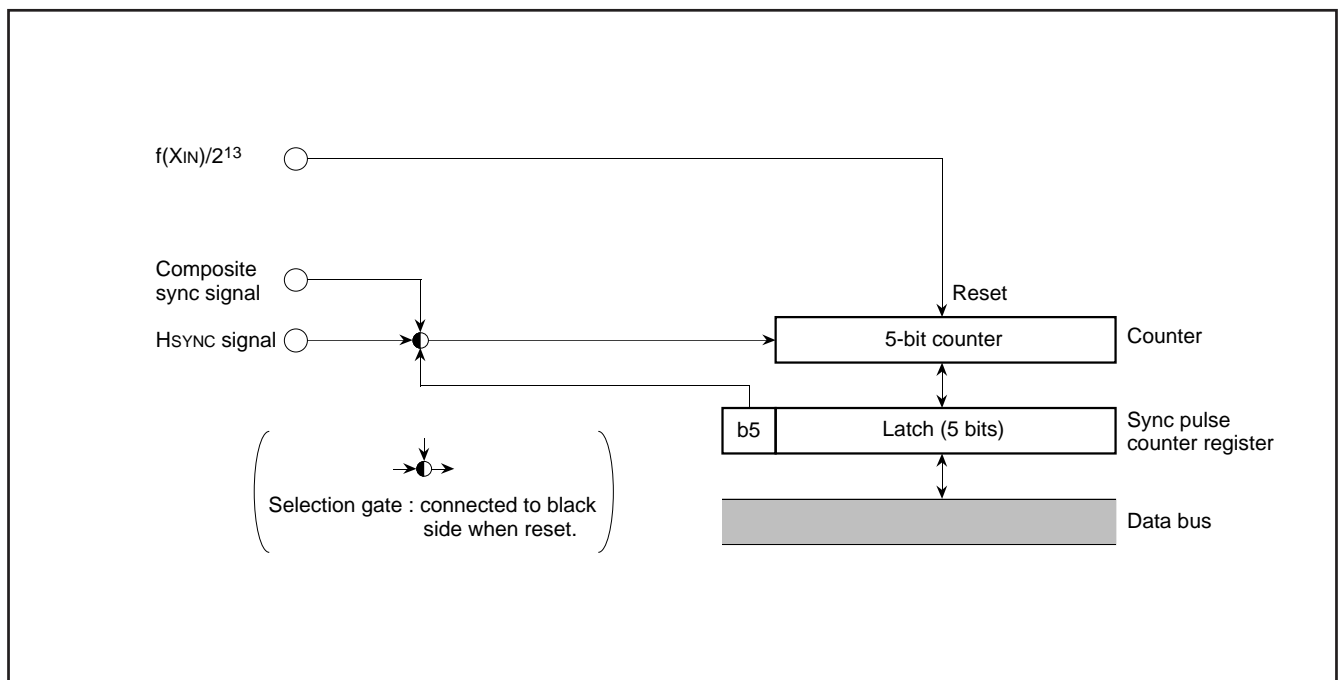


Fig. 8.10.13 Synchronous Signal Counter Block Diagram

## 8.11 OSD FUNCTIONS

Table 8.11.1 outlines the OSD functions.

This microcomputer incorporates an OSD circuit of 32 characters X 2 lines. And also, there are 2 display modes and they are selected by a block unit. The display modes are selected by bits 0 and 1 of block control register i (i = 1 and 2).

The features of each mode are described below.

**Table 8.11.1 Features of Each Display Mode**

Parameter	Display mode	
	CC mode (Closed caption mode)	OSD mode (Border OFF) (On-screen display mode)
Number of display characters	32 characters X 2 lines	
Dot structure	16 X 26 dots (Character display area : 16 X 20 dots)	16 X 20 dots
Kinds of characters	254 kinds	
Kinds of character sizes	1 kinds	8 kinds
Pre-divide ratio (See note)	X 2 (fixed)	X 2, X 3
Dot size	1Tc X 1/2H	1Tc X 1/2H, 1Tc X 1H, 2Tc X 2H, 3Tc X 3H
Attribute	Smooth italic, under line, flash	Border (black)
Character font coloring	1 screen : 8 kinds (per character unit)	
Character background coloring	_____	1 screen : 8 kinds (per character unit)
OSD output	R, G, B	
Raster coloring	Possible (per character unit)	
Function	Auto solid space function Window function	_____
Display position	Horizontal: 128 levels, Vertical: 512 levels	
Display expansion (multiline display)	Possible	

**Notes 1:** The divide ratio of the frequency divider (the pre-divide circuit) is referred as "pre-divide ratio" hereafter.

**2:** The character size is specified with dot size and pre-divide ratio (refer to 8.11.2 Dot Size).

The OSD circuit has an extended display mode. This mode allows multiple lines (3 lines or more) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 8.11.1 shows the configuration of OSD character. Figure 8.11.2 shows the block diagram of the OSD circuit. Figure 8.11.3 shows the OSD control register. Figure 8.11.4 shows the block control register i.

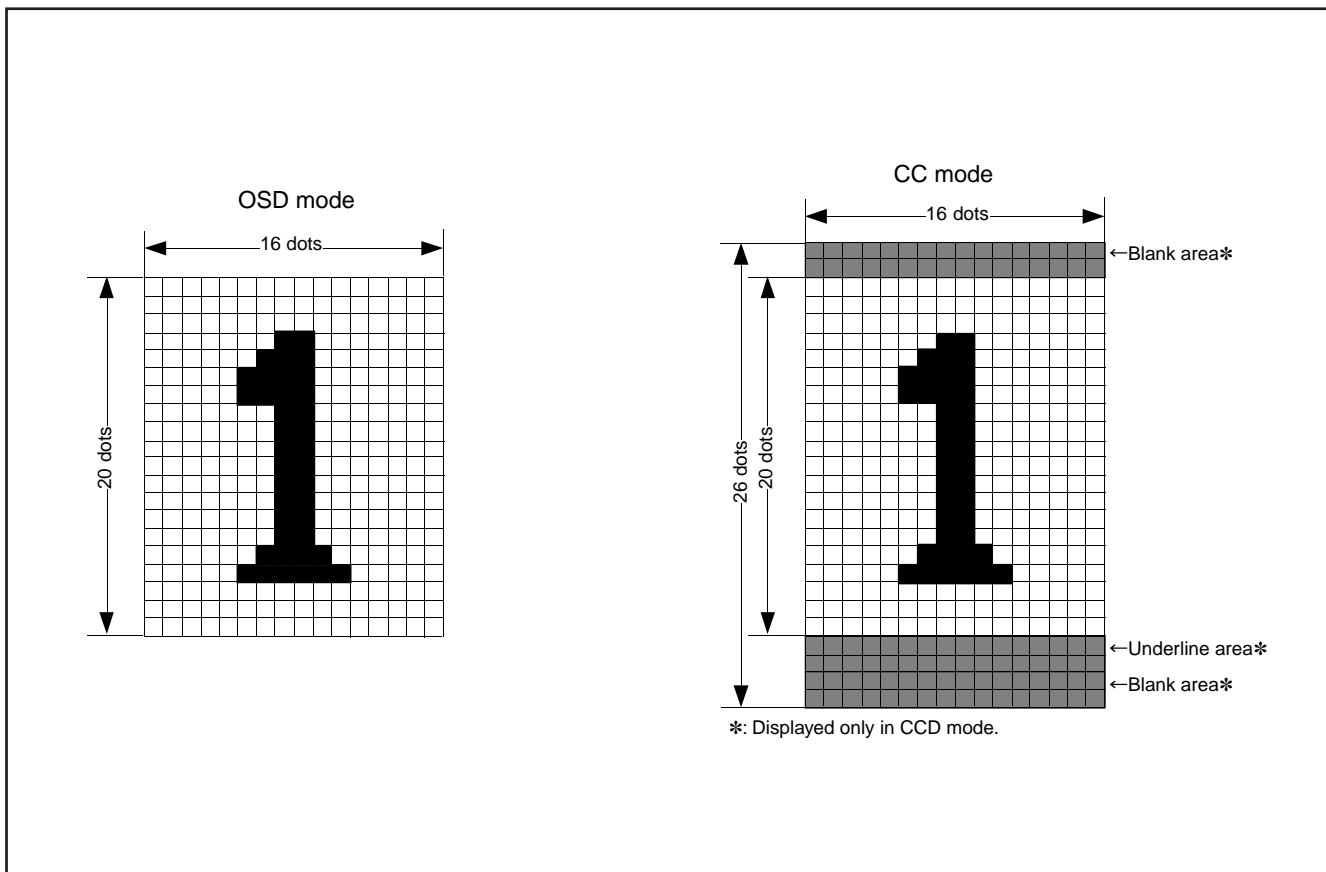


Fig. 8.11.1 Configuration of OSD Character Display Area

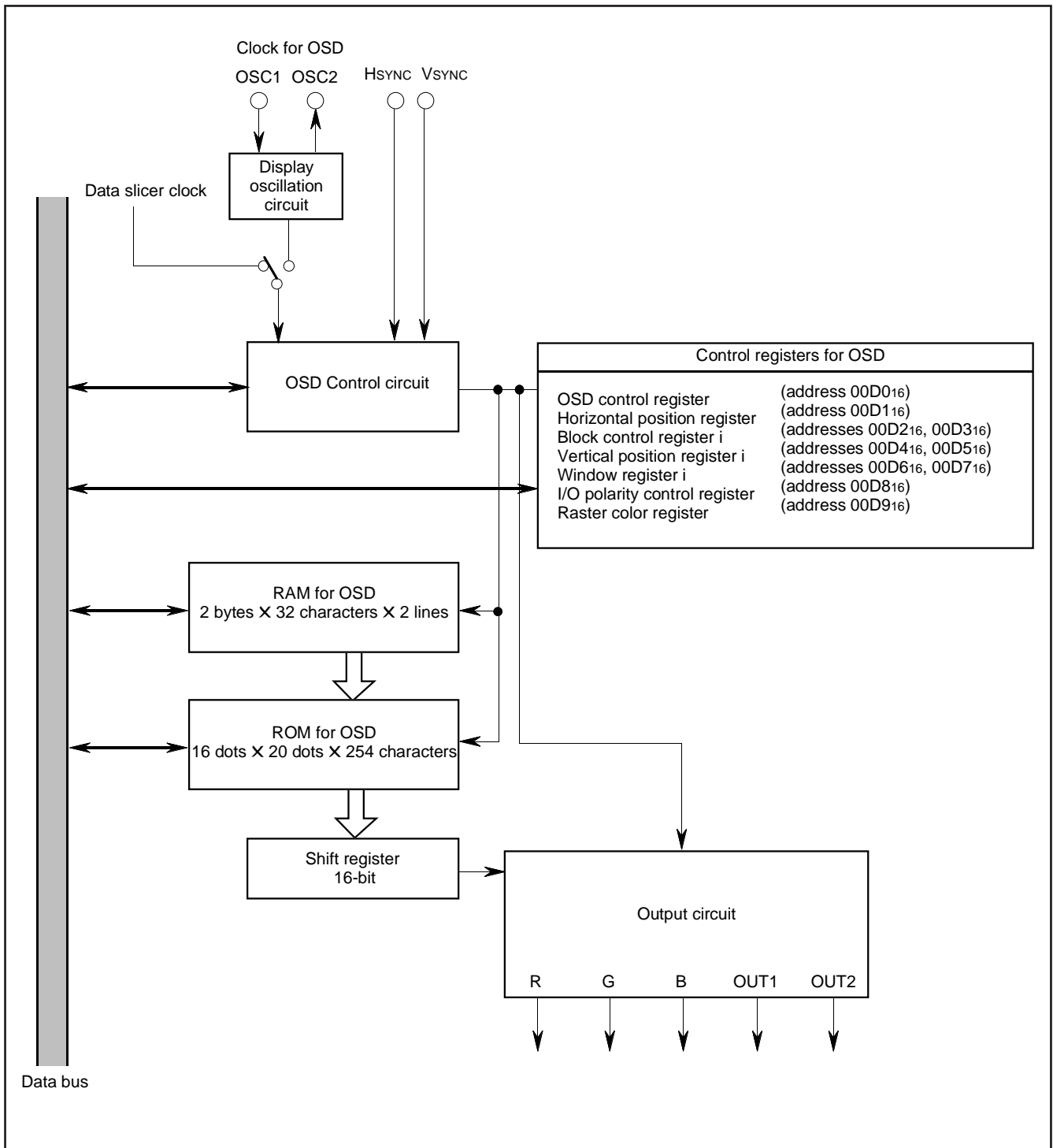
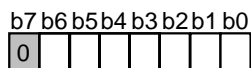


Fig. 8.11.2 Block Diagram of OSD Circuit

### OSD Control Register



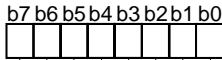
OSD control register (OC) [Address 00D016]

B	Name	Functions	After reset	R/W
0	OSD control bit (OC0) (See note)	0 : All-blocks display off 1 : All-blocks display on	0	R/W
1	Automatic solid space control bit (OC1)	0 : OFF 1 : ON	0	R/W
2	Window control bit (OC2)	0 : OFF 1 : ON	0	R/W
3	CC mode clock selection bit (OC3)	0 : Data slicer clock 1 : Clock from OSC1 pin	0	R/W
4	OSD mode clock selection bit (OC4)	0 : Data slicer clock 1 : Clock from OSC1 pin	0	R/W
5, 6	OSC1 clock selection bit (OC5, OC6)	b6 b5 0 0: 32 kHz oscillating 0 1: Do not set. 1 0: LC oscillating, Ceramic oscillating 1 1: Do not set.	0	R/W
7	Fix this bit to 0.		0	R/W

**Note:** Even this bit is switched during display, the display screen remains unchanged until a rising (falling) of the next V SYNC.

Fig. 8.11.3 OSD Control Register

**Block Control register i**



Block control register i (BCi) (i=1, 2) [Addresses 00D2 16 and 00D3 16]

B	Name	Functions	After reset	R	W
0, 1	Display mode selection bits (BCi0, BCi1) (See note 1)	b1 b0 0 0: Display OFF 0 1: CC mode 1 0: OSD mode (Border OFF) 1 1: OSD mode (Border ON)	Indeterminate	R	W
2, 3	Dot size selection bits (BCi2, BCi3)	b4 b3 b2 Pre-divide Ratio Dot Size 0 0 0 × 2 1Tc × 1/2H 0 0 1 1Tc × 1H 1 0 0 2Tc × 2H 1 0 1 3Tc × 3H	Indeterminate	R	W
4	Pre-divide ratio selection bit (BCi4)	b4 b3 b2 Pre-divide Ratio Dot Size 1 0 0 × 3 1Tc × 1/2H 1 0 1 1Tc × 1H 1 1 0 2Tc × 2H 1 1 1 3Tc × 3H	Indeterminate	R	W
5	OUT1/OUT2 output control bit (BCi5) (See note 1)	0: OUT1 output control 1: OUT2 output control	Indeterminate	R	W
6	Vertical display start position control bit (BCi6)	BC16: Block 1 BC26: Block 1	Indeterminate	R	W
7	Window top/bottom boundary control bit (BCi7)	BC17: Window top boundary BC27: Window bottom boundary	Indeterminate	R	W

**Notes 1:** Bit RA3 of OSD RAM controls OUT1 output when bit 5 is "0."  
Bit RA3 of OSD RAM controls OUT2 output when bit 5 is "1."  
**2:** Tc is OSD clock cycle divided in pre-divide circuit.  
**3:** H is HSYNC.

Fig. 8.11.4 Block Control Register i

### 8.11.1 Display Position

The display positions of characters are specified in units called a "block." There are 2 blocks, blocks 1 and 2. Up to 32 characters can be displayed in each block (refer to "8.11.5 Memory for OSD").

The display position of each block can be set in both horizontal and vertical directions by software.

The display start position in the horizontal direction can be selected for all blocks in common from 128-step display positions in units of  $4T_{osc}$  ( $T_{osc}$  = OSD oscillation cycle).

The display start position in the vertical direction for each block can be selected from 512-step display positions in units of  $1T_H$  ( $T_H$  = HSYNC cycle).

Blocks are displayed in conformance with the following rules:

- When the display position of block 1 is overlapped with that of block 2 (Figure 8.11.5 (b)), the block 1 is displayed on the front.
- When another block display position appears while one block is displayed (Figure 8.11.5 (c)), the block with a larger set value as the vertical display start position is displayed.

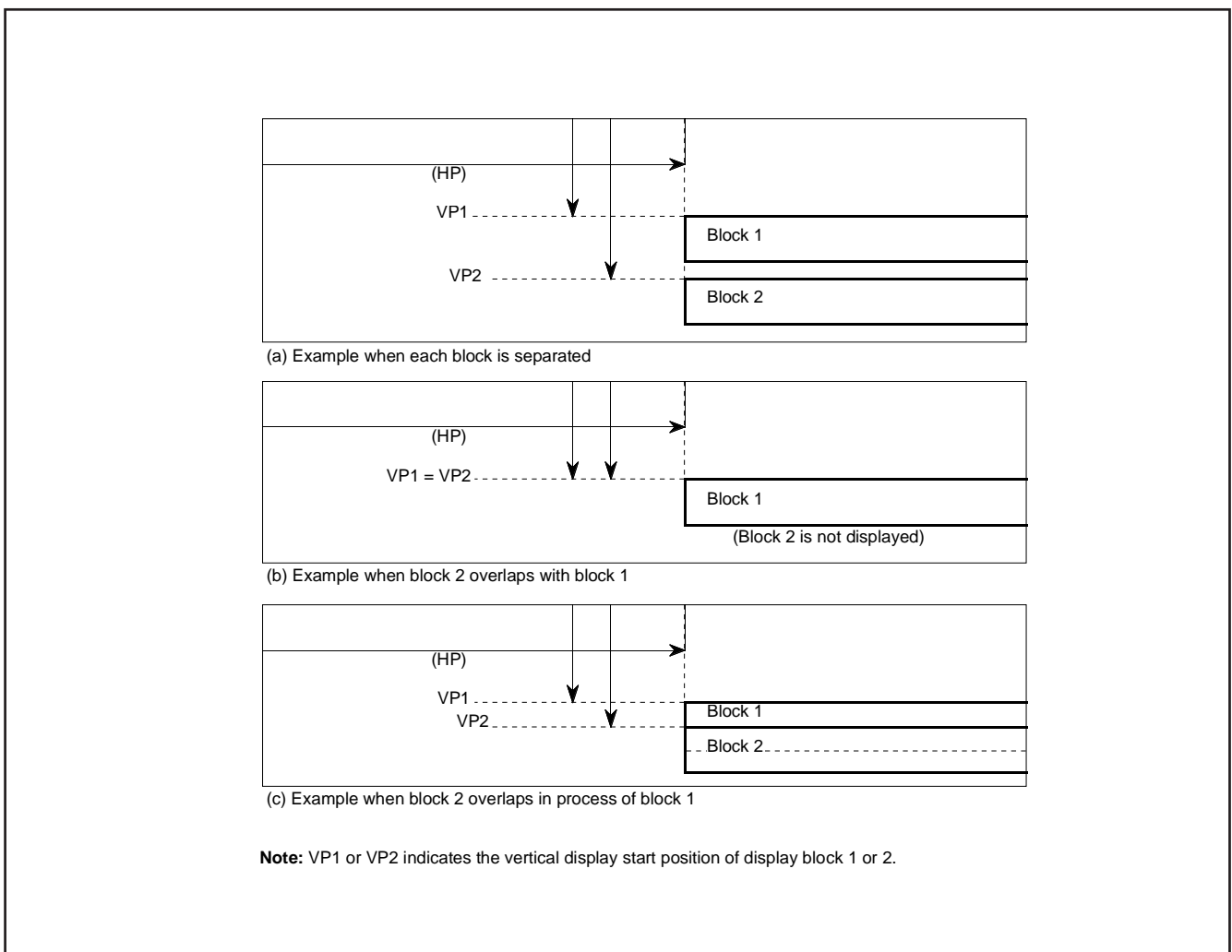


Fig. 8.11.5 Display Position



The vertical display start position is determined by counting the horizontal sync signal (HSYNC). At this time, when VSYNC and HSYNC are positive polarity (negative polarity), it starts to count the rising edge (falling edge) of HSYNC signal from after fixed cycle of rising edge (falling edge) of VSYNC signal. So interval from rising edge (falling edge) of VSYNC signal to rising edge (falling edge) of HSYNC signal needs enough time (2 machine cycles or more) for avoiding jitter. The polarity of HSYNC and VSYNC signals can select with the I/O polarity control register (address 00D816).

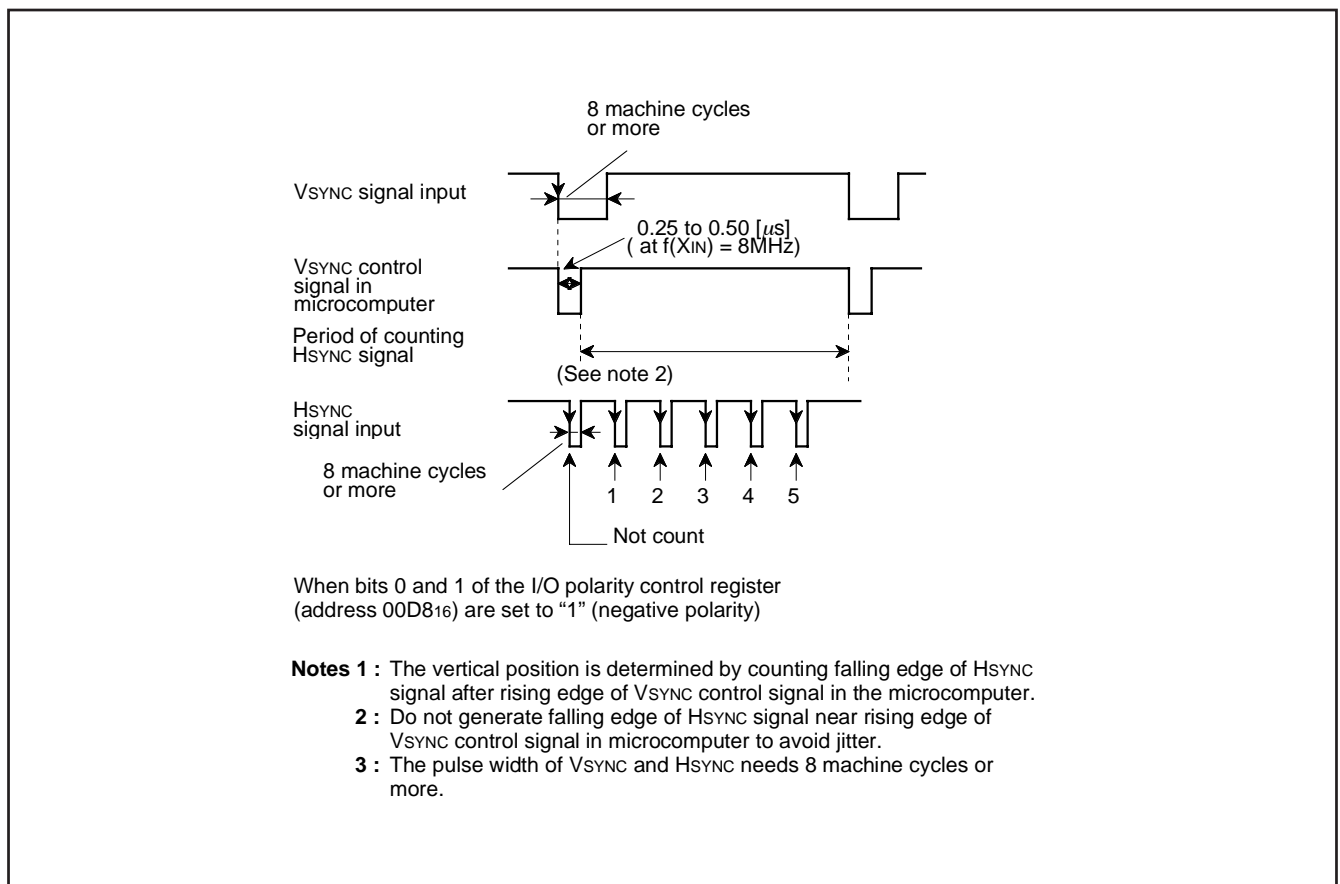


Fig. 8.11.6 Supplement Explanation for Display Position

The vertical display start position for each block can be set in 512 steps (where each step is 1TH (TH: HSYNC cycle)) as values "0016" to "FF16" in vertical position register i (i = 1 and 2) (addresses 00D416 and 00D516) and values "0" or "1" in bit 6 of block control register i (i = 1 and 2) (addresses 00D216 and 00D316). The vertical position registers is shown in Figure 8.11.7.

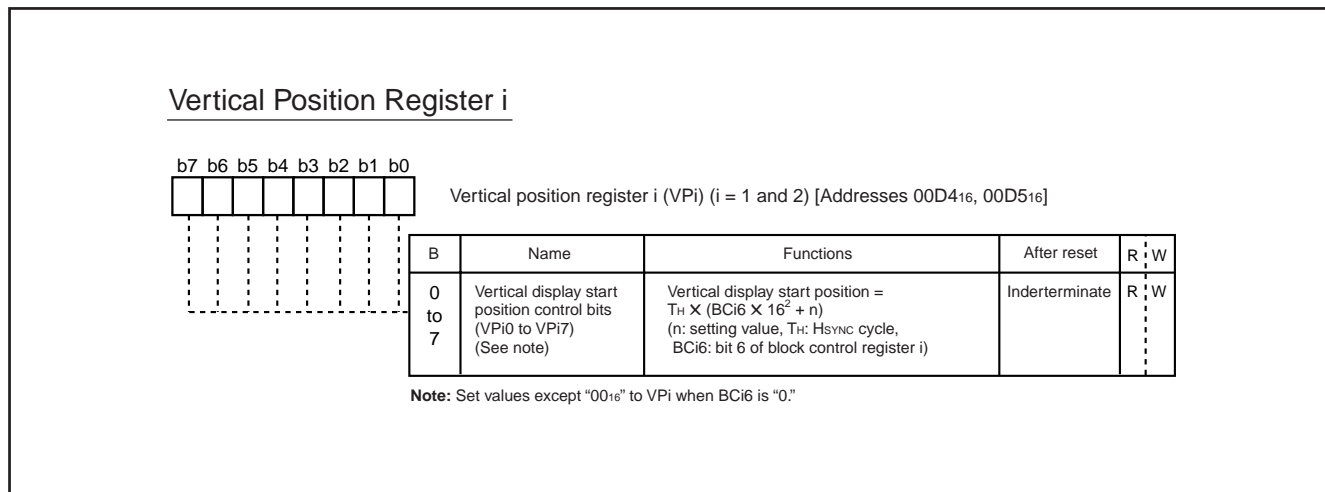


Fig. 8.11.7 Vertical Position Register i (i = 1 and 2)

The horizontal display start position is common to all blocks, and can be set in 128 steps (where 1 step is 4Tosc, TOSC being the OSD oscillation cycle) as values "0016" to "FF16" in bits 0 to 6 of the horizontal position register (address 00D116). The horizontal position register is shown in Figure 8.11.8.

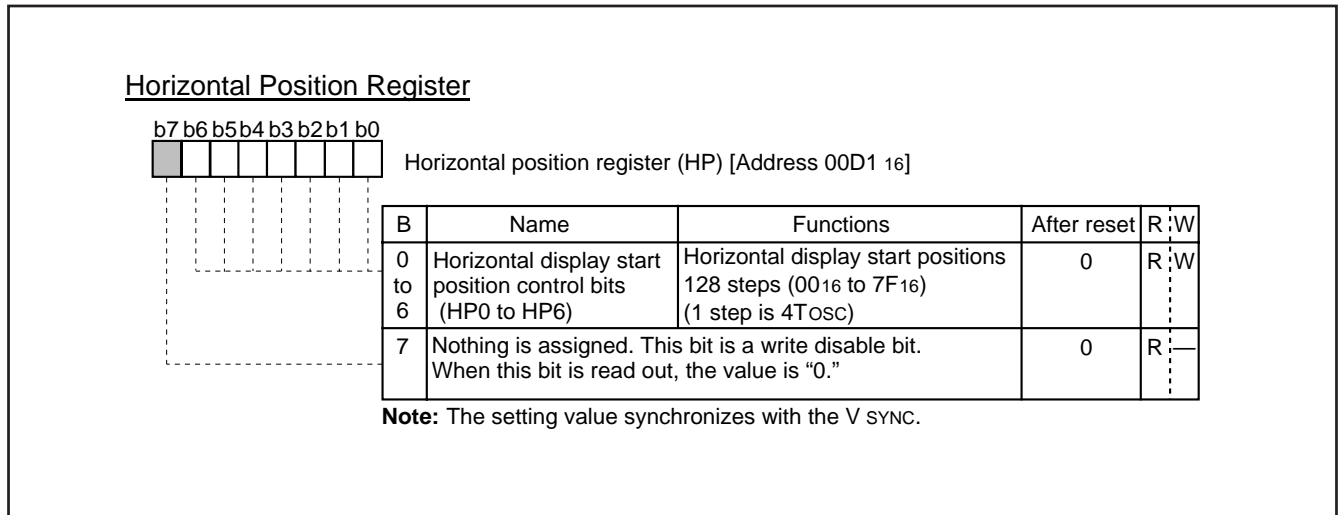


Fig. 8.11.8 Horizontal Position Register

- Notes**
- 1 : 1Tc (Tc : OSD clock cycle divided in pre-divide circuit) gap occurs between the horizontal display start position set by the horizontal position register and the most left dot of the 1st block. Accordingly, when 2 blocks have different pre-divide ratios, their horizontal display start position will not match.
  - 2 : The horizontal start position is based on the OSD clock source cycle selected for each block. Accordingly, when 2 blocks have different OSD clock source cycles, their horizontal display start position will not match.
  - 3 : When setting "0016" to the horizontal position register, it needs approximately 62Tosc (= Tdef) interval from a rising edge (when negative polarity is selected) of HSYNC signal to the horizontal display start position.

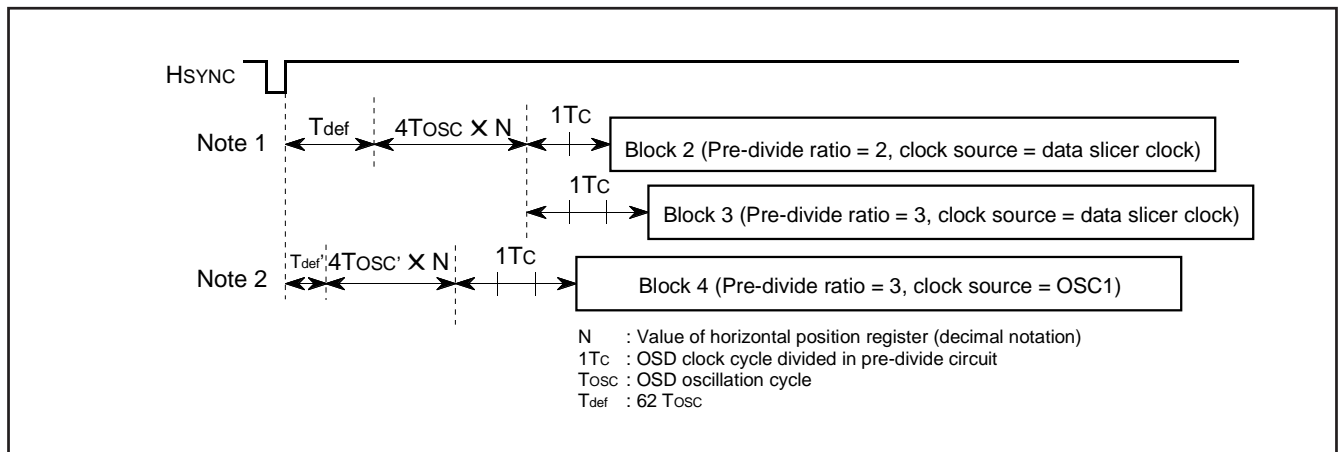


Fig. 8.11.9 Notes on Horizontal Display Start Position

### 8.11.2 Dot Size

The dot size can be selected by a block unit. The dot size in vertical direction is determined by dividing HSYNC in the vertical dot size control circuit. The dot size in horizontal is determined by dividing the following clock in the horizontal dot size control circuit : the clock gained by dividing the OSD clock source (data slicer clock, OSC1) in the pre-divide circuit. The clock cycle divided in the pre-divide circuit is defined as 1Tc.

The dot size of each block is specified by bits 2 to 4 of the block control register i.

Refer to Figure 8.11.4 (the structure of the block control register).

The block diagram of dot size control circuit is shown in Figure 8.11.10.

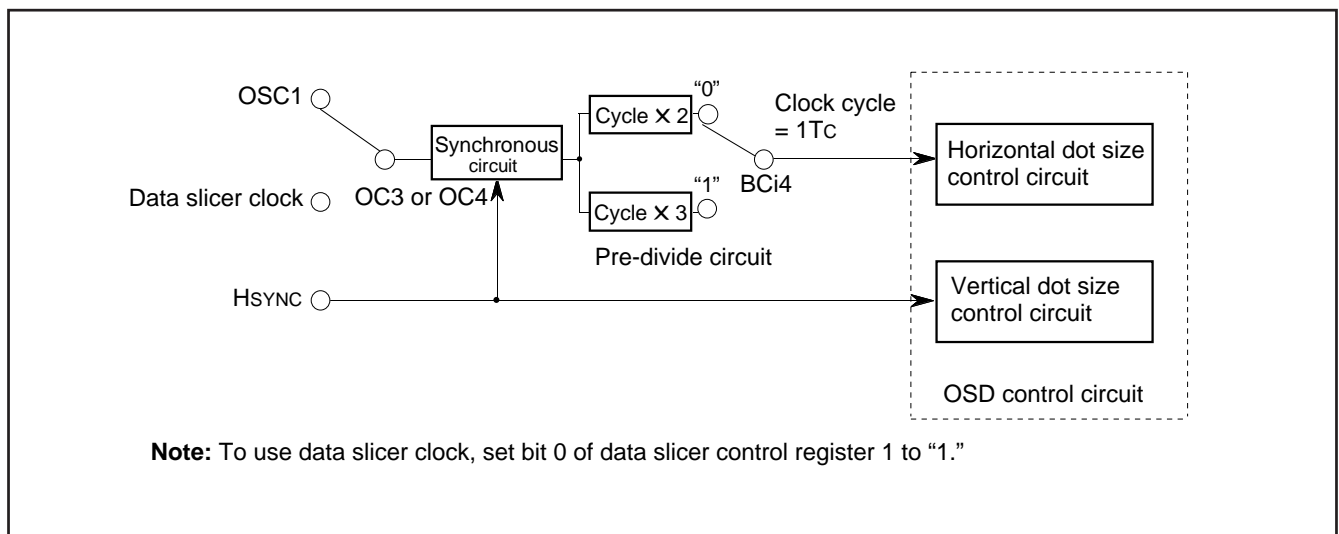


Fig. 8.11.10 Block Diagram of Dot Size Control Circuit

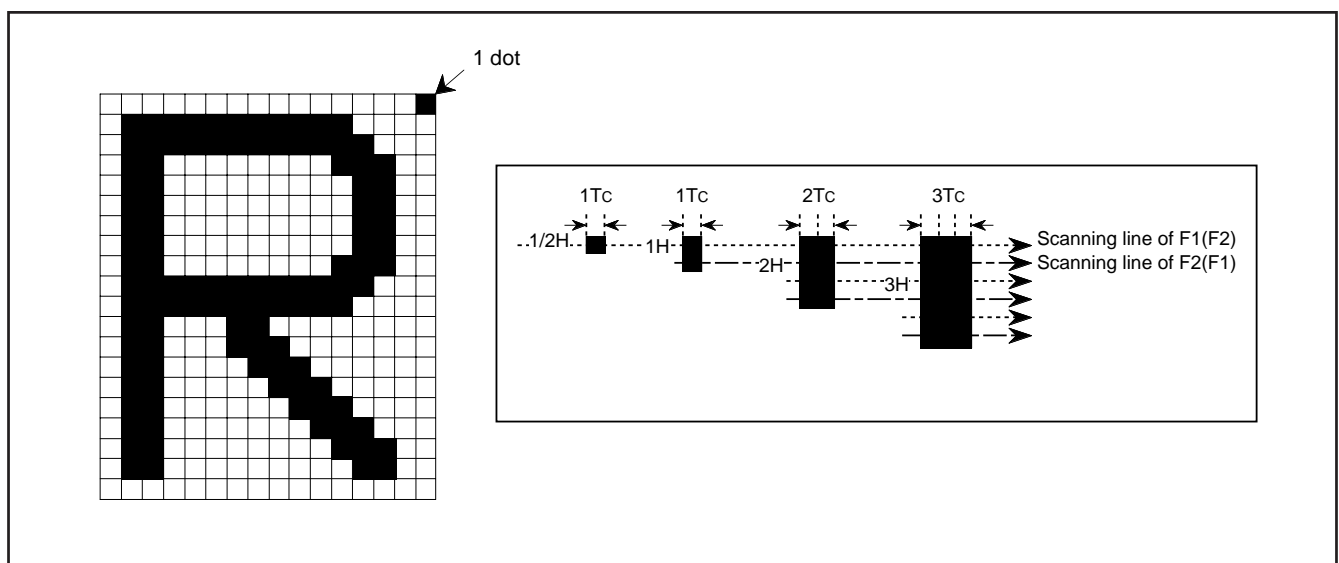


Fig. 8.11.11 Definition of Dot Sizes

### 8.11.3 Clock for OSD

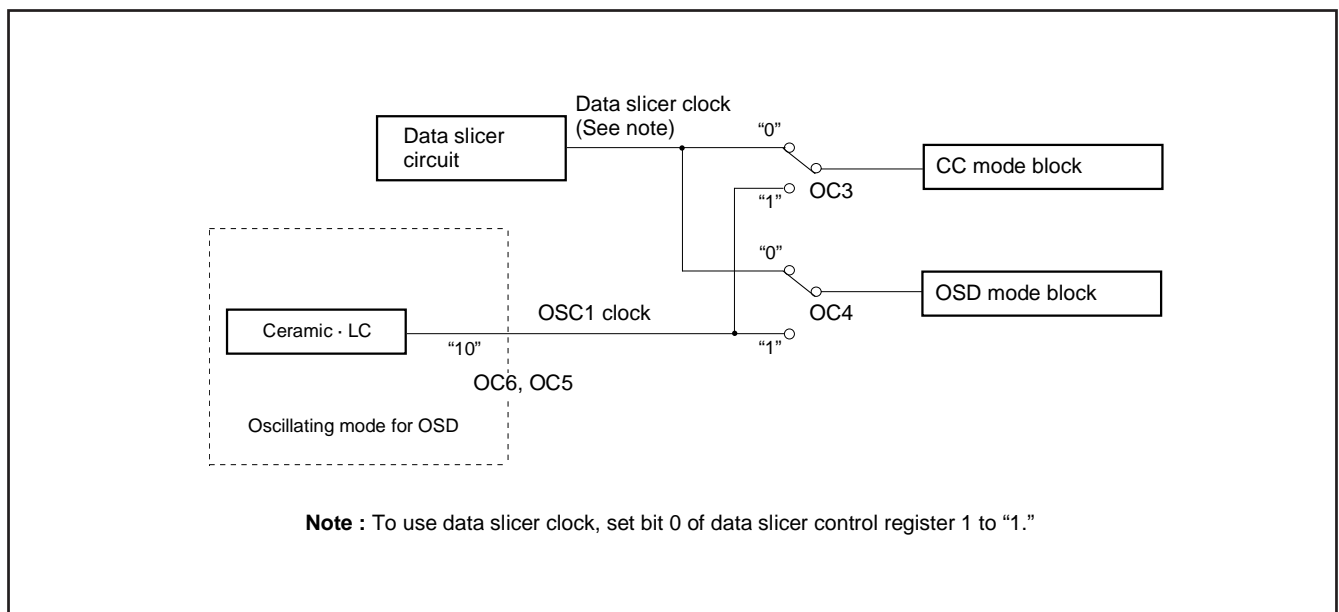
As a clock for display to be used for OSD, it is possible to select one of the following 3 types.

- Data slicer clock output from the data slicer (approximately 26 MHz)
- OSC1 clock supplied from the pins OSC1 and OSC2
- Clock from the ceramic resonator or the LC oscillator from the pins OSC1 and OSC2

This OSD clock for each block can be selected by the following bits : bit 7 of the raster color register (address 00D9<sub>16</sub>), bits 3 to 6 of the clock source control register (addresses 00D0<sub>16</sub>). A variety of character sizes can be obtained by combining dot sizes with OSD clocks. When not using the pins OSC1 and OSC2 for the OSD clock I/O pins, the pins can be used as sub-clock I/O pins or port P2.

**Table 8.11.2 Setting for P26/OSC1/XcIN, P27/OSC2/XcOUT**

Register	Function	OSD clock I/O Pin	Sub-clock I/O Pin	I/O Port
b7 of raster color register		0	0	1
OSD control register	b6	1	0	1
	b5	0	0	0



**Fig. 8.11.12 Block Diagram of OSD Selection Circuit**

### 8.11.4 Field Determination Display

To display the block with vertical dot size of 1/2H, whether an even field or an odd field is determined through differences in a synchronizing signal waveform of interlacing system. The dot line 0 or 1 (refer to Figure 8.11.14) corresponding to the field is displayed alternately.

In the following, the field determination standard for the case where both the horizontal sync signal and the vertical sync signal are negative-polarity inputs will be explained. A field determination is determined by detecting the time from a falling edge of the horizontal sync signal until a falling edge of the VSYNC control signal (refer to Figure 8.11.6) in the microcomputer and then comparing this time with the time of the previous field. When the time is longer than the comparing time, it is regarded as even field. When the time is shorter, it is regarded as odd field

The contents of this field can be read out by the field determination flag (bit 6 of the I/O polarity control register at address 00D8<sub>16</sub>). A dot line is specified by bit 5 of the I/O polarity control register (refer to Figure 8.11.14).

However, the field determination flag read out from the CPU is fixed to "0" at even field or "1" at odd field, regardless of bit 5.

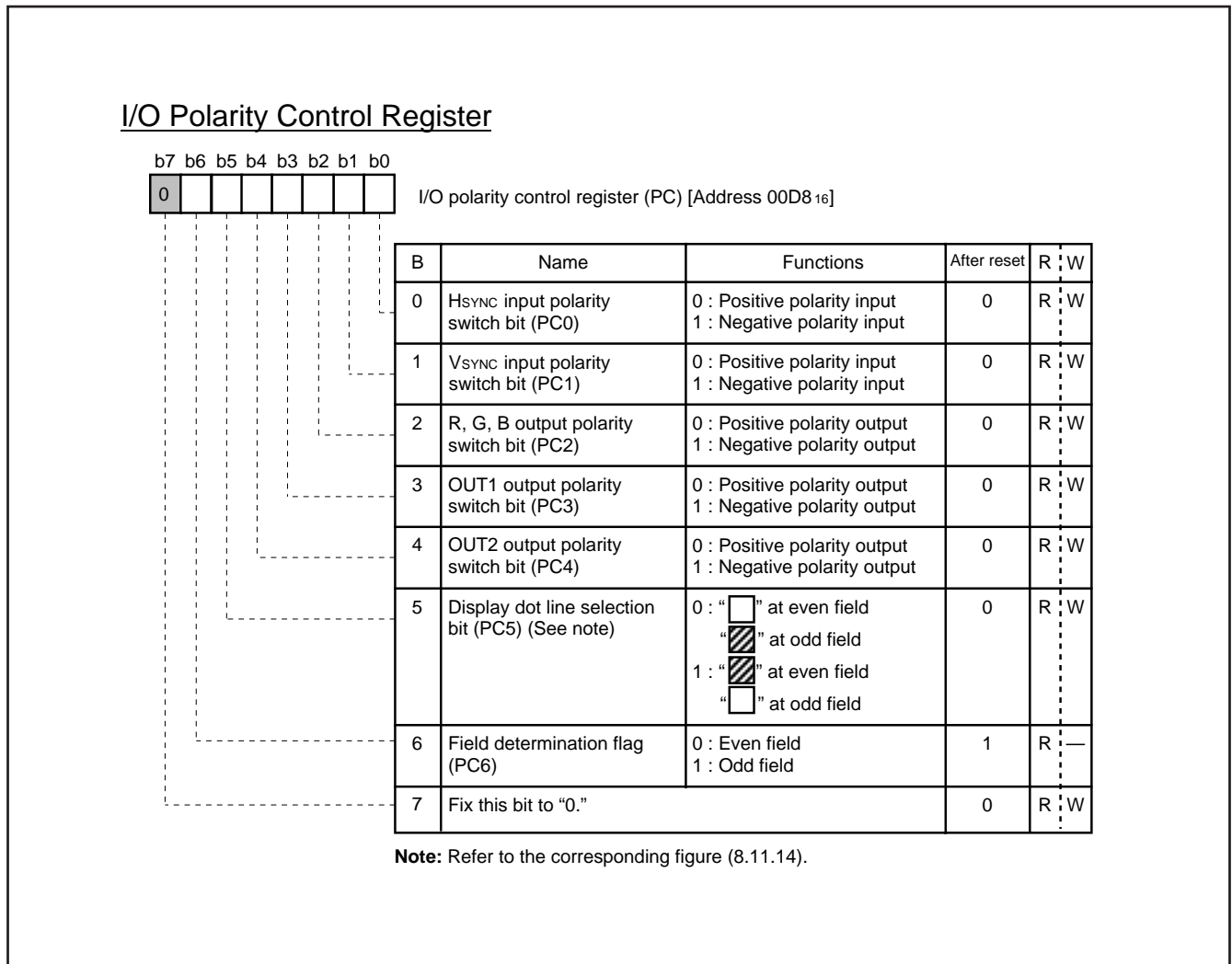
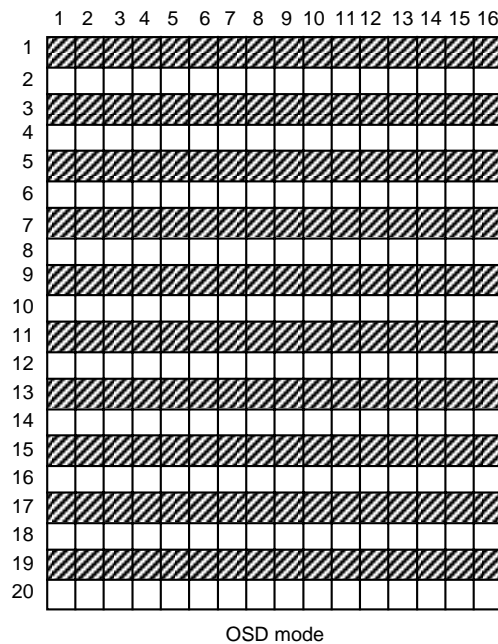
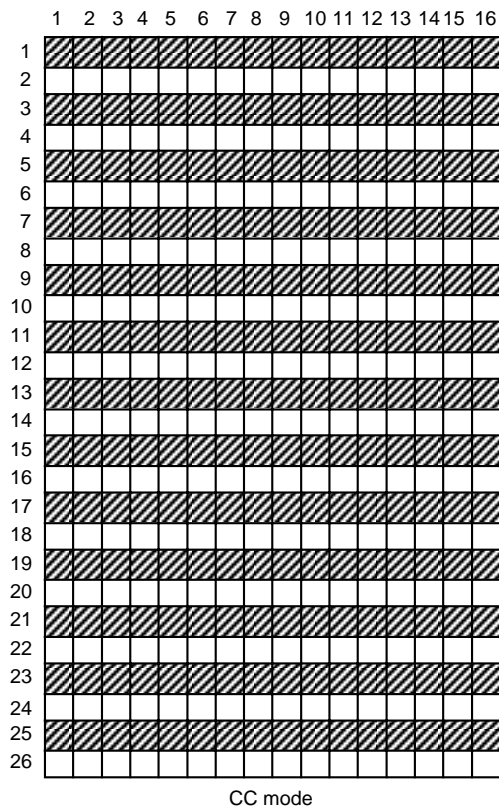


Fig. 8.11.13 I/O Polarity Control Register

Both Hsync signal and Vsync signal are negative-polarity input

Hsync		Field	Field determination flag(Note)	Display dot line selection bit	Display dot line
Vsync and Vsync control signal in microcomputer  Upper : Vsync signal  Lower : Vsync control signal in microcomputer		Odd	/	/	/
		Even	0 (T2 > T1)	0	Dot line 1 <input type="checkbox"/>
		Odd	1 (T3 < T2)	0	Dot line 0 <input checked="" type="checkbox"/>
				1	Dot line 1 <input type="checkbox"/>

When using the field determination flag, be sure to set bit 0 of the PWM mode register 1 (address 0208<sub>16</sub>) to "0."



When the display dot line selection bit is "0," the "□" font is displayed at even field, the "▨" font is displayed at odd field. Bit 6 of the I/O polarity control register can be read as the field determination flag : "1" is read at odd field, "0" is read at even field.

OSD ROM font configuration diagram

**Note :** The field determination flag changes at a rising edge of the Vsync control signal (negative-polarity input) in the microcomputer.

Fig. 8.11.14 Relation between Field Determination Flag and Display Font

### 8.11.5 Memory for OSD

There are 2 types of memory for OSD : OSD ROM used to store character dot data and OSD RAM used to specify the characters and colors to be displayed.

<M3727GM6/M8-XXXSP/FP, M37272E8SP/FP>

OSD ROM : addresses 1400<sub>16</sub> to 3BFF<sub>16</sub>

OSD RAM : addresses 0800<sub>16</sub> to 087F<sub>16</sub>

#### (1) OSD ROM (addresses 1400<sub>16</sub> to 3BFF<sub>16</sub>)

The dot pattern data for OSD characters is stored in OSD ROM. To specify the kinds of the character font, it is necessary to write the character code into the OSD RAM.

Data of the character font is specified shown in Figure 8.11.15.

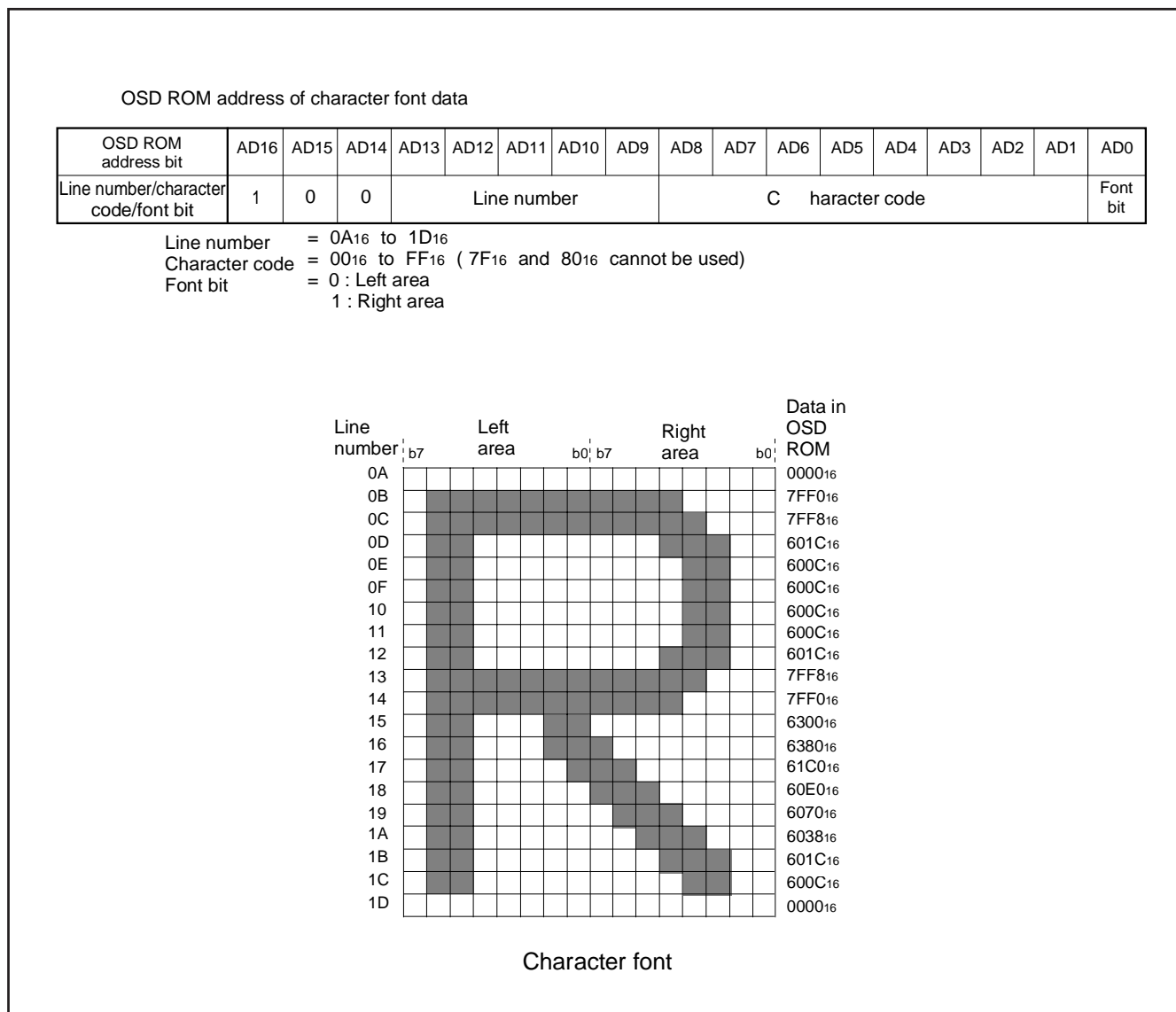


Fig. 8.11.15 Character Font Data Storing Address



**Notes 1** : The 80-byte addresses corresponding to the character code "7F<sub>16</sub>" and "80<sub>16</sub>" in OSD ROM are the test data storing area. Set data to the area as follows.

<Test data storing area>

■ M37272M6/M8-XXXSP/FP, M37272E8SP/FP

addresses 1000<sub>16</sub> + (4 + 2n) X 100<sub>16</sub> + FE<sub>16</sub> to

1000<sub>16</sub> + (5 + 2n) X 100<sub>16</sub> + 01<sub>16</sub>

(n = 0 to 19)

(1)Mask version (M3727GM6/M8-XXXSP/FP)

Set "FF<sub>16</sub>" to the area (We stores the test data to this area and the different data from "FF<sub>16</sub>" is stored for the actual products.) When using our font editor, the test data is written automatically.

(2)EPROM version (M37272E8SP/FP)

Set the test data to the area. When using our font editor, the test data is written automatically.

■M37272E8SP/FP

<"FF <sub>16</sub> "> address (test data)	<"80 <sub>16</sub> "> address (test data)
14FE <sub>16</sub> (09 <sub>16</sub> ), 14FF <sub>16</sub> (51 <sub>16</sub> )	1500 <sub>16</sub> (90 <sub>16</sub> ), 1501 <sub>16</sub> (A1 <sub>16</sub> )
16FE <sub>16</sub> (00 <sub>16</sub> ), 16FF <sub>16</sub> (52 <sub>16</sub> )	1700 <sub>16</sub> (00 <sub>16</sub> ), 1701 <sub>16</sub> (A2 <sub>16</sub> )
18FE <sub>16</sub> (12 <sub>16</sub> ), 18FF <sub>16</sub> (53 <sub>16</sub> )	1900 <sub>16</sub> (48 <sub>16</sub> ), 1901 <sub>16</sub> (A3 <sub>16</sub> )
1AFE <sub>16</sub> (00 <sub>16</sub> ), 1AFF <sub>16</sub> (54 <sub>16</sub> )	1B00 <sub>16</sub> (00 <sub>16</sub> ), 1B01 <sub>16</sub> (A4 <sub>16</sub> )
1CFE <sub>16</sub> (24 <sub>16</sub> ), 1CFF <sub>16</sub> (55 <sub>16</sub> )	1D00 <sub>16</sub> (24 <sub>16</sub> ), 1D01 <sub>16</sub> (A5 <sub>16</sub> )
1EFE <sub>16</sub> (00 <sub>16</sub> ), 1EFF <sub>16</sub> (56 <sub>16</sub> )	1F00 <sub>16</sub> (00 <sub>16</sub> ), 1F01 <sub>16</sub> (A6 <sub>16</sub> )
20FE <sub>16</sub> (88 <sub>16</sub> ), 20FF <sub>16</sub> (57 <sub>16</sub> )	2100 <sub>16</sub> (12 <sub>16</sub> ), 2101 <sub>16</sub> (A7 <sub>16</sub> )
22FE <sub>16</sub> (00 <sub>16</sub> ), 22FF <sub>16</sub> (58 <sub>16</sub> )	2300 <sub>16</sub> (00 <sub>16</sub> ), 2301 <sub>16</sub> (A8 <sub>16</sub> )
24FE <sub>16</sub> (90 <sub>16</sub> ), 24FF <sub>16</sub> (59 <sub>16</sub> )	2500 <sub>16</sub> (09 <sub>16</sub> ), 2501 <sub>16</sub> (A9 <sub>16</sub> )
26FE <sub>16</sub> (48 <sub>16</sub> ), 26FF <sub>16</sub> (5A <sub>16</sub> )	2700 <sub>16</sub> (00 <sub>16</sub> ), 2701 <sub>16</sub> (AA <sub>16</sub> )
28FE <sub>16</sub> (24 <sub>16</sub> ), 28FF <sub>16</sub> (5B <sub>16</sub> )	2900 <sub>16</sub> (81 <sub>16</sub> ), 2901 <sub>16</sub> (AB <sub>16</sub> )
2AFE <sub>16</sub> (00 <sub>16</sub> ), 2AFF <sub>16</sub> (5C <sub>16</sub> )	2B00 <sub>16</sub> (18 <sub>16</sub> ), 2B01 <sub>16</sub> (AC <sub>16</sub> )
2CFE <sub>16</sub> (24 <sub>16</sub> ), 2CFF <sub>16</sub> (5D <sub>16</sub> )	2D00 <sub>16</sub> (00 <sub>16</sub> ), 2D01 <sub>16</sub> (AD <sub>16</sub> )
2EFE <sub>16</sub> (48 <sub>16</sub> ), 2EFF <sub>16</sub> (5E <sub>16</sub> )	2F00 <sub>16</sub> (42 <sub>16</sub> ), 2F01 <sub>16</sub> (AE <sub>16</sub> )
30FE <sub>16</sub> (00 <sub>16</sub> ), 30FF <sub>16</sub> (5F <sub>16</sub> )	3100 <sub>16</sub> (24 <sub>16</sub> ), 3101 <sub>16</sub> (AF <sub>16</sub> )
32FE <sub>16</sub> (48 <sub>16</sub> ), 32FF <sub>16</sub> (50 <sub>16</sub> )	3300 <sub>16</sub> (00 <sub>16</sub> ), 3301 <sub>16</sub> (B0 <sub>16</sub> )
34FE <sub>16</sub> (90 <sub>16</sub> ), 34FF <sub>16</sub> (51 <sub>16</sub> )	3500 <sub>16</sub> (81 <sub>16</sub> ), 3501 <sub>16</sub> (B1 <sub>16</sub> )
36FE <sub>16</sub> (00 <sub>16</sub> ), 36FF <sub>16</sub> (52 <sub>16</sub> )	3700 <sub>16</sub> (0C <sub>16</sub> ), 3701 <sub>16</sub> (B2 <sub>16</sub> )
38FE <sub>16</sub> (01 <sub>16</sub> ), 38FF <sub>16</sub> (53 <sub>16</sub> )	3900 <sub>16</sub> (06 <sub>16</sub> ), 3901 <sub>16</sub> (B3 <sub>16</sub> )
3AFE <sub>16</sub> (80 <sub>16</sub> ), 3AFF <sub>16</sub> (54 <sub>16</sub> )	3B00 <sub>16</sub> (00 <sub>16</sub> ), 3B01 <sub>16</sub> (B4 <sub>16</sub> )

**2** : The character code "09<sub>16</sub>" is used for "transparent space" when displaying Closed Caption.

Therefore, set "00<sub>16</sub>" to the 40-byte addresses corresponding to the character code "09<sub>16</sub>."

<Transparent space font data storing area>

■ M3727GM6/M8-XXXSP/FP, M37272E8SP/FP

addresses 1000<sub>16</sub> + (4 + 2n) X 100<sub>16</sub> + 12<sub>16</sub> to

1000<sub>16</sub> + (4 + 2n) X 100<sub>16</sub> + 13<sub>16</sub>

(n = 0 to 19)

[	addresses 1412 <sub>16</sub> and 1413 <sub>16</sub>
	addresses 1612 <sub>16</sub> and 1613 <sub>16</sub>
	⋮
	addresses 3812 <sub>16</sub> and 3813 <sub>16</sub>
	addresses 3A12 <sub>16</sub> and 3A13 <sub>16</sub>

## (2) OSD RAM

The RAM for OSD is allocated at addresses 0800<sub>16</sub> to 087F<sub>16</sub>, and is divided into a display character code specification part, color code 1 specification part, and color code 2 specification part for each block. Table 8.11.3 shows the contents of the OSD RAM.

For example, to display 1 character position (the left edge) in block 1, write the character code in address 0800<sub>16</sub>, write the color code 1 at 0820<sub>16</sub>.

The structure of the OSD RAM is shown in Figure 8.11.16.

**Table 8.11.3 Contents of OSD RAM**

Block	Display Position (from left)	Character Code Specification	Color Code Specification
Block 1	1st character	0800 <sub>16</sub>	0820 <sub>16</sub>
	2nd character	0801 <sub>16</sub>	0821 <sub>16</sub>
	3rd character	0802 <sub>16</sub>	0822 <sub>16</sub>
	⋮	⋮	⋮
	30th character	081D <sub>16</sub>	083D <sub>16</sub>
	31st character	081E <sub>16</sub>	083E <sub>16</sub>
Block 2	32nd character	081F <sub>16</sub>	083F <sub>16</sub>
	1st character	0840 <sub>16</sub>	0860 <sub>16</sub>
	2nd character	0841 <sub>16</sub>	0861 <sub>16</sub>
	3rd character	0842 <sub>16</sub>	0862 <sub>16</sub>
	⋮	⋮	⋮
	30th character	085D <sub>16</sub>	087D <sub>16</sub>
	31st character	085E <sub>16</sub>	087E <sub>16</sub>
32nd character	085F <sub>16</sub>	087F <sub>16</sub>	

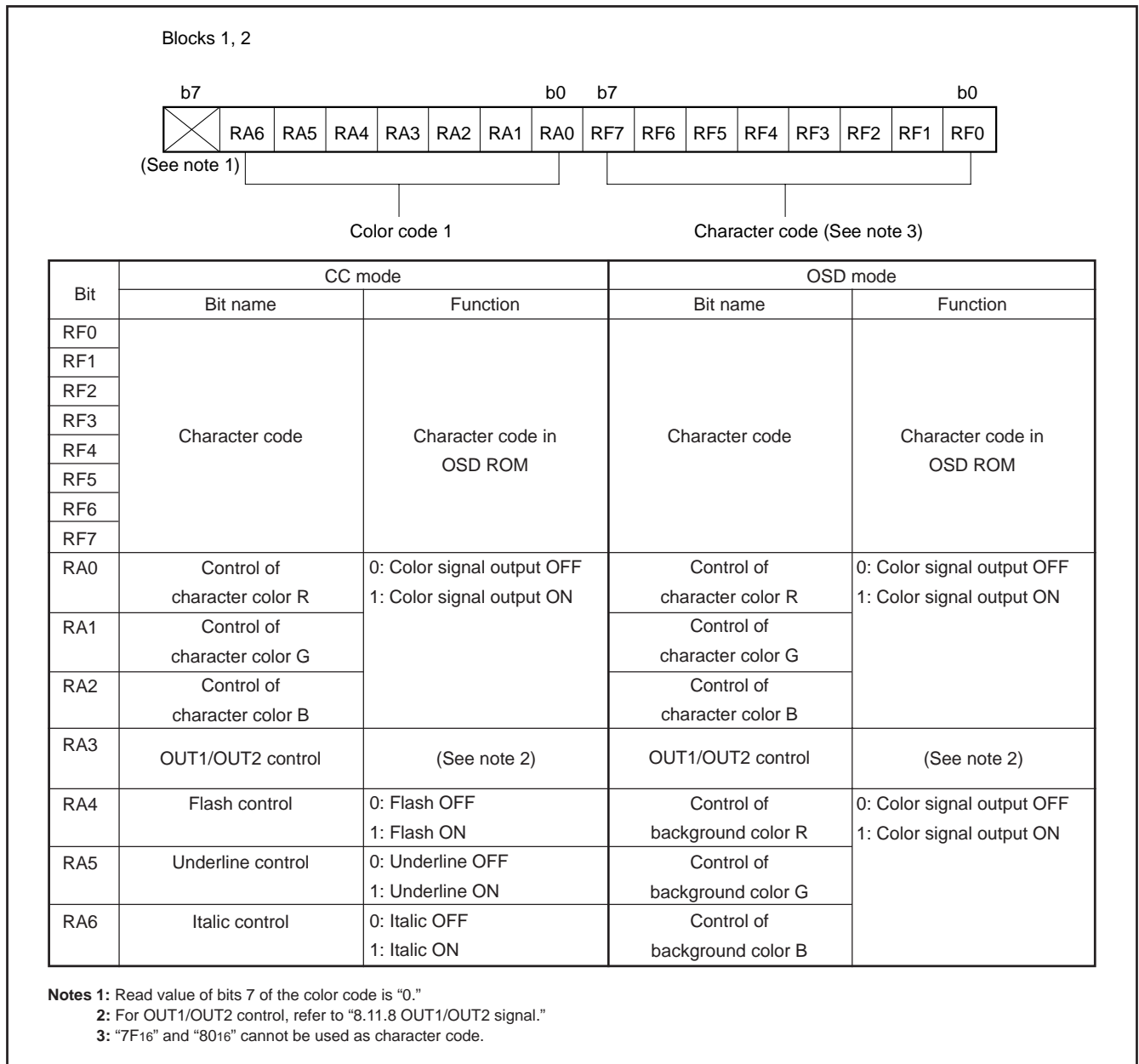


Fig. 8.11.16 Bit structure of OSD RAM

### 8.11.6 Character color

The color for each character is displayed by the color code.

<7 kinds>

Specified by bits 0 (R), 1 (G), and 2 (B) of the color code

### 8.11.7 Character background color

The character background color can be displayed in the character display area only in the OSD mode. The character background color for each character is specified by the color code.

<7 kinds>

Specified by bits 4 (R), 5 (G), and 6 (B) of the color code

**Note** : The character background color is displayed in the following part :  
(character display area)–(character font)–(border).  
Accordingly, the character background color does not mix with these color signal.

### 8.11.8 OUT1, OUT2 signals

The OUT1, OUT2 signals are used to control the luminance of the video signal. The output waveform of the OUT1, OUT2 signals is controlled by display mode, bit 5 of the block control register i (refer to Figure 8.11.4) and RA3 of OSD RAM. The setting values for

controlling OUT1, OUT2 and the corresponding output waveform is shown in Figure 8.11.17.

**Note :** When OUT2 signal is output, set bit 7 of OSD port control register (refer to Figure 8.11.28) to "1."

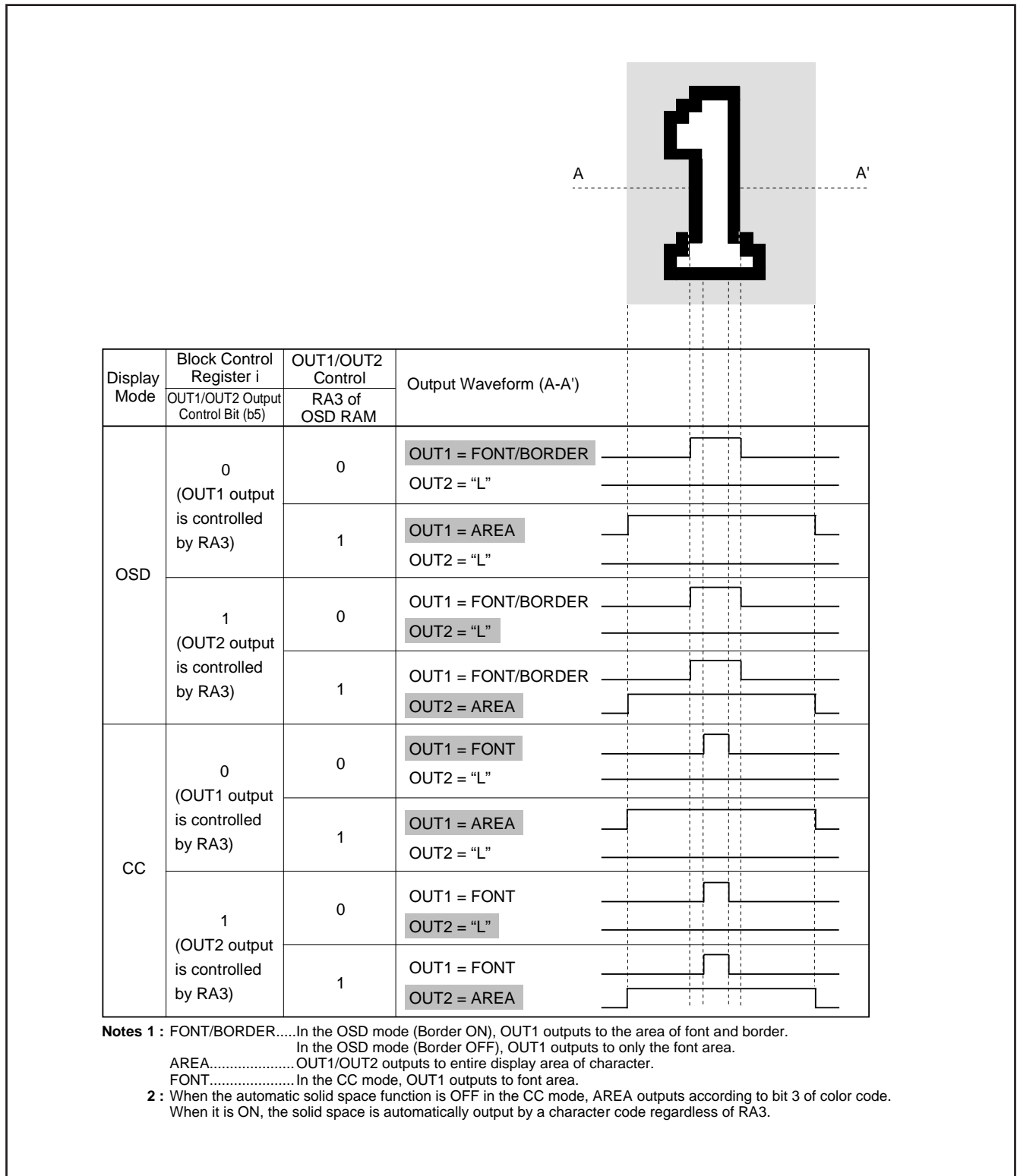


Fig. 8.11.17 Setting Value for Controlling OUT1, OUT2 and Corresponding Output Waveform

### 8.11.9 Attribute

The attributes (border, flash, underline, italic) are controlled to the character font. The attributes to be controlled are different depending on each mode.

CC mode ..... Flash, underline, italic (per character unit)

OSD mode ..... Border (per character unit)

#### (1) Under line

The underline is output at the 23th and 24th dots in vertical direction only in the CC mode. The underline is controlled by RA5 of OSD RAM. The color of underline is the same color as that of the character font.

#### (2) Flash

The character font and the underline are flashed only in the CC mode. The flash is controlled by RA4 of OSD RAM. As for character font part, the character output part is flashed, the character background part is not flashed. The flash cycle bases on the VSYNC count.

- VSYNC cycle  $\times 48 \approx 800$  ms (at display ON)
- VSYNC cycle  $\times 16 \approx 267$  ms (at display OFF)

#### (3) Italic

The italic is made by slanting the font stored in OSD ROM to the right only in the CC mode. The italic is controlled by RA6 of OSD RAM.

The display example of the italic and underline is shown in Figure 8.11.8. In this case, "R" is displayed.

- Notes 1:** When setting both the italic and the flash, the italic character flashes.
- 2:** The boundary of character color is displayed in italic. However, the boundary of character background color is not affected by the italic (refer to Figure 8.11.19).
- 3:** The adjacent character (one side or both side) to an italic character is displayed in italic even when the character is not specified to display in italic (refer to Figure 8.11.19).

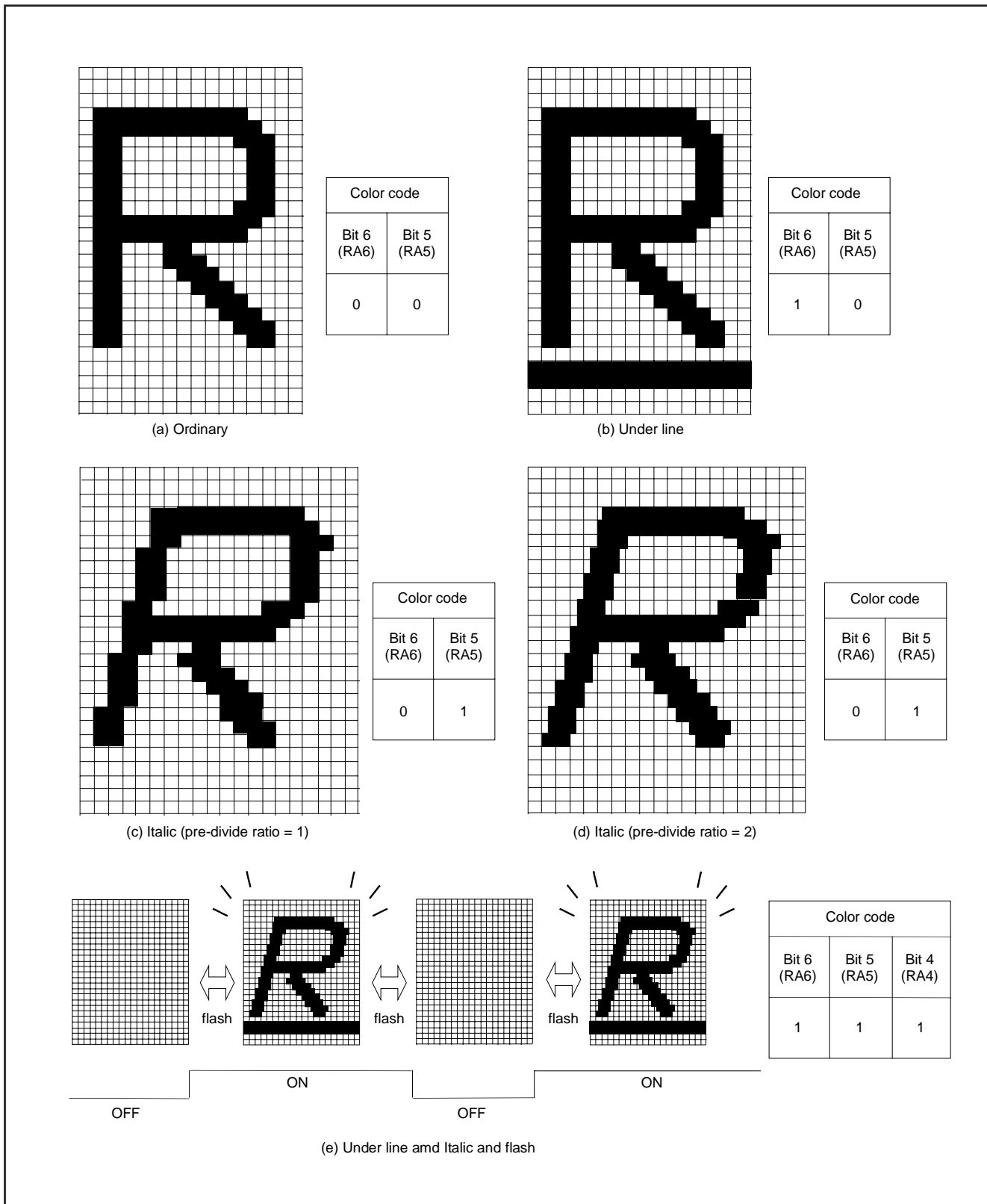


Fig. 8.11.18 Example of Attribute Display (in CC Mode)

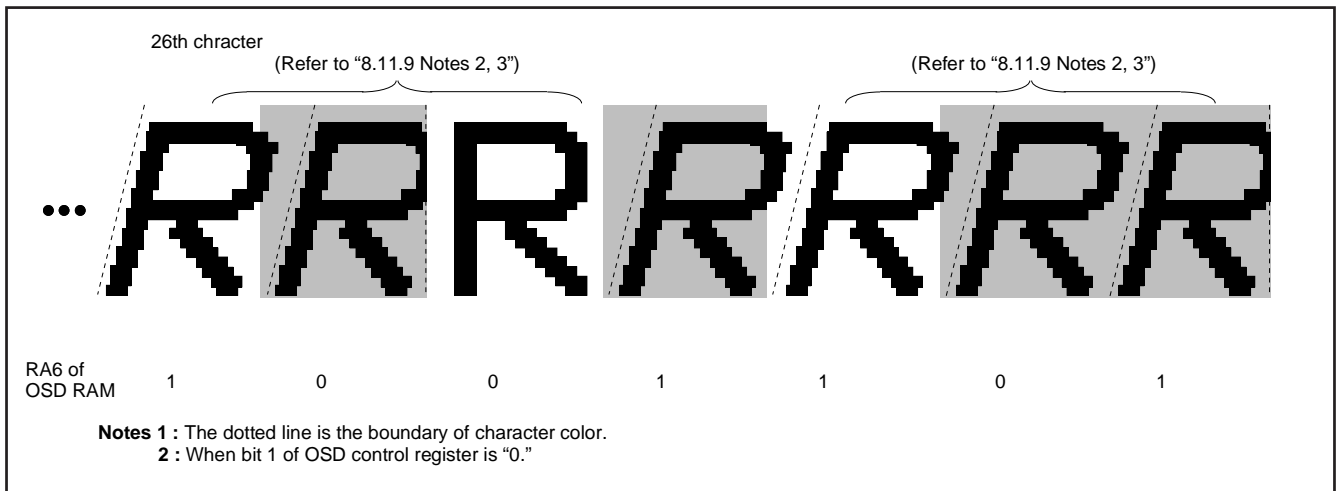


Fig. 8.11.19 Example of Italic Display



#### (4) Border

The border is output around of character font (all bordered) in the OSD mode. The border ON/OFF is controlled by bit 0 and 1 of the block control register i (refer to Figure 8.11.4). The OUT1 signal is used for border output. The horizontal size (x) of border is 1Tc (OSD clock cycle divided in pre-divide circuit) regardless of the character font dot size. The vertical size (y) different depending on the screen scan mode and the vertical dot size of character font.

- Notes 1 : The border dot area is the shaded area as shown in Figure 8.11.20.
- 2 : When the border dot overlaps on the next character font, the character font has priority (refer to Figure 8.11.22 A).  
When the border dot overlaps on the next character back ground, the border has priority (refer to Figure 8.11.22 B).
- 3 : The border in vertical out of character area is not displayed (refer to Figure 8.11.22).

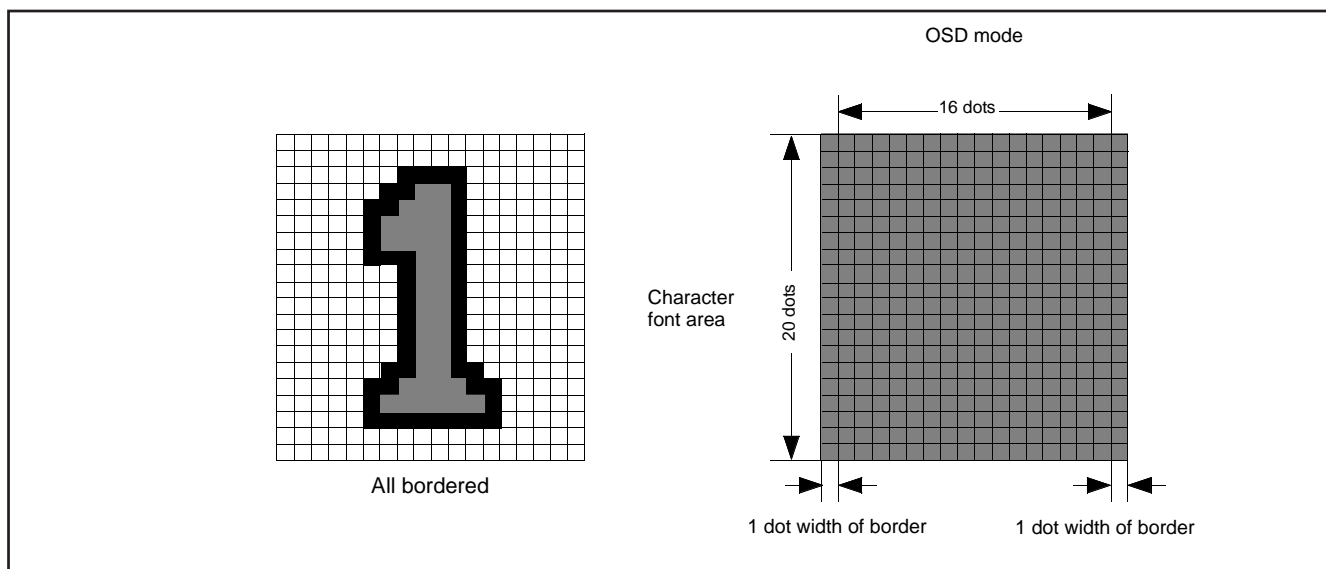


Fig. 8.11.20 Example of Border Display

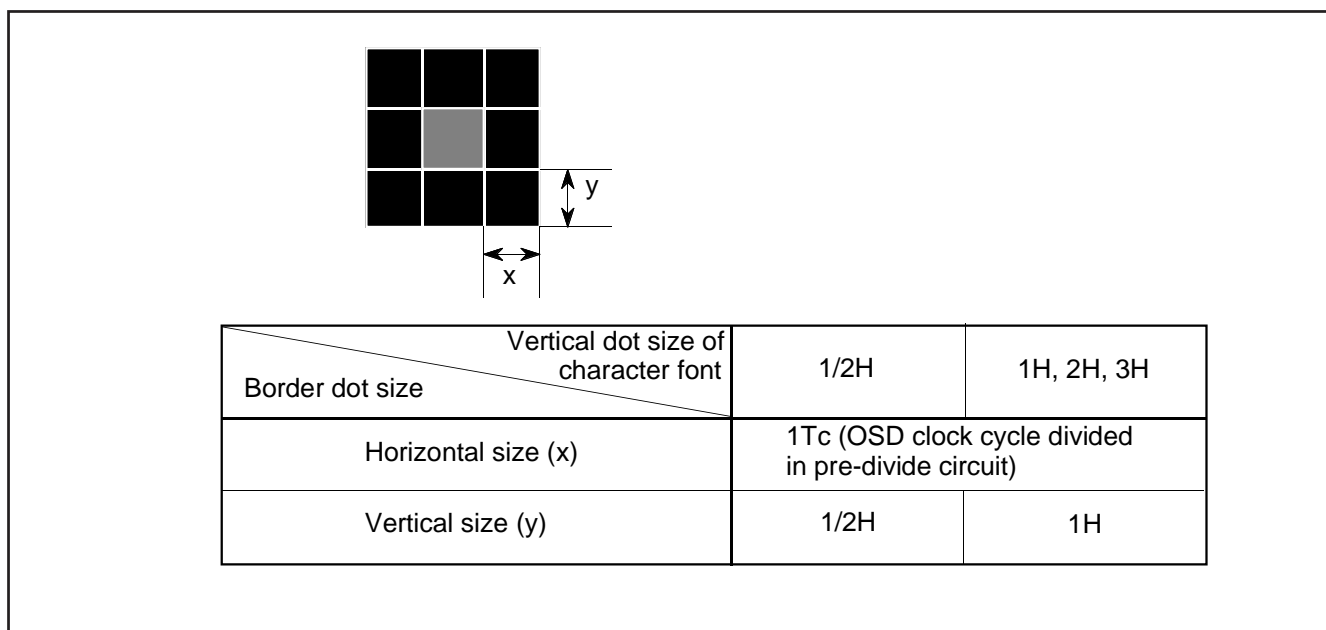


Fig. 8.11.21 Horizontal and Vertical Size of Border

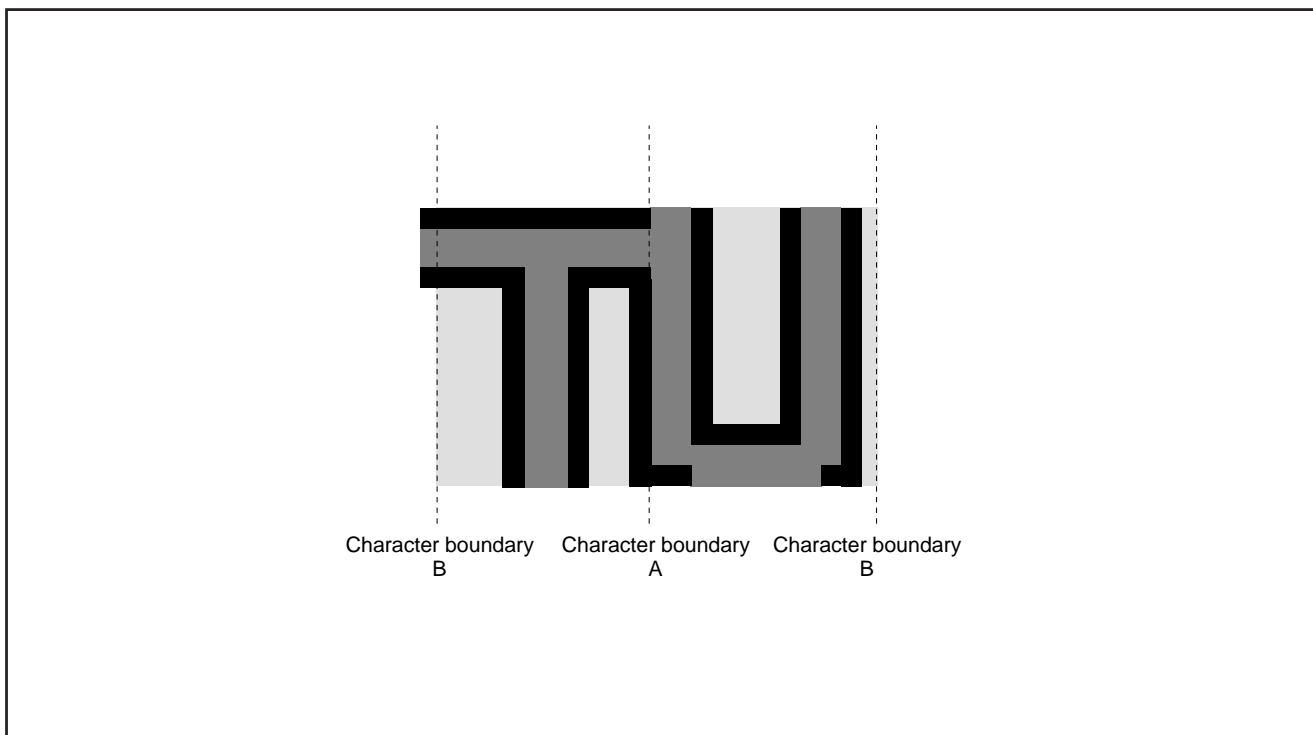


Fig. 8.11.22 Border Priority

### 8.11.10 Multiline Display

This microcomputer can ordinarily display 2 lines on the CRT screen by displaying 2 blocks at different vertical positions. In addition, it can display up to 16 lines by using OSD interrupts.

An OSD interrupt request occurs at the point at which display of each block has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical position registers) of a certain block, the character display of that block starts, and an interrupt occurs at the point at which the scanning line exceeds the block.

- Notes 1:** An OSD interrupt does not occur at the end of display when the block is not displayed. In other words, if a block is set to off display by the display control bit of the block control register (addresses 00D216, 00D316), an OSD interrupt request does not occur (refer to Figure 8.11.23 (A)).
- 2:** When another block display appears while one block is displayed, an OSD interrupt request occurs only once at the end of the another block display (refer to Figure 8.11.23 (B)).
- 3:** On the screen setting window, an OSD interrupt occurs even at the end of the CC mode block (off display) out of window (refer to Figure 8.11.23 (C)).

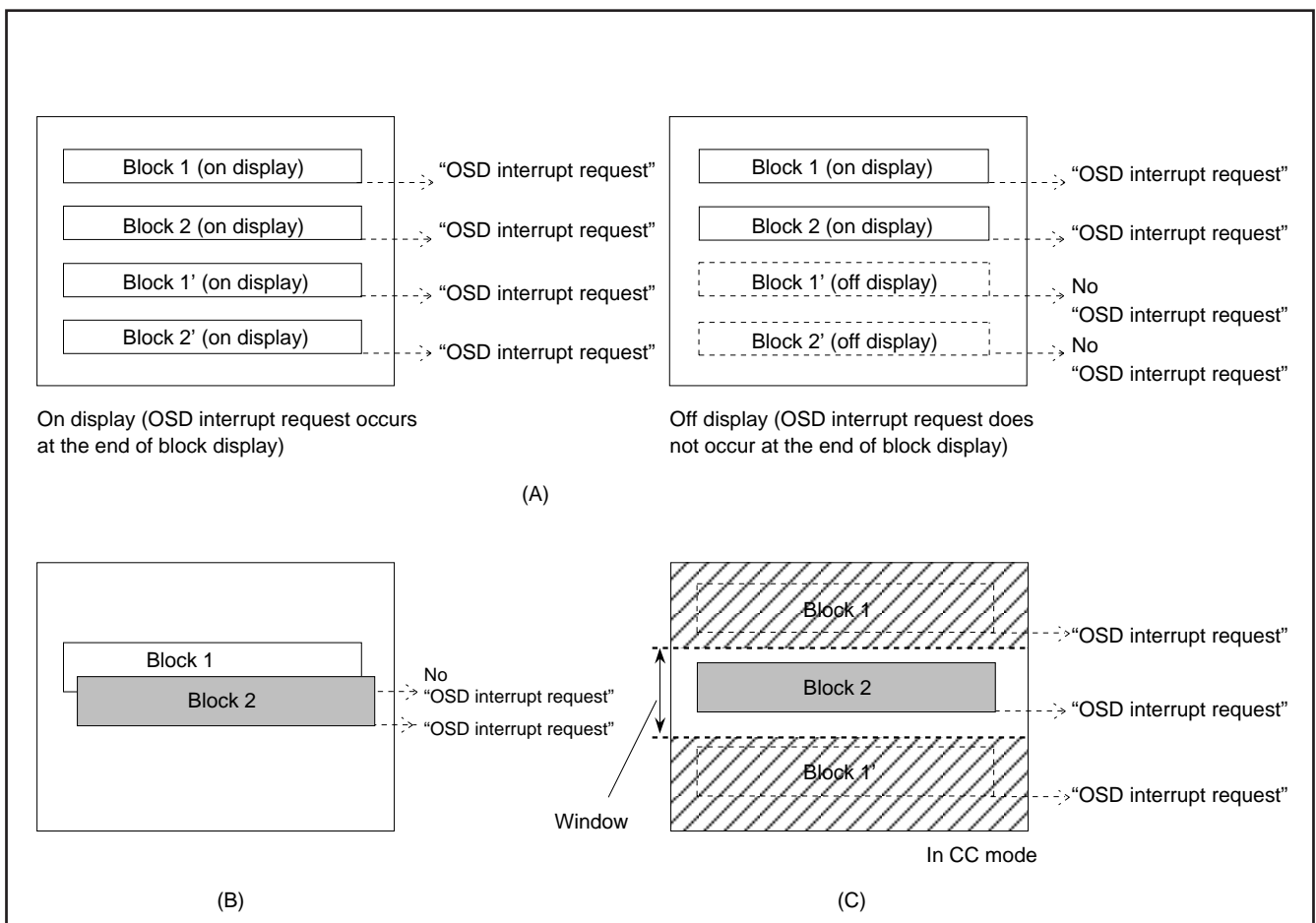


Fig. 8.11.23 Note on Occurrence of OSD Interrupt

### 8.11.11 Automatic Solid Space Function

This function generates automatically the solid space (OUT1 or OUT2 blank output) of the character area in the CC mode.

The solid space is output in the following area :

- Any character area except character code "09<sub>16</sub>"
  - Character area on the left and right sides of the above character
- This function is turned on and off by bit 1 of the OSD control register (refer to Figure 8.11.3).

**Notes :** The character code "09<sub>16</sub>" is used for "transparent space" when displaying Closed Caption. Therefore, set "00<sub>16</sub>" to the 40-byte addresses corresponding to the character code "09<sub>16</sub>".

<Transparent space font data storing area>  
 ■ M3727GM6/M8-XXXSP/FP, M37272E8SP/FP  
 addresses 1000<sub>16</sub> + (4 + 2n) × 100<sub>16</sub> + 12<sub>16</sub> to  
 1000<sub>16</sub> + (4 + 2n) × 100<sub>16</sub> + 13<sub>16</sub>  
 (n = 0 to 19)

[ addresses 1412<sub>16</sub> and 1413<sub>16</sub>  
 addresses 1612<sub>16</sub> and 1613<sub>16</sub>  
 ⋮  
 addresses 3812<sub>16</sub> and 3813<sub>16</sub>  
 addresses 3A12<sub>16</sub> and 3A13<sub>16</sub> ]

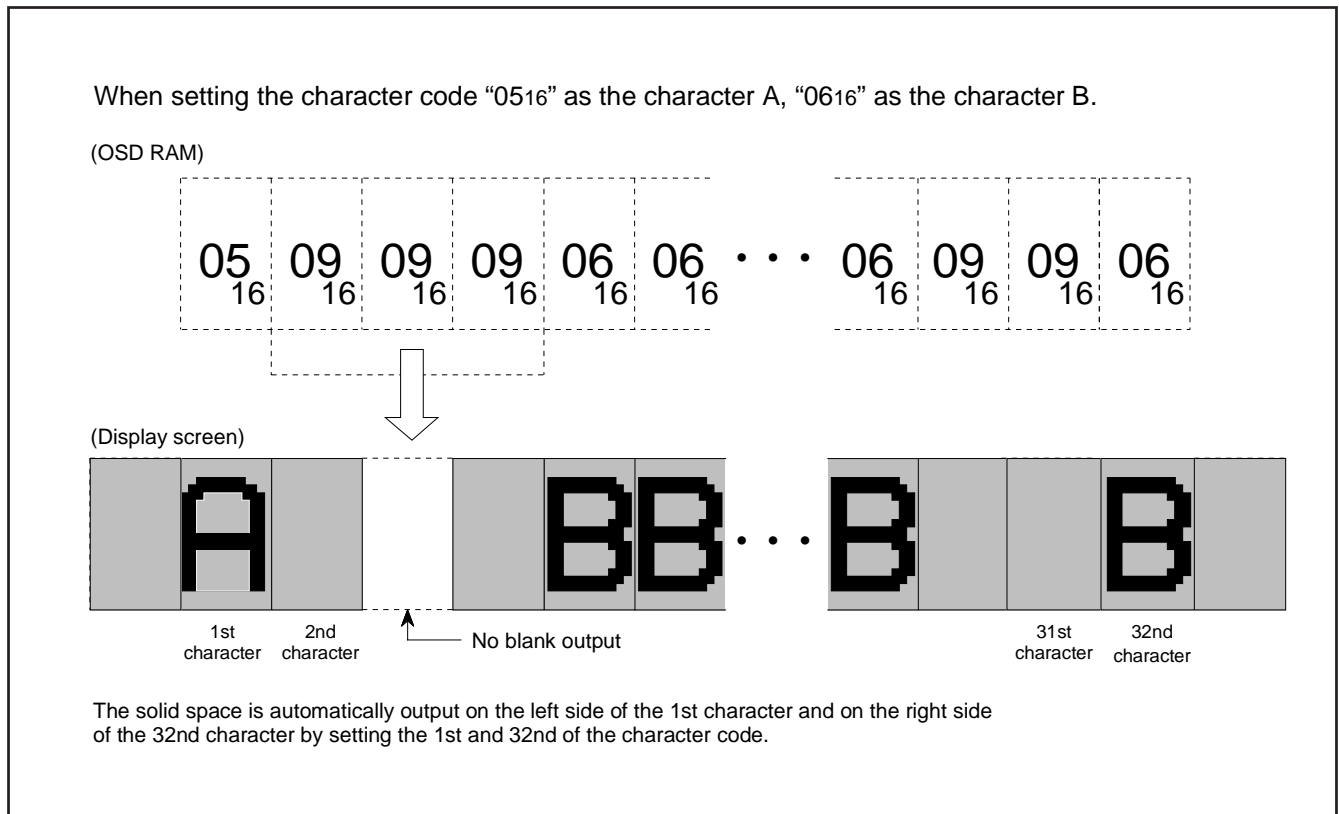


Fig. 8.11.24 Display Screen Example of Automatic Solid Space

### 8.11.12 Window Function

This function sets the top and bottom boundary of display limit on a screen. The window function is valid only in the CC mode. The top boundary is set by the window registers 1 and bit 7 of block control register 1. The bottom boundary is set by window registers 1 and bit 7 of block control register 2. This function is turned on and off by bit 2 of the OSD control register (refer to Figure 8.11.3).

The window registers 1 and 2 is shown in Figures 8.11.26 and 8.11.27.

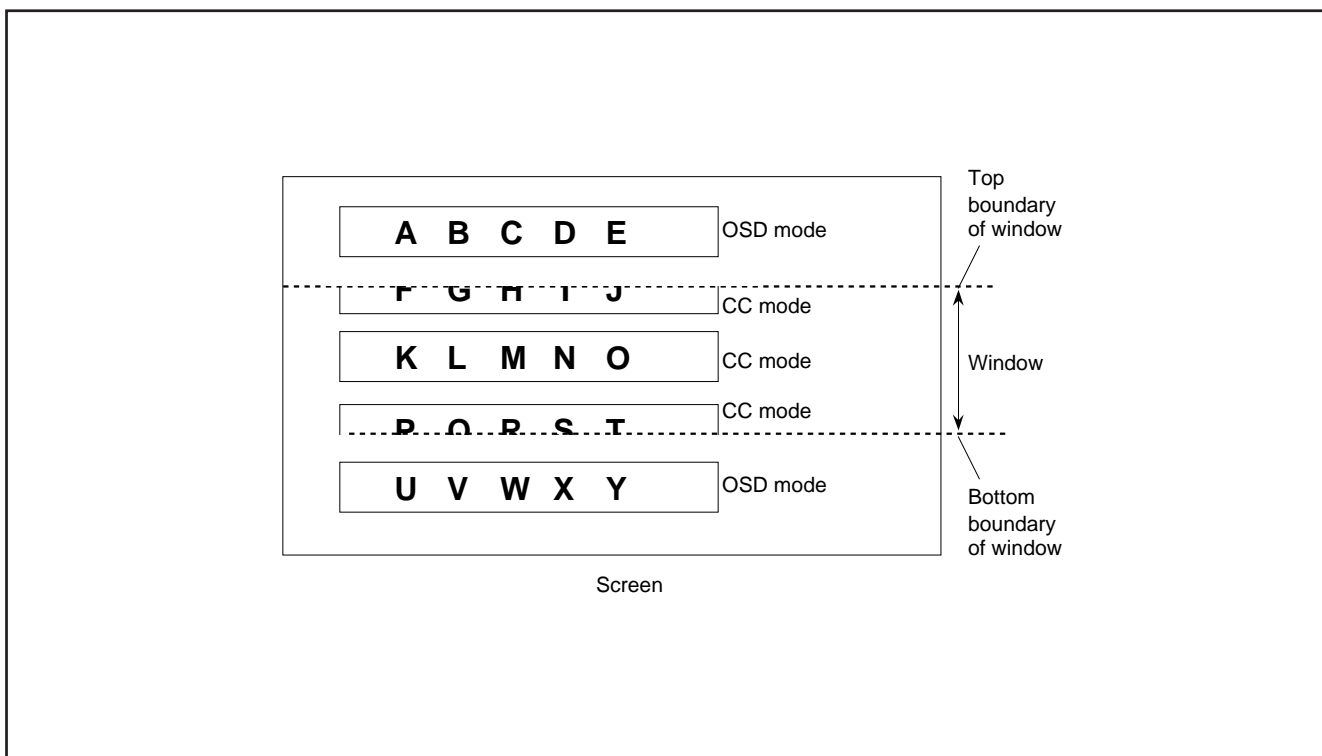


Fig. 8.11.25 Example of Window Function

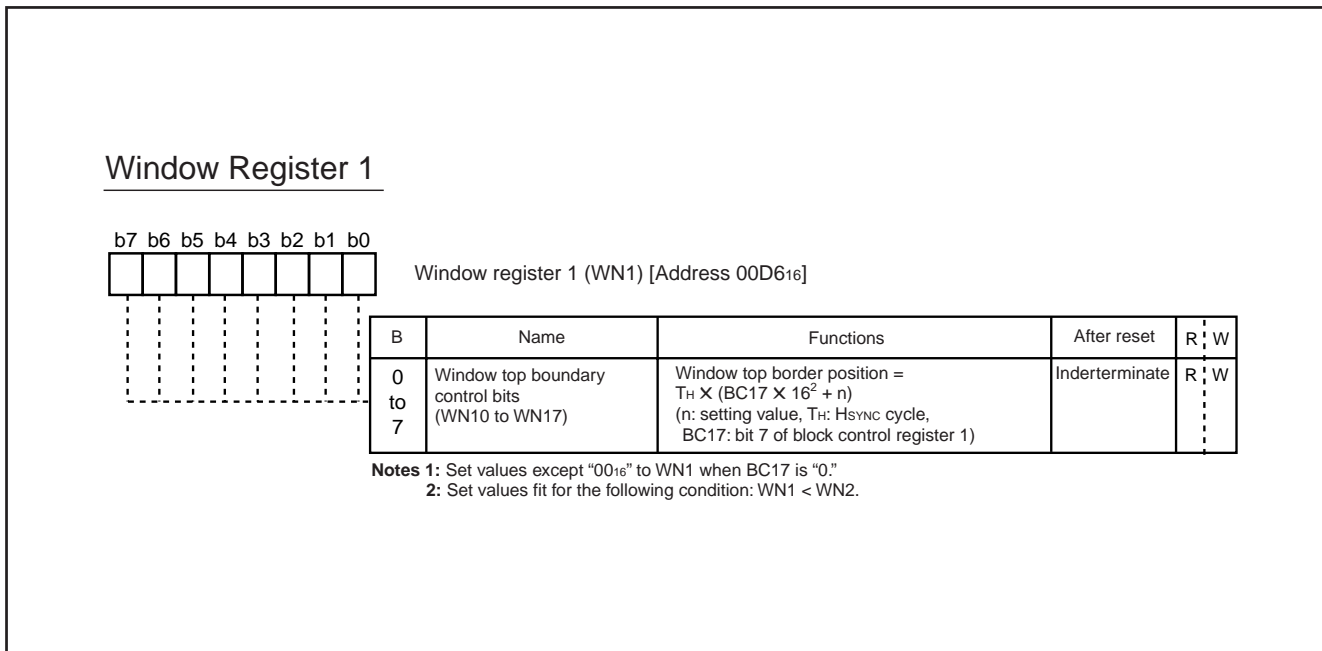


Fig. 8.11.26 Window Register 1

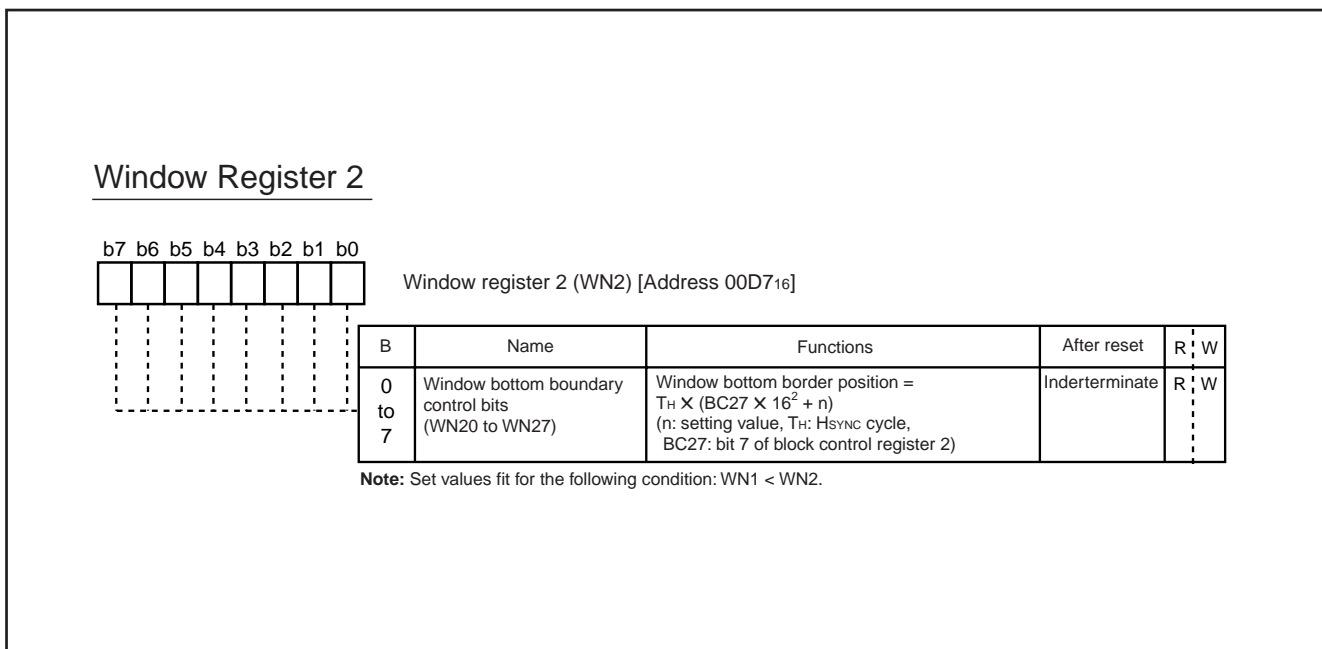


Fig. 8.11.27 Window Register 2

### 8.11.13 OSD Output Pin Control

The OSD output pins R, G, B and OUT1 can also function as ports P52–P55. Set corresponding bit of the OSD port control register (address 00CB16) to “0” to specify these pins as OSD output pins, or set it to “1” to specify it as a general-purpose port P5.

The OUT2 can also function as port P10. Set bit 0 of the port P1 direction register (address 00C316) to “1” (output mode). After that, set bit 7 of the OSD port control register to “1” to specify the pin as OSD output pin, or set it to “0” to specify as port P10.

The input polarity of the HSYNC, VSYNC and output polarity of signals R, G, B, OUT1 and OUT2 can be specified with the I/O polarity control register (address 00D8) . Set a bit to “0” to specify positive polarity; set it to “1” to specify negative polarity (refer to Figure 8.11.13).

The structure of the OSD port control register is shown in Figure 8.11.28.

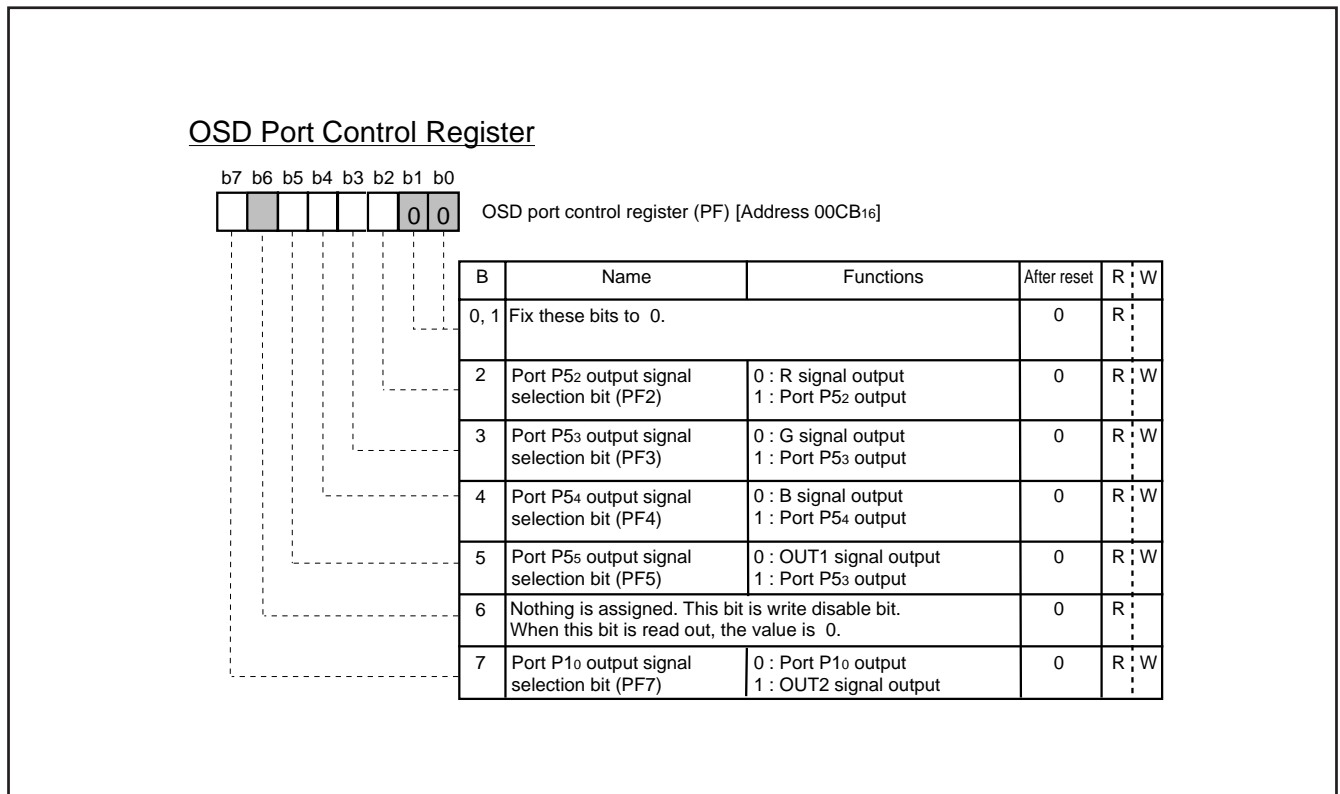


Fig. 8.11.28 OSD Port Control Register

### 8.11.14 Raster Coloring Function

An entire screen (raster) can be colored by setting the bits 4 to 0 of the raster color register. Since each of the R, G, B, OUT1, and OUT2 pins can be switched to raster coloring output, 8 raster colors can be obtained.

When the character color/the character background color overlaps with the raster color, the color (R, G, B, OUT1, OUT2), specified for the character color/the character background color, takes priority of the raster color. This ensures that character color/character background color is not mixed with the raster color.

The raster color register is shown in Figure 8.11.29, the example of raster coloring is shown in Figure 8.11.30.

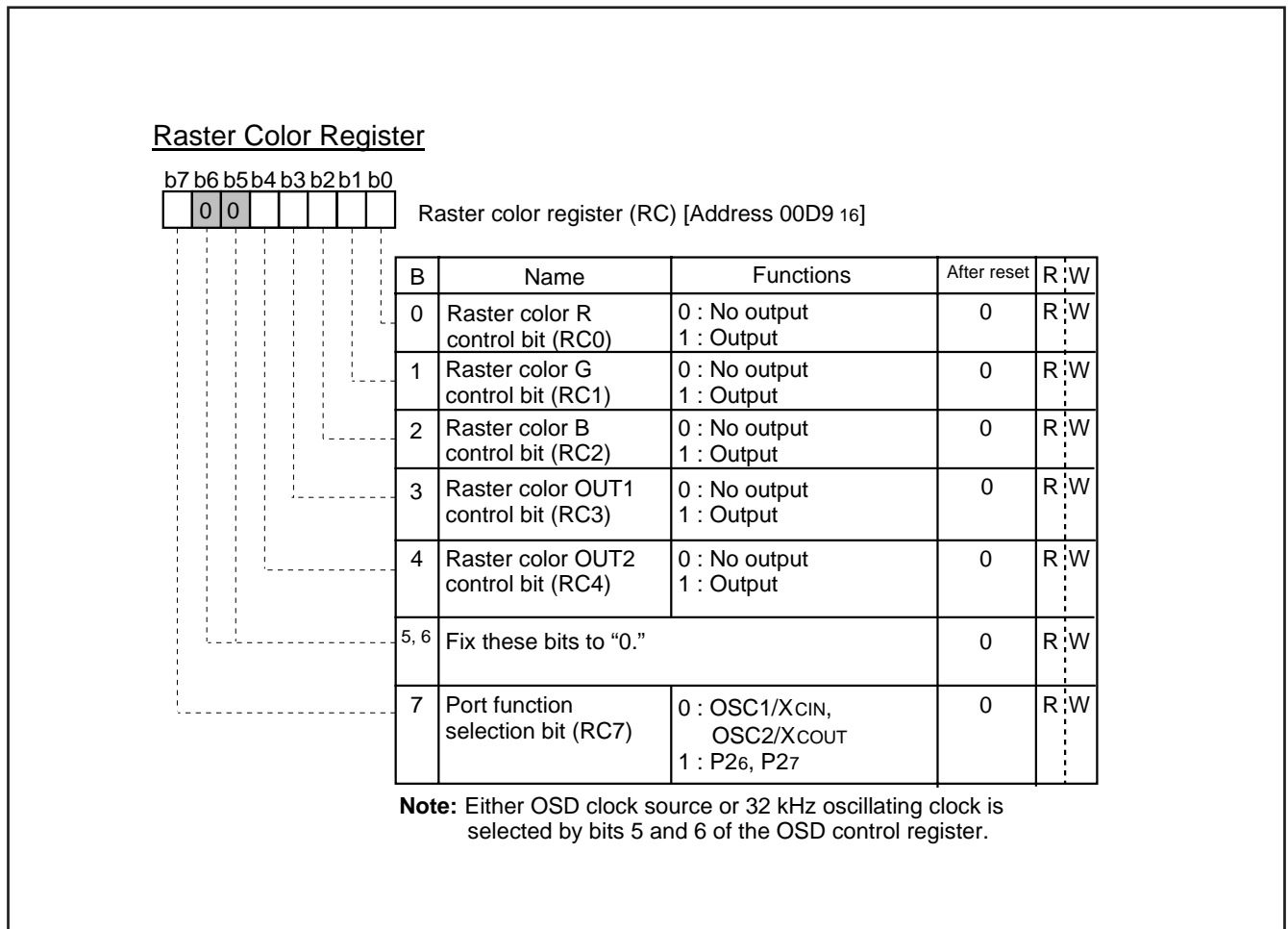


Fig. 8.11.29 Raster Color Register



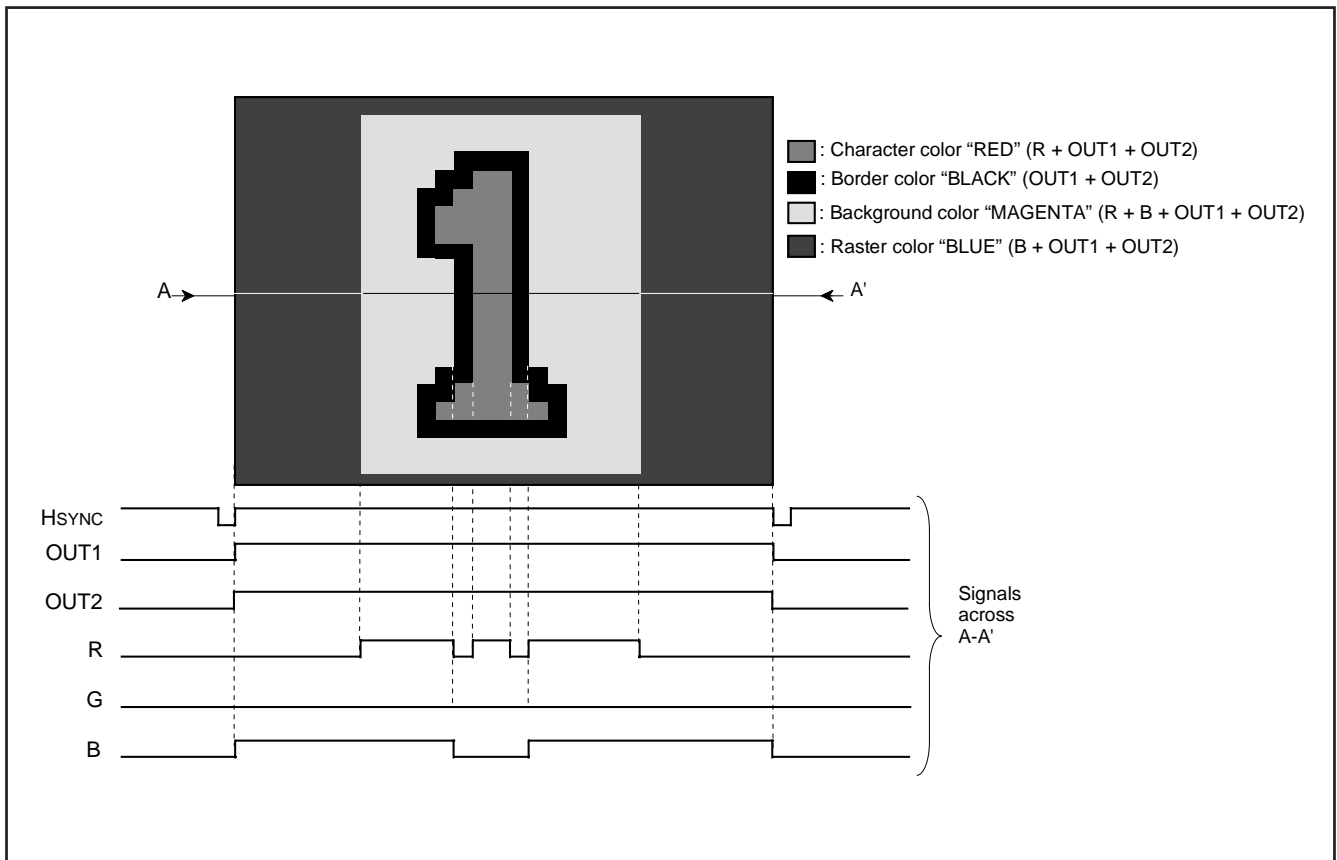


Fig. 8.11.30 Example of Raster Coloring

### 8.12 SOFTWARE RUNAWAY DETECT FUNCTION

This microcomputer has a function to decode undefined instructions to detect a software runaway.

When an undefined op-code is input to the CPU as an instruction code during operation, the following processing is done.

- ① The CPU generates an undefined instruction decoding signal.
- ② The device is internally reset because of occurrence of the undefined instruction decoding signal.
- ③ As a result of internal reset, the same reset processing as in the case of ordinary reset operation is done, and the program restarts from the reset vector.

Note, however, that the software runaway detecting function cannot be invalid.

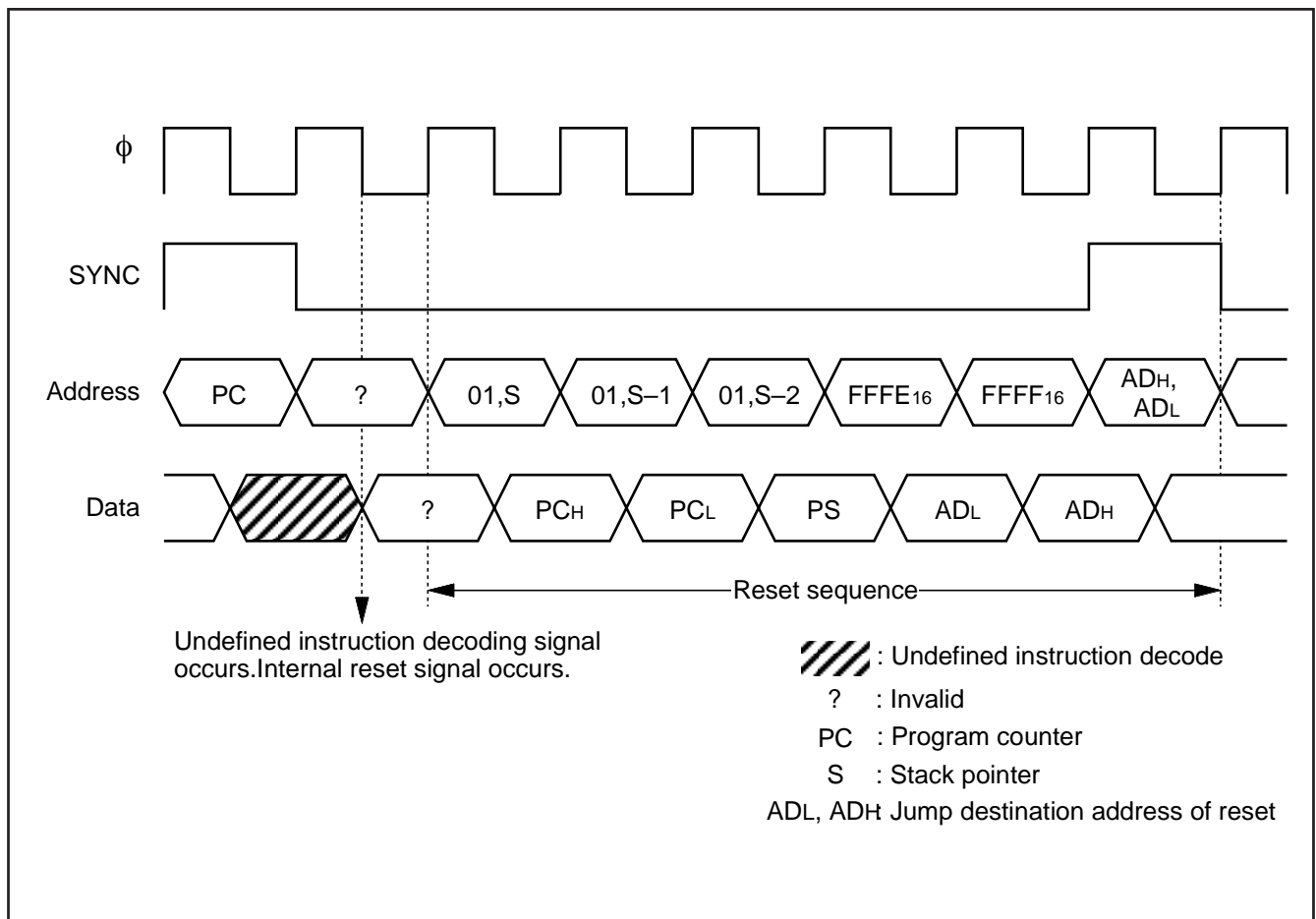


Fig.8.12.1 Sequence at Detecting Software Runaway Detection

### 8.13. RESET CIRCUIT

When the oscillation of a quartz-crystal oscillator or a ceramic resonator is stable and the power source voltage is  $5\text{ V} \pm 10\%$ , hold the  $\overline{\text{RESET}}$  pin at LOW for  $2\ \mu\text{s}$  or more, then return it to HIGH. Then, as shown in Figure 8.13.2, reset is released and the program starts from the address formed by using the content of address  $\text{FFFF}_{16}$  as the high-order address and the content of the address  $\text{FFFE}_{16}$  as the low-order address. The internal state of microcomputer at reset are shown in Figures 8.2.3 to 8.2.6.

An example of the reset circuit is shown in Figure 8.13.1. The reset input voltage must be kept  $0.9\text{ V}$  or less until the power source voltage surpasses  $4.5\text{ V}$ .

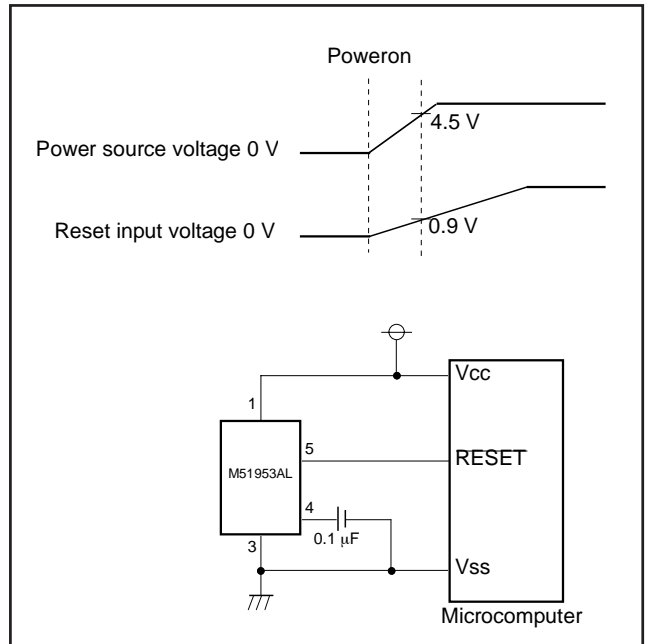


Fig.8.13.1 Example of Reset Circuit

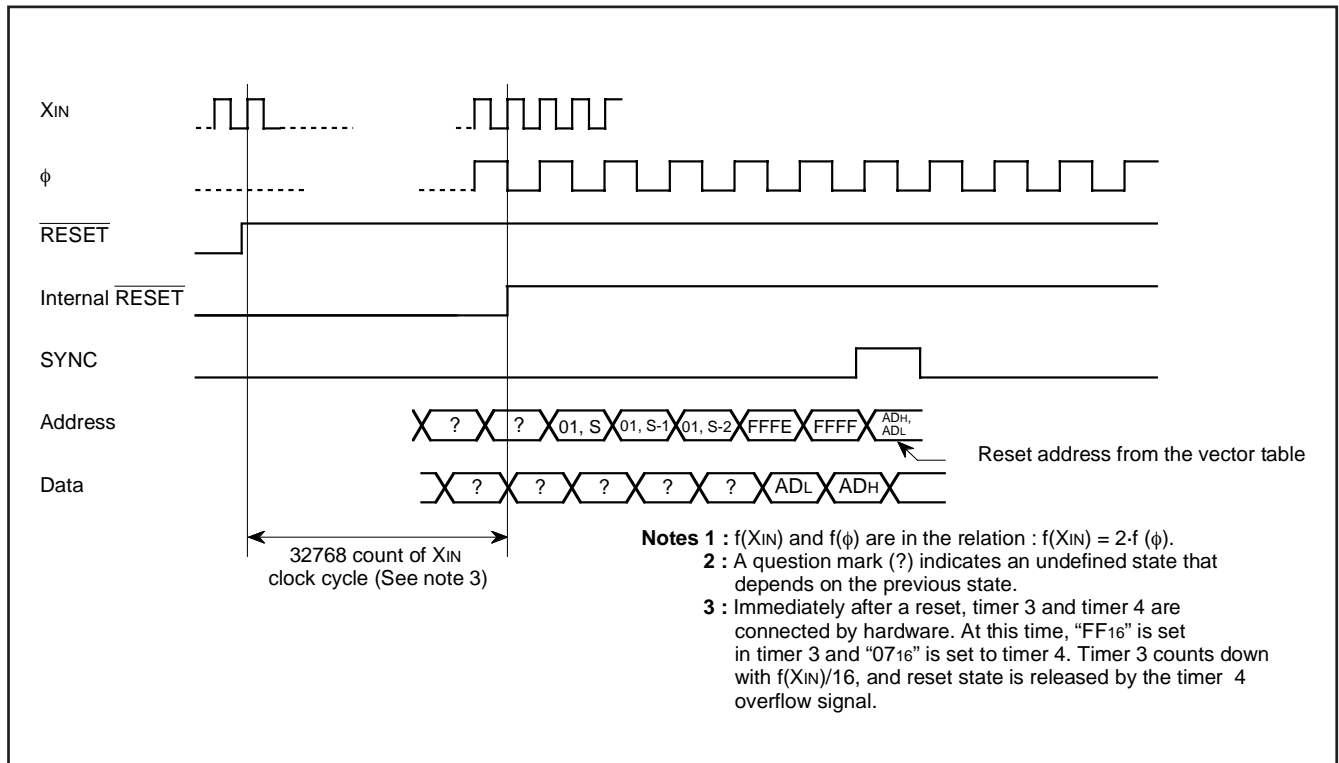


Fig.8.13.2 Reset Sequence

## 8.14 CLOCK GENERATING CIRCUIT

This microcomputer has 2 built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT. When using XCIN-XCOUT as sub-clock, clear bits 5 and 6 of the OSD control register to "0." To supply a clock signal externally, input it to the XIN (XCIN) pin and make the XOUT (XCOUT) pin open. When not using XCIN clock, connect the XCIN to Vss and make the XCOUT pin open.

After reset has completed, the internal clock  $\phi$  is half the frequency of XIN. Immediately after power on, both the XIN and XCIN clock start oscillating. To set the internal clock  $\phi$  to low-speed operation mode, set bit 7 of the CPU mode register to "1."

### 8.14.1 OSCILLATION CONTROL

#### (1) Stop Mode

The built-in clock generating circuit is shown in Figure 120. When the STP instruction is executed, the internal clock  $\phi$  stops at HIGH. At the same time, timers 3 and 4 are connected by hardware and "FF16" is set in timer 3 and "0716" is set in timer 4. Select  $f(XIN)/16$  or  $f(XCIN)/16$  as the timer 3 count source (set both bit 0 of the timer mode register 2 and bit 6 at address 00C716 to "0" before the execution of the STP instruction). Moreover, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction. The oscillator restarts when external interrupt is accepted. However, the internal clock  $\phi$  keeps its HIGH level until timer 4 overflows, allowing time for oscillation stabilization when a ceramic resonator or a quartz-crystal oscillator is used.

#### (2) Wait Mode

When the WIT instruction is executed, the internal clock  $\phi$  stops in the HIGH level but the oscillator continues running. This wait state is released at reset or when an interrupt is accepted (See note). Since the oscillator does not stop, the next instruction can be executed at once.

**Note:** In the wait mode, the following interrupts are invalid.

- VSYNC interrupt
- OSD interrupt
- All timer interrupts using external clock input from port pin as count source
- All timer interrupts using  $f(XIN)/2$  or  $f(XCIN)/2$  as count source
- All timer interrupts using  $f(XIN)/4096$  or  $f(XCIN)/4096$  as count source
- $f(XIN)/4096$  interrupt
- Multi-master I<sup>2</sup>C-BUS interface interrupt
- Data slicer interrupt
- A-D conversion interrupt

#### (3) Low-speed Mode

If the internal clock is generated from the sub-clock (XCIN), a low power consumption operation can be realized by stopping only the main clock XIN. To stop the main clock, set bit 6 (CM6) of the CPU mode register (00FB16) to "1." When the main clock XIN is restarted, the program must allow enough time to for oscillation to stabilize.

Note that in low-power-consumption mode the XCIN-XCOUT drivability can be reduced, allowing even lower power consumption. To reduce the XCIN-XCOUT drivability, clear bit 5 (CM5) of the CPU mode register (00FB16) to "0." At reset, this bit is set to "1" and strong drivability is selected to help the oscillation to start. When an STP instruction is executed, set this bit to "1" by software before executing.

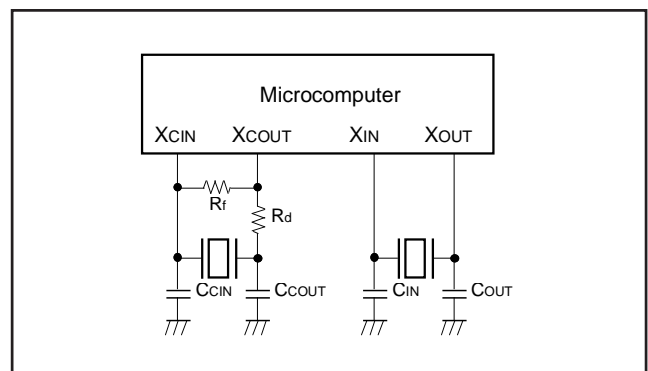


Fig.8.14.1 Ceramic Resonator Circuit Example

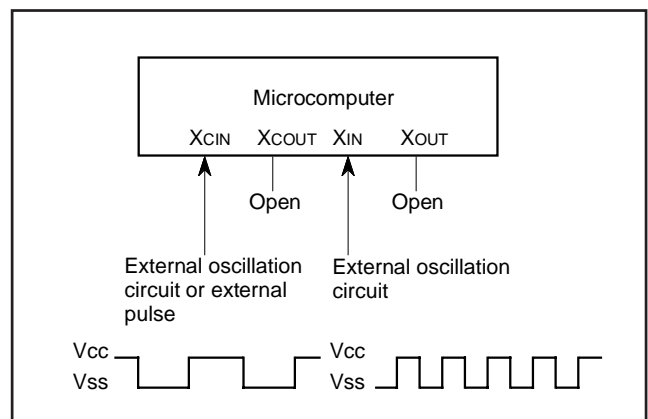


Fig.8.14.2 External Clock Input Circuit Example

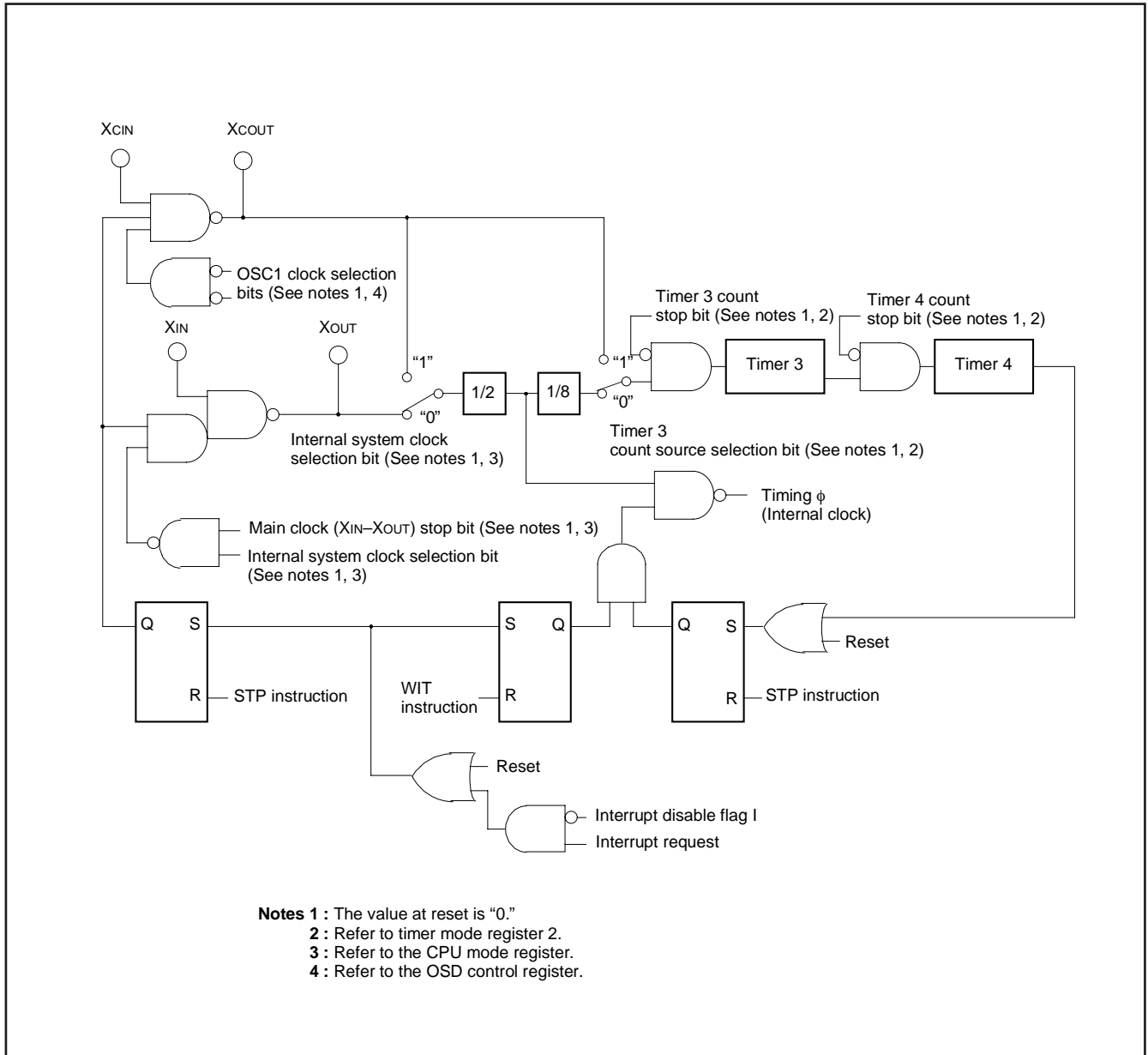


Fig.8.14.3 Clock Generating Circuit Block Diagram

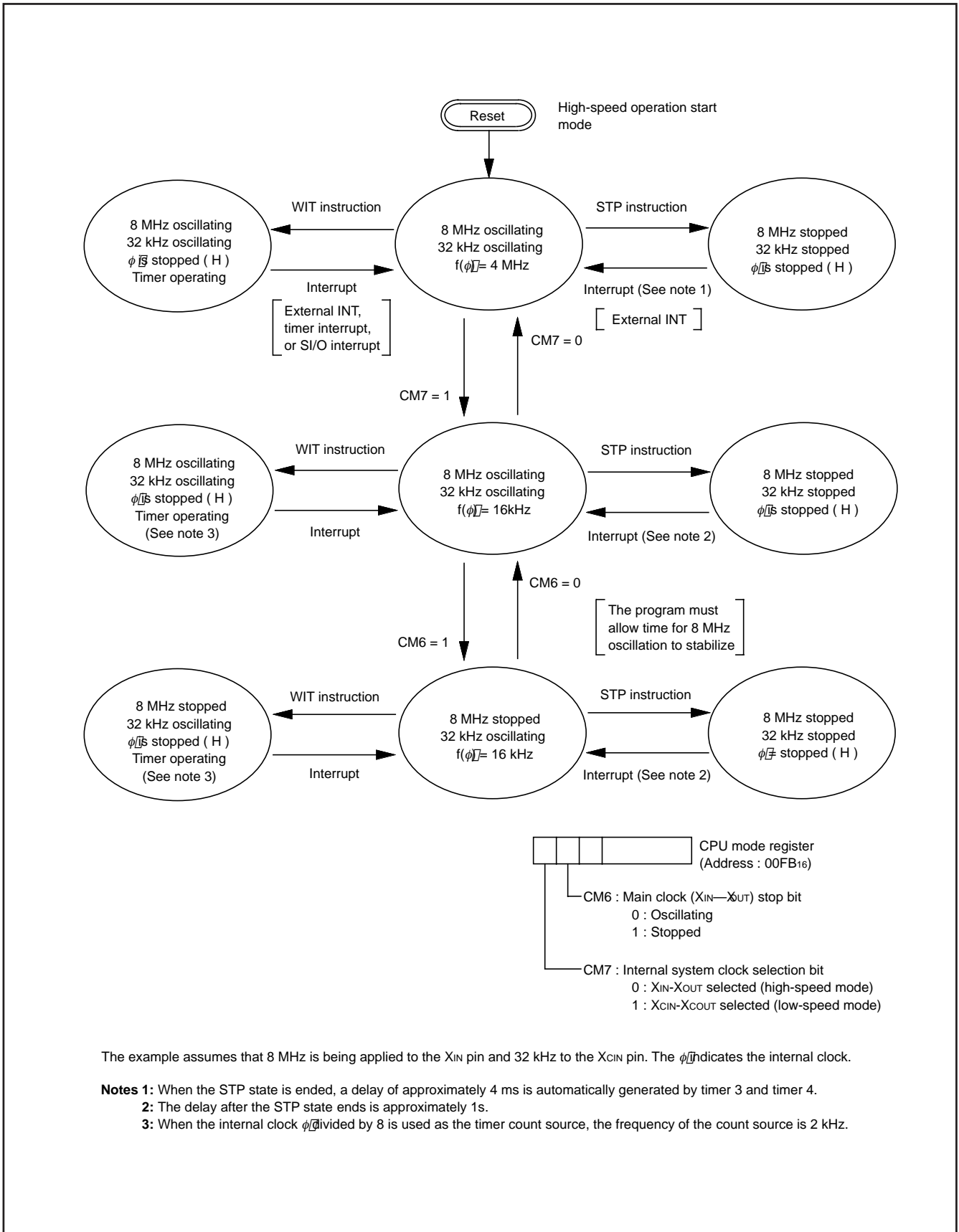


Fig.8.14.4 State Transitions of System Clock

### 8.15 DISPLAY OSCILLATION CIRCUIT

The OSD oscillation circuit has a built-in clock oscillation circuits, so that a clock for OSD can be obtained simply by connecting an LC, a ceramic resonator, or a quartz-crystal oscillator across the pins OSC1 and OSC2. Which of the sub-clock or the OSD oscillation circuit is selected by setting bits 5 and 6 of the OSD control register (address 00D016).

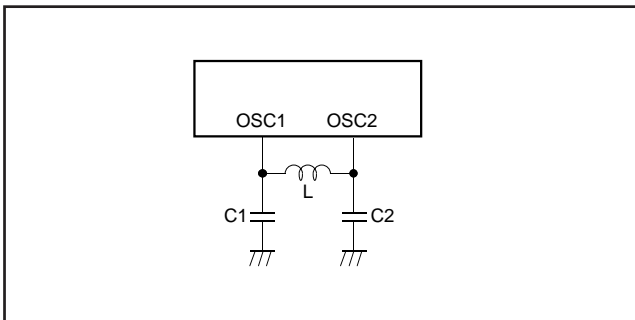


Fig.8.15.1 Display Oscillation Circuit

### 8.16 AUTO-CLEAR CIRCUIT

When a power source is supplied, the auto-clear function will operate by connecting the following circuit to the  $\overline{\text{RESET}}$  pin.

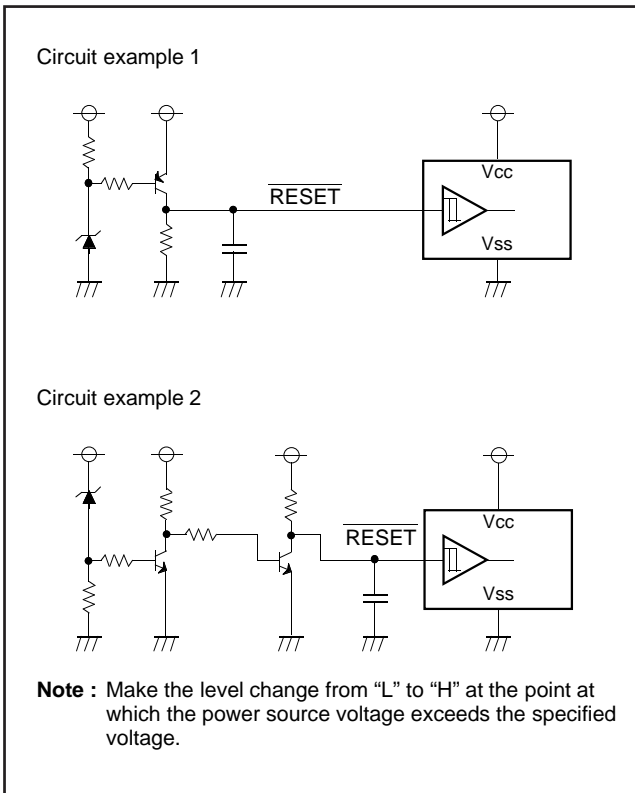


Fig.8.16.1 Auto-clear Circuit Example

### 8.17 ADDRESSING MODE

The memory access is reinforced with 17 kinds of addressing modes. Refer to SERIES 740 <Software> User’s Manual for details.

### 8.18 MACHINE INSTRUCTIONS

There are 71 machine instructions. Refer to SERIES 740 <Soft-ware> User’s Manual for details.

## 9. PROGRAMMING NOTES

- The divide ratio of the timer is  $1/(n+1)$ .
- Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- After the ADC and SBC instructions are executed (in the decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.
- An NOP instruction is needed immediately after the execution of a PLP instruction.
- In order to avoid noise and latch-up, connect a bypass capacitor ( $\approx 0.1\mu\text{F}$ ) directly between the VCC pin–VSS pin, AVCC pin–VSS pin, and the VCC pin–CNVSS pin, using a thick wire.
- M3727GM6/M8-XXXSP and M37272E8SP/FP are compatible, but please attention differences as follows:

Parameter	M37272E8SP/FP		M3727GM6/M8-XXXSP/FP	
Spec of 14th pins	AVcc		NC (Non connection)	
Power source voltage	Normal	Max.	Normal	Max.
When System operate				
$f(\text{Xin}) : 8\text{MFz}$	OSD : OFF Data slicer : OFF	15 mA	30 mA	10 mA
	OSD : ON Data slicer : ON	30mA	45 mA	25 mA
			25 mA	40 mA

\* Need to apply  $5\text{V} \pm 10\%$ , because 14th pin of M37272E8SP/FP is AVcc pin. M3727GM6/M8-XXXSP/FP is the non connection pin, but it is not connect to the inside of IC. You can apply voltage.

**10. ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub> , AV <sub>CC</sub>	Power source voltage V <sub>CC</sub> , AV <sub>CC</sub>	All voltages are based on V <sub>SS</sub> . Output transistors are cut off.	-0.3 to 6	V
V <sub>I</sub>	Input voltage CNV <sub>SS</sub>		-0.3 to 6	V
V <sub>I</sub>	Input voltage P00-P07, P10-P17, P20-P27, P30, P31, P50, P51, X <sub>IN</sub> , RESET, CV <sub>IN</sub>		-0.3-V <sub>CC</sub> + 0.3	V
V <sub>O</sub>	Output voltage P00-P07, P10-P17, P20-P27, P30, P31, P52-P55, X <sub>OUT</sub>		-0.3-V <sub>CC</sub> + 0.3	V
I <sub>OH</sub>	Circuit current P10-P17, P20-P27, P30, P31, P52-P55		0 to 1 (See note 1)	mA
I <sub>OL1</sub>	Circuit current P00-P07, P10, P15-P17, P20-P23, P26, P27, P52-P55		0 to 2 (See note 2)	mA
I <sub>OL2</sub>	Circuit current P11-P04		0 to 6 (See note 2)	mA
I <sub>OL3</sub>	Circuit current P24, P25, P30, P31		0 to 10 (See note 3)	mA
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25 °C	550	mW
T <sub>opr</sub>	Operating temperature		-10 to 70	°C
T <sub>stg</sub>	Storage temperature		-40 to 125	°C

**11. RECOMMENDED OPERATING CONDITIONS** (T<sub>a</sub> = -10 °C to 70 °C, V<sub>CC</sub> = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V <sub>CC</sub> , AV <sub>CC</sub>	Power source voltage (See note 4)	4.5	5.0	5.5	V
V <sub>SS</sub>	Power source voltage	0	0	0	V
V <sub>IH1</sub>	HIGH Input voltage P00-P07, P10-P17, P20-P27, P30, P31, P50, P51, RESET, X <sub>IN</sub>	0.8 V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>IH2</sub>	HIGH Input voltage SCL1, SCL2, SDA1, SDA2 (When using I <sup>2</sup> C-BUS)	0.7 V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>IL1</sub>	LOW Input voltage P00-P07, P10-P17, P20-P27, P30, P31	0		0.4 V <sub>CC</sub>	V
V <sub>IL2</sub>	LOW Input voltage SCL1, SCL2, SDA1, SDA2 (When using I <sup>2</sup> C-BUS)	0		0.3 V <sub>CC</sub>	V
V <sub>IL3</sub>	LOW Input voltage (See note 6) P50, P51, RESET, X <sub>IN</sub> , OSC1, TIM2, TIM3, INT1, INT2, INT3, S <sub>IN</sub> , SCL <sub>K</sub>	0		0.2 V <sub>CC</sub>	V
I <sub>OH</sub>	HIGH average output current (See note 1) P10-P17, P20-P27, P30, P31, P52-P55			1	mA
I <sub>OL1</sub>	LOW average output current (See note 2) P00-P07, P10, P15-P17, P20-P23, P26, P27, P52-P55			2	mA
I <sub>OL2</sub>	LOW average output current (See note 2) P11-P14			6	mA
I <sub>OL3</sub>	LOW average output current (See note 3) P24, P25, P30, P31			10	mA
f(X <sub>IN</sub> )	Oscillation frequency (for CPU operation) (See note 5) X <sub>IN</sub>	7.9	8.0	8.1	MHz
f(X <sub>CIN</sub> )	Oscillation frequency (for sub-clock operation) X <sub>CIN</sub>	29	32	35	kHz
f <sub>OSC</sub>	Oscillation frequency (for OSD) OSC1	26.5	27.0	27.0	MHz
f <sub>hs1</sub>	Input frequency TIM2, TIM3, INT1, INT2, INT3			100	kHz
f <sub>hs2</sub>	Input frequency SCL <sub>K</sub>			1	MHz
f <sub>hs3</sub>	Input frequency SCL1, SCL2			400	kHz
f <sub>hs4</sub>	Input frequency Horizontal sync. signal of video signal	15.262	15.734	16.206	kHz
V <sub>I</sub>	Input amplitude video signal CV <sub>IN</sub>	1.5	2.0	2.5	V



**12. ELECTRIC CHARACTERISTICS** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $f(XIN) = 8\text{ MHz}$ ,  $T_a = -10\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit	Test circuit
					Min.	Typ.	Max.		
I <sub>CC</sub>	Power source current	System operation	V <sub>CC</sub> = 5.5V, f(XIN) = 8MHz <small>(The upper row : M3727GM6/M8) (The lower row : M37272E8)</small>	OSD OFF Data slicer OFF		10 (15)	25 (30)	mA	1
				OSD ON Data slicer ON		25 (30)	40 (45)		
				V <sub>CC</sub> = 5.5V, f(XIN) = 0, f(XCIN) = 32kHz, OSD OFF, Data slicer OFF, Low-power dissipation mode set (CM5 = "0", CM6 = "1")		60	200	μA	
			Wait mode	V <sub>CC</sub> = 5.5 V, f(XIN) = 8 MHz		2	4	mA	
				V <sub>CC</sub> = 5.5 V, f(XIN) = 0, f(XCIN) = 32 kHz, Low-power dissipation mode set (CM5 = "0", CM6 = "1")		25	100		
Stop mode			1	10					
VOH	HIGH output voltage	P10–P17, P20–P27, P30, P31, P52–P55,	V <sub>CC</sub> = 5.5V, f(XIN) = 0, f(XCIN) = 0		2.4			V	2
VOL	LOW output voltage	P00–P07, P10, P15–P17, P20–P23, P26, P27, P52–P55	V <sub>CC</sub> = 4.5 V I <sub>OH</sub> = –0.5 mA				0.4	V	
	LOW output voltage	P24, P25, P30, P31	I <sub>OL</sub> = 0.5 mA				3.0		
	LOW output voltage	P11–P14	V <sub>CC</sub> = 4.5 V I <sub>OL</sub> = 10.0 mA	I <sub>OL</sub> = 3 mA			0.4		
V <sub>T+</sub> –V <sub>T–</sub>	Hysteresis (See note 6)	RESET, P50, P51, INT1, INT2, INT3, TIM2, TIM3, S <sub>IN</sub> , SCLK, SCL1, SCL2, SDA1, SDA2	V <sub>CC</sub> = 4.5 V  V <sub>CC</sub> = 5.0 V			0.5	1.3	V	3
I <sub>IZH</sub>	HIGH input leak current	P00–P07, P10–P17, P20–P27, P30, P31, RESET, P50, P51,	V <sub>CC</sub> = 5.5 V				5	μA	4
I <sub>IZL</sub>	LOW input leak current	P00–P07, P10–P17, P20–P27, P30, P31, P50, P51, RESET	V <sub>I</sub> = 5.5 V  V <sub>CC</sub> = 5.5 V				5	μA	4
I <sub>OZH</sub>	HIGH output leak current	P00–P05 (Only M37272E8SP/FP version)	V <sub>I</sub> = 0 V				10	μA	5
RBS	I <sup>2</sup> C-BUS • BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2)		V <sub>CC</sub> = 5.5 V				130	Ω	6

**Notes 1:** The total current that flows out of the IC must be 20 mA or less.

**2:** The total input current to IC (I<sub>OL1</sub> + I<sub>OL2</sub> + I<sub>OL3</sub>) must be 30 mA or less.

**3:** The total average input current for ports P30, P31, P24 and P25 to IC must be 20 mA or less.

**4:** Connect 0.1 μF or more capacitor externally between the power source pins V<sub>CC</sub>–V<sub>SS</sub> (and AV<sub>CC</sub>–V<sub>SS</sub>) so as to reduce power source noise.

Also connect 0.1 μF or more capacitor externally between the pins V<sub>CC</sub>–CNV<sub>SS</sub>. ( ) …M37272E8SP/FP

**5:** Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8 MHz.

**6:** P06, P07, P15, P23, P24 have the hysteresis when these pins are used as interrupt input pins or timer input pins. P11–P14 have the hysteresis when these pins are used as multi-master I<sup>2</sup>C-BUS interface ports. P20–P22 have the hysteresis when these pins are used as serial I/O pins.

**7:** Pin names in each parameter is described as below.

(1) Dedicated pins: dedicated pin names.

(2) Duple-/triple-function ports

- When the same limits: I/O port name.

- When the limits of functions except ports are different from I/O port limits: function pin name.

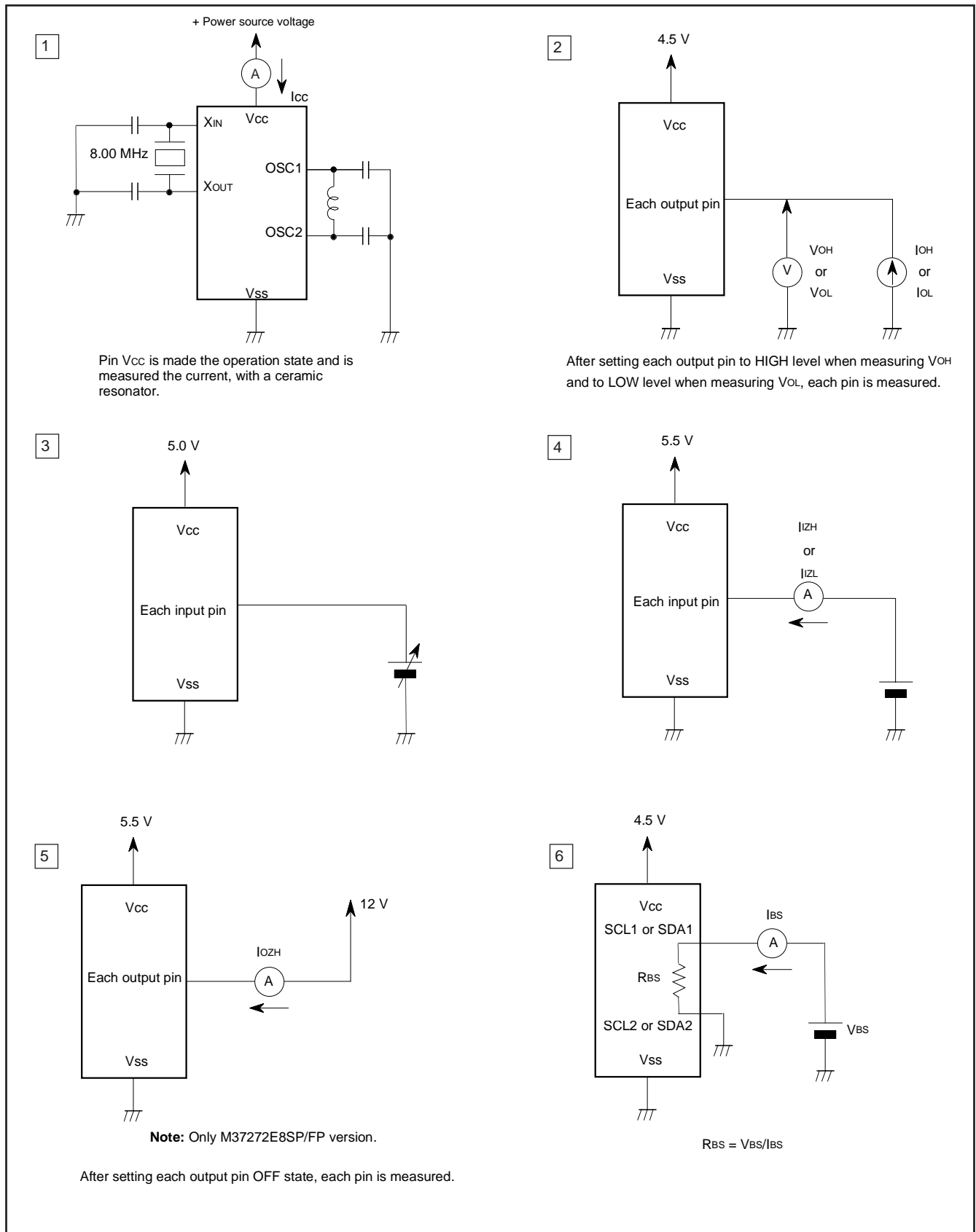


Fig.12.1 Measure Circuits

### 13. A-D CONVERTER CHARACTERISTICS

(VCC = 5 V ± 10 %, VSS = 0 V, f(XIN) = 8 MHz, Ta = -10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				6	bits
—	Non-linearity error				±1	LSB
—	Differential non-linearity error				±0.9	LSB
V0T	Zero transition error	IOL (SUM) = 0 mA			2	LSB
VFST	Full-scale transition error				-2	LSB

### 14. MULTI-MASTER I<sup>2</sup>C-BUS BUS LINE CHARACTERISTICS

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
tBUF	Bus free time	4.7		1.3		μs
tHD; STA	Hold time for START condition	4.0		0.6		μs
tLOW	LOW period of SCL clock	4.7		1.3		μs
tR	Rising time of both SCL and SDA signals		1000	20+0.1Cb	300	ns
tHD; DAT	Data hold time	0		0	0.9	μs
tHIGH	HIGH period of SCL clock	4.0		0.6		μs
tF	Falling time of both SCL and SDA signals		300	20+0.1Cb	300	ns
tSU; DAT	Data set-up time	250		100		ns
tSU; STA	Set-up time for repeated START condition	4.7		0.6		μs
tSU; STO	Set-up time for STOP condition	4.0		0.6		μs

**Note:** Cb = total capacitance of 1 bus line

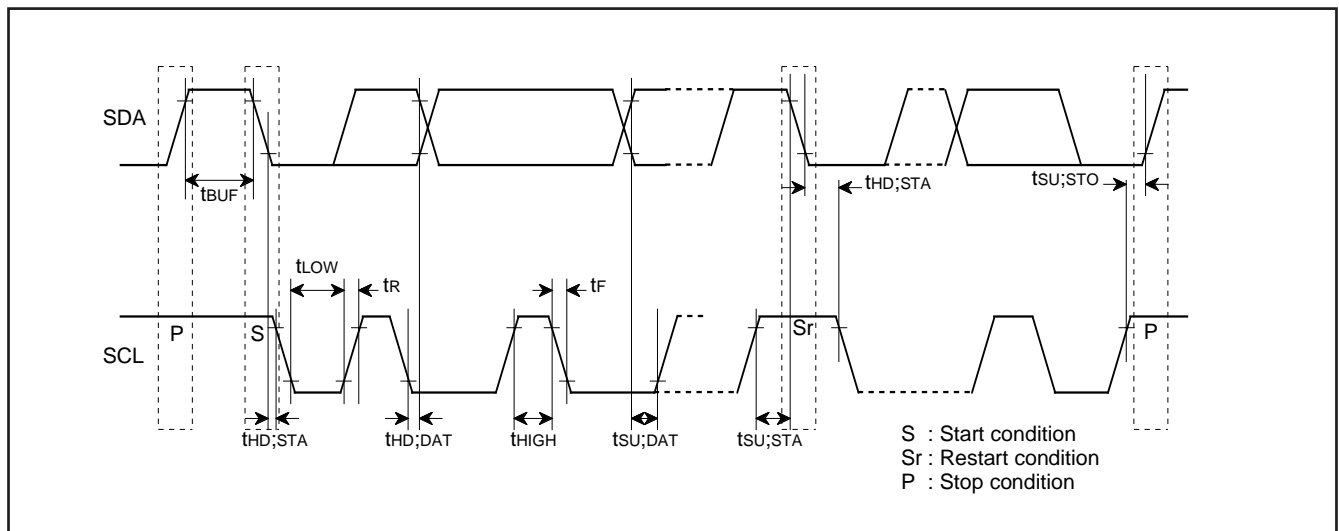


Fig.14.1 Definition Diagram of Timing on Multi-master I<sup>2</sup>C-BUS

## 15. PROM PROGRAMMING METHOD

The built-in PROM of the One Time PROM version (blank) and the built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37272E8SP	PCA7429G02
M37272E8FP	PCA7427

The PROM of the One Time PROM version (blank) is not tested or screened in the assembly process nor any following processes. To ensure proper operation after programming, the procedure shown in Figure 15.1 is recommended to verify programming.

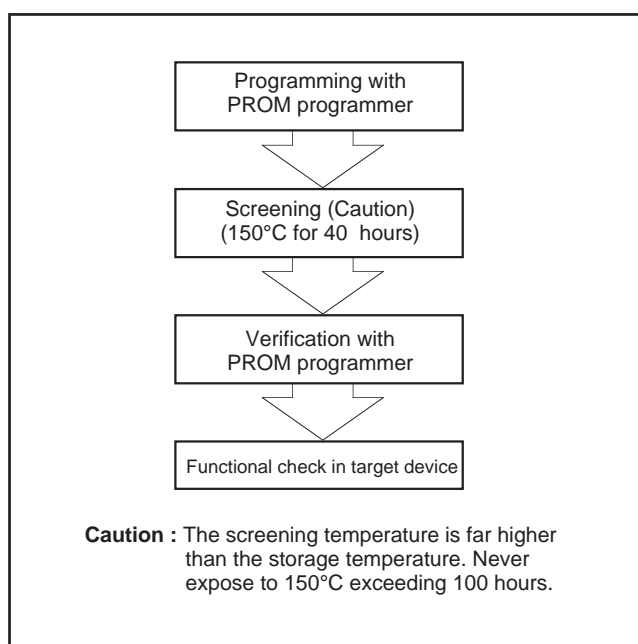


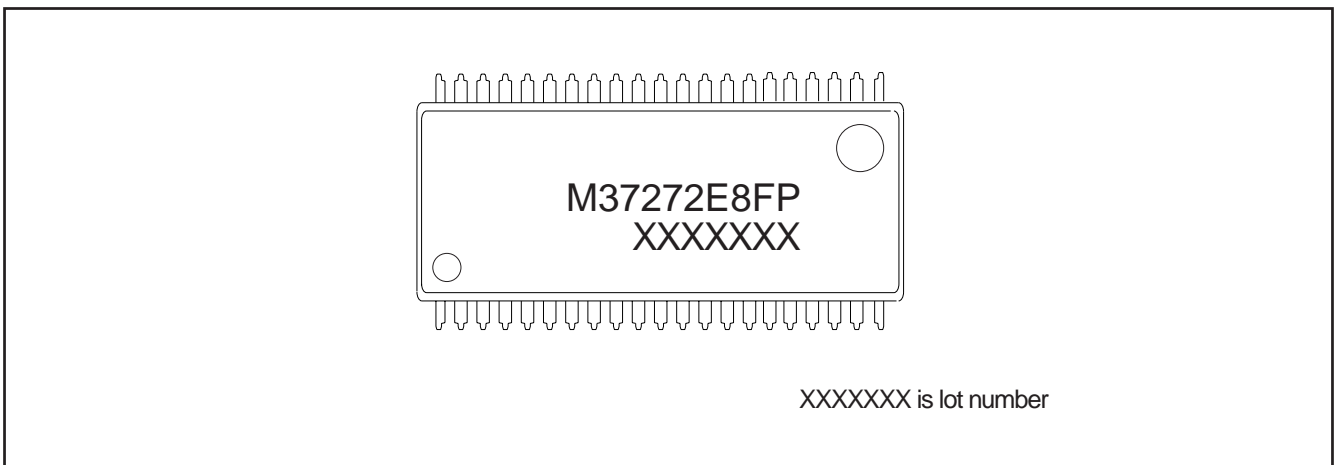
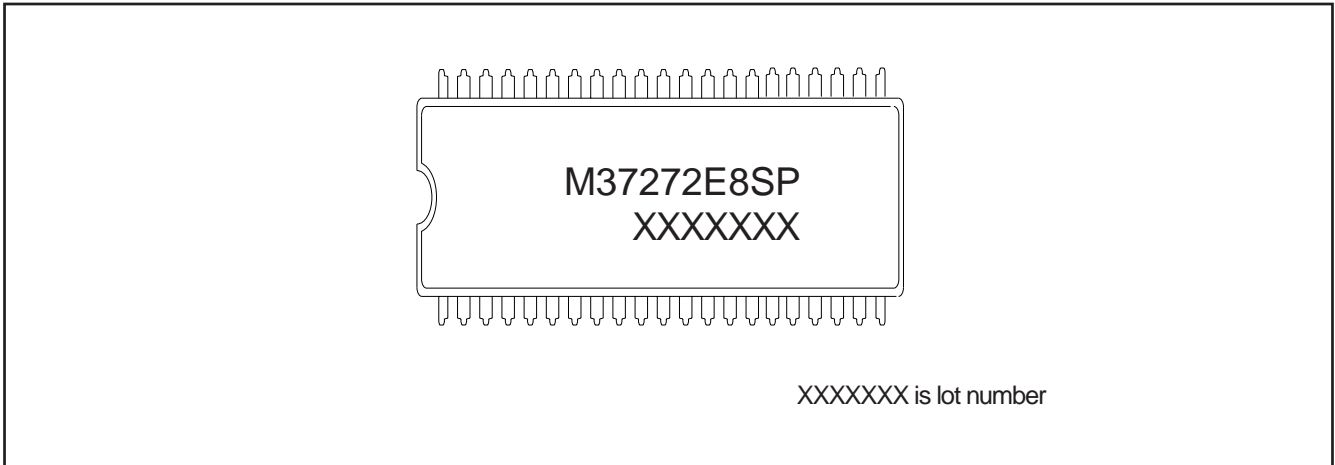
Fig. 15.1 Programming and Testing of One Time PROM Version

## 16. DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

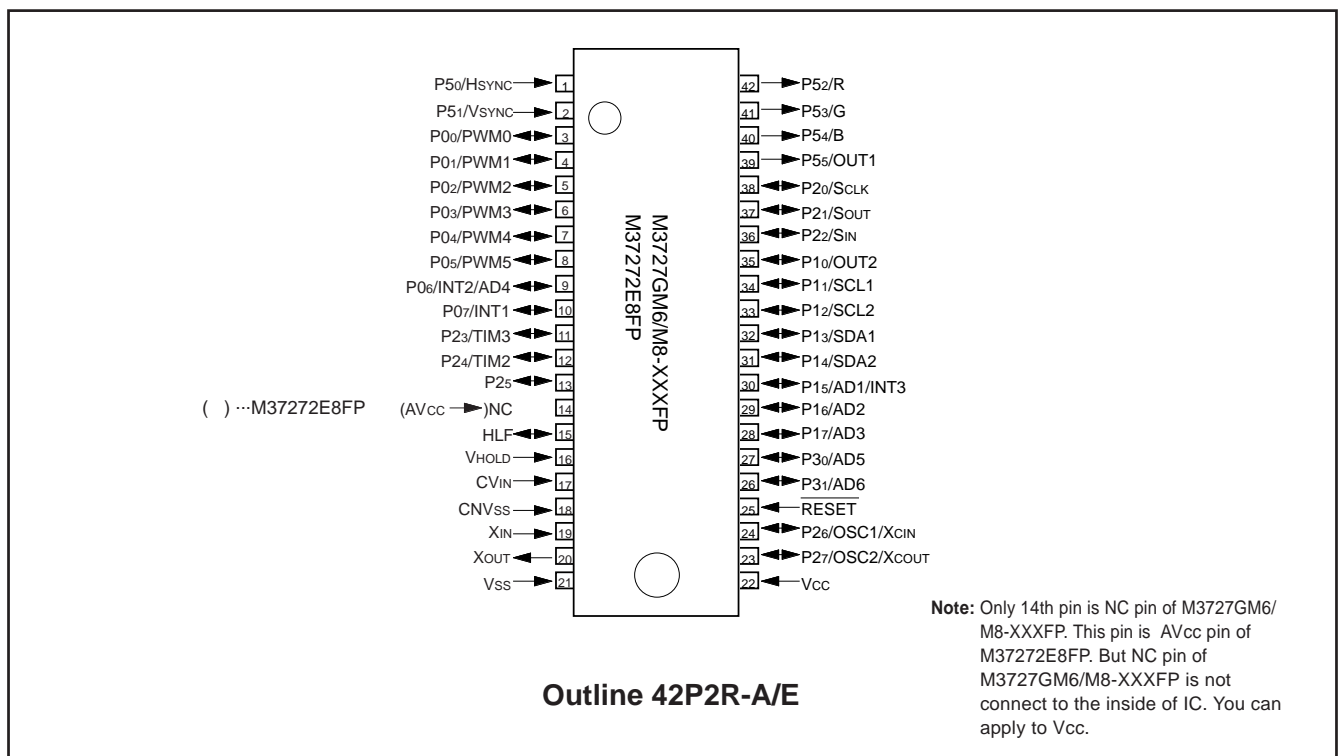
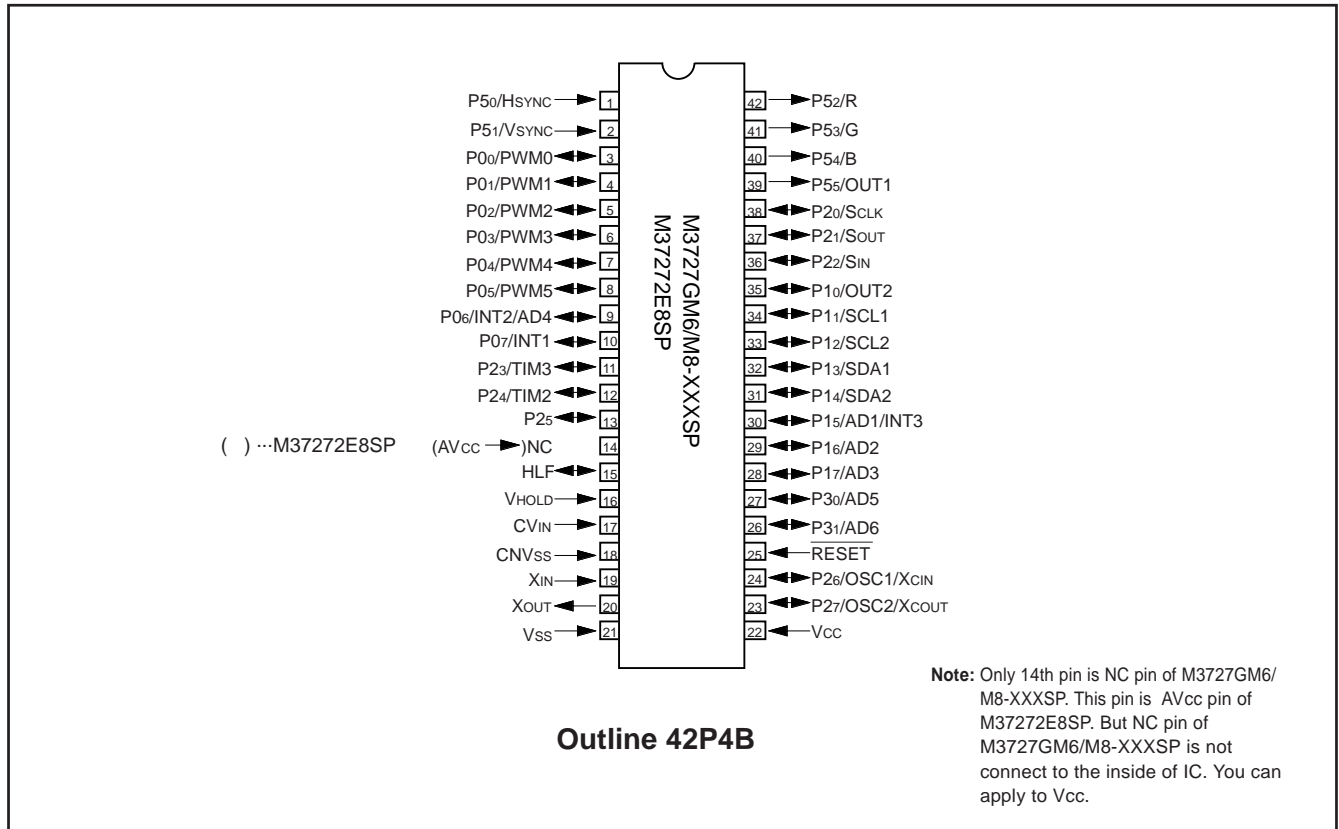
- Mask ROM Order Confirmation Form
- Mask Specification Form
- Data to be written to ROM, in EPROM form (28-pin DIP Type 27512, three identical copies) or FDK

### 17. ONE TIME PROM VERSION M37272E8SP/FP MARKING

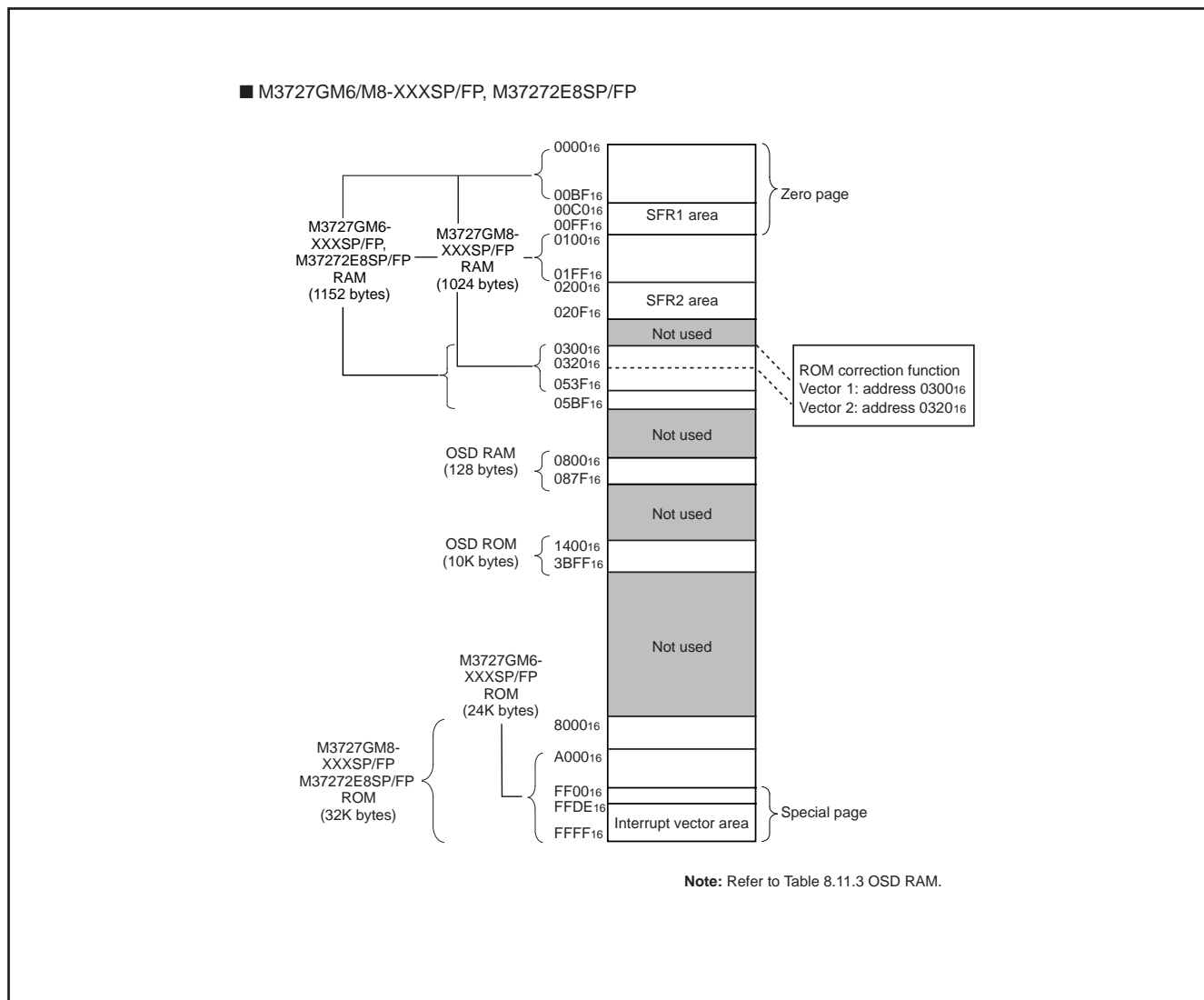


## 18. APPENDIX

### Pin Configuration (TOP VIEW)



### Memory Map





### Memory Map of Special Function Register (SFR)

#### ■ SFR1 Area (addresses C0<sub>16</sub> to DF<sub>16</sub>)

<Bit allocation>

- : Function bit
- : No function bit
- 0 : Fix this bit to "0" (do not write "1")
- 1 : Fix this bit to "1" (do not write "0")

<State immediately after reset>

- 0 : "0" immediately after reset
- 1 : "1" immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	Bit allocation								State immediately after reset								
		b7						b0		b7						b0		
C0 <sub>16</sub>	Port P0 (P0)																	?
C1 <sub>16</sub>	Port P0 direction register (D0)																	00 <sub>16</sub>
C2 <sub>16</sub>	Port P1 (P1)																	?
C3 <sub>16</sub>	Port P1 direction register (D1)																	00 <sub>16</sub>
C4 <sub>16</sub>	Port P2 (P2)																	?
C5 <sub>16</sub>	Port P2 direction register (D2)																	00 <sub>16</sub>
C6 <sub>16</sub>	Port P3 (P3)																	0 0 0 0 0 0 ? ?
C7 <sub>16</sub>	Port P3 direction register (D3)																	00 <sub>16</sub>
C8 <sub>16</sub>																		?
C9 <sub>16</sub>																		?
CA <sub>16</sub>	Port P5 (P5)																	?
CB <sub>16</sub>	OSD port control register (PF)																	00 <sub>16</sub>
CC <sub>16</sub>																		00 <sub>16</sub>
CD <sub>16</sub>																		?
CE <sub>16</sub>	Caption data register 3 (CD3)																	?
CF <sub>16</sub>	Caption data register 4 (CD4)																	?
D0 <sub>16</sub>	OSD control register (OC)																	00 <sub>16</sub>
D1 <sub>16</sub>	Horizontal position register (HP)																	00 <sub>16</sub>
D2 <sub>16</sub>	Block control register 1 (BC1)																	?
D3 <sub>16</sub>	Block control register 2 (BC2)																	?
D4 <sub>16</sub>	Vertical position register 1 (VP1)																	?
D5 <sub>16</sub>	Vertical position register 2 (VP2)																	?
D6 <sub>16</sub>	Window register 1 (WN1)																	?
D7 <sub>16</sub>	Window register 2 (WN2)																	?
D8 <sub>16</sub>	I/O polarity control register (PC)																	40 <sub>16</sub>
D9 <sub>16</sub>	Raster color register (RC)																	00 <sub>16</sub>
DA <sub>16</sub>																		?
DB <sub>16</sub>																		?
DC <sub>16</sub>	Interrupt input polarity control register (RE)																	00 <sub>16</sub>
DD <sub>16</sub>																		00 <sub>16</sub>
DE <sub>16</sub>																		00 <sub>16</sub>
DF <sub>16</sub>																		?

■ SFR1 Area (addresses E0<sub>16</sub> to FF<sub>16</sub>)

<Bit allocation>

- : } Function bit
- Name : }
- : No function bit
- 0 : Fix this bit to "0"  
(do not write "1")
- 1 : Fix this bit to "1"  
(do not write "0")

<State immediately after reset>

- 0 : "0" immediately after reset
- 1 : "1" immediately after reset
- ? : Indeterminate immediately after reset

Address	Register	Bit allocation								State immediately after reset										
		b7						b0						b7					b0	
E0 <sub>16</sub>	Data slicer control register 1 (DSC1)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	DSC12	DSC11	DSC10	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
E1 <sub>16</sub>	Data slicer control register 2 (DSC2)	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	DSC25	DSC24	DSC23	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
E2 <sub>16</sub>	Caption data register 1 (CD1)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	CDL17	CDL16	CDL15	CDL14	CDL13	CDL12	CDL11	CDL10	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
E3 <sub>16</sub>	Caption data register 2 (CD2)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	CDH17	CDH16	CDH15	CDH14	CDH13	CDH12	CDH11	CDH10	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
E4 <sub>16</sub>	Clock run-in detect register (CRD)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	CRD7	CRD6	CRD5	CRD4	CRD3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
E5 <sub>16</sub>	Data clock position register (DPS)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	DPS7	DPS6	DPS5	DPS4	DPS3	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
E6 <sub>16</sub>	Caption position register (CPS)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	CPS7	CPS6	CPS5	CPS4	CPS3	CPS2	CPS1	CPS0	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
E7 <sub>16</sub>	Data slicer test register 2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
E8 <sub>16</sub>	Data slicer test register 1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
E9 <sub>16</sub>	Synchronous signal counter register	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	HC5	HC4	HC3	HC2	HC1	HC0	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		
EA <sub>16</sub>	Serial I/O register (SIO)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
EB <sub>16</sub>	Serial I/O mode register (SM)	<input checked="" type="checkbox"/>	SM6	SM5	<input checked="" type="checkbox"/>	SM3	SM2	SM1	SM0	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
EC <sub>16</sub>	A-D control register 1 (AD1)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	ADC14	ADC12	ADC11	ADC10	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
ED <sub>16</sub>	A-D control register 2 (AD2)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	ADC25	ADC24	ADC23	ADC22	ADC21	ADC20	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		
EE <sub>16</sub>	Timer 5 (T5)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
EF <sub>16</sub>	Timer 6 (T6)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
F0 <sub>16</sub>	Timer 1 (T1)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
F1 <sub>16</sub>	Timer 2 (T2)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
F2 <sub>16</sub>	Timer 3 (T3)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
F3 <sub>16</sub>	Timer 4 (T4)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
F4 <sub>16</sub>	Timer mode register 1 (TM1)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	TM17	TM16	TM15	TM14	TM13	TM12	TM11	TM10	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
F5 <sub>16</sub>	Timer mode register 2 (TM2)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	TM27	TM26	TM25	TM24	TM23	TM22	TM21	TM20	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
F6 <sub>16</sub>	I <sup>2</sup> C data shift register (S0)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	D7	D6	D5	D4	D3	D2	D1	D0	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
F7 <sub>16</sub>	I <sup>2</sup> C address register (S0D)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	RBW	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
F8 <sub>16</sub>	I <sup>2</sup> C status register (S1)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	MST	TRX	BB	PIN	AL	AAS	AD0	LRB	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
F9 <sub>16</sub>	I <sup>2</sup> C control register (S1D)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	BSEL1	BSEL0	10BIT SAD	ALS	ESO	BC2	BC1	BC0	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
FA <sub>16</sub>	I <sup>2</sup> C clock control register (S2)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	ACK	ACK BIT	FAST MODE	CCR4	CCR3	CCR2	CCR1	CCR0	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
FB <sub>16</sub>	CPU mode register (CPUM)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	CM7	CM6	CM5	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	CM2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
FC <sub>16</sub>	Interrupt request register 1 (IREQ1)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	IN3R	VSCR	OSDR	TM4R	TM3R	TM2R	TM1R	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
FD <sub>16</sub>	Interrupt request register 2 (IREQ2)	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	TM56R	RIICR	IN2R	CKR	S1R	DSR	IN1R	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
FE <sub>16</sub>	Interrupt control register 1 (ICON1)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	IN3E	VSCOE	SDE	TM4E	TM3E	TM2E	TM1E	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
FF <sub>16</sub>	Interrupt control register 2 (ICON2)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	TM56C	TM56E	IICE	IN2E	CKE	S1E	DSE	IN1E	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

■ SFR2 Area (addresses 200<sub>16</sub> to 20F<sub>16</sub>)

<Bit allocation>

: } Function bit  
 Name : }

: No function bit

0 : Fix this bit to 0  
 (do not write 1 )

1 : Fix this bit to 1  
 (do not write 0 )

<State immediately after reset>

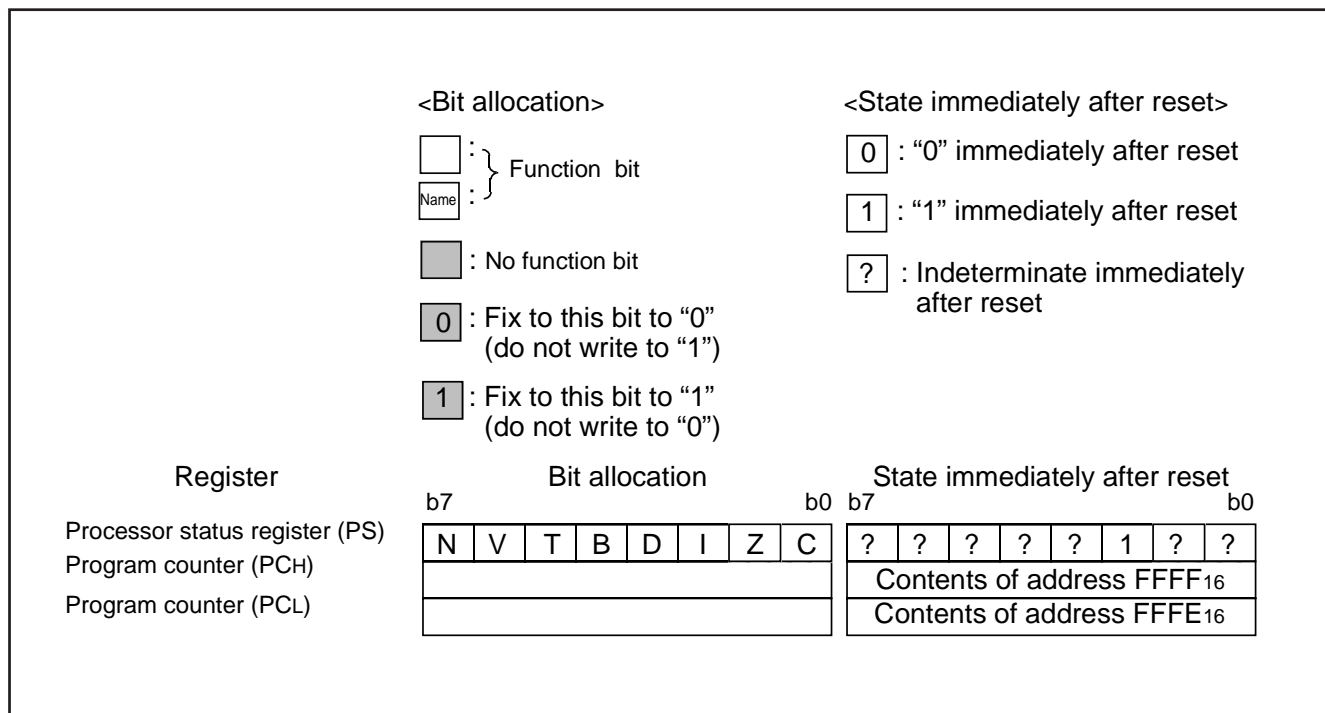
0 : 0 immediately after reset

1 : 1 immediately after reset

? : Indeterminate immediately after reset

Address	Register	Bit allocation								State immediately after reset							
		b7							b0	b7							0
200 <sub>16</sub>	PWM0 register (PWM0)																?
201 <sub>16</sub>	PWM1 register (PWM1)																?
202 <sub>16</sub>	PWM2 register (PWM2)																?
203 <sub>16</sub>	PWM3 register (PWM3)																?
204 <sub>16</sub>	PWM4 register (PWM4)																?
205 <sub>16</sub>	PWM5 register (PWM5)																?
206 <sub>16</sub>		00 <sub>16</sub>								?							
207 <sub>16</sub>		00 <sub>16</sub>								?							
208 <sub>16</sub>	PWM mode register 1 (PM1)							PM13									?
209 <sub>16</sub>	PWM mode register 2 (PM2)	0			PM25	M24	M23										0
20A <sub>16</sub>	ROM correction address 1 (high-order)																00 <sub>16</sub>
20B <sub>16</sub>	ROM correction address 1 (low-order)																00 <sub>16</sub>
20C <sub>16</sub>	ROM correction address 2 (high-order)																00 <sub>16</sub>
20D <sub>16</sub>	ROM correction address 2 (low-order)																00 <sub>16</sub>
20E <sub>16</sub>	ROM correction enable register (RCR)								RCR1							RCR0	00 <sub>16</sub>
20F <sub>16</sub>																	?

### Internal State of Processor Status Register and Program Counter at Reset



### Structure of Register

The figure of each register structure describes its functions, contents at reset, and attributes as follows:

<Example>

CPU Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

1 1 0 0

CPU mode register (CPUM) (CM) [Address 00FB16]

Bit position	Name	Functions	Values immediately after reset release (Note 1)	Bit attributes (Note 2)
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: 1 0: 1 1: } Not available	0	R;W
2	Stack page selection bit (See note) (CM2)	0: 0 page 1: 1 page	1	R;W
3, 4	Fix these bits to "1."		1	R;W
5	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is "1."		1	R;W
6, 7	Clock switch bits (CM6, CM7)	b7 b6 0 0: f(XIN) = 8 MHz 0 1: f(XIN) = 12 MHz 1 0: f(XIN) = 16 MHz 1 1: Do not set	0	R;W

Legend:  : Bit in which nothing is assigned

**Notes 1:** Values immediately after reset release  
 0 ..... "0" after reset release  
 1 ..... "1" after reset release  
 Indeterminate ••• Indeterminate after reset release

**Notes 2:** Bit attributes ..... The attributes of control register bits are classified into 3 types : read-only, write-only and read and write. In the figure, these attributes are represented as follows :

R ..... Read  
 W ..... Write

R ..... Read enabled  
 - ..... Read disabled  
 W ..... Write enabled  
 - ..... Write disabled  
 \* ..... "0" can be set by software, but "1" cannot be set.

**Address 00C1<sub>16</sub>, 00C3<sub>16</sub>, 00C5<sub>16</sub>**

**Port Pi Direction Register**

b7 b6 b5 b4 b3 b2 b1 b0



Port Pi direction register (PiD) (i=0,1,2) [Addresses 00C1<sub>16</sub>, 00C3<sub>16</sub>, 00C5<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Port Pi direction register	0 : Port P <i>i</i> 0 input mode 1 : Port P <i>i</i> 0 output mode	0	R	W
1		0 : Port P <i>i</i> 1 input mode 1 : Port P <i>i</i> 1 output mode	0	R	W
2		0 : Port P <i>i</i> 2 input mode 1 : Port P <i>i</i> 2 output mode	0	R	W
3		0 : Port P <i>i</i> 3 input mode 1 : Port P <i>i</i> 3 output mode	0	R	W
4		0 : Port P <i>i</i> 4 input mode 1 : Port P <i>i</i> 4 output mode	0	R	W
5		0 : Port P <i>i</i> 5 input mode 1 : Port P <i>i</i> 5 output mode	0	R	W
6		0 : Port P <i>i</i> 6 input mode 1 : Port P <i>i</i> 6 output mode	0	R	W
7		0 : Port P <i>i</i> 7 input mode 1 : Port P <i>i</i> 7 output mode	0	R	W

**Address 00C7<sub>16</sub>**

**Port P3 Direction Register**

b7 b6 b5 b4 b3 b2 b1 b0

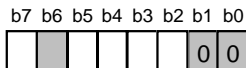


Port P3 direction register (P3D) [Address 00C7<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Port P3 direction register	0 : Port P3 <sub>0</sub> input mode 1 : Port P3 <sub>0</sub> output mode	0	R	W
1		0 : Port P3 <sub>1</sub> input mode 1 : Port P3 <sub>1</sub> output mode	0	R	W
2	Port P3 <sub>0</sub> output structure selection bit (P30C)	0 : CMOS output 1 : N-channel open-drain output	0	R	W
3	Port P3 <sub>1</sub> output structure selection bit (P30C)	0 : CMOS output 1 : N-channel open-drain output	0	R	W
4, 5, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are 0.		0	R	
6	Timer 3 count source selection bit (T3SC)	Refer to Timer section.	0	R	W

**Address 00CB<sub>16</sub>**

**OSD Port Control Register**

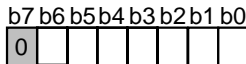


OSD port control register (PF) [Address 00CB<sub>16</sub>]

B	Name	Functions	After reset	R : W
0, 1	Fix these bits to 0.		0	R : W
2	Port P5 <sub>2</sub> output signal selection bit (PF2)	0 : R signal output 1 : Port P5 <sub>2</sub> output	0	R : W
3	Port P5 <sub>3</sub> output signal selection bit (PF3)	0 : G signal output 1 : Port P5 <sub>3</sub> output	0	R : W
4	Port P5 <sub>4</sub> output signal selection bit (PF4)	0 : B signal output 1 : Port P5 <sub>4</sub> output	0	R : W
5	Port P5 <sub>5</sub> output signal selection bit (PF5)	0 : OUT1 signal output 1 : Port P5 <sub>5</sub> output	0	R : W
6	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is 0.		0	R : W
7	Port P1 <sub>0</sub> output signal selection bit (PF7)	0 : Port P1 <sub>0</sub> output 1 : OUT2 signal output	0	R : W

**Address 00D0<sub>16</sub>**

**OSD Control Register**



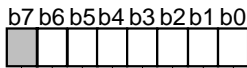
OSD control register (OC) [Address 00D0<sub>16</sub>]

B	Name	Functions	After reset	R : W
0	OSD control bit (OC0) (See note)	0 : All-blocks display off 1 : All-blocks display on	0	R : W
1	Automatic solid space control bit (OC1)	0 : OFF 1 : ON	0	R : W
2	Window control bit (OC2)	0 : OFF 1 : ON	0	R : W
3	CC mode clock selection bit (OC3)	0 : Data slicer clock 1 : Clock from OSC1 pin	0	R : W
4	OSD mode clock selection bit (OC4)	0 : Data slicer clock 1 : Clock from OSC1 pin	0	R : W
5, 6	OSC1 clock selection bit (OC5, OC6)	b6 b5 0 0 : 32 kHz oscillating 0 1 : Do not set. 1 0 : LC oscillating, Ceramic oscillating 1 1 : Do not set.	0	R : W
7	Fix this bit to 0.		0	R : W

**Note:** Even this bit is switched during display, the display screen remains unchanged until a rising (falling) of the next V SYNC.

**Address 00D1<sub>16</sub>**

Horizontal Position Register



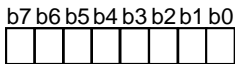
Horizontal position register (HP) [Address 00D1<sub>16</sub>]

B	Name	Functions	After reset	R/W
0 to 6	Horizontal display start position control bits (HP0 to HP6)	Horizontal display start positions 128 steps (00 <sub>16</sub> to 7F <sub>16</sub> ) (1 step is 4T <sub>osc</sub> )	0	R/W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R—

**Note:** The setting value synchronizes with the V SYNC.

**Address 00D2<sub>16</sub>, 00D3<sub>16</sub>**

Block Control register i



Block control register i (BCi) (i=1, 2) [Addresses 00D2<sub>16</sub> and 00D3<sub>16</sub>]

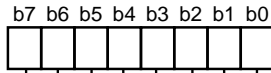
B	Name	Functions	After reset	R/W
0, 1	Display mode selection bits (BCi0, BCi1) (See note 1)	b1 b0 0 0: Display OFF 0 1: CC mode 1 0: OSD mode (Border OFF) 1 1: OSD mode (Border ON)	Indeterminate	R/W
2, 3	Dot size selection bits (BCi2, BCi3)	b4 b3 b2 Pre-divide Ratio   Dot Size 0 0 0   1Tc X 1/2H 0 0 1   1Tc X 1H 1 0 0   2Tc X 2H 1 0 1   3Tc X 3H x 2	Indeterminate	R/W
4	Pre-divide ratio selection bit (BCi4)	b4 b3 b2 Pre-divide Ratio   Dot Size 1 0 0   1Tc X 1/2H 1 0 1   1Tc X 1H 1 1 0   2Tc X 2H 1 1 1   3Tc X 3H x 3	Indeterminate	R/W
5	OUT1/OUT2 output control bit (BCi5) (See note 1)	0: OUT1 output control 1: OUT2 output control	Indeterminate	R/W
6	Vertical display start position control bit (BCi6)	BC16: Block 1 BC26: Block 1	Indeterminate	R/W
7	Window top/bottom boundary control bit (BCi7)	BC17: Window top boundary BC27: Window bottom boundary	Indeterminate	R/W

**Notes 1:** Bit RA3 of OSD RAM controls OUT1 output when bit 5 is "0."  
Bit RA3 of OSD RAM controls OUT2 output when bit 5 is "1."  
**2:** Tc is OSD clock cycle divided in pre-divide circuit.  
**3:** H is Hsync.



**Address 00D4<sub>16</sub>, 00D5<sub>16</sub>**

Vertical Position Register i



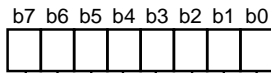
Vertical position register i (VPi) (i = 1 and 2) [Addresses 00D4<sub>16</sub>, 00D5<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 7	Vertical display start position control bits (VPi0 to VPi7) (See note)	Vertical display start position = $T_H \times (BCi6 \times 16^2 + n)$ (n: setting value, $T_H$ : Hsync cycle, BCi6: bit 6 of block control register i)	Indeterminate	R	W

**Note:** Set values except "00<sub>16</sub>" to VPi when BCi6 is "0."

**Address 00D6<sub>16</sub>**

Window Register 1



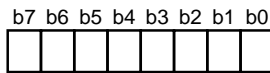
Window register 1 (WN1) [Address 00D6<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 7	Window top boundary control bits (WN10 to WN17)	Window top border position = $T_H \times (BC17 \times 16^2 + n)$ (n: setting value, $T_H$ : Hsync cycle, BC17: bit 7 of block control register 1)	Indeterminate	R	W

**Notes** 1: Set values except "00<sub>16</sub>" to WN1 when BC17 is "0."  
2: Set values fit for the following condition: WN1 < WN2.

**Address 00D7<sub>16</sub>**

Window Register 2



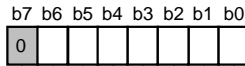
Window register 2 (WN2) [Address 00D7<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 7	Window bottom boundary control bits (WN20 to WN27)	Window bottom border position = $T_H \times (BC27 \times 16^2 + n)$ (n: setting value, $T_H$ : Hsync cycle, BC27: bit 7 of block control register 2)	Indeterminate	R	W

**Note:** Set values fit for the following condition: WN1 < WN2.

**Address 00D8<sub>16</sub>**

I/O Polarity Control Register



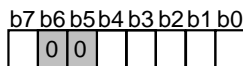
I/O polarity control register (PC) [Address 00D8<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	H <sub>SYNC</sub> input polarity switch bit (PC0)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
1	V <sub>SYNC</sub> input polarity switch bit (PC1)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
2	R, G, B output polarity switch bit (PC2)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
3	OUT1 output polarity switch bit (PC3)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
4	OUT2 output polarity switch bit (PC4)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
5	Display dot line selection bit (PC5) (See note)	0 : " " at even field " " at odd field 1 : " " at even field " " at odd field	0	R	W
6	Field determination flag (PC6)	0 : Even field 1 : Odd field	1	R	—
7	Fix this bit to "0."		0	R	W

**Note:** Refer to the corresponding figure (8.11.14).

**Address 00D9<sub>16</sub>**

Raster Color Register



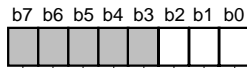
Raster color register (RC) [Address 00D9<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Raster color R control bit (RC0)	0 : No output 1 : Output	0	R	W
1	Raster color G control bit (RC1)	0 : No output 1 : Output	0	R	W
2	Raster color B control bit (RC2)	0 : No output 1 : Output	0	R	W
3	Raster color OUT1 control bit (RC3)	0 : No output 1 : Output	0	R	W
4	Raster color OUT2 control bit (RC4)	0 : No output 1 : Output	0	R	W
5, 6	Fix these bits to "0."		0	R	W
7	Port function selection bit (RC7)	0 : OSC1/XCIN, OSC2/XCOUT 1 : P26, P27	0	R	W

**Note:** Either OSD clock source or 32 kHz oscillating clock is selected by bits 5 and 6 of the OSD control register.

**Address 00DC<sub>16</sub>**

**Interrupt Input Polarity Register**

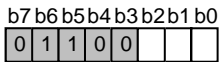


Interrupt input polarity register (RE) [Address 00DC<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	INT1 polarity switch bit (INT1)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	INT2 polarity switch bit (INT2)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	INT3 polarity switch bit (INT3)	0 : Positive polarity 1 : Negative polarity	0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

**Address 00E0<sub>16</sub>**

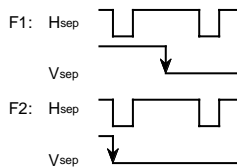
**Data Slicer Control Register 1**



Data slicer control register 1(DSC1) [Address 00E0<sub>16</sub>]

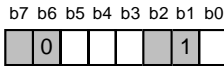
B	Name	Functions	After reset	R	W
0	Data slicer and timing signal generating circuit control bit (DSC10)	0: Stopped 1: Operating	0	R	W
1	Selection bit of data slice reference voltage generating field (DSC11)	0: F2 1: F1	0	R	W
2	Reference clock source selection bit (DSC12)	0: Video signal 1: Hsync signal	0	R	W
3, 4	Fix these bits to "0."		0	R	W
5, 6	Fix these bits to "1."		0	R	W
7	Fix this bit to "0."		0	R	W

Definition of fields 1 (F1) and 2 (F2)



**Address 00E1<sub>16</sub>**

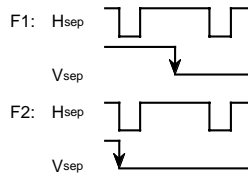
**Data Slicer Control Register 2**



Data slicer control register 2 (DSC2) [Address 00E1<sub>16</sub>]

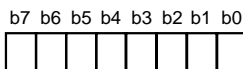
B	Name	Functions	After reset	R	W
0	Caption data latch completion flag 1 (DSC20)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R	—
1	Fix this bit to "1."		0	R	W
2	Test bit	Read-only	Indeterminate	R	—
3	Field determination flag(DSC23)	0: F2 1: F1	Indeterminate	R	—
4	Vertical synchronous signal (V <sub>sep</sub> ) generating method selection bit (DSC24)	0: Method (1) 1: Method (2)	0	R	W
5	V-pulse shape determination flag (DSC25)	0: Match 1: Mismatch	Indeterminate	R	—
6	Fix this bit to "0."		0	R	W
7	Test bit	Read-only	Indeterminate	R	—

Definition of fields 1 (F1) and 2 (F2)



**Address 00E4<sub>16</sub>**

**Clock Run-in Detect Register**

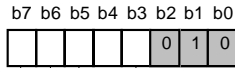


Clock run-in detect register (CRD) [Address 00E4<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 2	Test bits	Read-only	0	R	—
3 to 7	Clock run-in detection bit (CRD3 to CRD7)	Number of reference clocks to be counted in one clock run-in pulse period.	0	R	—

**Address 00E5<sub>16</sub>**

**Data Clock Position Register**

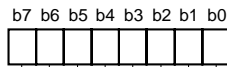


Data clock position register (DPS) [Address 00E5<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Fix this bit to "0."		1	R	W
1	Fix this bit to "1."		0	R	W
2	Fix this bit to "0."		0	R	W
3	Data clock position set bits (DPS3 to DPS7)		1	R	W
4 to 7			0		

**Address 00E6<sub>16</sub>**

**Caption Position Register**

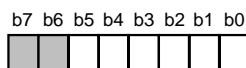


Caption Position Register (CPS) [Address 00E6<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 4	Caption position bits (CPS0 to CPS4)		0	R	W
5	Caption data latch completion flag 2 (CPS5)	0: Data is not latched yet and a clock-run-in is not determined. 1: Data is latched and a clock-run-in is determined.	Indeterminate	R	
6, 7	Slice line mode specification bits (in 1 field) (CPS6, CPS7)	Refer to the corresponding Table (Table 8.10.1).	0	R	W

**Address 00E9<sub>16</sub>**

**Sync Pulse Counter Register**

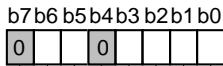


Sync pulse counter register (HC) [Address 00E9<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 4	Count value (HC0 to HC4)		0	R	
5	Count source (HC5)	0: Hsync signal 1: Composite sync signal	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are 0.		0	R	

**Address 00EB<sub>16</sub>**

Serial I/O Mode Register

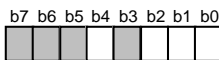


Serial I/O mode register (SM) [Address 00EB<sub>16</sub>]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: f(XIN)/4 or f(XCIN)/4 0 1: f(XIN)/16 or f(XCIN)/16 1 0: f(XIN)/32 or f(XCIN)/32 1 1: f(XIN)/64 or f(XCIN)/64	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Port function selection bit (SM3)	0: P20, P21 1: SCLK, SOUT	0	R	W
4	Fix this bit to "0."		0	R	W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W
6	Transfer clock input pin selection bit (SM6)	0: Input signal from SIN pin 1: Input signal from SOUT pin	0	R	W
7	Fix this bit to "0."		0	R	W

**Address 00EC<sub>16</sub>**

A-D Control Register 1

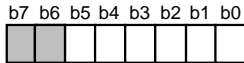


A-D control register 1 (AD1) [Address 00EC<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADC10 to ADC12)	b2 b1 b0 0 0 0: AD1 0 0 1: AD2 0 1 0: AD3 0 1 1: AD4 1 0 0: AD5 1 0 1: AD6 1 1 0: } Do not set. 1 1 1: }	0	R	W
3	This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
4	Storage bit of comparison result (ADC14)	0: Input voltage < reference voltage 1: Input voltage > reference voltage	Indeterminate	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

**Address 00ED<sub>16</sub>**

**A-D Control Register 2**

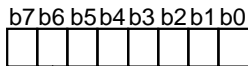


A-D control register 2 (AD2) [Address 00ED<sub>16</sub>]

B	Name	Functions	After reset	R	W
0 to 5	D-A converter set bits (ADC20 to ADC25)	b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 : 1/128Vcc 0 0 0 0 0 1 : 3/128Vcc 0 0 0 0 1 0 : 5/128Vcc ⋮ 1 1 1 1 0 1 : 123/128Vcc 1 1 1 1 1 0 : 125/128Vcc 1 1 1 1 1 1 : 127/128Vcc	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

**Address 00F4<sub>16</sub>**

**Timer Mode Register 1**



Timer mode register 1 (TM1) [Address 00F4<sub>16</sub>]

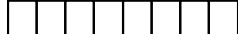
B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (TM10)	0: f(X <sub>IN</sub> )/16 or f(X <sub>CIN</sub> )/16 (See note) 1: Count source selected by bit 5 of TM1	0	R	W
1	Timer 2 count source selection bit 1 (TM11)	0: Count source selected by bit 4 of TM1 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (TM12)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (TM13)	0: Count start 1: Count stop	0	R	W
4	Timer 2 count source selection bit 2 (TM14)	0: f(X <sub>IN</sub> )/16 or f(X <sub>CIN</sub> )/16 (See note) 1: Timer 1 overflow	0	R	W
5	Timer 1 count source selection bit 2 (TM15)	0: f(X <sub>IN</sub> )/4096 or f(X <sub>CIN</sub> )/4096 (See note) 1: External clock from TIM2 pin	0	R	W
6	Timer 5 count source selection bit 2 (TM16)	0: Timer 2 overflow 1: Timer 4 overflow	0	R	W
7	Timer 6 internal count source selection bit (TM17)	0: f(X <sub>IN</sub> )/16 or f(X <sub>CIN</sub> )/16 (See note) 1: Timer 5 overflow	0	R	W

**Note:** Either f(X<sub>IN</sub>) or f(X<sub>CIN</sub>) is selected by bit 7 of the CPU mode register.

Address 00F5<sub>16</sub>

## Timer Mode Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 2 (TM2) [Address 00F5<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (TM20)	(b6 at address 00C7 <sub>16</sub> ) ↓ b0 0 0 : f(X <sub>IN</sub> )/16 or f(X <sub>CIN</sub> )/16 (See note) 0 1 : f(X <sub>CIN</sub> ) 1 0 : } 1 1 : } External clock from TIM3 pin	0	R	W
1, 4	Timer 4 count source selection bits (TM21, TM24)	b4 b1 0 0 : Timer 3 overflow signal 0 1 : f(X <sub>IN</sub> )/16 or f(X <sub>CIN</sub> )/16 (See note) 1 0 : f(X <sub>IN</sub> )/2 or f(X <sub>CIN</sub> )/2 (See note) 1 1 : f(X <sub>CIN</sub> )	0	R	W
2	Timer 3 count stop bit (TM22)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (TM23)	0: Count start 1: Count stop	0	R	W
5	Timer 5 count stop bit (TM25)	0: Count start 1: Count stop	0	R	W
6	Timer 6 count stop bit (TM26)	0: Count start 1: Count stop	0	R	W
7	Timer 5 count source selection bit 1 (TM27)	0: f(X <sub>IN</sub> )/16 or f(X <sub>CIN</sub> )/16 (See note) 1: Count source selected by bit 6 of TM1	0	R	W

**Note:** Either f(X<sub>IN</sub>) or f(X<sub>CIN</sub>) is selected by bit 7 of the CPU mode register.

Address 00F6<sub>16</sub>I<sup>2</sup>C Data Shift Register

b7 b6 b5 b4 b3 b2 b1 b0

I<sup>2</sup>C data shift register1 (S0) [Address 00F6<sub>16</sub>]

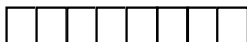
B	Name	Functions	After reset	R	W
0 to 7	D0 to D7	This is an 8-bit shift register to store receive data and write transmit data.	Indeterminate	R	W

**Note:** To write data into the I<sup>2</sup>C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.



Address 00F7<sub>16</sub>I<sup>2</sup>C Address Register

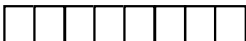
b7 b6 b5 b4 b3 b2 b1 b0

I<sup>2</sup>C address register (S0D) [Address 00F7<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Read/write bit (RBW)	<Only in 10-bit addressing (in slave) mode> The last significant bit of address data is compared. 0: Wait the first byte of slave address after START condition (read state) 1: Wait the first byte of slave address after RESTART condition (write state)	0	R	—
1 to 7	Slave address (SAD0 to SAD6)	<In both modes> The address data is compared.	0	R	W

Address 00F8<sub>16</sub>I<sup>2</sup>C Status Register

b7 b6 b5 b4 b3 b2 b1 b0

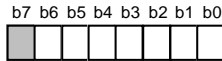
I<sup>2</sup>C status register (S1) [Address 00F8<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = "0" 1 : Last bit = "1" (See note)	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected (See note)	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address mismatch 1 : Address match (See note)	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected (See note)	0	R	—
4	I <sup>2</sup> C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	1	R	W
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave receive mode 0 1 : Slave transmit mode 1 0 : Master receive mode 1 1 : Master transmit mode	0	R	W

**Note :** These bits and flags can be read out, but cannot be written.

**Address 00F9<sub>16</sub>**

I<sup>2</sup>C Control Register



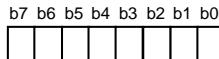
I<sup>2</sup>C control register (S1D address 00F9<sub>16</sub>)

B	Name	Functions	After reset	R : W
0 to 2	Bit counter (Number of transmit/recieve bits) (BC0 to BC2)	b2 b1 b0 0 0 0 : 8 0 0 1 : 7 0 1 0 : 6 0 1 1 : 5 1 0 0 : 4 1 0 1 : 3 1 1 0 : 2 1 1 1 : 1	0	R : W
3	I <sup>2</sup> C-BUS interface use enable bit (ESO)	0 : Disabled 1 : Enabled	0	R : W
4	Data format selection bit(ALS)	0 : Addressing mode 1 : Free data format	0	R : W
5	Addressing format selection bit (10BIT SAD)	0 : 7-bit addressing format 1 : 10-bit addressing format	0	R : W
6, 7	Connection control bits between I <sup>2</sup> C-BUS interface and ports	b7 b6 Connection port (See note) 0 0 : None 0 1 : SCL1, SDA1 1 0 : SCL2, SDA2 1 1 : SCL1, SDA1 SCL2, SDA2	0	R : W

**Note:** When using ports P11-P14 as I<sup>2</sup>C-BUS interface, the output structure changes automatically from CMOS output to N-channel open-drain output.

**Address 00FA<sub>16</sub>**

I<sup>2</sup>C Clock Control Register



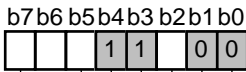
I<sup>2</sup>C clock control register (S2 : address 00FA<sub>16</sub>)

B	Name	Functions	After reset	R : W																														
0 to 4	SCL frequency control bits (CCR0 to CCR4)	<table border="1"> <thead> <tr> <th>Setup value of CCR4-CCR0</th> <th>Standard clock mode</th> <th>High speed clock mode</th> </tr> </thead> <tbody> <tr> <td>00 to 02</td> <td>Setup disabled</td> <td>Setup disabled</td> </tr> <tr> <td>03</td> <td>Setup disabled</td> <td>333</td> </tr> <tr> <td>04</td> <td>Setup disabled</td> <td>250</td> </tr> <tr> <td>05</td> <td>100</td> <td>400 (See note)</td> </tr> <tr> <td>06</td> <td>83.3</td> <td>166</td> </tr> <tr> <td>⋮</td> <td>500/CCR value</td> <td>1000/CCR value</td> </tr> <tr> <td>1D</td> <td>17.2</td> <td>34.5</td> </tr> <tr> <td>1E</td> <td>16.6</td> <td>33.3</td> </tr> <tr> <td>1F</td> <td>16.1</td> <td>32.3</td> </tr> </tbody> </table> (at φ = 4 MHz, unit : kHz)	Setup value of CCR4-CCR0	Standard clock mode	High speed clock mode	00 to 02	Setup disabled	Setup disabled	03	Setup disabled	333	04	Setup disabled	250	05	100	400 (See note)	06	83.3	166	⋮	500/CCR value	1000/CCR value	1D	17.2	34.5	1E	16.6	33.3	1F	16.1	32.3	0	R : W
Setup value of CCR4-CCR0	Standard clock mode	High speed clock mode																																
00 to 02	Setup disabled	Setup disabled																																
03	Setup disabled	333																																
04	Setup disabled	250																																
05	100	400 (See note)																																
06	83.3	166																																
⋮	500/CCR value	1000/CCR value																																
1D	17.2	34.5																																
1E	16.6	33.3																																
1F	16.1	32.3																																
5	SCL mode specification bit (FAST MODE)	0: Standard clock mode 1: High-speed clock mode	0	R : W																														
6	ACK bit (ACK BIT)	0: ACK is returned. 1: ACK is not returned.	0	R : W																														
7	ACK clock bit (ACK)	0: No ACK clock 1: ACK clock	0	R : W																														

**Note:** At 4000kHz in the high-speed clock mode, the duty is as below .  
 "0" period : "1" period = 3 : 2  
 In the other cases, the duty is as below.  
 "0" period : "1" period = 1 : 1

**Address 00FB<sub>16</sub>**

**CPU Mode Register**



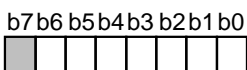
CPU mode register (CM) [Address 00FB<sub>16</sub>]

B	Name	Functions	After reset	R	W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: } Not available 1 0: } 1 1: }	0	R	W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R	W
3, 4	Fix these bits to "1."		1	R	W
5	XCOU <sub>T</sub> drivability selection bit (CM5)	0: LOW drive 1: HIGH drive	1	R	W
6	Main Clock (XIN-XOUT) stop bit (CM6)	0: Oscillating 1: Stopped	0	R	W
7	Internal system clock selection bit (CM7)	0: XIN-XOUT selected (high-speed mode) 1: XCIN-XCOU <sub>T</sub> selected (high-speed mode)	0	R	W

**Note:** This bit is set to "1" after the reset release.

**Address 00FC<sub>16</sub>**

**Interrupt Request Register 1**



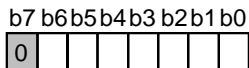
Interrupt request register 1 (IREQ1) [Address 00FC<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	OSD interrupt request bit (OSDR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	INT3 external interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

\*: "0" can be set by software, but "1" cannot be set.

Address 00FD<sub>16</sub>

Interrupt Request Register 2



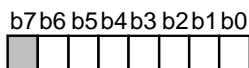
Interrupt request register 2 (IREQ2) [Address 00FD<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt request bit (INIR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
1	Data slicer interrupt request bit (DSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
2	Serial I/O interrupt request bit (S1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
3	f(X <sub>IN</sub> )/4096 interrupt request bit (CKR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
4	INT2 external interrupt request bit (IN2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
5	Multi-master I <sup>2</sup> C-BUS interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
6	Timer 5 • 6 interrupt request bit (TM56R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	*
7	Fix this bit to "0."		0	R	W

\*: "0" can be set by software, but "1" cannot be set.

Address 00FE<sub>16</sub>

Interrupt Control Register 1

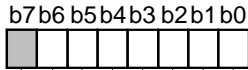


Interrupt control register 1 (ICON1) [Address 00FE<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	OSD interrupt enable bit (OSDE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	Vsync interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	INT3 external interrupt enable bit (IN3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

**Address 00FF<sub>16</sub>**

**Interrupt Control Register 2**

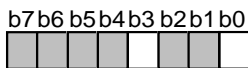


Interrupt control register 2 (ICON2) [Address 00FF<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt enable bit (IN1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Data slicer interrupt enable bit (DSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (S1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	f(XIN)/4096 interrupt enable bit (CKE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	INT2 external interrupt enable bit (IN2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	Multi-master I <sup>2</sup> C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Timer 5 • 6 interrupt enable bit (TM56E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Timer 5 • 6 interrupt switch bit (TM56C)	0 : Timer 5 1 : Timer 6	0	R	W

**Address 0208<sub>16</sub>**

**PWM Mode Register 1**

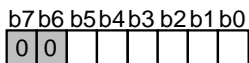


PWM mode register 1 (PM1) [Address 0208<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	PWM counts source selection bit (PM10)	0 : Count source supply 1 : Count source stop	0	R	W
1, 2	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		Indeterminate	R	—
3	PWM output polarity selection bit (PM13)	0 : Positive polarity 1 : Negative polarity	0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		Indeterminate	R	—

**Address 0209<sub>16</sub>**

PWM Mode Register 2

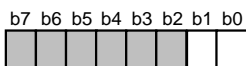


PWM mode register 2 (PM2) [Address 0209<sub>16</sub>]

B	Name	Functions	After reset	R	W
0	P0 <sub>0</sub> /PWM0 output selection bit (PM20)	0 : P0 <sub>0</sub> output 1 : PWM0 output	0	R	W
1	P0 <sub>1</sub> /PWM1 output selection bit (PM21)	0 : P0 <sub>1</sub> output 1 : PWM1 output	0	R	W
2	P0 <sub>2</sub> /PWM2 output selection bit (PM22)	0 : P0 <sub>2</sub> output 1 : PWM2 output	0	R	W
3	P0 <sub>3</sub> /PWM3 output selection bit (PM23)	0 : P0 <sub>3</sub> output 1 : PWM3 output	0	R	W
4	P0 <sub>4</sub> /PWM4 output selection bit (PM24)	0 : P0 <sub>4</sub> output 1 : PWM4 output	0	R	W
5	P0 <sub>5</sub> /PWM5 output selection bit (PW25)	0 : P0 <sub>5</sub> output 1 : PWM5 output	0	R	W
6, 7	Fix these bits to "0."		0	R	W

**Address 020E<sub>16</sub>**

ROM Correction Enable Register



ROM correction enable register (RCR) [Address 020E<sub>16</sub>]

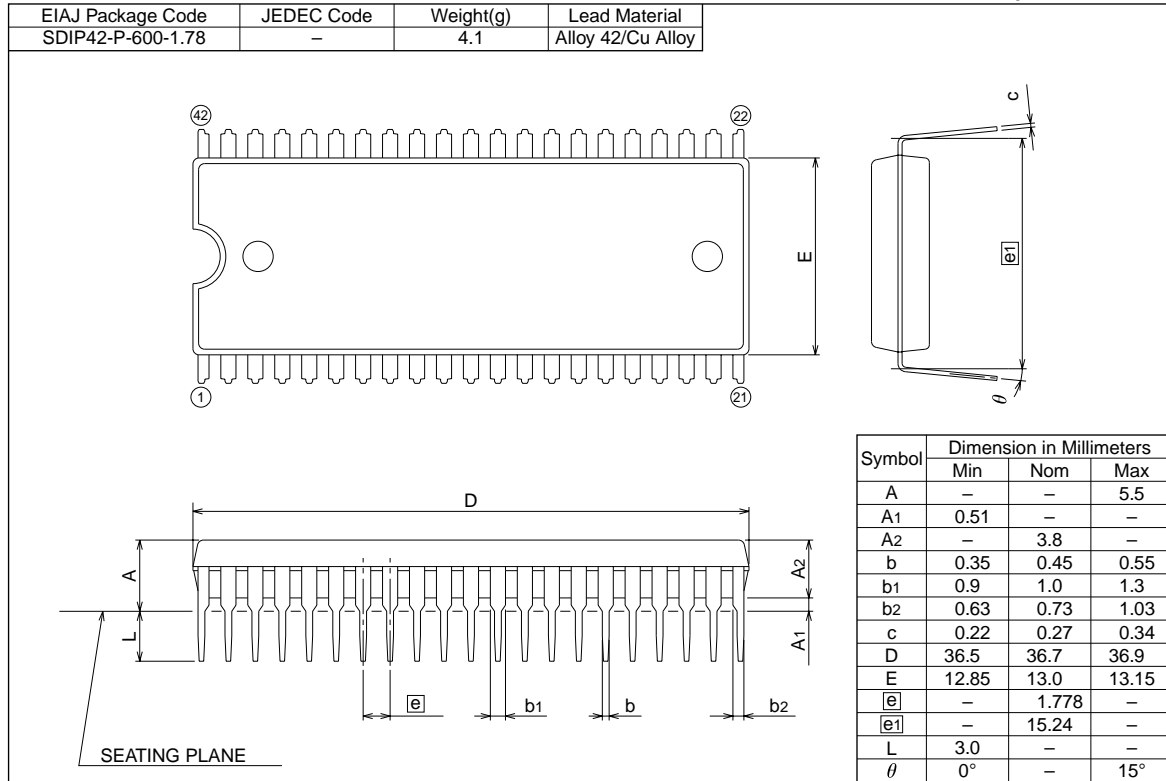
B	Name	Functions	After reset	R	W
0	Vector 1 enable bit (RC0)	0: Disabled 1: Enabled	0	R	W
1	Vector 2 enable bit (RC1)	0: Disabled 1: Enabled	0	R	W
2 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

### 19. PACKAGE OUTLINE

#### 42P4B

(MMP)

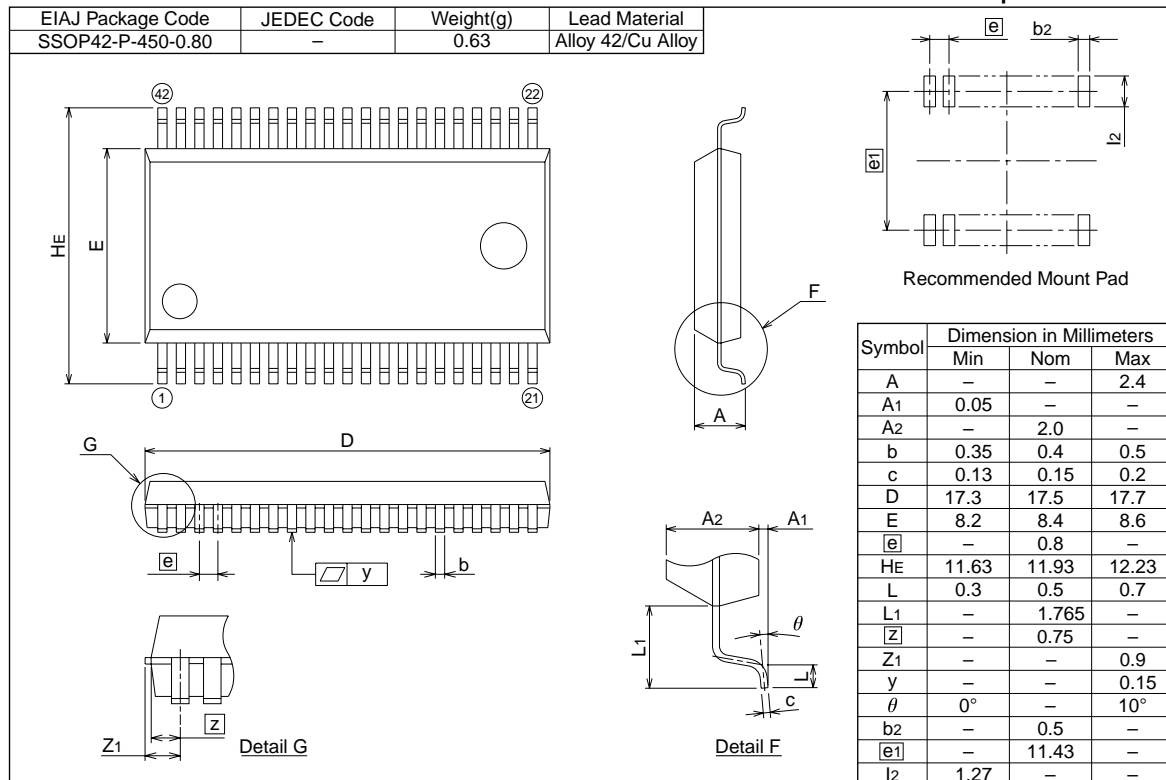
Plastic 42pin 600mil SDIP



#### 42P2R-A/E

(MMP)

Plastic 42pin 450mil SSOP







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