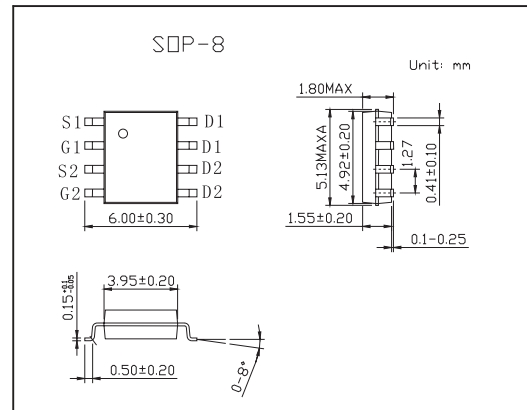
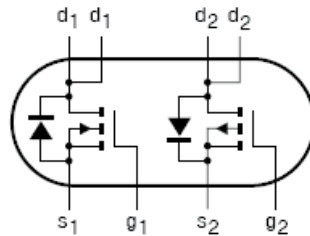


Complementary Enhancement Mode MOS Transistors KHC2300

■ Features

- High-speed switching
- No secondary breakdown.



■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain to Source Voltage	V_{DSS}	300	-300	V
Gate to Source Voltage	V_{GS}	± 20	± 20	V
Drain Current $T_s = 80^\circ\text{C}$ *1	I_D	340	-235	A
peak drain current *2	I_{DM}	14	-0.9	A
total power dissipation $T_s = 80^\circ\text{C}$; *3 $T_{amb} = 25^\circ\text{C}$; *4 $T_{amb} = 25^\circ\text{C}$; *5 $T_{amb} = 25^\circ\text{C}$; *6	P_{tot}	1.6 1.8 0.9 1.2		W
storage temperature	T_{stg}	-55 to 150		$^\circ\text{C}$
operating junction temperature	T_j	-55 to 150		$^\circ\text{C}$
thermal resistance from junction to soldering point	$R_{th\ j-s}$	43		K/W

*1. T_s is the temperature at the soldering point of the drain leads.

*2. Pulse width and duty cycle limited by maximum junction temperature.

*3. Maximum permissible dissipation per MOS transistor. (So both devices may be loaded up to 1.6 W at the same time).

*4. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 27.5 K/W.

*5. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.

*6. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on a printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.

KHC2300

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Type	Min	Typ	Max	Unit
drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0; I _D = 10 μA	N-Ch	300			V
		V _{GS} = 0; I _D = -10 μA	P-Ch	-300			V
gate-source threshold voltage	V _{GSth}	V _{GS} = V _{DS} ; I _D = 1 mA	N-Ch	0.8		2	V
		V _{GS} = V _{DS} ; I _D = -1 mA	P-Ch	-0.8		-2	V
drain-source leakage current	I _{DSS}	V _{GS} = 0; V _{DS} = 240 V	N-Ch			100	nA
		V _{GS} = 0; V _{DS} = -240 V	P-Ch			-100	nA
gate leakage current	I _{GSS}	V _{GS} = ±20 V; V _{DS} = 0	N-Ch			±100	nA
			P-Ch			±100	nA
drain-source on-state resistance	R _{Dson}	V _{GS} = 10 V; I _D = 170 mA	N-Ch			8	Ω
		V _{GS} = -10 V; I _D = -115 mA	P-Ch			17	Ω
input capacitance	C _{iss}	V _{GS} = 0; V _{DS} = 50 V; f = 1 MHz	N-Ch		57		pF
		V _{GS} = 0; V _{DS} = -50 V; f = 1 MHz	P-Ch		45		pF
output capacitance	C _{oss}	V _{GS} = 0; V _{DS} = 50 V; f = 1 MHz	N-Ch		15		pF
		V _{GS} = 0; V _{DS} = -50 V; f = 1 MHz	P-Ch		15		pF
reverse transfer capacitance	C _{rss}	V _{GS} = 0; V _{DS} = 50 V; f = 1 MHz	N-Ch		2.6		pF
		V _{GS} = 0; V _{DS} = -50 V; f = 1 MHz	P-Ch		3		pF
total gate charge	Q _G	V _{GS} = 10 V; V _{DS} = 50 V; I _D = 170 mA	N-Ch		2097		nC
		V _{GS} = 10 V; V _{DS} = -50 V; I _D = -115 mA	P-Ch		2137		nC
gate-source charge	Q _{GS}	V _{GS} = 10 V; V _{DS} = 50 V; I _D = 170 mA	N-Ch		75		nC
		V _{GS} = -10 V; V _{DS} = -50 V; I _D = -115 mA	P-Ch		68		nC
gate-drain charge	Q _{GD}	V _{GS} = 10 V; V _{DS} = 50 V; I _D = 170 mA	N-Ch		527		nC
		V _{GS} = -10 V; V _{DS} = -50 V; I _D = -115 mA	P-Ch		674		nC
turn-on time	t _{on}	V _{GS} = 0 to 10 V; V _{DD} = 50 V; I _D = 170 mA	N-Ch		2.5	10	ns
		V _{GS} = 0 to -10 V; V _{DD} = -50 V; I _D = -115 mA	P-Ch		4	10	ns
turn-off time	t _{off}	V _{GS} = 10 to 0 V; V _{DD} = 50 V; I _D = 170 mA	N-Ch		17	30	ns
		V _{GS} = -10 to 0 V; V _{DD} = -50 V; I _D = -115 mA	P-Ch		25	35	ns