

IN74AC240

Octal 3-State Inverting Buffer/Line Driver/Line Receiver
High-Speed Silicon-Gate CMOS

The IN74AC240 is identical in pinout to the LS/ALS240, HC/HCT240. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

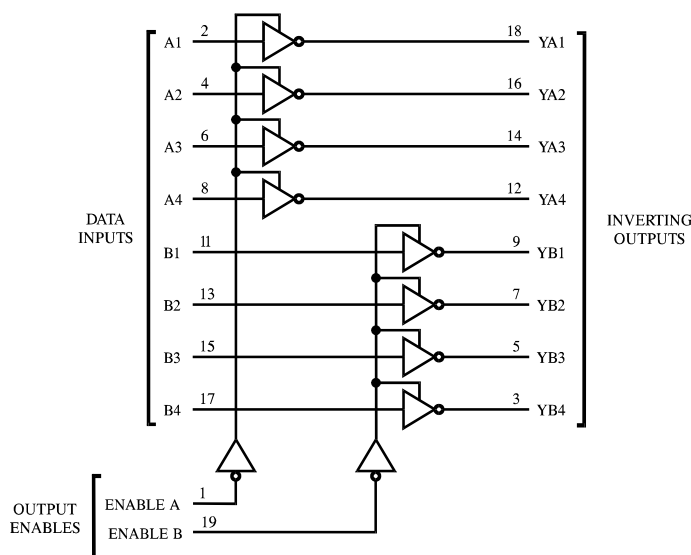
This octal inverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has inverting outputs and two active-low output enables.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A; 0.1 μ A @ 25°C
- High Noise Immunity Characteristic of CMOS Devices
- Outputs Source/Sink 24 mA

N SUFFIX PLASTIC
 DW SUFFIX SOIC

ORDERING INFORMATION
 IN74AC240N Plastic
 IN74AC240DW SOIC
 $T_A = -40^\circ$ to 85° C for all packages

LOGIC DIAGRAM



PIN 20 = V_{CC}
 PIN 10 = GND

PIN ASSIGNMENT

| | | | |
|----------|----|----|----------|
| ENABLE A | 1 | 20 | V_{CC} |
| A1 | 2 | 19 | ENABLE B |
| YB4 | 3 | 18 | YA1 |
| A2 | 4 | 17 | B4 |
| YB3 | 5 | 16 | YA2 |
| A3 | 6 | 15 | B3 |
| YB2 | 7 | 14 | YA3 |
| A4 | 8 | 13 | B2 |
| YB1 | 9 | 12 | YA4 |
| GND | 10 | 11 | B1 |

FUNCTION TABLE

| Inputs | | Outputs |
|--------------------|-----|---------|
| Enable A, Enable B | A,B | YA,YB |
| L | L | H |
| L | H | L |
| H | X | Z |

X = don't care
 Z = high impedance

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|--|------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V _{IN} | DC Input Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V |
| V _{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V |
| I _{IN} | DC Input Current, per Pin | ±20 | mA |
| I _{OUT} | DC Output Sink/Source Current, per Pin | ±50 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±50 | mA |
| P _D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit | |
|------------------------------------|---|--|-----------------|-----------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V | |
| V _{IN} , V _{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V | |
| T _J | Junction Temperature (PDIP) | | 140 | °C | |
| T _A | Operating Temperature, All Package Types | -40 | +85 | °C | |
| I _{OH} | Output Current - High | | -24 | mA | |
| I _{OL} | Output Current - Low | | 24 | mA | |
| t _r , t _f | Input Rise and Fall Time * (except Schmitt Inputs) | V _{CC} =3.0 V V _{CC} =4.5 V V _{CC} =5.5 V | 0 0 0 | 150 40 25 | ns/V |

* V_{IN} from 30% to 70% V_{CC}

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limits | | Unit |
|------------------|--|---|----------------------|----------------------|----------------------|------|
| | | | | 25 °C | -40°C to 85°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} =0.1 V | 3.0 4.5 5.5 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V |
| V _{IL} | Maximum Low - Level Input Voltage | V _{OUT} = V _{CC} -0.1 V | 3.0 4.5 5.5 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V |
| V _{OH} | Minimum High-Level Output Voltage | I _{OUT} ≤ -50 μA | 3.0 | 2.9 | 2.9 | V |
| | | | 4.5 | 4.4 | 4.4 | |
| | | | 5.5 | 5.4 | 5.4 | |
| | | *V _{IN} = V _{IL} I _{OH} =-12 mA I _{OH} =-24 mA I _{OH} =-24 mA | 3.0 4.5 5.5 | 2.56 3.86 4.86 | 2.46 3.76 4.76 | |
| V _{OL} | Maximum Low-Level Output Voltage | I _{OUT} ≤ 50 μA | 3.0 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | |
| | | | 5.5 | 0.1 | 0.1 | |
| | | *V _{IN} =V _{IH} I _{OL} =12 mA I _{OL} =24 mA I _{OL} =24 mA | 3.0 4.5 5.5 | 0.36 0.36 0.36 | 0.44 0.44 0.44 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} =V _{CC} or GND | 5.5 | ±0.1 | ±1.0 | μA |
| I _{OZ} | Maximum Three-State Leakage Current | V _{IN} (OE)= V _{IH} or V _{IL} V _{IN} =V _{CC} or GND V _{OUT} =V _{CC} or GND | 5.5 | ±0.5 | ±5.0 | μA |
| I _{OLD} | +Minimum Dynamic Output Current | V _{OLD} =1.65 V Max | 5.5 | | 75 | mA |
| I _{OHD} | +Minimum Dynamic Output Current | V _{OHD} =3.85 V Min | 5.5 | | -75 | mA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} =V _{CC} or GND | 5.5 | 8.0 | 80 | μA |

* All outputs loaded; thresholds on input associated with output under test.

+Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=3.0\text{ ns}$)

| Symbol | Parameter | V_{CC}^* V | Guaranteed Limits | | | | Unit |
|-----------|---|--------------------------------------|-------------------|-------------|---------------|-------------|------|
| | | | 25 °C | | -40°C to 85°C | | |
| | | | Min | Max | Min | Max | |
| t_{PLH} | Propagation Delay, A to YA or B to YB (Figure 1) | 3.3 5.0 | 1.5 1.5 | 8.0 6.5 | 1.0 1.0 | 9.0 7.0 | ns |
| t_{PHL} | Propagation Delay, A to YA or B to YB (Figure 1) | 3.3 5.0 | 1.5 1.5 | 8.0 6.0 | 1.0 1.0 | 8.5 6.5 | ns |
| t_{PZH} | Propagation Delay, Output Enable to YA or YB (Figure 2) | 3.3 5.0 | 1.5 1.5 | 10.5 7.0 | 1.0 1.0 | 11.0 8.0 | ns |
| t_{PZL} | Propagation Delay, Output Enable to YA or YB (Figure 2) | 3.3 5.0 | 1.5 1.5 | 10.0 8.0 | 1.0 1.0 | 11.0 8.5 | ns |
| t_{PHZ} | Propagation Delay, Output Enable to YA or YB (Figure 2) | 3.3 5.0 | 1.5 1.5 | 10.0 9.0 | 1.0 1.0 | 10.5 9.5 | ns |
| t_{PLZ} | Propagation Delay, Output Enable to YA or YB (Figure 2) | 3.3 5.0 | 1.5 1.5 | 10.5 9.0 | 1.0 1.0 | 11.5 9.5 | ns |
| C_{IN} | Maximum Input Capacitance | 5.0 | 4.5 | | 4.5 | | pF |
| C_{PD} | Power Dissipation Capacitance | Typical @25°C, $V_{CC}=5.0\text{ V}$ | | | | pF | |
| | | 45 | | | | | |

*Voltage Range 3.3 V is 3.3 V \pm 0.3 V
 Voltage Range 5.0 V is 5.0 V \pm 0.5 V

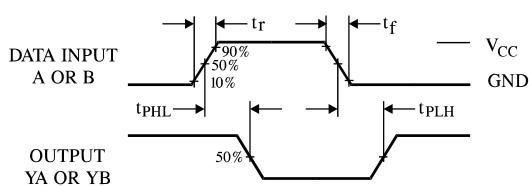


Figure 1. Switching Waveforms

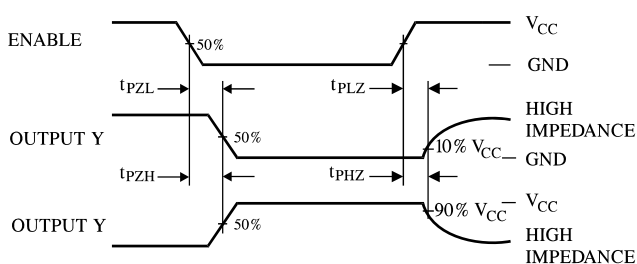
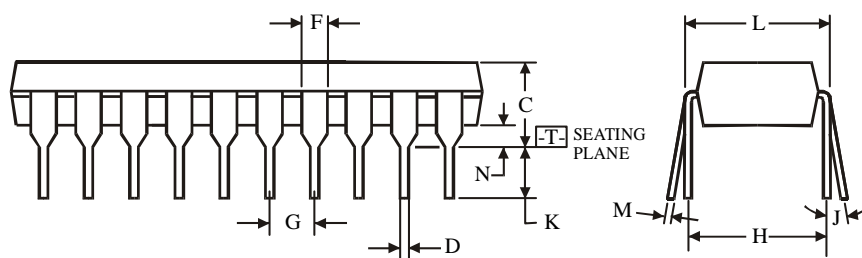
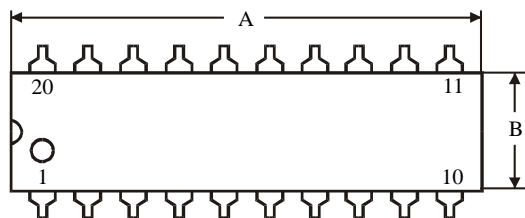
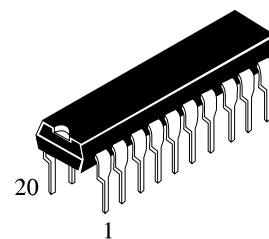


Figure 2. Switching Waveforms

N SUFFIX PLASTIC DIP
(MS - 001AD)



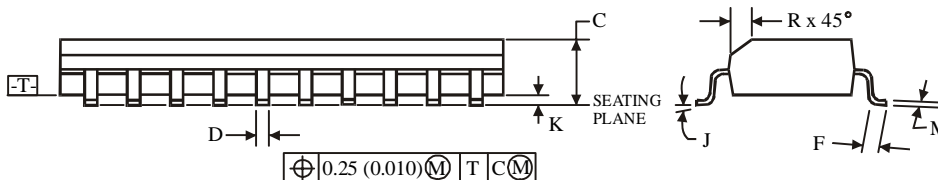
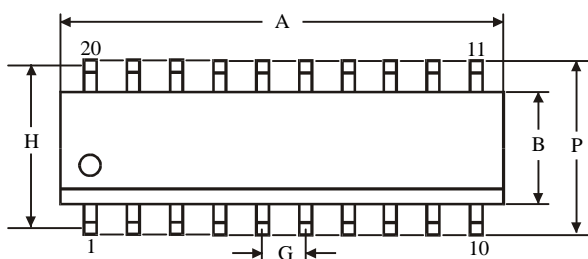
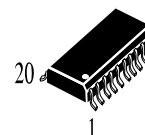
$\oplus 0.25 (0.010) \text{M} \text{T}$

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

| | Dimension, mm | |
|--------|---------------|-------|
| Symbol | MIN | MAX |
| A | 24.89 | 26.92 |
| B | 6.1 | 7.11 |
| C | | 5.33 |
| D | 0.36 | 0.56 |
| F | 1.14 | 1.78 |
| G | 2.54 | |
| H | 7.62 | |
| J | 0° | 10° |
| K | 2.92 | 3.81 |
| L | 7.62 | 8.26 |
| M | 0.2 | 0.36 |
| N | 0.38 | |

D SUFFIX SOIC
(MS - 013AC)



$\oplus 0.25 (0.010) \text{M} \text{T} \text{C} \text{M}$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side
for A; for B - 0.25 mm (0.010) per side.

| | Dimension, mm | |
|--------|---------------|-------|
| Symbol | MIN | MAX |
| A | 12.6 | 13 |
| B | 7.4 | 7.6 |
| C | 2.35 | 2.65 |
| D | 0.33 | 0.51 |
| F | 0.4 | 1.27 |
| G | 1.27 | |
| H | 9.53 | |
| J | 0° | 8° |
| K | 0.1 | 0.3 |
| M | 0.23 | 0.32 |
| P | 10 | 10.65 |
| R | 0.25 | 0.75 |