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# HD74ALVCH162270

## 12-bit to 24-bit Registered Bus Exchanger with 3-state Outputs

REJ03D0051-0300Z  
(Previous ADE-205-178A(Z))  
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Oct.02.2003

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### Description

The HD74ALVCH162270 is used in applications where data must be transferred from a narrow high speed bus to a wide lower frequency bus. The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low to high transition of the clock (CLK) input when the appropriate CLKEN inputs are low. The select ( $\overline{SEL}$ ) line selects 1B or 2B data for the A outputs. For data transfer in the A to B direction, a two stage pipeline is provided in the A to 1B path, with a single storage register in the A to 2B path. Proper control of the  $\overline{CLKENA}$  inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active low output enables ( $\overline{OEA}$ ,  $\overline{OEB}$ ). The control terminals are registered to synchronize the bus direction changes with CLK. Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include 26  $\Omega$  resistors to reduce overshoot and undershoot.

### Features

- $V_{CC} = 2.3\text{ V to }3.6\text{ V}$
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V}$  (@ $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.0\text{ V}$  (@ $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- High output current  $\pm 12\text{ mA}$  (@ $V_{CC} = 3.0\text{ V}$ )
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26  $\Omega$  series resistors, so no external resistors are required.

**Function Table**

Inputs			Outputs	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

**Output enable**

Inputs			Outputs		
CLKENA1	CLKENA2	CLK	A	1B	2B
X	H	↑	L	1B <sub>0</sub> <sup>*1,2</sup>	2B <sub>0</sub> <sup>*1</sup>
X	H	↑	H	1B <sub>0</sub> <sup>*1,2</sup>	2B <sub>0</sub> <sup>*1</sup>
L	L	↑	L	L <sup>*2</sup>	L
L	L	↑	H	H <sup>*2</sup>	H
H	L	↑	L	1B <sub>0</sub> <sup>*1</sup>	L
H	L	↑	H	1B <sub>0</sub> <sup>*1</sup>	H
H	H	X	X	1B <sub>0</sub> <sup>*1</sup>	2B <sub>0</sub> <sup>*1</sup>

**A- to-B storage ( $\overline{OEB} = L$ )**

Note: This functional table describes the case of transferring the same data for A to 1B path. For the case of transferring different data, see logic diagrams.

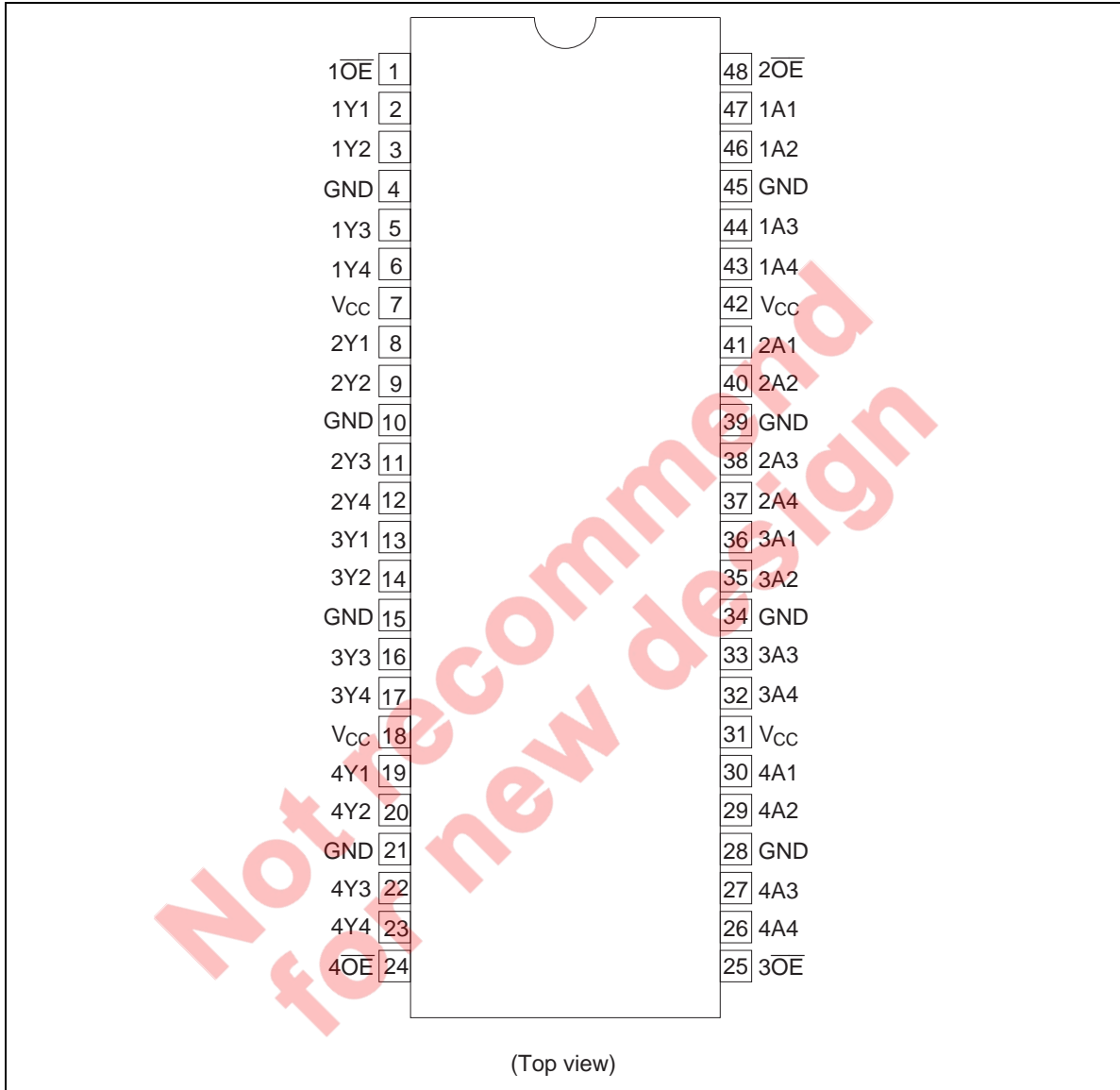
Inputs						Output A
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	
H	X	X	H	X	X	A <sub>0</sub> <sup>*1</sup>
X	H	X	L	X	X	A <sub>0</sub> <sup>*1</sup>
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

**B-to-A storage ( $\overline{OEA} = L$ )**

- H : High level
- L : Low level
- X : Immaterial
- Z : High impedance
- ↑ : Low to high transition

Notes: 1. Output level before the indicated steady state input conditions were established.  
 2. Two CLK edges are needed to propagate data.

Pin Arrangement



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 4.6	V	
Input voltage <sup>*1, 2</sup>	$V_I$	-0.5 to 4.6	V	Except I/O ports
		-0.5 to $V_{CC} + 0.5$		I/O ports
Output voltage <sup>*1, 2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$	V	
Input clamp current	$I_{IK}$	-50	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 50$	mA	$V_O = 0$ to $V_{CC}$
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	$\pm 100$	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) <sup>*3</sup>	$P_T$	1	W	TSSOP
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

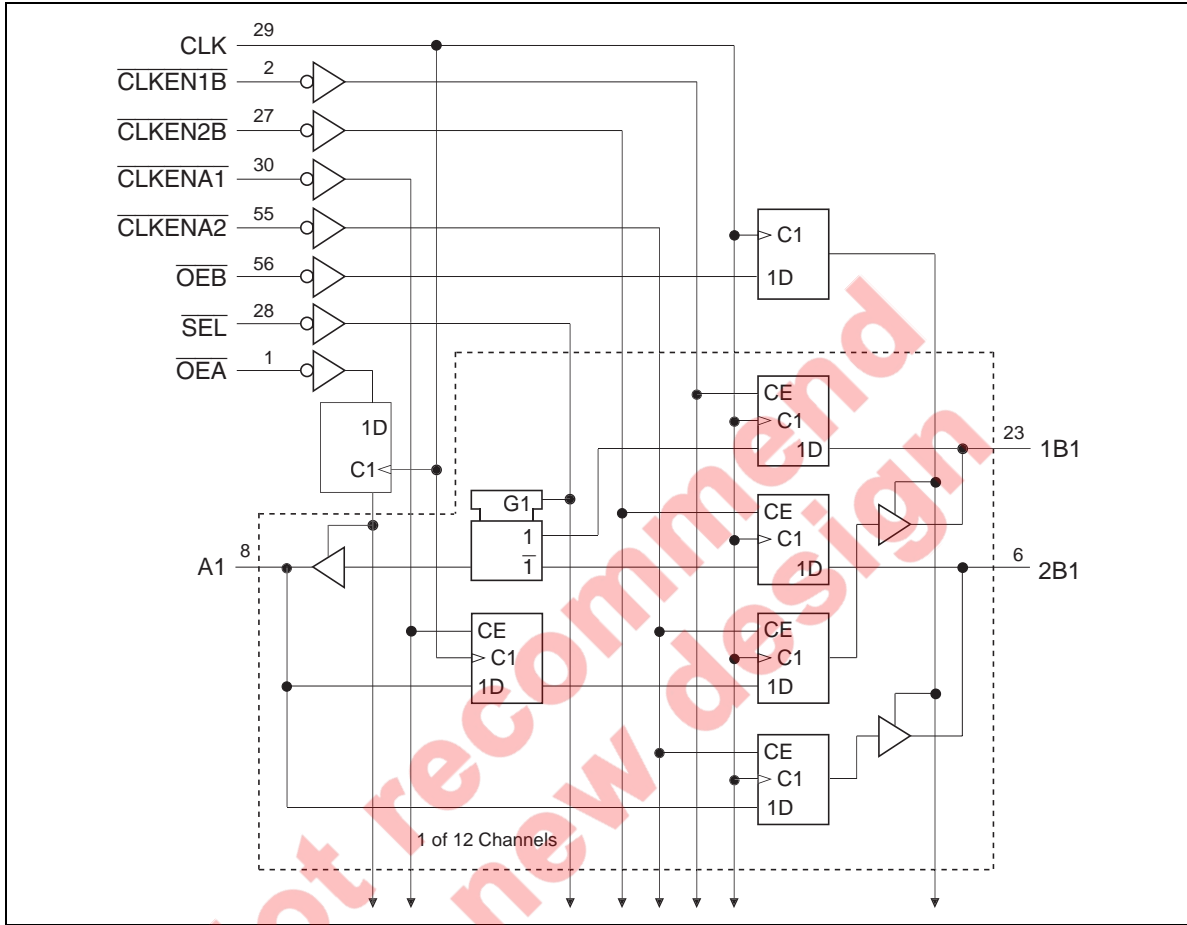
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

**Recommended Operating Conditions**

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	$V_{CC}$	2.3	3.6	V	
Input voltage	$V_I$	0	$V_{CC}$	V	
Output voltage	$V_O$	0	$V_{CC}$	V	
High level output current	$I_{OH}$	—	-6	mA	$V_{CC} = 2.3\text{ V}$
			-8		$V_{CC} = 2.7\text{ V}$
			-12		$V_{CC} = 3.0\text{ V}$
Low level output current	$I_{OL}$	—	6	mA	$V_{CC} = 2.3\text{ V}$
			8		$V_{CC} = 2.7\text{ V}$
			12		$V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	$T_a$	-40	85	$^\circ\text{C}$	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



**Electrical Characteristics**

(Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Max	Unit	Test Conditions	
Input voltage	V <sub>IH</sub>	2.3 to 2.7	1.7	—	V		
		2.7 to 3.6	2.0	—			
	V <sub>IL</sub>	2.3 to 2.7	—	0.7			
		2.7 to 3.6	—	0.8			
Output voltage	V <sub>OH</sub>	2.3 to 3.6	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA	
		2.3	1.9	—		I <sub>OH</sub> = -4 mA, V <sub>IH</sub> = 1.7 V	
		2.3	1.7	—		I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 1.7 V	
		3.0	2.4	—		I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 2.0 V	
		2.7	2.0	—		I <sub>OH</sub> = -8 mA, V <sub>IH</sub> = 2.0 V	
		3.0	2.0	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2.0 V	
		V <sub>OL</sub>	2.3 to 3.6	—		0.2	
	2.3		—	0.4	I <sub>OL</sub> = 4 mA, V <sub>IL</sub> = 0.7 V		
	2.3		—	0.55	I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V		
	3.0		—	0.55	I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.8 V		
	2.7		—	0.6	I <sub>OL</sub> = 8 mA, V <sub>IL</sub> = 0.8 V		
	3.0		—	0.8	I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V		
	Input current		I <sub>IN</sub>	3.6	—	±5	
		2.3		45	—	V <sub>IN</sub> = 0.7 V	
-45				—	V <sub>IN</sub> = 1.7 V		
3.0		75		—	V <sub>IN</sub> = 0.8 V		
		-75		—	V <sub>IN</sub> = 2.0 V		
3.6		—		±500	V <sub>IN</sub> = 0 to 3.6 V <sup>*1</sup>		
Off state output current		I <sub>OZ</sub>		3.6	—	±10	μA
Quiescent supply current	I <sub>CC</sub>	3.6	—	40	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

Note: 1. This is the bus hold maximum dynamic current required to switch the input from one state to another.

**Switching Characteristics**

(Ta = 0 to +70°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f <sub>max</sub>	2.5±0.2	135	—	—	MHz		
		2.7	135	—	—			
		3.3±0.3	135	—	—			
Propagation delay time	t <sub>PLH</sub>	2.5±0.2	2.5	—	6.9	ns	CLK	B
		2.7	—	—	6.4			
		3.3±0.3	1.7	—	5.6			
	t <sub>PHL</sub>	2.5±0.2	2.2	—	6.4	ns	CLK	A
		2.7	—	—	6.0			
		3.3±0.3	1.6	—	5.2			
		2.5±0.2	2.4	—	7.2	ns	SEL	A
		2.7	—	—	7.0			
		3.3±0.3	1.6	—	6.0			
Output enable time	t <sub>ZH</sub>	2.5±0.2	2.1	—	7.9	ns	CLK	A or B
		2.7	—	—	7.4			
		3.3±0.3	1.6	—	6.5			
Output disable time	t <sub>ZL</sub>	2.5±0.2	3.0	—	7.8	ns	CLK	A or B
		2.7	—	—	7.1			
		3.3±0.3	1.7	—	6.2			
Input capacitance	C <sub>IN</sub>	3.3	—	3.5	—	pF	Control inputs	
Output capacitance	C <sub>IN/O</sub>	3.3	—	9.0	—	pF	A or B ports	

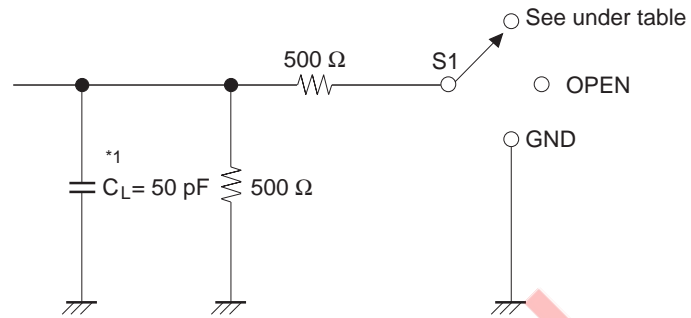
Switching Characteristics (cont.)

(Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)
Setup time	t <sub>su</sub>	2.5±0.2	4.1	—	—	ns	A data before CLK↑
		2.7	3.8	—	—		
		3.3±0.3	3.1	—	—		
		2.5±0.2	0.9	—	—		B data before CLK↑
		2.7	1.2	—	—		
		3.3±0.3	0.9	—	—		
		2.5±0.2	3.5	—	—		CLKENA1 or CLKENA2 before CLK↑
		2.7	3.2	—	—		
		3.3±0.3	2.7	—	—		
		2.5±0.2	3.4	—	—		CLKEN1B or CLKEN2B before CLK↑
		2.7	3.0	—	—		
		3.3±0.3	2.6	—	—		
		2.5±0.2	4.4	—	—		OE before CLK↑
		2.7	3.9	—	—		
		3.3±0.3	3.2	—	—		
Hold time	t <sub>h</sub>	2.5±0.2	0	—	—	ns	A data after CLK↑
		2.7	0	—	—		
		3.3±0.3	0.2	—	—		
		2.5±0.2	1.4	—	—		B data after CLK↑
		2.7	1.0	—	—		
		3.3±0.3	1.7	—	—		
		2.5±0.2	0	—	—		CLKENA1 or CLKENA2 after CLK↑
		2.7	0.1	—	—		
		3.3±0.3	0.3	—	—		
		2.5±0.2	0	—	—		CLKEN1B or CLKEN2B after CLK↑
		2.7	0	—	—		
		3.3±0.3	0.6	—	—		
		2.5±0.2	0	—	—		OE after CLK↑
		2.7	0	—	—		
		3.3±0.3	0.1	—	—		
Pulse width	t <sub>w</sub>	2.5±0.2	3.3	—	—	ns	CLK "H" or "L"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		



• Test Circuit

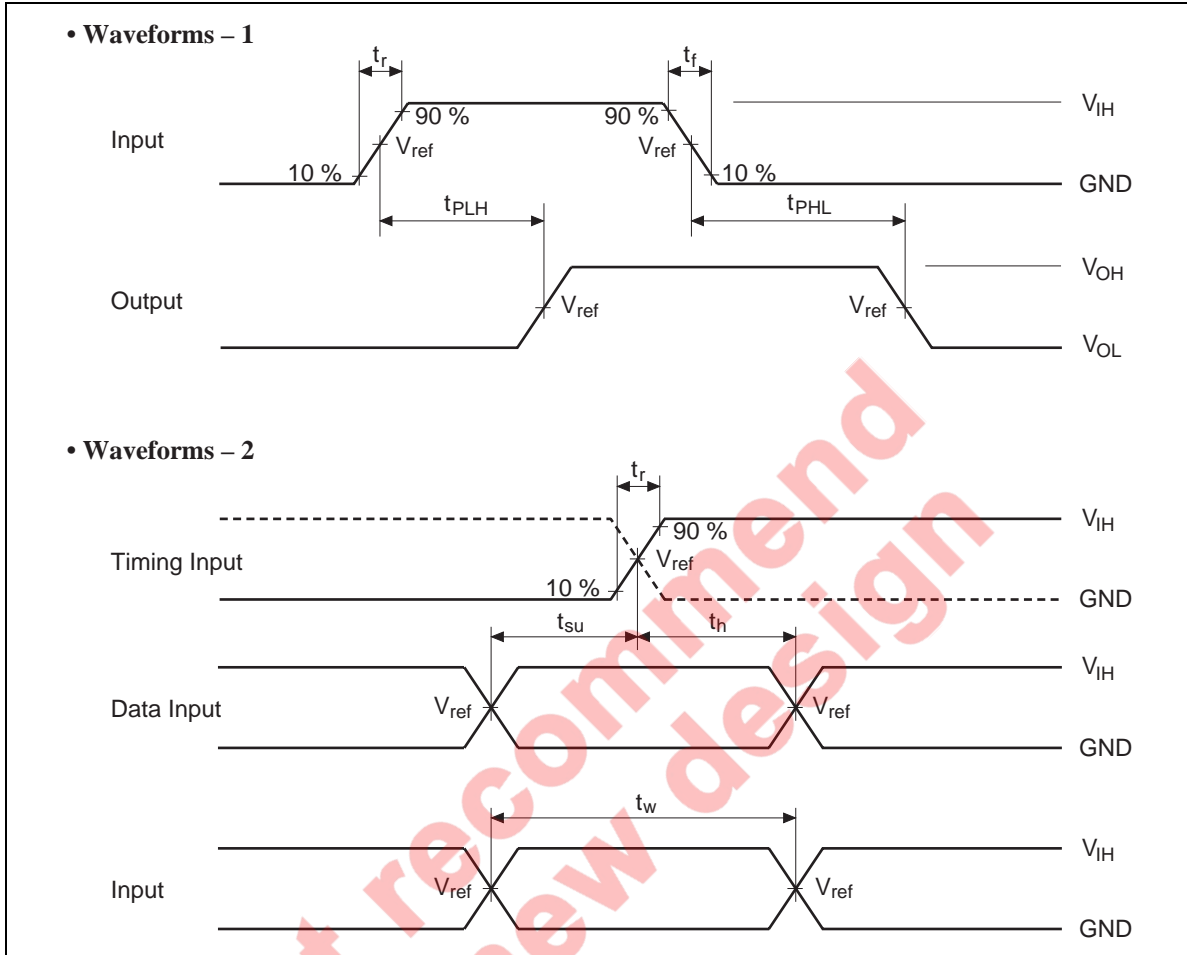


Load Circuit for Outputs

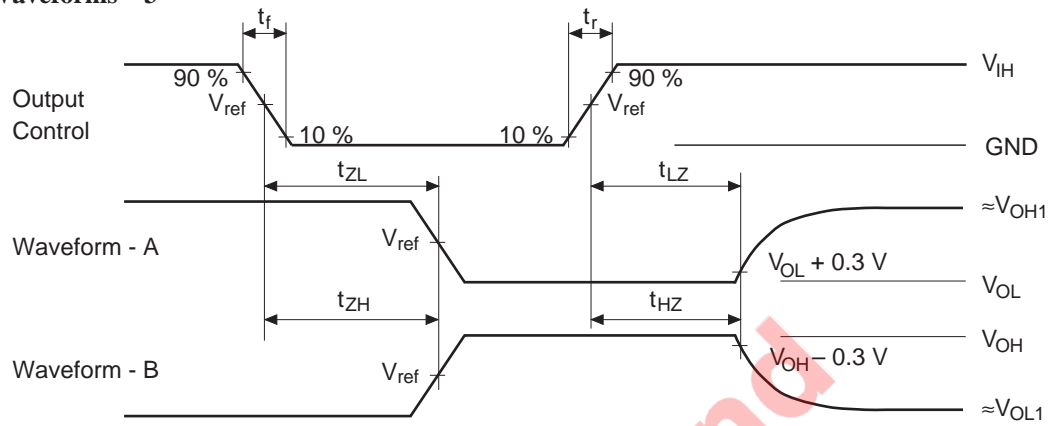
Symbol	$V_{CC}=2.5\pm 0.2\text{ V}$	$V_{CC}=2.7\text{ V},$ $3.3\pm 0.3\text{ V}$
$t_{PLH}/t_{PHL}$	OPEN	OPEN
$t_{su}/t_h/t_w$	OPEN	OPEN
$t_{ZH}/t_{HZ}$	GND	GND
$t_{ZL}/t_{LZ}$	4.6 V	6.0 V

Note: 1.  $C_L$  includes probe and jig capacitance.

Not recommended for new design



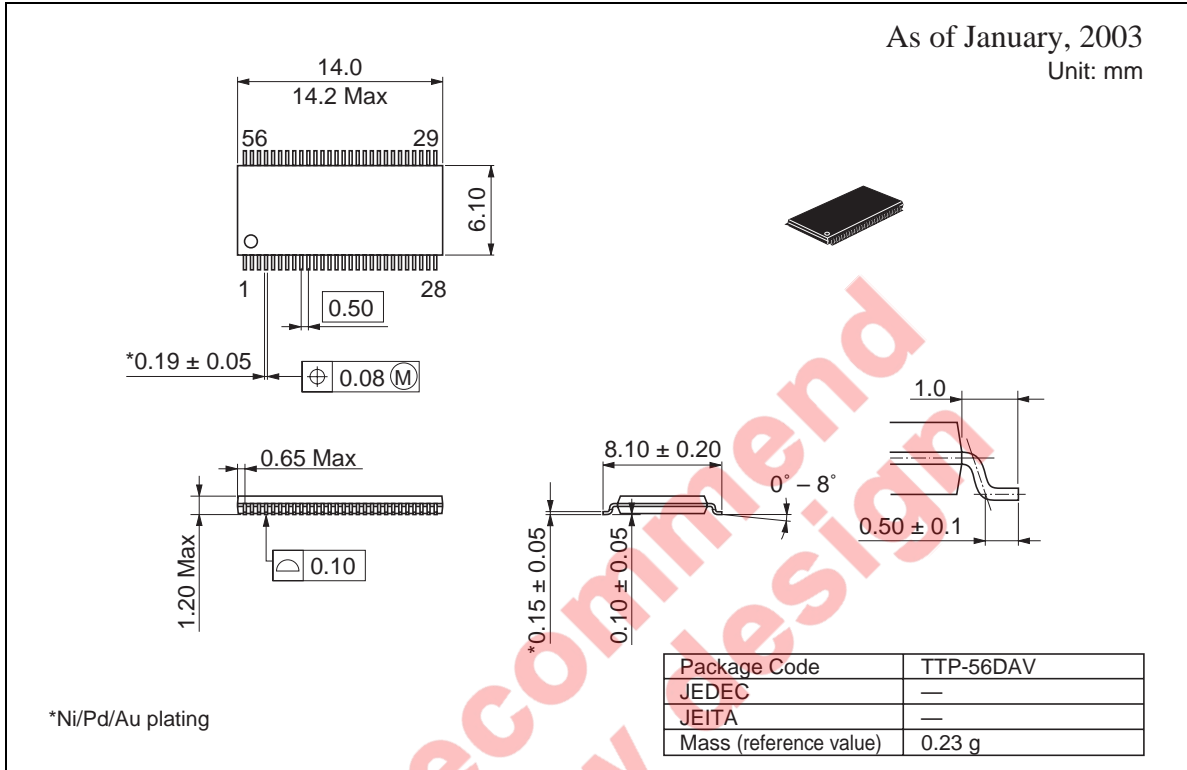
• Waveforms – 3



TEST	V <sub>CC</sub> =2.5±0.2 V	V <sub>CC</sub> =2.7 V, 3.3±0.3 V
V <sub>IH</sub>	2.3 V	2.7 V
V <sub>ref</sub>	1.2 V	1.5 V
V <sub>OH1</sub>	2.3 V	3.0 V
V <sub>OL1</sub>	GND	GND

- Notes:
1. All input pulses are supplied by generators having the following characteristics:  
PRR ≤ 10 MHz, Z<sub>o</sub> = 50 Ω, tr ≤ 2.5 ns, tf ≤ 2.5 ns.
  2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
  3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
  4. The output are measured one at a time with one transition per measurement.

Package Dimensions



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