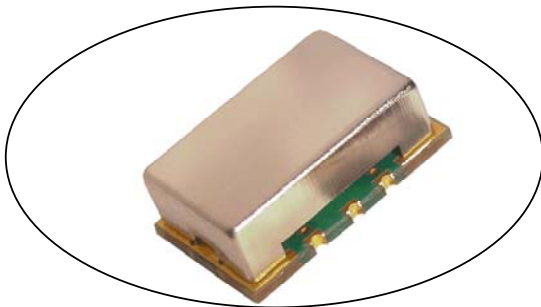


CVPD-970 Model
9X14 mm SMD, **3.3V, LVPECL**



Differential LVPECL VCXO

Frequency Range:	622.08MHz to 670MHz
Frequency Stability:	±25ppm
Temperature Range: (Option X)	0°C to 70°C -40°C to 85°C
Storage:	-55°C to 120°C
Input Voltage:	3.3V ± 0.3V
Control Voltage:	1.65V ± 1.65V
Input Current:	80mA Max
Output:	Differential LVPECL
Symmetry:	49/51% Typ, 45/55% Max
Rise/Fall Time:	0.4ns Max @ 20% to 80% Vcc
Pullability APR:	± 50ppm Min.
Linearity:	± 10% Max
Load:	Terminated to Vdd-2V into 50 ohms
Logic "1" Level:	Vcc-0.96V Min, Vcc-0.81V Max
Logic "0" Level:	Vcc-1.85V Min, Vcc-1.65V Max
Disable Time:	100ns Max
Start-up Time:	2ms Typ., 10ms Max
Modulation BW:	>10KHz @ -3dB
Sub-harmonics:	-40dBc
Period Jitter: (20,000 periods)	<5ps RMS (1-sigma) Max
Phase Jitter: 12KHz~20MHz	<1ps RMS (1-sigma) Max,
50KHz~80MHz	<1ps RMS (1-sigma) Max,
Phase Noise Typical:	
100Hz	-80 dBc/Hz
1KHz	-108 dBc/Hz
10KHz	-132 dBc/Hz
100KHz	-140 dBc/Hz
Aging:	<3ppm 1st/yr, <2ppm every year thereafter



Applications:

10 Gigabit Ethernet
OC192: Forward Error Correction
Broadband Networks
SONET/SDH/DWD
ATM
Network/switch
Telecom

Designed using FR5 PCB & HFF crystal technology to provide a very Low Noise, Low Jitter Voltage Controlled Clock Oscillator solution at a competitive price.

Specifications subject to change without notice.

TD-030607 Rev.C

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Crystek Crystals Corporation

12730 Commonwealth Drive • Fort Myers, FL 33913
239.561.3311 • 800.237.3061 • FAX: 239.561.1025 • www.crystek.com

CVPD-970 Model
9X14 mm SMD, 3.3V, LVPECL



Differential
LVPECL VCXO

Crystek Part Number Guide

CVPD-970 X-622.080

#1 #2 #3 #4

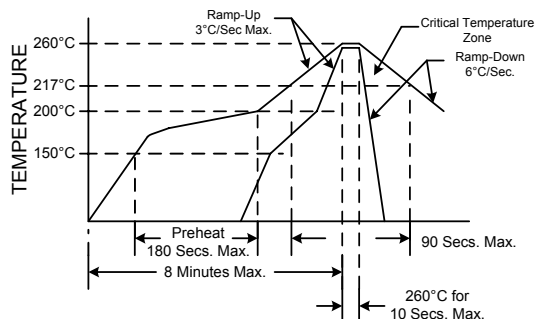
- #1 Crystek 9x14 SMD PECL VCXO
- #2 Model 970 = High Frequency 3.3V
- #3 Temp. Range: Blank = 0/70°C, X=-40/85°C
- #4 Frequency in MHz: 3 or 6 decimal places

Example:
 CVPD-970X-622.080 = 3.3V, -40/85°C, 622.080 MHz

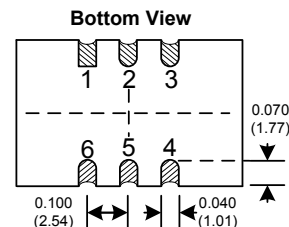
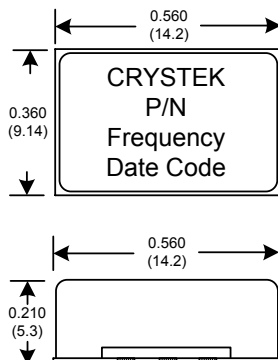
Standard Frequencies
MHz

622.0800	666.5143
625.0000	669.1281
644.5313	669.3265

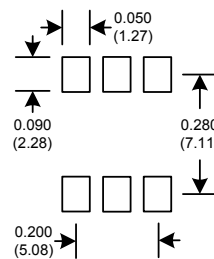
RECOMMENDED REFLOW SOLDERING PROFILE



NOTE: Reflow Profile with 240°C peak also acceptable.



SUGGESTED PAD LAYOUT



Pad	Connection
1	Volt Cont.
2	E/D
3	GND
4	OUT
5	COU
6	Vdd

Enable/Disable Function	
Pin 2	Output Pin
Open	Active
"0" level Vcc-1.620V Max	Active
"1" level Vcc-1.025V Min	Disabled
Disabled State: Pin 4 will assume a fixed level of logic "0" Pin 5 will assume a fixed level of logic "1"	

Mechanical:

- Shock:
- Solderability:
- Vibration:
- Solvent Resistance:
- Resistance to Soldering Heat:

- MIL-STD-883, Method 2002, Condition B
- MIL-STD-883, Method 2003
- MIL-STD-883, Method 2007, Condition A
- MIL-STD-202, Method 215
- MIL-STD-202, Method 210, Condition I or J

Environmental:

- Thermal Shock:
- Moisture Resistance:

- MIL-STD-883, Method 1011, Condition A
- MIL-STD-883, Method 1004

Packaging:

Tape/Reel: 100ea, 250ea, 500ea 24mm Tape

Specifications subject to change without notice.

TD-030607 Rev.C

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