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## Features

### General

- High-performance, Low-power secureAVR™ Enhanced RISC Architecture
  - 135 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low Power Idle and Power-down Modes
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to ± 4000V
- Operating Ranges: 2.7 to 5.5V
- Compliant with GSM, 3GPP and EMV 2000 Specifications
- Available in Wafers, Modules, and Industry-standard Packages

### Memory

- 128K Bytes of ROM Program Memory
- 112K Bytes of EEPROM, Including 128 OTP Bytes and 384-byte Bit-addressable Bytes
  - 1 to 128-byte Program / Erase
  - 1ms Program / 1ms Erase
  - Typically 500,000 Write/Erase Cycles at a Temperature of 25°C
  - 10 Years Data Retention
- 4K Bytes of RAM

### Peripherals

- One ISO 7816 Controller
  - Up to 625 kbps at 5 MHz
  - Compliant with T=0 and T=1 Protocols
- One I/O Port
- Programmable Internal Oscillator (Up to 20 MHz for Internal CPU Clock)
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level Interrupt Controller
- Checksum Accelerator

### Security

- Dedicated Hardware for Protection Against SPA/DPA Attacks
- Advanced Protection Against Physical Attack
- Environmental Protection Systems
- Voltage Monitor
- Frequency Monitor
- Light Protection
- Secure Memory Management/Access Protection (Supervisor Mode)

### Development Tools

- Voyager Emulation Platform (ATV4) to Support Software Development
- IAR Embedded Workbench® V4.20 Debugger or Atmel's AVR Studio® Version 4.07 or Above
- Software Libraries and Application Notes



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## Secure Microcontroller for Smart Cards

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## AT90SC 128112RU Summary

6530BS-SCIC-20Nov06



Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.

## Description

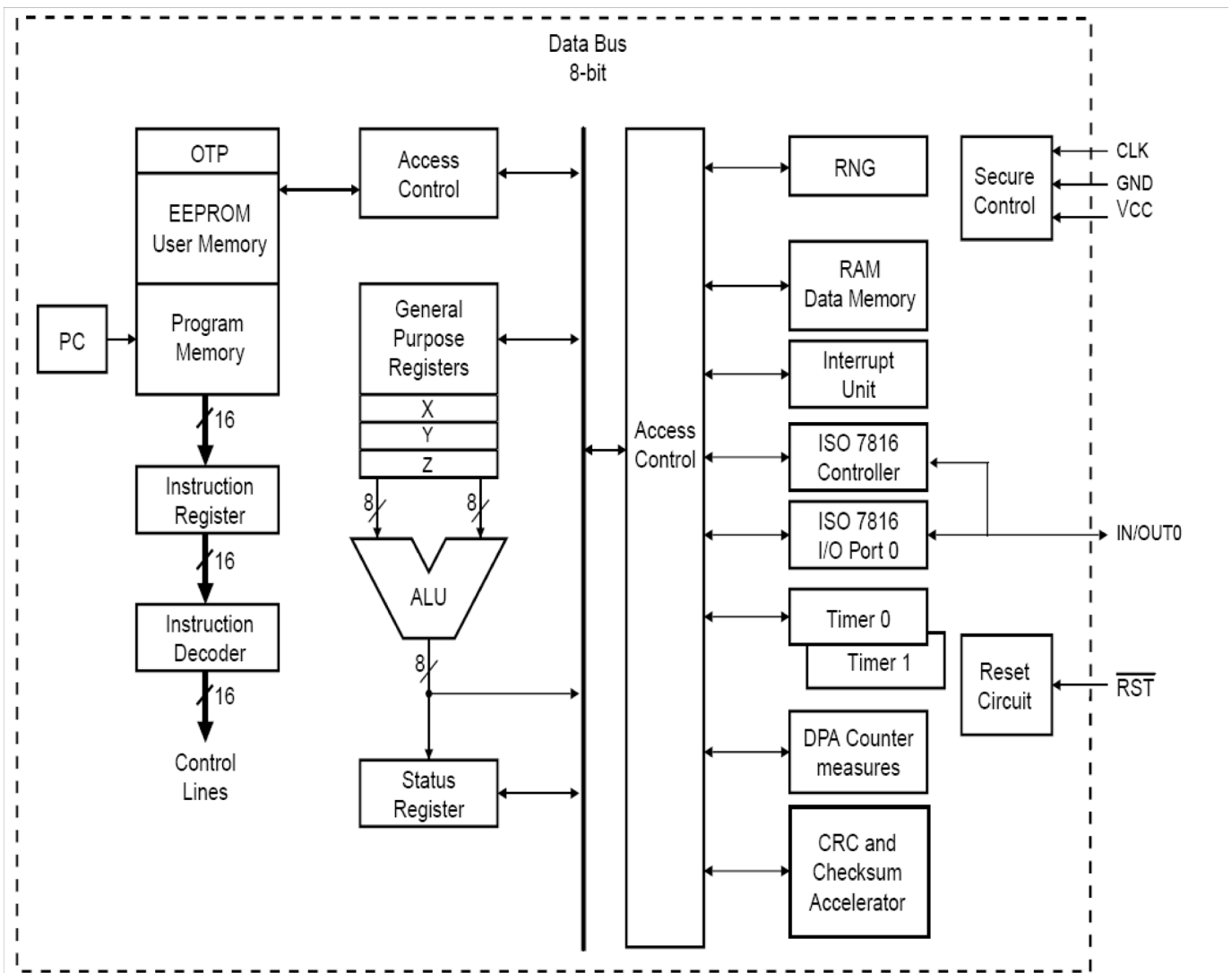
The AT90SC128112RU is a low-power, high-performance, 8/16-bit microcontroller with ROM program memory, EEPROM data memory, based on the secureAVR enhanced RISC architecture and with a contactless interface.

By executing powerful instructions in a single clock cycle, the AT90SC128112RU achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

The AT90SC128112RU uses the secureAVR architecture that allows the linear addressing of up to 8M bytes of code and up to 16M bytes of data as well as a number of new functional and security features. The AT90SC128112RU features 112K bytes of high-performance EEPROM (fast erase/write time, high endurance). The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system.

Additional security features include logical scrambling on program data and addresses, power analysis countermeasures, and memory accesses controlled by a supervisor mode.

**Figure 1.** shows a block diagram of the AT90SC128112RU





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### Literature Requests

[www.atmel.com/literature](http://www.atmel.com/literature)

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